IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR UNITED STATES PATENT

LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Inventor:

G. R. Mohan Rao – Allen, Texas

Attorneys:
Munck Wilson Mandala, LLP
P.O. Drawer 800889
Dallas, Texas 75380

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of U.S. Patent Application No. U.S. Application No. 14/950,553 filed on November 24, 2015, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM (Atty. Dkt. No. GRTD-32800), which published on June 2, 2016, as U.S. Application Publication No. 2016-0155496, now U.S. Patent No. 9,997,240 issued June 12, 2018, which is incorporated by reference in its entirety. U.S. Application No. 14/950,553 is a Continuation of U.S. Patent Application No. 14/525,411, filed October 28, 2014, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM, which published on October 1, 2015, as U.S. Publication No. 2015-0278013, now U.S. Patent No. 9,196,385, issued on November 24, 2015, (Atty. Dkt. No. GRTD-32620). Application No. 14/525,411 is a Division of U.S. Patent Application No. 13/455,267, filed April 25, 2012, published on January 24, 2013, as U.S. Publication No. 2013-0021846, now U.S. Patent No. 8,891,298, issued on November 18, 2014, entitled LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM (Atty. Dkt. No. GRTD-32619). Application No. 13/455,267 claims the benefit of U.S. Provisional Application No. 61/509,257, filed July 19, 2011, entitled LIFETIME MIXED LEVEL NAND FLASH SYSTEM (Atty. Dkt. No. GRTD-32624). Patent Nos. 9,997,240; 9,196,385; and 8,891,298 and Patent Application Publication Nos. 2015-0278013 and 2013-0021846 are hereby incorporated by reference in their entirety. This application also incorporates by reference the complete disclosure of U.S. Patent Application No. 12/256,362, filed October 22, 2008, published on April 30, 2009, as U.S. Publication No. 2009-0109787, now U.S. Patent No. 7,855,916, issued on December 21, 2010, entitled NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES (Atty. Dkt. No.

GRTD-32614). This application also incorporates by reference the complete disclosure of U.S. Patent Application No. 12/915,177, filed October 29, 2010, published on March 10, 2011, as U.S. Publication No. 2011-0060870, now U.S. Patent No. 8,194,452, issued on June 5, 2012, entitled NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES (Atty. Dkt. No. 32615).

TECHNICAL FIELD

[0002] This application relates to a system and method for providing reliable storage through the use of non-volatile memories and, more particularly, to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of single-level cell (SLC) and multi-level cell (MLC) NAND flash storage without substantially raising the cost of the NAND flash storage system. The memory in a total non-volatile memory system may contain some SRAM (static random-access memory), DRAM (dynamic RAM), RRAM (resistive RAM), PCM (phase change memory), MAGRAM (magnetic random-access memory), NAND flash, and one or more HDDs (hard disk drives) when storage of the order of several terabytes is required. The SLC non-volatile memory can be flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

BACKGROUND

[0003] Non-volatile memories provide long-term storage of data. More particularly, non-volatile memories can retain the stored data even when not powered. Magnetic (rotating) hard disk drives (HDD) dominate this storage medium due to lower cost compared to solid state disks (SSD). Optical (rotating) disks, tape drives and others have a smaller role in long-term storage systems. SSDs are preferred for their superior performance (fast access time), mechanical reliability and ruggedness, and portability. Flash memory, more specifically NAND flash, is the dominant SSD medium today.

[0004] RRAM, PCM, MAGRAM and others, wi1llikely play a larger role in the future, each of them having their own advantages and disadvantages. They may ultimately replace flash memories, initially for use as a "write buffer" and later to replace "SLC flash" and "MLC flash." MLC NAND flash is a flash memory technology using multiple levels per cell to allow more bits to be stored using the same number of transistors. In SLC NAND flash technology, each cell can exist in one of two states, storing one bit of information per cell. Most MLC NAND flash memory has four possible states per cell, so it can store two bits of information per cell.

[0005] These semiconductor technology driven "flash alternatives," i.e., RRAM, PCM, MAGRAM and others, have several advantages over any (SLC or MLC) flash because they: 1) allow data to be written over existing data (without prior erase of existing data), 2) allow for an erase of individual bytes or pages (instead of having to erase an entire block), and 3) possess superior endurance (1,000,000 write-erase cycles compared to typical 100,000 cycles for SLC flash and less than 10,000 cycles for MLC flash).

[0006] HDDs have several platters. Each platter contains 250-5,000 tracks (concentric circles). Each track contains 64 to 256 sectors. Each sector contains 512 bytes of data and has a unique "physical (memory) address." A plurality of sectors is typically combined to form a "logical block" having a unique "logical address." This logical address is the address at which the logical block of physical sectors appears to reside from the perspective of an executing application program. The size of each logical block and its logical address (and/or address ranges/boundaries) is optimized for the particular operating system (OS) and software

applications executed by the host processor. A computer OS organizes data as "files." Each file may be located (stored) in either a single logical block or a plurality of logical blocks, and therefore, the location of files typically traverses the boundaries of individual (physical) sectors. Sometimes, a plurality of files has to be combined and/ or modified, which poses an enormous challenge for the memory controller device of a non-volatile memory system.

[0007] SSDs are slowly encroaching on the HDD space and the vast majority of NAND flash in enterprise servers utilizes a SLC architecture, which further comprises a NAND flash controller and a flash translation layer (FTL). NAND flash devices are generally fragmented into a number of identically sized blocks, each of which is further segmented into some number of pages. It should be noted that asymmetrical block sizes, as well as page sizes, are also acceptable within a device or a module containing devices. For example, a block may comprise 32 to 64 pages, each of which incorporates 2 - 4 Kbit of memory. In addition, the process of writing data to a NAND flash memory device is complicated by the fact that, during normal operation of, for example, single-level storage (SLC) , erased bits (usually all bits in a block with the value of '1') can only be changed to the opposite state (usually '0') once before the entire block must be erased. Blocks can only be erased in their entirety, and, when erased, are usually written to '1' bits. However, if an erased block is already there, and if the addresses (block, page, etc.) are allowed, data can be written immediately; if not, a block has to be erased before it can be written to.

[0008] FTL is the driver that works in conjunction with an existing operating system (or, in some embedded applications, as the operating system) to make linear flash memory appear to the system like a disk drive, i.e., it emulates a HDD. This is achieved by creating "virtual" small blocks of data, or sectors, out of flash's large erase blocks and managing data on the flash so that it appears to be "write in place" when in fact it is being stored in different locations in the flash. FTL further manages the flash so that there are clean/ erased places to store data.

[0009] Given the limited number of writes that individual blocks within flash devices can tolerate, wear leveling algorithms are used within the flash devices (as firmware commonly known as FTL or managed by a controller) to attempt to ensure that "hot" blocks, i.e., blocks that are frequently written, are not rendered unusable much faster than other blocks. This task is

usually performed within a flash translation layer. In most cases, the controller maintains a lookup table to translate the memory array physical block address (PBA) to the logical block address (LBA) used by the host system. The controller's wear-leveling algorithm determines which physical block to use each time data is programmed, eliminating the relevance of the physical location of data and enabling data to be stored anywhere within the memory array and thus prolonging the service life of the flash memory. Depending on the wear-leveling method used, the controller typically either writes to the available erased block with the lowest erase count (dynamic wear leveling); or it selects an available target block with the lowest overall erase count, erases the block if necessary, writes new data to the block, and ensures that blocks of static data are moved when their block erase count is below a certain threshold (static wear leveling).

[0010] MLC NAND flash SSDs are slowly replacing and/ or coexisting with SLC NAND flash in newer SSD systems. MLC allows a single cell to store multiple bits, and accordingly, to assume more than two values; i.e., '0' or '1'. Most MLC NAND flash architectures allow up to four (4) values per cell; i.e., '00', '01', '10', or '11'. Generally, MLC NAND flash enjoys greater density than SLC NAND flash, at the cost of a decrease in access speed and lifetime (endurance). It should be noted, however, that even SLC NAND flash has a considerably lower lifetime (endurance) than rotating magnetic media (e.g., HDDs), being able to withstand only between 50,000 and 100,000 writes, and MLC NAND flash has a much lower lifetime (endurance) than SLC NAND flash, being able to withstand only between 3,000 and 10,000 writes. As is well known in the art, any "write" or "program" to a block in NAND flash (floating gate) requires an "erase" (of a block) before "write."

[0011] Despite its limitations, there are a number of applications that lend themselves to the use of MLC flash. Generally, MLC flash is used in applications where data is read many times (but written few times) and physical size is an issue. For example, flash memory cards for use in digital cameras would be a good application of MLC flash, as MLC can provide higher density memory at lower cost than SLC memory.

[0012] When a non-volatile storage system combines HDD, SLC and MLC (setting aside volatile memory for buffering, caching etc) in a single (hybrid) system, new improvements and

solutions are required to manage the methods of writing data optimally for improved life time (endurance) of flash memory. Accordingly, various embodiments of a NAND flash storage system that provides long lifetime (endurance) storage at low cost are described herein.

[0013] The following description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art. Thus, the present disclosure is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features described herein.

SUMMARY

[0014] According to one embodiment of the present disclosure, there is provided a system for storing data which comprises at least one MLC nonvolatile memory module (hereinafter referred to as "MLC module") and at least one SLC non-volatile memory module (hereinafter referred to as "SLC module"), each module comprises a plurality of individually erasable blocks. The data storage system according to one embodiment of the present disclosure further comprises a controller for controlling both the at least one MLC module and the at least one SLC module. In particular, the controller maintains an address map comprising a list of individual logical address ranges each of which maps to a similar range of physical addresses within either the at least one MLC module or the at least one SLC module. After each write to (flash) memory, the controller conducts a data integrity check to ensure that the data was written correctly. When the data was not written correctly, the controller modifies the table so that the range of addresses on which the write failed is remapped to the next available range of physical addresses within the at least one SLC module. The SLC module can be (NAND) flash, PCM, RRAM, MAGRAM or any other solid-state non-volatile memory as long as it has endurance that is superior to that of MLC flash, and it provides for data access speeds that are faster than that of MLC flash or rotating storage media (e.g., HDDs).

[0015] According to another embodiment of the present disclosure, there is provided a system for storing data which comprises a controller that is further adapted to determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and wherein the controller segregates those blocks that receive frequent writes into the at least one SLC non-volatile memory module and those blocks that receive infrequent writes into the at least one MLC nonvolatile module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The present disclosure will be more fully understood by reference to the following detailed description of one or more preferred embodiments when read in conjunction with the accompanying drawings, in which like reference characters refer to like parts throughout the views and in which:

[0017] FIG. 1 is a block diagram of a computer system incorporating one embodiment of the present disclosure;

[0018] FIGS. 2A and 2B are drawings depicting a translation table/address map in accordance with one embodiment of the present disclosure;

[0019] FIGS. 3A and 3B are a flow chart illustrating an exemplary method for use in implementing one embodiment of the present disclosure; and

[0020] FIG. 4 is a block diagram depicting one embodiment of the present disclosure for implementation within a NAND flash module.

DETAILED DESCRIPTION

[0021] The present disclosure is directed to the reliable storage of data in read and write memory, and, in particular, to the reliable storage of data in non-volatile memory, such as, for example, NAND flash. Generally, and in particular regard to NAND flash memory, two separate banks of NAND flash are maintained by a controller. One bank contains economical MLC NAND flash, while a second bank contains high endurance SLC NAND flash. The controller conducts a data integrity test after every write. If a particular address range fails a data integrity test, the address range is remapped from MLC NAND flash to SLC NAND flash. As the SLC NAND flash is used to boost the lifetime (endurance) of the storage system, it can be considerably lesser in amount than the MLC NAND flash. For example, a system may set SLC NAND flash equal to 12.5% or 25% of MLC NAND flash (total non-volatile memory storage space=MLC+SLC).

[0022] Turning to the Figures and to FIG. 1 in particular, a computer system 10 depicting one embodiment of the present disclosure is shown. A processor 12 is coupled to a device controller 14, such as a chipset, using a data link well known in the art, such as a parallel bus or packet-based link. The device controller 14 provides interface functions to the processor 12. In some computer systems, the device controller 14 may be an integral part of the (host) processor 12. The device controller 14 provides a number of input/output ports 16 and 18, such as, for example, serial ports (e.g., USB ports and Firewire ports) and network ports (e.g., Ethernet ports and 802.11 "Wi-Fi" ports). The device controller 14 may also control a bank of, for example, DRAM 20. In addition, the device controller 14 controls access to one or more disks 24, such as, for example, a rotating magnetic disk, or an optical disk, as well as two or more types of NAND flash memory. One type of NAND flash memory is a MLC NAND flash memory module 26. Another type of NAND flash memory is a SLC NAND flash memory module 28.

[0023] The device controller 14 maintains a translation table/address map which may include address translations for all devices in the computer system. Nonetheless, the discussion in the present disclosure will be limited only to NAND flash memory modules. In particular, the device controller 14 maintains a translation table that maps logical computer system addresses to physical addresses in each one of the MLC- and SLC-NAND flash memory modules 26 and 28,

respectively. As MLC flash memory is less expensive than SLC flash memory, on a cost per bit basis, the translation table will initially map all logical NAND flash addresses to the MLC NAND flash memory module 26. The address ranges within the translation table will assume some minimum quantum, such as, for example, one block, although a smaller size, such as one page could be used, if the NAND flash has the capability of erasing the smaller size quantum.

[0024] A "read-modify-write" scheme is used to write data to the NAND flash. Data to be written to NAND flash is maintained in DRAM 20. After each write to an address within a particular address range, the device controller 14 will—as time permits—perform a read on the address range to ensure the integrity of the written data. If a data integrity test fails, the address range is remapped from the MLC NAND flash memory module 26 to the next available address range in the SLC NAND flash memory module 28.

[0025] FIGS. 2A and 2B illustrate one embodiment of a translation table/address map of the present disclosure. In Figure. 2A, a list of logical address ranges (R0-RN) is translated to physical address ranges. As illustrated, all of the logical address ranges are translated to blocks on the MLC NAND flash memory module 26. However, through the application of a data integrity verification check (explained in more detail below) it is determined that, for example, address range R2 corresponds to failed quanta of data stored in block 2 of the MLC NAND flash memory module 26. FIG. 2B shows the quanta of data which failed the data integrity verification check (see FIG. 2A) remapped to the next available range of physical addresses within the SLC NAND flash memory module 28, in this example, SLC/block 0.

[0026] FIGS. 3A and 3B are a flow chart illustrating a method for utilizing a NAND flash memory system incorporating one embodiment of the present disclosure. The method begins in a step 100, when a command to write a quantum of data stored in DRAM to a particular location in NAND flash memory is received. In step 102, the quantum of data is read from DRAM into memory within the device controller (which acts as the memory controller). In step 104, both the logical address range and the NAND flash physical address range to which the quantum of data is to be written, is read into memory of the device controller. In step 106, the quantum of data to be written is combined with the contents of the NAND flash memory. In step 108, the NAND flash physical address range to be written is erased. In step 110, the combined data is written to

the appropriate NAND flash physical address range. In step 112 the NAND flash physical address range that was written in step 110 is read into device controller memory.

[0027] The flowchart continues in FIG. 3B. In step 114 the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical address range and the quantum of data to be written. In step 116, if the retained data matches the newly stored data in the NAND flash memory, the write was a success, and the method exits in step 118. However, if the retained data does not match the newly stored data in the NAND flash memory, the method executes step 120, which identifies the next quantum of available SLC NAND flash memory addresses. In step 122, a check is made to determine if additional SLC NAND flash memory is available, and, if not, the NAND flash memory system is marked as failed, prompting a system alert step 124. However, if additional SLC NAND flash memory is available, the failed NAND flash physical address range is remapped to the next available quantum of SLC NAND flash memory in step 126. Execution then returns to step 110, where the write is repeated.

[0028] Another application of one embodiment of the present disclosure, not depicted in any of the drawings, is to allocate "hot" blocks; i.e., those blocks that receive frequent writes, into the SLC NAND flash memory module 28, while allocating "cold" blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26. This could be accomplished within the device controller 14 described above, which could simply maintain a count of those blocks that are accessed (written to) most frequently, and, on a periodic basis, such as, for example, every 1000 writes, or every 10,000 writes, transfer the contents of those blocks into the SLC NAND flash memory module 28.

[0029] FIG. 4 depicts another embodiment of the present disclosure. The embodiment is entirely resident within a NAND flash module 50. In particular, a standard NAND flash interface 52 is managed by flash translation layer (FTL) logic 54. The flash translation layer (FTL) 54 manages two NAND flash memory banks 56 and 58, whereby memory bank 56 comprises a plurality of MLC NAND flash memory modules 60a and a plurality of SLC NAND flash memory modules 62a. Memory bank 58 comprises a plurality of MLC NAND flash memory modules 60b and a plurality of SLC NAND flash memory modules 62b.

[0030] This embodiment of the present disclosure could function similarly to the system level embodiment discussed earlier with reference to FIGS 1-3B, but the control functions, such as maintenance of the translation table/address map (FIGS. 2A and 2B), could be conducted within the flash translation layer (FTL) 54 instead of in a device controller 14.

[0031] Embodiments of the present disclosure relate to a system and method of increasing the reliability and lifetime of a NAND flash storage system, module, or chip through the use of a combination of multi-level cell (MLC) and single-level cell (SLC) NAND flash storage. The above description is presented to enable one of ordinary skill in the art to make and use the disclosure and is provided in the context of a patent application and its requirements. While this disclosure contains descriptions with reference to certain illustrative aspects, it will be understood that these descriptions shall not be construed in a limiting sense. Rather, various changes and modifications can be made to the illustrative embodiments without departing from the true spirit, central characteristics and scope of the disclosure, including those combinations of features that are individually disclosed or claimed herein. Furthermore, it will be appreciated that any such changes and modifications will be recognized by those skilled in the art as an equivalent to one or more elements of the following claims, and shall be covered by such claims to the fullest extent permitted by law.

WHAT IS CLAIMED IS:

1. A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements; and

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories.

2. The system of Claim 1, wherein the memory elements are a module, standalone device, or multi-chip package.

3. The system of Claim 1, wherein at least one of the volatile or nonvolatile memories are embedded in the at least one controller.

4. The system of Claim 1, wherein the nonvolatile memory is flash memory.

5. The system of Claim 1, wherein the nonvolatile memory is phase-change memory.

6. The system of Claim 1, wherein the nonvolatile memory is magnetic random access memory.

7. The system of Claim 1, wherein the volatile memory is dynamic random access memory.

8. The system of Claim 1, wherein the volatile memory is static random access memory.

9. The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

ABSTRACT

A flash controller for managing at least one MLC non-volatile memory module and at least one SLC non-volatile memory module. The flash controller is adapted to determine if a range of addresses listed by an entry and mapped to said at least one MLC non-volatile memory module fails a data integrity test. In the event of such a failure, the controller remaps said entry to an equivalent range of addresses of said at least one SLC non-volatile memory module. The flash controller is further adapted to determine which of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently and allocating those blocks that receive frequent writes to the SLC non-volatile memory module and those blocks that receive infrequent writes to the MLC non-volatile memory module.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/006,299	06/12/2018	G.R. MOHAN RAO	GRTD60-34138	6732

25883 7590 01/24/2019

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

EXAMINER	
REIDLINGER, RONALD LANCE	

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
01/24/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPdocketing@munckwilson.com
admin@dalpat.com
eofficeaction@appcoll.com

Office Action Summary	Application No. 16/006,299	Applicant(s) RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 12 June 2018.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-9 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-9 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 12 June 2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Claims 1-9 are pending.

Claim 1 is independent.

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4 and 7-9 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. (U.S. Patent Application Publication No. 2010/0172179, on record in parent application 13/455,267) in view of Goodson et al. ("Design Tradeoffs in a Flash Translation Layer," on record in parent application 13/455,267).

Regarding claim 1, Gorobets et al. teach,

A system for storing data (e.g. Fig. 20) comprising:

memory space containing volatile memory space (Fig. 15 Cache (RAM)) and nonvolatile memory space (Fig. 15, MLC Memory, including Main Memory and Binary Cache), wherein the nonvolatile memory space includes both multilevel cell (MLC) (Figs. 15, 20 Main Memory of MLC Memory) space (Figs. 15, 20 Main Memory of MLC Memory) and single level cell (SLC) space (Figs. 15, 20 Binary Cache of MLC Memory);

at least one controller (Fig. 8 Memory Manager No. 300; see also Fig. 15 Controller) to operate memory elements and associated memory space (Flash Memory No. 200);

at least one MLC nonvolatile memory element (Fig. 20 Main Portion MLC No. 2003; this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one SLC nonvolatile memory element (Fig. 20 Binary Portion No. 2001; again, this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one random access volatile memory element (see Fig. 15 Cache (RAM));

wherein the at least one controller (Fig. 8 Memory Manager No. 300; see also Fig. 15 Controller) of both maintain an address table in one or more of the memory elements (see ¶ [0096]); and

wherein the address table maps logical and physical addresses (memory manager in the controller maps logical addresses to physical addresses, see ¶ [0096]) adaptable to the system, wherein

the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories (see ¶ [0152-154], explaining the use of spare block pool management to increase lifetime of the memory device; mapping would be necessary to remap any logical address pointing to a retired block so that it points to a replacement block, or new physical address).

Gorobets et al. explain address translation layers for flash memory, but do not describe the specific term "an FTL flash translation layer."

Nevertheless, Goodson et al. document the purpose and motivation for using FTL for a flash memory device (see Title, "Design Tradeoffs in a Flash Translation Layer," and §§ 1-2, which explain the purpose of flash translation layers).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Goodson et al. to the teachings of Gorobets et al. such that an FTL (as explained by Goodson et al.) is used with the flash devide taught by Gorobets et al. for the purpose of allowing the files system of the flash memory device to maintain the block interface of the disk without sacrificing the tighter integration and control over how the flash is managed and because it hides the complexity of the flash by providing a logical block interface for the flash device.

Regarding claims 2 and 9, Gorobets et al. explain that flash memory is most commonly provided in the form of a memory card (i.e., module or standalone unit as claimed) or a flash drive (i.e., module or standalone unit or hard drive, as claimed) (see background ¶ [0015]). Because Gorobets et al. embodiments involve flash memory, the provisions of being a module, standalone device or hard drive, as claimed, are met.

Regarding claim 3, Gorobets et al. teach at least one of the volatile or nonvolatile memories are embedded in the at least one controller (see Fig. 15 volatile Cache (RAM) 102 is embedded within Controller).

Regarding claim 4, Gorobets et al. teach the nonvolatile memory (Figs. 15 MLC Memory) is flash memory because the device is a flash memory device (see ¶ [0135]; see also, Fig. 15, which labels the memory device as a "Flash Memory Device").

Regarding claim 7 and 8, although Gorobets et al. teach the volatile memory (Fig. 15 Cache (RAM) 102), they are silent with respect to the specific type of volatile memory—whether DRAM or SRAM as claimed. Gorobets et al. does not mention or show any aspects of the type of volatile memory employed

OFFICIAL NOTICE is taken that DRAM and SRAM are volatile memory types that have been frequently used as volatile memory in computer systems, and these two types of volatile memory are obvious variants and their tradeoffs are well-documented in the prior art. For example, although SRAM is faster than DRAM, SRAM requires more components per cell because typical prior art CMOS SRAM cell involve six transistors (6T-SRAM), whereas the counterpart typical DRAM cell requires one transistor and one capacitor (1T1C). DRAM, however, has been well-established in the industry as a main memory for computing systems. The real estate required per cell is smaller than that for SRAM, meaning more storage capacity at cheaper cost. The tradeoff is that DRAM must include refresh circuitry to account for decay rate of the capacitors. Although SRAM is typically used for cache memory, DRAM is often employed as well.

It would have obvious to one of ordinary skill in the art before the invention use DRAM or SRAM for the volatile memory as claimed because of the reasons discussed above.

Claim 5 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of Goodson et al., as applied to claim 1, in further view of De Ambroggi et al. (U.S. Patent Application Publication No. 2009/0268513, on record in parent application 13/455,267) and Kund et al. (U.S. Patent Application Publication No. 2010/0058018, on record in parent application 13/455,267).

Gorobets et al. fail to teach that the memory could be anything other than flash EEPROM or other types of charge trapping memory see e.g. ¶ [0010] describing the various types of memory.

De Ambroggi et al. teach that one type of resistive memory (RRAM), Phase Change (PCRAM or PCM) can be configured to be partially SLC and partially MLC.

Kund et al. teach generally that "Emerging memory technologies such as resistive memory (e.g., resistive random access memories such as phase change random access memory (PCRAM), conductive bridge random access memory (CBRAM), and magnetic random access memory (MRAM)) offer certain advantages over DRAM, Flash and other conventional types of memory devices in terms of switching speeds, size, power consumption, and non-volatility." ¶ [0016].

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the flash EEPROM taught by Gorobets et al. with the PCM taught by De Ambroggi et al. in view of the PCM advantages over flash EEPROM taught by Kund et al. because the emerging memories (such as PCRAM) offer switching speed, size, power-consumption, and non-volatility advantages over flash memory.

Claim 6 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of Goodson et al., as applied to claim 1, in further view of Chen et al. (U.S. Patent Application Publication No. 2009/0307418, on record in parent application 13/455,267) and Kund et al.

Gorobets et al. fail to teach that the memory could be anything other than flash EEPROM or other types of charge trapping memory see e.g. ¶ [0010] describing the various types of memory.

Chen et al. teach that MRAM could be used as SLC in conjunction with some other memory type being used as MLC to create a hybrid density memory. See e.g. ¶ [0031].

Kund et al. teach generally that "Emerging memory technologies such as resistive memory (e.g., resistive random access memories such as phase change random access memory (PCRAM), conductive bridge random access memory (CBRAM), and magnetic random access memory (MRAM)) offer certain

advantages over DRAM, Flash and other conventional types of memory devices in terms of switching speeds, size, power consumption, and non-volatility." ¶ [0016].

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the SLC flash EEPROM taught by Gorobets et al. with the SLC MRAM in view of the MRAM advantages over flash EEPROM taught by Kund et al. because the emerging memories (such as MRAM) offer switching speed, size, power-consumption, and non-volatility advantages over flash memory.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to R LANCE REIDLINGER whose telephone number is (571)270-7353. The examiner can normally be reached on M-F 1:00pm - 10:00pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rich T Elms can be reached on 571.272.1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer

Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R LANCE REIDLINGER/
Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 16/006,299	Applicant(s)/Patent Under Reexamination	
	Examiner R LANCE REIDLINGER	Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20100172179-A1	07-2010	Gorobets; Sergey Anatolievich	G06F12/0246	365/185.09
*	B	US-20090268513-A1	10-2009	De Ambroggi; Luca	G11C11/005	365/163
*	C	US-20100058018-A1	03-2010	Kund; Michael	G11C7/04	711/167
*	D	US-20090307418-A1	12-2009	Chen; Ming-Dar	G06F11/1048	711/105
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
*	U	Goodson et al, "Design Tradeoffs in a Flash Translation Layer." (Year: 2010)
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/006,299	RAO, G.R. MOHAN
	Examiner	Art Unit
	R LANCE REIDLINGER	2824

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Reviewed Prosecution & Search History of parent applications	01/19/2019	RLR

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

To: admin@dalpat.com,eofficeaction@appcoll.com,IPdocketing@munckwilson.com
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 25883

Jan 24, 2019 04:32:37 AM

Dear PAIR Customer:

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 25883 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
16006299	CTNF	01/24/2019	GRTD60-34138
	892	01/24/2019	GRTD60-34138

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	G.R. Mohan Rao	§	Conf. No.	6732
Serial No:	16/006,299	§	Group Art Unit:	2824
Filed:	June 12, 2018	§	Examiner:	Reidlinger, Ronald Lance

For: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Via EFS-Web
Mail Stop AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

The Applicant submits the following amendments and remarks in response to the Office Action dated January 24, 2019. If any extension of time for this Response is required, the Applicant requests that this be considered a petition therefore.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks begin on page 6 of this paper.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements; ~~and~~

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein;

the controller performing a data integrity test on stored data in a given one of the MLC and SLC nonvolatile memory elements after any access operation is performed thereon;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

2. (Currently Amended) The system of Claim 1, wherein the memory elements are a software module, a hardware module, a standalone device, or multi-chip package.

3. (Currently Amended) The system of Claim 1, wherein at least one of the volatile or nonvolatile memory elements ~~memories~~ are embedded in the at least one controller.

4. (Currently Amended) The system of Claim 1, wherein the MLC and SLC nonvolatile memory elements comprise [[is]] flash memory.

5. (Currently Amended) The system of Claim 1, wherein the memory in the SLC and MLC nonvolatile memory elements is phase-change memory.

6. (Currently Amended) The system of Claim 1, wherein the memory in the SLC and MLC nonvolatile memory elements is magnetic random access memory.

7. (Currently Amended) The system of Claim 1, wherein the random access volatile memory element is dynamic random access memory.

8. (Currently Amended) The system of Claim 1, wherein the random access volatile memory element is static random access memory.

9. (Original) The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

10. (New) The system of Claim 1, wherein the controller, upon detection of a failure of the data integrity test, remaps the data to the other of the MLC and SLC nonvolatile memory elements.

11. (New) The system of Claim 10, wherein the given one of the MLC and SLC nonvolatile memory elements is the MLC nonvolatile memory element.

12. (New) The system of Claim 10, wherein the SLC memory element has a higher endurance than the MLC memory element.

13. (New) The system of Claim 1, wherein the access operation is a Read operation.

14. (New) The system of Claim 1, wherein the access operation is a Write operation.

15. (New) The system of Claim 1, wherein the MLC is a 1 bit cell.

16. (New) The system of Claim 1, wherein the MLC is a multilevel cell, wherein the multilevel cell stores n bits per cell, wherein n is any integer greater than 1.

17. (New) The system of Claim 16, wherein the multilevel cell is a 3 bit cell.

18. (New) The system of Claim 16, wherein the multilevel cell is a 4 bit cell.

19. (New) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

at least one controller to maintain an address table in one or more of the memory elements;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein;

the controller performing a data integrity test on stored data in a given one of the MLC and SLC nonvolatile memory elements after any access operation is performed thereon;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

20. (Currently Amended) The system of Claim 19, wherein the memory elements are a software module, a hardware module, a standalone device, or multi-chip package.

21. (Currently Amended) The system of Claim 19, wherein at least one of the volatile or nonvolatile memory elements are embedded in the at least one controller.

REMARKS

Applicant has carefully reviewed the Office Action dated January 24, 2019. Applicant has amended Claims 1-8 and added new Claims 10-21 to more clearly point out the present inventive concept. No new matter has been added. Reconsideration and favorable action are respectfully requested.

Claim 1 has been amended to add the limitation wherein the controller is operable to perform a data integrity check after an access operation and, upon a failure of the data integrity check, remap the physical memory address space. Support for this can be found at paragraphs [0014], [0021], [0024], and [0025]. This remapping is for the purpose of endurance and, as such, after remapping, endurance will be increased. Further, new claims 10 – 21 further define this remapping as remapping from the MLC to the SLC, wherein the SLC is a higher endurance memory.

Claims 1 – 4 and 7 – 9 stand rejected under 35 U.S.C. §103(a) as unpatentable over the combination of Gorobets in view of Goodson. This rejection is respectfully traversed with respect to the claims as currently presented.

The Gorobets reference does not disclose or suggest a remapping operation wherein the remapping operation is for the purpose of improving the endurance. Rather, all that the Gorobets reference does is remap for wearability in accordance with a wearability algorithm. There is no integrity check that is performed for this operation. Further, there is no indication that the remapping of the physical address space will be from a memory element having a relatively lower endurance to another memory element having a relatively higher endurance. The Goodson reference does not cure this deficiency. Therefore, Applicant respectfully requests withdrawal of the 35 U.S.C. §103 rejection with respect to Claims 1 – 4 and 7 – 9.

Claim 5 has been rejected under 35 U.S.C. §103(a) in view of the additional reference Kund and Claim 6 has been rejected in view of the additional reference Chen. Claims 5 and 6 depend from Claim 1 and, therefore, for the reasons stated hereinabove, are believed to be allowable for the reasons described with respect hereinabove to Claim 1 and, therefore, Applicant respectfully requests withdrawal of the 35 U.S.C. §103 rejection with respect to Claims 5 and 6.

CONCLUSION

Applicant has now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicant respectfully requests full allowance of the claims as amended.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at patents@naifeh.com.

Recognizing that Internet communications are not secure, Applicant hereby authorizes the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. Applicant understands that a copy of these communications will be made of record in the application file.

Respectfully submitted,

/Bill R. Naifeh, Reg No. 44,962/

Bill R. Naifeh
Registration No. 44,962
Acting in a Representative Capacity
under 37 CFR 1.34

Bill R. Naifeh
Law Office of Bill Naifeh
15303 Dallas Parkway
Suite 700
Addison, TX 75001
972-726-9500
214-550-2542 (fax)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/006,299	06/12/2018	G.R. MOHAN RAO	GRTD60-34138	6732

25883 7590 12/13/2019

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380

EXAMINER
REIDLINGER, RONALD LANCE

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
12/13/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPdocketing@munckwilson.com
admin@dalpat.com
eofficeaction@appcoll.com

Office Action Summary	Application No. 16/006,299	Applicant(s) RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 26 June 2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-21 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-21 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 12 June 2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 are pending.

2. Claims 1 and 19 are independent.

Notice of Pre-AIA or AIA Status

3. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 112(a)

4. The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. **Claims 2, 5, 6 and 15-18 and 20 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement.** The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 2 and 20, there is no support for the memory elements being software.

Regarding claims 5 and 6, there is no support for the memory in the MLC nonvolatile memory nonvolatile memory elements being phase-change or magnetic random access memory.

Regarding claims 15-18, there is no support for the MLC being anything other than two bits.

Claim Rejections - 35 USC § 112(b)

6. The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 2, 15 and 19-21 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.**

Regarding claims 2 and 20, it is unclear what is meant by a memory element being a software module.

Regarding claim 15, it is unclear what is meant by a MLC having only one bit. An MLC must have at least two bits or it is an SLC.

Regarding claim 19, the following limitations establish conflicting antecedent basis,

"at least one controller to operate memory elements and associated memory space"

"at least one controller to maintain an address table in one or more of the memory elements"

It's unclear whether this is the same controller or a different one and to which each instance of the controller is referring.

Regarding claims 20 and 21, they are indefinite for depending on an indefinite claim.

Claim Rejections - 35 USC § 103

8. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory

basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

9. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. **Claims 1-4 and 7-17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. (U.S. Patent Application Publication No. 2010/0172179, on record in parent application 13/455,267) in view of Goodson et al. ("Design Tradeoffs in a Flash Translation Layer," on record in parent application 13/455,267) and Oribe et al. (US 2009/0172267 A1)**.

Regarding claim 1, Gorobets et al. teach,

A system for storing data (e.g. Fig. 20) comprising:

memory space containing volatile memory space (Fig. 15, 102 Cache (RAM), see e.g. ¶ [0135] "volatile RAM are employed as cache as . . . in a controller cache 102") and nonvolatile memory space (Fig. 15, MLC Memory, including Main Memory and Binary Cache), wherein the nonvolatile memory

space includes both multilevel cell (MLC) space (Fig. 15, 202 Main Memory of MLC Memory) and single level cell (SLC) space (Fig. 15, 204 Binary Cache of MLC Memory);

at least one controller (Fig. 8 Memory Manager No. 300; see also Fig. 15 Controller) to operate memory elements and associated memory space (Flash Memory No. 200);

at least one MLC nonvolatile memory element (Fig. 20 Main Portion MLC No. 2003; this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one SLC nonvolatile memory element (Fig. 20 Binary Portion No. 2001; again, this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one random access volatile memory element (see Fig. 15, 102 Cache (RAM));

wherein the at least one controller (Fig. 8 Memory Manager No. 300; see also Fig. 15 Controller) maintains an address table in one or more of the memory elements (see ¶ [0096]);

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein (see ¶ [0092]);

wherein the address table maps logical and physical addresses (memory manager in the controller maps logical addresses to physical addresses, see ¶ [0096]) adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories (see ¶ [0152-154], explaining the use of spare block pool management to increase lifetime of the memory device; mapping would be necessary to remap any logical address pointing to a retired block so that it points to a replacement block, or new physical address).

Gorobets et al. explain address translation layers for flash memory, but do not describe the specific term “an FTL flash translation layer.”

Nevertheless, Goodson et al. document the purpose and motivation for using FTL for a flash memory device (see Title, "Design Tradeoffs in a Flash Translation Layer," and §§ 1-2, which explain the purpose of flash translation layers).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Goodson et al. to the teachings of Gorobets et al. such that an FTL (as explained by Goodson et al.) is used with the flash device taught by Gorobets et al. for the purpose of allowing the files system of the flash memory device to maintain the block interface of the disk without sacrificing the tighter integration and control over how the flash is managed and because it hides the complexity of the flash by providing a logical block interface for the flash device.

Further, Gorobets et al. fail to explicitly teach the data integrity test and remapping in response to a failure of the test. Gorobets et al. clearly hints at such a test as it discusses errors and the need to relocate due to errors (see e.g. ¶¶ [0164]), but Gorobets et al. fail to teach that the errors are detected with an integrity test.

Oribe et al. teach in Fig. 7 using a data integrity test (i.e. bit error greater than threshold, see e.g. SP10, 12 and 14) to mark a block for refresh. See ¶ [0060]. Oribe et al. further teach that in a refresh the data is moved to a new block and the address management table is updated. See Fig. 8 and ¶¶ [0061 and 0056].

Using a data integrity test can put a high priority in moving data from bad blocks prior to them completely failing and losing the data. Thus it would have been obvious to one of ordinary skill in the art prior to the effective filing date to use the data integrity test to ensure that the data is saved.

Regarding claims 2 and 9, Gorobets et al. explain that flash memory is most commonly provided in the form of a memory card (i.e., module or standalone unit as claimed) or a flash drive (i.e., module or standalone unit or hard drive, as claimed) (see background ¶ [0015]). Because Gorobets et al.

embodiments involve flash memory, the provisions of being a hardware module, a standalone device or a hard disk drive, as claimed, are met.

Regarding claim 3, Gorobets et al. teach at least one of the volatile or nonvolatile memories are embedded in the at least one controller (see Fig. 15 volatile Cache (RAM) 102 is embedded within Controller).

Regarding claim 4, Gorobets et al. teach the MLC and SLC nonvolatile memory elements (Figs. 15 MLC Memory) is flash memory because the device is a flash memory device (see ¶ [0135]; see also, Fig. 15, which labels the memory device as a "Flash Memory Device").

Regarding claims 7 and 8, although Gorobets et al. teach the volatile memory (Fig. 15 Cache (RAM) 102), they are silent with respect to the specific type of volatile memory—whether DRAM or SRAM as claimed. Gorobets et al. does not mention or show any aspects of the type of volatile memory employed.

OFFICIAL NOTICE is taken that DRAM and SRAM are volatile memory types that have been frequently used as volatile memory in computer systems, and these two types of volatile memory are obvious variants and their tradeoffs are well-documented in the prior art. For example, although SRAM is faster than DRAM, SRAM requires more components per cell because typical prior art CMOS SRAM cell involve six transistors (6T-SRAM), whereas the counterpart typical DRAM cell requires one transistor and one capacitor (1T1C). DRAM, however, has been well-established in the industry as a main memory for computing systems. The real estate required per cell is smaller than that for SRAM, meaning more storage capacity at cheaper cost. The tradeoff is that DRAM must include refresh circuitry to account for decay rate of the capacitors. Although SRAM is typically used for cache memory, DRAM is often employed as well.

Therefore, it would have obvious to one of ordinary skill in the art before the invention use DRAM or SRAM for the volatile memory as claimed because of the reasons discussed above.

Regarding claim 10, Gorobets et al. teach remapping from the MLC to SLC and SLC to MLC, see ¶ [0157]. As discussed above in the rejection of claim 1, it would have been obvious to remap in response to a failure of the data integrity test.

Regarding claim 11, Gorobets et al. teach remapping from the MLC to SLC and SLC to MLC, see ¶ [0157]. Thus the given one could be either SLC or MLC.

Regarding claim 12, Gorobets et al. teach SLC has better endurance. See ¶ [0165].

Regarding claims 13 and 14, Gorobets et al. teach both read and write access operations, see ¶ [0009]. Oribe et al. further teach both write and read would happen prior to refresh, see e.g. SP2 or SP5 of Fig. 6

Regarding claims 15-17, Gorobets et al. teach that he MLC can be 1, 2 or 3 bits per cell (see ¶¶ [0158] & [0070]).

12. **Claim 5 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of Goodson et al. and Oribe et al., as applied to claim 1, and further in view of De Ambroggi et al. (U.S. Patent Application Publication No. 2009/0268513, on record in parent application 13/455,267) and Kund et al. (U.S. Patent Application Publication No. 2010/0058018, on record in parent application 13/455,267).**

Gorobets et al. fail to teach that the memory could be anything other than flash EEPROM or other types of charge trapping memory see e.g. ¶ [0010] describing the various types of memory.

De Ambroggi et al. teach that one type of resistive memory (RRAM), Phase Change (PCRAM or PCM) can be configured to be partially SLC and partially MLC.

Kund et al. teach generally that "Emerging memory technologies such as resistive memory (e.g., resistive random access memories such as phase change random access memory (PCRAM), conductive bridge random access memory (CBRAM), and magnetic random access memory (MRAM) offer certain

advantages over DRAM, Flash and other conventional types of memory devices in terms of switching speeds, size, power consumption, and non-volatility." ¶ [0016].

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the flash EEPROM taught by Gorobets et al. with the PCM taught by De Ambroggi et al. in view of the PCM advantages over flash EEPROM taught by Kund et al. because the emerging memories (such as PCRAM) offer switching speed, size, power-consumption, and non-volatility advantages over flash memory.

13. **Claim 6 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of Goodson et al. and Oribe et al., as applied to claim 1, in further view of Chen et al. (U.S. Patent Application Publication No. 2009/0307418, on record in parent application 13/455,267) and Kund et al.**

Gorobets et al. fail to teach that the memory could be anything other than flash EEPROM or other types of charge trapping memory see e.g. ¶ [0010] describing the various types of memory.

Chen et al. teach that MRAM could be used as SLC in conjunction with some other memory type being used as MLC to create a hybrid density memory. See e.g. ¶ [0031].

Kund et al. teach generally that "Emerging memory technologies such as resistive memory (e.g., resistive random access memories such as phase change random access memory (PCRAM), conductive bridge random access memory (CBRAM), and magnetic random access memory (MRAM)) offer certain advantages over DRAM, Flash and other conventional types of memory devices in terms of switching speeds, size, power consumption, and non-volatility." ¶ [0016].

Accordingly it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the SLC flash EEPROM taught by Gorobets et al. with the SLC MRAM in view of the MRAM advantages over flash EEPROM taught by Kund et al. because the emerging memories (such as

MRAM) offer switching speed, size, power-consumption, and non-volatility advantages over flash memory.

14. Claim 18 is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of Goodson et al. and Oribe et al., as applied to claims 1 and 16, and further in view of Lasser (US 2008/0181000 A1).

Gorobets et al. fail to teach 4 bit MLC. Lasser teaches that it was known to have one two three or four bits in a cell with the latter having the largest capacity. See ¶ [0009]. Accordingly it would have been obvious to one of ordinary skill in the art prior to the effective filing date to use 4 bit MLC to increase capacity.

15. **Claims 19-21 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Gorobets et al. in view of Oribe et al.**

Regarding claim 19, Gorobets et al. teach,

A system for storing data (e.g. Fig. 20) comprising:

memory space containing volatile memory space (Fig. 15 Cache (RAM)) and nonvolatile memory space (Fig. 15, MLC Memory, including Main Memory and Binary Cache), wherein the nonvolatile memory space includes both multilevel cell (MLC) (Figs. 15, 20 Main Memory of MLC Memory) space (Figs. 15, 20 Main Memory of MLC Memory) and single level cell (SLC) space (Figs. 15, 20 Binary Cache of MLC Memory);

at least one controller (Fig. 8 Memory Manager No. 300; see also Fig. 15 Controller) to operate memory elements and associated memory space (Flash Memory No. 200);

at least one MLC nonvolatile memory element (Fig. 20 Main Portion MLC No. 2003; this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one SLC nonvolatile memory element (Fig. 20 Binary Portion No. 2001; again, this is a primary characteristic of flash EEPROM of which this device is, see e.g. ¶ [0008]);

at least one random access volatile memory element (see Fig. 15 Cache (RAM));

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein (see ¶ [0092]);

wherein the at least one controller (Fig. 8 Memory Manager No. 300; see also Fig. 15 Controller) of both maintain an address table in one or more of the memory elements (see ¶ [0096]); and

wherein the address table maps logical and physical addresses (memory manager in the controller maps logical addresses to physical addresses, see ¶ [0096]) adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories (see ¶ [0152-154], explaining the use of spare block pool management to increase lifetime of the memory device; mapping would be necessary to remap any logical address pointing to a retired block so that it points to a replacement block, or new physical address).

at least one controller to maintain an address table in one or more of the memory elements (see ¶ [0096]);

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein(see ¶ [0092]);

wherein the address table maps logical and physical addresses (memory manager in the controller maps logical addresses to physical addresses, see ¶ [0096]) adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories memories (see ¶ [0152-154], explaining the use of spare block pool management to increase lifetime of the memory device; mapping would be necessary to remap any logical address pointing to a retired block so that it points to a replacement block, or new physical address).

Gorobets et al. fail to teach,

the controller performing a data integrity test on stored data in a given one of the MLC and SLC nonvolatile memory elements after any access operation is performed thereon;

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

Oribe et al. teach in Fig. 7 using a data integrity test (i.e. bit error greater than threshold, see e.g. SP10, 12 and 14) to mark a block for refresh. See ¶ [0060]. Oribe et al. further teach that in a refresh the data is moved to a new block and the address management table is updated See Fig. 8 and ¶¶ [0061 and 0056].

Using a data integrity test can put a high priority in moving data from bad blocks prior to them completely failing and losing the data. Thus it would have been obvious to one of ordinary skill in the art prior to the effective filing date to use the data integrity test to ensure that the data is saved.

Regarding claim 20, Gorobets et al. explain that flash memory is most commonly provided in the form of a memory card (i.e., module or standalone unit as claimed) or a flash drive (i.e., module or standalone unit or hard drive, as claimed) (see background ¶ [0015]). Because Gorobets et al. embodiments involve flash memory, the provisions of being a hardware module or a standalone device, as claimed, are met.

Regarding claim 21, Gorobets et al. teach at least one of the volatile or nonvolatile memory elements are embedded in the at least one controller. (See Fig. 15 Cache RAM is in the controller)

Response to Arguments

16. Applicant's arguments filed 26 June 2019 have been fully considered but they are not persuasive. Applicant's initial arguments appear to be directed towards the intended purpose of the limitations rather than the limitations themselves. Furthermore, Gorobets et al. does remap to improve endurance. See e.g. ¶ [0155]. Applicant's second argument that Gorobets et al. and the other

references fail to teach an integrity check is not directed towards the Oribe et al. reference and is moot in light of the new grounds for rejection.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R LANCE REIDLINGER whose telephone number is (571)270-7353. The examiner can normally be reached on M-F 1:00pm - 10:00pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rich T Elms can be reached on 571.272.1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained

from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R.L.R./
Examiner, Art Unit 2824

/J. H. Hur/
Primary Patent Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 16/006,299	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20090172267-A1	07-2009	ORIBE; Hiromichi	G11C16/3418	711/103
*	B	US-20080181000-A1	07-2008	Lasser; Menahem	G11C11/5628	365/185.03
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/006,299	RAO, G.R. MOHAN
	Examiner	Art Unit
	R LANCE REIDLINGER	2824

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Reviewed Prosecution & Search History of parent applications	01/19/2019	RLR
Searched for new limitations	12/09/2019	RLR

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/R LANCE REIDLINGER/ Examiner, Art Unit 2824	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S157	889	oribe.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/12/04 18:49
S158	0	S157 and count adj threshold	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/12/04 18:49
S159	1	S157 and "9,999"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/12/04 18:50
S160	1	16/006299.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/12/04 18:53
S161	1	16/006299.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/12/09 09:17
S163	122	four adj bits adj per adj cell & "2009"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/12/09 15:26
S164	2	11/836158.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/12/09 15:30

EAST Search History (Interference)

< This search history is empty>

12/ 9/ 2019 5:46:24 PM
C:\ Users\ rreidlinger\ Documents\ EAST\ Workspaces\ 13455267.wsp

To: admin@dalpat.com,eofficeaction@appcoll.com,IPdocketing@munckwilson.com
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 25883

Dec 13, 2019 03:28:29 AM

Dear PAIR Customer:

MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS, TX 75380
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 25883 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
16006299	CTFR	12/13/2019	GRTD60-34138
	892	12/13/2019	GRTD60-34138

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	G.R. Mohan Rao	§	Conf. No.	6732
Serial No:	16/006,299	§	Group Art Unit:	2824
Filed:	June 12, 2018	§	Examiner:	Reidlinger, Ronald

For: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AFTER FINAL AND RESPONSE TO OFFICE ACTION
WITH REQUEST FOR CONTINUED EXAMINATION

Dear Sir:

This communication is responsive to the Examiner's Final Office Action dated December 13, 2019. Reconsideration is respectfully requested.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

PGR2025-00011/PHI EX. 1012 Page 55 of 98

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein;

the controller performing a data integrity test on stored data in a given one of the MLC and SLC nonvolatile memory elements after any access operation is performed thereon;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

2. (Currently Amended) The system of Claim 1, wherein the FTL flash translation layer is ~~elements are memory~~ a software module, or a firmware module containing software updates ~~a hardware module, a standalone device, or multi-chip package~~.

PGR2025-00011/PHI EX. 1012 Page 56 of 98

3. (Previously presented) The system of Claim 1, wherein at least one of the volatile or nonvolatile memory elements are embedded in the at least one controller.

4. (Previously presented) The system of Claim 1, wherein the MLC and SLC nonvolatile memory elements comprise flash memory.

5. (Cancelled)

6. (Cancelled)

7. (Previously presented) The system of Claim 1, wherein the random access volatile memory element is dynamic random access memory.

8. (Previously presented) The system of Claim 1, wherein the random access volatile memory element is static random access memory.

9. (Original) The system of Claim 1, wherein the at least one SLC nonvolatile memory element includes a hard disk drive (HDD).

10. (Previously presented) The system of Claim 1, wherein the controller, upon detection of a failure of the data integrity test, remaps the data to the other of the MLC and SLC nonvolatile memory elements.

11. (Cancelled)

12. (Previously presented) The system of Claim 10, wherein the SLC memory element has a higher endurance than the MLC memory element.

13. (Previously presented) The system of Claim 1, wherein the access operation is a Read operation.

14. (Previously presented) The system of Claim 1, wherein the access operation is a Write operation.

15. (Cancelled)

16. (Previously presented) The system of Claim 1, wherein the MLC is a multilevel cell, wherein the multilevel cell stores n bits per cell, wherein n is any integer greater than 1.

17. (Previously presented) The system of Claim 16, wherein the multilevel cell is a 3 bit cell.

18. (Previously presented) The system of Claim 16, wherein the multilevel cell is a 4 bit cell.

19. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space, and to maintain an address table in one or more of the memory elements;

at least one MLC nonvolatile memory element;

at least one SLC nonvolatile memory element;

at least one random access volatile memory element;

~~at least one controller to maintain an address table in one or more of the memory elements;~~

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory elements for storage of data therein;

the controller performing a data integrity test on stored data in a given one of the MLC and SLC nonvolatile memory elements after any access operation is performed thereon;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer

PGR2025-00011/PHI EX. 1012 Page 58 of 98

of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

20. (Cancelled)

21. (Cancelled)

22. (New) The system of Claim 1, wherein frequently accessed requests to the memory space are moved from the MLC space or a random memory space, to the SLC space, and wherein a Write request to the memory space is placed in the SLC space as long as there is storage space available in the SLC space, wherein the SLC space is used as a write cache.

23. (New) The system of Claim 1, wherein frequently accessed requests to the memory space due to host writes to the random access volatile memory element, subsequently intended for the nonvolatile memory space, are moved from the MLC space to the SLC space.

24. (New) The system of Claim 1, wherein frequently accessed requests to the memory space due to wear leveling are moved from the MLC space to the SLC space.

25. (New) The system of Claim 1, wherein frequently accessed requests to the memory space due to read or write, or read, modify, or write, or data moves which contain frequent erases are moved from the MLC space to the SLC space.

REMARKS

Applicant has carefully reviewed the Office Action dated December 13, 2019. Applicant has amended claims 1, 2, and 19. Claims 5, 6, 11, 15, 20, and 21 have been cancelled. New claims 21-25 have been added. Reconsideration and favorable action is respectfully requested.

I. Rejections under 35 U.S.C. §112, first paragraph

Claims 2, 5, 6, 15-18, and 20 stand rejected under §112, first paragraph. Claims 5, 6, 15, and 20 have been cancelled.

Claim 2 has been amended to recite an "FTL flash transition layer." Applicant submits that the FTL flash translation layer being a software module is supported, for example, in paragraph [0009], which recites "firmware commonly known as FTL," with firmware being generally known to refer to software.

With respect to claim 16-18, the rejections states that "there is no support for the MLC being anything other than two bits." Applicant submits that MLCs of more than two bits are supported, for example, in paragraphs [0004] and [0010], portions of which are reproduced below:

> [0004] … MLC NAND flash is a flash memory technology using multiple levels per cell to allow more bits to be stored using the same number of transistors. In SLC NAND flash technology, each cell can exist in one of two states, storing one bit of information per cell. Most MLC NAND flash memory has four possible states per cell, so it can store two bits of information per cell.

> [0010] … MLC allows a single cell to store multiple bits, and accordingly, to assume more than two values; i.e., '0' or' 1'. Most MLC NAND flash architectures allow up to four (4) values per cell; i.e., '00', '01 ', '1 0', or' 11'….

Applicant directs the Examiner's attention to the statements that "MLC NAND flash is a flash memory technology using multiple levels per cell to allow more bits to be stored" (relative to SLC) and "MLC allows a single cell to store multiple bits," both indicating two or more bits without limiting the upper bound. Furthermore, the statements that "[m]ost MLC NAND flash memory has four possible states per cell, so it can store two bits of information per cell" and "[m]ost MLC NAND flash architectures allow up to four (4) values per cell" indicate that higher

numbers of bits must be available, since "most" MLCs provide two bits and other MLCs must therefore exist with different numbers of bits relative to "most" MLCs.

Accordingly, Applicant respectfully requests that the rejections under §112, first paragraph, be withdrawn.

II. Rejections under 35 U.S.C. §112, second paragraph

Claims 2, 15, and 19-21 stand rejected under §112(b), second paragraph. Claims 15, 20, and 21 have been cancelled.

Claim 2 has been amended to delete the "memory element" and to recite an "FTL flash transition layer." Applicant submits that the FTL flash translation layer being a software module is supported, for example, in paragraph [0009], which recites "firmware commonly known as FTL," with firmware being generally known to refer to software.

Claim 19 has been amended to clarify the language with respect to the "at least one controller."

Accordingly, Applicant respectfully requests that the rejections under §112, second paragraph, be withdrawn.

III. Rejections under 35 U.S.C. §103

A. Claims 1-4 and 7-18

Claims 1 – 4 and 7 – 17 stand rejected under 35 USC §103(a) as being unpatentable over the combination of *Gorobets* in view of *Goodson* and *Oribe*. Claim 18 stands rejected over the previous combination when further combined with *Lasser*. This rejection is respectfully traversed with respect to the claims as currently amended.

One issue that the Examiner specifically noted was that *Gorobets* fails to teach the data integrity test and so *Oribe* is used to support the rejection of this particular feature, stating as follows:

> Further, Gorobets et al. fail to explicitly teach the data integrity test and remapping in response to a failure of the test. Gorobets et al. clearly hints at such a test as it discusses errors and the need to relocate due to errors (see e.g. , ¶ ¶ [0164]), but Gorobets et al. fail to teach that the errors are detected with an integrity test.
>
> Oribe et al. teach in Fig. 7 using a data integrity test (i.e. bit error greater than threshold, see e.g. SPIO, 12 and 14) to mark a block for refresh. See , ¶ [0060]. Oribe et al. further teach that in a refresh the data is moved to a new block and the address management table is updated. See Fig. 8 and ¶ ¶ [0061 and 0056].
>
> Using a data integrity test can put a high priority in moving data from bad blocks prior to them completely failing and losing the data. Thus it would have been obvious to one of ordinary skill in the art prior to the effective filing date to use the data integrity test to ensure that the data is saved.

For informative purposes, the aspect of the data integrity test with respect to the current Specification will be described. The description is primarily with respect to the flowchart of Figures 3a-b, with the related description defined in ¶26 and ¶27 as follows:

> **[0026]** FIGS. 3A and 3B are a flow chart illustrating a method for utilizing a NAND flash memory system incorporating one embodiment of the present disclosure. The method begins in a step 100, when a command to write a quantum of data stored in DRAM to a particular location in NAND flash memory is received. In step 102, the quantum of data is read from DRAM into memory within the device controller (which acts as the memory controller). In step 104, both the logical address range and the NAND flash physical address range to which the quantum of data is to be written, is read into memory of the device controller. In step 106, the quantum of data to be written is combined with the contents of the NAND flash memory. In step 108, the NAND flash physical address range to be written is erased. In step 110, the combined data is written to the appropriate NAND flash physical address range. In step 112 the NAND flash physical address range that was written in step 110 is read into device controller memory.
>
> **[0027]** The flowchart continues in FIG. 3B. In step 114 the NAND flash physical address range that was read into device controller memory is compared with the retained data representing the combination of the previous contents of the physical range address and the quantum of data to be written. In step 116, if the retained data matches the newly stored data in the NAND flash memory, the write was a success, and the method exits in step 118. However, if the retained data does not match the newly stored data in the NAND flash memory, the method executes step 120, which identifies the next quantum of available SLC NAND flash memory addresses. In step 122, a check is made to determine if additional SLC NAND flash memory is available, and, if not, the NAND flash memory system is marked as failed, prompting a system alert step 124. However, if additional SLC NAND flash memory is available, the failed NAND flash physical address range is remapped to the next available quantum of SLC

NAND flash memory in step 126. Execution then returns to step 110, where the write is repeated.

This description, with respect to data integrity, relates primarily to Figure 3b, as follows:

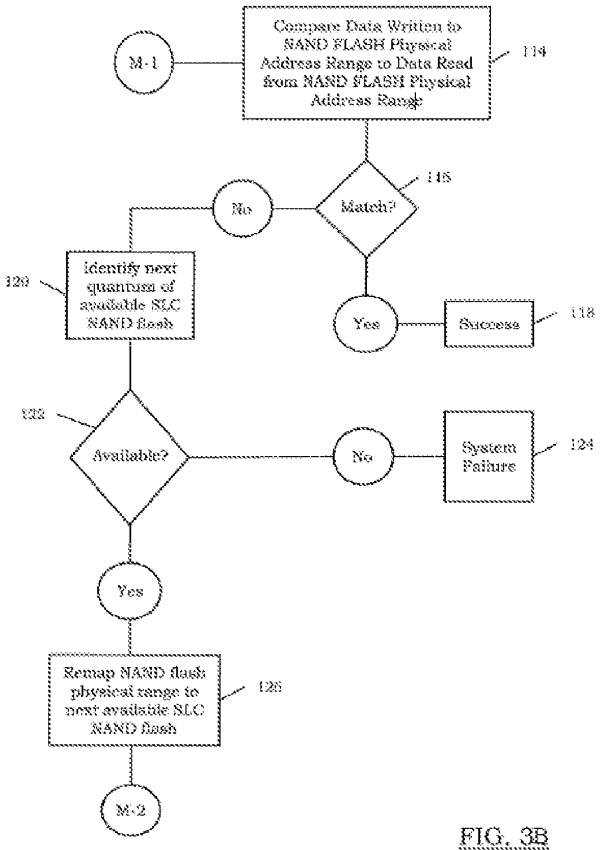


FIG. 3B

From this description and figure, it can be seen that the operation's first step, as defined in Claim 1, is to write the combined data to the appropriate NAND Flash, set forth in this portion of Figure 3a:

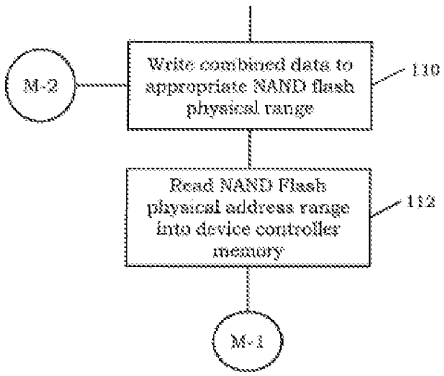


FIG. 3A

In this operation, the following steps are performed in sequence:

- a quantum of data to be transferred from DRAM to Flash is the subject of a Write command;
- the mapping of the logical address to the physical address in the Flash is then determined to which this quantum of data is to be written;
- the quantum of data to be written is then combined with the contents of the Flash in the associated physical address range and this is referred to as “combined data”;
- the Flash physical address range to be written is then erased in preparation for storing the new combined data therein;
- the combined data is then written to this recently erased physical address range;
- the recently written data is then accessed (Step 112) from the recently written physical address range in the Flash;
- this accessed data is then compared (Step 114) with what is termed “retained data” which represents “the combination of the previous contents of the physical address range and the quantum updated to be written.” Thus, the system retains

the data that was written to the Flash physical address range for a later data integrity check;

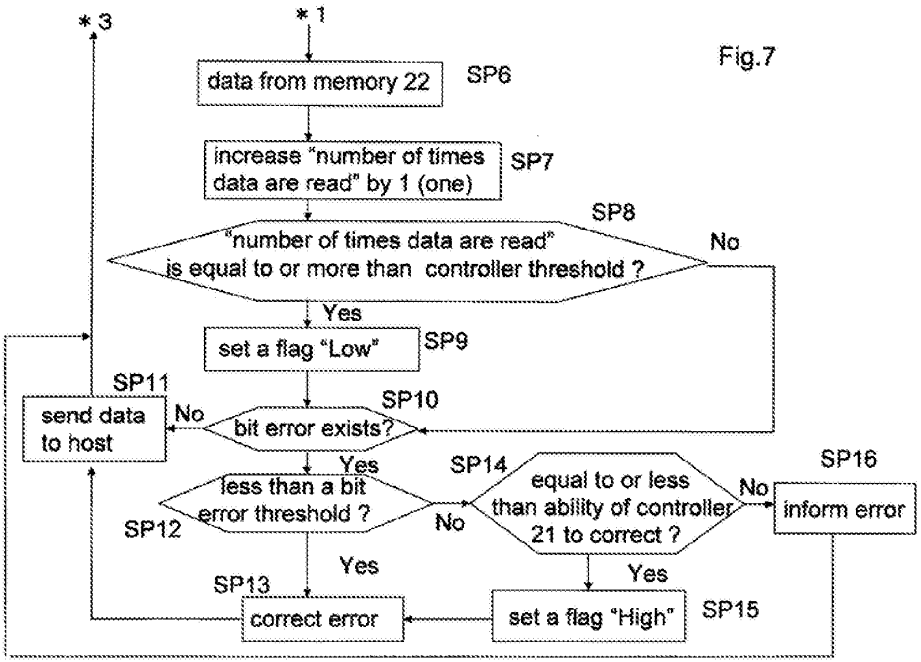
- a determination is then made as to whether the retained data matches the accessed data (Step 116);

- if the result of the matching operation is negative, this is determined to be a failed NAND flash physical address range;

- once a failed NAND flash physical address range has been determined as being present with respect to the currently to be written quantum of data, the next step is to determine if there are additional physical address ranges that can be written to in the NAND flash and, if so, the failed NAND flash physical address range is remapped and, if not, and indications made the system has failed.

Thus, the operation requires a retention of the data written to the Flash in order to perform the data integrity check and this is an important distinction.

The Examiner has relied upon Figure 7 in Oribe to support utilization of a data integrity test. This figure set forth as follows:



The operation of *Oribe* is considerably different than that associated with the currently claimed process. *Oribe* basically performs a wearability test by counting a number of times that date is read and comparing it to a threshold. Regardless of the determination, a bit error test is then performed (SP10). If a bit error exists with respect to the data that is read, the bit error compared to an error threshold. If it is below the threshold, this is a known proration that can be corrected and the error is corrected. However, if the bit error is above the threshold, then the system determines whether the error can be corrected by the controller. If not, the system is informed of the error. This operation is set forth in ¶ [0060] as follows:

> …. Then operation proceeds to step SP**10**, during which controller **21** determines whether a bit error exists in the data read from memory **22** in response to the command issued by host **1**. If the result of step SP**10** is "No", controller **21**, during step SP**11**, sends the data read from memory **22**, as is, to the host **1**. If the result of step SP**10** is "yes," controller **21** determines, during step SP**12**, whether the number of bit errors is less than the bit error threshold. If the result of step SP**12** is "yes", controller **21** corrects such a bit error during step SP**13**. Then controller **21** sends the data read from the executed physical block of memory **22** with the corrected data to the host **1**, as indicated by step SP**11**. If the number of bit errors is equal to or more than the bit error threshold ("No" in step SP**12**), controller **21** determines, during step SP**14**, whether the number of bit errors is equal to or less than the ability of controller **21** to correct the error. If the result of step SP**14** is "yes", the controller **21**, during step SP**15**, sets a "High"

> refresh flag in the refresh management table **222** for the command-executed physical block number. In addition, controller **21** corrects such a bit error, as indicated by step SP**13**, and then sends the corrected data to host **1**, as indicated by strep SP**11**. If the number of bit errors exceeds the ability of controller **21** to correct the bit errors, controller **21** sends a "system error" signal to host **1** (SP**16**).
>
> This error correction operation is defined in ¶ [0053] as follows:
>
> When user data are written to a flash memory, an error check code created during the data write operation is added to the user data. When the data are read from the flash memory, they are checked according to the error check code by an error correcting circuit (not shown) within the controller **21** to determine whether or not there is an error in the written data. If the number of bit errors is within the ability of the controller to correct the errors (e.g. 8 bits or less), the bit errors can be corrected. If the number of bit errors is more than the ability of controller **21** to correct the errors, the bit errors can not be corrected. This means that the block has become a bad (i.e. defective) block due to numerous data write or erase cycles being executed in the block.

It can be seen that the error check code is created during a data write operation such that, when read, a determination as to utilizing this error check code to correct the error can be made. However, this is not a compare operation with the data that was read but, rather, it is a determination that, if the integrity of the data has been compromised for some reason, it might be correctable depending upon how many bit errors are present. If too many bit errors are present, the error correction algorithm cannot correct the data. If a determination is made that the data cannot be corrected in *Oribe*, it is an indication that the block has become defective for some reason. At that point, this data is basically lost. There is no operation wherein this data can be written to another location. Claim 1 as amended provides:

> *wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.*

Applicant submits that neither *Gorobets* nor *Oribe* can remap the address space to a different physical range of addresses "and transfer of data corresponding to the stored data to those remapped physical addresses." *Oribe* can only determine that a block of Flash memory has failed but, after such a determination, any data stored therein is lost. Since the operation of a Flash memory after accessing data therefrom requires an Erase operation, it is this Erase operation that provides the most stress on the Flash memory, thus causing a particular section

to fail. Since neither *Gorobets* nor *Oribe* retain the data to be written for later comparison, neither suggests nor discloses such an operation, either singly or in combination

Claims 2-4, 7-10, 12-14, and 16-18 depend from and further limit claim 1, and therefore are allowable for at least the same reasons as claim 1.

B. Claim 19

Claim 19 includes similar language to that discussed above with respect to claim 1, and therefore is allowable for at least the same reason as claim 1.

C. Claims 22-25

New claims 22-25 depend from and further limit claim 1, and therefore are allowable for at least the same reasons as claim 1.

IV. Conclusion

For the reasons described above, Applicant submits that all pending claims are in condition for allowance. If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at tim@naifeh.com.

Recognizing that Internet communications are not secure, Applicant hereby authorizes the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. Applicant understands that a copy of these communications will be made of record in the application file.

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Bill R. Naifeh
Registration No. 44,962

Bill R. Naifeh
Law Office of Bill Naifeh
15303 Dallas Parkway
Suite 700
Addison, TX 75001
972-726-9500
214-550-2542 (fax)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	RAO, G.R. Mohan
Serial No.:	16/006,299
Confirmation No.:	6732
Filed:	June 12, 2018
Group:	2824
Examiner:	REIDLINGER, Ronald Lance
For:	LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

AMENDMENT

This communication is responsive to the Examiner's Office Action dated April 28, 2020. Reconsideration is respectfully requested.

Amendments to the Claims are reflected in the listing of claims beginning on page 2 of this paper.

Remarks/Arguments begin on page 7 of this paper.

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) memory space and single level cell (SLC) memory space;

at least one controller to operate memory elements and associated memory space;

at least one MLC nonvolatile memory element that can be mapped into the MLC memory space;

at least one SLC nonvolatile memory element that can be mapped into the SLC memory space;

at least one random access volatile memory ~~element~~;

an FTL flash translation layer, wherein the at least one controller, or FTL, or a combination of both maintain an address table in one or more of the memory elements and random access volatile memory;

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory ~~elements~~ for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in ~~a given one of~~ the MLC ~~and SLC~~ nonvolatile memory element ~~elements~~ after [[any]] at least a Write access operation [[is]] performed thereon by comparing the stored data to the retained data in the random access volatile memory;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

2. (Previously presented) The system of Claim 1, wherein the FTL flash translation layer is a software module, or a firmware module containing software updates.

3. (Currently Amended) The system of Claim 1, wherein at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller.

4. (Previously presented) The system of Claim 1, wherein the MLC and SLC nonvolatile memory elements comprise flash memory.

5. (Cancelled)

6. (Cancelled)

7. (Currently Amended) The system of Claim 1, wherein the random access volatile memory ~~element~~ is dynamic random access memory.

8. (Currently Amended) The system of Claim 1, wherein the random access volatile memory ~~element~~ is static random access memory.

9. (Cancelled)

10. (Currently Amended) The system of Claim 1, wherein the controller, upon detection of a failure of the data integrity test, remaps the data to the ~~other of the MLC and~~ SLC nonvolatile memory element ~~elements~~.

11. (Cancelled)

12. (Previously presented) The system of Claim 10, wherein the SLC memory element has a higher endurance than the MLC memory element.

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Currently Amended) The system of Claim 1, wherein the MLC is a multilevel cell, wherein the multilevel cell stores [[n]] at least 2 bits per cell~~, wherein n is any integer greater than 1~~.

17. (Cancelled)

18. (Cancelled)

19. (Currently Amended) A system for storing data comprising:

memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multilevel cell (MLC) space and single level cell (SLC) space;

at least one controller to operate memory elements and associated memory space, and to maintain an address table in one or more of the memory elements;

at least one MLC nonvolatile memory element that can be mapped into the nonvolitile memory space;

at least one SLC nonvolatile memory element that can be mapped into the nonvolitile memory space;

at least one random access volatile memory ~~element~~;

PGR2025-00011/PHI EX. 1012 Page 73 of 98

the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory ~~elements~~ for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;

the controller performing a data integrity test on stored data in ~~a given one of~~ the MLC ~~and SLC~~ nonvolatile memory element ~~elements~~ after [[any]] at least a Write access operation [[is]] performed thereon by comparing the stored data to the retained data in the random access volatile memory;

wherein the address table maps logical and physical addresses adaptable to the system, wherein the mapping is performed as necessitated by the system to maximize lifetime, and wherein the mapping maps blocks, pages, or bytes of data in either volatile or nonvolatile, or both, memories; and

wherein a failure of the data integrity test performed by the controller results in a remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Currently Amended) The system of Claim 1, wherein the contents of frequently accessed ~~requests to~~ portions of the memory space ~~due to read or write, or read, modify, or write,~~

~~or data moves which contain frequent erases~~ are periodically moved from the MLC space to the SLC space.

26. (New) The system of Claim 1 wherein the MLC allows a single cell to store multiple bits.

REMARKS

Applicant has carefully reviewed the Office Action dated April 28, 2020. Applicant has amended claims 1, 3, 7, 8, 10, 16, 19, and 25. Claims 9, 13, 14, 17, 18, and 22-24 have been cancelled. New claim 26 has been added. Reconsideration and favorable action is respectfully requested.

I. Interview Summary

Applicant thanks the Examiner for the telephone interview conducted on October 7, 2020. Applicant was represented by Tim Bliss (#50,925), Greg Howison (#30,646), and inventor Mohan Rao. Amendments to claims 1 and 19 were discussed with respect to the prior art reference *Oribe*, as well as support for the amendments. No final conclusion was reached as to allowability of the amended claims, with the Examiner reserving the right for further search and consideration.

II. Rejections under 35 U.S.C. §112, first paragraph

All claims rejected under §112, first paragraph, have been cancelled except for Claim 25. Claim 25 has been amended to clarify the scope of the claim. Claim 25 is supported, for example, in paragraph [0028] of the specification. Accordingly, Applicant respectfully requests that the rejection of Claim 25 under §112, first paragraph, be withdrawn.

III. Rejections under 35 U.S.C. §112, second paragraph

All claims rejected under §112, second paragraph, have been cancelled except for Claim 25. Claim 25 has been amended to address the rejected elements. Accordingly, Applicant respectfully requests that the rejection of Claim 25 under §112, second paragraph, be withdrawn.

IV. Rejections under 35 U.S.C. §103

A. Claims 1-4, 7-10, 12-14, and 16-19

Claims 1-4, 7-10, 12-14, 16, 17, and 19 stand rejected under 35 USC §103(a) as being unpatentable over combinations of *Gorobets* in view of *Goodson* and *Oribe*. This rejection is respectfully traversed with respect to the claims as currently amended.

The Examiner has stated that the one element missing from the primary references, *Gorobets* in view of *Goodson,* is a lack of performing a data integrity check. The relies upon *Oribe* for the support of this element. In view of the newly added limitations to Claims 1 and 19, this rejection is respectfully traversed.

Claims 1 and 19, as amended, include the following limitation:

> *the controller controlling access of the MLC and SLC nonvolatile memory elements and the random access volatile memory for storage of data therein, the controller, in at least a Write access operation to the MLC nonvolatile memory element, operable to store data in the MLC nonvolatile memory element and retain such stored data in the random access volatile memory;*
>
> *the controller performing a data integrity test on stored data in the MLC nonvolatile memory element after at least a Write access operation performed thereon by comparing the stored data to the retained data in the random access volatile memory;*

This limitation requires that the nonvolatile memory element "retain" the stored data and then, during a data integrity test, the stored data for a Write access is "compared" to the stored data. Support for these amendments is found, for example, in paragraph [0027] and Fig. 3B.

This is to be contrasted with the refresh operation of *Oribe*, in which, in response to some determination that a bit error rate has exceeded a certain threshold, data will be remapped or moved from that block of memory to another block. There is no comparison operation, as that is

not required in order to determine the bit error rate of data. All that is required is to merely analyze the data and the error correction bits to determine the bit error rate.

In the currently amended claims, the actual data that is being written to the memory is retained in nonvolatile memory and then written to memory. This data is subsequently read from the memory and compared to the retained data. This operation is not some operation that can be carried out by a conventional cache, as that cache is typically only designed to handle one block of data. In the nonvolatile memory, in order to facilitate a compare operation, if an entire block is being written to with new data, that entire block has to be retained in one portion of the memory and then written to the memory, followed by a subsequent Read of the memory, requiring that block of data to be placed in an additional area of the nonvolatile memory, thus requiring at least two blocks of memory space in the nonvolatile memory. A refresh operation only requires one block of data cache.

Oribe does not disclose or suggest any type of compare operation as part of the data integrity operation. The refresh operation does not in any way "retain" data in any type of data cache for the purposes of a refresh operation.

Applicant submits that neither *Gorobets* nor *Oribe* can remap the address space to a different physical range of addresses "and transfer of data corresponding to the stored data to those remapped physical addresses." *Oribe* can only determine that a block of Flash memory has failed but, after such a determination, any data stored therein is lost. Since the operation of a Flash memory after accessing data therefrom requires an Erase operation, it is this Erase operation that provides the most stress on the Flash memory, thus causing a particular section to fail. Since neither *Gorobets* nor *Oribe* retain the data to be written for later comparison, neither suggests nor discloses such an operation, either singly or in combination. *Goodson* fails to remedy this deficiency.

Claims 2-4, 7, 8, 10, 12, 16, and 25 depend from and further limit claim 1, and therefore are allowable for at least the same reasons as claim 1.

B. New claim 26

Support for new claim 26 is found, for example, in paragraph [0010], second sentence. Claim 26 depends from and further limits claim 1, and therefore is allowable for at least the same reasons as claim 1.

V. Conclusion

For the reasons described above, Applicant submits that all pending claims are in condition for allowance. If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at tim@naifeh.com.

Recognizing that Internet communications are not secure, Applicant hereby authorizes the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application by video conferencing, instant messaging, or electronic mail. Applicant understands that a copy of these communications will be made of record in the application file.

Respectfully submitted,

/Bill R. Naifeh, Reg. No. 44,962/

Bill R. Naifeh
Registration No. 44,962

Law Office of Bill Naifeh
P.O. Box 803423
Dallas, TX 75380
972-726-9500
214-550-2542 (fax)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

40672 7590 01/27/2021

BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

EXAMINER
REIDLINGER, RONALD LANCE

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/27/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/006,299	06/12/2018	G.R. MOHAN RAO	VRVN.01.01.US4	6732

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	04/27/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

40672 7590 01/27/2021

BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/006,299	06/12/2018	G.R. MOHAN RAO	VRVN.01.01.US4	6732

TITLE OF INVENTION: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	04/27/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
REIDLINGER, RONALD LANCE	2824	365-185030

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PGR2025-00011/PHI EX. 1012 Page 81 of 98

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/006,299	06/12/2018	G.R. MOHAN RAO	VRVN.01.01.US4	6732

40672 7590 01/27/2021
BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380

EXAMINER	
REIDLINGER, RONALD LANCE	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/27/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/006,299	Applicant(s) RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to communication(s) submitted 08 October 2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are See Continuation Sheet . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/R.L.R./	/Richard Elms/
Examiner, Art Unit 2824	Supervisory Patent Examiner, Art Unit 2824

Continuation of 3. The allowed claim(s) is/are: 1-4,7-8,10,12,16,19 and 25-26

DETAILED ACTION

1. Claims 1-4, 7, 8, 10, 12, 16, 19, 25 and 26 are pending.

2. Claims 1 and 19 are independent.

Notice of Pre-AIA or AIA Status

3. The present application is being examined under the pre-AIA first to invent provisions.

Response to Arguments

4. Applicant's arguments, see Remarks pp. 7-10 § II, III and IV, filed 08 October 2020, with respect to the rejections under pre-AIA 35 USC §§ 112, first paragraph, 112 second paragraph and 103(a) have been fully considered and are persuasive. All outstanding rejections have been withdrawn.

Allowable Subject Matter

5. Claims 1-4, 7, 8, 10, 12, 16, 19, 25 and 26 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claims 4, 7, 8, 10, 12, 16, 25 and 26, see Applicant's Remarks § IV pp. 8-9. See also the pertinent prior art below.

Regarding claim 19, see Applicant's Remarks § IV pp. 8-9. See also the pertinent prior art below.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Pertinent Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Miyachi et al. (US 8,140,800 B2) teach generally in the background about Read after Write (RAW) which retains data in the cache (typically volatile) and compares it to data written to the HDD (nonvolatile) to ensure the data is written reliably and correctly. Miyachi et al. fail to teach writing to a

MLC portion and conducting RAW and then remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance if failing RAW.

Lee (US 7,505,338 B2) teaches typical verification of programming i.e. reading to ensure the proper threshold voltage is programmed into the memory cell and comparing that data with what is temporarily stored in the page buffer. See col. 2 ll. 3-17 Lee further teaches that the cell can be changed to SLC if the program operation fails verification. See col. 6 ln. 64 to col. 7 ln. 8. Lee fails to teach remapping of the address space to a different physical range of addresses and transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test to achieve enhanced endurance.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to R LANCE REIDLINGER whose telephone number is (571)270-7353. The examiner can normally be reached on M-F 1:00pm - 10:00pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rich T Elms can be reached on 571.272.1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available

through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R.L.R./
Examiner, Art Unit 2824

/Richard Elms/
Supervisory Patent Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 16/006,299	Applicant(s)/Patent Under Reexamination RAO, G.R. MOHAN	
	Examiner R LANCE REIDLINGER	Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-8140800-B2	03-2012	Miyachi; Kazunari	G06F11/1076	711/165
*	B	US-7505338-B2	03-2009	Lee; Bong-Ryeol	G11C11/5621	365/185.09
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/006,299	RAO, G.R. MOHAN
	Examiner	**Art Unit**
	R LANCE REIDLINGER	2824

CPC							
Symbol						**Type**	**Version**
G11C	/	11	/	5635		F	2013-01-01
G06F	/	12	/	0246		I	2013-01-01
G11C	/	16	/	3495		I	2013-01-01
G06F	/	11	/	1068		I	2013-01-01
G06F	/	11	/	1072		I	2013-01-01
G11C	/	11	/	5621		I	2013-01-01
G11C	/	11	/	5678		I	2013-01-01
G11C	/	29	/	52		I	2013-01-01
G11C	/	29	/	76		I	2013-01-01
G11C	/	16	/	16		I	2013-01-01
G06F	/	2212	/	7202		A	2013-01-01
G11C	/	2211	/	5641		A	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

/R LANCE REIDLINGER/ Examiner, Art Unit 2824	16 January 2021	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/Richard Elms/ Supervisory Patent Examiner, Art Unit 2824	22 January 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3A & 3B

U.S. Patent and Trademark Office — Part of Paper No.: 20210116

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/006,299	RAO, G.R. MOHAN
	Examiner	Art Unit
	R LANCE REIDLINGER	2824

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G11C11/56	/	11	/	56
G06F12/02	/	12	/	02
G11C16/34	/	16	/	34
G06F11/10	/	11	/	10
G11C29/52	/	29	/	52
G11C29/00	/	29	/	00
G11C16/16	/	16	/	16

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

/R LANCE REIDLINGER/ Examiner, Art Unit 2824	16 January 2021	Total Claims Allowed:	
(Assistant Examiner)	(Date)	12	
/Richard Elms/ Supervisory Patent Examiner, Art Unit 2824	22 January 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3A & 3B

U.S. Patent and Trademark Office — Part of Paper No.: 20210116

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/006,299	RAO, G.R. MOHAN
	Examiner	**Art Unit**
	R LANCE REIDLINGER	2824

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	7	10	12	19										
2	2		11		20										
3	3	8	12		21										
4	4		13		22										
	5		14		23										
	6		15		24										
5	7	9	16	10	25										
6	8		17	11	26										
	9		18												

/R LANCE REIDLINGER/ Examiner, Art Unit 2824	16 January 2021	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/Richard Elms/ Supervisory Patent Examiner, Art Unit 2824	22 January 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3A & 3B

U.S. Patent and Trademark Office — Part of Paper No.: 20210116

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/006,299	RAO, G.R. MOHAN
	Examiner	Art Unit
	R LANCE REIDLINGER	2824

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F 11/1068, 11/1072, 12/0246, 2212/7202	01/16/2021	RLR
G11C 11/5621, 11/5635, 11/5678, 16/16, 16/3495, 29/52, 29/79, 2211/5641	01/16/2021	RLR

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Reviewed Prosecution & Search History of parent applications	01/19/2019	RLR
Searched for new limitations	12/09/2019	RLR
updated Search for new limitations	01/16/2021	RLR

/R LANCE REIDLINGER/ Examiner, Art Unit 2824	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/006,299	RAO, G.R. MOHAN
	Examiner	Art Unit
	R LANCE REIDLINGER	2824

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
G06F	11/1068, 11/1072, 12/0246, 2212/7202	01/16/2021	RLR
G11C	11/5621, 11/5635, 11/5678, 16/16, 16/3495, 29/52, 29/79, 2211/5641	01/16/2021	RLR

/R LANCE REIDLINGER/ Examiner, Art Unit 2824	

Bibliographic Data

Application No: 16/006,299

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /R LANCE REIDLINGER/ Examiner's Signature | Initials

Title: LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
06/12/2018	365	2824	VRVN.01.01.US4
RULE			

APPLICANTS

VERVAIN, LLC, Dallas, TX, UNITED STATES

INVENTORS

G.R. MOHAN RAO, ALLEN, TX, UNITED STATES

CONTINUING DATA

This application is a CON of 14950553 11/24/2015 PAT 9997240

14950553 is a CON of 14525411 10/28/2014 PAT 9196385

14525411 is a DIV of 13455267 04/25/2012 PAT 8891298

13455267 has PRO of 61509257 07/19/2011

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

06/29/2018

STATE OR COUNTRY

UNITED STATES

ADDRESS

BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380
UNITED STATES

FILING FEE RECEIVED

$785

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	207	fail$3 near3 (program$4 writ$3) with Single adj (level bit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 22:12
S170	222	compar$3 with retain$3 near2 data with (writ$3 program$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:00
S171	21	S170 same cache	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:00
S172	5,699	Read adj after adj write	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:04
S173	0	S170 same SLC same (MLC TLC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:05
S174	2	S170 same (MLC TLC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:05
S175	7	fail$3 near3 (verif$3 verification) with remap$4 with SLC	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:13
S176	15	fail$3 near3 (verif$3 verification) with SLC	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:14
S177	59	fail$3 near3 (verif$3 verification) with Single adj (level bit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:17
S178	50	fail$3 near3 (program$4) with remap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:21
S179	14	fail$3 near3 (verif$3 verification) with remap$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:21
S180	63	fail$3 near3 (program$4) with SLC	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:22
S182	31	S180 and (verif$3 verification)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/01/16 17:23

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	34,242	(G11C11/5635 or G11C16/16 or G06F11/1068 or G06F11/1072 or G11C11/5621 or G11C11/5678 or G11C29/52 or G11C29/76 or G06F12/0246 or G11C16/3495 or G11C2211/5641 or G06F2212/7202).cpc.	US-PGPUB; USPAT	OR	ON	2021/01/16 22:16
L3	366,139	map$4.clm.	US-PGPUB; USPAT	OR	ON	2021/01/16 22:19
L4	37,268	(MLC (multi multiple plural) adj (level state bit)).clm.	US-PGPUB; USPAT	OR	ON	2021/01/16 22:20
L5	12,262	(SLC single adj (level state bit)).clm.	US-PGPUB; USPAT	OR	ON	2021/01/16 22:20
L7	417,924	test$4.clm.	US-PGPUB; USPAT	OR	ON	2021/01/16 22:21
L8	128,591	volatile.clm.	US-PGPUB; USPAT	OR	ON	2021/01/16 22:21
L9	9,829	address adj2 table.clm.	US-PGPUB; USPAT	OR	ON	2021/01/16 22:22
L10	0	3 4 5 7 8 9	US-PGPUB; USPAT	AND	ON	2021/01/16 22:22
L12	16	3 4 5 8 9	US-PGPUB; USPAT	AND	ON	2021/01/16 22:27
L13	12	2 and 12	US-PGPUB; USPAT	AND	ON	2021/01/16 22:27

1/16/2021 10:29:50 PM
C:\Users\rreidlinger\Documents\EAST\Workspaces\16006299.wsp

To: patents@naifeh.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 40672

Jan 27, 2021 04:26:35 AM

Dear PAIR Customer:

BILL R. NAIFEH
PO BOX 803423
DALLAS, TX 75380
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 40672 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
16006299	NOA	01/27/2021	VRVN.01.01.US4
	892	01/27/2021	VRVN.01.01.US4

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM