

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PHISON ELECTRONICS CORPORATION,

Petitioner

v.

VERVAIN, LLC,

Patent Owner

Post-Grant Review Case No. PGR2025-00011

Patent 11,967,370

PETITION FOR POST-GRANT REVIEW OF

U.S. PATENT NO. 11,967,370

TABLE OF CONTENTS

I.	INTRODUCTION:	1
II.	MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1):	6
	A. REAL PARTY-IN-INTEREST UNDER 37 C.F.R. § 42.8(B)(1):	6
	B. RELATED MATTERS UNDER 37 C.F.R. § 42.8 (B)(2):	6
	C. LEAD AND BACK UP COUNSEL UNDER 37 C.F.R. § 42.8(B)(3):	7
	D. SERVICE INFORMATION UNDER 37 C.F.R. § 42.8(B)(4):	7
III.	ADDITIONAL REQUIREMENTS:	8
	A. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15:	8
	B. TIMING UNDER 37 C.F.R. § 42.202:	8
	C. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.204(A):	8
IV.	NAND FLASH TECHNOLOGY BACKGROUND	8
	A. CHARACTERISTIC NATURE OF NAND FLASH MEMORY	9
	B. CHARACTERISTIC NAND FLASH MEMORY MANAGEMENT	12
	C. INTRODUCTION OF MLC AND SLC FLASH	12
	D. KNOWN HYBRID USE OF SLC AND MLC NAND FLASH MODULES WITH STRATEGIES OF PREFERENTIAL MAPPING, WEAR LEVELING AND ERROR MANAGEMENT	14
V.	THE ‘370 PATENT: 2012 COMMON SPECIFICATION AND 2018 CHANGE	16
	A. THE COMMON SPECIFICATION RECITED AND RELIED ON A KNOWN HYBRID SYSTEM OF MLC AND SLC MODULES AND ITS OPERATION.	17
	B. THE FIRST THREE LIFETIME PATENTS ON OPERATION OF A KNOWN HYBRID MLC-SLC NAND FLASH MEMORY SYSTEM.	18

C.	2018 ‘300 PATENT ABSTRACTION OF THE DISCLOSED HYBRID MLC-SLC FLASH SYSTEM.....	19
D.	FURTHER RESHUFFLING	21
E.	THE CHALLENGED CLAIMS OF THE ‘370 PATENT:	22
F.	PERSON OF ORDINARY SKILL IN THE ART	26
VI.	37 C.F.R. § 42.204(B)(3): CLAIM CONSTRUCTION	26
VII.	GROUND 1: THE CHALLENGED CLAIMS LACK A WRITTEN DESCRIPTION DESCRIBING THE CLAIMED SUBJECT MATTER IN ACCORDANCE WITH 35 U.S.C. § 112(A).....	30
A.	THE CHALLENGED CLAIMS LIMITED BY “MEMORY SPACE” ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A).	31
B.	THE CHALLENGED CLAIMS LIMITED BY “MEMORY ELEMENT” ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A).	31
C.	THE CHALLENGED CLAIMS LIMITED BY “AT LEAST ONE . . . MEMORY ELEMENT” ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A) AND FAIL TO RECITE A USEFUL SYSTEM FOR STORING DATA.....	32
D.	THE CHALLENGED CLAIMS LIMITED BY “TRANSFER” OF “STORED DATA” TO SLC ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A) AND INOPERATIVE.....	33
E.	CLAIMS 6 TO 10, FOR ALTERNATIVE TECHNOLOGIES SUBSTITUTED FOR MLC OR SLC, ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A).	34
F.	CLAIMS 14 AND 15, FOR “TEMPORARY TRANSFER,” ARE UNSUPPORTED UNDER 35 U.S.C. § 112(A).	34
VIII.	GROUND 2: THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B).	35
A.	THE CHALLENGED CLAIMS LIMITED BY “MEMORY SPACE” ARE INDEFINITE UNDER 35 U.S.C. § 112(B).	36
B.	THE CHALLENGED CLAIMS LIMITED BY “MEMORY ELEMENT” ARE INDEFINITE UNDER 35 U.S.C. § 112(B).	36

C. THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B) FOR THEIR RECITATION OF A “CONTROLLER” LIMITED BY FUNCTIONS IN THE CLAIMS THAT ARE UNSUPPORTED BY STRUCTURE (PHYSICAL OR ALGORITHMIC) IN THE SPECIFICATION.	36
D. THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B) BECAUSE THEY RECITE METHOD STEPS IN A CLAIM TO A SYSTEM.	38
E. THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(B) BECAUSE IT IS UNCERTAIN ON WHAT AND WHEN THE RECITED DATA INTEGRITY TEST IS TO BE PERFORMED.	40
IX. GROUND 3: CLAIMS 1-18 ARE OBVIOUS UNDER 35 U.S.C. § 103 OVER GAVENS IN VIEW OF POSITA KNOWLEDGE.	42
A. CLAIM 1 IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA.	43
1. [1a] an MLC non-volatile memory space including at least one MLC non-volatile memory element;.....	45
2. [1a] an SLC non-volatile memory module space including at least one SLC non-volatile memory element; and	46
3. [1c] a controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element wherein the controller is adapted to:	48
4. [1d] a) maintain an address map of the MLC and SLC non-volatile memory spaces, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element;.....	48
5. [1e] b) [1e1] determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test performed at the controller based upon received data retained at the controller and which received data is stored in the at least one MLC non-volatile memory element as stored data,	

and, in an event of such a failure, the controller [1e2] remaps the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element and, [1e3] the stored data is transferred from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element. 52

- B. CLAIMS 2, 3, 12 AND 13, LIMITING “MINIMUM QUANTA OF [LOGICAL] ADDRESSES” TO ONE BLOCK OR ONE PAGE AND “MEMORY ELEMENTS” TO BLOCKS OR PAGES WITH PHYSICAL ADDRESSES, ARE OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA. 54**
- C. CLAIMS 4 AND 5, WITH MLC AND SLC ELEMENTS LIMITED TO NAND FLASH, ARE OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA. 56**
- D. CLAIMS 6 THROUGH 10, LIMITED TO SUBSTITUTION OF ALTERNATIVE TECHNOLOGIES FOR MLC AND SLC, ARE OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA. 57**
- E. CLAIM 11, LIMITED TO THE CONTROLLER “TRANSFERRING CONTENT ON A PERIODIC BASIS,” IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA..... 58**
- F. CLAIMS 14 AND 15, LIMITING “TRANSFER” TO A BEING “TEMPORARY,” ARE OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA..... 59**
- G. CLAIM 16, LIMITING “OPERATIONS OF THE CONTROLLER” TO “ENHANCE A LIFETIME” OF THE RECITED MLC AND SLC MEMORY ELEMENTS, IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA..... 61**
- H. CLAIM 17, LIMITED TO THE RECITED DATA INTEGRITY TEST PERFORMED “DURING A WRITE OPERATION,” IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA. . 62**
- I. CLAIM 18 IS OBVIOUS OVER GAVENS, INCLUDING INCORPORATED REFERENCES, IN VIEW OF KNOWLEDGE OF THE POSITA..... 63**

1.	[18a] providing an MLC non-volatile memory space including at least one MLC non-volatile memory element;.....	64
2.	[18b] providing an SLC non-volatile memory space including at least one SLC non-volatile memory element; and	64
3.	[18c] maintaining, using a controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element;.....	64
4.	[18d] an address map of the MLC and SLC non-volatile memory spaces, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element;.....	65
5.	[18e] [18e1]determining, using the controller, if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test performed at the controller based upon received data retained at the controller and which received data is stored in the at least one MLC non-volatile memory element as stored data; in an event of such a failure, [18e2] remapping, using the controller, the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element; and [18e3] transferring the stored data from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element using the controller.	66
X.	THE PENDING LITIGATIONS IN THE WESTERN DISTRICT OF TEXAS DO NOT WARRANT DENYING INSTITUTION.....	67
XI.	CONCLUSION	71

TABLE OF AUTHORITIES

CASES

Amgen Inc. v. Sanofi,

598 U.S. 594 (2023)-----31

Apple Inc. v. Fintiv, Inc.,

IPR2020-00019 (P.T.A.B. Mar. 20, 2020)----- 67, 68

Aristocrat Techs. Austl. Pty Ltd. v. Int’l Game Tech.,

521 F.3d 1328 (Fed. Cir. 2008)-----37

Egenera, Inc. v. Cisco Sys.,

972 F.3d 1367 (Fed. Cir. 2020)-----37

Ergo Licensing, LLC v. CareFusion 303, Inc.,

673 F.3d 1361 (Fed. Cir. 2012)-----37

IPXL Holdings, LLC v. Amazon.com, Inc.,

430 F.3d 1377 (Fed. Cir. 2005)-----39

KSR Int’l Co. v. Teleflex Inc.,

550 U.S. 398 (2007)-----42

Media Rights Techs., Inc. v. Capital One Fin. Corp.,

800 F.3d 1366 (Fed. Cir. 2015)-----37

Nautilus, Inc. v. Biosig Instruments,

572 U.S. 898 (2014)-----35

Phillips v. AWH Corp.,

415 F.3d 1303 (Fed. Cir. 2005). -----26

Rain Computing, Inc. v. Samsung Electronics America, Inc.,

989 F.3d 1002 (Fed. Cir. 2021)-----37

Rembrandt Data Technologies, LP v. AOL, LLC,

641 F.3d 1331 (Fed. Cir. 2011)-----40

Vervain, LLC v. Kingston Technology Company, Inc., et al,

No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024)-----3, 69

Vervain, LLC v. Micron Technology, Inc., et al,

No. 6:21-cv-00487 (W.D. Tex. filed May 10, 2021) ----- 3

Vervain, LLC v. Phison Electronics Corp.,

No. 1:24-cv-00259 (W.D. Tex. filed March 8, 2024)----- 3, 6, 68, 69

Vervain, LLC v. Western Digital Corp., et al.,

No. 6:21-cv-00488 (W.D. Tex. filed May 10, 2021) ----- 3

STATUTES

35 U.S.C. § 101 ----- 39, 71

35 U.S.C. § 103 ----- 25, 42, 71

35 U.S.C. § 112(a)-----	passim
35 U.S.C. § 112(b) -----	passim
35 U.S.C. § 112(f)-----	37

OTHER AUTHORITIES

37 C.F.R. § 42.6(e) -----	72, 73
37 C.F.R. § 42.8(a)(1)-----	6
37 C.F.R. § 42.8(b)(1) -----	6
37 C.F.R. § 42.8(b)(2) -----	6
37 C.F.R. § 42.8(b)(3) -----	7
37 C.F.R. § 42.8(b)(4) -----	7
37 C.F.R. § 42.10(b) -----	7
37 C.F.R. § 42.15 -----	8
37 C.F.R. § 42.24(a)(ii)-----	73
37 C.F.R. § 42.200(b)-----	26
37 C.F.R. § 42.202 -----	8
37 C.F.R. § 42.204(a) -----	8
37 C.F.R. § 42.204(b)(3) -----	26
37 C.F.R. § 42.204(b)(4) -----	30
37 C.F.R. § 42.204(b)(5) -----	30

LIST OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,967,370 titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1002	Declaration of Carl Sechen, Ph.D.
1003	U.S. Provisional Application No. 61/509,257, titled “IMPROVED LIFETIME MIXED LEVEL NAND FLASH SYSTEM” by Rao
1004	U.S. Patent No. 7,855,916, titled “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES,” to Rao
1005	U.S. Patent No. 8,891,298, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1006	Excerpts from prosecution history of ’298 patent
1007	U.S. Patent No. 9,196,385, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1008	Excerpts from prosecution history of ’385 patent
1009	U.S. Patent No. 9,997,240, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1010	Excerpts from prosecution history of ’240 patent
1011	U.S. Patent No. 10,950,300, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao
1012	Excerpts from prosecution history of ’300 patent
1013	U.S. Patent No. 11,830,546, titled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” to Rao

1014-1024	<i>Intentionally omitted</i>
1025	Excerpts from Rino Micheloni, et al., <i>INSIDE NAND FLASH MEMORIES</i> (Springer 2010)
1026	Excerpts from <i>NONVOLATILE MEMORY TECHNOLOGIES WITH EMPHASIS ON FLASH: A COMPREHENSIVE GUIDE TO UNDERSTANDING AND USING NVM DEVICES</i> (Joe E. Brewer & Manzur Gill eds. Wiley-IEEE Press 2008)
1027	Excerpts from <i>MICROSOFT COMPUTER DICTIONARY</i> (5 th ed. 2002)
1028-1029	<i>Intentionally omitted</i>
1030	Yu Cai et al., <i>Program Interference in MLC NAND Flash Memory: Characterization, Modeling and Mitigation</i> (IEEE 2013)
1031	Kang-Deog Suh et al., <i>A 3.3 V 32 Mb NAND Flash Memory with Incremental Step Pulse Programming Scheme</i> , 30 IEEE J. Solid State Circuits 1149 (Nov. 1995)
1032	Eitan Yaakobi et al., <i>Error Characterization and Coding Schemes for Flash Memories</i> (2010 IEEE Globecom Workshops, Miami, FL at 1856-60)
1033	Evans, Chris, “Enterprise MLC: How flash vendors are boosting MLC write endurance” (June 3, 2011)
1034	Nelson Duann, <i>SLC & MLC Hybrid</i> (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008)
1035	Ashish Jagmohan et. al., <i>Adaptive Endurance Coding for NAND Flash</i> (2010 IEEE Globecom Workshops, Miami, FL at 1841-45)
1036	Sungjin Lee et al., <i>FlexFS: A Flexible Flash File System for MLC NAND Flash Memory</i> (2009 USENIX Annual Technical Conference, San Diego, CA, June 14-19, 2009)

1037	Minyoung Sung & Kanghee Kim, <i>Asymmetric Flash Volume Management</i> , 58 <i>IEEE Transactions on Consumer Electronics</i> 455 (May 2012)
1038	Greg Atwood et al., Intel StrataFlash™ <i>Memory Technology Overview</i> , Intel Technology J. (Q4 1997)
1039	Taehee Cho et al., “A 3.3 V 1 Gb multi-level NAND flash memory with non-uniform threshold voltage distribution,” 2001 <i>IEEE International Solid-State Circuits Conference. Digest of Technical Papers</i> , ISSCC (Cat. No.01CH37177) (2001)
1040	U.S. Patent No. 6,456,528, titled for “SELECTIVE OPERATION OF A MULTI-STATE NON-VOLATILE MEMORY SYSTEM IN A BINARY MODE” to Chen
1041	U.S. Patent No. 8,078,794, titled “HYBRID SSD USING A COMBINATION OF SLC AND MLC FLASH MEMORY ARRAYS,” to Lee et al.
1042	U.S. Patent Appl. Pub. No. 2008/0140918, titled “HYBRID NON-VOLATILE SOLD STATE MEMORY SYSTEM” by Sutardja
1043	U.S. Patent Appl. Pub. No. 2009/0327591, titled “SLC-MLC COMINATION FLASH STORAGE,” by Moshayedi
1044	U.S. Patent Appl. Pub. No. 2010/0172179, titled “SPARE BLOCK MANAGEMENT OF NON-VOLATILE MEMORIES,” by Gorobets et al.
1045	U.S. Patent No. 8,634,240, titled “NON-VOLATILE MEMORY AND METHOD WITH ACCELERATED POST-WRITE READ TO MANAGE ERRORS,” to Gavens et al.
1046	U.S. Patent No. 8,806,301, titled “DATA WRITING METHOD FOR A FLASH MEMORY, AND CONTROLLER AND STORAGE SYSTEM USING THE SAME,” to Yu et al.

1047	U.S. Patent Appl. Pub. No. 2010/0115192, titled “WEAR LEVELING METHOD FOR NON-VOLATILE MEMORY DEVICE HAVNG SINGLE AND MULTI LEVEL MEMORY CELL BLOCKS,” by Lee
1048	U.S. Patent Appl. Pub. No. 2011/0271043, titled “SYSTEM AND METHOD FOR ALLOCATING AND USING SPARE BLOCKS IN A FLASH MEMORY,” to Segal et al.
1049	U.S. Patent Appl. Pub. No. 2011/0153912, titled “MAINTAINING UPDATES OF MULTI-LEVEL NON-VOLATILE MEMORY IN BINARY NON-VOLATILE MEMORY,” by Gorobets et al.
1050	U.S. Patent No. 5,930,167, titled “MULTI-STATE NON-VOLATILE FLASH MEMORY CAPABLE OF BEING ITS OWN TWO STATE WRITE CACHE,” to Lee et al.
1051	U.S. Patent Appl. Pub. No. 2010/0172180, titled “NON-VOLATILE MEMORY AND METHOD WITH WRITE CACHE PARTITIONING,” by Paley et al.
1052	<i>Intentionally omitted</i>
1053	U.S. Patent Appl. Pub. No. 2009/0268513, titled “MEMORY DEVICE WITH DIFFERENT TYPES OF PHASE CHANGE MEMORY,” by De Ambroggi et al.
1054	U.S. Patent Appl. Pub. No. 2009/0307418, titled “MULTI-CHANNEL HYBRID DENSITY MEMORY STORAGE DEVICE AND CONTROL METHOD THEREFOR,” by Chen et al.
1055	U.S. Patent Appl. Pub. No. 2010/0058018, “MEMORY SCHEDULER FOR MANAGING INTERNAL MEMORY OPERATIONS,” by Kund et al.
1056	U.S. Patent App. Pub. No. 2009/0172267, “REFRESH METHOD OF A FLASH MEMORY,” by Oribe et al.

1057	U.S. Patent No. 5,936,971, titled “MULTI-STATE FLASH EEPROM SYSTEM WITH CACHE MEMORY, to Harari et al.
1058	PCT Pub. No. WO 03/027828, “METHOD OF WRITING DATA TO NON-VOLATILE MEMORY,” by Gorobets et al.
1059-1060	<i>Intentionally omitted</i>
1061	Duane H. Oto et al., <i>High-Voltage Regulation and Process Considerations for High-Density 5 V-Only E²PROM’s</i> , SC-18 IEEE J. Solid State Circuits 532 (Oct. 1983)
1062	Gheorghe Samachisa et al., <i>A 128K Flash EEPROM Using Double-Polysilicon Technology</i> , SC-22 IEEE J. Solid State Circuits 676 (Oct. 1987)
1063	Masaki Momodomi et al., <i>An Experimental 4-Mbit CMOS EEPROM with a NAND-Structured Cell</i> , 24 IEEE J. Solid State Circuits 1238 (Oct. 1989)
1064	Tae-Sun Chung et al., <i>A survey of Flash Translation Layer</i> , 55 J. Systems Architecture 332-43 (2009)
1065	Yoshihisa Iwata et al., <i>A High-Density NAND EEPROM with Block-Page Programming for Microcomputer Applications</i> , 25 IEEE J. Solid-State Circuits 417 (Apr. 1990)
1066	Simona Boboila and Peter Desmoyers, <i>Write Endurance in Flash Drives: Measurements and Analysis</i> , Usenix Conference (Feb. 2010)
1067	SiliconSystems, <i>Increasing Flash SSD Reliability</i> , StorageSearch.com (April 2005)
1068	Taehee Cho et al., <i>A Dual-Mode NAND Flash Memory: 1-Gb Multilevel and High-Performance 512-Mb Single Level Modes</i> , 36 IEEE J. Solid State Circuits 1700 (Nov. 2001)

1069	Ken Takeuchi, <i>A Multipage Cell Architecture for High-Speed Programming Multilevel NAND Flash Memories</i> , 33 IEEE J. Solid-State Circuits 1228 (Aug. 1998)
1070	Garth Goodson & Rahul Iyer, <i>Design Tradeoffs in a Flash Translation Layer</i> , HPCA [High Performance Computer Architecture] WEST 2010 Conference, Bangalore, India
1071	Taeho Kgil et al., <i>Improving NAND Flash Based Disk Caches</i> , Int’l Symposium on Computer Architecture 327 (IEEE 2008)
1072	Seongcheol Hong & Dungkun Shin , <i>NAND Flash-based Disk Cache Using SLC/MLC Combined Flash Memory</i> , 21, 22 (2010 Int’l Workshop on Storage Network Architecture and Parallel I/O)
1073-1079	<i>Intentionally omitted</i>
1080	Docket list for <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex., filed March 8, 2024)
1081	Docket list for <i>Vervain, LLC v. Kingston Technology Company, Inc.</i> , No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024)
1082	First Amended Complaint, Doc. No. 9 in <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex.)
1083	Signed Agreed Scheduling Order, Doc. No. 16 in <i>Vervain, LLC v. Phison Electronics Corp.</i> , No. 1:24-cv-00259 (W.D. Tex.)

I. INTRODUCTION:

Phison Electronics Corporation (“Phison” or “Petitioner”) requests post-grant review (“PGR”) of claims 1-18 (the “Challenged Claims”) of U.S. Patent No. 11,967,370, entitled “LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” issued Apr. 23, 2024 (“the ‘370 patent”) (Ex. 1001), assigned to Vervain, LLC (“Vervain” or “Patent Owner”). The ‘370 patent was issued on the sixth continuation application¹ of a chain of continuations from U.S. Pat. Appl. No. 13/455,267, filed on April 25, 2012,² which claimed priority of U.S. Provisional

¹ U.S. Appl. No. 18/390,193, which was filed Dec. 20, 2023.

² This application issued as U.S. Patent No. 8,891,298 (“the “298 patent,” Ex. 1005). It was followed by continuation U.S. Appl. No. 14/525,411, filed Oct. 28, 2014, issued as U.S. Patent No. 9,196,385 (the “385 patent,” Ex. 1007), by continuation U.S. Appl. No. 14/950,553, filed Nov. 24, 2015, issued as U.S. Patent No. 9,997,240 (the “240 patent,” Ex. 1009), by continuation U.S. Appl. No. 16/006,299, filed Jun. 12, 2018, issued as U.S. Patent No. 10,950,300 (the “300 patent,” Ex. 1011), by U.S. Appl. No. 17/203,385, filed Mar. 16, 2021, issued as U.S. Patent No. 11,830,546 (the “546 patent,” Ex. 1013), by continuation U.S. Appl. No. 18/387,546, issued as U.S. Patent No. 11,967,369 (the “369 patent”), leading by continuation to the ‘370 patent.

App. No. 61/509,257, entitled “IMPROVED LIFETIME MIXED LEVEL NON-VOLATILE MEMORY SYSTEM,” filed on July 19, 2011 (“Provisional,” Ex. 1003) and incorporated by reference U.S. Patent No. 7,855,916 (“Rao ‘916,” Ex. 1004).^{3, 4}

A branch continuation application issued as U.S. Patent Nos. 11,854,612 (“the ‘612 patent”), and two later continuation applications so far issued as U.S. Patents Nos. 12,119,054 and 12,136,455. The first eight of these ten “Lifetime Patents,” all based on the same April 25, 2012, specification claiming July 19, 2011, priority, are currently asserted (First Amended Complaint, Ex. 1082, leave to amend granted, Ex. 1080 [Dec. 18, 2024, entry]) by Vervain against Phison in *Vervain, LLC v. Phison*

³ (U.S. Pat. Appl. No. 12/256,362, incorporated in the ‘370 patent [1:38-45], along with U.S. Pat. Appl. No. 12/915,177, both entitled, “NONVOLATILE MEMORY SYSTEMS WITH EMBEDDED FAST READ AND WRITE MEMORIES,” the latter issued as U.S. Patent No. 8,194,452.)

⁴ Forty information disclosure statement (“IDS”) documents were filed with the April 25, 2012, ‘298 application (cited here by “IDS#_” in reference to their listing on the three IDSs filed that day [Ex. 1006 at 26-36]).

Electronics Corp., No. 1:24-cv-00259 (W.D. Tex. originally filed March 8, 2024).⁵

Petitioner has petitioned for reviews by this Board in seven pending proceedings.⁶

⁵ All are asserted against a customer of Phison in *Vervain, LLC v. Kingston Technology Company, Inc., Kingston Digital, Inc., and Kingston Technology Corp.*, No. 1:24-cv-00254 (W.D. Tex. filed March 7, 2024). The first four patents were asserted previously in *Vervain, LLC v. Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Technology Texas, LLC*, No. 6:21-cv-00487 (W.D. Tex. filed May 10, 2021, settled April 21, 2023) and *Vervain, LLC v. Western Digital Corp., et al*, No. 6:21-cv-00488 (W.D. Tex. filed May 10, 2021, settled Aug. 8, 2023). Micron petitioned this Board for *inter partes* review in *Micron Technology, Inc. v. Vervain, LLC*, IPR2021-001547 (‘298 patent), IPR2021-001548 (‘385 patent), IPR2021-001549 (‘240 patent), and IPR2021-001550 (‘300 patent), which were instituted on April 8 and 11, 2022, and terminated on April 4, 2023, on settlement after hearing but prior to final written decision.

⁶ *Phison Electronics Corp. v. Vervain, LLC*, PGR2024-00047 (‘546 patent, accorded filing date Aug. 27, 2024 [Paper No. 5]), PGR2024-00048 (‘612 patent accorded filing date Sept. 25, 2024 [Paper No. 5]), IPR2025-00212 (‘298 patent, accorded filing date Nov. 25, 2024 [Paper No. 5]), IPR2025-00213 (‘385 patent, filed Dec. 4,

This Petition demonstrates by a preponderance of the evidence that the Challenged Claims are unpatentable as one of ten patent groups that, by variations of words ambiguously or never used in the common specification, lay claim to a functionally described, known by 2011 “data integrity test” operation for hybrid systems of “MLC” and “SLC” NAND flash “modules” established a decade earlier. Although the first three Lifetime Patents claimed this operation and a variation of known wear leveling use of a “controller” for the known MLC and SLC systems (distinguished in prosecution only by a recited wear leveling “transfer”), beginning in 2018, the remaining Lifetime Patents, on the same 2012 functional description, claimed abstract “memory spaces” with “MLC” and “SLC” “memory elements” operated with the “data integrity test.” In the ‘300 prosecution, a previously undistinguished, but NAND-flash common “random access volatile memory” (“RAVM”) was elevated then demoted from an “element” in the “memory space” (which has no practical function). The ‘546 patent re-elevated the RAVM and added the also previously undistinguished, but NAND-flash common “controller memory” – but not to the “memory space.” The subject ‘370 patent claims reshuffled “memory space” and “memory element” without the RAVM and “controller memory” – and,

2024), IPR2025-00214 (‘240 patent, filed Dec. 6, 2024), IPR2025-00215 (‘300 patent, filed Dec. 17, 2024) and PGR2025-00010 (‘369 patent, filed Dec. 26, 2024).

in *both* independent claims, recited a nonsensical “**transfer**” to SLC of data found to have **failed** the recited data integrity test. Except for that nonsensical recitation, none of these variations have any technological import – as they may not, in view of the 2012 common “support” of a two-paragraph functional (and ambiguous) description of “a method for utilizing a NAND flash memory system.” The variations serve only as a veil for verbal legerdemain in procurement of now ten and 2024 assertion of eight Lifetime Patents, all based on the same 2012 inadequate, functional description of a known in 2011 NAND flash error management operation.

Independent system claim 1 and method claim 18 recharacterize the common specification’s and first three patents’ known MLC and SLC modules – comprising “individually erasable [flash] blocks” – as “memory spaces” and “memory elements” with no import other than obfuscation. They recite a controller with admitted prior art logical-to-physical (“L2P”) address mapping necessary for NAND flash operation. They recite the controller’s operation of a data integrity test together with other recitations (except for a *wear leveling* “transfer”) previously found undistinguished from a prior art MLC-SLC system – with a *different* “**transfer**” recited *nonsensically* for the ‘370-claimed *data integrity test*.

These terms (and others in the dependent claims) themselves and in recited combination invalidate the Challenged Claims for lack of support and/or operability (Ground 1) and for indefiniteness (Ground 2). Were the Challenged Claims to

survive these challenges – *and the recited “transfer” corrected* – to the extent understood by a POSITA, they are known prior art, exemplified by U.S. Patent No. 8,634,240 to Gavens et al. (“Gavens,” Ex. 1045) and its incorporated references, or obvious in view of the knowledge of the POSITA (Ground 4). Post-Grant Review of the Challenged Claims is eminently appropriate to stop the proliferation of bad patents such as the ‘370 patent, with their verbal variations of claims to the same well-known NAND flash technology.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1):

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1):

Petitioner Phison Electronics Corporation is the real party-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8 (b)(2):

As set forth further at note 5 *supra*, the ‘370 patent (along with seven other patents based on the same specification) is currently asserted by Vervain against Phison and its customer (separately) in the Western District of Texas. In the Phison case a claim construction hearing (on twelve terms proposed by Phison and its customer) is tentatively scheduled for January 9, 2025, and jury selection tentatively scheduled for December 15, 2025 (*Vervain, LLC v. Phison Electronics Corp.*, No. 1:24-cv-00259, Doc. No. 16 (W.D. Tex. July 15, 2024) (Exs. 1080 and 1083). Resolution of this proceeding may simplify that litigation and promote settlement.

C. Lead and Back Up Counsel Under 37 C.F.R. § 42.8(b)(3):

Pursuant to 37 C.F.R. § 42.8(b)(3), lead counsel for this Petition is Hsuanyeh Chang, PhD (Reg. No. 73,431) and back-up counsel are Stephen Y. Chow (Reg. No. 31,338), Douglas E. Chin (Reg. No. 66,713), and Peter Yi (Reg. No. 61,790). Pursuant to 37 C.F.R. § 42.10(b), Petitioner has filed a power of attorney designating the above-identified counsel.

D. Service Information Under 37 C.F.R. § 42.8(b)(4):

Pursuant to 37 C.F.R. § 42.8(b)(4) service information for the Petition is as follows:

Lead Counsel	Back-Up Counsel
Hsuanyeh Chang, PhD Reg. No. 73,431 HSUANYEH LAW GROUP PC 11 Beacon Street, Suite 900 Boston MA 02108 (617) 886-9088 (Phone) hsuanyeh@hsuanyeh.com	Stephen Y. Chow Reg. No. 31,338 HSUANYEH LAW GROUP PC 11 Beacon Street, Suite 900 Boston MA 02108 (617) 886-9288 (Phone) Stephen.Y.Chow@hsuanyeh.com
	Douglas E. Chin Reg. No. 66,713 HSUANYEH LAW GROUP PC 11 Beacon Street, Suite 900 Boston MA 02108 (617) 886-9488 (Phone) Doug.Chin@hsuanyeh.com
	Peter Yi Reg. No. 61,790 HSUANYEH LAW GROUP PC 11 Beacon Street, Suite 900

	Boston MA 02108 (617) 886-9188 (Phone) Peter.Yi@hsuanyeh.com
--	---

Petitioner consents to electronic service at the above-identified email addresses.

III. ADDITIONAL REQUIREMENTS:

A. Payment of Fees Under 37 C.F.R. § 42.15:

The required fees are submitted herewith from Deposit Account No. 50-6685 (Order No. 1280-0016). If any additional fees are due at any time during this proceeding, the Office is authorized to charge such fees to Deposit Account No. Deposit Account No. 50-6685 (Order No. 1280-0016).

B. Timing Under 37 C.F.R. § 42.202:

The present petition for post-grant review is filed within nine months after the grant of the ‘370 patent.

C. Grounds for Standing Under 37 C.F.R. § 42.204(a):

Petitioner certifies that: (1) the ‘370 patent is eligible for post-grant review; and (2) Petitioner is not barred or estopped from requesting post-grant review of any claims of the ‘370 patent on the grounds identified herein.

IV. NAND FLASH TECHNOLOGY BACKGROUND

Petitioner’s expert, Dr. Carl Sechen, has provided in his declaration (“Sechen,” Ex. 1002) a deep analysis of the known NAND flash technology relied

upon by the Lifetime Patents (Sechen Section V), the embodiments admitted or advanced in the common specification (Sechen Section VII), the evolution of the Lifetime Patent claims from specific NAND flash technology to abstractions (Sechen Section VIII), specific defects in the '370 claims (Sechen Section IX), and the obviousness of those claims over the Gavens (Ex. 1045) in view of the POSITA's knowledge of the art (Sechen Section X). Following is a summary of the NAND flash memory technology (reviewed by Dr. Sechen) underlying the Challenged Claims to a "system for storing data," based on abstracted, but known MLC and SLC NAND flash modules and a controller coupled to them and maintaining known NAND flash address mapping, further "adapted" to perform a "data integrity test."

A. Characteristic Nature of NAND Flash Memory

A **NAND flash cell** is type of transistor with a floating gate that can retain electrical charges associated with "threshold voltages" that, applied to a control gate, allows conduction of electrical current from drain to source. (Sechen ¶¶ 26 [Fig. 2.1(a)], 40 [Figures 6 and 7 from Atwood {Ex. 1038}] and 41.)

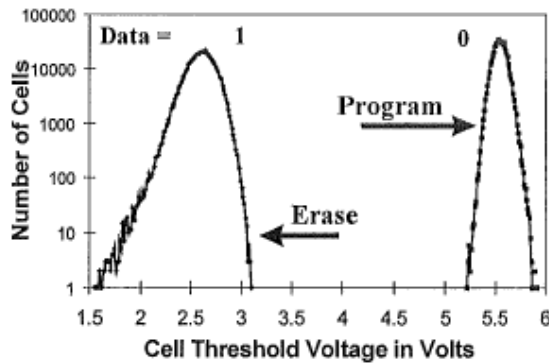


Figure 6: Single bit/cell array threshold voltage histogram

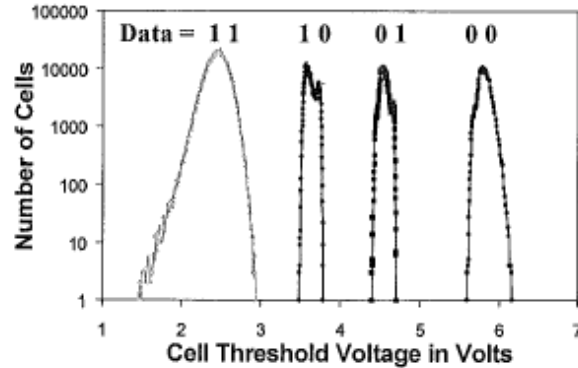


Figure 7: Two bit/cell array threshold voltage histogram

These threshold voltages may be chosen to represent information to be stored, in “classic” NAND memory operation, using two threshold voltage levels (Figure 6), the lower level to represent (“store”) a logical “1” and the higher level to store a “0” of one bit of digital computer data. (*Id.*) The same storage cell can use four threshold voltage levels (Figure 7) to represent four values corresponding to two bits of binary computer data (which in NAND memory operation is sourced from two distinct groups, “pages,” of logical data). (*Id.*) An n power of two (2^n : eight, sixteen, . . .) threshold levels may be used in NAND flash operation to represent corresponding bits of n pages (*id.* ¶¶ 40 and 42-43). But a cell or group of cells do not constitute “memory,” which requires circuitry for selecting, programming (writing) and reading the cell or group of cells (*id.* ¶¶ 26 and 29)

To form **NAND flash memory**, storage cells are hard wired in strings (bit-line “columns”) and word-line “rows” forming “**pages**” each typically 2K storage cells **programmed** (written) **page by page**. (*Id.* ¶ 26.) NAND flash is so

characterized by wiring of its storage cells in typically 64-page “**blocks**,” individually **erased in unison** to prepare for writing of new pages (*id.* ¶¶ 28-30). Unlike magnetic hard disk drives and other technologies that allow “write in place” of data at a physical location assigned to prior versions, in NAND flash programming, an update to stored data must be written to a physical location that is erased in preparation (“erase before write”); erasure, a much longer process than writing, is done in the background, when there are no user-requested read or write operations. (*Id.*) To maintain logical visibility to the user of a NAND flash memory device such as a Solid State Drive (“SSD”) (shown at Sechen ¶ 30), there are maintained and updated tables in or available to a **NAND flash device controller**, shown as a hardware module or chip on an SSD circuit board (*id.*) to “map” logical locations to physical locations in the NAND flash memory array (“**L2P mapping**”), which update for each data write (*id.* ¶¶ 30 and 31). The physical instances of NAND flash pages and blocks determine the **Physical Block** Addresses (“PBA”) mapped from the construct of **Logical Block** Addresses (“LBA”). (*Id.* ¶¶ 32-34.) This mapping and remapping is performed with the software **Flash Translation Layer** (“FTL”) of the controller with **address tables** in **controller RAM** and **backup** in the flash memory. (*Id.* ¶¶ 31-38.) The physical reading, writing and erasing of NAND flash cells is performed by circuitry in a NAND flash memory module, shown in multiples in Sechen paragraphs 29 and 30 (“flash,” “flash memory” or just

“NAND”) on a board, along with a block diagram identifying reading, writing and erasing functions (*id.* ¶ 29). A POSITA would understand this to be a **NAND flash memory or module**. (*Id.* ¶ 30.)

B. Characteristic NAND Flash Memory Management

Sechen paragraphs 34-38 outline common processes in the use of NAND flash memory. These include **bad block management** and **garbage collection** to make available adequate numbers of blocks for new writes without unnecessary, time-consuming erasures. Typically, “hot” data, *i.e.*, frequently updated (such as system) data, and “cold” (not-“hot”) data are clustered in respective physical blocks in order to facilitate efficient (fewer erase-and-re-writes) collecting of “valid” (un-updated) stored data and freeing up the blocks they otherwise occupy. Related “**wear leveling**” processes (“dynamic” at the time of writing and “static” in the background) even out write and erase stresses on NAND memory blocks – which have limited expected “endurance” (“lifetime”) – aiming to avoid premature failure or retirement of enough blocks that would compromise system use. (Sechen ¶ 39 [**system lifetime**].)

C. Introduction of MLC and SLC Flash

Multi-level cell (MLC) NAND flash, developed in 1992-97 as described in Atwood (Ex. 1038), was the use of the NAND storage cell with four threshold voltage levels to represent two bits of information. (Sechen ¶¶ 40-41.) The first

known use of the term “SLC” was in a 2001 article that called the established technology “**single-level program cell NAND flash (SLC)**” and compared it with then new MLC. (Ex. 1039, Sechen ¶ 42.) Although the terms have been shortened over the years, a POSITA would understand that “MLC” refers to the use of NAND storage cells, each storing two bits written in two passes – a “lower” (least significant bit, “LSB”) logical page and then a distinct “upper” (most significant bit, “MSB”) logical page. (*Id.* ¶ 43.) That is, MLC flash memory allows writing **two logical data pages into one physical page of memory**. As reviewed at Sechen paragraph 43 (particularly Sechen note 17), the programming of MLC memory is more complex and stressful than SLC because of MLC’s narrower window for distinct threshold charges and its multiple passes of writing; also, a page-wide set of latches (**page buffer**) is required for reading *each* level of logical page programming. Thus, a POSITA would understand that different circuitry is required for **MLC NAND flash memory** than for **SLC NAND flash memory**, and that **SLC NAND flash memory is incapable of storing more than one logical data page in one physical page of memory**.

Two-state operation of MLC (later called **pseudo-SLC** or “**pSLC**”) was known by 2002. (Sechen ¶ 49; U.S. Patent No. 6,456,528 to Chen for “Selective Operation of a Multi-State Non-Volatile Memory System in a Binary Mode” [“Chen ‘528,” Ex. 1040] [one-bit *mode* of writing only one logical data page into one MLC

physical page of memory])). This mode of MLC use, applying the MLC memory circuitry and pulsed/phased writing, has inferior performance and endurance relative to “real” SLC. (Sechen ¶ 49.) A SanDisk suite of patents (incorporating by reference among others, Chen ‘528) disclosed lower-density (pSLC) *mode* use of MLC modules through partitioning and configuration for multiple reasons, including error management and faster processing for caching writes (*e.g.*, Gavens [Ex. 1045]; *also* U.S. Patent No. 8,806,301 to Yu et al., published Apr. 14, 2011 [Ex. 1046]; explained at Sechen ¶¶ 53-56 [error management] and 45 [caching]).

D. Known Hybrid Use of SLC and MLC NAND Flash Modules with Strategies of Preferential Mapping, Wear Leveling and Error Management

Because of the compression of its threshold levels and its multiple passes of writing, MLC NAND flash was well-known to wear more quickly (have less “endurance”) and programmed more slowly than SLC NAND flash. (Sechen ¶¶ 40-42 and 45 [use of SLC as a cache for MLC].) Thus, it was proposed as early as 2008 to use hybrid systems of **SLC modules** and **MLC modules** in which more **frequently written/updated data**, such as system data, user directories, and certain user files, would be written **preferentially to** a more robust **SLC module** while less frequently updated data would be written to the MLC module. (Sechen ¶ 46; Nelson Duann, SLC & MLC Hybrid (Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008) [“Duann,” Ex. 1034]; U.S. Patent No. 8,078,794 to Lee et al.,

published Sept. 4, 2008 [“Lee ‘794,” Ex. 1041].) SLC was also used for faster-written **cache** upstream of slower memory such as MLC and HDD. (Sechen ¶ 45.)

This **SLC module preference** was applied in 2008-09 to a variety of **wear leveling** techniques to avoid premature failure of a system by some components reaching their endurance limits before others (Sechen ¶¶ 47-48 and 58-60; *e.g.*, Sutardja [Ex. 1042]; Moshayedi [Ex. 1043].)

Additional tools or techniques were known in the art before the priority date to avoid premature failure by applying **error management near the end of life** of the system, with **preferential writing to SLC** upon failure of some “data integrity test” of an MLC location. (Sechen ¶¶ 53-56 and 58-61, *e.g.*, Gavens [Ex. 1045].)

The availability to the POSITA of these **preferential writing to SLC** techniques to avoid premature failure makes obvious independent claims 1 and 18 of the ‘370 patent through their claim elements reciting *remapping* to SLC. Nothing disclosed in the ‘370 patent specification was new relative to the 2011 state of the art of NAND flash technology; to the contrary, the disclosed embodiments would not be enabled without the understood (by a POSITA) physical operation of the distinctly referenced SLC and MLC modules as SLC NAND flash modules and MLC NAND flash modules with supporting circuitry at least for their distinct organizations, reading, writing and erasing. But claims 1 and 18 both **nonsensically**

require “**transfer**” of **erroneous data** to SLC, rendering those independent claims inoperative and all claims depending from them invalid.

V. THE ‘370 PATENT: 2012 Common Specification and 2018 Change

The 2012 common specification of the Lifetime Patents discloses no more technology than known, hybrid MLC and SLC NAND flash memory module systems with two proposed features of operation, variants of common flash wear leveling and error management. The first three patents claimed that known system with those operational features and were issued based on the perceived novelty of their recited *wear leveling* “transfer” of data to SLC. In the 2018 application resulting in the ‘300 patent, the same 2012 system was rewritten in claims for a “memory space” abstraction mentioned in the specification only as quantity of storage, while elevating to a claim element an RAVM used in various flash memory roles and not clearly identified in the common specification, much less as an advance in the art. In the next, ‘546 patent, common “controller memory,” ambiguously referenced in the common specification, was introduced to the claim language. The subject ‘370 patent claims partly returned to the pre-2018 structure, but with “memory spaces” and “memory elements” and without wear leveling – and a nonsensical **transfer** to SLC of **data** found to have **failed** the data integrity test.

A. The Common Specification Recited and Relied on a Known Hybrid System of MLC and SLC Modules and Its Operation.

The core disclosed system of known MLC NAND flash and SLC NAND flash modules is described multiple times in the specification. (*E.g.*, ‘370 4:26-31, 5:19-23, 7:12-18; Sechen ¶ 69.) Fig. 4 shows a physical memory device module including two banks each including 8+ **MLC flash memory modules** and 2+ **SLC NAND flash memory modules**). A controller “coupled” to the MLC and SLC modules performs L2P/FTL functions essential for NAND flash operation and also performs common wear leveling. (3:10-44 [BACKGROUND FTL/wear leveling]; *compare* Sechen ¶¶ 34-36.) Only two features are proposed in the DETAILED DESCRIPTION, for “increasing the reliability and lifetime of a NAND flash storage system” (5:13-7:44).

The first, “data integrity test” feature is shown as the NAND flash method steps of Figs. 3A and 3B, explained in the text (6:24-61). Dr. Sechen identifies (¶ 71) substantial ambiguities and inconsistencies even as to the disclosed comparison of “**stored data**” and “**retained data**.” The specification text is unclear as to whether addresses are compared or data written to those addresses (Sechen note 39) and what “**device controller memory**” is referenced at different steps (Sechen note 38). The only RAVM mentioned is “**DRAM**” where data to be written to flash is held (6:28-30); “DRAM 20” of generic Fig. 1 is explained as “controlled” by the controller 14 among other possible memories such as rotating disk or the distinct MLC and SLC

modules (5:32-51). But “**volatile memory**” is admitted in the ‘370 BACKGROUND for “**buffering, caching**” (4:5-6).

The second feature is functionally stated in two sentences, the first describing wear leveling by “**allocat[ing]** ‘hot’ blocks i.e., those **blocks** that receive frequent writes, into the **SLC NAND flash memory module 28**, while allocating ‘cold’ blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26.” (6:62-7:1.) A second sentence suggests implementation by “**maintain[ing]** a count of those blocks that are accessed (written to) most frequently” and “**transfer[ring]** the contents of those blocks into the SLC NAND flash memory module 28” – “on a **periodic basis**” such as “every 10,000 writes.” (7:1-7 [emphasis added].) Multiple ambiguities were introduced (Sechen ¶ 73), as whether the referenced blocks are the **physical blocks** individually erased in flash memory **or logical blocks** mapped to them in flash operation.

B. The First Three Lifetime Patents on Operation of a Known Hybrid MLC-SLC NAND Flash Memory System

The first three Lifetime Patents claimed the known, physical hybrid flash system of (1) an **MLC memory module** (‘298 [Ex. 1005] 7:31-32, ‘385 [Ex. 1007] 7:14-15, ‘240 [Ex. 1009] 7:31-32), (2) a distinct **SLC memory module** (‘298 7:33-34, ‘385 7:16-17, ‘240 7:33-34) and (3) a **controller/FTL** “coupled” to the **modules** performing *ordinary* **L2P address mapping** (‘298 7:13-25, ‘385 7:19-28, ‘240 7:35-

46), **adding operational features of a data integrity test** (‘298 7:26-32, ‘385 7:29-36, ‘240 7:47-54) and **wear leveling** (‘298 8:1-9, ‘385 7:41-8:4, ‘240 7:55-87). The only limitation not found in the prior art multi-modal NAND flash system of U.S. Patent Appl. Pub. No. 2010/0172179 (“Gorobets ‘179,” Ex. 1044) was the recited wear-leveling “**transfer**” of the contents of “blocks” (not clearly logical or physical) (Sechen ¶¶ 75-78; *e.g.*, Sept. 2, 2014, [‘298] Notice of Allowability at 2 [Ex. 1006 at 80]; June 17, 2014, [‘298] Office Action at 7-8 [Ex. 1006 at 45-46]).

C. 2018 ‘300 Patent Abstraction of the Disclosed Hybrid MLC-SLC Flash System

On June 12, 2018 – six years after the April 25, 2012, filing of the specification common to all the Lifetime Patents – the application resulting in the ‘300 patent was filed with its original independent claim rewriting the base hybrid MLC-SLC NAND flash memory system into an unsupported and vague mix of “memory spaces” and “memory elements,” including “at least one random access volatile memory element” (June 12, 2018, [‘300] Application at 14 [Ex. 1012 at 14]), although the only RAVM mentioned in the common specification relating to any suggested invention was the “DRAM” where host data is received for the disclosed data integrity test (‘370 6:14-16) and “volatile memory” in the BACKGROUND art for “caching, buffering” (3:61-62). As explained at paragraphs 80 and 81 of the Sechen declaration, the new terms and recitations had no basis in the specification

and made no contribution to structural clarity (notice), but to the contrary, appeared intentionally vague to cover technology other than the known and relied-upon (for operational structure) system of MLC and SLC NAND flash modules; moreover there was no claim to the *wear leveling* “transfer” that distinguished Gorobets ‘179 (Sechen ¶ 81; *failed data integrity test* “transfer” nonsensically stated as of “data corresponding to stored data” found to have failed, ‘370 8:8-12, 9:6-8). Confronted without the *wear leveling* transfer with continuing rejection over the Gorobets ‘179 multi-modal NAND flash system, amendments were made that altered connections between the claim elements. (Sechen ¶¶ 82, 83.) In partial resolution of the vagueness of “memory space,” the claims were amended so that the MLC and SLC “memory elements” were “mapped” to their respective “memory spaces,” that, with the recited controller mapping, made clear that those “memory spaces” were logical addresses or “logical address space.” (Sechen note 49, discussing Oct. 8, 2020, [‘300] Amendment at 2-5 [Ex. 1012 at 71-74]. Ultimately, the ‘300 claims were allowed after an argument that the asserted art did not disclose enough “conventional cache” to perform the comparison of the recited data integrity test. (Sechen ¶ 83, quoting the argument at Oct. 8, 2020, [‘300] Amendment at 9 [Ex. 1012 at 78] and reciting the Examiner’s reliance at Jan. 27, 2021, [‘300] Notice of Allowability at 2 [Ex. 1012 at 86].) But no such departure from conventional NAND flash was

suggested, much less disclosed in the specification or limited in the claims – and given NAND writing by *page* (e.g., Sechen ¶ 29), unnecessary.

D. Further Reshuffling

In the ‘546 patent, the terms “MLC memory module” and “SLC memory module” returned as part of a “bank of nonvolatile memory” (‘546 7:37-41), but with each module only requiring one undefined “element” – in contrast to the pre-2018 patents requiring at least a flash “individually erasable block” (Sechen ¶ 84). The ‘546 patent independent claim 1 recited a “controller memory” in various roles, including, after receiving and “transferring” data to MLC, “reading the stored data [in MLC] to the controller memory and comparing the stored data in the controller memory in the [MLC] to the retained data that was associated with the stored data in the [RAVM] by the controller” (‘546 8:15-21 [emphasis added]). Although the controller was recited as “operable” to “retain such received data” in RAVM (e.g., ‘546 8:5-9), no such operation was disclosed in the specification. ‘546 claim 1 did get the failed data integrity test transfer right, of “data corresponding to the retained data” (‘546 8:31-34). However, the ‘370 claim language reshuffling omitted RAVM, controller memory, “module” in favor of “memory space” and “memory element” – and returned to the ‘300 patent **nonsensical** *failed data integrity test transfer* to SLC of the “stored data” found to have failed (‘370 8:7-10, 9:26-29). This claim language shuffling for the only disclosed *data integrity test* should not be

tolerated – especially in the apparent attempt to extend claims 14 and 15 to *unrelated SLC caching*.

E. The Challenged Claims of the ‘370 Patent:

Challenged claim 1 of the ‘370 patent is exemplary:

1. A system for storing data comprising:

[1a] an MLC non-volatile memory space including at least one MLC non-volatile memory element;

[1b] an SLC non-volatile memory module space including at least one SLC non- volatile memory element; and

[1c] a controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element wherein the controller is adapted to:

[1d] a) maintain an address map of the MLC and SLC non-volatile memory spaces, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element;

[1e] b) [1e1] determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, **fails**

a **data integrity test** performed at the controller based upon received data retained at the controller and which received data is stored in the at least one **MLC** non-volatile memory element as **stored data**, and, in an event of such a failure, the controller [1e2] **remaps** the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element and, [1e3] the **stored data** is **transferred from** the at least one **MLC** non-volatile memory element to the at least one **SLC** non-volatile memory element.

(7:45-8:10 [emphasis and labels added].) Notably, element [1a] substitutes the abstract “memory space” for the corresponding “module” and “memory element” for “a plurality of individually erasable blocks” of ‘298 claim 1 (‘298 7:9-10). Element [1b] inconsistently recites “memory module space” in an otherwise like substitution (‘298 7:11-12). Although element [1d] and [1b], controller functions a) and b) roughly correspond to ‘298 controller functions a) (‘298 7:16-25 [L2P/FTL]) and b) (‘298 7:26-33 [data integrity test]), the ‘298 controller wear leveling functions c) and d) (‘298 8:1-9 [with the “transfer” function deemed novel]) are omitted. The ‘370 element [1e1] data integrity test is “based upon received data retained at the controller” and “stored data” stored in MLC [understood to be tested], roughly as disclosed in the DETAILED DESCRIPTION (6:42-47, Sechen ¶ 73). However, while element [1e2] (remapping to SLC of the logical “entry” originally mapped to

MLC) tracks ‘298 controller function b) and the DETAILED DESCRIPTION (6:56-59, element [1e3] nonsensically calls for the “stored data” in the MLC location that just failed the comparison test to be “transferred” to SLC (*see* Sechen ¶¶ 84, 90, 97, and 114-115). There is no utility in keeping the erroneous data. Independent claim 18, mirroring the same controller functions, repeats the nonsensical “transfer.” The remaining claims 2-17 all depend from claim 1. Claims 2 and 3 respectively call for the “minimum quanta of [logical] addresses” to be a “block” or a “page.” Claims 4-10 call for the MLC and SLC blocks to be NAND flash memory, resistive random-access memory (RRAM), phase change memory (PCM) or magnetic random access memory (MAGRAM). Claim 11 calls for “a transfer of content on a periodic basis.” Claims 12 and 13 respectively call for the MLC and SLC elements to each “comprise” a “block” or a “page” “with physical addresses. Claims 14 and 15 respectively states that “the [nonsensically recited] transfer of the stored data from [MLC found to have failed the data integrity test] to [SLC] is “temporary” and “temporary” until MLC “is available.” Claim 16 calls for the “operations of the controller” to “enhance a lifetime” of one MLC and one SLC element. Claim 17 calls for the data integrity test determination to be made “during a write operation.”

In view of the literal claims and disclosure of the ‘370 patent, the accompanying prior art references and supporting declaration of Dr. Sachen (Ex.

1002), Petitioner respectfully requests cancellation of the Challenged Claims as summarized in the following table.

Grounds	Exhibits
Ground 1: Claims 1-18 are invalid under 35 U.S.C. § 112(a) because ‘370 patent specification fails to provide enabling written description, including the nonsensical transfer.	1001, 1002, 1004
Ground 2: Claims 1-12 are invalid under 35 U.S.C. § 112(b) for failing to particularly point out and distinctly claim the subject matter which the inventor regards as his or her invention, including because of failure to disclose structure for controller functions, recitation of method steps in the system claims, and undefined terms and inconsistent recitation.	1001, 1002, 1005, 1007, 1009, 1011, 1044, 1045, 1082
Ground 3: Claims 1-12 are unpatentable under U.S.C. § 103 as obvious over Gavens and incorporated disclosures in view of a	1001, 1002, 1004, 1005, 1006, 1007, 1009, 1039, 1040, 1041, 1042, 1043,

POSITA's knowledge of NAND flash technology.	1045, 1049, 1050, 1051, 1053, 1054, 1055, 1056, 1057, 1058, 1070, 1072
--	--

F. Person of Ordinary Skill in the Art

A person of ordinary skill in the art at the time of the claimed inventions would have a bachelor's degree in computer engineering, electrical engineering, computer science, or a closely related field, along with at least two years of experience in the design, development, implementation, or management of memory devices and systems. A person with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the development and use of memory devices and systems. As is common, one could obtain equivalent knowledge and perspective from other life experiences as well. (Sechen ¶¶ 63 and 64).

VI. 37 C.F.R. § 42.204(b)(3): CLAIM CONSTRUCTION

Under 37 C.F.R. § 42.200(b), claims in a post-grant review proceeding are construed using the same standard as that in a civil action. This includes “construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent,” *id.* The standard for claim construction is set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005).

MLC and SLC memory/module/element have the following meanings based on POSITA understanding (Sections IV(C)-(D) and V(A)-(B) *supra*: Sechen ¶¶ 42-50, 66-69, 75-78, 80, 84 and 87), especially because of Dr. Rao’s specific choice of using the term “SLC module” and not “SLC mode” in the DETAILED DESCRIPTION, given his disclosure of a SLC chip in the incorporated Rao ‘916 (Ex. 1004, Figs. 6 and 7) and the distinct reference to “SLC” mode in the documents submitted with the 2012 specification:⁷

- **“MLC memory modules”** means “modules comprising MLC non-volatile memory” *where*

“MLC non-volatile memory” means “**non-volatile memory cells arranged with circuitry *capable* of storing multiple logical pages in a single physical page of cells**” and

- **“SLC memory module”** means “module comprising SLC non-volatile memory” *where*

“SLC non-volatile memory” means “**non-volatile memory cells arranged with circuitry *incapable* of storing multiple logical pages in a single physical page of cells**”

⁷ (E.g., Sechen notes 14, 15 & 19, Ex. 1068 (IDS#11), Ex. 1069 (IDS#8), Ex. 1071 (IDS#2)).

When MLC first appeared, distinguishing the established two-threshold-voltage level memory as “SLC,” “level” referred to its single “level” of memory programming (Sechen ¶¶ 40-43): a cell cannot be a “memory” without the means for writing and retrieving, namely the circuitry (Sechen ¶ 26, note 6), where **SLC memory** does not have the circuitry to store two pages in one page of cells (‘370 3:1-5 [SLC can only be written once], Sechen ¶¶ 43, 49, 87 and notes 17 & 51). “Module,” used in the specification and the first three patents, is a complete hardware component, interchangeable with a chip (Sechen ¶ 30, note 8). In the ‘370 claims, the terms “MLC” and “SLC” modify “memory space” and “memory elements.” Because of the known and disclosed “page architecture” of NAND flash (Rao ‘916 1:39-58, Fig. 9; Sechen note 34, ¶ 87), to the extent that those terms are not found indefinite or inoperative, “**MLC memory space**” and “**SLC memory space**” should be construed as the **modules** of the respective **nonvolatile memories** defined above; “**MLC memory element**” and “**SLC memory element**” should be construed as NAND-mappable/addressable physical pages that are those distinct memory types (*MLC pages that each can be mapped to multiple logical pages simultaneously and SLC pages that can only be mapped to one logical page*).

“**Enhance a Lifetime**”: This term, used in claim 16, is not explained in the DETAILED DESCRIPTION. (Sechen note 26 and ¶ 81). If the term is not found unenabled or indefinite, “enhance a **lifetime**” should be construed in the general

understanding of the POSITA as an act to avoid premature failure of a NAND flash component (*id.*).

Data Integrity Test, “Transfer”: As explained by Dr. Sechen (§ 90), the claimed data integrity test, disclosed only as steps of flowchart Figs. 3A and 3B (explained as a method of operation at 6:24-61), is performed after a write of a logical page, without intervening operations, “based on” “match”-type “comparing” (Sechen note 40), because no other basis is disclosed. Moreover, the data integrity test should be performed immediately after a write operation, as that is the only reasonable understanding of the DETAILED DESCRIPTION of Figs. 3A and 3B (§ 71 above, particularly note 34). As in that description, the claims do not clearly specify where and how “stored data” and “retained data” are held. The term “transfer” is not used in that description of the claimed data integrity test, but only in the description of wear leveling, which though serving to distinguish the first three patents from Gorobets ‘179 (§§ 75-78 above), is fraught with issues of opaqueness (*e.g.*, Sechen note 45). A POSITA would understand that the data integrity test of the Fig. 3A and 3B flowchart is performed without delay in the write operation, where failure results in remapping (steps 120 and 122 if SLC is available) and return (“M-2” in the figures) to execution of step 110 – writing to the remapped physical address (6:49-61), thus any disclosed “transfer” is the writing of the “retained data” (including reading it first) to the remapped physical location. Thus, although the

specified object of the term “transfer” in the ‘370 claims (elements [1e3] and [12e3] and claims 14 and 15) is nonsensical, “transfer” is disclosed as writing of “retained data” to a remapped physical address (6:49-61), so that a POSITA would construe the term to mean the immediate (after determination of test failure) reading of logical data from one physical location and writing the data to another physical location. (Sechen ¶ 90.)

* * * * *

Grounds for Review Under 37 C.F.R. § 42.204(b)(4)-(5):

VII. GROUND 1: THE CHALLENGED CLAIMS LACK A WRITTEN DESCRIPTION DESCRIBING THE CLAIMED SUBJECT MATTER IN ACCORDANCE WITH 35 U.S.C. § 112(a).

As reviewed at paragraphs 79-84 of the Sechen declaration, the abstraction in the ‘300 patent of unsupported “memory space” and “memory elements,” departing from the known hybrid memory system of SLC and MLC NAND flash modules with NAND flash-defined blocks, and the subsequent further shuffling of terms do not identify any advance in the art overlooked in the pre-2018 patents but merely provide a verbal thicket to support the proliferation of Lifetime Patents. If there were some such advance in the recited “memory spaces” and “memory elements,” it needed to be identified and enabled. If the “memory space” construct is to cover a genus of “all nonvolatile memory having superior endurance to MLC NAND,” the specification must enable the full scope of the invention. *Amgen Inc. v. Sanofi*, 598

U.S. 594, 610 (2023) (substantial research results not adequate). As shown in Section IX, there is no invention here at all, but even before one gets there, the ‘370 patent claim language reshuffling is exposed for unsupported and inoperable relationships between new terms, including those identified at paragraphs 91-99 of Dr. Sechen’s declaration – not least of which was the nonsensical “transfer” of erroneous data to SLC – which invalidate the Challenged Claims under 35 U.S.C. § 112(a):

A. The Challenged Claims Limited by “Memory Space” Are Unsupported Under 35 U.S.C. § 112(a).

The Challenged Claims are unsupported by any written description of the term “memory space” (7:47, 7:49, 7:35, 8:64, 8:67, 9:4), where the term was used only to describe *market share* (2:56), and relative *storage capacity* (5:29-31). To the extent that the terms are intended to capture something other than the disclosed “memory modules,” there is no support for a system with the recited operation other than the POSITA-understood MLC and SLC NAND flash memory modules and their understood operation. (Sechen ¶¶ 84 and 91.) The Challenged Claims thus fail as unsupported under 35 U.S.C. § 112(a).

B. The Challenged Claims Limited by “Memory Element” Are Unsupported Under 35 U.S.C. § 112(a).

The Challenged Claims are unsupported by any written description of the term “memory element” (7:48, 7:50, 8:65, 8:67, and *passim*), which is not even mentioned in the specification and for which “element” appears only as a boilerplate reference

to claim elements (7:42-43). (*Also* Sechen ¶¶ 80, 84 and 92.) To the extent that “memory elements” is considered a material limitation of the claimed system (as they must be), it is unsupported in the specification, and the Challenged Claims fail as unsupported under 35 U.S.C. § 112(a).

C. The Challenged Claims Limited by “At Least One . . . Memory Element” Are Unsupported Under 35 U.S.C. § 112(a) and Fail To Recite a Useful System for Storing Data.

The Challenged Claims, to a system merely having “at least one [MLC]/[SLC] non-volatile memory element” in each “[MLC]/[SLC] non-volatile memory space” (7:47-50, 8:64-67), even if the term “memory element” were itself to pass the 35 U.S.C. §§ 112(a) and 112(b) challenges here, are unsupported under § 112(a) and fail to recite a useful system for storing data. The specification discloses two two-bank embodiments that purport to avail of the superior endurance of SLC. There is suggested a beneficial mix in “SLC NAND flash equal to 12.5% or 25% of MLC NAND flash” (5:16-18), which is consistent with Fig. 4 showing two banks each of 2+ SLC modules compared to 8+ MLC modules (which with MLCs storing twice SLCs, meeting the suggested 12.5% ratio). Figs. 6a and 6b of incorporated Rao ‘916 (Ex. 1004) show a Samsung NAND flash chip K9F108XOA with a “1024M + 32M BIT NAND FLASH ARRAY,” clearly an SLC “module” (Fig. 8 [100K p/e cycle]). The context thus is one SLC module of 1,024 blocks of 64 pages each. Contrasting with this disclosure (and thus unsupported by it), each of the “system[s] for storing

data” recited in the claims of the ‘370 patent is met with just one SLC memory element and one MLC memory element each in a plurality of MLC modules – and a POSITA would understand, in the “page architecture” of NAND flash (*e.g.*, Rao ‘916 1:39-58) in which the write operations are of a page, that an “MLC” and an “SLC” “memory element” should be construed respectively as one MLC physical page (row of cells) and one SLC physical page (Sechen ¶ 87). If “modules” of one page of physical memory satisfied the literal requirements of the systems recited in the Challenged Claims, as literally it would, that system would not be a useful one. There could be no multiple writes, given the NAND flash requirement of writing each update to another physical address, much less mapping to “enhance lifetime” of the system as in claim 16 (8:54-58). Nor is this helped by construing “elements” as “blocks,” as the only disclosed, wear leveling enhancements require multiple blocks (6:62-7:7) and modules noted above. For at least these reasons, claim 1 of the ‘370 patent and all its dependent claims, are invalid under 35 U.S.C. § 112(a).

D. The Challenged Claims Limited by “Transfer” of “Stored Data” to SLC Are Unsupported Under 35 U.S.C. § 112(a) and Inoperative.

Claim elements [1e3] and [18e3] (“transfer . . . the stored data from [the MLC element determined to have failed the data integrity test] to [an SLC element]”) are unsupported and inoperative. (8:7-10, 9:26-28, Sechen ¶ 97). The DETAILED DESCRIPTION only supports, upon the “stored data” failing a comparison test the

rewriting (step 110) of the data retained in the controller memory to a remapped SLC location (6:49-61; Sechen ¶ 71). The “transfer” of the stored data in MLC found to have failed, as recited in claim elements [1e3] and [18e3], is nonsensical – contradictory to remapping elements [1e2] and [18e2] and inoperative for the functioning of a memory system, much less to enhance its lifetime. For at least these reasons, claim 1 of the ‘370 patent and all its dependent claims are invalid under 35 U.S.C. § 112(a).

E. Claims 6 to 10, for Alternative Technologies Substituted for MLC or SLC, Are Unsupported Under 35 U.S.C. § 112(a).

As explained at Sechen notes 3 and 33, the recited technologies operate on a fundamentally different principle of “write in place” than the MLC and SLC NAND flash memories that require writing to a different location for updating logical data. Aside from suggesting that these technologies are substitutable for the SLC module, there is nothing in the specification to adapt to the different technologies the special NAND read, write and erase operations (including multiple passes for reading and writing MLC). (Sechen ¶ 98.) Thus, claims 6 to 10 are unsupported.

F. Claims 14 and 15, for “Temporary Transfer,” Are Unsupported Under 35 U.S.C. § 112(a).

Even if the nonsensical transfer of stored data recited in [1e3] were rewritten to be consistent with remapping element [1e2], the DETAILED DESCRIPTION of Figs. 3A and 3B (Sechen ¶ 71) and reasonable operation of NAND flash, the

intentional “temporary” nature of the “transfer” recited by claims 14 and 15 is not supported in the specification. (Sechen ¶ 99.) That any data in a flash memory location is “temporary” is a given for any updated data, since any updating needs to be written to another location. (*Id.*) That data in an SLC location is written to an MLC location is common in SLC caching known before 2011 (Sechen ¶ 43, *see* Section IX(F) *infra*), but that would not meet the base claim 1 requirement of failure of its data integrity test. Both claims 14 and 15 thus fail as unsupported under 35 U.S.C. § 112(a).

VIII. GROUND 2: THE CHALLENGED CLAIMS ARE INDEFINITE UNDER 35 U.S.C. § 112(b).

The Challenged Claims are invalid for indefiniteness under 35. U.S.C. 112(b) (formerly para. 2), because they recite limitations that, under *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898 (2014), considering the claims as a whole and as informed by the extrinsic record, fail to inform a POSITA with reasonable certainty about the scope of the claimed invention. A patent must be “precise enough to afford clear notice of what is claimed, thereby ‘appris[ing] the public of what is still open to them.’” *Id.* at 909. “Otherwise there would be a zone of uncertainty which enterprise and experimentation may enter only at the risk of infringement claims.” *Id.* Dr. Sechen identifies at paragraphs 79-99 multiple defects in the ‘370 patent claims, but Petitioner expressly raises here the following 35 U.S.C. § 112(b) defects:

A. The Challenged Claims Limited by “Memory Space” Are Indefinite Under 35 U.S.C. § 112(b).

As explained at Section VII(A), the term “memory space” (7:47, 7:49, 7:35, 8:64, 8:67, 9:4) is used in the common specification only as a measure of memory capacity, failing to support the Challenged Claims that recite the term. Unlike the disclosed and previously claimed MLC and SLC modules, there is no boundary for the abstract memory space except as suggested by its constituent “memory elements,” which are themselves indefinite as explained in the next section. The Challenged Claims thus fail as indefinite under 35 U.S.C. § 112(b).

B. The Challenged Claims Limited by “Memory Element” Are Indefinite Under 35 U.S.C. § 112(b).

The Challenged Claims, limited by the open-ended term “memory element” (7:48, 7:50, 8:65, 8:67, and *passim*; see Sechen ¶ 80) are indefinite as that term. On its face, “memory element” is so open-ended that it could be any of ‘300 claim 1’s mapping of “blocks, pages, or bytes of data” (‘300 [Ex. 1011] 8:25-26), or even a cell. The Challenged Claims thus fail as indefinite under 35 U.S.C. § 112(b).

C. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) for Their Recitation of a “Controller” Limited by Functions in the Claims that Are Unsupported by Structure (Physical or Algorithmic) in the Specification.

Although two of the three main components of the disclosed and claimed in the ‘298, ‘385 and ‘240 patents (Exs. 1005, 1007 and 1009) memory system are well-understood MLC and SLC NAND flash modules with their supporting physical

organization of and operations with NAND flash pages and blocks, the “controller” was left open-ended with no physical structure or even a tether to technology. That indefiniteness remains in the ‘370 patent, compounded by the abstraction of the NAND flash modules into “memory spaces” and “memory elements.” Thirty-five U.S.C. § 112(f) has been applied through § 112(b) to find indefinite a functionally claimed limitation of a general term (“nonce” word) which is not supported in the specification by adequate disclosure of structure (physical or algorithmic). *E.g.*, *Rain Computing, Inc. v. Samsung Electronics America, Inc.*, 989 F.3d 1002 (Fed. Cir. 2021). “Controller” is such a nonce word, and the specification does not adequately disclose structure for its claimed functions. Even if not recited in connection with a nonce word, the term fails under § 112(f) if it recites “a function but not sufficient structure for performing the function.” *Egenera, Inc. v. Cisco Sys.*, 972 F.3d 1367, 1373 (Fed. Cir. 2020). Where there are multiple claimed functions, as in ‘370 claim 1, there must be disclosed “adequate corresponding structure to perform all of the claimed functions.” *Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1374 (Fed. Cir. 2015). Where, as in claim 1, a general purpose computer or processor is claimed, special programming (an algorithm) is required to be disclosed. *Ergo Licensing, LLC v. CareFusion 303, Inc.*, 673 F.3d 1361, 1364–65 (Fed. Cir. 2012); *Aristocrat Techs. Austl. Pty Ltd. v. Int’l Game Tech.*, 521 F.3d 1328, 1333 (Fed. Cir. 2008).

The DETAILED DESCRIPTION recited no physical structure and no special programming for the “controller,” only general functions of NAND flash operation and the data integrity test (Sechen ¶¶ 70-73). The functions recited in claim 1 for the controller include maintaining an address map [1d] (7:54), determin[ing] if data in a physical address range fails a data integrity test by perform[ing] that test and if failed, remap[ping] the logical address and [nonsensically] transferr[ing] the data in the failed physical location [1e] (7:64-8:11). These functions are presented in the specification with no more detail than in the claims. (Sechen ¶¶ 71, 72 and 94.) Even if one might presume the details of ordinary NAND flash controller function, any such presumption does not apply to technologies having different write-in-place operation (*e.g.*, Sechen notes 3 & 32). The Challenged Claims fail to inform a POSITA with reasonable certainty and are therefore indefinite under 35 U.S.C. § 112(b).

D. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) Because They Recite Method Steps in a Claim to a System.

Section V *supra* (Sechen Section VIII) showed that ‘370 claim 1 is merely a verbally camouflaged recitation of a hybrid MLC-NAND flash system known in 2011 and described and relied upon in the DETAILED DESCRIPTION with a data

integrity test feature.⁸ Notwithstanding and corroborated by the post-2018 recitation of known RAVM and controller memory, there was no new apparatus or *capability* disclosed or claimed. The only thing putatively new was the “method for utilizing a NAND flash memory system” (6:24-25) of Figs. 3A and 3B described in functional steps (6:24-61) and claimed in ‘370 as verb steps of the controller: maintain[ing] an address map [1d] (7:54), determin[ing] if data in a physical address range fails a data integrity test by perform[ing] that test and if failed, remap[ping] the logical address and [nonsensically] transfe[rri]ng the data in the failed physical location [1e] (7:64-8:11). Such claiming of a physical system (known or otherwise) reciting method steps is invalid for impermissibly mixing product and process limitations across different § 101 classifications, found to be indefinite under § 112(b). *IPXL Holdings, LLC v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005); Manual of Patent Examining Procedure (“MPEP”) § 2173.05(p)(II).⁹ The rule is particularly

⁸ The other feature in the DETAILED DESCRIPTION, wear leveling with a “transfer” that distinguished it from Gorobets ‘179 (Ex. 1044) (Sechen ¶¶ 75-78), an example of multi-mode NAND flash memory, is not claimed in the ‘370 patent.

⁹ The rule provides notice to a manufacturer of a product of whether its physical product infringes without knowledge whether a user of the product performs steps that infringe. Here, as alleged by Patent Owner in the pending suit, Phison is “a

applicable here where the controller is the conventional NAND flash apparatus for performing the functional steps recited (maintaining an address table, controlling access, transferring, reading, and comparing data) and no new *capability* was disclosed or claimed (or implied) – only the *option* of performing the data integrity test at an unspecified time (*see* Section VIII(E) *infra*). *See Rembrandt Data Technologies, LP v. AOL, LLC*, 641 F.3d 1331, 1339 (Fed. Cir. 2011). Thus, the Challenged Claims are invalid under 35 U.S.C. § 112(b) as indefinite.

E. The Challenged Claims Are Indefinite Under 35 U.S.C. § 112(b) Because It Is Uncertain on What and When the Recited Data Integrity Test Is To Be Performed.

The claims 1 and 18 recited step, “determine [determining] if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test,” suffers from multiple ambiguities. First, as noted by Dr. Sechen (¶ 96), it is unclear how a “range of physical addresses” is “within” a “memory element.” More importantly, the step is recited as a test on “a range of addresses listed by an entry,” that is a logical address (that is indeed mapped to a range of physical addresses). But

market leader in [manufacturing] NAND Flash controllers” (Amended Complaint [Ex. 1082] ¶ 6), while a user may elect to use error management features only late in the life of a NAND flash system, if at all. (*E.g.*, Sechen note 20.)

it makes no sense that a data integrity test is performed on the logical rather than the physically stored data, as recited as “received data [stored in the MLC element being tested]” for one component of the “basis” of the data integrity test (8:2-4, 9:18-20). The only “basis” disclosed in the DETAILED DESCRIPTION is a match-type comparison of “stored data” with “retained data.” (6:42-53; Sechen ¶¶ 71 and 90.) Even more importantly, there is no recitation of when the data integrity test is performed. Unlike the “maintaining an address map” function [1d] and [18d], which is continuous, a continuous data integrity test would be impractical and unsupported (retained data, for example, would need to be continuously retained, exhausting memory smaller than the stored data memory). The DETAILED DESCRIPTION introduces in one place that “the controller conducts a data integrity test after every write.” (5:23-34 [emphasis added].) However, in a more detailed explanation, the execution of the test is qualified by “if time permits” (6:3-6) – which is unexplained. Moreover, it would be wasteful to perform such a data integrity test throughout the life of the system. Known error management techniques (Gavens [Ex. 1045] shown in Section IX *infra* to disclose the recited data integrity test) delayed to near the end of life of the system (*e.g.*, Sechen note 20), applied only to a sampling of writes (Gavens 6:3-16), or not at all. While those techniques forestall premature end of system life near its end, there was no disclosure of how the DETAILED DESCRIPTION data integrity test helped, much less the one unclearly claimed in

‘370 claims 1 and 18. The Challenged Claims are invalid under 35 U.S.C. § 112(b) as indefinite.

IX. GROUND 3: CLAIMS 1-18 ARE OBVIOUS UNDER 35 U.S.C. § 103 OVER GAVENS IN VIEW OF POSITA KNOWLEDGE.

The ‘370 patent claims are obvious under *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007) because there is no gap between the prior art of multiple hybrid SLC-MLC NAND flash systems with post-write read error management (Section IV *supra*) and the scope of the ‘370 claims. (Sechen ¶ 100): To the extent understandable, independent claim 1 of the ‘370 patent claims a memory system that would describe known hybrid MLC-SLC flash memory systems as described in the DETAILED DESCRIPTION [Sechen Section VII(B)] with known, necessary L2P mapping operations and at some unspecified time(s) performs a “data integrity test” by comparing data to be written to flash (“retained data”) with the data actually written to flash (“stored data”), one of two embodiments suggested in the specification to “boost” or “increase” “lifetime.” Multiple alternative “data integrity checks” and approaches to avoid premature unreliability of NAND flash systems, including SLC-MLC hybrids, have been detailed in multiple prior art textbooks, articles and patents, as reviewed in [Sechen Section V(C)]. One printed publication

example, Gavens [Ex. 1045] and its incorporated references, discloses or renders obvious the Challenged Claims in view of the knowledge of the POSITA.

A. Claim 1 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶ 101): Gavens (Ex. 1045), among the SanDisk portfolio and incorporating by reference others of that portfolio,¹⁰ is a published reference that

¹⁰ See, e.g., U.S. Patent No. 6,456,528 to Chen (“Chen ‘528”), Ex. 1040, incorporated by reference at Gavens 16:29-40 (binary mode operation); U.S. Patent Appl. Pub. No. 2011/0153912 by Gorobets et al. (“Gorobets ‘912”), Ex. 1049, incorporated by reference at Gavens 20:53-59 (post-write-read error management with binary mode portion); U.S. Patent No. 5,930,167 to Lee et al. (“Lee ‘167”), Ex. 1050, incorporated by reference at Gavens 17:57-67 (MLC with binary mode cache); U.S. Patent Appl. Pub. No. 2010/0172180 by Paley et al. (“Paley ‘180”), Ex. 1051, incorporated by reference at Gavens 8:41-42 (block management system). In turn, both Gorobets ‘912 (¶¶ [0020], [0024]) and Paley ‘180 (¶¶ [0023], [0027]) incorporate by reference U.S. Patent No. 5,936,971 to Harari et al. (“Harari”), Ex. 1057, for using RAM in write cache for flash, and PCT Pub. No. WO 03/027828 by Gorobets et al. (“Gorobets PCT”), Ex. 1058, for buffering mapping information. Hereinafter, it should be understood that reference to a specific portion of any of the

discloses a complete multi-modal NAND flash system with the ordinary L2P/FTL function of its controller, a variety of post-write read error detection and management schemes, and the capability of and compatibility for employing other known tools (disclosed in incorporated documents and exemplified in paragraphs 58-61 above) used to avoid premature NAND system failure.

The Gavens system is not a “pure” SLC-MLC hybrid system. Since the 2001 (*e.g.*, Cho, Ex. 1039) emergence of the terms “multi-level program cell” (MLC) memory and (thereby distinguished) “single level program cell” (SLC) memory, there have been many implementations of hybrid MLC memory modules and SLC memory modules availing of the endurance advantages of SLC. (Sechen ¶ 102, *e.g.*, Lee ’794 [Ex. 1041], Sutardja [Ex. 1042], and Moshayedi [Ex. 1043].) Many NVM implementations disclosed in the SanDisk patent portfolio, such as Gavens, involve the partitioning and configuration of some MLC (or TLC) blocks for one-level (two states) or pseudo-SLC (pSLC) operation. (Sechen ¶¶ 49-50 and 53-56.) The pSLC mode of operation enjoys superior endurance compared to MLC in multi-level mode – though not as superior or as fast as “real” (native”) SLC memory which uses

above references is understood to be disclosed by Gavens due to incorporation by reference, as if the incorporated document was explicitly contained in Gavens.

different circuitry. (Sechen ¶¶ 49, 102; *also* Gavens 12:6-10.) It would be obvious to a POSITA to use an MLC module operating entirely in pSLC mode (and thus be considered a pSLC memory module, which, as mentioned in [Sechen ¶ 49], are marketed as such), still with endurance superior to MLC in multi-level mode, or to use a “real” or “native” SLC module, both with assured success. (Sechen ¶ 102.) Gavens clearly is a system for storing data as recited in the claim 1 preamble. (Sechen ¶ 105, Gavens Fig. 1 (90), 8:13-17.) It discloses or makes obvious, with its incorporated references, each of the limitations of the following elements of claim 1 in view of the knowledge of the POSITA:

1. [1a] an MLC non-volatile memory space including at least one MLC non-volatile memory element;

(Sechen ¶ 106): Gavens discloses a bank of non-volatile memory chips including MLC (NAND flash) memory. (Fig. 1; 8:13-21). The base memory chip of Gavens meets the characteristics of the POSITA-understood MLC flash memory module of cells, circuitry and programming explained in [Sechen ¶¶ 26-30, 42 and 43]. The array of memory cells 200 is partitioned into a first portion 410 configured for lower density (*e.g.*, pseudo-SLC) operation and a second portion 420 configured for high density (*e.g.*, native MLC, having each cell storing multiple bits) operation. (Fig. 14A, 16:15-22.) It particularly meets Phison’s multiple level page programming requirement (distinguishing from SLC) set forth in [Sechen ¶ 87], as programming of those levels of logical pages is disclosed in Fig. 23 (25:18-26:30).

The Gavens controller maps logical “memory spaces” (addresses) to the physical memory (addresses) (8:36-39). To the extent that claim element [1a] is understood, the Gavens memory chip satisfies the “memory space” limitation, and any of the recited partitions or smaller addressable memory – particularly the NAND flash writable physical page (row of cells, *e.g.*, [Sechen ¶ 87]) – satisfies the “memory element” limitation. Gavens discloses claim element **[1a]**.

2. [1a] an SLC non-volatile memory module space including at least one SLC non-volatile memory element; and

(Sechen ¶ 108): Gavens does not disclose the use of a “native” SLC flash memory module or chip as described at [Sechen ¶ 102] because the Gavens memory module or chip 100 is capable, with its circuitry, of programming more than one logical page into a physical page, as explained in [Sechen ¶ 87]. However, Gavens discloses partitioning, configuration and use of portions of its memory array 200 in 1-bit mode, the “pseudo-SLC” mode explained at [Sechen ¶ 49]. Specifically, Gavens discloses, as a base system for multiple operational embodiments, “[a] first portion has each memory cell storing one bit of data and [a] second portion has each memory cell storing more than one bit of data” (4:32-34, 12:6-8 [calling memory operating in 1-bit mode “binary” or “SLC” memory]). Regarding one aspect of the difference, it is explained that the first portion, being “configured as lower density storage[,] . . . operates with a wider margin of error than that of the second portion”

(18:16-20, also 12:6-10, 21:6-9). As explained in [Sechen ¶ 102], it would be obvious to a POSITA to substitute a “real” SLC flash memory module for the Gavens first portion, with a similar, if not wider margin of error than binary mode operation of MLC (*see* [Sechen ¶ 49]) and achieve similar, if not better results with the same NAND flash controller Fig. 1(102) with great expectation of success. Again, the Gavens controller maps logical “memory spaces” to the physical memory (8:36-39) and would be capable of writing to different NAND flash modules, as would be presumed in its memory array. As it is the memory module that performs the physical reading and writing based on controller commands and addresses, the NAND flash controller would be capable of writing to both MLC and “native” SLC (*e.g.*, Moshayedi [Ex. 1043] Figs. 1, 2, ¶¶ [0036]-[0038] [controller 102 controlling virtual-to-physical mapping with RAM 214 for four channels of commercial SLC chips 112 and MLC chips 114]). To the extent that claim element [1b] is understood, the Gavens memory chip itself, or with an obvious addition of an SLC memory chip such as shown in Moshayedi, satisfies the “memory space” limitation, and any of the recited partitions or smaller addressable memory – particularly the NAND flash writable physical page (row of cells, *e.g.*, ¶ 87 above) – satisfies the “memory element” limitation. Gavens, in view of POSITA knowledge, makes obvious claim element [1b].

3. **[1c] a controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element wherein the controller is adapted to:**

(Sechen ¶ 110): Gavens Fig. 1 shows controller 102, which is coupled to and manages one or more memory chips 100 in the memory device 90 (8:17-18, 32-35) and thus addressable “elements” in those chips. As explained in [Sechen ¶¶ 102 and 108], it would be obvious, using known FTL, to provide a “real” SLC in place of Gavens’s memory operated in 1-bit mode. Gavens, in view of the POSITA’s knowledge of NAND flash, renders obvious claim element **[1c]**.

4. **[1d] a) maintain an address map of the MLC and SLC non-volatile memory spaces, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element;**

(Sechen ¶¶ 111 and 112): Gavens discloses the ordinary NAND controller function (‘370 2:37-3:20 [writing host data to NAND flash nonvolatile memory]; [Sechen ¶¶ 30-38]): “A memory block management system implemented in the controller stages the sectors and maps and stores them to the physical structure of the memory array” (8:36-39). Gavens discloses updating of “a directory in a block management system embedded in the firmware of the controller (see Fig. 1)” to direct accesses to one or the other portions of the memory (17:17-19, 18:47-49,

18:64-66). Gavens, for further explanation of block management, incorporated by reference Paley ‘180 (Ex. 1051, [note 10 supra]), which provides further detail:

A memory-side memory manager 300 is implemented in the controller 100 of the memory system 90 to manage the storage and retrieval of the data of host logical sectors among metablocks of the flash memory 200. The memory manager comprises a front-end system 310 and a back-end system 320. The front-end system 310 includes a host interface 312. The back-end system 320 includes a number of software modules for managing erase, read and write operations of the metablocks. The memory manager also maintains system control data and directory data associated with its operations among the flash memory 200 and the controller RAM 130.

(¶ [0155] [emphasis added]; *also* Gorobets ‘912 ¶ [0095].) Paley explains the use of “the currently prevalent LBA interface” (¶ [0020]). “The memory manager 300 is preferably implemented in the controller 100. It translates logical addresses received from the host into physical addresses within the memory array, where the data are actually stored, and then keeps track of these address translations.” (¶ [0150].) Referring to Fig. 9, “the media management layer 330” (¶ [0157]) and “dataflow and sequencing layer 340” (¶ [0158]) combine to perform the role of FTL. Specifically, the media management layer handles “updates, tables and lists used for logical-to-physical address translation and free block management, and wear leveling based on hot counts” (¶ [0201] [emphasis added]). As further explained in

the incorporated Gorobets PCT (Ex. 1058), the media management layer is implemented in firmware “control[ing] the transfer of data sectors between the logical interface 14 to host 12 and the physical interface 18 to Flash memory 20” (Gorobets PCT 13:5-8 [emphasis added]) with the following algorithms:

The data structures required to support the Cyclic Storage [7:20-24: “method of ensuring uniformity of distribution of use”¹¹] media management algorithms [18:1-10: (1) Data Write location to write host data, (2) Block Erase controlling erasure of obsolete data, (3) Block Sequencing of flash blocks used for storing data, and (4) Address Translation controlling “mapping of host logical addresses to physical memory addresses”] are stored principally in flash memory 10 together with the host data sectors, with only a very limited amount of control data being held temporarily in the control processor’s volatile RAM 30. Information held in the volatile memory 30 is non-critical, and can be reconstructed from flash memory if the power supply is interrupted.

(27:22-28:5 [emphasis added].) As explained at [Sechen ¶ 34], it was well-known, as corroborated by Goodson [Ex. 1070] submitted with the 2012 ‘298 application

¹¹ An objective is “to obtain even use of blocks in the non-volatile memory for storage of data over a long period of operation, and to avoid ‘hot-spots’ in non-volatile memory usage, thereby increasing the reliability of the memory system.” (Gorobets PCT 2:4-8 [emphasis added].)

[Ex. 1006]), that the address tables were loaded in controller RAVM and backed up in the flash memory. The NAND flash memory system disclosed in Gavens as further detailed in its incorporated references [note 10 *supra*] explained:

The top level of hierarchy of the mapping structure [Fig. 5 schematic of the “address translation process”] is the sector address table 52, which is a master table containing a physical address for every logical sector stored in the system 10 and which is stored in Flash memory 20. . . .

The sector address record 56 is a list stored in the controller’s memory volatile memory SRAM 30 It may also be reconstructed during device initiation from the sequence of recently written sectors which may be traced in the Flash memory 20. The intermediate temporary sector address table 54 is contained in flash memory 20 and is updated with the contents of the sector address record 56

This hierarchy of mapping structures . . . efficiently supports logical to physical address translation . . . even if electrical power is unpredictably removed from the system 10.

(Gorobets PCT [Ex. 1058] 26:11-27:21 [emphasis added].) Gavens thus discloses a controller that maintains address tables mapping logical addresses (seen by the host computer) to pSLC and MLC physical pages (elements) to be written. As explained at [Sechen ¶ 102], the same L2P/FTL addressing applies to substituted “real” SLC (*e.g.*, Lee ‘794 Fig. 3 reproduced at [Sechen ¶ 46]). Gavens and its incorporated references disclose element **[1d]**.

5. [1e] b) [1e1] determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test performed at the controller based upon received data retained at the controller and which received data is stored in the at least one MLC non-volatile memory element as stored data, and, in an event of such a failure, the controller [1e2] remaps the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element and, [1e3] the stored data is transferred from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element.

(Sechen ¶ 114): In one variant of the Gavens post-write-read error management embodiment of Figs. 14 and 15 (explaining text at 16:13-17:42), user data is written to the higher density (*e.g.*, MLC) portion as a “first copy.” (Gavens 16:41-45.) Then, in a “post write read,” there may be a check for errors [1e1] “by comparison with the **original copy** which may be cached” (16:46-49 [emphasis added]). If the number of error bits is less than a predetermined amount, the first copy is deemed valid and subsequent reads of the data page will be from that copy with any errors corrected by ECC. (16:50-56.) If the number is greater, then a copy is written to the lower density, lower error rate (more robust, *e.g.*, pSLC) portion; this is performed in one embodiment by copying from a cached copy “of the original data.” (17:9-11.) In the Gavens NAND flash technology corpus, “[u]sing RAM in a write cache operating with flash memory has been disclosed” (*e.g.*, Gorobets ‘912 [Ex. 1049] ¶ [0024], Paley ‘180 [Ex. 1051] ¶ [0027]). The “original data”

temporarily stored (“cached” in RAM, understood to be RAVM) is compared to the stored (in flash) data, and if the stored data fails to match, the “original data” (temporarily stored or “retained”) is sent to the more robust pSLC. Thus, this error management variant discloses a data integrity test on written (stored) data that compares it against retained (cached) “original data” in RAM cache. It would be obvious that the “stored data” to be compared would be written to the controller memory (where the Gavens/Gorobets cache has space for at least two write units, nominally, “pages”) for comparison using logic on the controller chip (*e.g.*, incorporated Rao ‘916 [Ex. 1004] Fig. 1 [“ALU”]). The “original data” – corresponding to the logical address (in the address table) – is rewritten to the more robust (pSLC) portion (Gavens 17:9-12). For that to occur, the original data (associated with the logical address entry in the L2P address table) must be remapped [1e2] to the physical address of memory operating in pSLC mode, and any “transfer” in this context is the writing of that original data to the remapped location (physical address). As explained at [Sechen ¶ 97], however, the “transfer” recited at [1e3] nonsensically transfers to SLC the “stored data” found to have failed the data integrity test. That should invalidate claim 1 (Section VII(D) *supra*). However, if the Board rewrites [1e3] to be consistent with [1e2] and the DETAILED DESCRIPTION, the resulting transfer to SLC of the “original data” – corresponding

to the logical address entry in the L2P table – is disclosed by Gavens’s rewriting to the lower density portion, obviously substitutable with SLC.

(Sechen ¶ 115): A POSITA would understand that access to the “stored data” and “retained data” are directed by the Gavens controller and compared “at” the controller using its logic; this clearly meets the [1e1] limitation that the data integrity test is performed “at” the controller “based” on the “stored data” and “retained data.” The use of “real” SLC memory instead of a binary-mode portion of the MLC memory does not increase overall latency, since “copying” of the “stored data” is from the MLC, involving relatively slow decoding (reading), and reading of the “retained data” is from relatively fast controller RAM; any subsequent “transfer” (write) for element [1e3] would be faster for “real” SLC than pSLC (*see* [Sechen notes 11 & 45]). Gavens and its incorporated references, in view of POSITA knowledge, make obvious reasonably read claim element [1e].

* * * * *

(Sechen ¶ 137): Gavens and its incorporated references make obvious, in view of knowledge of the POSITA, each limitation, read reasonably, of ‘370 **claim 1**.

B. Claims 2, 3, 12 and 13, Limiting “Minimum Quanta of [Logical] Addresses” to One Block or One Page and “Memory Elements” to Blocks or Pages with Physical Addresses, Are Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 110-120, 123): Claims 2, 3, 12 and 13, the system of claim 1 wherein [2] *“the minimum quanta of addresses is equal to one block,”* [3] *“the minimum quanta of addresses is equal to one page,”* [12] *“the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element comprise a block with physical addresses,”* and [13] *“the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element comprise a page with physical addresses,”* are obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]), the “block” is the base unit for flash memory erase (‘370 3:4-5; Sechen ¶ 28) and the “page” is the base unit for flash memory write (Rao ‘916 [Ex. 1004] 1:39-43 [page architecture]; Sechen ¶ 27) in the mapping/translation of “a list of logical addresses” to “physical address ranges” such as “blocks” of an MLC module (‘370 11-15). Specifically, Gavens shows a “virtual block” (Fig. 20C, 21:22) and its incorporated Paley ‘180 (Ex. 1051) explains block-level addressing (¶ [0016] (“logical blocks”), ¶ [0163] (“logical address LBA”). Gavens discloses a minimum quanta of addresses equal to one page. (Fig. 4 (70), 10:19-20, 41-47, 20:2-4 [a page 70 is a group of memory cells enabled to be sensed or programmed in parallel], 3:21-22 [a page of memory elements are read or programmed together], 11:20-29 [A page is a minimum unit of programming and reading], 9:36-40 [the memory array 200 is arranged in rows and columns of memory cells, addressable by word lines and bit lines].) Thus, both block-level and

page-level addressing is disclosed for the minimum “quanta” of “logical addresses” and mapped “physical addresses.” As explained at [Sechen ¶¶ 102 and 106], “real” SLC is obviously substitutable for Gavens pSLC and the same L2P/FTL addressing applies to substituted “real” SLC (*e.g.*, Lee ‘794 [Ex. 1041] Fig. 3 at [Sechen ¶ 46]).

Gavens and its incorporated references, in view of knowledge of the POSITA, disclose **claims 2, 3, 12 and 13.**

C. Claims 4 and 5, with MLC and SLC Elements Limited to NAND Flash, Are Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 126 and 129): Claims 4 and 5, the system of claim 1 wherein [4] “*the at least one MLC non-volatile memory element is NAND flash memory*” and [5] “*the at least one SLC non-volatile memory element is NAND flash memory,*” are obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]), the supporting disclosure is about NAND flash (*e.g.*, ‘370 5:16-31). Gavens, which would be understood by a POSITA to describe a NAND flash system with multiple MLC NAND flash modules, expressly describes its MLC non-volatile memory modules as including MLC NAND flash memory elements, which by definition are flash memory. (Fig. 4, 9:49-50 [page of memory cells in the memory array 200 is organized in the NAND configuration], 1:18-19, 4:14-18 [flash memory having a first portion and a second portion storing higher density compared to the first portion], 2:65-66, 8:65-67 [flash memory devices with NAND string structures;

Fig. 1 (90) [flash memory device].) As explained at [Sechen ¶¶ 102 and 108], a POSITA would readily and successfully substitute for Gavens's partitions of MLC memory elements configured for 2-state pseudo-SLC operation a "real" SLC non-volatile memory module, which is understood to include SLC NAND flash memory elements. As to Gavens's MLC NAND flash memory operated in pseudo-SLC mode, they are also described as flash memory. (Fig. 4, 9:49-50 [a page of memory cells in the memory array 200 is organized in the NAND configuration], 1:18-19, 4:14-18 [flash memory having a first portion and a second portion storing higher density compared to the first portion], 2:65-66, 8:65-67 [flash memory devices with NAND string structures], Fig. 1 [flash memory device 90].) Gavens, in view of the knowledge of the POSITA, discloses **claims 4 and 5**.

D. Claims 6 through 10, Limited to Substitution of Alternative Technologies for MLC and SLC, Are Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 132-133, 136, 139-140, 143 and 146-147): Claims 6-10, the system of claim 1 wherein [6] "*the at least one MLC non-volatile memory element is resistive random-access memory (RRAM)*," [7] "*the at least one SLC non-volatile memory element is resistive random-access memory (RRAM)*," [8] "*the at least one MLC non-volatile memory element is phase change memory (PCM)*," [9] "*the at least one SLC non-volatile memory element is phase change memory (PCM)*," and [10] "*the at least one SLC non-volatile memory element is magnetic random-access*

memory (MA-GRAM),” are obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]): To the extent that these technologies are disclosed in the specification adequately to enable these claimed substitutions (with their “write in place” operation contrasting with NAND flash “erase before write,” Sechen notes 3 & 33), their substitutions are obvious in view of background knowledge of the POSITA. That knowledge was exemplified by the ‘298 Examiner’s rejection of the same substitutions (Sechen ¶ 75), citing Gorobets ‘179 (Ex. 1044, a hybrid MLC-SLC NAND flash system like Gavens) in view of De Ambroggi (Ex. 1053) (RRAM, PCM) or Chen ’418 (Ex. 1054) (MRAM), and Kund (Ex. 1055) (alternative technologies having advantages over flash memory). Gavens, in view of the knowledge of the POSITA, discloses **claims 6 through 10.**

E. Claim 11, Limited to the Controller “Transferring Content on a Periodic Basis,” Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

(Sechen ¶¶ 150-151): Claim 11, the system of claim 1 “*wherein the controller causes a transfer of content on a periodic basis,*” obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]), Gavens “transfers content on a periodic basis,” It is unclear whether the recited “transfer” refers to the nonsensical “transfer” of data integrity test claim element [1e3] ([Sechen ¶¶ 97 and 114]); otherwise it has no antecedent in the claim 1. Construing claim 11 “transfer” generally as reading of logical data from one physical location

and writing the data to another physical location (Section VI *supra*), such transfer are made by the Gavens controller “on a periodic basis.” As explained at [Sechen ¶ 73], the use of the term “periodic” in the DETAILED DESCRIPTION (7:1-7) for wear leveling is in tension with the p-e count thresholds recited in the same sentence. To the extent that “periodic” means “occasional,” applied to the dynamic (upon writing) error management actions disclosed in Gavens and incorporated references as reviewed at [Section X(A)(5), Sechen ¶ 114] are “occasional” or responsive to conditions. As explained at [note 11 *supra*], the Gavens NAND flash memory controllers also perform wear leveling functions that are periodic. Gavens discloses that the controller performs operations in the background on a periodic basis. (15:39-41 [data retention errors can be alleviated by periodically refreshing the threshold levels of the cells in a “read scrub” operation], incorporated by reference Lee ‘167 (Ex. 1050) (2:7-10, 30-37 [new data is initially stored in SLC. Later, preferably in the background without slowing down other operations, the data is read out of SLC and reprogrammed into MLC].) Gavens and incorporated references, in view of the knowledge of the POSITA, make obvious **claim 11**.

F. Claims 14 and 15, Limiting “Transfer” to a Being “Temporary,” Are Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA.

(Sechen ¶¶ 160 and 163): Claims 14 and 15, the system of claim 1 wherein [14] “the transfer of the stored data from the at least one MLC non-volatile memory

element to the at least one SLC non-volatile memory element is temporary” and [15] “the transfer of the stored data from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element is temporary until an MLC non-volatile memory element is available,” are obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]), the ordinary operation of NAND flash memory rewrites updated data to new locations and garbage collection for even static data. As explained at [Sechen ¶ 99], even if the nonsensical transfer of “stored data” recited in [1e3] were rewritten to the “retained data” as disclosed in the specification, the “temporary” nature of the transferred data recited by claims 14 and 15 is not supported in the specification. However, it is well known that any data in a flash memory location is “temporary,” and is a given for any updated data, since any updating needs to be written to another location (*e.g.*, 3:1-5, [Sechen ¶¶ 26 and 34]). Thus, the temporary nature of any transfer of data is satisfied by any data that is updated or moved in ordinary NAND flash wear leveling or garbage collection, as managed by the Gavens controller (Section IX(A)(4) *supra*, [Sechen ¶¶ 111-112]). If the base claim [1e3] transfer is not rewritten, and only bad data is transferred to SLC, one might expect that bad data to be purged (and thus temporary) at least in garbage collection. Moreover, concerning claim 15, temporary storage (caching) of data in SLC has been long known for performance (throughput) rather than error management purposes (*e.g.*, [Sechen ¶ 45], *see* Hong [Ex. 1072] at

23 [different caching strategies]). Thus, incorporated in Gavens (note 10 above) Lee ‘167 (Ex. 1050), issued in 1997, disclosed the use of MLC in 1-bit (pSLC) mode as a faster write cache for ordinary mode SLC (Abs: “Data coming into the memory is initially written in available blocks in two states since writing in more than two states takes significantly more time. At a later time, in the background, the cached data is read, compressed and written back into fewer blocks of the memory in multi-state”). But this SLC caching is not covered by claim 15, which requires a claim 1 transfer of “bad data” to SLC ([Sechen ¶¶ 97 and 114]), but even if corrected, requires the transferred data to have been originally mapped and written to MLC – not to SLC cache. If the data rewritten to SLC in the Section IX(A)(5) Gavens embodiment were “cold” or infrequently updated data, at least some would be moved to more (relatively) worn MLC in ordinary static wear leveling (*e.g.*, 3:42-44, [Sechen ¶ 36]) performed by Gavens flash controllers (note 11 *supra*). Thus the Gavens embodiment obviously includes some “temporary” transfers to SLC and even back to MLC and to that extent discloses **claims 14 and 15**.

G. Claim 16, Limiting “Operations of the Controller” To “Enhance a Lifetime” of the Recited MLC and SLC Memory Elements, Is Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA.

(Sechen ¶ 166): Claim 16, the system of claim 1 “*wherein operations of the controller enhance a lifetime of the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element,*” is obvious at least because,

in addition to the obviousness of the base claim (Section [IX(A) *supra*]), Gavens uses a controller that performs wear leveling (Gorobets PCT (Ex. 1058)13:5-8, note 11 *supra*), known to be the most effective enhancer of NAND flash system life (*e.g.*, Sechen note 13). Gavens and its incorporated references, in view of the knowledge of the POSITA, make obvious **claim 16**.

H. Claim 17, Limited to the Recited Data Integrity Test Performed “During a Write Operation,” Is Obvious Over Gavens, Including Incorporated references, in View of Knowledge of the POSITA.

(Sechen ¶ 169): Claim 17, the system of claim 1 “*wherein the controller determines during a write operation if the range of addresses listed by the entry and mapped to the similar range of physical addresses within the at least one MLC non-volatile memory element, fails the data integrity test,*” is obvious at least because, in addition to the obviousness of the base claim (Section [IX(A) *supra*]), a write operation is the only context for which the recited data integrity test is disclosed and the “post-write-read” Gavens error management embodiment is disclosed for exactly that context, continuing the write operation to SLC if the read from data written to the MLC (“stored data”) fails to match the “retained data” (Section IX(A)(5) *supra*, Sechen ¶ 14). Gavens and its incorporated references, in view of the knowledge of the POSITA, make obvious **claim 17**.

I. Claim 18 Is Obvious Over Gavens, Including Incorporated References, in View of Knowledge of the POSITA.

Claim 18 is virtually identical to claim 1: a method claim “providing” the MLC and SLC “memory spaces”/“memory element” and “using” a controller coupled to those elements (8:64-9:3) performing the same functions recited in gerundial form (*compare* 7:44-53 with 9:1-12 [maintain/maintain address map] *and* 7:34-10 with 9:13-29 [determine/determining failure of data integrity test resulting in maps/mapping and transferred/transferring]. Both only claim the known and relied upon hybrid MLC-SLC memory system ([1a]-[1b]/[18a]-[18b]) with a controller performing ordinary, necessary L2P mapping ([1c]-[1d]/[18c]-[18d]) with an abbreviated (baselessly broadened) version of the Figs. 3A and 3B data integrity test ([1e1]-[1e2]/[18e1]-[18e2]) – but both reciting unsupported, internally inconsistent, nonsensical “transfer” to SLC of “stored data” found to have failed the data integrity test ([1e3]/[18e3]). Both should be invalidated for that “transfer” (Section VII(D) *supra*), which is not the “transfer” in the only other disclosed (wear leveling) feature, which was found to distinguish over another hybrid MLC-SLC system, Gorobets ‘179 (Sechen ¶ 75), but not recited in claims 1 and 18. If claim element [18e] is corrected, claim element 18 still recites nothing new or unobvious over the Gavens hybrid MLC-SLC system and its methods of “post-write read to manage errors” (Sechen ¶ 171).

1. **[18a] providing an MLC non-volatile memory space including at least one MLC non-volatile memory element;**

As shown at Section IX(A)(1) to meet virtually identical claim language, Gavens discloses MLC “memory space” and constituent “memory elements,” to the extent understandable, and thus discloses claim element **[18a]**. (Sechen ¶ 172.)

2. **[18b] providing an SLC non-volatile memory space including at least one SLC non-volatile memory element; and**

As shown at Section IX(A)(2) to meet virtually identical claim language, Gavens discloses SLC “memory space” and constituent “memory elements,” to the extent understandable, with obvious substitution of “real” SLC for the pSLC mode of Gavens MLC, and thus discloses or makes obvious claim element **[18b]**. (Sechen ¶ 173.)

3. **[18c] maintaining, using a controller coupled to the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element;**

As shown at Section IX(A)(3) to meet virtually identical claim language (except “maintain” in element [1d]), Gavens discloses an ordinary controller controlling MLC “memory space” and constituent “memory elements,” to the extent understandable, with obvious substitution of “real” SLC for the pSLC mode of Gavens MLC, and thus discloses or makes obvious claim element **[18c]**. (Sechen ¶ 174)).

4. **[18d] an address map of the MLC and SLC non-volatile memory spaces, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a similar range of physical addresses within either the at least one SLC non-volatile memory element or within the at least one MLC non-volatile memory element;**

As shown at Section IX(A)(4) to meet virtually identical claim language (except “maintain” in element [18c]), Gavens and incorporated references disclose ordinary controller functions including the recited L2P mapping plus ordinary wear leveling with MLC “memory space” and constituent “memory elements,” to the extent understandable, with obvious substitution of “real” SLC for the pSLC mode of Gavens MLC, and thus discloses or makes obvious element **[18d]**. (Sechen ¶ 175]).

5. **[18e] [18e1]determining, using the controller, if a range of addresses listed by an entry and mapped to a similar range of physical addresses within the at least one MLC non-volatile memory element, fails a data integrity test performed at the controller based upon received data retained at the controller and which received data is stored in the at least one MLC non-volatile memory element as stored data; in an event of such a failure, [18e2] remapping, using the controller, the entry to a next available equivalent range of physical addresses within the at least one SLC non-volatile memory element; and [18e3] transferring the stored data from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element using the controller.**

As shown at Section IX(A)(5) to meet virtually identical claim language, Gavens discloses in at least one embodiment a post-write-read error management method including testing at the controller “stored data” in MLC and “retained data,” the “original data” mapped to that MLC location and, upon failure, remapping to pSLC mode memory, which would obviously be substitutable with “real” SLC, thereby disclosing or making obvious claim elements [18e1] and [18e2]. Claim 18, as claim 11, should be invalidated for the unsupported, inconsistent and inoperative element [18e3] requiring “transfer” to SLC of the “stored data” found to have failed the data integrity test. (Section VII(D) *supra*.) If the Board were to correct [18e3] to be consistent with the [18e2] remapping of the logical (original) data, Gavens, with the obvious substitution of “real” SLC, renders obvious claim element **[18e]**. (Sechen ¶¶ 114-115, 176.)

* * * * *

Gavens and its incorporated references, in view of the knowledge of the POSITA, make obvious **claim 18**.

* * * * *

In sum, Gavens (Ex. 1045) and its incorporated references, in view of the knowledge of the POSITA, make obvious each of the Challenged Claims 1-18 of the ‘370 patent. (Sections X(A)-(I) *supra*; Sechen ¶¶ 100-177.)

X. THE PENDING LITIGATIONS IN THE WESTERN DISTRICT OF TEXAS DO NOT WARRANT DENYING INSTITUTION.

With eight current patents asserted by Vervain against Phison based on varying word claims to the same two “data integrity test” and “wear leveling” functions described in the same specification for a known hybrid SLC-MLC NAND flash memory, review by this Board is more appropriate than by the District Court where those word variations can escape scrutiny. Construction of the multiple terms of the eight patents are restricted in number (12) in the District Court (per “side” in related cases as present here), even counting contentions of indefiniteness. As demonstrated in the above-stated grounds (Sections VII-IX *supra*), the case against this patent is compelling. Balancing of the six factors set forth by the Board in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential) does not warrant denying institution here. Rather, institution would best serve the

interest in “system efficiency, fairness, and patent quality” (*id.* at 5), allowing due resolution of the substantial patentability questions (*id.* at 15).

As to *Fintiv* Factor 5, the petitioner and defendant in the parallel proceeding are the same party. Phison filed this petition expeditiously, where it received first notice of Vervain’s assertion in the Complaint filed March 8, 2024, and the First Amended Complaint filed May 13, 2024 (Ex. 1082), leave to amend granted Dec. 18, 2024 (Ex. 1080). No substantive opinions have issued regarding the scope or validity of the Challenged Claims. The parallel proceeding is still in an early stage: the Court recently granted-in-part Phison’s motion to dismiss (*see* Docket List [Ex. 1080] entries 12, 24, 26 and 38), Phison has not otherwise answered, fact discovery just commenced and claim construction materials exchanged in accordance with the Scheduling Order (Ex. 1083). A *Markman* hearing, initially scheduled for December 5, 2024, is postponed until January 9, 2025. ([Ex. 1080] entry 39) Thus, as to Factor 3, there has not been overriding investment in the parallel proceeding; to the contrary, the requirements of the parallel proceeding limited *Markman* construction to twelve terms between the parties for eight patents of verbal variations of the same specification. Thus, as to Factor 4, there is overlap, in the greater inclusiveness of the requested review as the District Court will not consider all the issues properly raised in this Petition, pending PGR2024-00047, PGR2024-00048, IPR2025-00212, IPR2025-00213, IPR2025-00214 and IPR2025-00215, PGR2025-00010 and others

that Petitioner may petition.

Factors 1 and 2 do not significantly weigh for or against instituting the requested IGR. Petitioner does not know if the District Court will stay the case if trial by this Board is instituted and the Court has *tentatively* set jury selection for December 15, 2025 (Scheduling Order [Ex. 1083] at 4).

Regarding the sixth factor, the merits strongly weigh in favor of instituting trial as shown through the strength of the grounds in this Petition. “Other circumstances” favor institution. As described at note 5 *supra*, there are separate suits by Patent Owner Vervain (following the same template) against Phison and a customer (Kingston Docket List [Ex. 1081]). This presents the complexity of eight patents with method and apparatus claims that Vervain asserts against multiple, sometimes competing products (that thus must be held confidential between the defendants) that implicate third-party actors who may be implicated in divided or indirect infringement as users who select the configuration or performance of the claimed system. Moreover, unlike Phison, its customer defendant in the other case moved to dismiss for improper venue and to transfer (Kingston Docket List [Ex. 1081] entries 13 and 20) with attendant discovery and confidentiality proceedings (*id.* entries 15 and 16).

The interest of the public in cleaning away such verbal variants of questionable innovation in the eight Vervain patents are best served by the requested

review. The Board may take notice that such litigation, if it reaches trial, will have been drastically reduced in claims and theories asserted – beginning with the limitation of terms for construction for eight patents. A trial before the Board, in contrast, may resolve all Challenged Claims reviewed, substantially simplifying district court trial without the extensive district court discovery for which the America Invents Act offered this alternative before the Board – especially appropriate for the recent Lifetime Patents issued on verbal variations. And, of course, Petitioner has shown its case to be compelling.

XI. CONCLUSION

Petitioner submits that for the reasons set forth above, it has been shown that more likely than not, the Challenged Claims are invalid under all of 35 U.S.C. §§ 101, 112(a), 112(b), and 103 and should reviewed by the Board and canceled.

Date: December 31, 2024

Respectfully submitted,
Attorneys for Petitioner

/Hsuanyeh Chang, Ph.D./
Hsuanyeh Chang, Ph.D. (Reg. No. 73,431)
hsuanyeh@hsuanyeh.com
Stephen Y. Chow (Reg. No. 31,338)
Stephen.Y.Chow@hsuanyeh.com
Douglas E. Chin (Reg. No. 66,713)
Doug.Chin@hsuanyeh.com
Peter Yi (Reg. No. 61,790)
Peter.Yi@hsuanyeh.com
Hsuanyeh Law Group, PC
11 Beacon Street, Suite 900
Boston, MA 02108
(617) 886-0988

CERTIFICATION OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above-captioned Petition for Inter Partes Review of U.S. Patent No. 11,967,370 (and accompanying exhibits), was served in its entirety on December 31, 2024, upon Patent Owner's correspondent of record via USPS Priority Mail:

*Patent owner's correspondent
address of record for U.S. Patent No. 11,967,370*

*MUNCK WILSON MANDALA L.L.P
P.O. Drawer 800889
DALLAS TX 75380
UNITED STATES*

/Hsuanyeh Chang, Ph.D./
Hsuanyeh Chang, Ph.D. (Reg. No. 73,431)
hsuanyeh@hsuanyeh.com
Stephen Y. Chow (Reg. No. 31,338)
Stephen.Y.Chow@hsuanyeh.com
Douglas E. Chin (Reg. No. 66,713)
Doug.Chin@hsuanyeh.com
Peter Yi (Reg. No. 61,790)
Peter.Yi@hsuanyeh.com
Hsuanyeh Law Group, PC
11 Beacon Street, Suite 900
Boston, MA 02108
(617) 886-9088

CERTIFICATION OF WORD COUNT (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the attached Petition, including footnotes, but not the cover page, exhibit list, table of contents, mandatory notices, and certifications, contains 16,037 words, as measured by the Word Count function of Microsoft Word. This is less than the limit of 18,700 words as specified by 37 C.F.R. § 42.24(a)(ii).

/Hsuanyeh Chang, Ph.D./
Hsuanyeh Chang, Ph.D. (Reg. No. 73,431)