IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

VERVAIN, LLC, Plaintiff, v. PHISON ELECTRONICS CORPORATION, Defendant.	)	C.A. No. 1:24-cv-00259-ADA Jury Trial Demanded

PHISON'S FINAL INVALIDITY CONTENTIONS

Defendant Phison Electronics Corporation ("Phison") discloses its final invalidity contentions to Plaintiff Vervain, LLC ("Vervain"). Phison contends that each of the asserted claims listed on page 2 of Vervain's Preliminary Infringement Contentions served on June 21, 2024, is invalid under 35 U.S.C. §101, § 103, and/or § 112. These contentions are based on Phison's good faith evaluation of information known to Phison at this time. Phison reserves the right to amend or supplement these contentions in view of information obtained later in the case, for example, through discovery, amendments to Vervain's contentions, the Court's claim construction ruling, applicable case law and authorities, and/or any other reasons permitted by the Federal Rules of Civil Procedure, the Local Rules of the Western District of Texas, or an order of the Court. Phison incorporates by reference all invalidity arguments and evidence (e.g., prior art references, declarations, claim charts, and exhibits) in the following cases:

- *Vervain, LLC v. Micron Tech. Inc.*, No. 6:21-cv-00487-ADA (W.D. Tex)
- *Vervain, LLC v. Western Digital Corp.*, No. 6:21-cv-00488-ADA (W.D. Tex.)
- *Vervain, LLC v. Kingston Tech. Co.*, No. 1:24-cv-00254-ADA (W.D. Tex)

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- *Micron Tech. Inc. v. Vervain, LLC*, IPR2021-01547 (P.T.A.B.)
- *Micron Tech. Inc. v. Vervain, LLC*, IPR2021-01548 (P.T.A.B.)
- *Micron Tech. Inc. v. Vervain, LLC*, IPR2021-01549 (P.T.A.B.)
- *Micron Tech. Inc. v. Vervain, LLC*, IPR2021-01550 (P.T.A.B.)
- *Phison Elecs. Corp. v. Vervain, LLC*, PGR2024-00047 (P.T.A.B.)
- *Phison Elecs. Corp. v. Vervain, LLC*, PGR2024-00048 (P.T.A.B.)
- *Phison Elecs. Corp. v. Vervain, LLC*, IPR2025-00212 (P.T.A.B.)
- *Phison Elecs. Corp. v. Vervain, LLC*, IPR2025-00213 (P.T.A.B.)
- *Phison Elecs. Corp. v. Vervain, LLC*, IPR2025-00214 (P.T.A.B.)
- *Phison Elecs. Corp. v. Vervain, LLC*, IPR2025-00215 (P.T.A.B.)
- *Phison Elecs. Corp. v. Vervain, LLC*, PGR2025-00010 (P.T.A.B.)
- *Phison Elecs. Corp. v. Vervain, LLC*, PGR2025-00011 (P.T.A.B.)
- *Kingston Tech. Co. v. Vervain, LLC,* IPR2025-00614 (P.T.A.B.)
- *Kingston Tech. Co. v. Vervain, LLC*, IPR2025-00616 (P.T.A.B.)

I. GROUNDS OF INVALIDITY UNDER 35 U.S.C. § 103

Phison sets forth the following grounds of invalidity under 35 U.S.C. § 103 based on the identified prior art references and/or applicant admitted prior art. Phison contends that each asserted claim is invalid under 35 U.S.C. § 103. Attached are claim charts setting forth where in the prior art references each element of the asserted claims is found. All citations in the claim charts are to the primary reference unless indicated otherwise. The citations in the claim charts are provided as examples and are not meant to exhaustively cite every portion of a reference with the same or similar disclosure. A citation to a figure should be considered a citation to the corresponding description as well, and a citation to a description of a figure should be considered a citation to the figure as well.

A. U.S. Patent No. 8,891,298

As shown in Exhibit A1:

- Claims 1, 3-5, and 11 of the ’298 patent are obvious under 35 U.S.C. § 103 based on U.S. Pat. No. 8,634,240 (“Gavens”).
- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of U.S. Pat. Appl. Pub. No. 2008/0140918 (“Sutardja”).

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- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of U.S. Pat. No. 8,612,804 (“Kang”).

- Claims 1, 3-5, and 11 of the ’298 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Sutardja.

- Claims 1, 3-5, and 11 of the ’298 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of U.S. Pat. Appl. Pub. No. 2009/0327591 (“Moshayedi”).

- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi and Sutardja.

- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi and Kang.

- Claims 1, 3-5, and 11 of the ’298 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Duann, Nelson, “SLC & MLC Hybrid,” Silicon Motion Flash Memory Summit, Santa Clara, CA, Aug. 12, 2008, available at https://files.futurememorystorage.com/proceedings/2008/20080812_F2A_Duann.pdf (last visited July 26, 2024) (“Duann”).

- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Duann and Sutardja.

- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Duann and Kang.

As shown in Exhibit A2:

- Claims 1, 3-5, and 11 of the ’298 patent are obvious under 35 U.S.C. § 103 based on Sutardja.

- Claims 1, 3-5, and 11 of the ’298 patent are obvious under 35 U.S.C. § 103 based on Sutardja in view of Gavens.

As shown in Exhibit A3:

- Claims 1, 3-5, and 11 of the ’298 patent are obvious under 35 U.S.C. § 103 based on Moshayedi.

- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Moshayedi in view of Sutardja.

- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Moshayedi in view of Kang.

- Claims 1, 3-5, and 11 of the ’298 patent are obvious under 35 U.S.C. § 103 based

on Moshayedi in view of Gavens.

- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Moshayedi in view of Gavens and Sutardja.

- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Moshayedi in view of Gavens and Kang.

As shown in Exhibit A4:

- Claims 1, 3-5, and 11 of the ’298 patent are obvious under 35 U.S.C. § 103 based on Duann in view of Gavens.

- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Duann in view of Gavens and Sutardja.

- Claim 11 of the ’298 patent is obvious under 35 U.S.C. § 103 based on Duann in view of Gavens and Kang.

B. U.S. Patent No. 9,196,385

As shown in Exhibit B1:

- Claims 1, 3-5, and 11-13 of the ’385 patent are obvious under 35 U.S.C. § 103 based on Gavens.

- Claims 1, 3-5, and 11-13 of the ’385 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Sutardja.

- Claims 1, 3-5, and 11-13 of the ’385 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi.

- Claim 11 of the ’385 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi and Sutardja.

- Claim 11 of the ’385 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi and Kang.

- Claims 1, 3-5, and 11-13 of the ’385 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Duann.

- Claim 11 of the ’385 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Duann and Sutardja.

- Claim 11 of the ’385 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Duann and Kang.

As shown in Exhibit B2:

- Claims 1, 3-5, and 11-13 of the ’385 patent are obvious under 35 U.S.C. § 103 based on Sutardja.

- Claims 1, 3-5, and 11-13 of the ’385 patent are obvious under 35 U.S.C. § 103 based on Sutardja in view of Gavens.

As shown in Exhibit B3:

- Claims 1, 3-5, and 11-13 of the ’385 patent are obvious under 35 U.S.C. § 103 based on Moshayedi.

- Claim 11 of the ’385 patent is obvious under 35 U.S.C. § 103 based on Moshayedi in view of Sutardja.

- Claim 11 of the ’385 patent is obvious under 35 U.S.C. § 103 based on Moshayedi in view of Kang.

- Claims 1, 3-5, and 11-13 of the ’385 patent are obvious under 35 U.S.C. § 103 based on Moshayedi and Gavens.

- Claim 11 of the ’385 patent is obvious under 35 U.S.C. § 103 based on Moshayedi in view of Gavens and Sutardja.

- Claim 11 of the ’385 patent is obvious under 35 U.S.C. § 103 based on Moshayedi in view of Gavens and Kang.

As shown in Exhibit B4:

- Claims 1, 3-5, and 11-13 of the ’385 patent are obvious under 35 U.S.C. § 103 based on Duann in view of Gavens.

- Claim 11 of the ’385 patent is obvious under 35 U.S.C. § 103 based on Duann in view of Gavens and Sutardja.

- Claim 11 of the ’385 patent is obvious under 35 U.S.C. § 103 based on Duann in view of Gavens and Kang.

C. U.S. Patent No. 9,997,240

As shown in Exhibit C1:

- Claims 1-2 and 6-7 of the ’240 patent are obvious under 35 U.S.C. § 103 based on Gavens.

- Claims 1-2 and 6-7 of the ’240 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Sutardja.

- Claims 1-2 and 6-7 of the ’240 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi.

- Claims 1-2 and 6-7 of the ’240 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Duann.

As shown in Exhibit C2:

- Claims 1-2 and 6-7 of the ’240 patent are obvious under 35 U.S.C. § 103 based on Sutardja.

- Claims 1-2 and 6-7 of the ’240 patent are obvious under 35 U.S.C. § 103 based on Sutardja in view of Gavens.

As shown in Exhibit C3:

- Claims 1-2 and 6-7 of the ’240 patent are obvious under 35 U.S.C. § 103 based on Moshayedi.

- Claims 1-2 and 6-7 of the ’240 patent are obvious under 35 U.S.C. § 103 based on Moshayedi in view of Gavens.

As shown in Exhibit C4:

- Claims 1-2 and 6-7 of the ’240 patent are obvious under 35 U.S.C. § 103 based on Duann in view of Gavens.

D. U.S. Patent No. 10,950,300

As shown in Exhibit D:

- Claims 1-5 and 7-12 of the ’300 patent are obvious under 35 U.S.C. § 103 based on Gavens.

- Claim 5 of the ’300 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi.

- Claim 5 of the ’300 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Duann.

- Claim 10 of the ’300 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Sutardja.

- Claim 10 of the ’300 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi and Sutardja.

- Claim 10 of the ’300 patent is obvious under 35 U.S.C. § 103 based on Gavens in

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view of Moshayedi and Kang.

- Claim 10 of the ’300 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Duann and Sutardja.

- Claim 10 of the ’300 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Duann and Kang.

E. U.S. Patent No. 11,830,546

As shown in Exhibit E:

- Claims 1-6 of the ’546 patent are obvious under 35 U.S.C. § 103 based on Gavens.

- Claim 5 of the ’546 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi.

- Claims 5-6 of the ’546 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Duann.

F. U.S. Patent No. 11,854,612

As shown in Exhibit F:

- Claims 1-6 of the ’612 patent are obvious under 35 U.S.C. § 103 based on Gavens.

- Claim 5 of the ’612 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi.

- Claims 5-6 of the ’612 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Duann.

G. U.S. Patent No. 11,967,369

As shown in Exhibit G:

- Claims 1-6 and 9-10 of the ’369 patent are obvious under 35 U.S.C. § 103 based on Gavens.

- Claim 5 of the ’369 patent is obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi.

- Claims 5-6 of the ’369 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Duann.

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H. U.S. Patent No. 11,967,370

As shown in Exhibit H:

- Claims 1, 3-5, 11, and 14-18 of the '370 patent are obvious under 35 U.S.C. § 103 based on Gavens.
- Claims 14-15 of the '370 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Sutardja.
- Claims 14-15 of the '370 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Moshayedi.
- Claims 14-15 of the '370 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Duann.
- Claims 14-15 of the '370 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of U.S. Pat. No. 8,886,990 ("Meir") and Sutardja.
- Claims 14-15 of the '370 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Meir and Moshayedi.
- Claims 14-15 of the '370 patent are obvious under 35 U.S.C. § 103 based on Gavens in view of Meir and Duann.

I. Additional Prior Art

In addition to the prior art identified in the attached exhibits, Phison identifies below additional prior art that discloses or renders obvious one or more limitations of the asserted claims, is relevant to show the state of the art or the knowledge of a person of ordinary skill in the art (POSITA), or provides reasons for modifying or combining the teachings of the prior art.

- US5043940 Harari
- US5172338 Mehrotra et al.
- US5297148 Harari et al.
- US5315541 Harari et al.
- US5559956 Sukegawa
- US5570315 Tanaka et al.

- US5719808 Harari et al.
- US5721862 Sartore et al.
- US5867429 Chen et al.
- US5903495 Takeuchi et al.
- US6046935 Takeuichi et al.
- US6345001 Mokhlesi
- US6426893 Conley et al.
- US6901498 Conley
- US7366013 Roohparvar
- US7366014 Micheloni et al.
- US7366073 Roohparvar
- US7864572 Yeh et al.
- US8001317 Yeh et al.
- US8103820 Yeh et al.
- US8250286 Yeh
- US20030174555 Conley et al.
- US20040083335 Gonzalez et al.
- US20090138654 Sutardja
- US20090193184 Yu et al.
- US20110099460 Dusija et al.
- US20110302364 Yeh et al.
- US6522580 Chen et al.
- US6567307 Estakhri

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- US6643188 Tanaka et al.
- US6657891 Shibata et al.
- US6901498 Conley
- US6914823 Chen et al.
- US6917542 Chen et al.
- US7000063 Friedman et al.
- US7009889 Tran et al.
- US7254059 Li et al.
- US7336538 Crippa et al.
- US7366826 Gorobets et al.
- US7453712 Kim et al.
- US7366826 Gorobets et al.
- US7505338 Lee
- US7508715 Lee
- US7545673 Lasser
- US7653779 Fein et al.
- US7676626 Lee et al.
- US7733729 Boeve
- US7853749 Kolokowsky
- U57917709 Gorobets
- US8040744 Gorobets et al.
- US8120960 Varkony
- US8214700 Chen

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- US8250333 Gorobets et al.
- US8356152 You
- US8516172 Karamcheti et al.
- US8612804 Kang et al.
- US8656256 Weathers et al.
- US8725938 Yano et al.
- US8972472 Kanter et. al.
- US9026716 Kang et al.
- US20050237814 Li et al.
- US20050251617 Sinclair et al.
- US20060053246 Lee
- US20070061502 Lasser et al.
- US20070266200 Gorobets et al.
- US20070283081 Lasser
- US20080082736 Chow et al.
- US20090228739 Cohen et al.
- US20100017650 Chin et al.
- US20100115192 Lee.
- US20100174845 Gorobets et al.
- US20100174846 Paley et al.
- US20100174847 Paley et al.
- US20100318879 Yu
- US20110087950 Yu et al.

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- US20110096601 Gavens et al.
- US20120311244 Huang et al.
- US8806301 Yu et al
- Bauer et al., A multilevel-cell 32 Mb flash memory. In *1995 IEEE International Solid-State Circuits Conference. Digest of Technical Papers* (Vol. 38, pp. 132-133, 351). IEEE.
- Bez et al., Introduction to Flash Memor, *PROCEEDINGS OF THE IEEE, VOL. 91, NO. 4, APRIL 2003*, 91(4), pp.489–502.
- Boboila & Desnoyers, Write Endurance in Flash Drives – Slides at *Computer Scienc, Department of* Northeastern University
- Brian Kumagai, Pseudo-SLC NAND Improves Critical-App Reliability (https://www.electronicdesign.com/markets/automation/article/21140513/kioxia-pseudo-slc-nand-improves-critical-app-reliabilitywhile-cutting-costs)
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- Hsieh et al., Energy-Efficient and Performance-Enhanced Disks Using Flash Memory Cache, *ISLPED'07, August 27–29, 2007, Portland, Oregon, USA. Copyright 2007 ACM 978-1-59593-709-4/07/0008, pp 334-339*
- Hu et al., "Achieving Page-Mapping FTL Performance at Block-Mapping FTL Cost," *Proceedings of the 2010 IEEE Conference*, *ISBN 978-1-4244-7153-9/10, © 2010 IEEE*

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- Ricco et al., Nonvolatile Multilevel Memories for Digital Applications, *Proceedings of the IEEE*, *vol. 86, no. 12*, Dec. 1998.
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- "512M x 8 Bit/ 1 G x 8 Bit NAND Flash Memory," *Samsung K9L8G08U1A, K9G4G08U0A, K9G4G08B0A Datasheet*, *Preliminary FLASH MEMORY,* Samsung Electronics
- "1 G x 8 Bit/ 2G x 8 Bit NANO Flash Memory," *Samsung K9G8G08B0A-P Datasheet*, *Preliminary FLASH MEMORY,* Samsung Electronics
- "1G x 8 Bit / 2G x 8 Bit NAND Flash Memory, " *Samsung K9LAG08U1A, K9G8G08U0A, K9G8G08B0A, Preliminary FLASH MEMORY,* Samsung Electronics
- "1G x 8 / 2G x 8 Bit NANO Flash Memory," *Samsung K9LAG08U1A,K9G8G08U0A, K9G8G08B0A Datasheet*, *Advance FLASH MEMORY,* Samsung Electronics
- "1G x 8 Bit / 2G x 8 Bit NAND Flash Memory," Samsung K9K8G08U0B, K9WAG08U1B, *Advance FLASH MEMORY,* Samsung Electronics
- "1G x 8 Bit / 2G x 8 Bit NAND Flash Memory," *Samsung K9WAG08U1M,*

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J. Reasons to Combine

It would have been obvious to combine the cited references for one or more of the following rationales. The cited references are analogous art within the same field of endeavor, such as flash memory technology. Therefore, a person of ordinary skill in the art (POSITA) would have known about these references. The cited references disclose solutions that address the same or similar problems, such as data integrity failure, wear leveling, bad block management, and balancing the advantages and disadvantages associated with hybrid systems of single-level cell (SLC) and multi-level cell (MLC) NAND flash memories. A POSITA would have been motivated to combine the teachings of the cited references to solve the problem or

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improve the described technology. The proposed combinations would have yielded predictable results with a reasonable expectation of success, because the proposed combinations combine known elements or known techniques in known ways.

II. GROUNDS OF INVALIDITY UNDER 35 U.S.C. § 112 (AND RELATED NON-SUBJECT MATTER ELIGIBILITY UNDER 35 U.S.C. § 101)

Phison sets forth the following grounds of invalidity under 35 U.S.C. § 112. Each asserted claim is invalid under § 112 for one or more of the grounds explained below, which also include non-subject matter eligibility challenges under § 101, namely lack of utility (inoperativeness) and improper mix of patent classification in hybrid product/process claims. Citations to the common specification are made in reference to the first asserted patent, the ’298 patent.

A. “Memory Element” Is Unsupported, Indefinite and Inoperative

Claim 1-5 and 7-12 of the ’300 patent, claims 1-6 of the ’546 patent, claims 1-6 of the ‘612 patent, claims 1-6 and 9-10 of the ‘369 patent, and claims 1, 3-5, 11, and 14-18 of the ’370 patent are invalid under 35 U.S.C. §§ 101, 112(a) and 112(b) due to its use in the following contexts:

- “memory element(s)” (claims 1, 3-4, 7-8, and 12 of the ’300 patent, claims 1 and 3-6 of the ’546 patent, claims 1 and 3-6 of the ’612 patent, claims 1 and 3-6 of the ’369 patent, and claims 1, 4-5, 11, and 14-18 of the ’370 patent)

The term “memory element” is unsupported and indefinite in context. The specification nowhere mentions the term “element” except in a boilerplate reservation of elements in claim drafting. Specifically, the specification never uses the term “element” to describe a physical unit of memory. Because the word “element” has a very broad meaning, a POSITA would not understand to what unit (or grouping) of memory the term “memory element” in the claims refers in any memory context, let alone the NAND flash technology disclosed. Furthermore,

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"memory element," in the recited contexts fails to supply the physical read/write/erase capabilities required for the NAND flash operation disclosed in the specification to provide a useful system as claimed. Thus, the claims' use of the indefinite term "memory element" fails under 35 U.S.C. § 101 (utility), § 112(b) (definiteness), and § 112(a) (enablement and possession).

B. "Memory Space" Is Unsupported, Indefinite and Inoperative

Claims 1-12 of the '300 patent, claims 1-7 of the '546 patent, claims 1-7 of the '612 patent, and claims 1-6 and 9-10 of the '369 patent are invalid under 35 U.S.C. §§ 112(a) and 112(b) due to the following claim language:

- "memory space containing volatile memory space and nonvolatile memory space, wherein the nonvolatile memory space includes both multi-level cell (MLC) space and single level cell (SLC) space" (claim 1 of the '300 patent, claim 1 of the '546 patent,)
- "memory space containing logical and physical volatile memory space and nonvolatile memory space, wherein the logical and physical nonvolatile memory space includes both multi-level cell (MLC) logical and physical memory space and single level cell (SLC) logical and physical memory space;" (claim 1 of the '369 patent)
- "at least one random access volatile memory element that exists in the logical volatile memory space" (claim 1 of the '369 patent)
- "memory space containing volatile memory" (claim 1 of the '612 patent)
- "remapping . . . the address space to a different physical range of addresses" (claim 1 of the '612 patent).

The word "space" appears in the specification only in the context of the market space for hard disk drives, "HDD space." A POSITA would understand "memory space" to be a *storage capacity property* of a memory. To the extent that "memory space" is an abstraction of the disclosed system physical components of an MLC flash module and a distinct SLC flash module, that use is unsupported by the specification, unenabled for non-NAND flash memory and different physical organizations of NAND flash memory that a POSITA understands include the

input/output circuity required for NAND flash operation. As written in the '300 and '546 patents, the term is also ambiguous as to whether the term refers to an abstract quantity of memory or physical structure. Regarding the '369 patent, the claim recites the nonsensical statement that physical random access volatile memory must *exist* in the logical volatile memory space. As to the '612 patent, a POSITA would understand the term "volatile memory" to be a physical thing; it is nonsensical for a property (memory space or address space) to contain a physical thing (volatile memory). Even if "memory space" in '300 might be construed as logical address space to which physical elements of MLC and SLC nonvolatile memories were "mapped," there is no such mapping for the recited volatile elements – and '369 further divides "memory space" into "logical and physical" memory space – abstract constructs (see section III(A)). Furthermore, "memory element," in the recited contexts fails to supply the physical read/write/erase capabilities required for the NAND flash operation disclosed in the specification to provide a useful system as claimed. Thus, the claims' use of the indefinite term "memory space" fails under 35 U.S.C. § 101 (utility), § 112(b) (definiteness), and § 112(a) (enablement and possession).

C. "Controller" as Recited Is Indefinite.

Claims 1, 3-5, and 11 of the '298 patent, claims 1, 3-5, and 11-13 of the '385 patent, claims 1-2 and 6-7 of the '240 patent, claim 1-5 and 7-12 of the '300 patent, claims 1-6 of the '546 patent, claims 1-6 and 9-10 of the '369 patent, and claims 1, 3-5, 11, and 14-18 of the '370 patent, are invalid under 35 U.S.C. § 112(b) due to lack of disclosure of structure (physical or algorithmic) for the abstract "controller" defined only by function in the claims:

- "controller" (claims 1 and 11 of the '298 patent, claim 1 of the '385 patent, claims 1 and 6 of the '240 patent, claims 1 and 12 of the '300 patent, claim 1 of the '546 patent, claim 1 of the '369 patent, and claims 1, 11, and 16-17 of the '370 patent)

The "system(s) for storing data" of the '298, '385 and '240 patents are recited only as

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three components. Two are physical, an MLC NAND flash module and an SLC flash module, each with "individually erasable blocks" characteristic of and defining NAND flash operation and understood by a POSITA to include the physical circuitry for organizing, reading, writing and erase them. The third is an abstract "controller," not limited to any physical hardware module (NAND flash or otherwise) or software module, and other than being abstractly "coupled" to the two, understood physical modules, limited only as performing recited functions.

Thirty-five U.S.C. § 112(f) has been applied through § 112(b) to find indefinite a functionally claimed limitation of a general term ("nonce" word) which is not supported in the specification by adequate disclosure of structure (physical or algorithmic). "Controller" is such a nonce word, and even if the word suggests some structure, the specification does not adequately disclose structure for its claimed functions. In the independent claims of the '298, '385 and '240 patents, which share recitation of functions a)-d) labeled in '298 claim 1, at least functions c) and d) are inadequately disclosed in the specification's vague description (6:24-35) of "allocating," counting "access" to, and transferring "contents" of "blocks." These terms are ambiguous at different parts of the description as to their reference to the physical blocks that define NAND flash or to the "logical blocks" visible to the host (user) as data, which are mapped and written to different physical blocks upon each update in NAND flash operation (see sections II(F) and II(G)). Claim 11 of the '298 patent and claims 1 and 6 of the '240 patent recite a "periodic basis" applied vaguely in the same description (section II(F)). At least the above vagueness renders the '298, '385 and '240 patents indefinite.

The indefiniteness of "controller" is exacerbated in '300 patent's and the following four patents' claims to systems or methods for storing data by replacing the well-understood physical MLC and SLC modules with the abstract and unsupported terms "memory spaces" (see section

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II(B)) and "memory elements" (see section II(A)), such that there is no understood physical circuitry to define the claimed systems. See section II(O).

In the '300 patent, the functions of the "controller" are "to operate memory elements and associated memory space," to "maintain an address table [that "maps logical and physical addresses adaptable to the system"], and "control[] access" of memory elements "for storage of data therein." The claims also call for the controller to be "operable" to store data in the newly formulated MLC element and a newly recited random access volatile memory. None of this is disclosed in the specification. The claims further call for the controller "performing a data integrity test . . . after at least a Write access operation . . . by comparing the stored data to the retained data" where failure "results in a remapping . . . to achieve enhanced endurance." There is no disclosure of how often and how long after a write operation (assumed for NAND flash operation) an integrity test is performed and how this function "achieves enhanced endurance." Finally, because the controller is responsible for maintaining the address table that does the mapping, its mapping function "is performed as necessitated by the system to maximize lifetime." That function is abstract, indefinite and nowhere disclosed, much less enabled in the specification. (Section II(D).).

The '546 controller is limited to similar functions and thus suffers from lack of structural support in the specification. Additionally, the controller operates "Read access" where there is no disclosure in the specification of "Read access" other than assumed for NAND flash reading (confused in the specification's often imprecise usage of "reading into" instead of "writing").

The '369 controller is limited to functions similar to those noted above regarding the '300 patent and thus suffers from lack of structural support in the specification.

The '370 controller is also limited to similar functions to those described above and thus

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suffers from lack of structural support in the specification. Claim 16 requires that "operations of the controller enhance a lifetime of the at least one MLC non-volatile memory element and the at least one SLC non-volatile memory element." There is no algorithm for this operation disclosed in the specification much less how any operation can enhance the lifetimes of both elements where the disclosed preferential writing decreases the expected lifetime of one element, leaving the expected lifetime of the other unaffected.

Accordingly, each of the patents in suit is invalid for indefiniteness of the recited "controller" for which no structure is provided by the claims or in the specification.

D. "Controlling" as Recited Is Unsupported and Indefinite.

Claims 1-6 of the '612 patent are invalid under 35 U.S.C. §§ 112(a) and (b) at least due to the following claim language:

- "controlling during Write access operations and Read access operations a plurality of MLC memory modules, each including at least one MLC nonvolatile memory element and at least one SLC memory module including at least one SLC nonvolatile memory element and associated memory space using at least one controller" (claim 1 of the '612 patent).

It is unclear what the "controlling" step means or involves when performed "during Write access operations and Read access operations." There are no examples or explanations given in the specification about how the "at least one controller" is "controlling" the "memory modules" and "memory element[s]" "during Write access operations and Read access operations." Therefore, the claims are invalid as unsupported and indefinite.

E. The Limitation that "the mapping . . . performed as necessitated by the system to maximize lifetime" Is Unsupported, Indefinite and Inoperative.

Claims 1-12 of the '300 patent, claims 1-7 of the '546 patent, claims 1-7 of the '612 patent, and claims 1-10 of the '369 patent are invalid under 35 U.S.C. §§ 112(a) and 112(b) and § 101 due at least to the following claim language:

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- "the mapping is performed as necessitated by the system to maximize lifetime" (claim 1 of the '300 patent, claim 1 of the '546 patent, and claim 1 of the '612 patent)
- "the mapping is performed as necessitated by the memory system to maximize lifetime" (claim 1 of the '369 patent)

These claims fail under 35 U.S.C. § 112(a) because the specification does not disclose a mapping technique that maximizes lifetime even for NAND flash memory; as the identified patents expand their reach to "memory elements" other than NAND flash technology for which logical to physical address mapping may be different and remapping of physical addresses for updates to data at a logical address are not required (*e.g.*, PCM). The specification itself makes no claim to *maximize* lifetime, but only to "boost the lifetime" or "provide long lifetime" for a NAND flash storage system, and even then, without providing any explanation of how preferential mapping into an SLC module (under the imperfectly disclosed circumstances of write-fail and "hot blocks") achieves any of those goals or results. The claim to "maximize lifetime" is not enabled (and such an invention not shown to be "possessed") because there is no evidence in the specification that either of the disclosed NAND flash mapping schemes does in fact maximize lifetime of the claimed system or component. The limitation is indefinite in failing to provide notice to a POSITA of what mapping is referenced, what is "necessitated" by what system, and what it means to "maximize lifetime" of what – multiple axes of uncertainty.

There is no connection described or disclosed between the recited "mapping" and any physical action such as writing or any effect on the lifetime of anything. Even a hypothetical (and impermissible) rewriting of the claim to include "writing," would be unsupported, as nothing in the specification discloses what writing, and when it might occur. Each update in NAND flash operation requires remapping to a new physical location, and writing to that location *decreases* expected lifetime of that physical component (which the passing of time also does); preferential writing to some memory lowers the expected lifetime of that component while

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leaving the unpreferred memory in the same state of expected lifetime. Thus, for NAND flash operation, this limitation is inoperative. The mapping to maximize lifetime limitation is unenabled/unpossessed under 35 U.S.C. § 112(a), indefinite under § 112(b), and inoperative under § 101 as failing to define a useful system for storing data since every mapping (and assumed write) does not extend the lifetime of anything, much less "maximize" it.

F. The Limitations Placing "the retained data in the random access volatile memory" Are Unsupported and Indefinite.

Claims 1-5 and 7-12 of the '300 patent, claims 1-6 of the '546 patent, claims 1-6 of the '612 patent, and claims 1-6 and 9-10 of the '369 patent are invalid under 35 U.S.C. § 112(a) due to the following claim language:

- "the retained data in the random access volatile memory" (claims 1 and 12 of the '300 patent)
- "retain such received data in the random access volatile memory as retained data" (claim 1 of the '546 patent)
- "comparing the stored data **in** the controller memory **in** the given one of the MLC nonvolatile memory elements to the retained data that was associated with the stored data in the random access volatile memory by the controller (claim 1 of the '546 patent, claim 1 of the '612 patent, and claim 1 of the '369 patent)
- "the retained data that was associated with the stored data in the random access volatile memory" (claim 1 of the '546 patent, claim 1 of the '612 patent, and claim 1 of the '369 patent)
- "retaining the received data in the random access volatile memory as retained data" (claim 1 of the '612 patent)
- "retain such received data in the random access volatile physical memory element as retained data associated with the stored data" (claim 1 of the '369 patent)

There is no written description support for the above-quoted claim recitations. The specification explains that the retained data is stored in the controller memory, not the random access volatile memory. The claim limitation that the retained data is stored in the random access volatile memory was new matter added by a claim amendment during the prosecution of

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the ’300 patent just after Vervain took over prosecution from Greenthread, LLC. *See* Prosecution History of U.S. Pat. Appl. No. 16/006,299, Amendment at 2 (U.S.P.T.O. Oct. 8, 2020). During the prosecution of the ’546 patent, the applicant argued that the controller memory and the random access volatile memory are two distinct data stores. *See* Prosecution History of U.S. Pat. Appl. No. 17/203,385, Amendment at 11-17 (U.S.P.T.O. Sept. 22, 2023). The inconsistency is further exacerbated by the grammatically confused reference to “stored data” “in the controller memory in the given one of the MLC nonvolatile memory elements.” Thus, the limitations are unsupported under 35 U.S.C. § 112(a) and indefinite under § 112(b).

G. The Object and Count of “Access” Cannot Be Determined and Are Unsupported and Indefinite.

Claims 1, 3-5, and 11 of the ’298 patent, claims 1, 3-5, and 11-13 of the ’385 patent, and claims 1-5 and 6-7 of the ’240 patent are invalid under 35 U.S.C. §§ 112(a) and 112(b) due to the following claim language:

- “accessed most frequently” (claim 1 of the ’298 patent, claim 1 of the ’385 patent, and claims 1 and 6 of the ’240 patent)
- “a count of the number of times each one of the blocks is accessed” (claim 1 of the ’298 patent and claims 1 and 12 of the ’385 patent)
- “accessed less frequently” (claim 12 of the ’385 patent)
- “a count value of those blocks that are accessed most frequently” (claim 6 of the ’240 patent)

The claim recitations divide a confusing two sentences of the specification (6:24-35) that appear to describe wear leveling. The first sentence describes “allocating” into the SLC NAND module “hot” blocks that “receive frequent writes,” which are understood by the POSITA to be “hot” data in the wear-leveling of the time, tracked by logical blocks mapped and remapped to the physical blocks that are a basis of NAND flash systems, and, in known schemes with SLC and MLC memory (discussed in Section I), are written into an SLC NAND module. However,

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the second sentence confusingly recites "maintain[ing] a count of those blocks that are accessed (written) most frequently," reciting a "periodic basis" of numbers of writes and a "count of those blocks that are accessed . . . most frequently" – not the count of access (writes) to those blocks – and at such intervals, the contents of those blocks are transferred into the SLC NAND module. This doesn't make sense if the referenced block were the logical block, as any "content" of that block is in the mapped physical block, which would be transferred to a physical block in the SLC NAND module, and at the next period, transferred again. The claims attempt to rationalize this by separating the import of the first wear-leveling sentence (frequently written data, logical blocks) in controller function c) of the '298 patent and a restatement in controller function d) of transfer of content, carried over in claim 1 of the '385 patent and claim 6 of the '240 patent. However, in claim 1 of the '240 patent, the "counted block" is a physical block in the MLC module and transfer is "of the contents of the counted blocks in the MLC non-volatile memory module determined to have received frequent writes after reaching the predetermined count value" ('240 7:67-8:3, introducing a "threshold" reading of the described periodicity). This is unsupported by the specification. The remaining claims recited above remain ambiguous as in the specification whether access is counted for physical or logical blocks (which determines how those counts are tracked).

H. The Claimed "transfer [of] the contents of the counted blocks" Is Unsupported, Indefinite, and Inoperative.

Claim 1 of the '298 patent, claim 1 of the '385 patent, and claims 1 and 6 of the '240 patent are invalid under 35 U.S.C. §§ 101, 112(a) and 112(b) due to the following claim language:

- "allocate those blocks by transferring" (claim 1 of the '298 patent, claims 1 and 12 of the '385 patent)
- "transfer the contents of the counted blocks" (claim 1 of '240 patent)

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- "transfer the contents of those counted blocks" (claim 6 of '240 patent)

As explained in Section II(F) above, the specification's two sentence description of what appears to be wear leveling (6:24-35) left open not only accesses to which (logical or physical) blocks are counted, but accordingly whether data is transferred from a physical block that reaches a threshold write count (that defines the end of a period) or from physical block mapped to a logical block that has been accessed to above the threshold count. As explained in the previous section, it is pointless to transfer data already known to be "hot" each time the data-writing counted for the logical block reaches the next period. On the other hand, if the count is for writes to a physical block and the count reaches a write threshold (reflecting wear on the block) for writing of "cold" data, transfer of that data to SLC wastes its usefulness of SLC that is intended for more frequent writes. In either case, the transfer is inoperative to enhance the lifetime of the system, the expressed purpose of the claimed inventions. Accordingly, the recited limitations fail under §§ 101, 112(a) and 112(b).

I. The Timing of Testing, Remapping and Transfer Is Indefinite.

Claims 1 and 12 of the '300 patent, claim 1 of the '546 patent, claim 1 of the '612 patent, claim 1 of the '369 patent, and claim 18 of the '370 patent are invalid under 35 U.S.C. § 112(b) due to the following claim language:

- "performing a data integrity test . . . after at least a Write operation" (claims 1 and 12 of the '300 patent, and claim 1 of the '612 patent)
- "performing a data integrity test . . . after the at least a Write operation" (claim 1 of the '546 patent and claim 1 of the '369 patent)
- "determining . . . if a range of addresses fails a data integrity test" (claim 18 of the '370 patent)
- "failure of the data integrity test . . . results in a remapping" (claims 1 and 12 of the '300 patent, claim 1 of the '546 patent, and claim 1 of the '369 patent)
- "remapping, responsive to a failure of the data integrity test" (claim 1 of the '612

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patent)

- "in an event of such a failure, remapping" (claim 18 of the '370 patent)
- "failure of the data integrity test . . . results in . . . transfer" (claim 12 of the '300 patent, claim 1 of the '612 patent
- "transferring" (claim 1 of the '612 patent)
- "in an event of such a failure . . . transferring" (claim 18 of the '370 patent)

The above language directly limits the claimed systems or methods but fails to specify when the functions/steps are performed. The specification is ambiguous, stating in one place that a data integrity test in the disclosed system is performed "after every write" (4:55-56) and in another that it is performed after "each write to an address within a particular address range . . . as time permits" (5:34-36). The latter formulation is indefinite because it doesn't specify what particular logical or physical address provides the condition. A POSITA, manufacturer or user is faced with the question whether the claimed, resource-heavy bit-by-bit matching of "stored data" with "retained data" and transferring into SLC of the latter upon failure (unlike common ECC schemes tolerating some error in the stored data) are required (for infringement) with "every write" or "as time permits" and for the continuous lifetime of the system or otherwise. Phison reserves the possibility of showing that the approach of the claims as construed is practically inoperative. Nonetheless, the recited limitations remain indefinite under 35 U.S.C. § 112 (b).

J. The Recited Transfer of Failed Data Is Unsupported and Inoperative.

Claim 12 of the '300 patent and claims 1, 3-5, 11, and 14-18 of the '370 patent are invalid under 35 U.S.C. §§ 101 and 112(a) due to the following claim language:

- "transfer of data corresponding to the stored data to those remapped physical addresses from those determined to have failed the data integrity test" (claim 12 of the '300 patent)
- "the stored data is transferred from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element" (claim 1 of the '370

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patent)

- "transferring the stored data from the at least one MLC non-volatile memory element to the at least one SLC non-volatile memory element" (claim 18 of the '370 patent)

There is no written description support for transferring data that failed the data integrity check, so that the limitation is unsupported. However, the new matter in the claims is nonsensical: it calls for the "stored data" that was found to fail the recited data integrity test to be transferred into SLC NAND flash memory, thereby propagating incorrect data. This does not define a useful system. The limitations thus fail under 35 U.S.C. §§ 101 and 112(a).

K. The Limitation "determine if a range of addresses listed by an entry . . . fails a data integrity test" Is Unsupported and Inoperative.

Claim 1 of the '298 patent, claim 1 of the '385 patent, claims 1 and 6 of the '240 patent, and claim 1 of the '370 patent are invalid under 35 U.S.C. §§ 101 and 112(b) due to the following claim language:

- "determine if a range of addresses listed by an entry and mapped to a similar range of physical addresses . . . fails a data integrity test" (claim 1 of the '298 patent, claim 1 of the '385 patent, claims 1 and 6 of the '240 patent, and claim 1 of the '300 patent)

Fig. 3B (114) shows the step, "Compare Data Written to NAND FLASH Physical Address Range to Data Read from NAND Flash Physical Address Range," not a range of logical addresses listed by an entry and mapped to physical addresses (of the MLC module) where the data is written before it is tested (compared against "retained data"). The specification stated incorrectly that in step 114: "the NAND flash physical address that was read into device controller memory is compared . . .." The claim limitations do not reflect the correct disclosure and thus are not enabled under 35 U.S.C. § 112(a). The listed claims also are manifestly inoperative under § 101 because they nonsensically compare an address to data.

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L. The Limitations of Random Access Memory Embedded in the Controllers Are Unsupported.

Claim 3 of the ’300 patent, claim 3 of the ’546 patent, claim 3 of the ’612 patent, and claim 3 of the ’369 patent are invalid under at least 35 U.S.C. § 112(a) due to the following claim language:

- “at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller” (claim 3 of the ’300 patent and claim 3 of the ’546 patent)
- “embedding at least one of the random access volatile memory or the MLC and SLC nonvolatile memory elements in the at least one controller” (claim 3 of the ’612 patent)
- “at least one of the random access volatile physical memory element or the MLC and SLC nonvolatile memory elements are embedded in the at least one controller” (claim 3 of the ’369 patent)

There is no description of the random access volatile memory, the MLC nonvolatile memory, or the SLC nonvolatile memory that is embedded inside the controller. For example, Figure 1 illustrates the DRAM 20, the MLC flash (module) 26, and the SLC flash (module) 28 outside of the device controller 14. As stated in Section II(C), there is no disclosure of any physical structure of the controller, except that, in explanation of Fig. 3A, there is introduced “memory within the device controller.” However, the applicant distinguished this controller memory from the random access volatile memory during prosecution. *See* Prosecution History of U.S. Pat. Appl. No. 17/203,385, Amendment at 11-17 (U.S.P.T.O. Sept. 22, 2023). Thus, these limitations fail under 35 U.S.C. § 112(a).

Further, the “embedding” step of claim 3 of the ‘612 patent is inoperative and thus invalid under 35 U.S.C. § 101, because it is not and cannot be any part of a “method for storing data,” but is instead part of a method for constructing a memory system. It could not possibly be implemented along with the actual data storing steps such as maintaining, mapping, storing,

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performing a data integrity test, *etc*., that appear in the base claim. A user of the method of storing data (*i.e.*, a user of the accused devices) would not undertake to manufacture a memory device while using that memory device. The embedding step of claim 3 is thus nonsensical and invalid as noted.

M. The Limitation, "the controller is a software module[] or a firmware module" Is Unsupported.

Claim 2 of the '612 patent is invalid under 35 U.S.C. § 112(a) due to the following claim language:

- "the controller is a software module, or a firmware module containing software updates" (claim 2 of the '612 patent)

As explained in Section II(C), there is no physical structure recited in the specification of the claims for the abstract "controller." The applicant did not describe or claim the controller as any "module," much less a NAND flash controller module that would have incorporated understood structure as the disclosed and recited SLC and MLC modules structure. Thus, this limitation fails under 35 U.S.C. § 112(a).

N. Limitations of Temporary Transfer Are Unsupported and Indefinite.

Claim 14 of the '370 patent is invalid under 35 U.S.C. §§ 112(a) and 112 (b) due to the following claim language:

- "transfer of stored data . . . is temporary" (claim 14 of the '370 patent)

There is no written description support for this claim term. As explained in section II(H), the timing of the transfer is indefinite. As explained in section II(I), this particular transfer is incorrectly recited as transfer of data that is determined to be incorrect. The limitation fails §§ 112(a) and 112 (b).

Claim 15 of the '370 patent is also invalid under 35 U.S.C. §§ 112(a) and 112 (b) due to the following claim language:

- "temporary until an MLC non-volatile memory element is available" (claim 15 of the '370 patent)

As for claim 15, there is no written description support for this limitation. Moreover, there is no claim or specification explanation of what the availability of MLC memory has to do with the data transferred to SLC, and particularly the incorrect data recited in the independent claim 1. There is no claim recitation that the data transferred to SLC would be transferred to newly available MLC, which would be contrary to the import of the disclosed and claimed preferential transfer into an SLC module. Thus, the limitation fails §§ 112(a) and 112 (b).

O. Improper Mixing of Product and Process Limitations Under 35 U.S.C. §§ 101 and 112(b)

All the asserted patents are based on known NAND flash memory systems with variations of three functions following the method steps of Fig. 3A and 3B and the imprecise and apparently ambiguous description of "allocation" and "transfer" relative to frequently written logical or physical blocks. In essence, these are claims to a method of operation of a system. However, stated as system clams reciting the functional steps of the controller (also addressed in section II(C)) the claims are invalid for impermissibly mixing product and process claims across different § 101 classifications, found to be indefinite under § 112(b). *IPXL Holdings, LLC v. Amazon.com, Inc.*, 430 F.3d 1377, 1384 (Fed. Cir. 2005); Manual of Patent Examining Procedure ("MPEP") § 2173.05(p)(II). Reserving assertion against other claims or based other process steps:

Claims 1 and 12 of the '300 patent, and all their dependent claims, are invalid under 35 U.S.C. §§ 101 and 112(b) due to the following claim language:

- "the controller controlling access of the MLC and SLC …" (claims 1 and 12 of the '300 patent)

The "controlling" method step is impermissibly recited within the system claim.

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Claims 1 of the ’300 and ‘546 patents are also invalid under 35 U.S.C. §§ 101 and 112(b) for indefiniteness where the “controller *performing* a data integrity test.” These are method steps within the system claims, which render the claims invalid under *IPXL* and MPEP § 2173.05(p)(II).

Claim 7 of the ’300 patent is also invalid under 35 U.S.C. §§ 101 and 112(b) for indefiniteness where the “controller . . . *remaps* the data.” This is a method step within the system claim, which renders the claim invalid under *IPXL* and MPEP § 2173.05(p)(II).

Claim 11 of the ’298 patent and claim 11 of the ‘285 patent are also invalid under 35 U.S.C. §§ 101 and 112(b) for indefiniteness where the “controller (or FTL) . . . *causes* the transfer of content.” These are method steps within the system claims, which render the claims invalid under *IPXL* and MPEP § 2173.05(p)(II).

P. System Claims Not Incorporating the Disclosed SLC NAND Flash Module and MLC NAND Flash Module Structures Are Unsupported and Inoperative.

Claims 1 and 12 of the ’300 patent, claim 1 of the ‘370 patent and all their dependent claims, are invalid under 35 U.S.C. §§ 101 and 112(a) due to the following claim language:

- “A system for storing data comprising: memory space . . .; at least one controller . . .; at least one MLC nonvolatile memory element . . .; at least one SLC nonvolatile memory element . . .; at least one random access volatile memory . . .; an FTL flash translation layer . . ..” (claim 1 of the ’300 patent)
- “A system for storing data comprising: memory space . . .; at least one controller . . .; at least one MLC nonvolatile memory element . . .; at least one SLC nonvolatile memory element . . .; at least one random access volatile memory . . ..” (claim 12 of the ’300 patent)
- “A system for storing data comprising: an MLC non-volatile memory space . . .; an SLC non-volatile memory space . . .; and a controller . . ..” (claim 1 of the ‘370 patent)

Specifically disclosed in the common specification and recited in the ‘298, ‘385, and ‘240 patents are (1) SLC NAND flash memory modules including individually erasable blocks and (2)

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MLC NAND flash memory modules including individually erasable blocks and circuitry. These are understood by the POSITA to include circuity for physically reading/writing/erasing those blocks of cells of individually writable pages, with substantial differences between SLC and MLC modules (*e.g.*, decoding physical addresses to different page/pass writes). Without the incorporation of the POSITA-understood physical reading/writing/erasing circuitry of the SLC and MLC modules, a system recited with only the controller functions (directing module action) is unsupported under 35 U.S.C. § 112(a) and completely inoperative, failing as a useful system under 35 U.S.C. § 101. The "memory spaces" and "memory elements" recited in claims 1 (even with the FTL) and 12 of the '300 patent and claim 1 of the '370 patent do not provide the required bridge of physical action from a controller to NAND flash modules. As explained in Sections II(A) and II(B), "memory spaces" and "memory elements" are themselves unsupported, indefinite and inoperative. Their substitution for understood NAND flash modules with understood read/write/erase circuitry in the recited claims is unsupported under 35 U.S.C. § 112(a) and renders the claimed systems inoperative under 35 U.S.C. § 101.

Q. System Claims Not Incorporating a Minimum Useful Amount of SLC and MLC Memory Are Unsupported and Inoperative.

Claims 1 and 12 of the '300 patent, claim 1 of the '546 patent, claim 1 of the '369 patent, and claim 1 of the '370 patent, and all their dependent claims, are invalid under 35 U.S.C. §§ 101 and 112(a) due to the following claim language:

- "A system for storing data comprising: memory space . . .; at least one MLC nonvolatile memory element . . .; at least one SLC nonvolatile memory element . . ." (claim 1 of the '300 patent)
- "A system for storing data comprising: memory space . . .; at least one controller . . .; at least one MLC nonvolatile memory element . . .; at least one SLC nonvolatile memory element . . .." (claim 12 of the '300 patent)
- "A system for storing data comprising: memory space . . .; a bank of nonvolatile memory, including: a plurality of MLC memory modules, each including at least one

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MLC nonvolatile memory element; and at least one SLC memory module including at least one SLC nonvolatile memory element . . ..” (claim 1 of the ’546 patent)

- “A memory system for storing data comprising: memory space . . .; a bank of physical nonvolatile memory, including: a plurality of physical MLC memory modules, each including at least one physical MLC nonvolatile memory element . . .; and at least one SLC memory module including at least one physical SLC nonvolatile memory element . . ..” (claim 1 of the ’369 patent)

- “A system for storing data comprising: an MLC non-volatile memory space including at least one MLC non-volatile memory element . . .; an SLC non-volatile memory space including at least one SLC non-volatile memory element . . ..” (claim 1 of the ‘370 patent)

The specification discloses two two-bank embodiments that purport to avail of the superior endurance of SLC. There is suggested a beneficial mix is “SLC NAND flash equal to 12.5% or 25% of MLC NAND flash” (5:10-11), which is consistent with Fig. 4 showing two banks each of 2+ SLC modules compared to 8+ MLC modules (which with MLCs storing twice SLCs, meeting the suggested 12.5% ratio). Figs. 6a and 6b of incorporated U.S. Patent 8,195,452 show a Samsung NAND flash chip K9F108XOA with a “1024M + 32M BIT NAND FLASH ARRAY,” clearly a “module” of 1-bit cells, *i.e.*, SLCs. The context thus is one SLC module of 1,024 blocks of 64 pages each. Contrasting with this context, each of the “system(s) for storing data” recited in the claims of the ‘300, ‘546, ‘369, and ‘370 patents is met with just one SLC memory element and one MLC memory element (for the ‘546 and ‘369 a plurality of MLC memory elements, one each in a plurality of MLC modules). As explained in sections II(A) and II(B), “memory spaces” and “memory elements” are themselves unsupported, indefinite and inoperative, although it is recited in claims 1 and 12 of the ‘300 patent and claim 1 of the ‘546 patent that their systems’ mapping is of “blocks, pages, or bytes of data.” If a single block satisfies the requirements of the systems recited in the claims of the ‘300, ‘546, ‘369, and ‘370 patents, as literally it would (even allowing mapping of two blocks in claims 1 and 12 of the ‘300 patent and claim 1 of the ‘546 patent), that system would not be a useful one. It would be much

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less than the system disclosed by the specification as having multiple SLC and MLC modules each of a thousand blocks, useful for the disclosed and claimed preferential writing to an SLC module. In a minimal, single-blocks system as claimed, there could be no multiple writes to count given the NAND flash requirement of writing each update to another physical address, much less to enhance or maximize lifetime of the block or the system. And there is nothing in the specification describing the sufficient number of blocks or "memory elements" needed for the claimed inventions to enhance or maximize lifetime, or any way to determine a sufficient number. For at least these reasons, claims 1 and 12 of the '300 patent, claim 1 of the '546 patent, claim 1 of the '369 patent, and claim 1 of the '370 patent, and all their dependent claims, are invalid under 35 U.S.C. §§ 101 and 112(a).

R. "Block" Is Indefinite.

Claims 1, 3-5, and 11 of the '298 patent, claims 1, 3-5, and 11-13 of the '385 patent, and claims 1-2 and 6-7 of the '240 patent are invalid under 35 U.S.C. § 112(b) due to the following claim language:

- "block(s)" (claims 1-2 of the '298 patent, claims 1-2 and 12-13 of the '385 patent, claims 1 and 6 of the '240 patent)

The meaning of the claim term "block" is unclear. The specification discloses both logical blocks and physical blocks. A logical block is associated with a unit of data (i.e., the unit of data appears to be stored in the logical block from the perspective of the host computer) and has a logical block address (LBA). '298 patent col. 2:13-17. The host computer manages data, such as files, using logical blocks. *Id.* col. 2:17-23, 2:67-3:1. A physical block represents a unit of memory and has a physical block address (PBA). *Id.* col. 2:31-38, 2:66-67.

The claims ambiguously recite "blocks" without qualifying each instance of the term with either "logical" or "physical." Therefore, a person of ordinary skill in the art reading the claims is

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left to guess whether each instance of the term "blocks" is referring to logical blocks or physical blocks. The specification does not help resolve these ambiguities. For example, the specification describes wear leveling as follows:

> allocate "hot" blocks; i.e., those blocks that receive frequent writes, into the SLC NAND flash memory module 28, while allocating "cold" blocks; i.e., those blocks that only receive infrequent writes, into the MLC NAND flash memory module 26.

Id. col. 6:25-29. These hot blocks and cold blocks are terms of art in the flash memory field that can refer to logical blocks of data that are written (or modified) frequently and infrequently, respectively. It was well known at the time of the asserted patents that wear leveling by transferring hot blocks of data, which are frequently written, to SLC physical blocks that have high endurance and transferring cold blocks of data, which are infrequently written, to MLC physical blocks that have low endurance can prolong the lifetime of flash memory.

The claims, however, appear to conflate logical blocks and physical blocks by using the ambiguous term "blocks." For example, claim 1 of the '298 patent recites, "at least one MLC non-volatile memory module comprising a plurality of individually erasable blocks" and "at least one SLC non-volatile memory module comprising a plurality of individually erasable blocks." These instances of "erasable blocks" refer to physical blocks.

Later, the claim recites, "determine which of the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules are accessed most frequently by maintaining a count of the number of times each one of the blocks is accessed." The claim recitation "the blocks of the plurality of the blocks in the MLC and SLC non-volatile memory modules" has antecedent basis in the "erasable blocks" recited earlier in the claim and thus appears to be referring to physical blocks. However, the specification describes determining hot blocks, which are logical blocks, that receive frequent writes. Thus, it is unclear whether the determined

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"blocks" in the claim is referring to logical blocks or physical blocks.

Next, the claim recites "allocate those blocks that receive the most frequent writes by transferring the respective contents of those blocks to the at least one SLC non-volatile memory module." The claim recitation "those blocks" refers to "which of the blocks," which is a subset of "the plurality of the blocks in the MLC and SLC non-volatile memory modules." Accordingly, the recitation "those blocks" appears to refer to physical blocks. However, if the claim recitation "those blocks" refers to physical blocks, it is unclear how transferring the contents (i.e., data) stored in those physical blocks to the SLC non-volatile memory module would result in allocating "those [physical] blocks" to the SLC non-volatile memory module. On the contrary, Vervain interprets "those blocks that receive the most frequent writes" as logical blocks in its preliminary infringement contentions by alleging that the claim recitation "those blocks that receive the most frequent writes" reads on "frequently accessed *data*." Vervain's Preliminary Infringement Contentions Ex. A-1 at 33 (emphasis added). Thus, even Vervain conflates the meaning of the recited "blocks" as logical blocks and physical blocks.

III. GROUNDS OF INVALIDITY UNDER 35 U.S.C. § 101

Phison sets forth the following grounds of invalidity under 35 U.S.C. § 101. Each asserted claim is invalid under § 101 for one or more of the grounds explained below. Citations to the common specification are made in reference to the first asserted patent, the '298 patent. Other § 101 challenges are presented in Section II above.

A. "memory space"

Claims 1-12 of the '300 patent, claims 1-7 of the '546 patent, claims 1-7 of the '612 patent, claims 1-10 of the '369 patent, and claims 1-18 of the '370 patent are invalid under 35 U.S.C. § 101 because they are directed to or recite the abstract idea of "memory space(s)."

As discussed in section II(B), a POSITA would understand "memory space" to be a

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storage capacity property of a memory. The unqualified claiming of a property is an abstract idea or "disembodied concept" at the heart of what the Supreme Court's 35 U.S.C. § 101 jurisprudence regards as unpatentable subject matter. The claims fail to *integrate* the claimed "memory space" into a practical application, and they do not provide an inventive concept to counterweigh (provide "significantly more than") the unqualified claiming of the property of "memory space". Particularly, the remaining limitations of these claims simply recite "well-understood, routine, and/or conventional" elements in a conventional arrangement and fail to recite an inventive concept. This is further illustrated in the analysis of these claims presented in the §§ 102/103 prior art contentions in section I. Thus, the claims fail the Alice/Mayo test and are ineligible subject matter under 35 U.S.C. § 101.

The same conclusion may be reached for the unqualified nature of the claiming of "memory space," which extends to subject matter well established to be outside of the scope of the patent statute. For example, the claim does not require that the "memory space" property be other than some transitory "signal" (information); it thus is ineligible as a "signal *per se*".

B. "flash translation layer (FTL)… adapted to… maintain an address [map/table]"

The claims of the '385, '300, '546 and '369 patents each claim as a component a "flash translation layer" or FTL. The specification makes clear, and a POSITA would understand, that FTL is a type of software. As such, the FTL is an abstract idea, a process that could readily be performed in the human mind or with the aid of pen and paper. For example, claim 1 of the '385 patent recites "a flash translation layer… adapted to: a) maintain an address map of at least one of the MLC and SLC non-volatile memory modules, the address map comprising a list of logical address ranges accessible by a computer system, the list of logical address ranges having a minimum quanta of addresses, wherein each entry in the list of logical address ranges maps to a

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similar range of physical addresses within either the at least one SLC non-volatile memory module or within the at least one MLC non-volatile memory module." Such a mapping could readily be performed in the human mind. Similarly, claim 1 of the '300 '546, and '369 patent recites an "FTL… maintain(s) an address table…" (It is noted that the '300 patent requires that the "FTL… maintain an address table in one or more of the memory elements and random access volatile memory" and the '369 patent requires that the "FTL… maintain an address table in one or more of the physical memory elements", but this amounts to nothing more than specifying the type of "pen and paper" that must be used for record keeping and does not preclude the FTL be performed as a mental process.) The additional limitations of these claims are "well-understood, routine, and/or conventional," are in a conventional arrangement, and do not meet the eligibility exceptions for claims reciting or directed to an abstract idea. This is further illustrated in the analysis of these claims presented in the §§ 102/103 prior art contentions in section I. Thus, the claims are ineligible subject matter under 35 U.S.C. § 101.

Additionally, the claims of the '385, '300, '546 and '369 patents place no restriction on where the FTL exists. Thus, these claims do not limit the FTL to a non-transitory signal, and all claims of the '385, '300, '546 and '369 patents are thus ineligible as claiming a "signal *per se.*"

IV. DOCUMENT PRODUCTION

Phison has produced the prior art references relied upon in the final invalidity contentions.

Dated: February 28, 2025

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CERTIFICATE OF SERVICE

I, Yanwei Jiang, hereby certify that on February 28, 2025, a copy of the foregoing Phison's Final Invalidity Contentions was served on all counsel of record for Plaintiff Vervain, LLC via electronic mail.

/s/ Yanwei Jiang
Yanwei Jiang