UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: PGR2025-00021
U.S. Patent No. 12,010,838 B2
Issue Date: June 11, 2024

Title: STAIRCASE STRUCTURE FOR MEMORY DEVICE

PETITION FOR POST GRANT REVIEW OF U.S. PATENT NO. 12,010,838 PURSUANT TO 35 U.S.C. §§321-329 AND 37 C.F.R. §42

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1. Claims 1 and 12 26

[1.Pre] "A staircase structure of a memory device, comprising:" 26

[12.Pre] "A memory device comprising": 26

[1.A] / [12.A] "a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and" 27

[1.B] / [12.B] "a landing pad disposed over a second portion of the second material layer," 30

[1.B.1] / [12.B.1] "wherein the landing pad comprises a first side surface and a second side surface," 32

[1.B.2] / [12.B.2] "wherein the first side surface is in contact with the first material layer and the second side surface is laterally displaced from a side surface of the second portion of the second material layer." 33

2. Claim 4 38

[4] "wherein the landing pad comprises a conductive material." 38

3. Claim 5 38

[5] "wherein the conductive material comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof." 38

4. Claims 6 and 20 38

[6] / [20] "wherein the second material layer is disposed over a first portion of another first material layer, and wherein a side surface of a second portion of the another first material layer is laterally displaced from the second side surface of the landing pad." 39

5. Claims 7 and 17 40

[7] / [17] "wherein the second material layer comprises a first conductive material and the landing pad comprises a second conductive material substantially the same as the first conductive material." 41

6. Claim 13 41

[13] "wherein the first side surface comprises a curved side surface." 41

7. Claim 14 49

[14] "further comprising another second material layer disposed on the first material layer, wherein a first lateral distance between the first side surface and a side surface of the another second material layer is smaller than a second lateral distance between the second side surface and the side surface of the another second material layer." 49

8. Claim 15 50

[15] "wherein the second side surface is laterally displaced from the first side surface, and wherein a first lateral distance between the first side surface and the first portion of the second material layer is smaller than a second lateral distance between the second side surface and the first portion of the second material layer." 50

9. Claim 16 52

[16] "wherein the second material layer comprises tungsten, and titanium nitride." 52

10. Claim 19 52

[19] "a dielectric layer disposed over the first material layer and the landing pad, wherein the first material layer comprises a first dielectric material and the dielectric layer comprises a second dielectric material, wherein the first dielectric material is substantially the same as the second dielectric material, and wherein the first dielectric material comprises silicon oxide." 52

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[3] / [18] "wherein a lateral distance between the second side surface and the side surface of the second portion of the second material layer is between 10 nm and 300 nm." .54

C. *Ground 3*: Claims 1, 4-7, 12, 16-17, and 19-20 Are Obvious Over Lee 60

1. Claims 1 and 12 60

[1.Pre] "A staircase structure of a memory device, comprising:" 60

[12.Pre] "A memory device comprising": 60

[1.A] / [12.A] "a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and" 61

[1.B] / [12.B] "a landing pad disposed over a second portion of the second material layer," 63

[1.B.1] / [12.B.1] "wherein the landing pad comprises a first side surface and a second side surface," 64

[1.B.2] / [12.B.2] "wherein the first side surface is in contact with the first material layer and the second side surface is laterally displaced from a side surface of the second portion of the second material layer" 64

2. Claim 4 70

[4] "wherein the landing pad comprises a conductive material." 71

3. Claim 5 71

[5] "wherein the conductive material comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof." 71

4. Claims 6 and 20 72

[6] / [20] "wherein the second material layer is disposed over a first portion of another first material layer, and wherein a side surface of a second portion of the another first material layer is laterally displaced from the second side surface of the landing pad." 72

5. Claims 7 and 17 74

[7] / [17] "wherein the second material layer comprises a first conductive material and the landing pad comprises a second conductive material substantially the same as the first conductive material." 74

6. Claim 16 74

[16] "wherein the second material layer comprises tungsten, and titanium nitride." 75

7. Claim 19 75

[19] "a dielectric layer disposed over the first material layer and the landing pad, wherein the first material layer comprises a first dielectric material and the dielectric layer comprises a second dielectric material, wherein the first dielectric material is substantially the same as the second dielectric material, and wherein the first dielectric material comprises silicon oxide." 75

D. *Ground 4*: Claims 3 and 18 Are Obvious Over Lee and Haller 77

[3] / [18] "wherein a lateral distance between the second side surface and the side surface of the second portion of the second material layer is between 10 nm and 300 nm." .77

E. *Ground 5*: Claims 13, 14, and 15 Are Obvious Over Lee and Park ... 80

1. Claim 13 80

[13] "wherein the first side surface comprises a curved side surface." 80

2. Claim 14 85

[14] "further comprising another second material layer disposed on the first material layer, wherein a first lateral distance between the first side surface and a side surface of the another second material layer is smaller than a second lateral distance between the second side surface and the side surface of the another second material layer." 85

3. Claim 15 87

[15] "wherein the second side surface is laterally displaced from the first side surface, and wherein a first lateral distance between the first side surface and the first portion of the second material layer is smaller than a second lateral distance between the second side surface and the first portion of the second material layer." 87

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LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 12,010,838 B2 to Lu et al. (the "'838 patent")
1002	File History of U.S. Patent No. 12,010,838 B2 to Lu et al.
1003	Declaration of Dr. Jack C. Lee
1004	*Curriculum Vitae* of Dr. Jack C. Lee
1005	U.S. Patent No. 10,229,929 to Kim et al. ("Kim")
1006	U.S. Patent Publication No. 2014/0191389 A1 to Lee et al. ("Lee")
1007	U.S. Patent No. 9,941,153 to Yang ("Yang")
1008	U.S. Patent No. 9,520,402 to Haller et al. ("Haller")
1009	U.S. Patent No. 10,297,543 to Park et al. ("Park")
1010	U.S. Patent No. 9,589,978 to Yip
1011	Aritome, "NAND Flash Memory Technologies" (2016)
1012	Micheloni et al., "Inside Solid State Drives (SSDs)" (2nd Ed. 2018)
1013	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017
1014	U.S. Patent Publication No. 2016/0218107 A1 to Lee ("Lee 107")
1015	U.S. Patent Publication No. 2015/255385 to Lee
1016	U.S. Patent No. 9,373,540 to Hyun
1017	U.S. Patent Publication No. 2011/0031630 A1 to Hashimoto
1018	Excerpts from the File History of PCT/CN2018/098962
1019	File History of U.S. Patent Application No. 16/126,956

Exhibit	Description
1020	File History of U.S. Patent Application No. 16/885,858
1021	U.S. Patent No. 9,343,452 to Yun et al. ("Yun")
1022	U.S. Patent Publication No. 2018/0026046 A1 to Nam et al. ("Nam")
1023	Minute Order (case schedule), Dkt. No. 141, dated September 18, 2024 in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1024	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1025	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, LTD.'s Disclosure of YMTC II Asserted Claims and Infringement Contentions, dated October 2, 2024 in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1026	Docket from *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:24−cv−04223−RFL which has been consolidated with Case No. 3:23-cv-05792-RFL

I. Introduction

Petitioner Micron Technology, Inc. ("Petitioner") requests PGR of claims 1, 3-7, and 12-20 (the "Challenged Claims") of U.S. Patent 12,010,838 (Ex. 1001, the "'838 patent"), assigned to Yangtze Memory Technologies Co., Ltd. ("Patent Owner"). As explained in this Petition, it is more likely than not that at least one of the challenged claims is unpatentable as obvious.

The '838 patent relates generally to 3D NAND memory devices. Typical, prior art 3D NAND devices include vertically oriented strings of memory cells. These memory cell strings pass through alternating layers of conductive and insulating material stacked on a substrate. The stacked conductive/insulating layers of these types of devices were routinely formed with a staircase structure outside of the area where the memory cells are located. This staircase structure allows for electrical interconnection with landing pads on each of the conductive layers.

The '838 patent's claims a memory device with a particular type of landing pad. This Petition addresses independent claims 1 and 12. Both of these claims require "landing pad[s]" located on top of a conductive or "second material layer." Each "landing pad" must have a "first side surface" that is "in contact" with an adjacent insulating layer or "first material layer." The "second side surface" of this same "landing pad" must be "laterally displaced" from the side of the underlying conductive layer. An example of a landing pad structured this way is shown in

Figure 8:

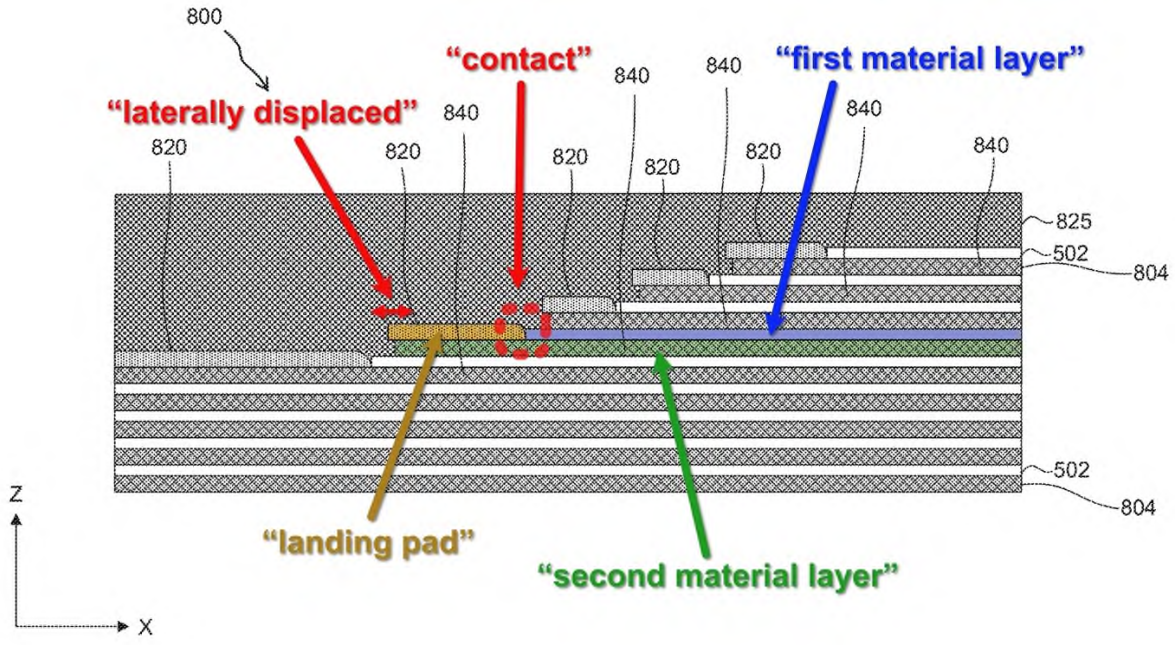


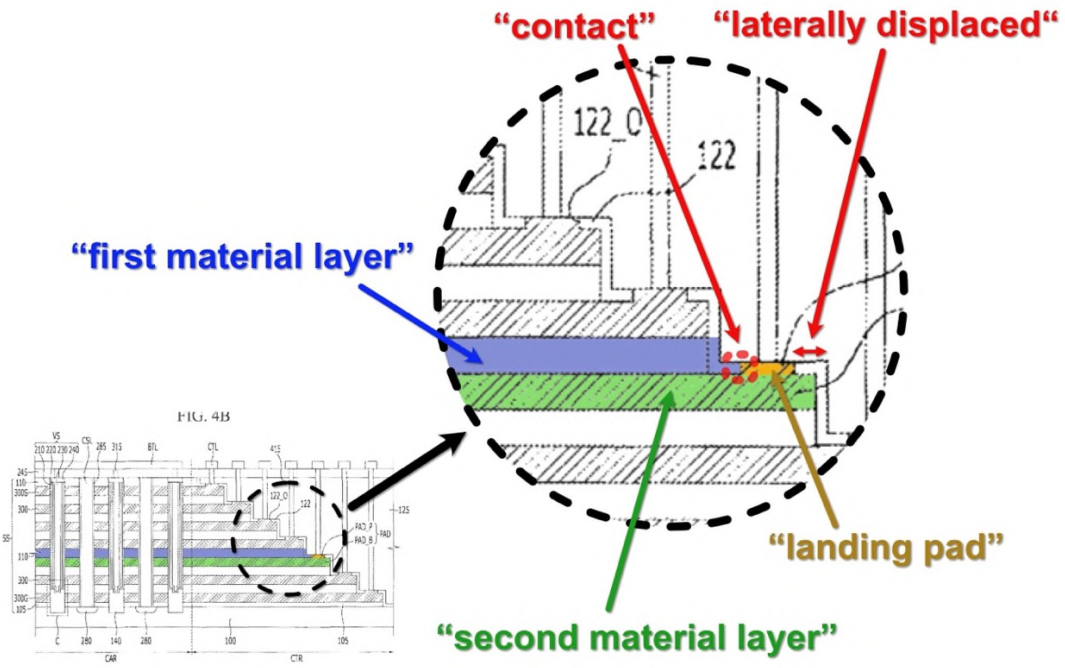
FIG. 8

Ex. 1001, Fig. 8 (annotated).

The prior art makes clear, however, that there was nothing patentable about this. This Petition focuses on the following primary references: U.S. Patent No. 10,229,929 to Kim et al. (Ex. 1005, "Kim") and U.S. Pub. 2014/0191389A1 to Lee et al. (Ex. 1006, "Lee"). Patent claims can be rendered obvious by a single prior art reference that teaches every claim limitation. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1372-73 (Fed. Cir. 2019). This is what both Kim and Lee do: a POSITA would have understood that these references' memory devices include the very type of landing pad that the '838 patent's claims require.

Kim—just like the '838 patent—teaches a 3D memory device with a stacked

staircase structure. The stack is formed from alternating conductive and insulating layers. Further, in Kim, each of the conductive layers in this stack includes a landing pad at its end (which Kim calls a "PAD_P") to facilitate electrical connection. Figure 4B below provides an example:

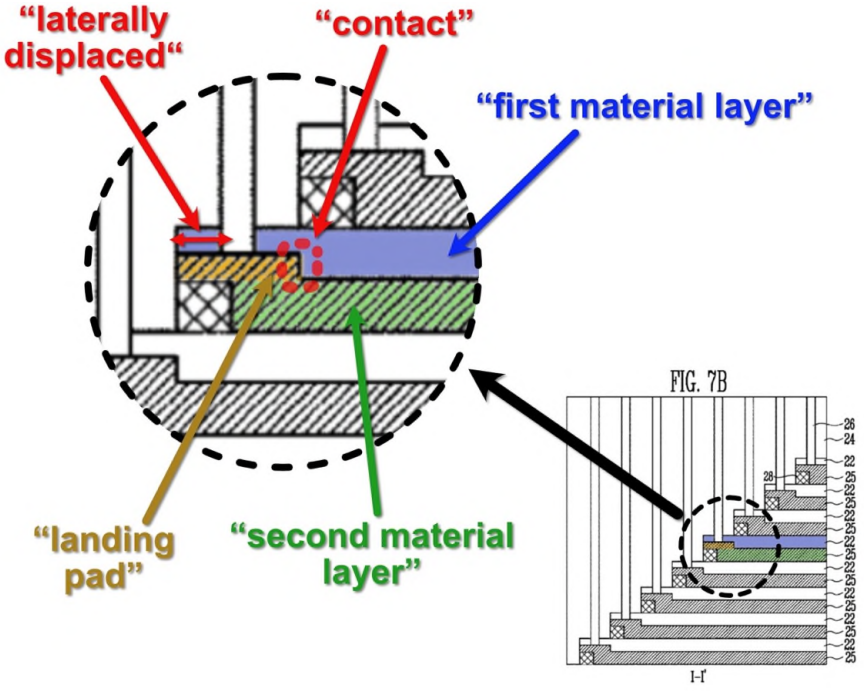


Kim, Fig. 4B (annotated). As shown, Kim's landing pad is in "contact" with the adjacent insulation layer. It is also set back from—and thus "laterally displaced" from—the side of the conductive layer on which it sits. As discussed in ***Ground 1***, this renders claims 1, 4-7, 12-17, and 19-20 obvious

Ground 2 addresses dependent claims 3 and 18. These claims require that the "lateral displace[ment]" of the claimed "landing pad" fall within a specific numerical range: "10 nm and 300 nm." Kim does not discuss the dimensions of its memory device. Another reference—U.S. Patent No. 9,941,153 to Yang (Ex. 1007,

"Yang")—provides this missing information, rendering the claims obvious.

As discussed in ***Ground 3***, claims 1, 4-7, 12, 16-17, and 19-20 are also obvious over Lee. Lee provides yet another example of a 3D memory device. Lee's device includes alternately arranged insulating layers and conductive layers that form a staircase structure. Landing pad—which Lee calls a "pad portion PAD"—are located the end of each conductive layer. Figure 7B of Lee shows one embodiment of Lee's device. In this figure, the side of the pad is aligned with the underlying conductive layer. Lee also teaches that a "barrier layer" 28 can be applied to Figure 7B to increase the distance between the pad and adjacent conductive layers. *See* Lee, [0049]-[0050]; Fig. 8B. The below modified version of Figure 7B shows this:



Id., Fig. 7B (modified to include crosshatched layer 28 and annotated). Due to the

presence of this layer 28, Lee's landing pad is not only in "contact" with the adjacent insulation layer, but it also overhangs and is "laterally displaced" from the conductive layer.

Ground 4 explains why the "lateral displace[ment]" numerical range required by claims 3 and 18 would have been obvious when the example dimensions of U.S. Patent No. 9,520,402 to Haller et al. (Ex. 1008, "Haller") are applied to Lee. Haller teaches a 30 nm thick layer that is structurally and functionally analogous to Lee's layer 28.

Finally, ***Ground 5*** explains why claims 13 and 15—which both require that the landing pad have a "curved" surface—would have been obvious when Lee's square pad is rounded following the teachings of U.S. Patent No. 10,297,543 to Park et al. (Ex. 1009, "Park").

II. Mandatory Notices

A. Real Party-in-Interest

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

On July 12, 2024, Patent Owner YMTC asserted the '838 patent and U.S. Patent Nos. 10,672,711, 10,879,164, 10,879,254, 10,886,291, 11,101,276, 11,145,666, 11,450,604, 11,482,532, 11,568,941, and 11,581,322 against Micron in district court (the "YMTC2 case"). On August 21, 2024, this district court litigation

was consolidated with *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC,* Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) ("Co-Pending Litigation"). U.S. Patent Nos. 10,658,378, 10,861,872, 10,868,031, 10,937,806, 10,950,623, 11,468,957, 11,501,822, and 11,600,342 were asserted by Patent Owner in the first-filed case, leading to a total of 19 patents-at-issue in the now consolidated Co-Pending Litigation.

In addition to this Petition for post grant review, Petitioner is filing (or has filed) petitions for *inter partes* review of the other asserted patents in the Co-Pending Litigations:

Patent	**PTAB Proceeding**	**Wave**
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions

Patent	PTAB Proceeding	Wave
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	
10,672,711	IPR2025-00117	Wave 3 Petitions
10,879,164	IPR2025-00118	
10,879,254	IPR2025-00034	
10,879,254	IPR2025-00119	
10,886,291 (claims 1-5, 8-9, 11-12, & 14-19)	IPR2025-00244	
10,886,291 (claims 6-7, 10, & 20)	IPR2025-00294	
11,101,276	IPR2025-00228	
11,145,666	IPR2025-00189	
11,450,604	IPR2025-00035	
11,482,532	IPR2025-00245	
11,568,941	IPR2025-00190	
11,581,322	IPR2025-00191	
12,010,838	IPR2025-00229	

Petitioner previously filed a petition seeking IPR of the claims of the ’838 patent in November 2024. *See* IPR2025-00229. Because the petition in that prior proceeding was filed within the 9-month window following the ’838 patent’s June

2024 issuance, Petitioner intends to move to terminate the premature IPR in lieu of this timely PGR.

C. Counsel, Service, and Fee Information

Petitioner designates the following counsel:

Lead Counsel	**Back-Up Counsel**
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Petitioner consents to service by electronic mail at the following addresses: P52PTABDocket@orrick.com, PTABDocketJJL2@orrick.com, PTABDocketJ3B3@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner attaches a Power of Attorney.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

III. Requirements for PGR

A. Grounds for Standing

Petitioner certifies that the '838 patent is available for PGR, and that Petitioner is not barred or estopped from requesting this PGR. The '838 patent claims priority back to an August 2017 foreign filing and an August 2018 PCT application. As a result, it is subject to the provisions of the AIA. The patent issued on June 11, 2024. This petition is being filed within 9 months of that date.

B. Identification of Challenge and Statement of Precise Relief Requested

Petitioner requests PGR of claims 1, 3-7, and 12-20. This petition discusses claim construction, explains why the claims are unpatentable, provides details regarding where the various claim limitations are found in the prior art, and is supported by the accompanying Declaration of Dr. Jack C. Lee (Ex. 1003), a leading expert in the 3D memory field.

The application underlying the '838 patent—U.S. App. 17/447,456—was filed September 13, 2021. The patent facially identifies itself as a continuation of May 28, 2020 and September 10, 2018 U.S. applications and an August 6, 2018 PCT filing. Ex. 1001, Cover. The patent also makes a priority claim back to an August 28, 2017 foreign filing. *See id.* For purposes of this Petition only, it is assumed that the '838 patent is entitled to the benefit of this August 28, 2017 date.

Petitioner relies on Kim (Ex. 1005), Lee (Ex. 1006), Yang (Ex. 1007), Park

(Ex. 1009), and Haller (Ex. 1008). These references are all prior art to the '838 patent. *See* Section VII.B.

Petitioner challenges claims 1, 3-7, and 12-20 on the following grounds:

Ground 1: Claims 1, 4-7, and 12-17, and 19-20 are obvious over Kim;

Ground 2: Claims 3 and 18 are obvious over Kim and Yang;

Ground 3: Claims 1, 4-7, 12, 16-17, and 19-20 are obvious over Lee;

Ground 4: Claims 3 and 18 are obvious over Lee and Haller; and

Ground 5: Claims 13, 14, and 15 are obvious over Lee and Park.

IV. Institution Should Be Granted

Petitioner has established that the '838 patent's claims are unpatentable. All other requirements for PGR have been met. The Board should institute PGR.

A. There Are No Grounds for a § 314 Discretionary Denial in this Case

There is a pending district court action involving the '838 patent. The PTAB has explained that it "will not … discretionarily deny institution in view of parallel district court litigation where a petition presents compelling evidence of unpatentability." 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: the claims of the '838 patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute a post-grant proceeding in light of a parallel district court

proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) ("*Fintiv*"). In particular: the district court may stay the case, any potential trial will occur years from now, little district court work has occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes PGR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24, 7 (PTAB June 16, 2020) (informative); *Fintiv* 6-9, 12 (similar).

2. Proximity of the Court's Trial Date

The Board has noted that this factor does not weigh against institution if final decision and trial could occur at approximately the same time. *Nvidia Corp. v. Invensas Corp.*, IPR2020-00603, Paper 11, 19 (PTAB Sept. 3, 2020). On September 18, 2024, the district court entered a scheduling order which set a trial date of June 15, 2026. *See* Ex. 1023. If PGR is instituted, it should be nearing completion by this time. Moreover, given the amount of time until trial, it is also entirely possible that trial will occur much later than scheduled. *See also* Ex. 1024 (indicating an average of 48.9 months to trial). This weighs in favor of institution. *See, e.g.*,

Juniper Networks, Inc. v. Wsou Invs., LLC, IPR2021-00538, Paper 9 at 9-10 (PTAB Aug. 18, 2021).

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings and consolidation, little substantive progress has been made. Virtually no substantive progress has been made in connection with the later asserted YMTC patents. This includes the '838 patent and other "Wave 3" patents discussed above. *See supra* § II.B. The parties have exchanged preliminary infringement and invalidity contentions for the Wave 3 patents but have not taken any depositions regarding any of the patents in the Co-Pending Litigation. Fact discovery is still ongoing. Terms for construction have been identified, but no claim-construction positions have been exchanged for the Wave 3 patents, no briefing has been filed, no claim-construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution*, 10-11.

The Board also has explained that institution is appropriate where "the petitioner filed the petition expeditiously…." *Fintiv*, 11. Here, on July 12, 2024, PO asserted eleven Wave 3 patents against Petitioner—asserting 149 claims for the Wave 3 patents. Ex. 1025. Petitioner proceeded with diligence, starting the filing

of eleven petitions approximately three months after being served with the YMTC2 complaint. Ex. 1026. This petition was filed within six months of the filing of the Complaint. This also weighs strongly in favor of institution.

4. Issue Overlap

Should the Board institute, Micron stipulates that it will not advance in District Court any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution,* 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that plainly teaches the claimed subject matter. Thus, this factor also weighs in favor of institution.

B. Denial Under § 325(d) Would Be Inappropriate

Kim was not cited by Patent Owner or considered by the Examiner during prosecution of the ’838 patent. *See generally* Ex. 1002. While Lee is identified on the face of the patent among many other references, it was not discussed by the

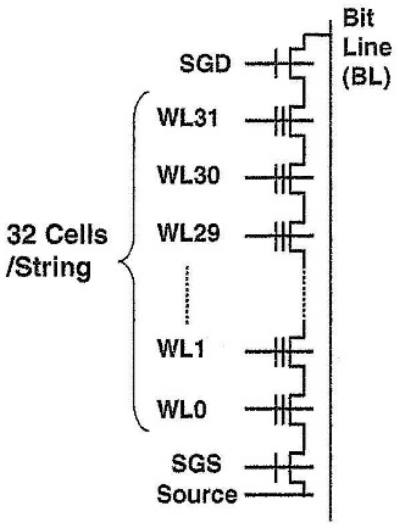
Examiner or used to reject any of the pending claims. Indeed, as explained in Section V.C below, the Examiner only rejected claims 1 and 12 for double patenting. These claims were not rejected over any third-party prior art. While certain other originally filed claims in the '838 patent were rejected over other, different third-party prior art, these claims did not require the same type of "landing pad" that is both in "contact" with insulation and "laterally displaced" from a conductive layer that claims 1 and 12 now require. Thus, the issues and prior art references raised by this Petition are unique and were not the subject of any meaningful discussion during prosecution. Moreover, it constituted error for the Examiner to allow claims 1 and 12. The claims plainly embrace prior art memory devices, including those disclosed in Kim and Lee.

V. The '838 Patent

A. Technological Background

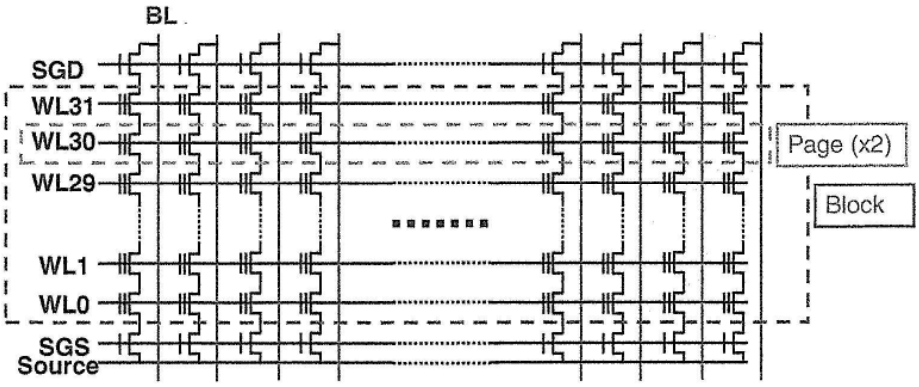
The '838 patent and the prior art discussed in this petition relate to 3D memory. One type of memory that is often implemented as 3D memory is "flash memory." Ex. 1010, 1:24-28. "NAND flash" stores data in a "cell" formed from a transistor. Ex. 1011, 38-39; Ex. 1012, 109; *see also* Ex. 1003, ¶¶ 39-46.

NAND cells are arranged in "string[s]" with multiple cells "connected in series." Ex. 1011, 38. Word lines connect to each memory cell's control gate. *Id.*, 38-39. One such string is shown below:

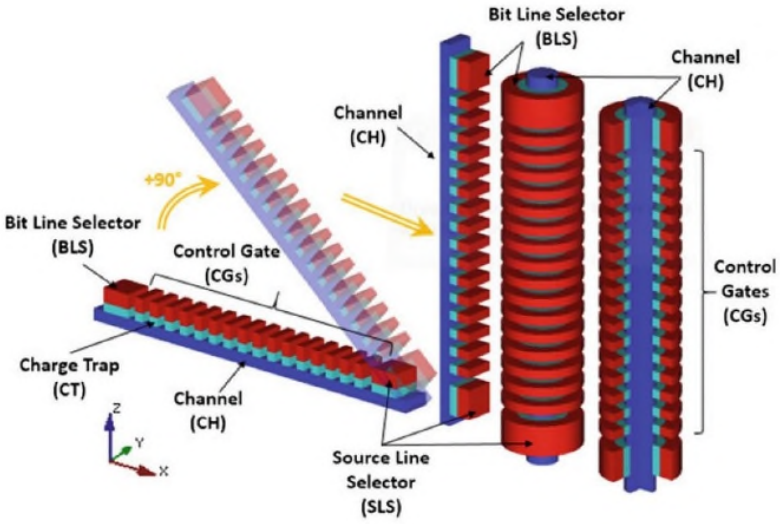


Id., 39.

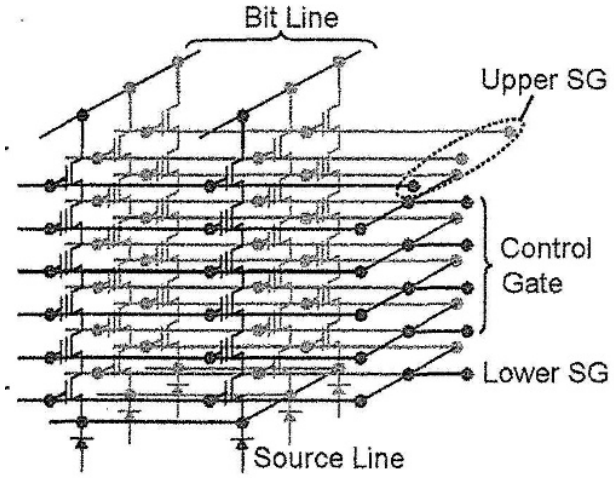
Early NAND devices were formed as two-dimensional arrays of cells on a substrate surface. Ex. 1011, 38.



Id., 40. "[T]o further scale down the memory cell size," 3D NAND was developed in 2006. *Id.*, 292. A "modern 3D NAND structure" effectively "turn[s] the 2D NAND string upside" "resulting" in a "3D structure" with a "vertical channel." Ex. 1013, 3.



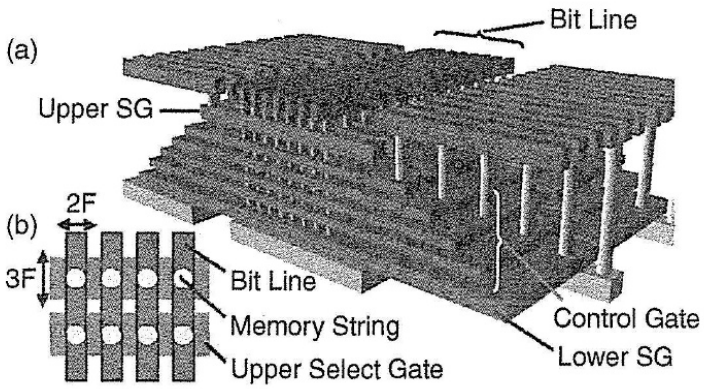
Ex. 1012, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



Ex. 1011, 296; *see also* Ex. 1003, ¶¶ 47-55.

3D NAND includes "multi-stacked layers of gate (plate)" material alternated with "dielectric" in a "[s]tack." Ex. 1011, 294. "Each" layer of "electrode plate acts as a control gate." *Id.*, 295. "[T]he control gates … are connected" to the memory's

"metal layers at [a] stair-like gate structure" with contact points located outside the memory array. *Id.*, 295, 297.



Id. at 296; *see also* Ex. 1003, ¶¶ 56-61.

B. Overview

The '838 patent relates to "a staircase structure for" a "3D memory device…." Ex. 1001, 1:41-43. The patent purports to provide "yield and manufacturing cost improvements." *Id.* at 1:43-46. But it never explains why that is the case.

The patent's "3D memory device" includes a "staircase structure[.]" Ex. 1001, 5:34-36. As shown in Figure 8, the staircase structure includes alternating "insulating layer[s] 502" and "wordline layer[s] 804." *Id.*, 9:51-55. Each wordline includes a "landing pad 820 and a conductive layer 840" and is intended to "control a portion of a memory string in the stacked storage region of a memory device." *Id.*, 9:62-66. The "landing pad 820 contacts a portion of a side of insulating layer 502." *Id.*, 9:66-10:3. The "landing pad 820" can be "made of the same or different conductive material as conductive layer 840." *Id.*, 10:6-10.

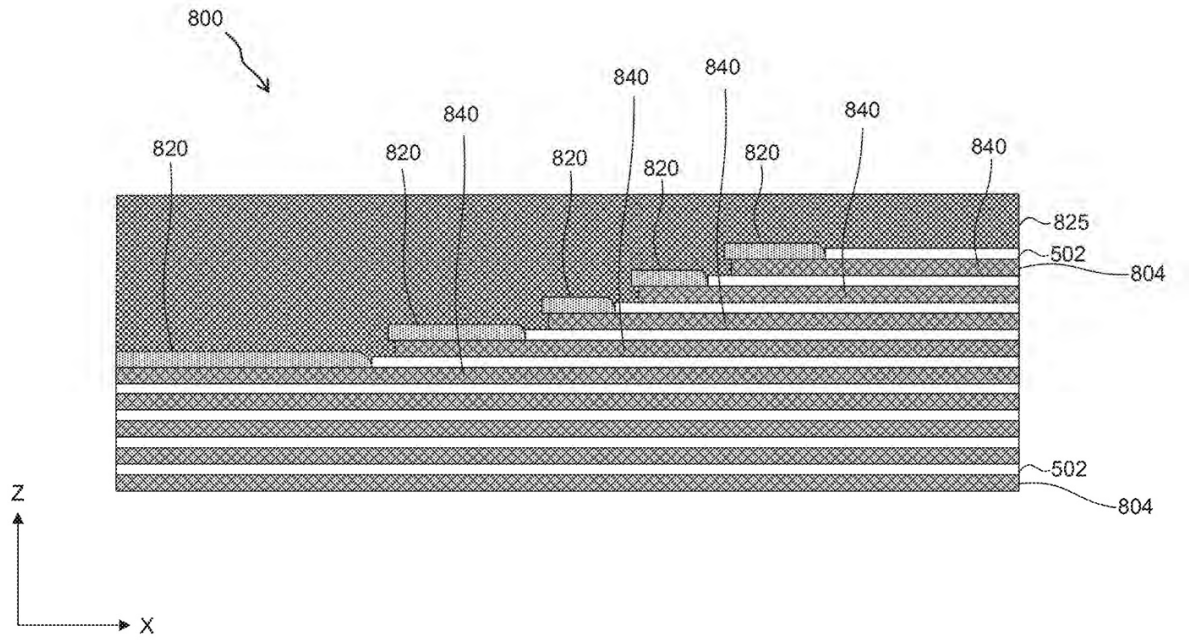


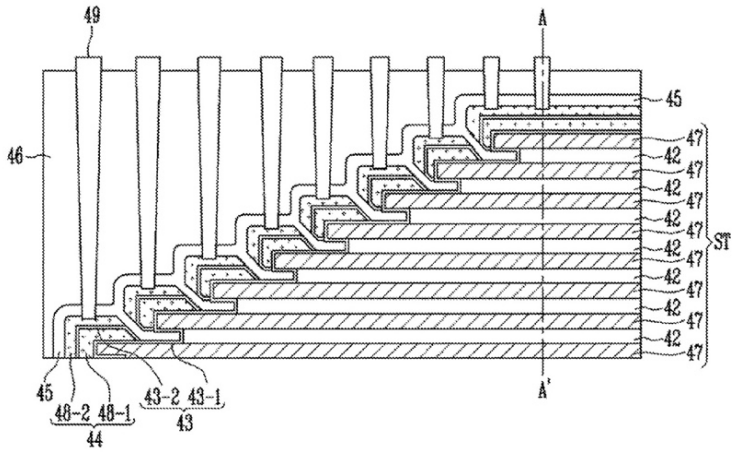
FIG. 8

Id., Fig. 8.

C. Prosecution History

The ’838 patent was filed September 13, 2021 as U.S. App. 17/447,456 (the “’456 App.”). *See* Ex. 1001, Cover. Original independent claim 1 of the patent was rejected as anticipated by U.S. Pub. 2016/0218107A1 to Lee (“Lee 107,” Ex. 1014). Ex. 1002, pp. 150-159. Lee 107 is different from the Lee reference addressed in this Petition. Original claim 1 of the ’838 patent also differs from issued claim 1: rather than including limitations relating to a landing pad’s “side surface[s],” it referenced the pad’s “bottom” and “top” surfaces. *Id.*, p. 39. In support of the rejection, the Examiner relied on Figure 4C from Lee 107:

FIG. 4C



Id., p. 154 (citing Ex. 1014, Fig. 4C). Another independent claim—claim 9 (which corresponds to issued claim 1)—was only rejected for double patenting. Ex. 1002, pp. 155-158. In response, the applicant cancelled claim 1 and filed a terminal disclaimer. *See id.*, pp. 192-200. This then led to allowance of claim 9. *See id.*, pp. 202-209. While prosecution continued in connection with certain other claims, no additional prior art was discussed. *See id.*

The ’838 patent also identifies itself as a continuation three other applications. *See* Ex. 1001, Cover. Prior art was discussed during prosecution of these applications. *See, e.g.*, Exs. 1015-1017. But none of this art was used to reject the ’838 patent’s claims. *See generally* Ex. 1002. And none includes the same disclosure as Kim and Lee. Moreover, the claims at issue in these other applications were materially different from claims 1 and 12 of the ’838 patent. *See, e.g.*, Ex. 1018, pp. 21-24; Ex. 1019, pp. 36-39; Ex. 1020, pp, 31-32.

VI. Claim Construction

The Board applies the same *Phillips* claim construction standard used by district courts. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). For purposes of this petition, Petitioner submits that the terms of the '838 patent's claims do not require further construction and can be afforded their plain and ordinary meaning. *See* Ex. 1003, ¶ 90.

The '838 patent's specification does include a section discussing the meaning of certain of the terms used by claims 1 and 12. For instance, the specification explains that the terms "on," "above," and "over" "should be interpreted in the broadest manner such that 'on' not only means 'directly on' something, but also includes the meaning of 'on' something with an intermediate feature or a layer therebetween." Ex. 1001, 4:4-12. The patent also explains that "the term 'layer' refers to a material portion including a region with a thickness." *Id.*, 4:39-48. A "layer can be a region of homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure." *Id.*, 4:46-48. "[A] layer can be located between any set of horizontal planes" and can even "include multiple layers." *Id.*, 4:48-59. A POSITA would have recognized that none of this operates to limit the '838 patent's claims. *See* Ex. 1003, ¶¶ 145-147, 161-162. Instead, it simply serves to confirm that the patent intends the claims to be

interpreted broadly. *See id.* Additional details regarding how a POSITA would have interpreted the '838 patent's claims are provided in the sections below.

VII. Level of Ordinary Skill in the Art

A POSITA in the field of the '838 patent would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) 3D memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may substitute for professional experience). *See* Ex. 1003, ¶¶ 36-37. This POSITA would also have been aware of and generally knowledgeable about 3D memory's structure, its component parts, and how it operates. *Id.*

VIII. Prior Art Overview

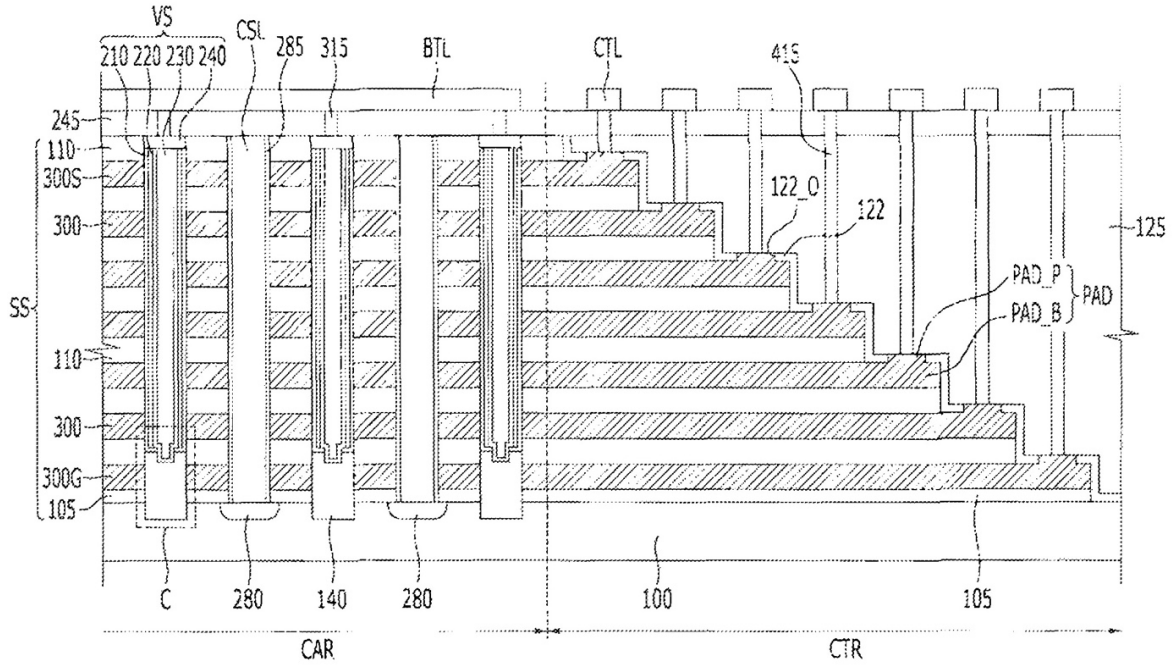
A. Kim

Kim was filed in the U.S. on July 18, 2017. Kim, Cover. It is prior art under AIA § 102(a)(2).

Kim relates to "semiconductor memory devices having enhanced reliability." Kim, 1:38-39. Kim's device can be implemented as a "3D semiconductor memory device[.]" *Id.*, 1:26-30. The device includes a "cell array region" CAR and a "contact region" CTR. *Id.*, 1:41-46. The "contact region" includes a "contact structure" with a "stepwise structure." *Id.*, 1:40-47.

Figure 4B provides an example of Kim's "contact region":

FIG. 4B

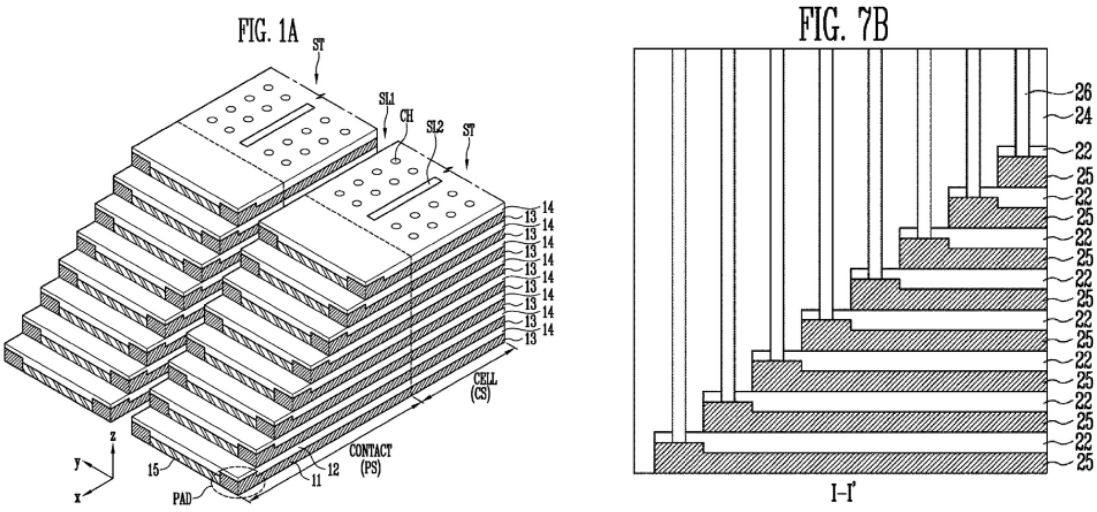


Kim, Fig. 4B. As shown, a staircase-shaped "stacking structure SS" is formed from a "plurality" of alternating "insulating layers 110 and … gate electrodes 300" located over a "substrate 100." *Id.*, 5:53-55; Fig. 4B. The "gate electrodes" are formed from conductive material. *Id.*, 6:31-35. The insulating layer 110 can be integrated with an "auxiliary insulating layer 122." *Id.*, 9:29-38. Each gate electrode 300 includes a "pad unit PAD" formed from "a base pad PAD_B and a protrusion pad PAD_P…." *Id.*, 7:58-62. The pad units PAD "electrically and physically connect" the gate electrodes 300 to an upper "connection line CTL." *Id.*, 9:64-66. As shown in Figure 4B, "protrusion pad PAD_P" is located "inside" and is touching the sides of "opening 122_O" in Kim's insulation layer 122. *Id.*, 9:21-23.

B. Lee

Lee was filed in the U.S. on March 18, 2013 and published July 10, 2014. Lee, Cover. It is prior art under AIA §§ 102(a)(1) and 102(a)(2).

Lee relates to "three-dimensional (3D) non-volatile memory devices." Lee, [0005], [0008]-[0009]. The device includes a "stacked structure ST" with alternately arranged "insulating layers" and "conductive layers." *Id.*, [0020]-[0021]. The "stacked structure ST" is "patterned stepwise." *Id.*, [0021]. According to Lee, existing three-dimensional memories encountered difficulties when "form[ing] pad portions": contacts could either punch through or not contact the conductive layer resulting in electrical problems. *Id.* To address this, Lee includes "pad portions PAD" at the end of each of conductive layers in a "contact region CONTACT" of its "stacked structure ST." *Id.*, [0022]-[0023]. "The pad portions PAD" have a "greater thickness than unexposed portions of the … conductive layer[s]." *Id.*, [0023].



Id., Figs. 1A, 7B. Per Lee, a "barrier layer" 28 can be included under each of its contact pads to shorten the underlying conductive layer and ensure that there is "sufficient distance" between conductive parts. *Id.*, [0049]-[0050]; Fig. 8B.

C. Yang

Yang was filed in the U.S. on December 22, 2016 and published April 10, 2018. Yang, Cover. It is prior art under AIA §§ 102(a)(1) and 102(a)(2).

Yang relates to "a pad" for a 3D "memory device" with a staircase structure. Yang, 1:6-10; *see also id.*, Fig. 2. Yang discusses the dimensions of its device's staircase, conductive and insulating layers, and pads at length. *See id.*, 5:45-6:28; 7:22-65; 10:7-21.

D. Park

Park was filed in the U.S. on June 13, 2017 and issued on May 21, 2019. Park, Cover. It is prior art under AIA § 102(a)(2).

Park relates to a "vertical semiconductor device" with an array of "stacked" "memory cells." Park, 1:14-19. The device includes a staircase-shaped "connection region" with alternating conductive gate electrodes and insulating layers. *Id.*, 6:7-11. Raised "[p]ad region[s] PAR" are located on the ends of gate electrodes. *Id.*, 6:7-11, 6:36-47, 7:4-16. Rather than having straight sides, an "end 79b" of each of these "raised pad portion[s]" 78 may be "rounded" to "prevent a short circuit" between the pad and an "adjacent … conductive layer pattern 72c." *Id.*, 11:35-41; Fig. 7

E. Haller

Haller (Ex. 1008) was filed in the U.S. on August 25, 2015 and issued December 13, 2016. Haller, Cover. It is prior art under AIA §§ 102(a)(1) and 102(a)(1).

Haller relates to a "3D memory device" with a "staircase structure." Haller, 4:8-12. Haller's device includes an "etch stop" at the end of each of its conductive wordline layers. *Id.*, 2:6-9. The etch stop is dimensioned to "prevent … physical or electrical contact" between adjacent wordlines. *Id.*, 2:19-23; *see also id.*, Fig. 9

IX. The Challenged Claims of the '838 Patent Are Obvious

A. *Ground 1*: Claims 1, 4-7, 12-17, and 19-20 Are Obvious Over Kim

Kim, when considered in view of the knowledge of a POSITA, renders claims 1, 4-7, and 12-17, and 19-20 obvious.

1. Claims 1 and 12

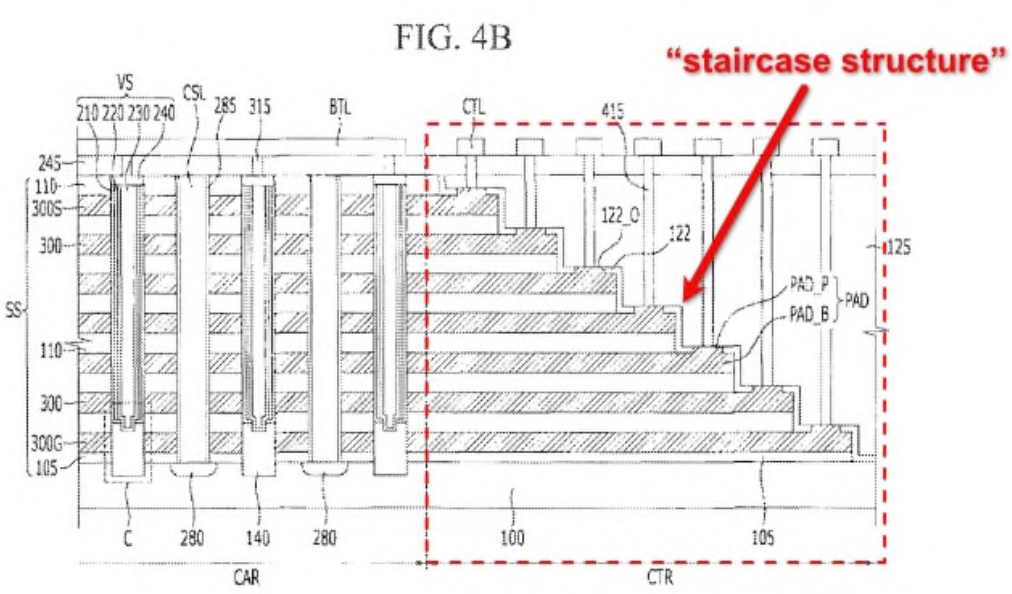
With the exception of their preambles, independent claims 1 and 12 are identical. Thus, they will be assessed together.

[1.Pre] "A staircase structure of a memory device, comprising:"

[12.Pre] "A memory device comprising":

To the extent this preamble language is limiting, it is taught by Kim. Kim relates to "a semiconductor memory device." Kim, Abstract; *see also id.*, 1:15-17; 1:38-39; 3:43-44; Fig. 1. This device can be a "3D semiconductor memory device[]" with "memory cells … arrayed in 3D" for purposes of improving "integration." *Id.*, 1:26-30; *see also id.*, Figs. 3, 4A, 4B, 5-9; Ex. 1003, ¶¶ 132-136.

Kim's memory device includes a ***"staircase structure."*** The device includes both a "cell array region" and an adjacent "contact region." Kim, 1:40-47. The "contact region" has a "stepwise structure." *Id.; see also id.*, 1:15-17; *see also id.*, 3:52-62; 5:33-39; 6:42-46. Kim's ***"staircase structure"*** is annotated in Figure 4B below:



Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 137-143.

[1.A] / [12.A] "a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and"

Claims 1 and 12 next require a ***"first material layer"*** that is ***"disposed over a first portion"*** of a ***"second material layer."***

As explained, the '838 patent uses the term "layer" broadly: a "layer" does not need to be only a single, defined layer of homogenous material. Instead, a "layer can include ***multiple*** layers" and can be "***inhomogeneous***." Ex. 1001, 4:39-59 (emphasis added). The patent also explains that a "layer" can simply be material "located between any set of horizontal planes…." *Id.*, 4:48-51.

Kim teaches what this limitation requires. Kim's memory device includes a staircase-shaped "stacking structure SS" formed from a "plurality" of alternating "insulating layers 110 and … gate electrodes 300" located "on the substrate 100."

Kim, 5:53-55; *see also id.*, 1:41-46.

According to Kim, "[t]he plurality of insulating layers 110 may be, for example, silicon oxide layers." Kim, 6:35-36. The device also includes an "auxiliary insulating layer 122." *Id.*, 9:12-13. "The auxiliary insulating layer 122 may include the same or similar material as the insulating layer 110" such that "a boundary between the auxiliary insulating layer 122 and the insulating layer 110 may not be distinguished and the auxiliary insulating layer 122 and the insulating layer 110 may form one structure." *Id.*, 9:29-38. Moreover, right after patterning its staircase, Kim forms the auxiliary layer 122, such that portions of the conformal insulating layer becomes "one structure" with the insulating layers 122 to extend the insulating layers in the horizonal direction. *Id.*, 12:34-37.

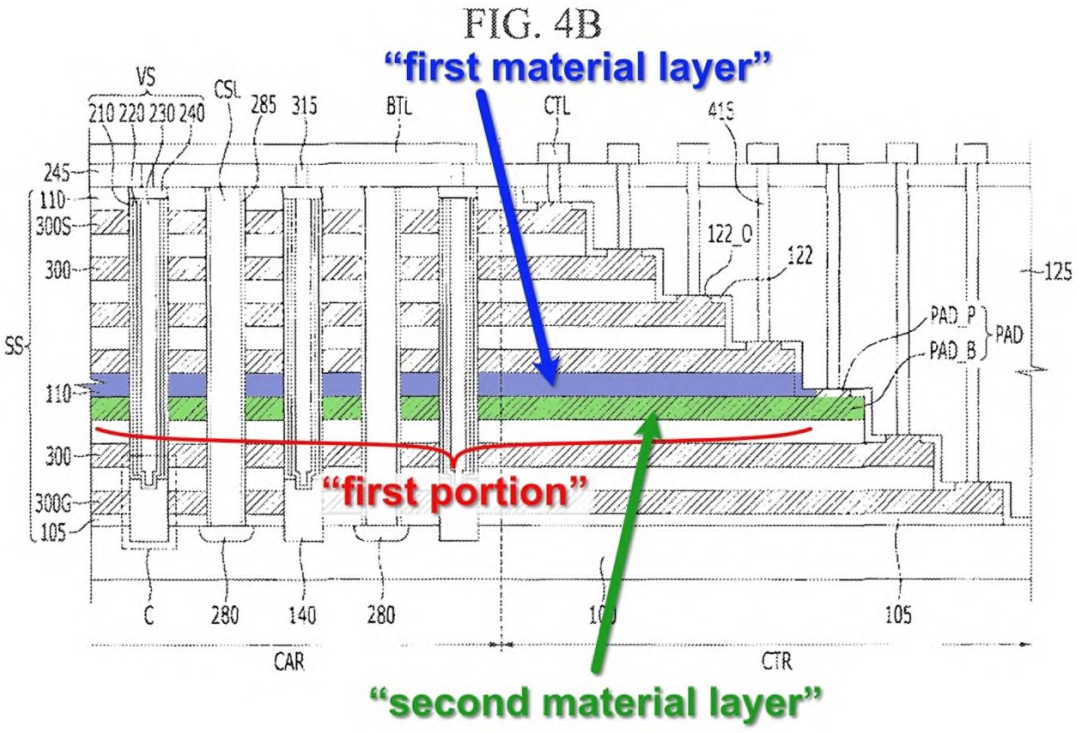
A POSITA would have understood that Kim's insulating layer 110 and the adjacent portion of auxiliary insulation layer 122 together constitute the claimed ***"first material layer."*** *See* Ex. 1003, ¶¶ 144-154. Layers 110 are located between and serve to separate the gate electrodes 300 making up Kim's stack. Kim, 5:53-55; Fig. 4B. Further, layer 122 also forms an integral part of this same stacked, layered structure. Layer 122 is not simply a conformal or protecting layer of oxide applied over complete conductive layers with contact pads. Instead, this layer is applied ***before*** Kim's contact pads are formed. *See id.*, 12:34-37; Fig. 11. Moreover, the layer is used to form the contact pads: the pads are formed within a shaped opening

etched in this insulating layer 122. *See id.*, 12:61-13:11, 13:51-14:17; Figs. 13, 16, 17. The layer 122 remains behind in Kim's final device. *See, e.g., id.*, Fig. 17. Put another way, unlike other layers in Kim like "buried insulating layer 125" (*see id.*, 9:56-63), layer 122 does more than simply cover and protect the staircase's conductive layers. It is used to define and is thus part of Kim's stacked staircase structure. *See* Ex. 1003, ¶¶ 154-163. Because of this, and because these layers are formed from the same material such that they "form one structure" as Kim explains, a POSITA would have understood that they together form a ***"first material layer."*** *Id*. Again, the '838 patent plainly embraces insulating layers—like that taught by Kim—formed from multiple components. *See* Ex. 1001, 4:39-56 (a "layer" can be "inhomogeneous" and formed from "multiple" layers). Moreover, consistent with the '838 patent's explanation that a "layer" can be the material "located between any set of horizontal planes" (*id.*, 4:48-51), in Kim insulating layer 110 and the adjacent portion of auxiliary insulating layer 122 are located between the planes formed by the bottom of one gate electrode 300 and the top of another gate electrode 300. *See, e.g.*, Kim, Fig. 4B.

Next, Kim's device also includes the claimed ***"second material layer"***: there are "gate electrodes 300" located between insulating layers in the stacking structure. Kim, 5:53-55; *see also id.*, 1:41-46. The "gate electrodes 300" can be formed from conductive material such as, among other things, "metal." *Id.*, 6:31-35; Ex. 1003, ¶¶

164-166.

An example ***"first material layer"*** (the combination of insulating layer 110 and auxiliary insulating layer 122) and ***"second material layer"*** (the gate electrode 300) are annotated in Figure 4B below. As shown, the ***"first material layer"*** is ***"disposed over a first portion"*** of the ***"second material layer"***:



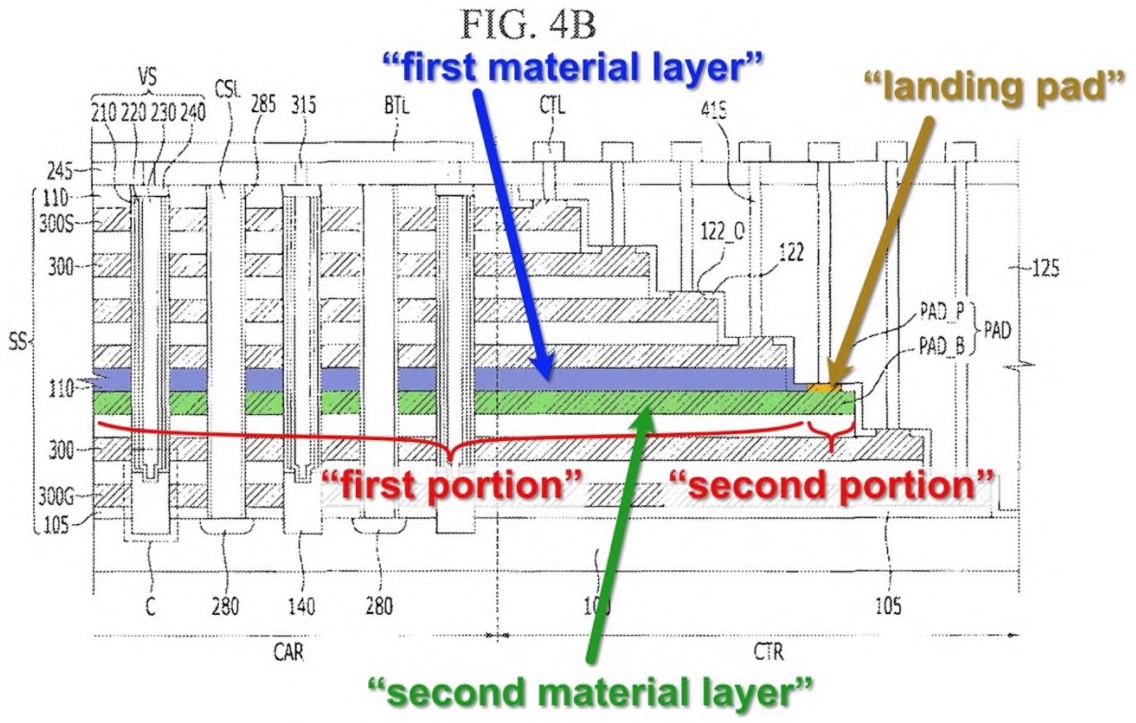
Kim, Fig. 4B (annotated); *see also* Ex. 1003, ¶ 167.

[1.B] / [12.B] "a landing pad disposed over a second portion of the second material layer,"

Kim teaches the claimed ***"landing pad."*** Per Kim, "[a]n end of" each of its "gate electrode[s] 300" is "exposed through the stepwise structure" and includes a "pad unit PAD" formed from "a base pad PAD_B and a protrusion pad PAD_P…." Kim, 7:58-62. "The base pad PAD_B may be a part of the gate electrode 300 in the

contact region CTR." *Id.*, 7:63-64. "The protrusion pad PAD_P may contact the … uppermost surface of the base pad PAD_B." *Id.*, 8:3-10; *see also id.*, 7:61-62; 10:23-25. The pad units PAD "electrically and physically connect[]" the gate electrodes 300 to a "connection line CTL" via a "word line contact plug 415." *Id.*, 9:64-66. The "gate electrode 300" and the attached "base pad PAD_B and … protrusion PAD_P" may be formed from the same "common material composition" such as a "metal." *Id.*, 6:31-35, 14:12-17.

This is shown in Figure 4B. Kim's device includes a ***"landing pad"*** (protrusion pad PAD_P) that is located over a ***"second portion"*** of a ***"first material layer"*** (the PAD_B at the end of gate electrode 300):

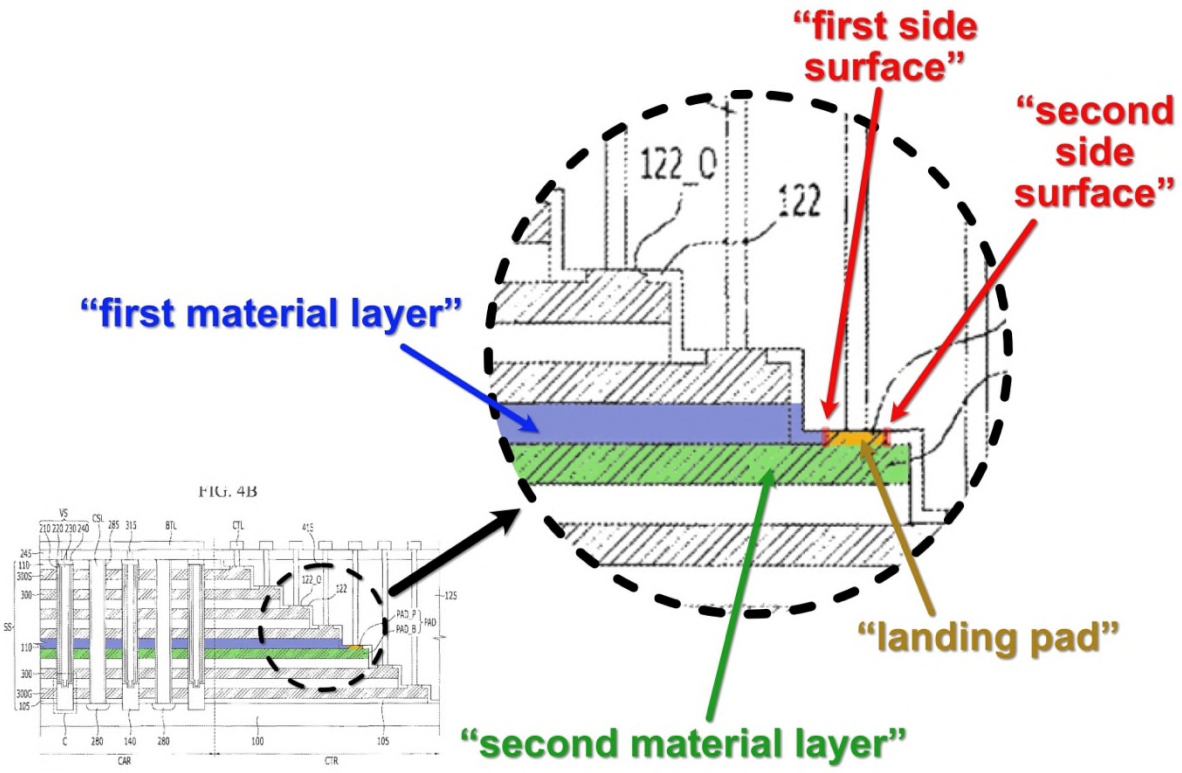


Kim, Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 168-175.

[1.B.1] / [12.B.1] "wherein the landing pad comprises a first side surface and a second side surface,"

This is taught by Kim. In Kim, each "gate electrode 300" includes a "pad unit PAD" at its end. Kim, 7:58-59. And each of these "pad unit[s]" includes a "base pad PAD_B and a protrusion pad PAD_P contacting a surface of the base PAD_B." *Id.*, 7:59-62. As explained above, Kim's "protrusion pad PAD_P" is the claimed ***"landing pad."***

Kim also discusses the shape of this protrusion pad. In particular, the "protrusion pad PAD_P" extends upward from the "surface of the base pad PAD_B" such that it has an "island shape" or a "step with respect to the surface of the base pad." Kim, 8:23-28. The "protrusion pad" can also have a "rectangular parallel[] shape" with either straight or "curved" side surfaces. *Id.*, 8:29-34. This results in the ***"landing pad"*** (the protrusion pad PAD_P) having both a ***"first side surface"*** (the side facing inwards towards the stacking structure) and a ***"second side surface"*** (the side facing outwards) as these claims require:

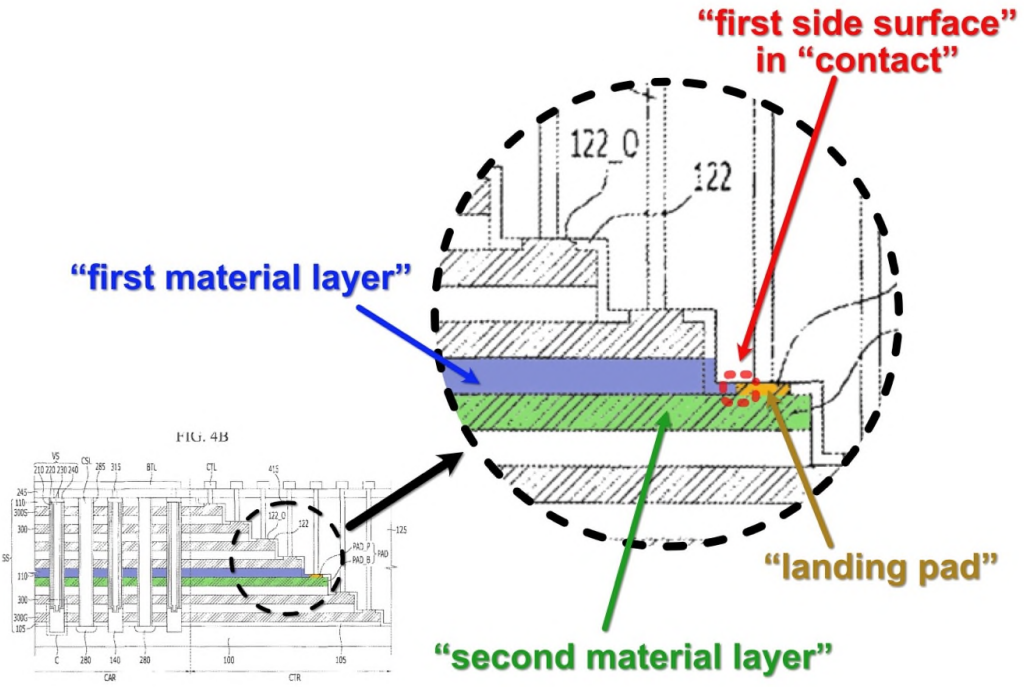


Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 176-182.

[1.B.2] / [12.B.2] "wherein the first side surface is in contact with the first material layer and the second side surface is laterally displaced from a side surface of the second portion of the second material layer."

Kim, in view of the knowledge of a POSITA, renders this limitation obvious. To begin, the ***"first side surface"*** of Kim's ***"landing pad"*** is in ***"contact with the first material layer"*** as required. As explained, Kim's stacking structure includes "insulating layers 110" and "auxiliary insulating layers 122" made from the same material such that they "form one structure." Kim, 9:29-38; *see also id.*, 12:34-37, Fig. 11. Together, layers 110 and 122 correspond to the claimed ***"first material layer."*** *See* Ex. 1003, ¶¶ 185-187. Kim also explains that "auxiliary insulating layer 122" has an "opening 122_O and the protrusion pad PAD_P" is located "inside" this

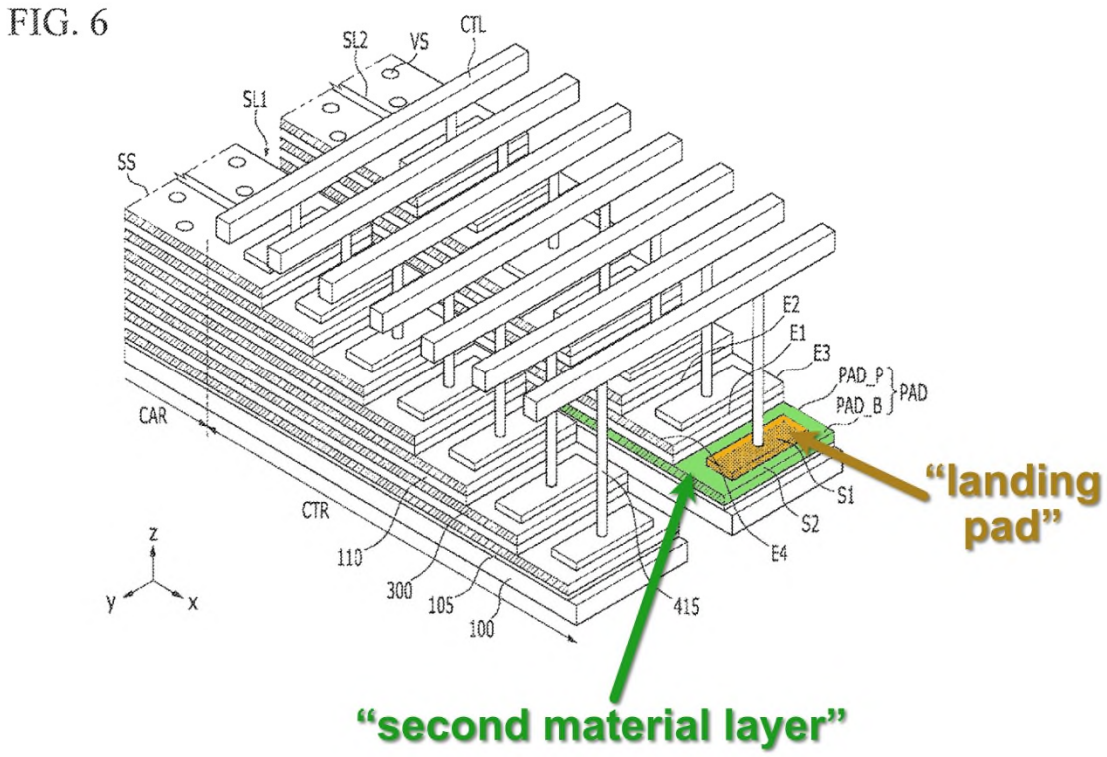
"opening 122_O." Kim, 9:21-23; *see also id.*, 13:51-14:17, Figs. 16-17 (opening 122_O filled with conductive material to form PAD_P during gate electrode forming process). Because Kim's protrusion pad PAD_P is located within and fills the opening 122_O in its auxiliary insulation layer 122, a POSITA would have understood that there is ***"contact"*** between the ***"first side surface"*** of Kim's ***"landing pad"*** (protrusion pad PAD_P) and its ***"first material layer"*** (auxiliary insulating layer 122 adjacent to insulating layer 110):



Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 188-190.

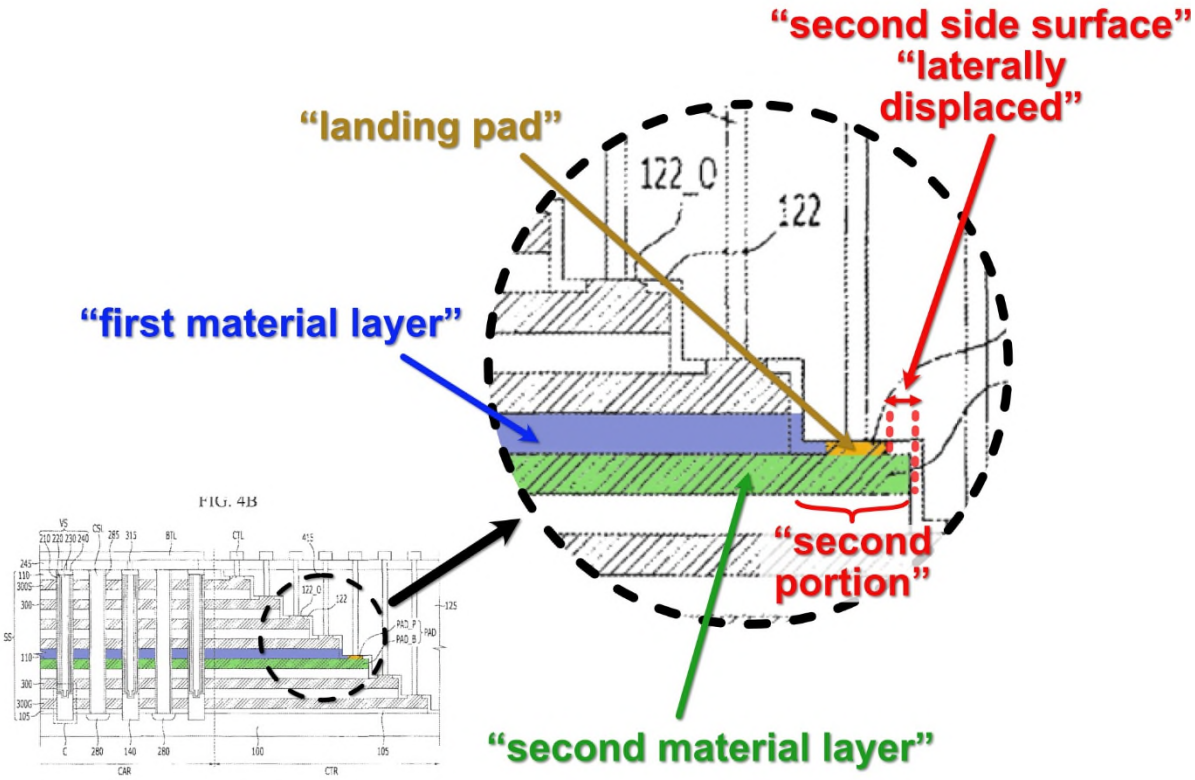
Next, Kim explains that its "base pad PAD_B may include four edges E1, E2, E3, and E4." Kim, 8:35-36. Edges E1 and E2 are "perpendicular to the extension direction (x-direction) of the gate electrode 300" (*i.e.*, at the point where the base

pad begins along the electrode's length, and at the very end of the gate electrode). *Id.*, 8:36-46. The "protrusion pad PAD_P" may be formed and located such that it is "***inside*** from the edges E1 and E2" and does not "align[]" with or "overlap" those edges. *Id.*, 8:47-51 (emphasis added). Thus, "[t]he protrusion pad PAD_P may have a shape in which the protrusion pad PAD_P is ***inside and spaced apart from the edges E1 and E2***" leaving "portions S2 of the respective base pad PAD_B" uncovered by protrusion pad PAD_P. *Id.*, 8:51-59; *see also id.*, 8:11-22 ("pad PAD_P … may be smaller than the entire area … of the base pad PAD_B.") An example of this is shown in the three-dimensional view provided in Figure 6. As shown, the protrusion pad PAD_P is situated away from and inside the edges E1 and E2 defining the beginning and end of the base pad PAD_B at the end of the gate electrode 300 (note that layer 122 is not shown in this figure):



Id., Fig. 6 (annotated); *see also id.*, Figs. 5, 7.

Figure 4B provides a cross-sectional view. As shown, because Kim's ***"landing pad"*** (protrusion pad PAD_P) is located inside the edges of the underlying ***"second portion of the second material layer"*** (base pad PAD_P at the end of electrode 300), the landing pad's ***"second side surface"*** (the pad's rightmost side in the figure) is ***"laterally displaced"*** from the ***"side surface of the second portion of the second material layer"*** (the end of electrode 300):



Kim, Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 191-196. While the '838 patent's figures do provide an example of a landing pad that overhangs an underlying conductive layer, the claims are not limited to just this arrangement. Instead, the claims provide only that the "landing pad" be "laterally displaced" from the side surface of the underlying layer. The claims do not specify or limit the direction in which this displacement occurs. It follows that the landing pad can either be displaced inward and back from the edge of the underlying conductive layer (like Kim's landing pads) or displaced outward and away from the edge of the conductive layer (like the example landing pads shown in Figure 8 of the '838 patent). *See id.*, ¶¶ 197-200. Consistent with this, the '838 patent explains that the term

"lateral/laterally" simply means "nominally parallel to a lateral surface of a substrate." Ex. 1001, 5:6-8. Thus, any displacement in a direction parallel to the substrate surface qualifies as the claimed "lateral displacement." *See* Ex. 1003, ¶¶ 201-202.

2. Claim 4

Claim 4 depends on claim 1 and further requires:

[4] "wherein the landing pad comprises a conductive material."

This is taught by Kim. Kim explains that its "gate electrode 300" along with the attached "base pad PAD_B and … protrusion PAD_P" can all be formed from the same "common material composition" such as a "metal." Kim, 6:31-35, 14:12-17; *see also* Ex. 1003, ¶¶ 203-205.

3. Claim 5

Claim 5 depends on claim 4 and further requires:

[5] "wherein the conductive material comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof."

This is also taught by Kim. Per Kim, its pad can be made from material falling within the claim scope, including "metal (for example tungsten, copper, and aluminum), metal nitride …, or a combination thereof." Kim, 6:31-35; *see also* Ex. 1003, ¶¶ 206-209.

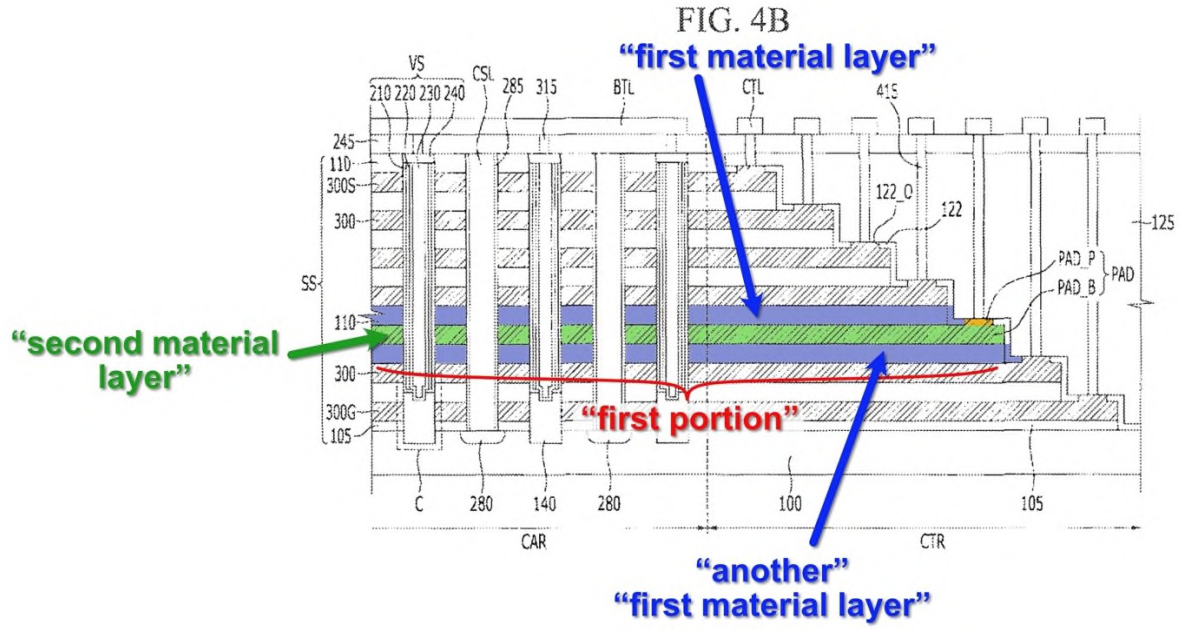
4. Claims 6 and 20

Claim 6 depends on claim 1. Claim 20 depends on claim 12. Both claims

further require:

[6] / [20] "wherein the second material layer is disposed over a first portion of another first material layer, and wherein a side surface of a second portion of the another first material layer is laterally displaced from the second side surface of the landing pad."

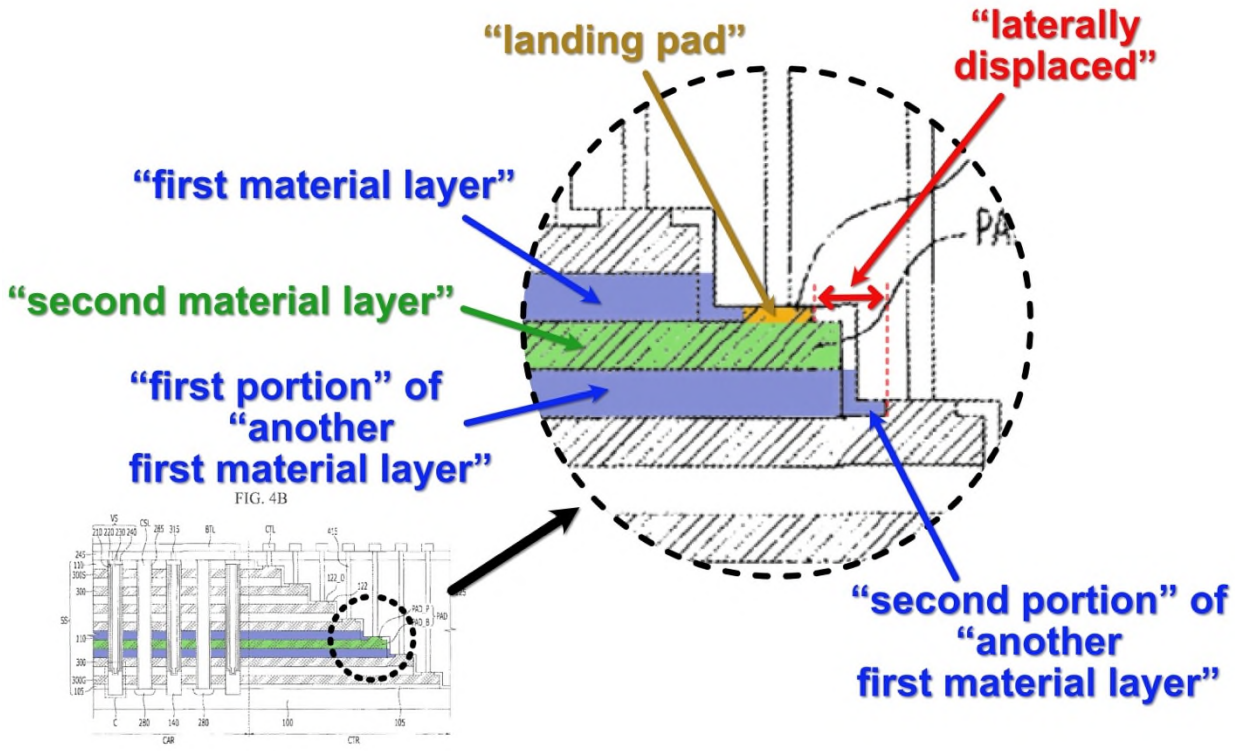
Kim teaches what these claims require. Kim's "stacking structure SS" includes a "plurality" of alternating "insulating layers 110 and … gate electrodes 300." Kim, 5:53-55; *see also id.*, 1:41-46. Because it includes alternating conductive and insulating layers, Kim's ***"second material layer"*** (the gate electrode 300) is located over ***"a first portion of another first material layer"*** (the insulating layer 110 immediately below the gate electrode):



Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 210-213.

Further, each insulating layer 110 can be integrated with an "auxiliary insulating layer 122" such that layers 110 and 122 form "one structure." Kim, 9:12-

13, 9:29-38. As shown below, because Kim's insulating layers include both layer 110 and 122, a ***"a side surface of a second portion of the another first material layer"*** (the portion of auxiliary insulating layer 122 adjacent to layer 110) is ***"laterally displaced from the second side surface of the landing pad"*** (the side of the pad portion PAD_P located on the upper gate electrode 300):



Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 214-215.

5. Claims 7 and 17

Claim 7 depends on claim 1. Claim 17 depends on claim 12. Both claims further require:

[7] / [17] "wherein the second material layer comprises a first conductive material and the landing pad comprises a second conductive material substantially the same as the first conductive material."

This is taught by Kim. As explained when discussing claim 4 above, "gate electrode 300," "base pad PAD_B and … protrusion PAD_P" may all be formed from the same "common material composition" such as a "metal." Kim, 6:31-35, 14:12-17; *see also* Ex. 1003, ¶¶ 216-219.

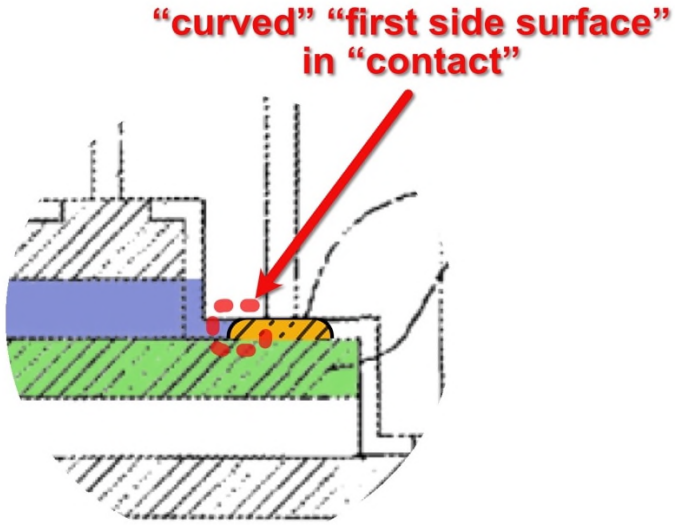
6. Claim 13

Claim 13 depends on claim 12 and further requires:

[13] "wherein the first side surface comprises a curved side surface."

Kim teaches that the ***"first side surface"*** of its ***"landing pad"*** that is in ***"contact"*** with its ***"first material layer"*** is (or at the very least obviously can be) ***"curved."*** Kim explains that while its figures show "[e]mbodiments … in which the protrusion pad PAD_P has a rectangular parallel[] shape[,]" "the protrusion pad PAD_P is not limited thereto and … may have a shape including a curved surface based on a virtual rectangular parallel[] shape, a cylindrical shape, or any shape." Kim, 8:29-34. A POSITA would have understood that this teaches a variety of different protrusion pad PAD_P shapes, many of which have the type of ***"curved"*** side surface claim 13 requires.

For example, a POSITA would have understood that when Kim references a "curved surface based on a virtual rectangular parallel[] shape," PAD_P would obviously be shaped in the manner shown in the demonstrative below:

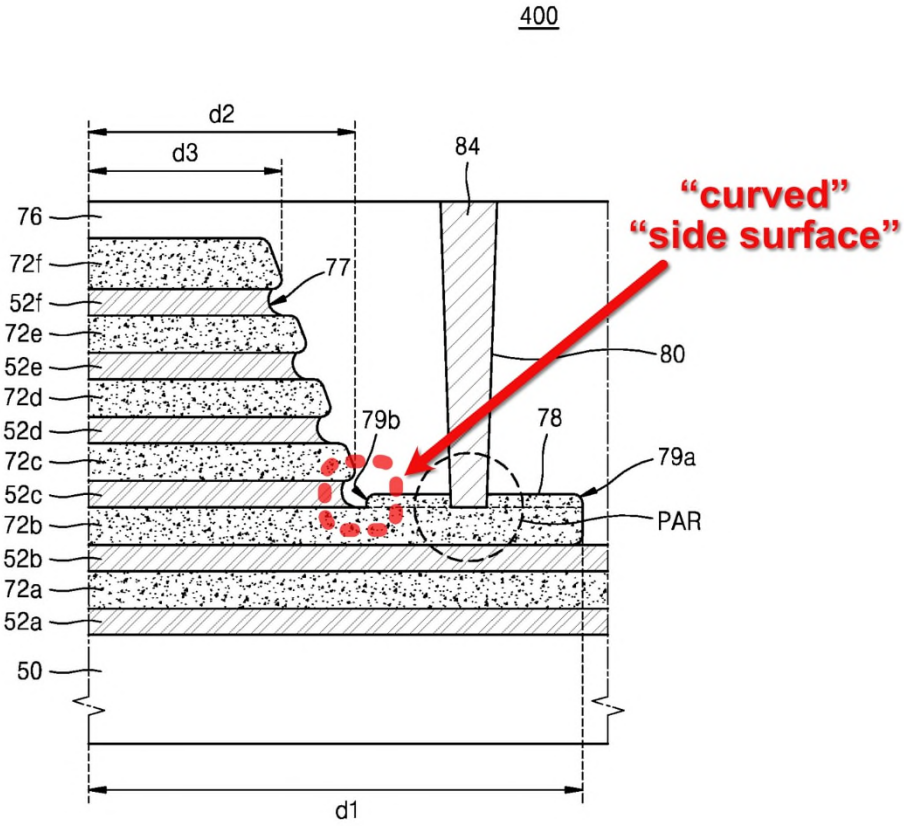


Ex. 1003, ¶¶ 222-225 (annotated, modified). As can be seen, just as Kim teaches, the pad continues to have a generally rectangular shape. And it continues to be located in the opening in auxiliary insulation layer 122. But now, the pad's sides are "curved" in the area where they contact auxiliary insulation layer 122. Kim, 8:29-34; *see also* Ex. 1003, ¶ 225.

Contact pads with this type of "curved" side surfaces were well-known in the art at the time the '838 patent was filed. For example, a reference to Park (Ex. 1009) teaches a "vertical semiconductor device" with an array of "stacked" "memory cells." Park, 1:14-16. Park's device—like Kim's—includes a staircase-shaped "connection region" with "pad region[s] PAR" located on the end of gate electrodes. *Id.*, 6:7-12, 6:36-47. Each "pad region PAR" includes a "raised pad portion" 7828. *Id.*, 7:4-16. Park goes on to explain that the "end 79b" of the "raised pad portion" 78 may be "rounded" to "prevent a short circuit" between the pad and an "adjacent

… conductive layer pattern 72c." *Id.*, 11:35-41. This is shown in Figure 7:

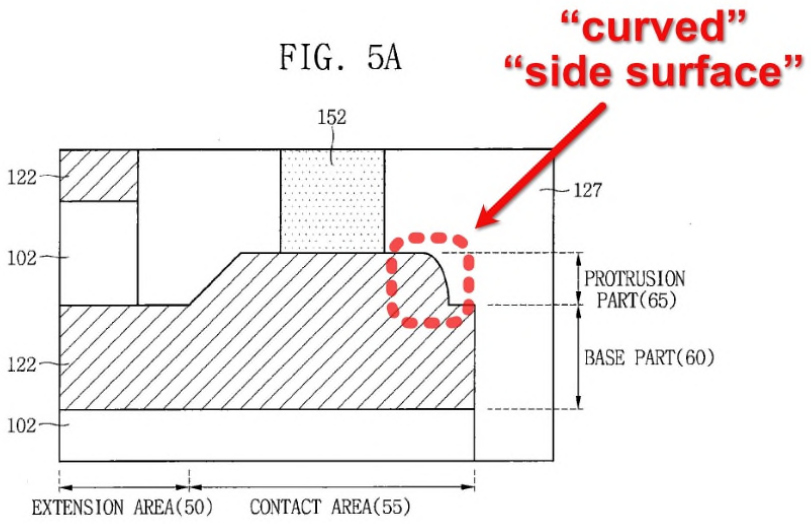
FIG. 7



Id., Fig. 7 (annotated).

Another reference to Yun (Ex. 1021) also relates to a "[s]emiconductor device[] having three-dimensionally arranged memory cells…" Yun, 1:33-35. The device has a "stepped" or "cascade structure." *Id.*, 9:22-25. The steps hold "contact area[s] 55" that are "co-planar with" the device's "gate electrodes" and have both a "base part 60 and a protrusion part 65." *Id.*, 8:11-20. Per Yun, the "protrusion part 65" may have either "inclined" or "rounded" "side surface[s]." *Id.*, 8:33-40. An

example of this is shown below (with the "rounded" surface shown on the right side of the contact pad):



Id., Fig. 5A (annotated).

A reference to Nam (Ex. 1022) provides yet another example. Nam—like Kim, Park, and Yun—teaches a "semiconductor device" formed from memory cell strings arranged in a three-dimensional array. *See* Nam, [0005], [0025], [0033]; Fig. 2. Gate electrodes connecting to the memory cells may "have a stepped shape having step structures." *Id.*, [0043]. Layers of insulation are located between the gate electrodes. *Id.*. Each gate electrode includes a "pad region" at its end where "the gate electrode … is connected to a contact 187." *Id.*, [0057]. And, among other shapes, as shown below this "pad region" can have a "bull nose" or "convex" shape. *Id.*, [0066].

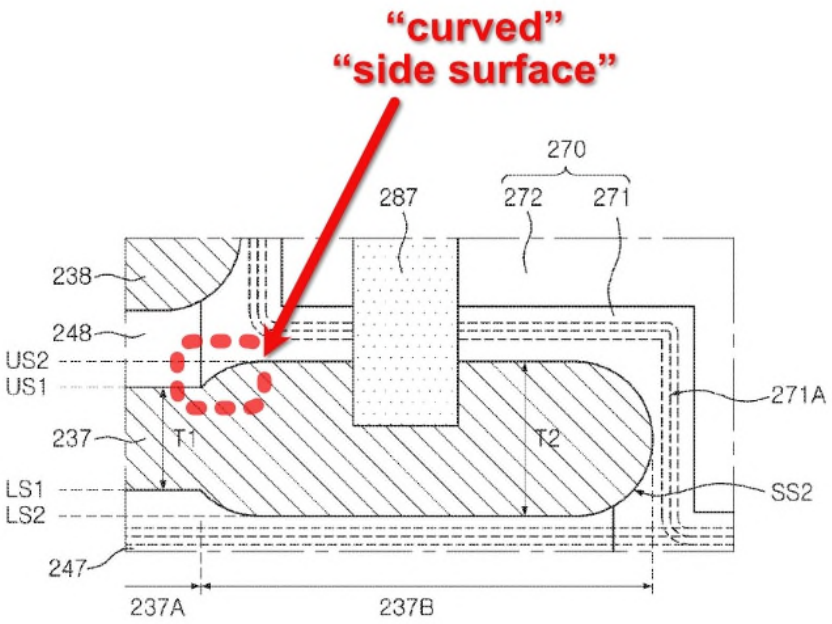


FIG. 8A

Id., Fig. 8A (annotated); *see also* Ex. 1003, ¶¶ 226-240.

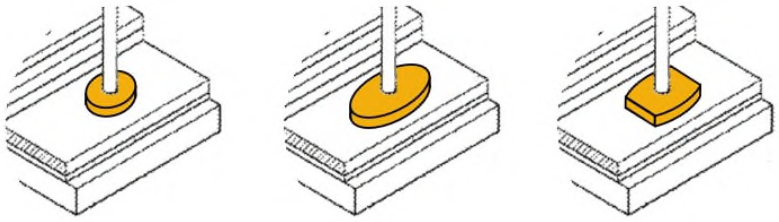
A POSITA would have been motivated to employ a contact pad with curved side surfaces when implementing Kim. To begin, Kim itself already contemplates that its pad can have a "curved surface." Kim, 8:29-34. This type of pad was also well known in the art. *See, e.g.*, Park, Fig. 7; Yun, Fig. 5A; Nam, Fig. 8A. Thus, contact pads with curved side surfaces would have been among the available design choices a POSITA would have considered for use. *See* Ex. 1003, ¶¶ 241-244. Additionally, a POSITA would have recognized that using a "curved" side surface with Kim's pads would have improved Kim by increasing the minimum distance between the pad and adjacent conductive layers, thereby reducing the risk of short circuit. *See* Park, 11:35-41. This would have further motivated use of such a pad

with Kim. *See* Ex. 1003, ¶¶ 245-247.

A POSITA would also have had every reason to believe that a curved pad could be successfully used with Kim. Again, this is one of the shapes that Kim already contemplates and deems acceptable. *See* Kim, 8:29-34. And it had also been successfully used in other semiconductor memory devices with staircase structures. *See, e.g.*, Park, Fig. 8; Yun, Fig. 5A. Moreover, Kim explains that the opening in auxiliary insulation layer 122 that will eventually contain its protrusion pad PAD_P obtains its shape via an "ion injection process." Kim, 13:1-11. More particularly, Kim explains that ion injection is used to form an appropriately shaped "doped region 122_I" in insulating layer 122. *See id.* This doped region is then etched away to form "opening 122_O" "simultaneously with the process of removing the sacrificial layer 120" which forms "gaps 260." *Id.*, 13:55-14:8. Then both the gaps 260 and openings 122_O are filled with conductive material to form the gate electrodes and pads. *See id.*, 14:9-17; *see also* Figs. 12-16. A POSITA would have recognized that this process could be readily adapted to form a curved opening that surrounds a curved contact pad. *See, e.g.*, Park, 7:17-29 (referencing the use of "ion implantation" and "oxidation" to form a "raised pad portion" with "rounded" sides); Nam, [0066], [0098]-[0107]; Figs. 30-39 (discussing and depicting the use of "an ion implantation process" to form a "convex" contact pad). Ion implantation would be employed to form a "doped region 122_I" with a rounded

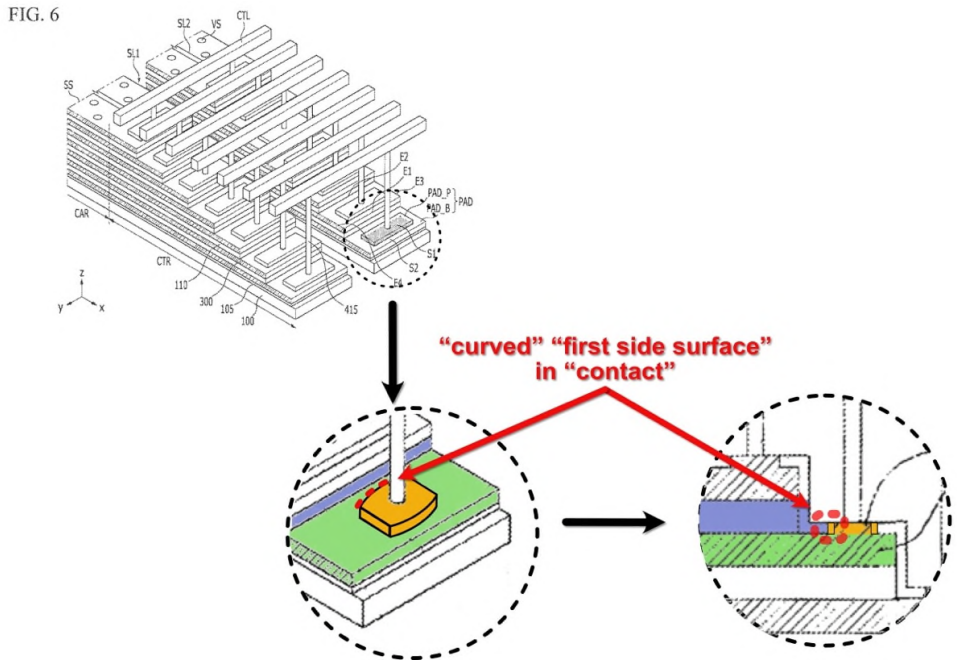
as opposed to rectangular shape resulting in a contact pad with rounded sides once the gate and pad formation process is completed. *See* Ex. 1003, ¶¶ 248-260.

Next, a POSITA would have understood that Kim's "cylindrical[ly]"-shaped protrusion pads PAD_P also include the type of ***"curved"*** surface that claim 13 requires. A POSITA would have understood that a "cylindrical" contact pad can be implemented as, for instance, a right cylinder, an elliptical cylinder, or even a generally rectangular pad with two sides that follow a cylindrical pattern. This latter shape is another way a POSITA would obviously have followed Kim's instruction to form a pad with a "curved surface based on a virtual rectangular parallel[] shape…." Kim, 8:29-34. Examples of how a POSITA would have understood these pads to be shaped are shown below:



Ex. 1003, ¶¶ 261-263. Employing any of these "cylindrical" contact pads also results the claimed ***"landing pad"*** having a ***"curved" "first side surface"*** that is in ***"contact"*** with Kim's ***"first material layer."*** This is shown in the demonstrative below generated using Figure 6 of Kim. The rectangular protrusion pad PAD_P in that figure has been replaced with a pad with curved sides that follow a cylindrical shape. While auxiliary insulation layer 122 is not shown in the three-dimensional

view of Figure 6, a side view has been added to the demonstrative below to show how the pad, even though now shaped with curved sides following the general shape of a cylinder, will continue to be located within the opening through and will contact the side of auxiliary insulation layer 122:



Id., ¶¶ 264-266.

A POSITA also would have been motivated to employ this shape and would have expected to succeed when doing so. Kim itself identifies "cylindrical"-shaped contact pads as acceptable and contemplates their use. A POSITA would consider this to be nothing more than a minor variation in design from the rectangular pads shown in Kim's figures. Ex. 1003, ¶¶ 267-269. And this type of pad could be made following the same process Kim employs to make its rectangular pad (just with differently shaped mask patterns to account for the curves of the cylinder). *See id.*,

¶ 270. Indeed, a POSITA would have understood that rounded contacts would not only have been achievable, but would have been easier to manufacture than a contact with perfectly straight sides. *See id.*, ¶¶ 223, 270.

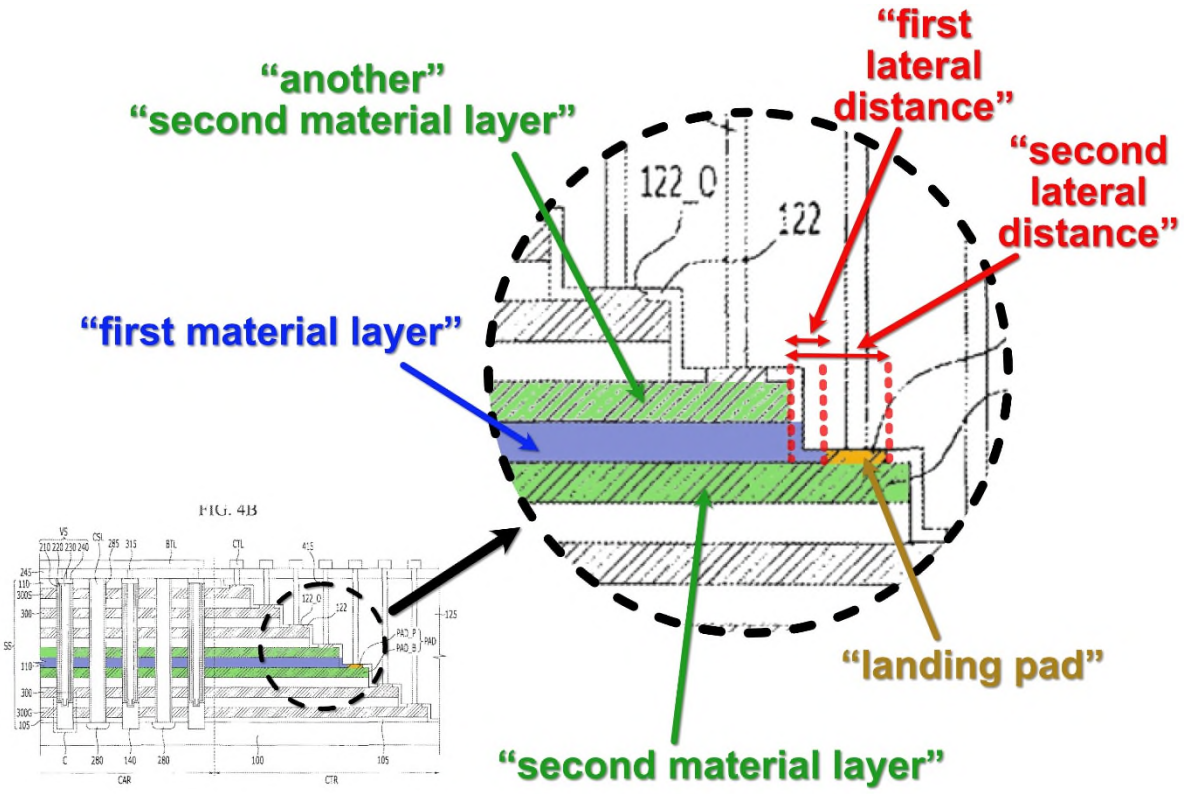
7. Claim 14

Claim 14 depends on claim 13 and further requires:

[14] "further comprising another second material layer disposed on the first material layer, wherein a first lateral distance between the first side surface and a side surface of the another second material layer is smaller than a second lateral distance between the second side surface and the side surface of the another second material layer."

Again, Kim's "stacking structure SS" includes a "plurality" of alternating "insulating layers 110 and … gate electrodes 300." Kim, 5:53-55; *see also id.*, 1:41-46. Because it includes alternating conductive and insulating layers, there is ***"another second material layer"*** (a further gate electrode 300) that is ***"disposed on the first material layer"*** (the insulation layer combination 110, 122 discussed in connection with claims 1 and 12 above). Further, Kim's device has a "stepwise structure." *Id.*, 1:40-47; *see also id.*, 1:15-17. This causes conductive layers higher in the stacking structure to be stepped back from lower layers. Because of this, the "***first lateral distance between the first side surface and a side surface of the another second material layer"*** (the distance between a pad's left side in Figure 4B and the side of the gate electrode in the layer above the pad) is ***"smaller"*** than ***"second lateral distance between the second side surface and the side surface of***

the another second material layer" (the distance between the same pad's right side and the side of the gate electrode in the layer above the pad):



Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 272-275.

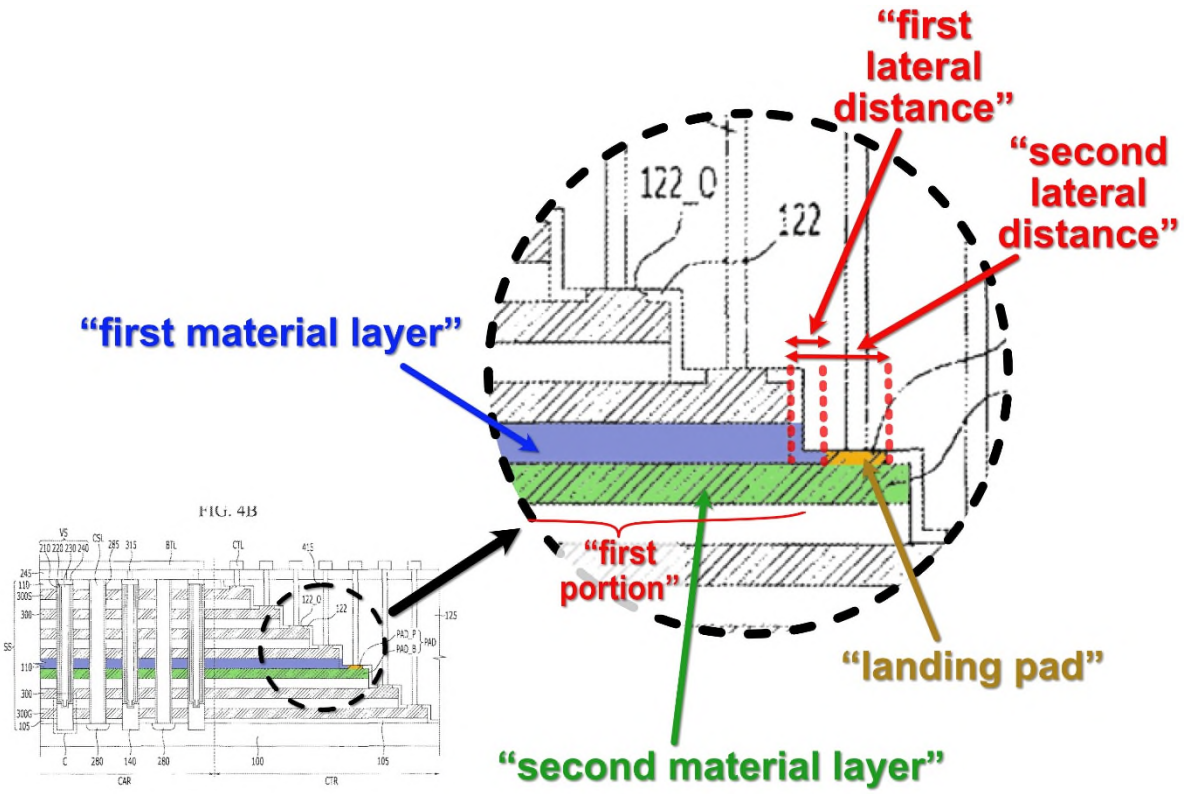
8. Claim 15

Claim 15 depends on claim 13 and further requires:

[15] "wherein the second side surface is laterally displaced from the first side surface, and wherein a first lateral distance between the first side surface and the first portion of the second material layer is smaller than a second lateral distance between the second side surface and the first portion of the second material layer."

A POSITA would have considered what this claim requires to be obvious in view of Kim. Kim explains that its protrusion pad has a "width." Kim, 11:57-12:7. Because it has a width, the ***"first"*** and ***"second" "side surface[s]"*** of the pad are

"laterally displaced" from each other as this claim requires. *See* Ex. 1003, ¶¶ 277-279. Moreover, the pad's width and location on the underlying gate electrode causes "***a first lateral distance between the first side surface and the first portion of the second material layer"*** (the distance between the leftmost edge of the protrusion pad and the gate electrode layer 300 to the left of the base pad) to be ***"smaller"*** than a ***"second lateral distance between the second side surface and the first portion of the second material layer"*** (the distance between the rightmost edge of the protrusion pad and the gate electrode layer 300 to the left of the base pad):



Kim, Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 280-281.

9. Claim 16

Claim 16 depends on claim 12 and further requires:

[16] "wherein the second material layer comprises tungsten, and titanium nitride."

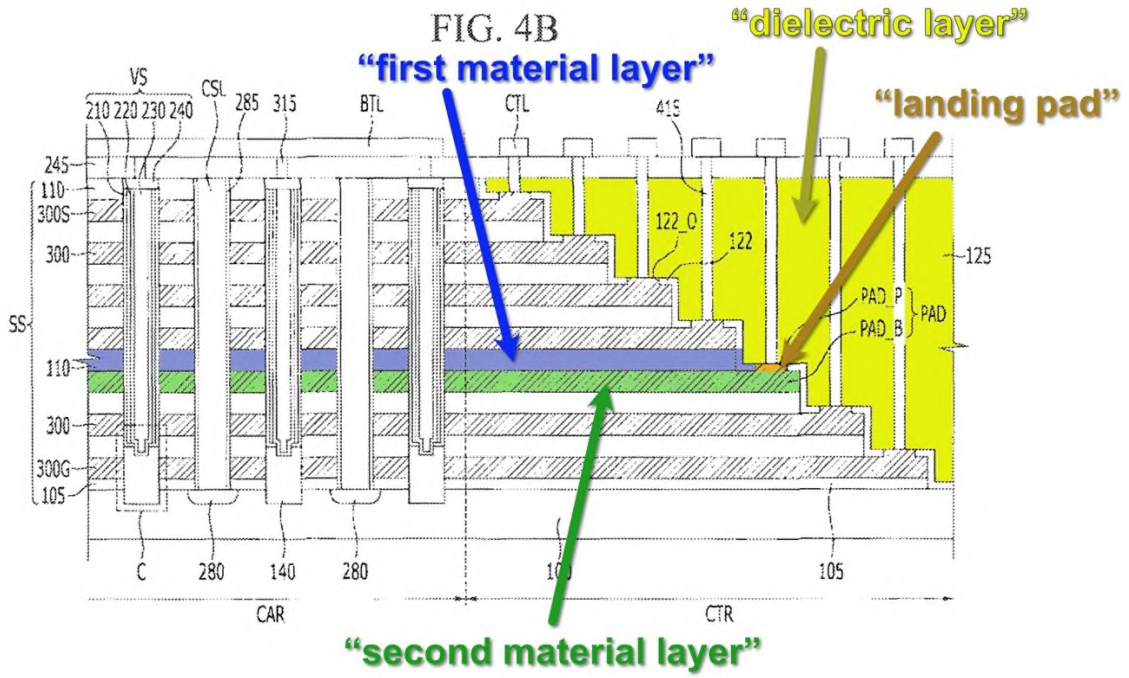
This is taught by Kim. Kim's gate electrodes 300 can be formed from "combination[s]" of materials including "metal" like "tungsten" and "metal nitride" such as "nitride titanium." Kim, 6:31-35; *see also* Ex. 1003, ¶¶ 283-284.

10. Claim 19

Claim 19 depends on claim 12 and further requires:

[19] "a dielectric layer disposed over the first material layer and the landing pad, wherein the first material layer comprises a first dielectric material and the dielectric layer comprises a second dielectric material, wherein the first dielectric material is substantially the same as the second dielectric material, and wherein the first dielectric material comprises silicon oxide."

Kim teaches a device that includes the claimed ***"dielectric layer disposed over the first material layer and the landing pad."*** Kim's device includes a "buried insulating layer 125." Kim, 9:56-57. This layer is formed over the "auxiliary insulating layer." *Id.*, 13:12-20. As shown below this layer 125—Kim's ***"dielectric layer"***—is located over both the ***"first material layer"*** (the insulating layers 110 and 122) and the ***"landing pad"*** (the protrusion pad PAD_P):



Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 286-289.

Next, Kim explains that its "insulating layer 125" is formed from an "insulating material." Kim, 13:15-17. This insulating material can be an "oxide layer." *Id.*, 9:61-67. Kim's "insulating layer 110" and "auxiliary insulating layer 122" are also formed from an "oxide layer." *Id.*, 9:29-31. Kim further explains that this oxide can be "silicon oxide." *Id.*, 12:26-29. Thus, just as this claim requires, Kim's ***"dielectric layer"*** (layer 125) and "***first dielectric material"*** (layers 110 and 122) are formed from ***"substantially the same"*** material: ***"silicon oxide."*** *See* Ex. 1003, ¶¶ 289-292.

B. *Ground 2*: Claims 3 and 18 Are Obvious Over Kim and Yang

Claim 3 depends on claim 1. Claim 18 depends on claim 12. Both claims further require:

[3] / [18] "wherein a lateral distance between the second side surface and the side surface of the second portion of the second material layer is between 10 nm and 300 nm."

A POSITA would have understood Kim, when considered in view of the example dimensions of Yang, to render this obvious. As explained in Ground 1, Kim teaches a three-dimensional memory device with ***"landing pads"*** (Kim's protrusion pad portions PAD_P) that are located within the bounds of and ***"laterally displaced"*** from the sides of a lower ***"second material layer"*** (Kim's gate electrode 300 and base pad portion PAD_B) by a ***"lateral distance."*** *See supra* Section IX.A.1.[1.B.2]. While Kim does not provide a numerical example quantifying the distance between the side of its landing pad and the side of the conductive layer below it, a POSITA would have considered it obvious to employ a value falling within the range required by these claims: "***10 nm and 300 nm***."

Yang (Ex. 1007) exemplifies this. Yang, like Kim, relates to "a pad structure applied to a three-dimensional (3D) memory device and a manufacturing method of the pad structure." Yang, 1:6-10. The device includes both an "array region" and a "pad region." *Id.*, 4:32-39. Figure 2 provides a "cross-sectional view" of the "pad region." *Id.*, 4:38-48. Yang's "pad region" is structurally analogous to Kim's

staircase-shaped stacking structure: it includes a stack of "material pairs 132" with a "stair step structure" located over a "substrate 100." *Id.*, 4:32-36, 4:43-48. The material pairs are alternating "conductive layers" 114 and "dielectric layer[s]" 106. *Id.*, 4:56-65. Each conductive layer includes a "pad 120" at its end that allows for electrical connection to a contact "plug[] 124." *Id.*, 4:43-51. As shown below, like Kim's protrusion pads, Yang's pads 120 are sized such that they are offset from the edges of and located within the bounds of the conductive layer on which they sit. The pads are located approximately in middle of each step of the staircase structure:

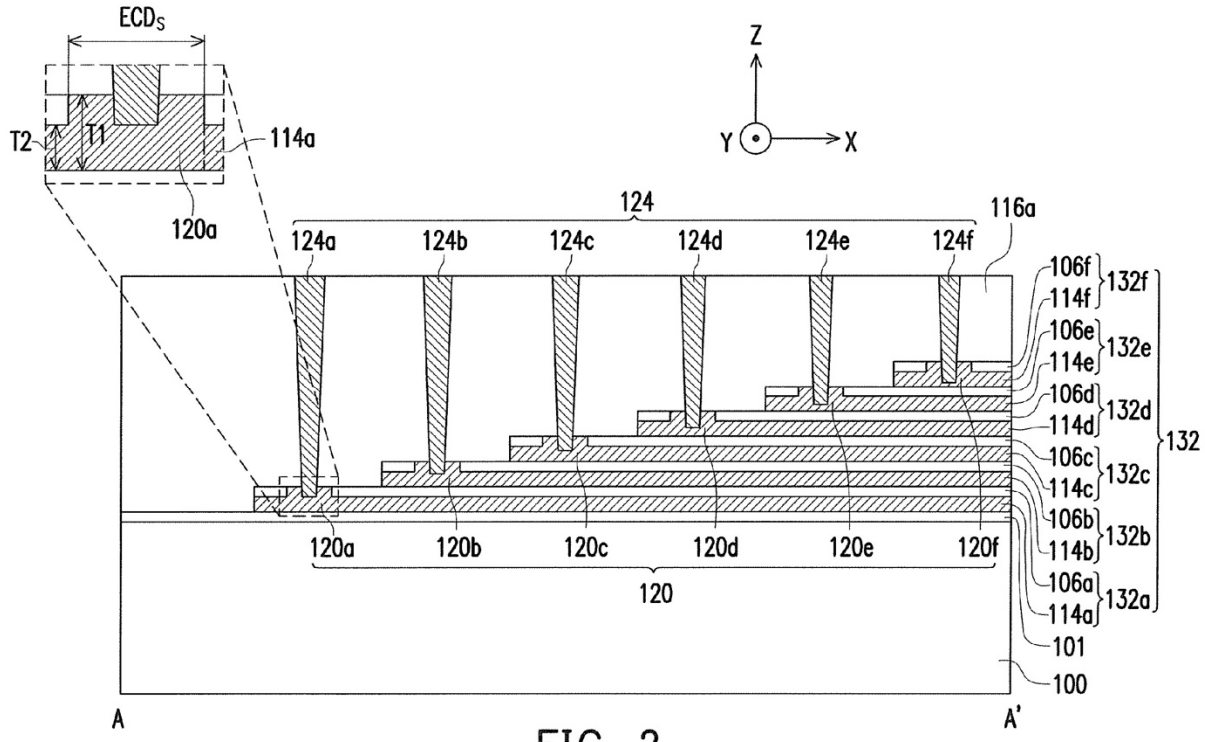


FIG. 2

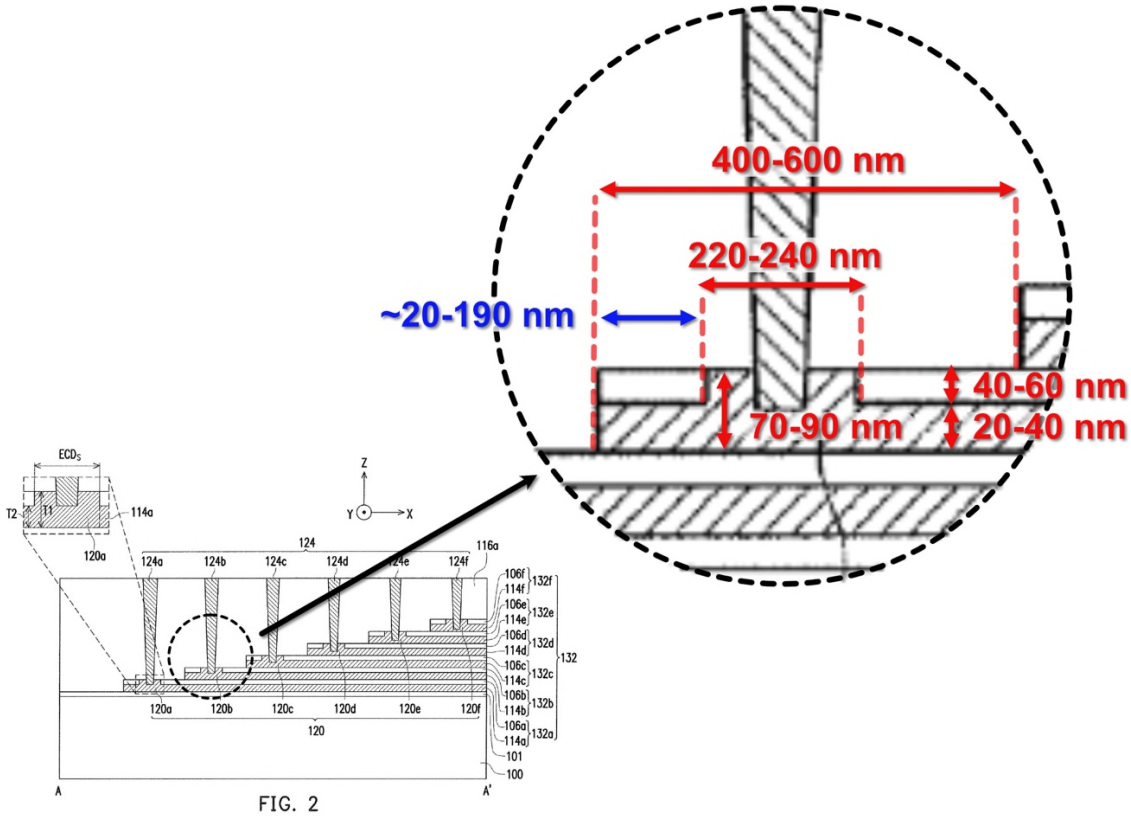
Id., Fig. 2; Ex. 1003, ¶¶ 296-306.

Yang goes on to teach that its pads 120 are dimensioned to avoid "electrical failures caused by over-etching during a process of manufacturing contact

openings." Yang, 1:44-47; *see also id.*, 3:41-47; 5:45-58. Yang provides example dimensions for the various components making up its device that are intended to provide this benefit. According to Yang, each of the conductive layers 114 has a thickness in the range of "20 nm to 40 nm." *Id.*, 6:7-28. The insulating layers 106 have thicknesses in the range of "40 nm to 60 nm." *Id.* The portion of the conductive layer where the contact pad sits has an increased thickness of "70 nm to 90 nm." *Id.*, 5:54-58. Each of steps in Yang's staircase structure can be "400 nm to 600 nm" long. *Id.*, 7:22-65 (referencing a distances D1 and D2 employed during step formation); Figs. 3E-3H. The contact pads themselves have a "width ECDs" that "is greater than the sum of the width ECDc of the contact openings 122" connecting to the pads and "two specification values S (i.e., ECDs>ECDc+2S)." *Id.*, 10:7-21. Thus, if the contact is formed using a "193 nm-ArF excimer laser stepper," "the specification value S may be in a range of 10 nm to 20 nm, for instance." *Id.*, 10:17-21. So, in this example, the pad width ECDs would be in the range of ~220-240 nm. *See* Ex. 1003, ¶¶ 307-312.

Given these dimensions, if the pads are located approximately in the middle of each staircase step, Yang's pad will be set back from the edge of the underlying conductive layer 114 by ~80-190 nm. *See* Ex. 1003, ¶ 312. A POSITA would have understood that Yang also contemplates placing the pads closer to the step edge. But, as shown in Figure 2, when doing so the space between the pad edge and the

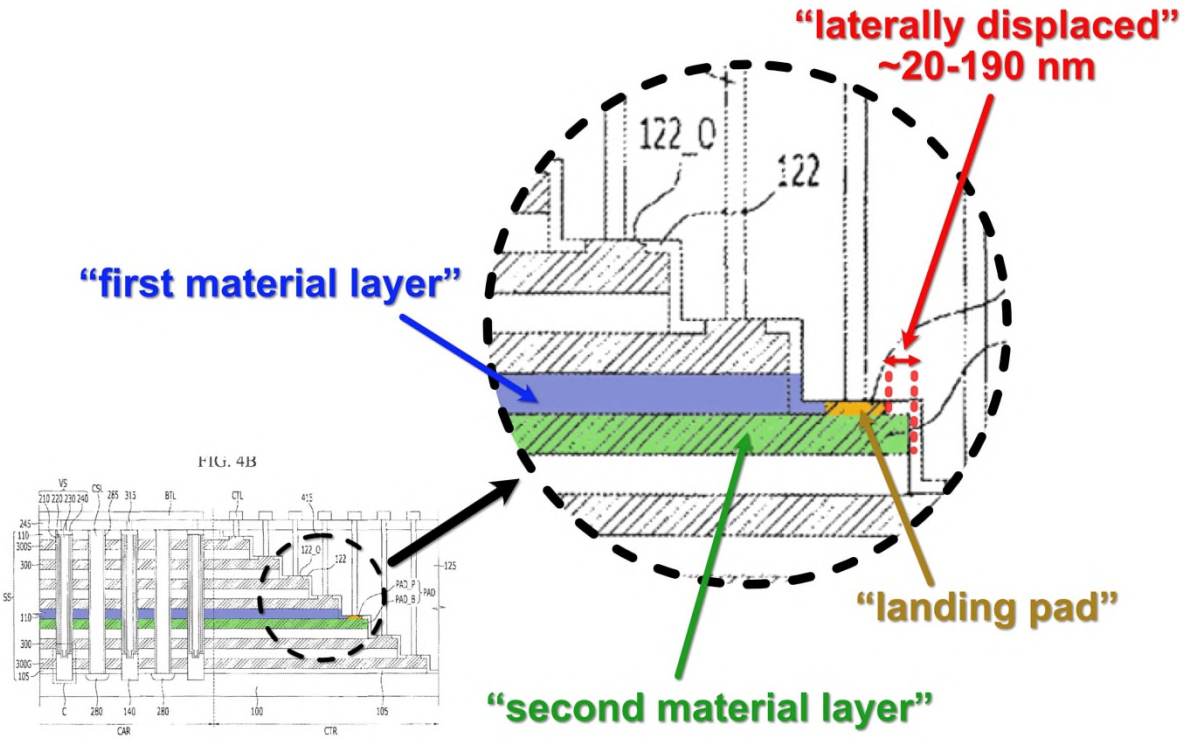
end of underlying conductive layer still correspond to at least the minimum thickness of the conductive and insulating layers. *See* Yang, Fig. 2. Thus, a POSITA would have understood that Yang's pads would be set back by at least 20nm, resulting in a total possible pad setback range of 20-190nm. *See* Ex. 1003, ¶¶ 313-316. The below annotated version of Figure 2 shows all these various dimensions:



Yang, Fig. 2 (annotated); *see also* Ex. 1003, ¶ 317.

Applying these example dimensions to Kim results in the claimed subject matter. Kim's protrusion pads would be set back—or ***"laterally displaced"*** by a ***"lateral distance"***—from the edge of the underlying conductive layer by an amount somewhere within the range of 20-190 nm. *See* Ex. 1003, ¶¶ 318-319. This is within

the range of "***10 nm and 300 nm***" required by claims 3 and 18:



Kim, Fig. 4B (annotated); *see also* Ex. 1003, ¶ 319.

A POSITA would have been motivated to dimension Kim's device this way and would have expected to succeed when doing so. Again, Kim does not include any numerical examples specifying the dimensions of its three-dimensional memory device. Thus, when implementing Kim, a POSITA would have to consult other references and their own background knowledge. *See* Ex. 1003, ¶¶ 320-322. Given its similarities with Kim, a POSITA would have considered Yang to be a particularly apt example. *See id.*, ¶ 323. Both Kim and Yang relate to three-dimensional memory devices with a staircase-shaped contact region. *See id.*, ¶ 324. Both references also teach that contact pads are located on each step. *See id.*, ¶ 325. And in both

references, the contact pads are offset from and located within the bounds of an underlying conductive layer. *See id.*, ¶ 326. This similarity in design would have provided a POSITA with a strong motivation to consult Yang when implementing Kim. *See id.*, ¶ 327. Moreover, both Kim and Yang explain that their devices are structured to avoid "electrical failures" resulting from "over-etching." *E.g.*, Yang, 3:39-44; Kim, 9:39-45. This similarity in purpose would also have motivated use of Yang's example dimensions with Kim. *See* Ex. 1003, ¶¶ 326-327. A POSITA would also have considered use of Yang's example dimensions to be nothing more than a routine, obvious design choice. *See id.*, ¶¶ 328-329. Kim already contemplates that the width of its contact pads can be adjusted. *See, e.g.*, Kim, 11:57-12:12. Yang simply provides a range of different pad dimensions and offsets that would have been obvious to employ as part of this adjustment process. *See* Ex. 1003, ¶¶ 330-333.

A POSITA would also have had a reasonable expectation of success. Again, the similarity and purpose and design between Kim and Yang would have confirmed to a POSITA that the example dimensions set forth in Yang are not only applicable to Kim, but can be successfully employed when implementing Kim's device. *See* Ex. 1003, ¶¶ 334-335.

C. *Ground 3*: Claims 1, 4-7, 12, 16-17, and 19-20 Are Obvious Over Lee

Lee, when considered in view of the knowledge of a POSITA, renders claims 1, 4-7, 12, 16-17, and 19-20 obvious.

1. Claims 1 and 12

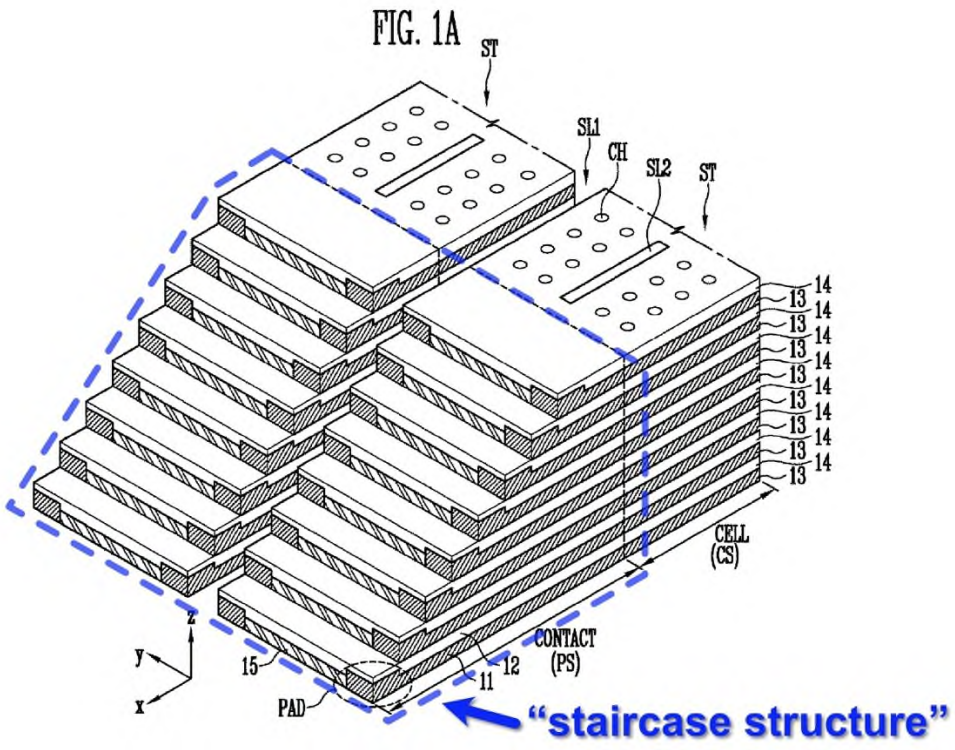
Claims 1 and 12 will again be assessed together.

[1.Pre] "A staircase structure of a memory device, comprising:"

[12.Pre] "A memory device comprising":

To the extent this preamble language is limiting, it is taught by Lee. Lee relates to "three-dimensional (3D) non-volatile memory devices." Lee, [0005], [0008]-[0009]. Figure 13 of Lee depicts "the configuration of a memory system according to an embodiment of the… invention." *Id.*, [0017]. As shown, "memory system 100" can include "non-volatile memory device 12 and a memory controller 110." *Id.*, [0085]-[0090]; Fig. 13; *see also* Ex. 1003, ¶¶ 339-342.

Lee also explains that its memory device includes both a "contact region CONTACT" and a "cell region CELL." Lee, [0020]. The contact region "may be patterned stepwise." *Id.*, [0021]; *see also id.*, [0009]. Lee's ***"staircase structure"*** (the stepped portion of the CONTACT region) is shown in Figure 1A below:



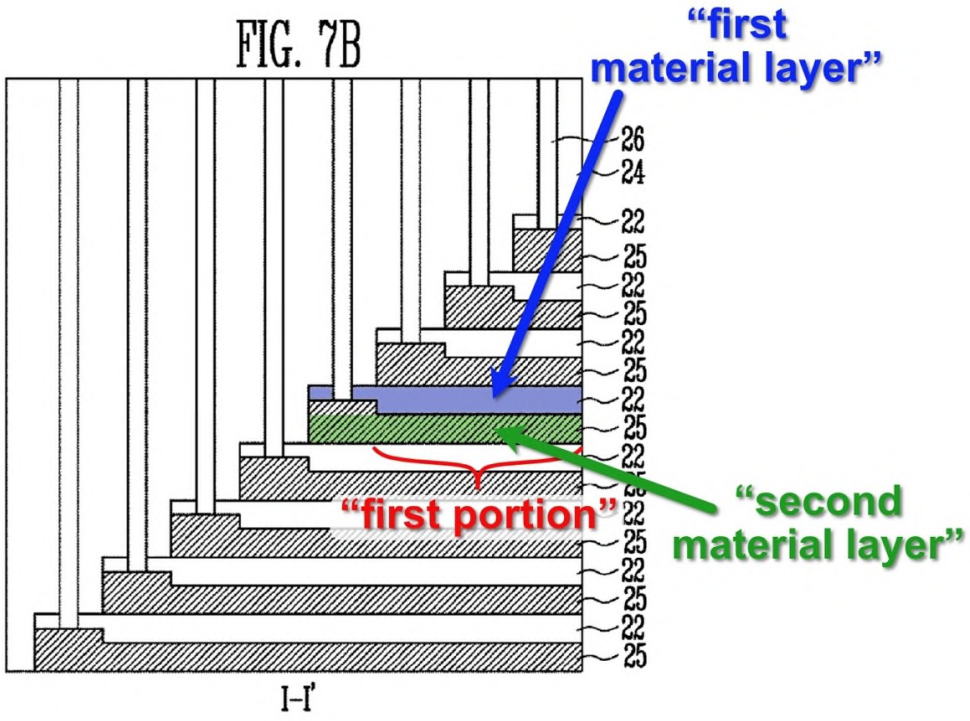
Id., Fig. 1A (annotated); *see also* Ex. 1003, ¶¶ 343-347.

[1.A] / [12.A] "a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and"

Claims 1 and 12 next require a ***"first material layer"*** that is ***"disposed over a first portion"*** of a ***"second material layer."***

Lee's device includes a "stacked structure ST" that is "patterned stepwise." Lee, [0021]. The "stacked structure ST" is formed from "conductive layers … and insulating layers … that are formed alternately with each other on the substrate." *Id.* "Each step" includes "at least one conductive layer … and at least one insulating layer…." *Id.* The "insulating layer" is "located on" the "top surface of each step." *Id.*; *see also id.*, [0010].

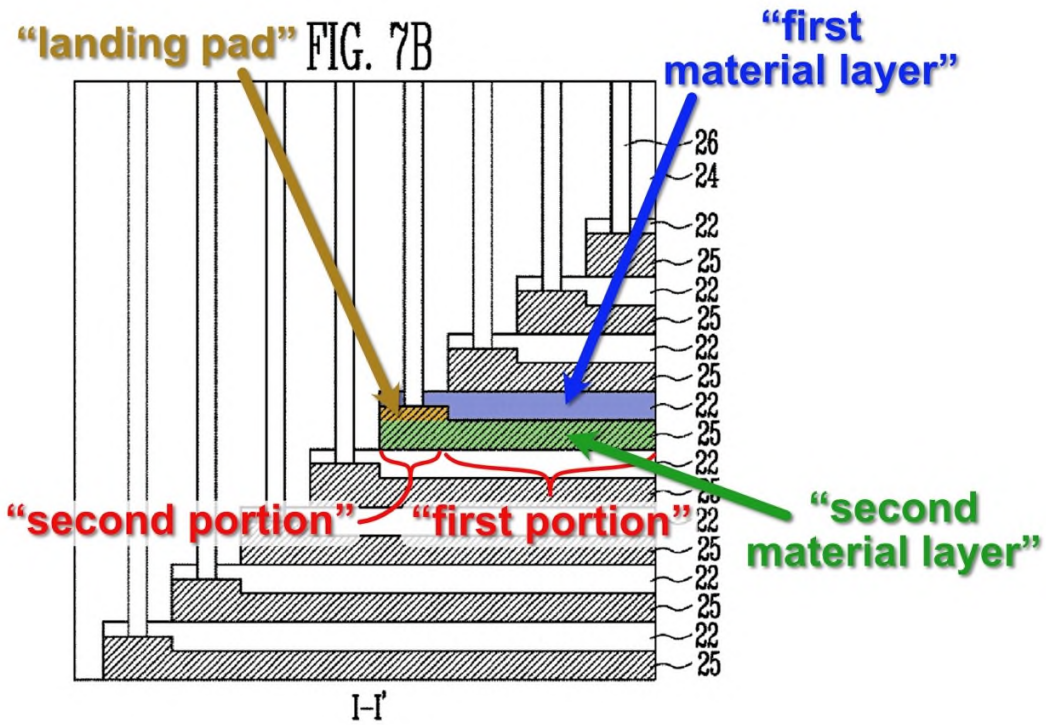
Figure 7B below provides an example. Layers 22 are "interlayer insulating layers." Lee, [0046]. Layers 25 are "conductive layers." *Id.*, [0041]. As shown, a ***"first material layer"*** (insulating layer 22) is ***"disposed over a first portion"*** of the ***"second material layer"*** (conductive layer 25). The conductive layer also includes two distinct portions: one portion includes the contact pad, the other does not:



Id., Fig. 7B (annotated); *see also id.*, Figs. 1A, 6B; Ex. 1003, ¶¶ 348-354. While layer 22 extends over the entirety of the conductive layer 25 below it, this is not precluded by claims 1 or 12. The claims require only that an insulating layer be "disposed over a first portion" of an underlying conductive layer. They do not prohibit the insulating layer from also covering other portions of the same conductive layer.

[1.B] / [12.B] "a landing pad disposed over a second portion of the second material layer,"

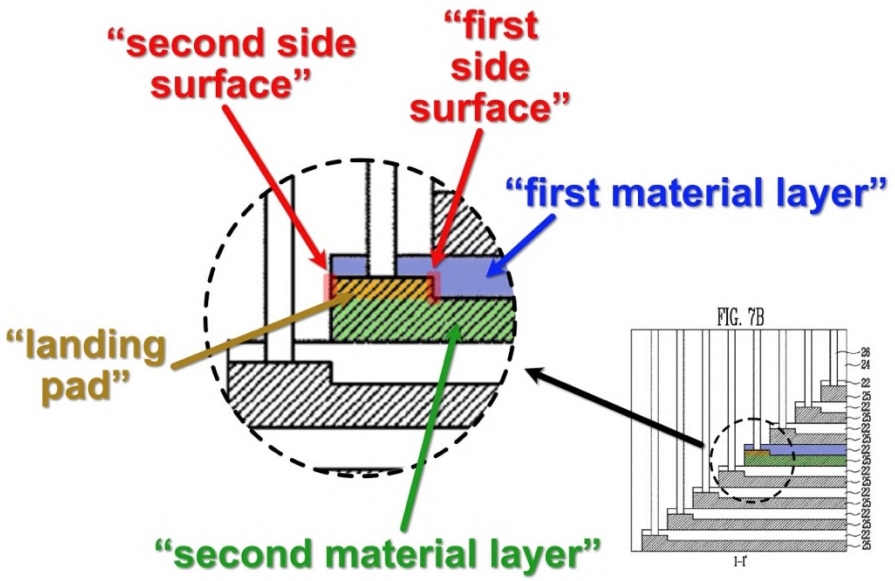
Lee also teaches the claimed ***"landing pad."*** According to Lee, each of the "conductive layers" may include a "pad portion PAD" at its end that has "a greater thickness" than other portions of "the … conductive layer." Lee, [0023]; *see also id.*, [0009]; [0027]. The "pad portions PAD" allow "contact plugs 26" to be "coupled" to each of Lee's conductive layers without creating defects. *Id.*, [0042]-[0043]. This pad portion PAD on the end of each of Lee's conductive layer is the claimed ***"landing pad."*** As shown, it is located over a ***"second portion"*** of Lee's ***"second material layer"*** (conductive layer 25):



Id., Fig. 7A (annotated); *see also id.*, Fig. 1A; Ex. 1003, ¶¶ 355-360.

[1.B.1] / [12.B.1] "wherein the landing pad comprises a first side surface and a second side surface,"

This is also taught by Lee. Lee's "pad portion PAD" has a "greater thickness" than the "conductive layer" on which it sits. Lee, [0023]. The PAD includes "side wall[s.]" *Id.*, [0050]. Because of this, the ***"landing pad"*** (the pad portion PAD) has both a ***"first side surface"*** (the side facing inwards towards insulation and conductive layers) and a ***"second side surface"*** (the side facing outwards):

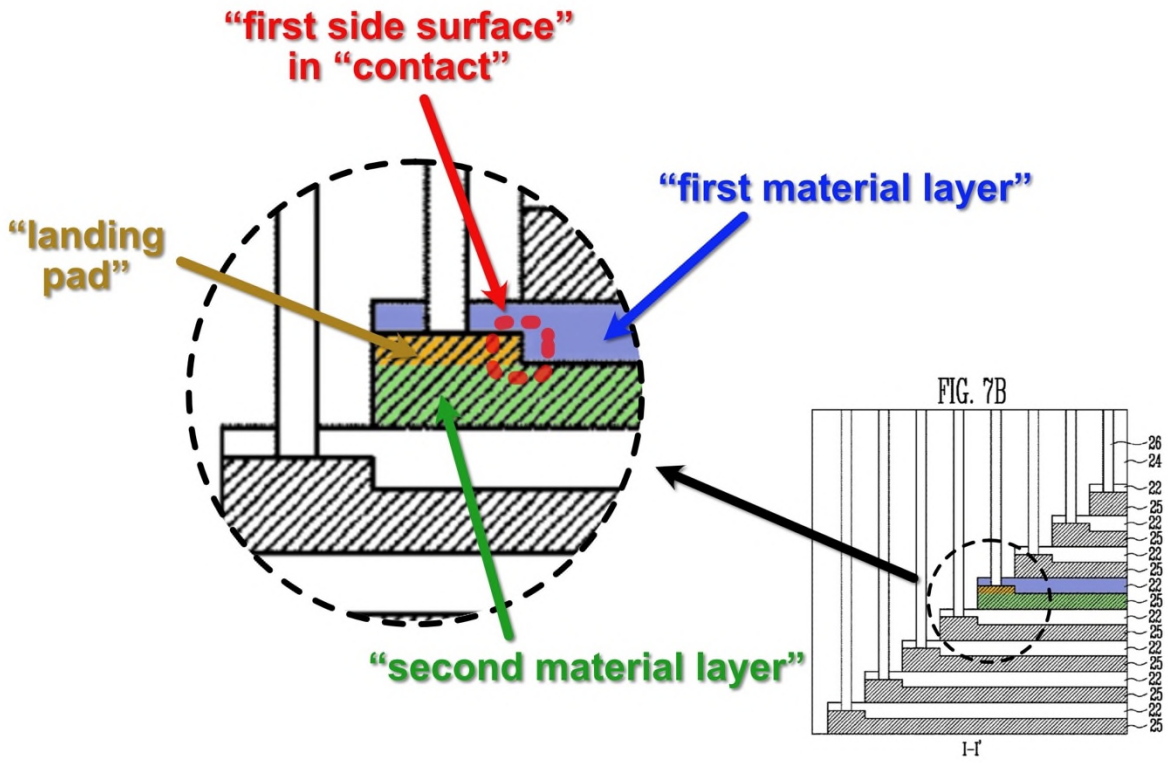


Id., Fig. 7B; *see also* Ex. 1003, ¶¶ 361-364.

[1.B.2] / [12.B.2] "wherein the first side surface is in contact with the first material layer and the second side surface is laterally displaced from a side surface of the second portion of the second material layer"

A POSITA would have considered this limitation obvious. To begin, the ***"first side surface"*** of Lee's ***"landing pad"*** (pad portion PAD) is in ***"contact"*** with the ***"first material layer"*** (insulating layer 22 in Figure 7B). This is shown in the

below:

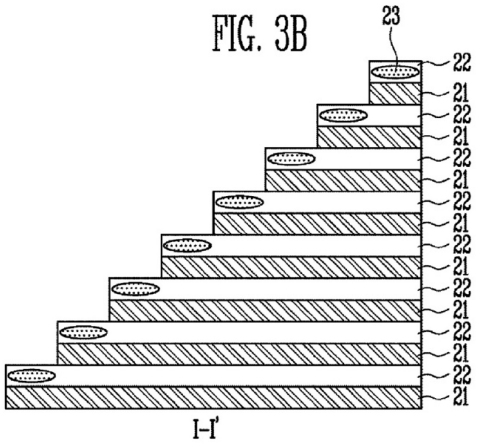


Lee, Fig. 7B (annotated); *see also* Ex. 1003, ¶¶ 365-366.

The process Lee employs to form its pad portion PAD confirms that there is contact between the PAD and the adjacent insulating layer. Lee begins by forming "a plurality of first material layers 21 and a plurality of second material layers 22 … alternately with each other." Lee, [0029]. The "layers 21," which will eventually be replaced by Lee's "conductive layers," are "formed of materials having a high etch selectivity with respect to second material layers 22." *Id.*, [0030]. The "second material layers 22" are "an insulating layer such as an oxide layer." *Id.* Lee then employs an "ion implantation process" to "implant[]" "impurity regions 23" into the

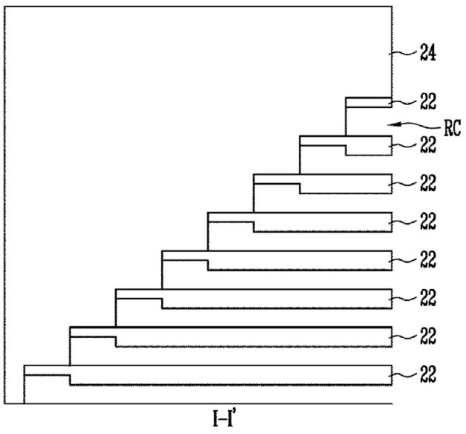
insulating layers 22. *Id.*, [0034]. These impurity regions will eventually form the thicker portions of Lee's pad portions PAD. *See id.*, [0038]-0041]. This is shown in Figure 3B below:

FIG. 3B



Id., Fig. 3B. Then, Lee etches layers 21 using an isotropic etch step. *Id.*, [0038]. Following this, Lee performs a second wet etch step to remove the impurity regions 23 to form "recessed regions RC" between the remaining portions of the insulating layers 22. *Id.*. This is shown in Figure 5B:

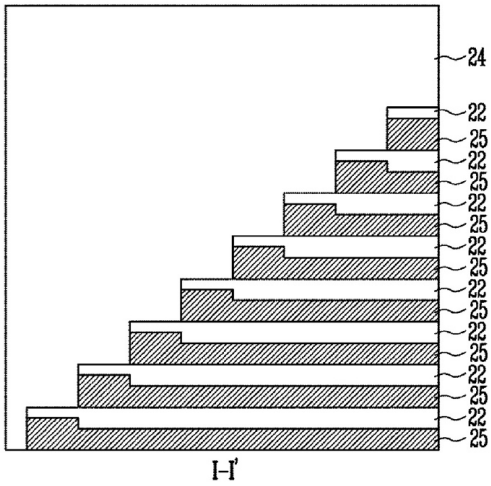
FIG. 5B



Id., Fig. 5B. The openings are then filled with "conductive layers 25" forming "pad

portions PAD exposed at the end of stacked structure ST." *Id.*, [0041].

FIG. 6B

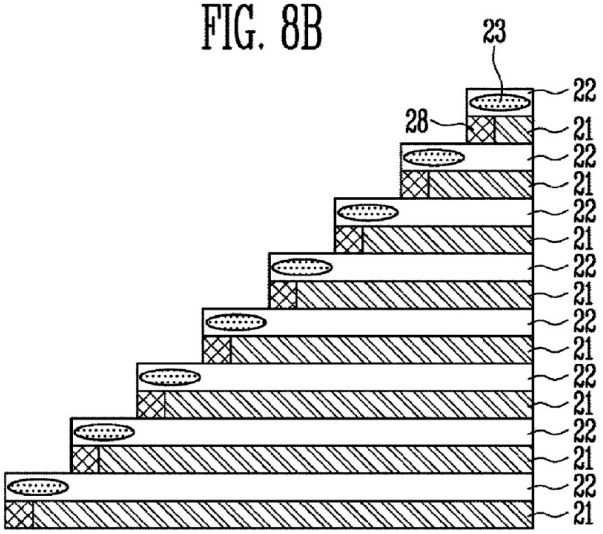


Id., Fig. 6B. Because Lee's pad portions PAD are formed within an opening in its insulating layers 22, a POSITA would have understood that the sides of the pad portions PAD contact the sides of the insulating layers. *See* Ex. 1003, ¶¶ 367-378.

Next, a POSITA also would have considered it obvious to structure Lee's memory device such that its ***"landing pad"*** (pad portion PAD) is ***"laterally displaced"*** from a ***"side surface"*** of the underlying conductive layer. According to Lee, "additional processes" can be applied during the manufacture of the device shown in Figure 7B to produce a modified structure. Lee, [0047]. For instance, "before an impurity implantation process is performed, side walls of the first material layer 21 exposed at respective steps may be oxidized to thereby form a plurality of barrier layers 28." *Id.*, [0048]. Lee explains that this "barrier layer" is included "in order to ensure an etch margin when the ends of the recessed regions

RC are extended." *Id.*, [0049]. In particular, while the "recessed region RC" continues to "extend … in a Z direction and thereby increase the thickness of the pad portions PAD," extension in the "X direction" is now limited by the barrier. *Id.* This helps ensure there is "sufficient distance may be ensured between the stacked conductive layers" to prevent "deterioration" of "a breakdown voltage." *Id.* The "barrier layer" 28 remains behind in the final product. *Id.*, [0050]. Figure 8B shows this barrier layer 28 after ion implantation but before etching:

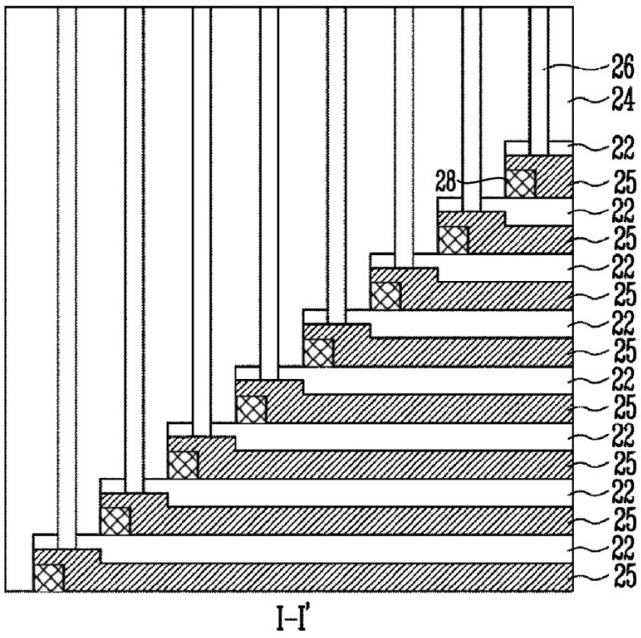
FIG. 8B



Id., Fig. 8B.

While Lee does not include a figure showing the device after the sacrificial layers and ion implanted regions 23 in figure 8B are etched away and replaced with conductive material, a POSITA would have understood the following to result:

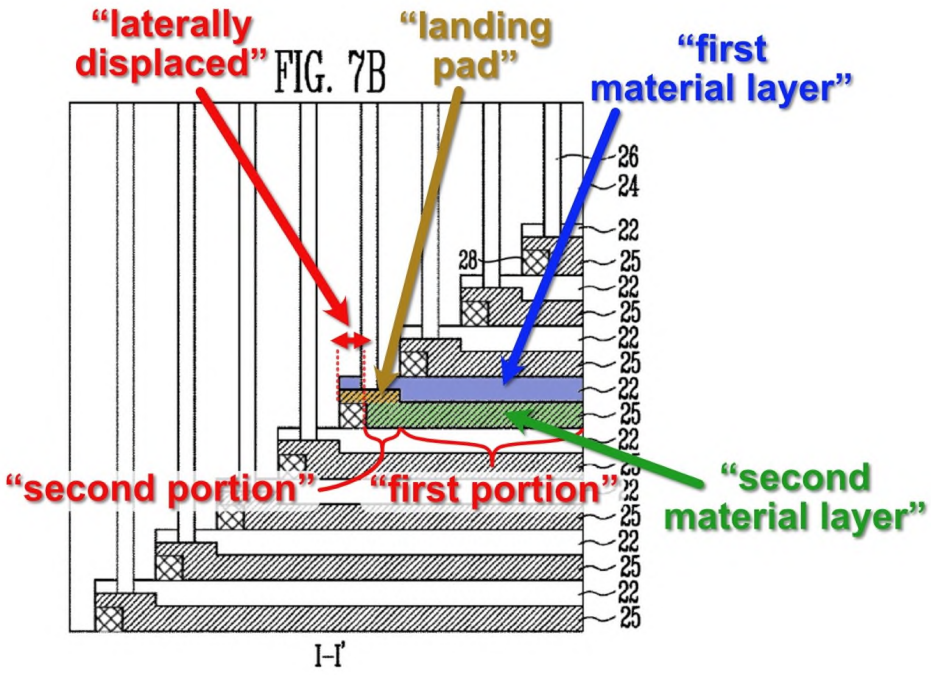
FIG. 7B



Lee, Fig. 7B (modified); Ex. 1003, ¶¶ 379-385. The above figure was created by modifying Figure 7B of Lee to include barrier layer 28 from Figure 8B. *See id.*, ¶ 386. The barrier layer 28 replaced a portion of the sacrificial layer 21 that served as a precursor to conductive layer 25 and limited etching in the X direction. *See id.*, ¶ 387. This in turn reduced the length of each of Lee's conductive layers 25. *See id.* Because the ion implanted region 23 in insulating layer 22 had the same physical extent in Figure 8B as Figure 7B (albeit with the implanted region in Figure 8B partially located over the underlying barrier layer 28), Lee's pad portion PAD will continue to have the same size as shown in Figure 7B. *See id.*, ¶ 388. The only change was to layer 25 which now has reduced length due to the presence of barrier layer 28. *See id.*, ¶ 389. This causes the PAD in the finished device to extend over

the barrier layer 28 that—per Lee—remains behind. *See id.*, ¶ 390.

This modified structure including barrier layer 28 is what this claim requires. Not only is the ***"first side surface"*** (the right side of the pad in Fig. 7B) of Lee's ***"landing pad"*** (pad portion PAD) still in ***"contact"*** with the ***"first material layer"*** (insulating layer 22), but the pad's "***second side surface"*** (the left side of the pad) is now ***"laterally displaced"*** from the ***"side surface of the second portion of the second material layer"*** (the end of conductive layer 25 that is adjacent to now included barrier layer 28):



Lee, Fig. 7B (modified); Ex. 1003, ¶¶ 391-393.

2. Claim 4

Claim 4 depends on claim 1 and further requires:

[4] "wherein the landing pad comprises a conductive material."

This is taught by Lee. In particular, Lee's layers 25 and pad portions PAD at the ends of those layers are, according to Lee, formed from "conductive" material. Lee, [0040]-[0041]; *see also* Ex. 1003, ¶¶ 395-396.

3. Claim 5

Claim 5 depends on claim 4 and further requires:

[5] "wherein the conductive material comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof."

While Lee does not indicate what specific conductive material its layers 25 and PAD portions are made from, it does identify "tungsten (W)" as an example conductive material usable in its device. Lee, [0074]. A POSITA would have considered use of this material obvious, along with other well-known conductive materials used in the art c. *See* Ex. 1003, ¶¶ 398-403. These other materials included, for instance, metals such as tungsten, aluminum, copper, cobalt, nickel, hafnium, platinum, and titanium, doped silicon, metal silicides, metal nitrides, and combinations of these various materials. Park, 10:51-45; Nam, [0094]; Kim, 6:31-36. A POSITA would have recognized that any of these materials would have been acceptable for use and would have been obvious to employ when forming Lee's conductive layers. *See* Ex. 1003, ¶¶ 403-405. Indeed, tungsten was the most commonly used standard gate layer material because it can be readily deposited as part of a gate replacement process and has a high conductivity and low resistivity

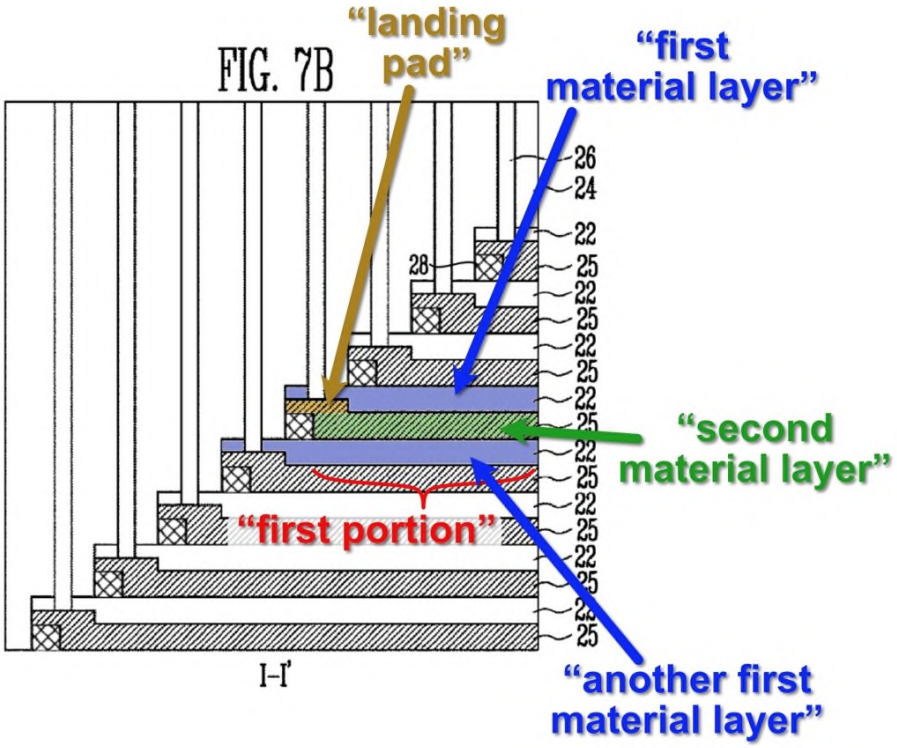
(resulting in fast access operations). *See, e.g.*, Ex. 1011, 318, 320; Ex. 1003, ¶ 405.

4. Claims 6 and 20

Claim 6 depends on claim 1. Claim 20 depends on claim 12. Both claims further require:

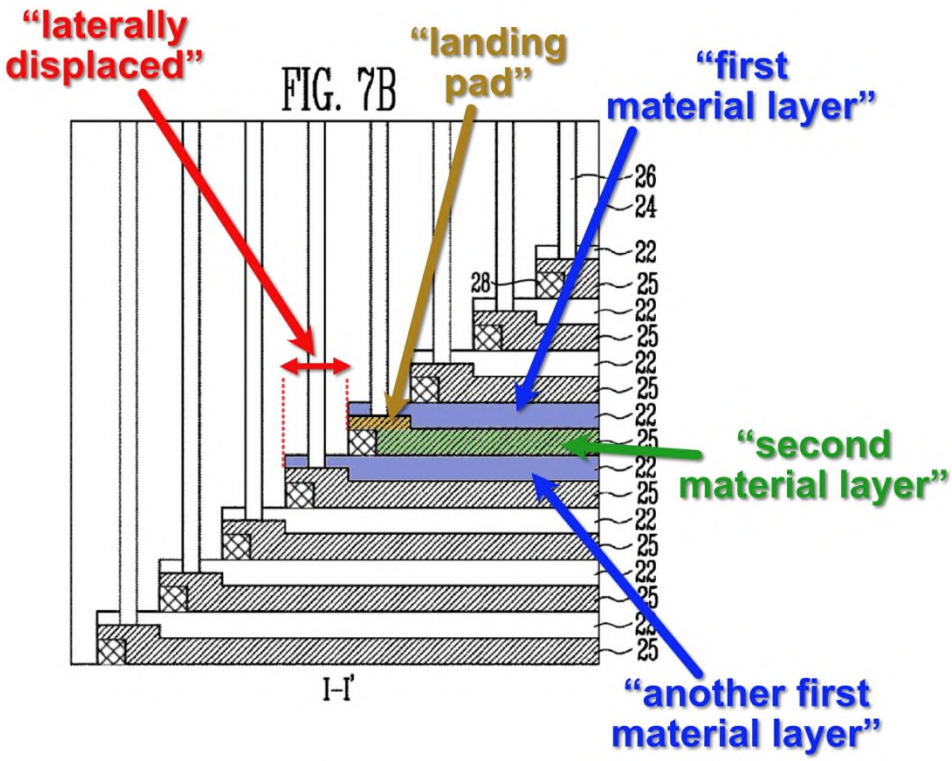
[6] / [20] "wherein the second material layer is disposed over a first portion of another first material layer, and wherein a side surface of a second portion of the another first material layer is laterally displaced from the second side surface of the landing pad."

Lee teaches what these claims require. Again, Lee's device includes a "stacked structure ST" formed from alternating "conductive layers" and "insulating layers." Lee, [0021]; *see also id.*, [0010], [0041], [0046]; Figs. 1A, 7A. Because of this, each of Lee's ***"second material layer"*** (conductive layer 25) is located over ***"a first portion of another first material layer"*** (the portion of insulating layer 22 immediately below this conductive layer):



Id., Fig. 7B (modified and annotated); Ex. 1003, ¶¶ 407-409.

Next, in Lee, "[e]ach step of the stacked structure ST that is patterned stepwise" includes "one conductive layer" and "one insulating layer." Lee, [0021]. In Figure 7B, "the insulating layer" is "located on a top surface of each step." *Id.* As shown below, this results in ***"a side surface of a second portion of the another first material layer"*** (the portion of a lower insulating layer 22 that extends out beyond an upper adjacent conductive layer 25 to form a step) being ***"laterally displaced"*** from ***"the second side surface of the landing pad"*** (the leftmost side of Lee's pad portion PAD):



Id., Fig. 7B (annotated and modified); Ex. 1003, ¶¶ 410-412.

5. Claims 7 and 17

Claim 7 depends on claim 1. Claim 17 depends on claim 12. Both claims further require:

[7] / [17] "wherein the second material layer comprises a first conductive material and the landing pad comprises a second conductive material substantially the same as the first conductive material."

This is taught by Lee: both conductive layer 25 and the pad portion PAD at this layer's end is made from the same "conductive" material. Lee, [0040]-[0041]; *see also* Ex. 1003, ¶¶ 413-415.

6. Claim 16

Claim 16 depends on claim 12 and further requires:

[16] "wherein the second material layer comprises tungsten, and titanium nitride."

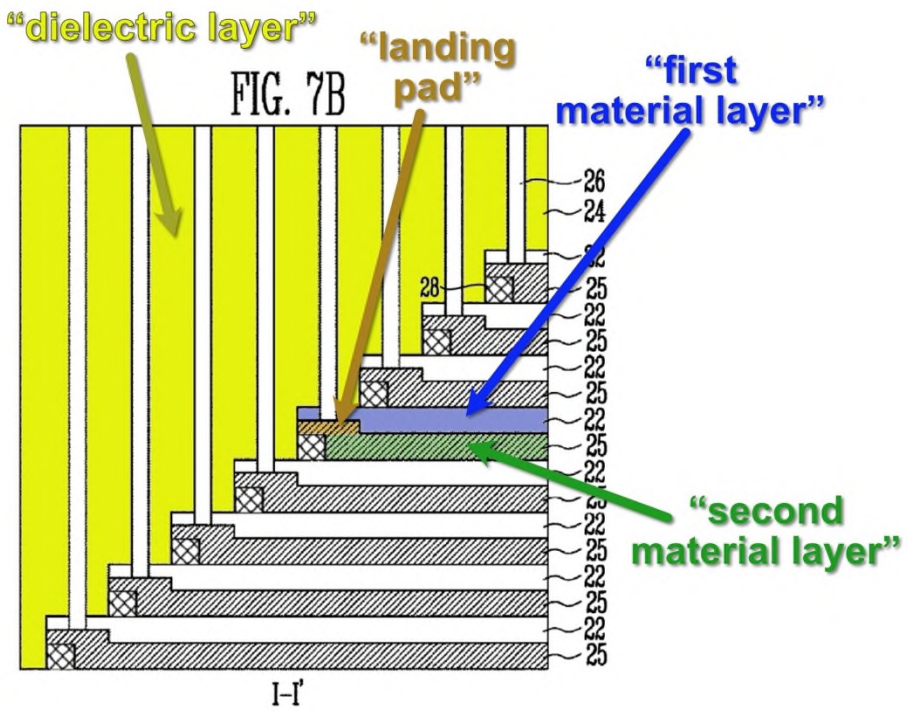
A POSITA would have considered this obvious for the same reasons explained in connection with claim 5: a POSITA would have known of and considered it obvious to use any of the various, well-known conductive materials routinely employed in memory devices when implementing Lee. *See supra* discussion of claim 5. And these well-known materials included "combinations" of materials such as a "metal" like "tungsten" and a "metal nitride" like "nitride titanium." Kim, 6:31-36; Nam, [0094]; *see also* Ex. 1003, ¶¶ 416-419.

7. Claim 19

Claim 19 depends on claim 12 and further requires:

[19] "a dielectric layer disposed over the first material layer and the landing pad, wherein the first material layer comprises a first dielectric material and the dielectric layer comprises a second dielectric material, wherein the first dielectric material is substantially the same as the second dielectric material, and wherein the first dielectric material comprises silicon oxide."

Lee teaches a device that includes the claimed ***"dielectric layer disposed over the first material layer and the landing pad"*** an "interlayer insulating layer 24" is "formed on" its other "material layers…" Lee, [0036]. As shown below this layer 24—Lee's "***dielectric layer"***—is located over both the ***"first material layer"*** (insulating layer) and the ***"landing pad"*** (the pad portion PAD):



Id., Fig. 4B (annotated); *see also* Ex. 1003, ¶¶ 421-423.

Next, Lee explains that both layer 24 and the layers 22 located within its stacked structures are "insulating layer[s]." Lee, [0029], [0036]. Lee also explains that its device's "insulating layer[s]" can be an "oxide layer." *Id.*, [0030]. Thus, a POSITA would have recognized that Lee's ***"dielectric layer"*** (layer 24) and "***first dielectric material"*** (layers 22) are (or at least obviously could be) formed from ***"substantially the same"*** material: an insulating oxide. *See* Ex. 1003, ¶¶ 424-426. While Lee does not specifically mention ***"silicon oxide,"*** a POSITA would have recognized that this was the most widely and commonly used insulating material in memory devices. *See, e.g.*, Kim, 6:35-46 (referencing the use of "silicon oxide" "insulating layers"); Nam, [0048] (similarly referencing the use of "silicon oxide"

layers); Park, 8:1-2 (same). Thus, a POSITA would have understood that Lee's reference to "oxide layer[s]" includes layers of silicon oxide. *See* Ex. 1003, ¶¶ 427-429.

D. *Ground 4*: Claims 3 and 18 Are Obvious Over Lee and Haller

Claim 3 depends on claim 1. Claim 18 depends on claim 12. Both claims further require:

[3] / [18] "wherein a lateral distance between the second side surface and the side surface of the second portion of the second material layer is between 10 nm and 300 nm."

A POSITA would have understood Lee, when considered in view of the example dimensions of Haller, to render this obvious. As discussed in connection with claim 1, Lee employs a "barrier layer" 28 that operates to limit etching in the X direction during manufacture of its memory device. The barrier layer 28 remains behind in Lee's final device and increases the distance between Lee's pad portion PAD and adjacent conductive layers. *See* Lee, [0049]. Further, as claims 1 and 12 require, this layer also causes Lee's ***"landing pad"*** (the pad portion PAD) to be ***"laterally displaced"*** from its ***"second material layer"*** (conductive layer 25) by a distance equal to the thickness of layer 28. *See supra* Section IX.C.1.[1.B.2]. Lee does not provide an example of layer 28's thickness. A POSITA, however, would have considered it obvious that this layer would have a thickness falling within the range required by this claim.

Haller (Ex. 1008) provides an example. Haller relates to a "3D memory device" with a "staircase structure." Haller, 4:8-11. Haller explains that in prior art memory devices, problems may arise when performing an "etch process" to form contacts to the device's wordline layers. *Id.*, 1:30-35. In particular, the etch may either "punch[] through" the wordline or "leak[]" over the wordline edge "creating an undesired short circuit." *Id.* To avoid this, Haller includes an "etch stop" at the end of each conductive wordline layer in its staircase structure. *Id.*, 2:6-9. This etch stop "prevent[s] … physical or electrical contact of the wordline contact structure with an adjacent wordline of the staircase structure." *Id.*, 2:19-23. This etch stop includes a component labeled as "spacer 502" in Figure 9:

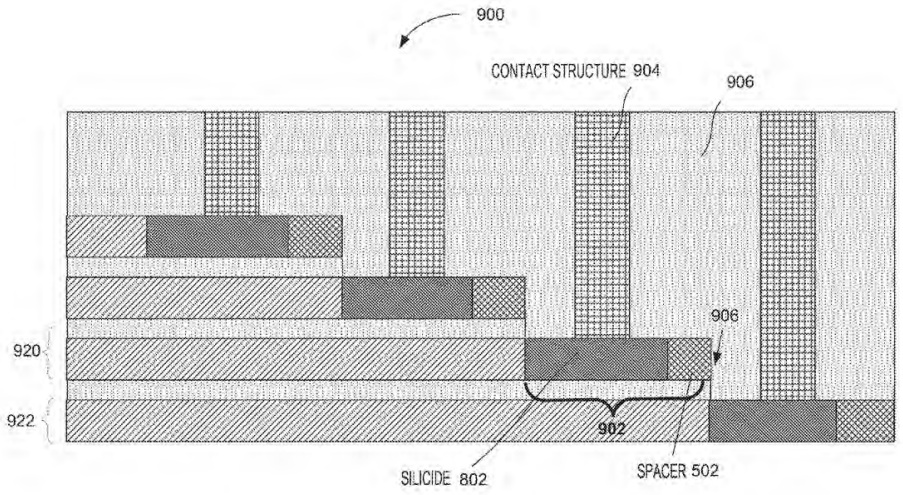
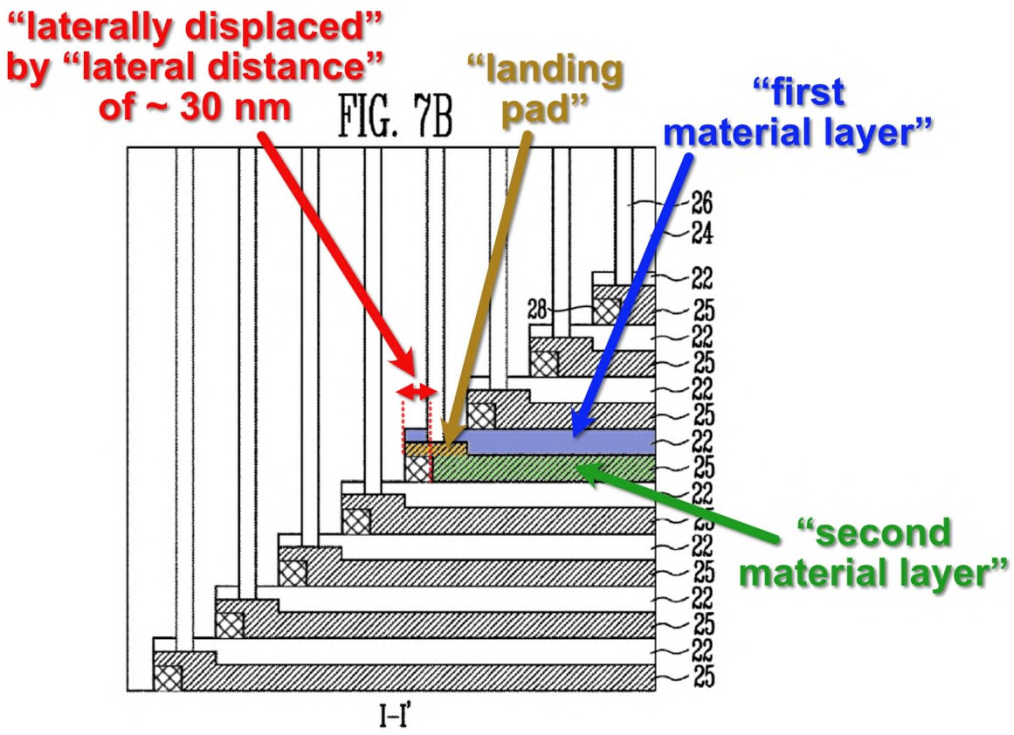


FIG. 9

Id., Fig. 9; 6:28-63. Haller explains that the spacer 502 is formed by depositing "insulative dielectric material" into a "recess" that is "30 nm in length." *Id.*, 4:37-5:7; Figs. 3-5; *see also* Ex. 1003, ¶¶ 433-446.

Applying Haller's example spacer and etch stop dimension—30 nm—to Lee renders this claim obvious. Lee's layer 28 would have a thickness of 30 nm causing its ***"landing pad"*** (pad portion PAD) to overhang—or be ***"laterally displaced"*** by a ***"lateral distance"***—from the edge of the underlying "second material layer" (conductive layer 25) by approximately 30 nm. *See* Ex. 1003, ¶ 447. This is within the range of "***10 nm and 300 nm***" required by claims 3 and 18:



Lee, Fig. 7B (modified and annotated); *see also* Ex. 1003, ¶ 447.

A POSITA would have been motivated to use Haller's example dimension with Lee and would have had a reasonable expectation of success when doing so. Again, Lee does not include example dimensions for its memory device. Thus, a POSITA would out of necessity have needed to consult both their background

knowledge and other references when implementing Lee. *See* Ex. 1003, ¶¶ 448-452. A POSITA would have considered Haller to be particularly relevant. It relates to the same type of three-dimensional memory device with a staircase structure as Lee. *See id.*, ¶ 451. And, like Lee it employs an etch stop on each of its conductive layers to avoid short circuits. *See id*. This similarity in purpose and design would have provided a strong motivation to employ Haller's example dimension with Lee. *Id.*, ¶ 452. Moreover, a POSITA would have recognized that layers in three-dimensional memory devices routinely had thicknesses in the range of approximately 20-90 nm. Yang, 6:7-28. This would have confirmed to a POSITA that Haller's example etch stop spacer thickness would not only have been obvious to employ with Lee, but that dimensioning Lee's layer 28 this way would have been successful. *See* Ex. 1003, ¶¶ 453-456.

E. *Ground 5*: Claims 13, 14, and 15 Are Obvious Over Lee and Park

Lee, when considered in view of Park and the knowledge of a POSITA, renders claims 13, 14, and 15 obvious.

1. Claim 13

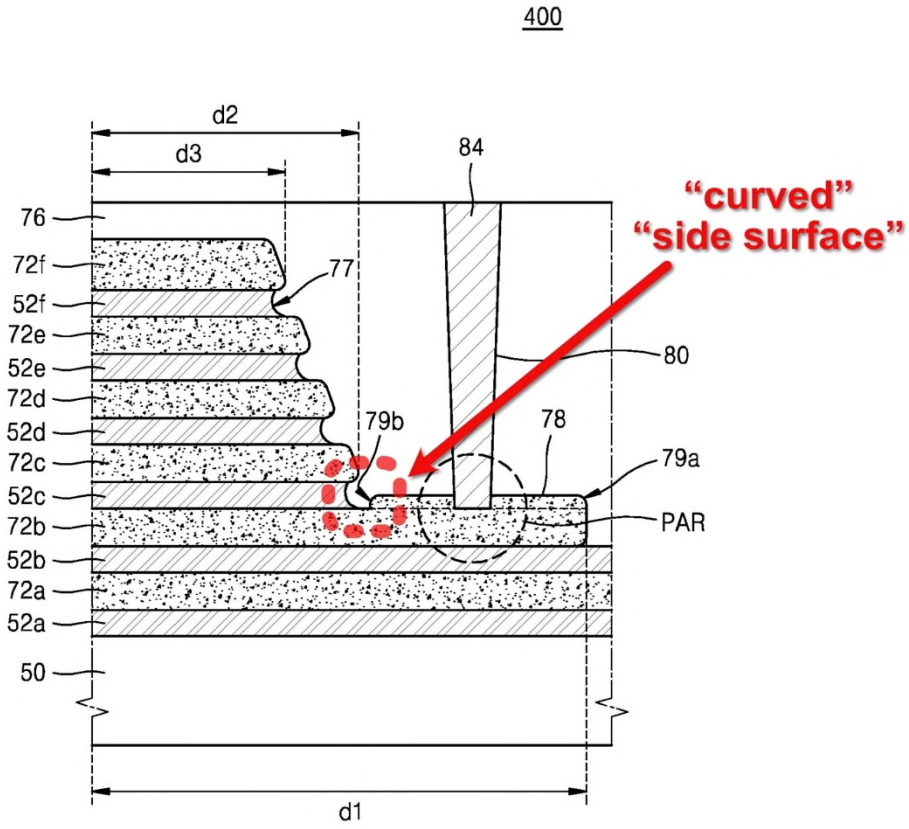
Claim 13 depends on claim 12 and further requires:

[13] "wherein the first side surface comprises a curved side surface."

Lee depicts its pad portions PAD as having straight sides in its figures. Regardless, a POSITA would have considered it obvious to make the ***"side surface"*** of Lee's ***"landing pad" "curved"*** in view of Park's teachings. Again, Park teaches

a three-dimensional memory device that includes a staircase-shaped "connection region" with "pad region[s] PAR" located on the end of gate electrodes. Park, 6:7-12, 7:36-47. Further, each of Park's electrodes terminates with a "pad region PAR" that includes a "raised pad portion" 78. *Id.*, 7:4-16. Per Park, the "end 79b" of this "raised pad portion" 78 may be "rounded" to "prevent a short circuit" between the pad and an "adjacent … conductive layer pattern 72c." *Id.*, 11:35-41. Park achieves its rounded contact pad by performing an "oxidation process" and "ion implanting impurities" "into" an "insulating layer" to create an "additional sacrificial layer" "having a higher etching rate" than the surrounding insulation. *Id.*, 12:16-24, 12:39-47. The sacrificial material is then removed and replaced with conductive material to form insulation-surrounded electrodes and curved pads. *Id.*, 12:48-56. This is shown in Figure 7 from Park:

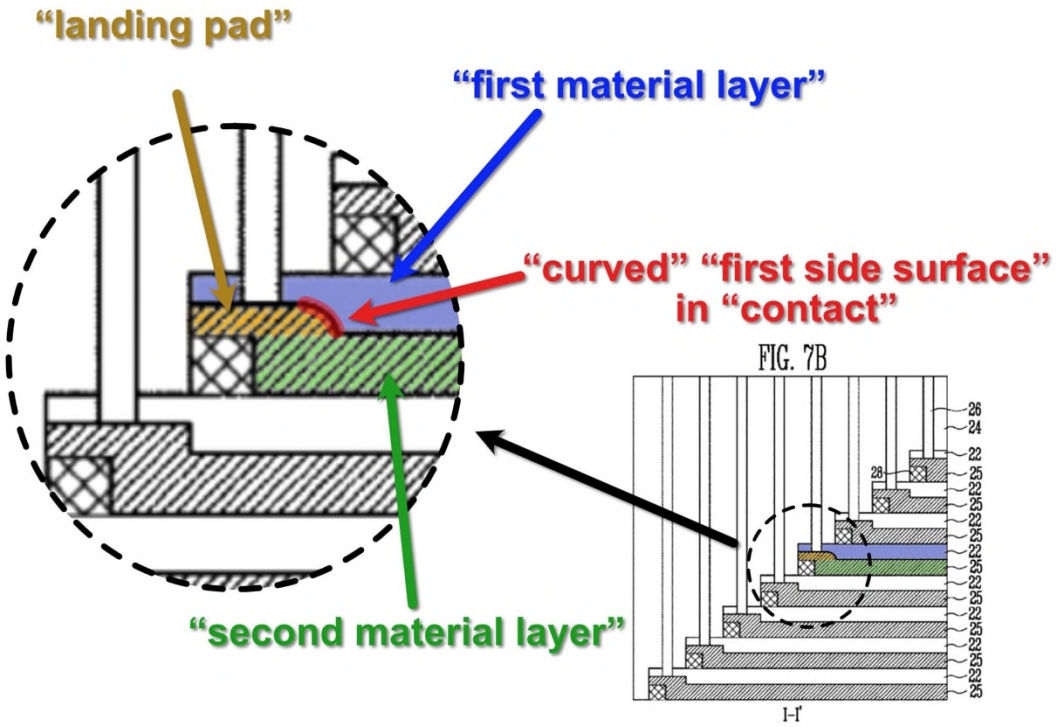
FIG. 7



Id., Fig. 7 (annotated); *see also* Ex. 1003, ¶¶ 460-467. This same process—the implantation of impurities into a layer of insulation to form an etchable region—was also used by other prior art to form contact pads with rounded sides surrounded by insulation. *See, e.g.*, Nam, [0097]-[0105]; Figs. 30-37; *see also* Ex. 1003, ¶¶ 468-469.

Applying Park's teachings to Lee—and making at least the end of Lee's pad portion PAD facing its conductive layers rounded—results in what this limitation requires. Now, the ***"first side surface"*** of Lee's ***"landing pad"*** (pad portion PAD)

that is in ***"contact"*** with the ***"first material layer"*** (insulating layer 22) is ***"curved."*** This is shown in the below demonstrative figure created by further modifying Figure 7B of Lee (note that this figure now includes two modifications: pad rounding following Park's teaching, and the incorporation of layer 28 from Figure 8B of Lee):



Lee, Fig. 7B (modified and annotated); Ex. 1003, ¶¶ 470-477.

A POSITA would have been motivated to make the end of Lee's pad portion PAD facing its insulating and conductive layers rounded. Again, Park explains that rounding the contact pad helps "prevent a short circuit" between the pad and an "adjacent" conductive layer. Park, 11:35-41. Lee already incorporates the barrier layer 28 for purposes of ensuring that there is "sufficient distance … between the stacked conductive layers (pad portions)." Lee, [0049]. Increasing this distance,

according to Lee, reduces the risk that the "breakdown voltage" between these layers may be "deteriorated." *Id.* A POSITA would have understood that applying Park's teachings and rounding Lee's pad portions PAD is both consistent with and supplements this goal. Rounded pad corners would serve to further increase the distance between adjacent conductive layers resulting in an additional reduction in the risk of short circuit and breakdown. *See* Ex. 1003, ¶¶ 478-482.

Contact pads with rounded, curved side surfaces were also a known, routinely used alternative for memory devices with staircase structures at the time the '838 patent was filed. *See, e.g.*, Kim, 8:29-34 (noting that contact pads can have a "curved surface"); Park, 11:35-41 (contact pad can be "rounded"); Yun, 8:33-40 (contact pad can have "rounded" "side surface"; Nam, [0066] (contact pad can have "bull nose" or "convex" shape). Given the prevalence of contact pads with this shape in the prior art, a POSITA would have considered the use of rounded/curved pads with Lee to be nothing more than a routine, obvious design choice. *See* Ex. 1003, ¶¶ 483-484.

A POSITA would also have had every reason to believe that a curved pad could be successfully used with Lee. Again, numerous prior art references identified this type of pad as acceptable for three-dimensional memory devices with staircase structures. *See, e.g.*, Kim, 8:29-34 Park, Fig. 8; Yun, Fig. 5A; Nam, Fig. 8A. Moreover, Lee explains that the shape of its pad portion PAD is controlled via an "ion implantation process." Lee, [0035], [0038]-[0041]. A POSITA would have

recognized that this type of process could be readily adapted to form a curved contact pad. *See, e.g.,* Park, 7:17-29 ("ion implantation" and "oxidation" employed to form pad with "rounded" sides); Nam, [0066], [0098]-[0107]; Figs. 30-39 (discussing use of "an ion implantation process" at length to form "convex" contact pad); *see also* Ex. 1003, ¶¶ 485-489. For example, POSITA would have recognized that Park's process could be readily applied to Park to round Park's contact pads. Lee's ion implantation and etching steps would be performed in the same manner as Lee already teaches. See *id.*, ¶¶ 471-472 . Then, once the openings shown in Figure 5B of Lee are formed, oxidant would be introduced into the opening for a controlled period of time to produce a rounded opening (and later, a rounded contact pad). *See id.*, ¶¶ 472-474.

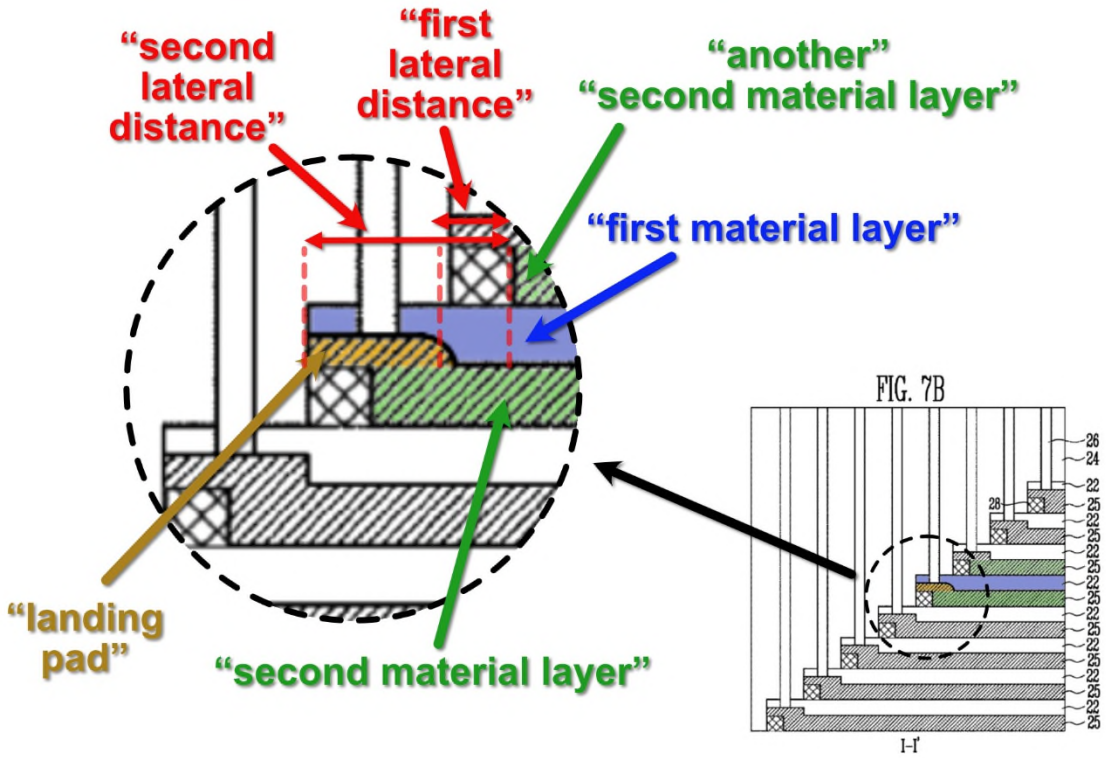
2. Claim 14

Claim 14 depends on claim 13 and further requires:

[14] "further comprising another second material layer disposed on the first material layer, wherein a first lateral distance between the first side surface and a side surface of the another second material layer is smaller than a second lateral distance between the second side surface and the side surface of the another second material layer."

This is taught by Lee. Again, Lee's device includes alternating conductive and insulating layers. Lee, [0021]; *see also id.,* [0010], [0041], [0046]; Figs. 1A, 7A. Because of this, there is ***"another second material layer"*** (a further conductive layer 25) that is ***"disposed on the first material layer"*** (the insulation layer 22

discussed in connection with claims 1 and 12 above). Further, Lee's device is formed "stepwise." *Id.*, [0021]; *see also id.*, [0009]. This causes upper conductive layers to be stepped back from lower layers. Because of this, the "***first lateral distance between the first side surface and a side surface of the another second material layer***" (the distance between a pad's right side in Fig. 7B and the side of the conductive layer above the pad) is ***"smaller"*** than ***"second lateral distance between the second side surface and the side surface of the another second material layer"*** (the distance between the same pad's left side and the conductive layer):



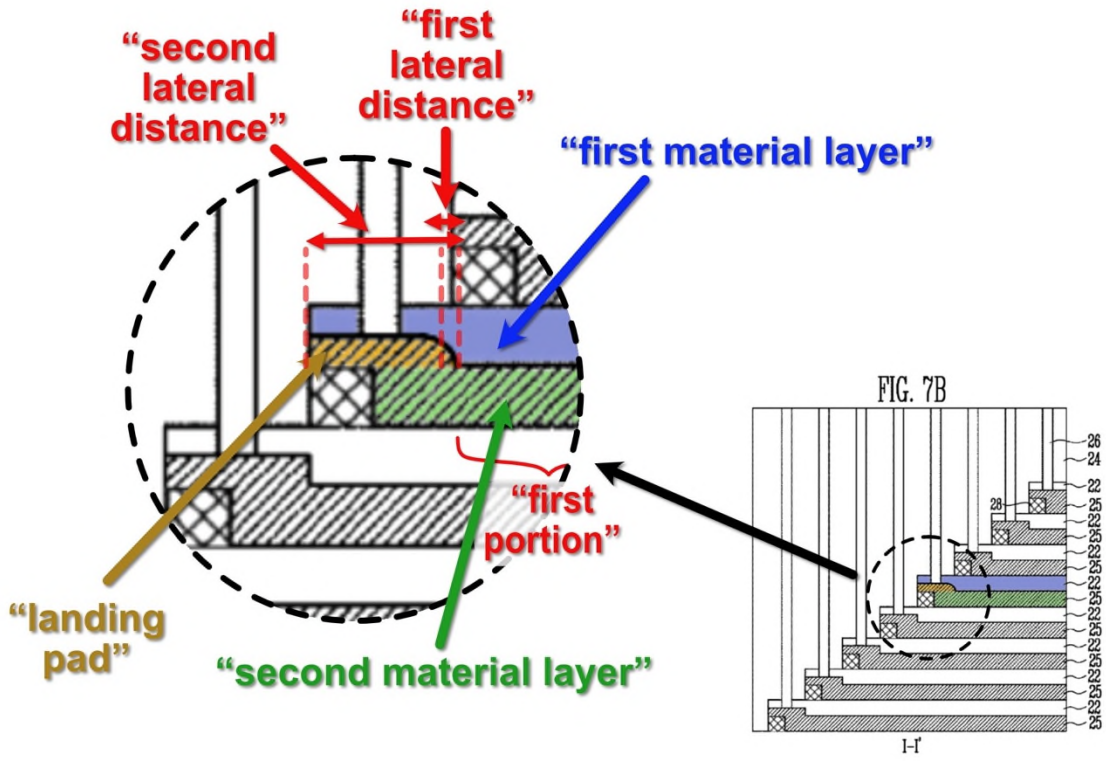
Id., Fig. 7B (modified and annotated); *see also* Ex. 1003, ¶¶ 491-495.

3. Claim 15

Claim 15 depends on claim 13 and further requires:

[15] "wherein the second side surface is laterally displaced from the first side surface, and wherein a first lateral distance between the first side surface and the first portion of the second material layer is smaller than a second lateral distance between the second side surface and the first portion of the second material layer."

This is taught by Lee. As shown in the figure below, because Lee's pad portion PAD has a width, the ***"first"*** and ***"second" "side surface[s]"*** of the pad are "***laterally displaced"*** from each other. Moreover, the pad's width and location on the underlying conductive layer 25 causes "***a first lateral distance between the first side surface and the first portion of the second material layer" (***the distance between the rightmost edge of the pad and conductive layer 25) to be ***"smaller"*** than a ***"second lateral distance between the second side surface and the first portion of the second material layer"*** (the distance between the leftmost edge of the pad and same conductive layer):



Lee, Fig. 7B (modified and annotated); *see also* Ex. 1003, ¶¶ 496-499.

F. Secondary Considerations

There is no evidence in the '838 patent's prosecution history of any pertinent secondary considerations of nonobviousness.

X. Conclusion

For the foregoing reasons, Petitioner respectfully requests institution of PGR and cancellation of claims 1, 3-7, and 12-20.

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR POST GRANT REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 14,047 words.

Dated: January 6, 2025

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for Post Grant Review and associated documents and exhibits were caused to be served on January 6, 2025 via overnight courier upon the following counsel of record for Patent Owner:

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