

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: PGR2025-00021
U.S. Patent No. 12,010,838 B2
Issue Date: June 11, 2024

Title: STAIRCASE STRUCTURE FOR MEMORY DEVICE

**DECLARATION OF DR. JACK C. LEE IN SUPPORT OF
PETITION FOR POST GRANT REVIEW OF
U.S. PATENT NO. 12,010,838**

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I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in the claims of U.S. Patent No. 12,010,838, which I refer to herein as the ’838 patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of \$680 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My *curriculum vitae* (“CV”) is Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and three-dimensional memory technology.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University

of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. This includes classes relating to, among other things, 3D memory technology. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professorship in Engineering in the Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

10. My current research and teaching interests include semiconductor devices, semiconductor memory applications (including non-volatile memory), fabrication processes, silicon-on-insulator technologies, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, and alternative channel materials. I routinely encounter and address topics relating to NAND flash memory, and more specifically 3D NAND flash memory, in my research. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

11. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. Many of these relate to the structure and operation of memory devices, including non-volatile memory such as NAND flash memory and 3D NAND flash memory. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

12. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to

silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

13. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. ASSIGNMENT AND MATERIALS CONSIDERED

14. I have been asked to provide analysis and explain the subject matter of the '838 patent, including the state of the art when the application underlying the '838 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '838 patent including how that art relates to the challenged claims of the '838 patent and to provide my opinions regarding whether that art invalidates the claimed subject matter.

15. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the claims of the '838 patent. Therefore, the fact that I do not address a particular point should

not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

16. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this PGR or related proceedings on the '838 patent.

17. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the '838 patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

Exhibit	Description
1005	U.S. Patent No. 10,229,929 to Kim et al. (“Kim”)
1006	U.S. Patent Publication No. 2014/0191389 A1 to Lee et al. (“Lee”)
1007	U.S. Patent No. 9,941,153 to Yang (“Yang”)
1008	U.S. Patent No. 9,520,402 to Haller et al. (“Haller”)
1009	U.S. Patent No. 10,297,543 to Park et al. (“Park”)
1010	U.S. Patent No. 9,589,978 to Yip
1011	Aritome, “NAND Flash Memory Technologies” (2016)
1012	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1013	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017

Exhibit	Description
1014	U.S. Patent Publication No. 2016/0218107 A1 to Lee (“Lee 107”)
1015	U.S. Patent Publication No. 2015/255385 to Lee
1016	U.S. Patent No. 9,373,540 to Hyun
1017	U.S. Patent Publication No. 2011/0031630 A1 to Hashimoto
1018	Excerpts from the File History of PCT/CN2018/098962
1019	File History of U.S. Patent Application No. 16/126,956
1020	File History of U.S. Patent Application No. 16/885,858
1021	U.S. Patent No. 9,343,452 to Yun et al.
1022	U.S. Patent Publication No. 2018/0026046 A1 to Nam et al.

IV. UNDERSTANDING OF THE LAW

18. I am not an attorney, but have been instructed in and applied the law as described in this section.

19. I understand that the first step in comparing an asserted claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the claims of the alleged invention in Section V below.

20. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of

claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

21. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

22. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

23. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

24. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

25. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

26. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

27. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed

at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

28. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

29. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

30. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

31. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a "nexus," between any such secondary indicia and the claimed invention.

32. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

33. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

34. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

35. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

36. In my opinion, a POSITA in the field of the '838 patent would have had a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or

teaching) 3D memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may substitute for professional experience).

37. In my opinion, this POSITA would also have been aware of and generally knowledgeable about 3D memory's structure, its component parts, and how it operates.

38. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile 3D NAND flash memory—I was a person of more than the ordinary level of skill in the art as of August 2017. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed by taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGICAL BACKGROUND

39. Before addressing the '838 patent in detail, some background on the technology of the '838 patent should be considered.

40. The '838 patent and the prior art discussed in this petition relate generally to three-dimensional (or "3D") memory. One type of memory that is currently implemented as 3D memory is flash.

41. "Flash memory" is a form of "non-volatile memory." Ex. 1010, 1:24-26. "Non-volatile memory is memory that can retain its data values for some extended period without the application of power." *Id.*, 1:26-28. Two common types

of flash memory array architectures are the NAND and NOR architectures. NAND offers a higher integration density and occupies a larger market than NOR flash.

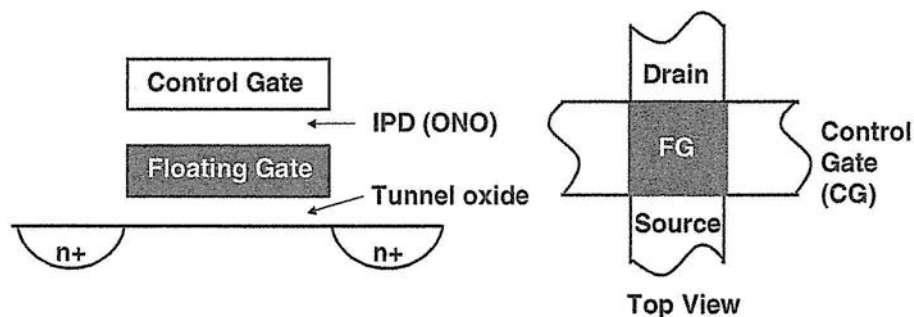
42. NAND flash was first developed in 1987. *See* Ex. 1011, 22.

43. NAND flash stores data in a memory “cell” formed from a single transistor that is the logical equivalent of a NOT AND circuit. Ex. 1011, 38-39.

44. In one known type of NAND flash, the memory cell is formed from a “Nch MOS transistor with [a] poly-silicon floating gate (FG).” Ex. 1011, 38-39. The FG is electrically isolated by the surrounding insulating layer, hence the name, “floating” gate and electrons placed on the floating gate are trapped. In other words, “charge is stored in [the] FG” and the “potential of [the] FG is controlled by [a] control gate (CG) voltage with capacitive coupling between [the] CG and FG.” *Id.* When negative-charge electrons are stored in the FG, these trapped charges push electrons away from the surface of the substrate (the channel) due to coulombic force. The CG would have to be applied a higher voltage to attract electrons back to the channel in order to turn on the transistor. This means that a negative-charged FG causes an increase in the threshold voltage (e.g., to V_{T0}), in comparison to the threshold voltage of an uncharged FG (V_{T1}). Therefore, by sensing the transistor current by applying a voltage (V_{READ}) on the CG where $V_{T1} < V_{\text{READ}} < V_{T0}$, one can determine whether the FG is charged (i.e., the cell is of bit “0”) or uncharged (bit “1”). This is essentially the *reading* operation of a NAND flash cell. To *program*

(or *write*) a NAND flash memory cell, a high voltage (V_{pgm}) is applied to the CG while keeping substrate/source/drain at 0V. “Electrons are injected to the floating gate (FG)” by “a tunneling mechanism through the tunnel oxide” *Id.*, 44. The threshold voltage of the memory cell would increase from V_{T1} to V_{T0} . “An erase operation is performed by applying high-voltage (V_{era}) to substrate...while keeping CG at 0V” *Id.* Electrons in the FG are ejected to the substrate through the tunnel oxide.

45. The below figure provides an example of a flash memory cell:

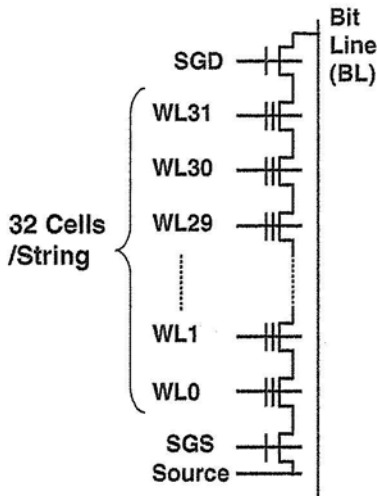


Ex. 1011, 39.

46. Other NAND flash employ a transistor with a “charge trap” layer. *See* Ex. 1012, 109. In this type of transistor, charge is stored in “non-conducting dielectric layer”—like silicon nitride—instead of a floating gate. *See id.*

47. NAND flash memory cells are arranged in so-called “string[s]” with multiple cells “connected in series.” Ex. 1011, 38. The source of one cell is connected to the drain of the next one. Depending on the technology, typically a

string consists of 32 to 128 NAND cells. An example of one such string is shown below:

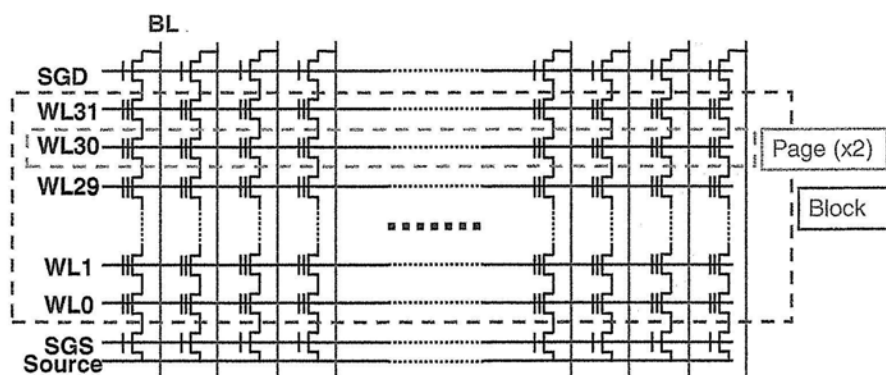
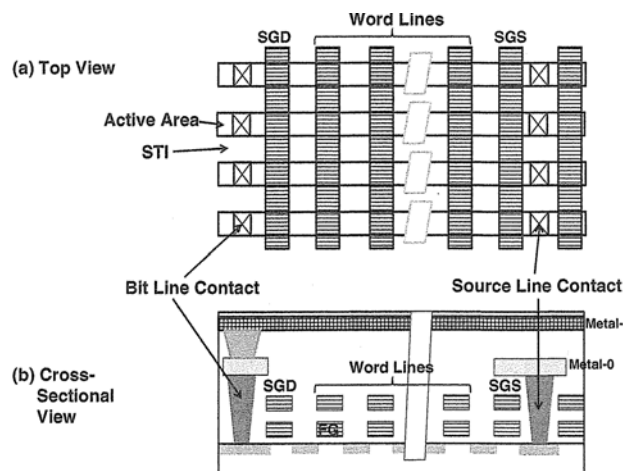


Id., 39.

48. Early NAND flash devices were formed as two-dimensional arrays on a substrate surface.

49. Here, the “memory array is formed by straight active area lines ... and straight gate lines” located on a substrate surface. Ex. 1011, 38. Memory cells are located at the “intersection[s]” of the lines. *Id.*

50. An example of a two-dimensional NAND flash memory array is shown below. Figures (a) and (b) illustrate the top view and the cross-sectional view of the memory array, respectively. The third figure shows the circuit schematic drawing of the memory array.



Ex. 1011, 40.

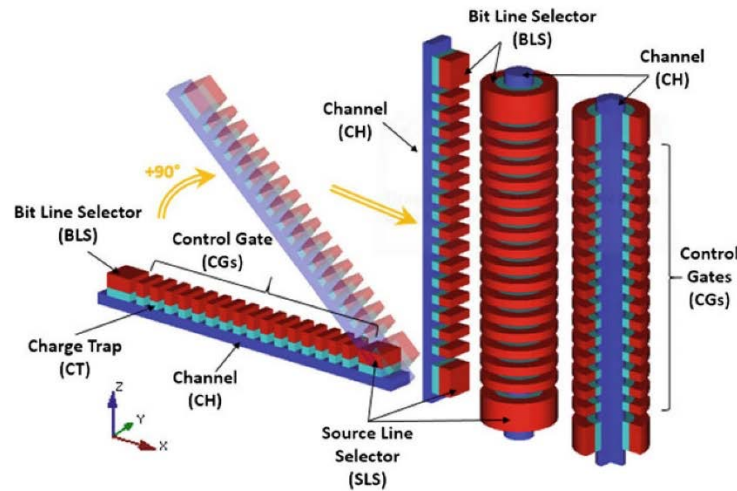
51. As also shown, the cells are grouped into “page[s]” extending along the word lines and “block[s]” which include all the pages along the bit lines, excluding the SGD and the SGS select transistors Ex. 1011, 40. “[R]ead and program operations are performed per page” while “the erase operation is performed per block.” *Id.*, 39. For example, to *read* a selected group of cells, e.g., all the memory cells on the page along WL30 in the circuit schematic above, the voltage on the CG (WL30) is pulled up to V_{READ} while all other word lines (unselected cells) are pulled up above V_{T0} . This way all “[the] unselected cells act as pass transistors.” *Id.*, 45.

A string is selected by a bit line and the drain-end select gate transistor (SGD). The string of memory cells along a bit line would conduct if the selected cell is programmed to bit “1”, i.e. uncharged FG. The *program* operation of the NAND flash is similar to the read operation, except a higher voltage (V_{pgm}) is used on the selected page. The *erase* operation is performed in the entire block consisting of multiple pages. “The word[]lines of the selected blocks are grounded” (*id.*, 47) while high erase voltage (V_{era}) is applied to the p-well (i.e., the “substrate” in the memory cell area). This causes extraction of electrons from the FG into the p-well via tunneling mechanism. All the memory cells in the block are then set to bit “1.” Since the block size is the minimum granularity of erase operation, reducing the block size could reduce the system burden of the data management and thereby improve system performance.

52. To boost data storage densities and reduce cost per gigabit, the art developed so-called “three-dimensional (3D) NAND flash cells” starting in about 2006. Ex. 1011, 292.

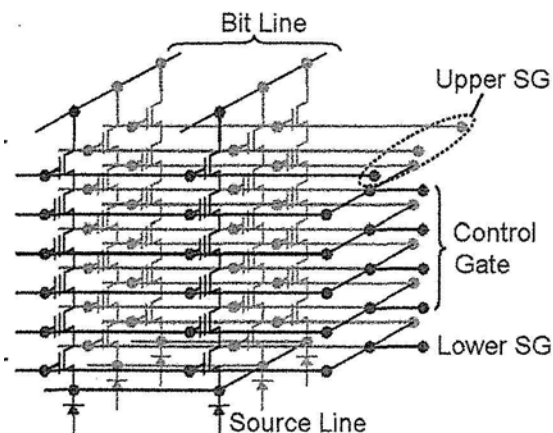
53. In 3D NAND, rather than arranging memory cells in a two-dimensional array, 3D NAND arranges cells in a three-dimensional array that is built up in layers. “Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block” and “turning the 2D NAND string upside,” “resulting” in a “3D structure” with a “vertical channel.” Ex. 1013, 3.

54. The following image provides an example:



Ex. 1012, 122.

55. Multiple of such vertical channels are then repeated in a three-dimensional array:



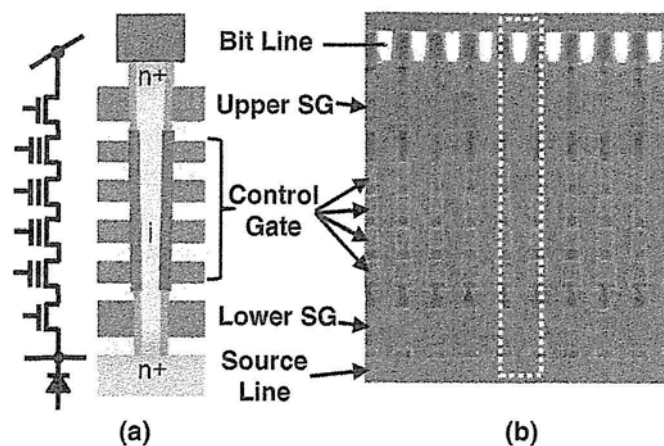
Ex. 1011, 296.

56. 3D NAND includes “multi-stacked layers of gate (plate)” material alternated with “dielectric” “deposited” in a “[s]tack.” Ex. 1011, 294. The flash memory device offers the industry’s highest layer count and the highest areal density

(bits per unit area). A “through-hole is fabricated through” the layers and is “filled by memory film ... and channel poly-Si” to form a string of vertically arranged memory cells. *Id.*, 294-95. “Each” layer of “electrode plate acts as a control gate except the lowest plate,” which “function[s] as the lower select gate (lower SG)”, i.e., SGS, the source-end select gate transistor. *Id.*, 295.

57. “A single bit” of memory cell “is located” at “the intersection of a control gate plate” and the memory film/poly-Si channel. Ex. 1011, 295.

58. An example 3D NAND vertical memory cell string is shown below:

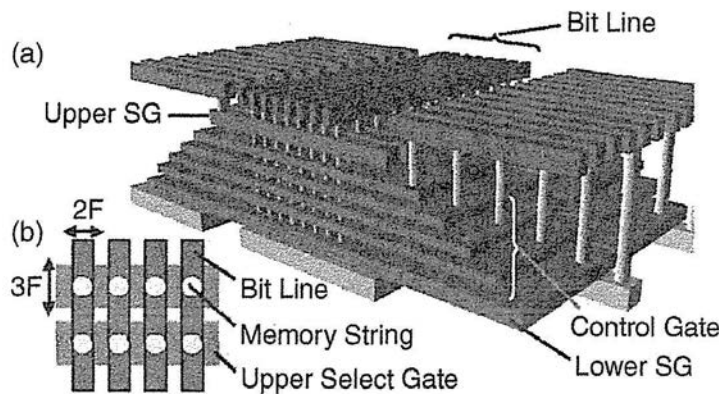


Ex. 1011, 296.

59. For purposes of programming the cells in a memory string, the “string is selected by a bit line and an upper select gate (upper SG).” Ex. 1011, 295.

60. “[T]he control gates and upper/lower SG are connected” to the memory’s conductive “layers at [a] stair-like gate structure” located outside the memory array. Ex. 1011, 295, 297. The stair-like (terrace) structure is created to

expose and allow connection to each conductive layer via vertical word line contacts. The conductive layers are insulated from each other by insulating materials, also known as “dielectrics.” The dielectric layers serve the purposes of preventing interference of electrical signals from one conductive layer to other layers and providing structural support so that the conductive structures do not collapse. An example of this is shown below:



Ex. 1011, 296.

61. “Production of 3D NAND flash memory ... started in August 2013.”

Ex. 1011, 393.

VII. THE '838 PATENT

A. Effective Filing Date

62. I understand that the application leading to the '838 patent was filed on September 13, 2021.

63. Based on my review of the '838 patent, I note that it identifies itself as a continuation of U.S. applications filed September 10, 2018 and May 28, 2020 and

a PCT application filed August 6, 2018. It also identifies an August 28, 2017 foreign filing.

64. For purposes of this declaration, I have been instructed to use August 28, 2017 as the effective filing date of the '838 patent. My opinions in this declaration were formed from the perspective of a POSITA as of August 28, 2017, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

B. Overview

65. The '838 patent relates generally to “a staircase structure for a memory device (e.g., 3D memory device).” Ex. 1001, 1:41-43.

66. The patent notes that this structure somehow results in “yield and manufacturing cost improvements.” Ex. 1001, 1:43-45. But it never explains why that is the case.

67. The patent goes on to reference a “3D memory device” with a “staircase structure[.]” Ex. 1001, 5:34-36.

68. “FIG. 8 illustrates a cross-sectional view of a staircase structure 800 with a dielectric layer 825 disposed thereon.” Ex. 1001, 9:40-42.

69. The structure includes alternating “insulating layer[s] 502” and “wordline layer[s] 804.” Ex. 1001, 9:51-55.

70. Each wordline layer includes a “landing pad 820 and a conductive layer 840” and is intended to “control a portion of a memory string in the stacked storage region of a memory device.” Ex. 1001, 9:62-66.

71. The “landing pad 820 contacts a portion of a side of insulating layer 502.” Ex. 1001, 9:66-10:3.

72. The “landing pad 820” can be “made of the same or different conductive material as conductive layer 840.” Ex. 1001, 10:6-10.

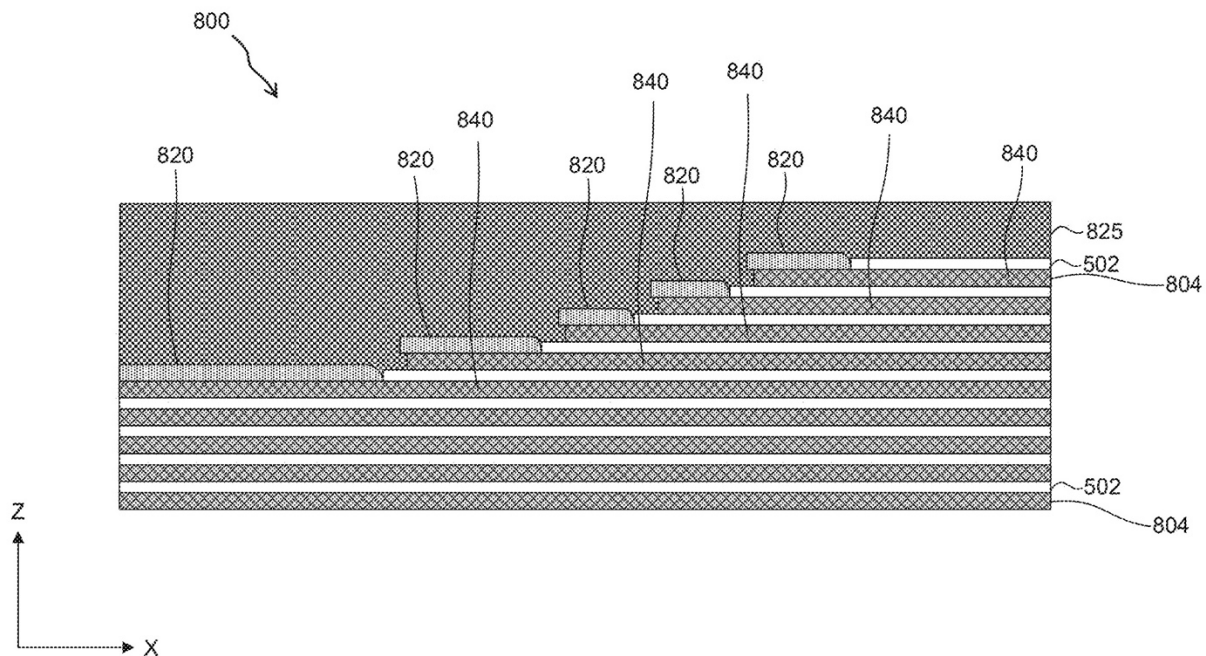


FIG. 8

Id., Fig. 8

C. Prosecution History

73. As noted above, I have reviewed the '838 patent's prosecution history.

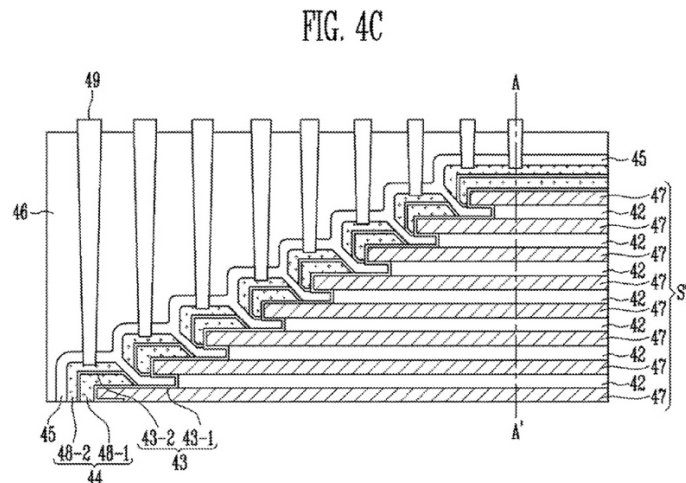
74. The '838 patent was filed May 28, 2020 as U.S. App. 16/885,858 (the "'858 App.") and identifies itself as a continuation of both a 2018 PCT application (PCT/CN2018/098962) and U.S. App. 16/126,956 (the "'956 App."). *See* Ex. 1001, Cover.

75. During prosecution of the application underlying the '838 patent, original independent Claim 1 was rejected as anticipated by U.S. Pub. 2016/0218107 A1 to Lee ("Lee 107," Ex. 1014). Ex. 1002, pp. 150-159.

76. Lee 107 is different from the Lee reference addressed in this Petition.

77. Original Claim 1 of the '838 patent also differed from issued Claim 1: rather than including limitations relating to a landing pad's "side surface[s]," it referenced the pad's "bottom" and "top" surfaces. Ex. 1002, p. 39.

78. In support of the rejection, the Examiner relied on Figure 4C from Lee 107, which is reproduced below:



Ex. 1002, p. 154 (citing Ex. 1014, Fig. 4C).

79. Original independent Claim 9 (which corresponds to issued Claim 1 in the '838 patent) was only rejected for double patenting. Ex. 1002, pp. 155-158.

80. In response, the applicant cancelled Claim 1 and filed a terminal disclaimer. *See* Ex. 1002, pp. 192-200.

81. This then led to allowance of Claim 9. *See* Ex. 1002, pp. 202-209. While prosecution continued in connection with certain other claims, no further prior art was discussed. *See id.*

82. Again, as I note above, the '838 patent also identifies itself as a continuation three other applications. *See* Ex. 1001, Cover.

83. Prior art was discussed during prosecution of these applications. *See, e.g.,* Exs. 1009-1011.

84. Based on my review of the "'838 patent's own prosecution, I note that none of this art was used to reject the '838 patent's claims. *See generally* Ex. 1002.

85. Moreover, the claims at issue in these other applications were materially different from Claims 1 and 12 of the '838 patent. *See, e.g.,* Ex. 1018, pp. 21-24; Ex. 1019, pp. 36-39; Ex. 1020, pp. 31-32.

D. Claims

86. For reference, Claims 1, 3-7, and 12-20 of the '838 patent are reproduced below:

1. A staircase structure of a memory device, comprising:
 - a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and
 - a landing pad disposed over a second portion of the second material layer, wherein the landing pad comprises a first side surface and a second side surface, and wherein the first side surface is in contact with the first material layer and the second side surface is laterally displaced from a side surface of the second portion of the second material layer.
3. The staircase structure of claim 1, wherein a lateral distance between the second side surface and the side surface of the second portion of the second material layer is between 10 nm and 300 nm.
4. The staircase structure of claim 1, wherein the landing pad comprises a conductive material.
5. The staircase structure of claim 4, wherein the conductive material comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof.
6. The staircase structure of claim 1, wherein the second material layer is disposed over a first portion of another first material layer, and wherein a side surface of a second portion of the another first material layer is laterally displaced from the second side surface of the landing pad.

7. The staircase structure of claim 1, wherein the second material layer comprises a first conductive material and the landing pad comprises a second conductive material substantially the same as the first conductive material.

12. A memory device, comprising:

a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and

a landing pad disposed over a second portion of the second material layer, wherein the landing pad comprises a first side surface and a second side surface, and wherein the first side surface is in contact with the first material layer and the second side surface is laterally displaced from a side surface of the second portion of the second material layer.

13. The memory device of claim 12, wherein the first side surface comprises a curved side surface.

14. The memory device of claim 13, further comprising another second material layer disposed on the first material layer, wherein a first lateral distance between the first side surface and a side surface of the another second material layer is smaller than a second lateral distance between the second side surface and the side surface of the another second material layer.

15. The memory device of claim 13, wherein the second side surface is laterally displaced from the first side surface, and wherein a first

lateral distance between the first side surface and the first portion of the second material layer is smaller than a second lateral distance between the second side surface and the first portion of the second material layer.

16. The memory device of claim **12**, wherein the second material layer comprises tungsten, and titanium nitride.

17. The memory device of claim **12**, wherein the second material layer comprises a first conductive material and the landing pad comprises a second conductive material substantially the same as the first conductive material.

18. The memory device of claim **12**, wherein a lateral distance between the second side surface and the side surface of the second portion of the second material layer is between 10 nm and 300 nm.

19. The memory device of claim **12**, further comprising:

a dielectric layer disposed over the first material layer and the landing pad, wherein the first material layer comprises a first dielectric material and the dielectric layer comprises a second dielectric material, wherein the first dielectric material is substantially the same as the second dielectric material, and wherein the first dielectric material comprises silicon oxide.

20. The memory device of claim **12**, wherein the second material layer is disposed over a first portion of another first material layer, and wherein a side surface of a second portion of the another first material layer is laterally displaced from the second side surface of the landing pad.

VIII. CLAIM CONSTRUCTION

87. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in a post grant review, and I have applied them in forming my opinions. I understand that during post grant review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

88. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the “intrinsic evidence” or “intrinsic record”).

89. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the “extrinsic evidence” or the “extrinsic record”), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

90. In my opinion, the terms of the '838 patent's claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration. I have provided further discussion of how a POSITA would have understood the '838 patent's claim terms in the sections below.

IX. UNPATENTABILITY ANALYSIS

91. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '838 patent, a POSITA would have considered Claims 1, 3-7, and 12-20 of the '838 patent to be unpatentable as obvious over the prior art discussed in this declaration.

A. Overview of the Prior Art

92. The following paragraphs provide an overview of the main prior art references I discuss throughout this declaration.

1. Kim

93. Kim (Ex. 1005) indicates on its face that it was filed in the U.S. on July 18, 2017. *See* Kim, Cover. In view of this date filing, which is before the '838 patent's own August 2017 effective filing date, I understand that Kim is prior art under 35 U.S.C. § 102(a)(2).

94. Kim relates to “semiconductor memory devices having enhanced reliability.” Kim, 1:38-39.

95. The device can be implemented as a “3D semiconductor memory device[]” with “memory cells ... arrayed in 3D.” Kim, 1:26-30.

96. According to Kim, the device includes a “cell array region” and a “contact region.” Kim, 1:41-46.

97. The “cell array region” includes “memory cell[s]” arranged in vertically oriented memory “cell strings.” Kim, 4:26-28; *see also* Fig. 3 (showing Kim's 3D

array of memory cells with multiple example cell strings “CS”). The “contact region” includes a “stacking structure” with a “stepwise structure.” *Id.*, 1:40-47.

FIG. 4B

Kim, Fig. 4B.

100. The “gate electrodes” are formed from conductive material. Kim, 6:31-35.

101. The insulating layer 110 can be integrated with an “auxiliary insulating layer 122.” Kim, 9:29-38.

102. Each gate electrode 300 includes a “pad unit PAD” formed from “a base pad PAD_B and a protrusion pad PAD_P...” Kim, 7:58-62. The pad units PAD “electrically and physically connect” the gate electrodes 300 to an upper “connection line CTL.” *Id.*, 9:64-66.

103. As shown in Figure 4B, “protrusion pad PAD_P” is located “inside” and is touching the sides of “opening 122_O” in Kim’s insulation layer 122. Kim, 9:21-23.

104. While PAD_P is shown with a rectangular shape in the figure, Kim explains that it can “[also] have a shape including a curved surface based on a virtual rectangular parallel[] shape, a cylindrical shape, or any shape.” Kim, 8:29-34.

2. Lee

105. Lee (Ex. 1006) indicates on its face that was filed in the U.S. on March 18, 2013 and published on July 10, 2014. Lee, Cover. In view of these dates of filing and publication, both of which pre-date the ’838 patent’s own August 2017 filing, I understand that Lee is prior art under AIA §§ 102(a)(1) and 102(a)(2).

106. Lee relates to “semiconductor device[s]” such as “three-dimensional (3D) non-volatile memory devices.” Lee, ¶¶ [0005], [0008]-[0009].

107. Per Lee, this type of device is intended to “increase[] ... integration” of a memory by including more memory cells in a smaller space. Lee, ¶ [0005].

108. Lee goes on to explain that this type of memory includes “interlayer insulating layers and word lines stacked alternately with each other” over a substrate. Lee, ¶ [0006].

109. “[C]hannel layers” pass through the stack to form “[m]emory cells.” Lee, ¶ [0006]. The stack is “patterned stepwise” to allow for connection or contact with each layer. *Id.*, ¶ [0009].

110. According to Lee, existing three-dimensional memories encountered difficulties when “form[ing] pad portions on word lines stacked on top of one another....” Lee, ¶ [0007]. In these devices, “a punch phenomenon may occur in which a contact plug passes through a pad portion, or the contact plug and the pad portion are not coupled to each other since a pad portion is not exposed along a bottom surface of a contact hole.” *Id.*

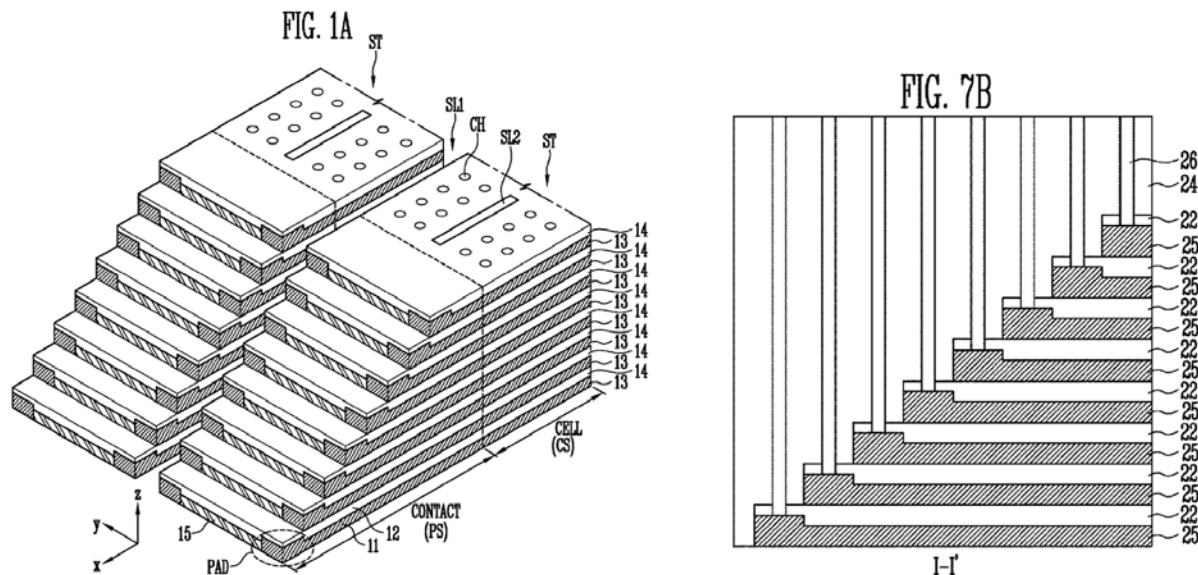
111. Lee then goes on to discuss a “semiconductor device” that, like known three-dimensional memories, includes a “stacked structure ST” with alternately arranged “insulating layers” and “conductive layers.” Lee, ¶¶ [0020]-[0021].

112. The “stacked structure ST” is “patterned stepwise” with an “insulating layer ... located on [the] top surface of each step.” Lee, ¶ [0021].

113. To address the problems with prior art memories, however, Lee includes “pad portions PAD” at the end of each of conductive layers in a “contact region CONTACT” of its stepped “stacked structure ST.” Lee, ¶¶ [0022]-[0023].

114. “The pad portions PAD” have a “greater thickness than unexposed portions of the ... conductive layer[s].” Lee, ¶ [0023]. Use of a thicker pad prevents the various contact problems experienced by prior art devices. *See id.*, ¶ [0043].

115. Lee’s pads are shown in both Figures 1A (a three-dimensional view) and 7B (a cross-sectional view):



Lee, Figs. 1A, 7B.

3. Yang

116. Yang indicates on its face that it was filed in the U.S. on December 22, 2016 and published April 10, 2018. Yang, Cover. In view of these dates of filing

and publication, both of which pre-date the '838 patent's own August 2017 filing, I understand that Yang is prior art under AIA §§ 102(a)(1) and 102(a)(2).

117. Yang relates to “a pad ... applied to a three-dimensional (3D) memory device” with a stepped structure. Yang, 1:6-10; *see also id.*, Fig. 2.

118. Yang discusses the dimensions of its device's steps, conductive and insulating layers, and pads at length. *See* Yang, 5:45-6:28; 7:22-65; 10:7-21.

4. Park

119. Park (Ex. 1009) indicates on its face that it was filed in the U.S. on June 13, 2017. Park, Cover. As this date of filing pre-dates the '838 patent's own August 2017 filing, I understand that Park is prior art under AIA § 102(a)(2).

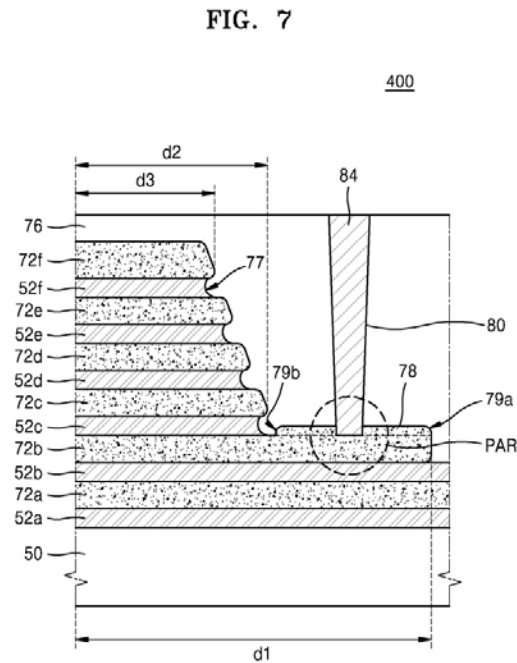
120. Park relates to a “vertical semiconductor device” with an array of “stacked” “memory cells.” Park, 1:14-19.

121. The device includes a stepped “connection region” with alternating conductive gate electrodes and insulating layers. Park, 6:7-11.

122. Raised “[p]ad region[s] PAR” are located on the ends of gate electrodes. Park, 6:7-11, 6:36-47, 7:4-16.

123. Park also explains that rather than having straight sides, an “end 79b” of each of these “raised pad portion 78” may be “rounded” to “prevent a short circuit” between the pad and an “adjacent ... conductive layer pattern 72c.” Park, 11:35-41.

124. This is shown in Figure 7 from Park below:



Park, Fig. 7.

5. Haller

125. Haller (Ex. 1008) indicates on its face that it was filed in the U.S. on August 25, 2015 and issued December 13, 2016. Haller, Cover. In view of these dates of filing and issuance, both of which pre-date the '838 patent's own August 2017 filing, I understand that Haller is prior art under AIA §§ 102(a)(1) and 102(a)(2).

126. Haller relates to a “3D memory device” with a “staircase structure.” Haller, 4:8-12.

127. Haller's device includes an “etch stop” at the end of each of its conductive wordline layers. Haller, 2:6-9.

128. The etch stop is dimensioned to “prevent ... physical or electrical contact” between adjacent wordlines. Haller, 2:19-23; *see also id.*, Fig. 9

B. Ground 1: Claims 1, 4-7, 12-17, and 19-20 Are Obvious Over Kim

129. In my opinion, a POSITA would have considered Kim to be within the scope of the prior art and highly relevant to the patentability of the ’838 patent’s claims.

130. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Kim renders Claims 1, 4-7, and 12-17, and 19-20 of the ’838 patent obvious.

1. Claims 1 and 12

131. With the exception of their preambles, independent Claims 1 and 12 are identical. Because of this similarity, I will assess these claims together below.

[1.Pre] “A staircase structure of a memory device, comprising:”

[12.Pre] “A memory device comprising”:

132. To the extent this preamble language is limiting, in my opinion it is taught by Kim.

133. Kim relates to “a semiconductor memory device.” Kim, Abstract.

134. Indeed, Kim repeatedly explains that “[e]mbodiments of the inventive concepts relate to semiconductor memory devices....” Kim, 1:15-17; *see also id.*, 1:38-39 (“[T]he inventive concepts ... provide semiconductor memory devices having enhanced reliability.”); 3:43-44 (“FIG. 1 is a block diagram illustrating a

schematic configuration of a plan view [of] a semiconductor memory device....”);
Fig. 1.

135. Moreover, Kim explains that it relates not just to memory, but to three-dimensional memory. In particular, Kim’s device can be a “3D semiconductor memory device[]” with “memory cells ... arrayed in 3D” for purposes of improving “integration.” Kim, 1:26-30; *see also id.*, Figs. 3, 4A, 4B, 5-9.

136. The “integration” of a memory device refers to the number of memory cells arranged in a particular space. By forming its memory three-dimensionally, Kim is able to locate more memory cells within a given device footprint.

137. In my opinion, Kim also teaches that its memory device includes a “*staircase structure.*”

138. According to Kim, the “semiconductor memory device” includes both a “cell array region” and an adjacent “contact region.” Kim, 1:40-47.

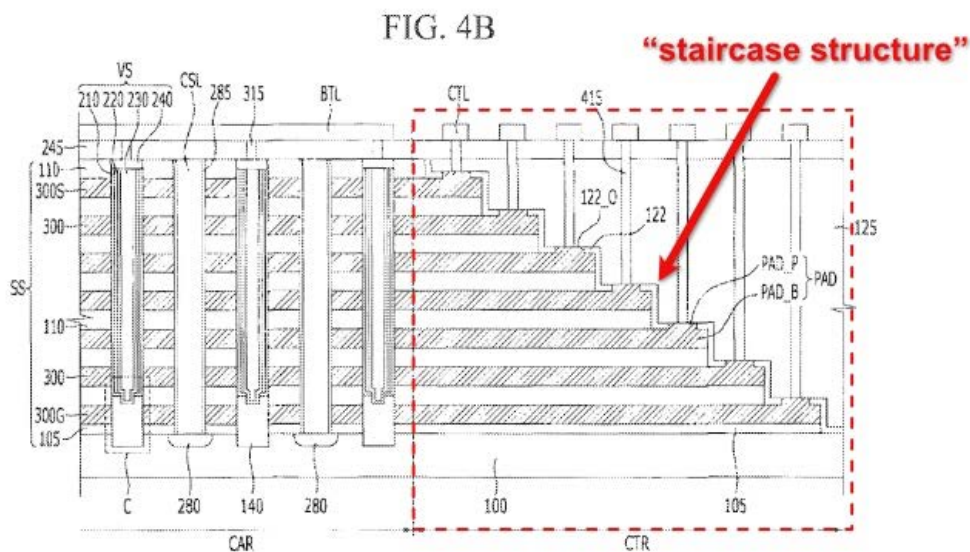
139. The “contact region” includes a “contact structure” with a “stepwise structure.” Kim, 1:40-47. The “stepwise structures” facilitate connection to its conductive layers. *Id.*, 1:15-17.

140. Figure 4B, which is reproduced below, provides an example of this stepped contact structure.

141. As shown in the figure, Kim's device includes a "cell array region (CAR)" that includes "vertical pattern structures VS" forming strings of memory cells. Kim, 5:33-39.

142. A "contact region CTR" with a stepped structure is "positioned on the periphery of the cell array region CAR." Kim, 5:33-39; *see also* 3:52-62 (similarly explaining that Kim's "memory device" includes a "cell array region (CAR)" with "a plurality of memory cells" and an adjacent "contact region CTR"); 6:42-46 (the "vertical pattern structures VS" are "surrounded by the" step-shaped "stacking structure SS on an xy-direction plane").

143. Kim's "***staircase structure***" is shown in Figure 4B below:



Kim, Fig. 4B (annotated).

[1.A]/[12.A] “a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and”

144. Claims 1 and 12 next require a ***“first material layer”*** that is ***“disposed over a first portion”*** of a ***“second material layer.”***

145. Before discussing Kim’s teachings, I will briefly summarize how the ’838 patent uses the term “layer.”

146. The ’838 patent includes a paragraph discussing the term “layer.” *See* Ex. 1001, 4:36-56

147. In this paragraph, the patent explains that a “layer” does not need to be only a single, defined layer of homogenous material. Instead, a “layer can include ***multiple*** layers” and can be ***“inhomogeneous.”*** Ex. 1001, 4:39-59 (emphasis added). The patent also explains that a “layer” can simply be material “located between any set of horizontal planes....” *Id.*, 4:48-51.

148. Moving back to Kim, Kim explains that its memory device includes a step-shaped “stacking structure SS” formed from a “plurality” of alternating “insulating layers 110 and ... gate electrodes 300” located “on the substrate 100.” Kim, 5:53-55.

149. Likewise, Kim notes that the “stacking structure” includes “a plurality of insulating layers and a plurality of gate electrodes alternately stacked on the substrate. The stacking structure may” have “a stepwise structure....” Kim, 1:41-46.

150. “The plurality of insulating layers 110 may be, for example, silicon oxide layers.” Kim, 6:35-36.

151. Kim’s device includes an “auxiliary insulating layer 122.” Kim, 9:12-13.

152. “The auxiliary insulating layer 122 may include the same or similar material as the insulating layer 110” such that “a boundary between the auxiliary insulating layer 122 and the insulating layer 110 may not be distinguished and the auxiliary insulating layer 122 and the insulating layer 110 may form one structure.” Kim, 9:29-38.

153. Kim forms the auxiliary layer 122 immediately after forming its staircase such that this layer such becomes “one structure” with the insulating layers 122 to extend the insulating layers in the horizontal direction. Kim, 12:34-37.

154. In my opinion, a POSITA would have understood that Kim’s insulating layer 110 and the adjacent portion of auxiliary insulation layer 122 together constitute the claimed “*first material layer.*”

155. To begin, in Kim, insulating layers 110 are located between and serve to separate the gate electrodes 300 making up Kim’s stack. Kim, 5:53-55; Fig. 4B.

156. A POSITA would have recognized that auxiliary insulating layer 122 also forms an integral part of this same stack. It is not simply a conformal or protecting layer of oxide applied over complete conductive layers with contact pads.

157. Rather than being a protective layer, auxiliary layer 122 is applied *before* Kim's contact pads are formed. In particular, after "the plurality of insulating layers 110" are "patterned in the stepwise structure in the contact region CTR," then the auxiliary insulating layer 122: is "formed thereon." *See* Kim, 12:34-37; Fig. 11.

158. Then, the auxiliary insulating layer 122 is used to form the contact pads. An "ion injection process" is used to form a "doped region 122_I" in the layer. Kim, 12:61-13:11. This doped region will eventually correspond to the contact pads. Another "buried insulating layer 125" is applied over the staircase structure. *Id.*, 13:15-20. Then, sacrificial layers and the doped region are etched away to form openings, including an "opening 122_O" that will correspond to the pads. *Id.*, 13:51-14:17. The openings are then filled with conductive material. *Id.*, Figs. 13, 16, 17. The layer 122 remains behind in Kim's final device. *See, e.g., id.*, Fig. 17.

159. Put another way, Kim's layer 122 does more than simply cover and protect the staircase's conductive layers. Instead, it is used during the formation of Kim's contact pads, is part of what defines the pads' structure, and is thus part of Kim's stacked staircase structure.

160. Because the layer 122, along with layer 110, is used to define Kim's stacked structure, and because layers 110 and 122 are formed from the same material such that they "form one structure" as Kim itself states, in my opinion a POSITA would have understood that they together form a "*first material layer.*"

161. While I recognize that Kim labels the layers 110 and 122 with separate item numbers, as I have explained the '838 patent states that the term “layer” is meant to embrace insulating layers formed from multiple components. *See* Ex. 1001, 4:39-59 (explaining that a “layer” can be “inhomogeneous” and formed from “multiple” layers).

162. Moreover, the '838 patent also explains that a “layer” can be the material “located between any set of horizontal planes.” Ex. 1001, 4:48-51.

163. This is what Kim teaches: insulating layer 110 and the adjacent portion of auxiliary insulating layer 122 are located between the planes formed by the bottom of one gate electrode 300 and the top of another, adjacent gate electrode 300. *See, e.g.,* Kim, Fig. 4B.

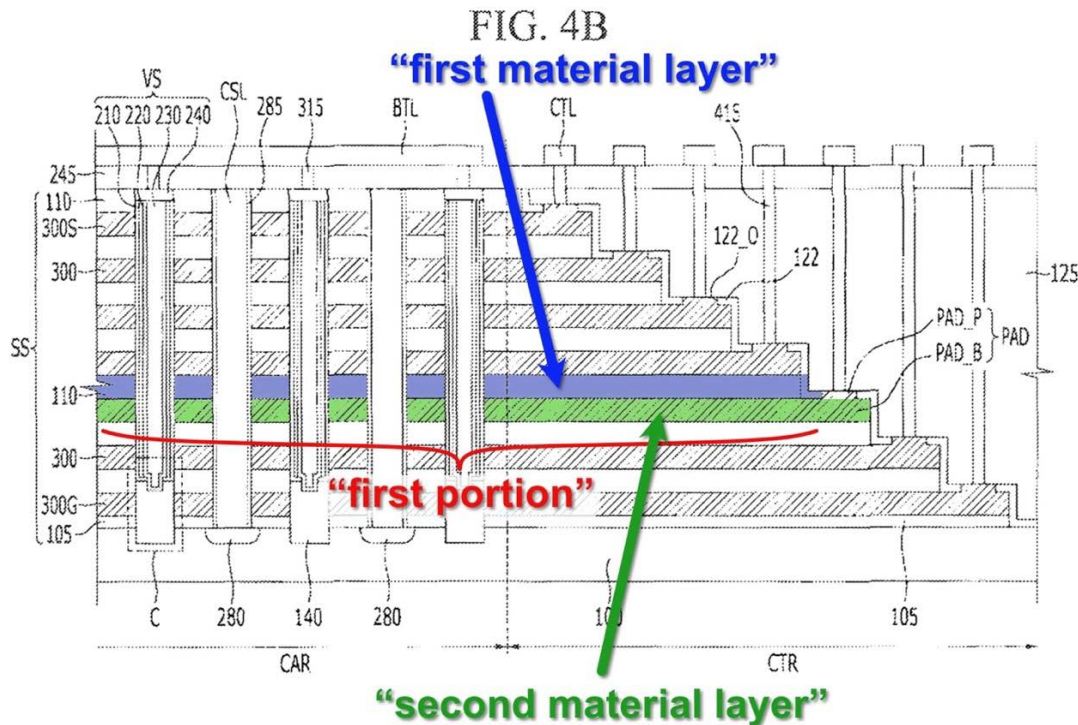
164. Next, Kim’s device also includes the claimed “***second material layer.***”

165. Again, as I noted above, in Kim, there are “gate electrodes 300” located between insulating layers in the stacking structure. Kim, 5:53-55; *see also id.*, 1:41-46.

166. The “gate electrodes 300” can be formed from conductive material such as, among other things, “metal (for example, tungsten, copper, and aluminum). . . .” Kim, 6:31-35.

167. Figure 4B is reproduced below. As shown in this figure, Kim includes a “***first material layer***” (the combination of Kim’s insulating layer 110 and auxiliary

insulating layer 122) and “*second material layer*” (the gate electrode 300). As also shown, the “*first material layer*” is “*disposed over a first portion*” of the “*second material layer*”:



Kim, Fig. 4B (annotated).

[1.B]/[12.B] “a landing pad disposed over a second portion of the second material layer,”

168. In my opinion, Kim teaches the claimed “*landing pad.*”

169. As I have explained, Kim’s “stacking structure SS” includes alternating “insulating layers 110 and ... gate electrodes 300[.]” Kim, 5:53-55.

170. “An end of” each “gate electrode 300” is “exposed through the stepwise structure” and includes a “pad unit PAD” formed from “a base pad PAD_B and a protrusion pad PAD_P...” Kim, 7:58-62.

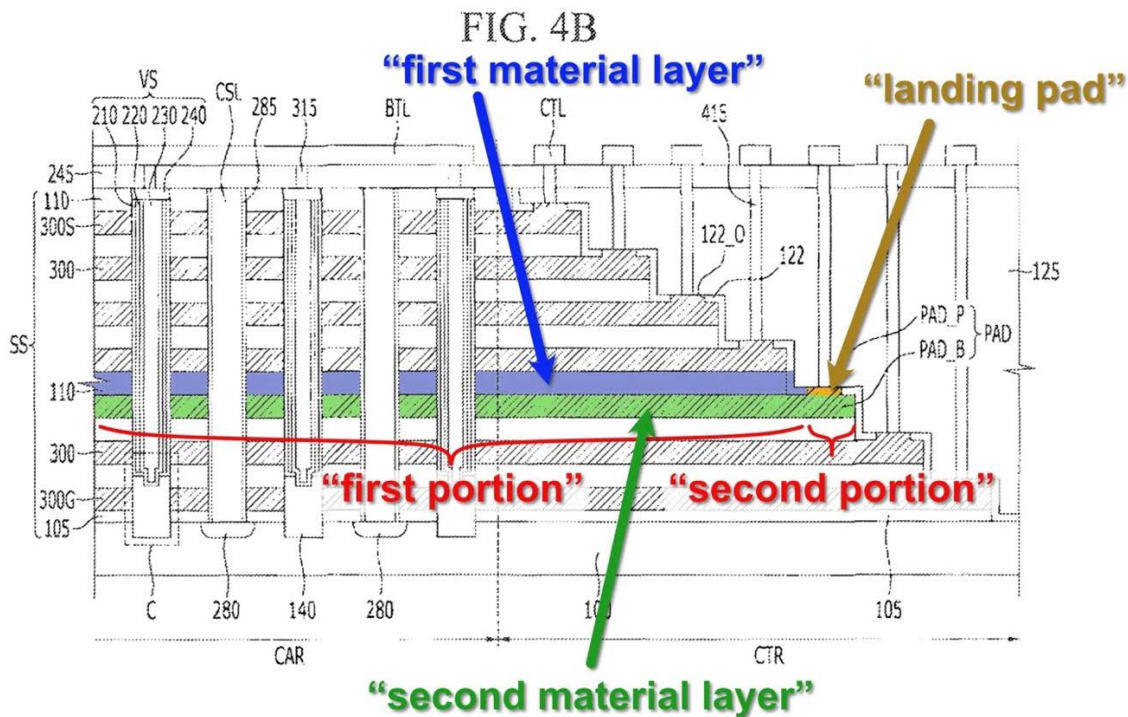
171. “The base pad PAD_B may be a part of the gate electrode 300 in the contact region CTR.” Kim, 7:63-64. “The protrusion pad PAD_P may contact the ... uppermost surface of the base pad PAD_B.” *Id.*, 8:3-10; *see also id.*, 7:61-62 (noting that the “protrusion pad PAD_P contact[s] a surface of the base pad PAD_B”); 10:23-25 (similarly referencing location of “the protrusion pad PAD_P” on a “surface of the base pad PAD_B” and”).

172. The pad units PAD “electrically and physically connect” the gate electrodes 300 to a “connection line CTL” via a “word line contact plug 415.” Kim, 9:64-66.

173. The “gate electrode 300” and the attached “base pad PAD_B and ... protrusion PAD_P” may be formed from the same “common material composition” such as a “metal.” Kim, 6:31-35, 14:12-17.

174. Put another way, each PAD on the end of Kim’s gate electrodes is made from metal and allows for electrical interconnection between the gate electrode and an associated word line (or connection line CTL) via a contact plug that contacts the protrusion pad PAD_P.

175. This structure is shown in Figure 4B from Kim below. Kim’s device includes a “*landing pad*” (protrusion pad PAD_P, annotated orange) that is located over a “*second portion*” of a “*first material layer*” (the PAD_B at the end of gate electrode 300, annotated green):



Kim, Fig. 4B (annotated).

[1.B.1] / [12.B.1] “wherein the landing pad comprises a first side surface and a second side surface,”

176. This, in my opinion, is taught by Kim.

177. Kim explains that each “gate electrode 300” includes a “pad unit PAD” at its end. Kim, 7:58-59.

178. Further, each of these “pad unit[s]” includes a “base pad PAD_B and a protrusion pad PAD_P contacting a surface of the base PAD_B.” Kim, 7:59-62.

179. As I explained above, Kim’s “protrusion pad PAD_P” is the claimed **“landing pad.”**

180. Kim also discusses the shape of this protrusion pad. In particular, the “protrusion pad PAD_P” extends upward from the “surface of the base pad PAD_B”

[1.B.2] / [12.B.2] “wherein the first side surface is in contact with the first material layer and the second side surface is laterally displaced from a side surface of the second portion of the second material layer.”

183. In my opinion, Kim, in view of the knowledge of a POSITA, renders this limitation obvious.

184. In Kim, the ***“first side surface”*** of Kim’s ***“landing pad”*** is in ***“contact with the first material layer”*** as this limitation requires.

185. As I have explained, Kim’s stacking structure includes “insulating layers 110” and “auxiliary insulating layers 122” made from the same material such that they “form one structure.” Kim, 9:29-38.

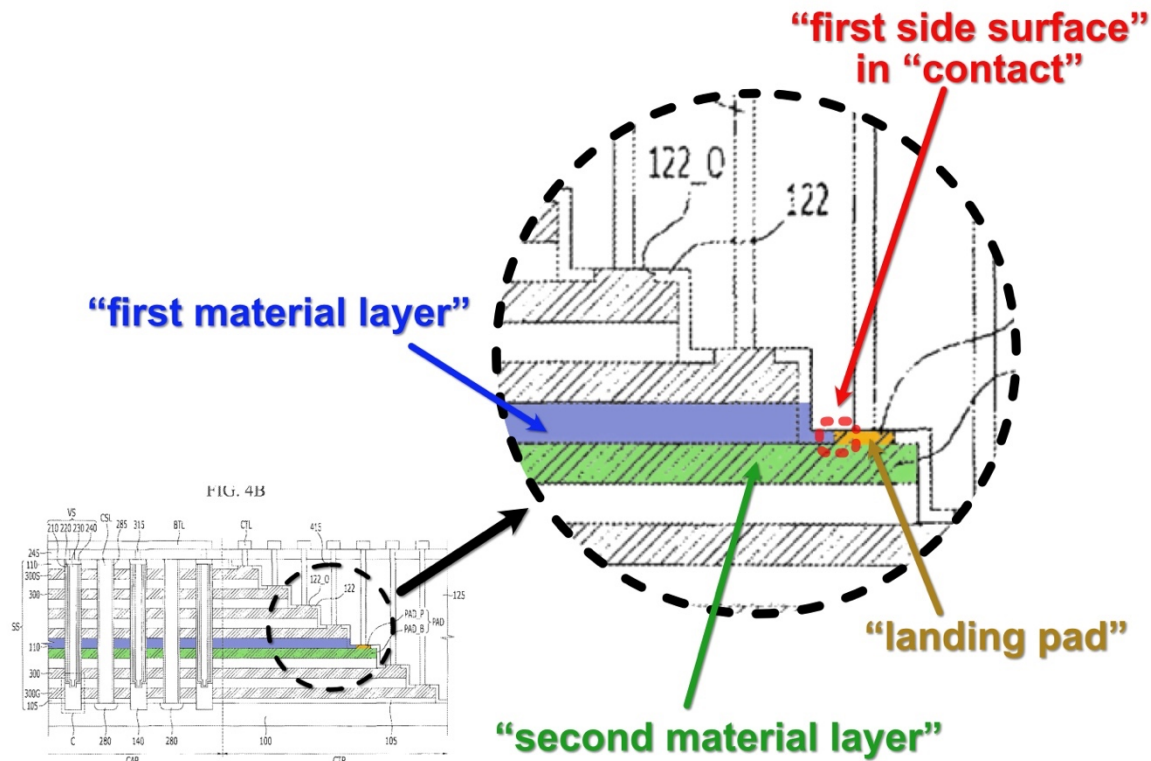
186. Further, in Kim, the insulation layers 110 and auxiliary insulation layers 122 are formed sequentially before the protrusion pads. *See, e.g.*, Kim, 12:34-37; Fig. 11. Then, the layer 122 is used to shape the pads. *See id.*, 12:61-13:11.

187. In my opinion, and as I explained in greater detail above when discussion limitation [1.A], layers 110 and 122 together correspond to the claimed ***“insulating layer.”***

188. Kim also explains that “auxiliary insulating layer 122” has an “opening 122_O and the protrusion pad PAD_P” is located “inside” this “opening 122_O.” Kim, 9:21-23.

189. This opening 122_O is filled with conductive material to form PAD_P during gate electrode forming process. Kim, 13:51-14:17, Figs. 16-17.

190. Figure 4B is reproduced below. The portion of this figure showing one of Kim's protrusion pads PAD_P is expanded to right. As shown, because Kim's protrusion pad PAD_P is located within and fills the opening 122_O in its auxiliary insulation layer 122, there is there is *"contact"* between the *"first side surface"* of Kim's *"landing pad"* (the protrusion pad PAD_P) and its *"first material layer"* (the auxiliary insulating layer 122):



Kim, Fig. 4B (annotated).

191. Next, Kim explains that its "base pad PAD_B may include four edges E1, E2, E3, and E4." Kim, 8:35-36. Edges E1 and E2 are "perpendicular to the extension direction (x-direction) of the gate electrode 300" (i.e., at the point where

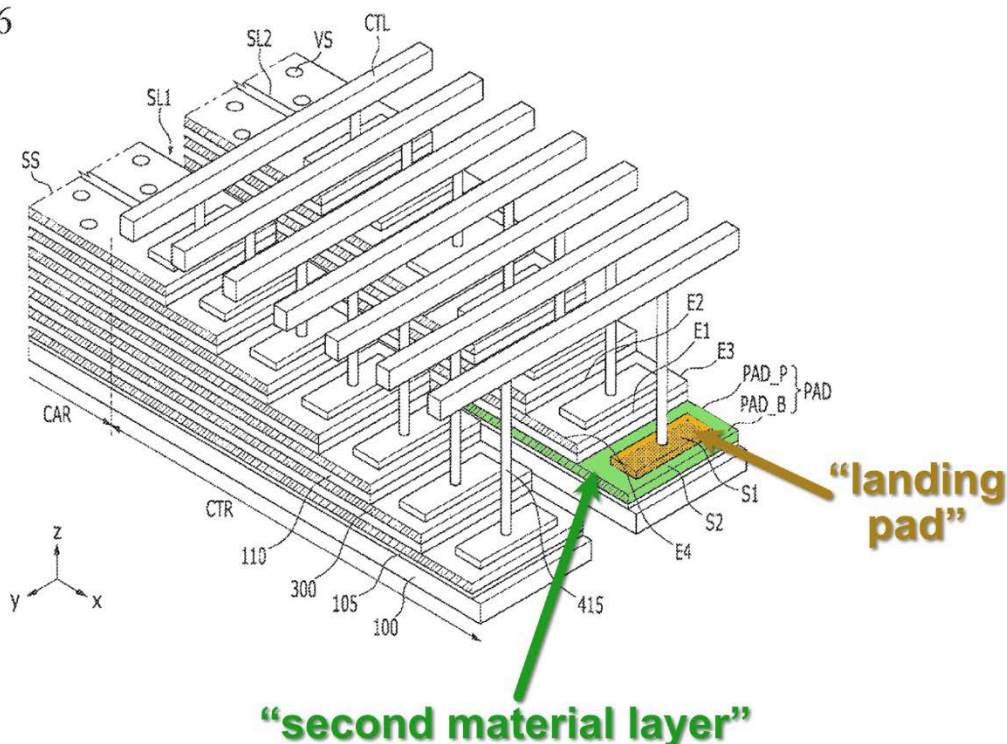
the base pad begins along the electrode's length, and at the very end of the gate electrode). *Id.*, 8:36-46.

192. Kim goes on to explain that the “protrusion pad PAD_P” may be formed and located such that it is “**inside** from the edges E1 and E2” and does not “align[]” with or “overlap” those edges. Kim, 8:47-51 (emphasis added). Thus, “[t]he protrusion pad PAD_P may have a shape in which the protrusion pad PAD_P is **inside and spaced apart from the edges E1 and E2**” leaving “portions S2 of the respective base pad PAD_B” uncovered by protrusion pad PAD_P. *Id.*, 8:51-59. Put another way, the “area in which the protrusion pad PAD_P contacts the base PAD_B **may be smaller** than the entire area ... of the base pad PAD_B.” *Id.*, 8:11-22 (emphasis added). So, Kim teaches a protrusion pad PAD_P that is smaller than the conductive layer on which it sits and thus has sides that are offset from the sides of that conductive layer.

193. An example of this is shown in the three-dimensional view provided in Figure 6, which I have reproduced in annotated form below.

194. As shown, the protrusion pad PAD_P (one of which is annotated orange) is situated away from and inside the edges E1 and E2 defining the beginning and end of the base pad PAD_B at the end of the gate electrode 300 (which has been annotated green):

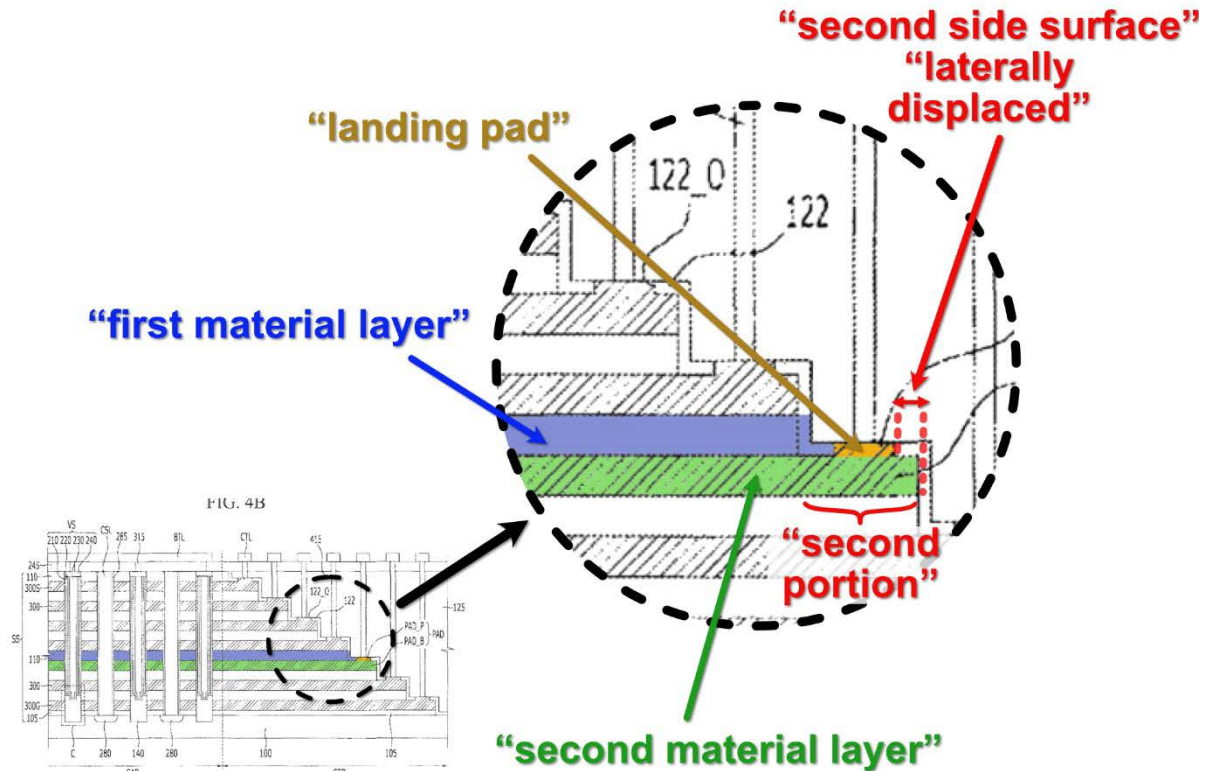
FIG. 6



Kim, Fig. 6 (annotated).

195. Figure 4B, reproduced below with annotations, provides a cross-sectional view.

196. As shown in this figure, because Kim's *"landing pad"* (the protrusion pad PAD_P, annotated orange) is located inside the edges of the underlying *"second portion of the second material layer"* (the base pad PAD_P at the end of electrode 300, annotated green), the landing pad's *"second side surface"* (the pad's rightmost side in the figure) is *"laterally displaced"* from the *"side surface of the second portion of the second material layer"* (the end of electrode 300):



Kim, Fig. 4B (annotated).

197. I recognize that in Figure 8 of the '838 patent, the depicted landing pad overhangs an underlying conductive layer. *See* Ex. 1001, Fig. 8.

198. In my opinion, a POSITA would have recognized that the claims are not limited to just this arrangement.

199. Claims 1 and 12 provide only that the “landing pad” be “laterally displaced” from the side surface of the underlying layer. The claims do not specify or limit the direction in which this displacement occurs.

200. It follows that the landing pad can either be displaced inward and back from the edge of the underlying conductive layer such that it is offset from that

conductive layer (like Kim’s landing pads) or displaced outward and away from the edge of the conductive layer such that it overhangs that conductive layer (like the example landing pads shown in Figure 8 of the ’838 patent).

201. Consistent with the claim language itself, the ’838 patent explains that the term “lateral/laterally” simply means “nominally parallel to a lateral surface of a substrate.” Ex. 1001, 5:6-8.

202. So, when the claim requires a “second side surface” that is “laterally displaced,” it is referring to displacement in any direction parallel to the substrate surface. It does not matter which direction this displacement occurs in, so long as the displacement is in the plane parallel to the substrate (so, for instance, in the context of Figure 4B of Kim, displacement either to the right or to the left of the figure qualifies as the claimed “lateral[] displace[ment]”).

2. Claim 4

203. Claim 4 depends on Claim 1 and further requires:

[4] “wherein the landing pad comprises a conductive material.”

204. This, in my opinion, is taught by Kim.

205. Kim explains that its “gate electrode 300” along with the attached “base pad PAD_B and ... protrusion PAD_P”—the latter of which is the claimed “***landing pad***”—can all be formed from the same “common material composition” such as a “metal.” Kim, 6:31-35, 14:12-17.

3. Claim 5

206. Claim 5 depends on Claim 4 and further requires:

[5] “wherein the conductive material comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof.”

207. This, in my opinion, is also taught by Kim.

208. Kim provides a list of example conductive materials that can be used to form its gate electrodes 300, base pads PAD_D, and protrusion pads PAD_P.

209. These materials include “metal (for example tungsten, copper, and aluminum), metal nitride ..., or a combination thereof.” Kim, 6:31-35.

4. Claims 6 and 20

210. Claim 6 depends on Claim 1. Claim 20 depends on Claim 12. Both Claims further require:

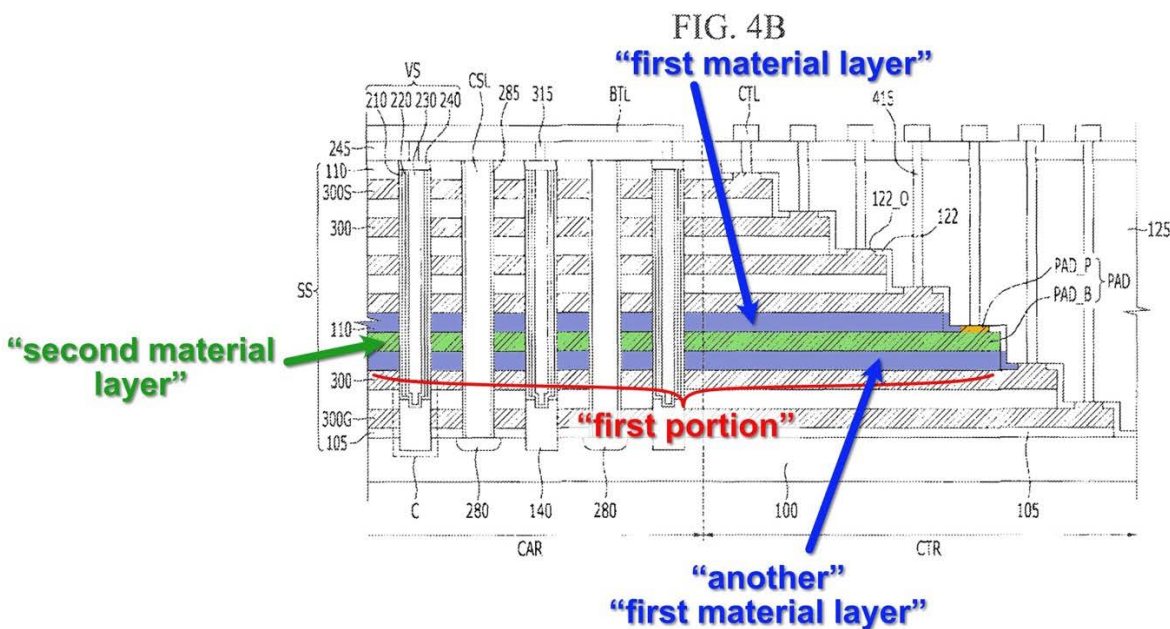
[6]/[20] “wherein the second material layer is disposed over a first portion of another first material layer, and wherein a side surface of a second portion of the another first material layer is laterally displaced from the second side surface of the landing pad.”

211. In my opinion, Kim teaches what these claims require.

212. Kim’s “stacking structure SS” includes a “plurality” of alternating “insulating layers 110 and ... gate electrodes 300.” Kim, 5:53-55; *see also id.*, 1:41-46 (the “stacking structure” includes “insulating layers” and “gate electrodes” that are “alternatively stacked.”)

213. Figure 4B is reproduced below (again in annotated form). As shown, because Kim’s stacked, staircase structure includes alternating conductive and

insulating layers, Kim’s ***“second material layer”*** (the gate electrode 300, annotated) is located over ***“a first portion of another first material layer”*** (the insulating layer 110 immediately below the gate electrode):

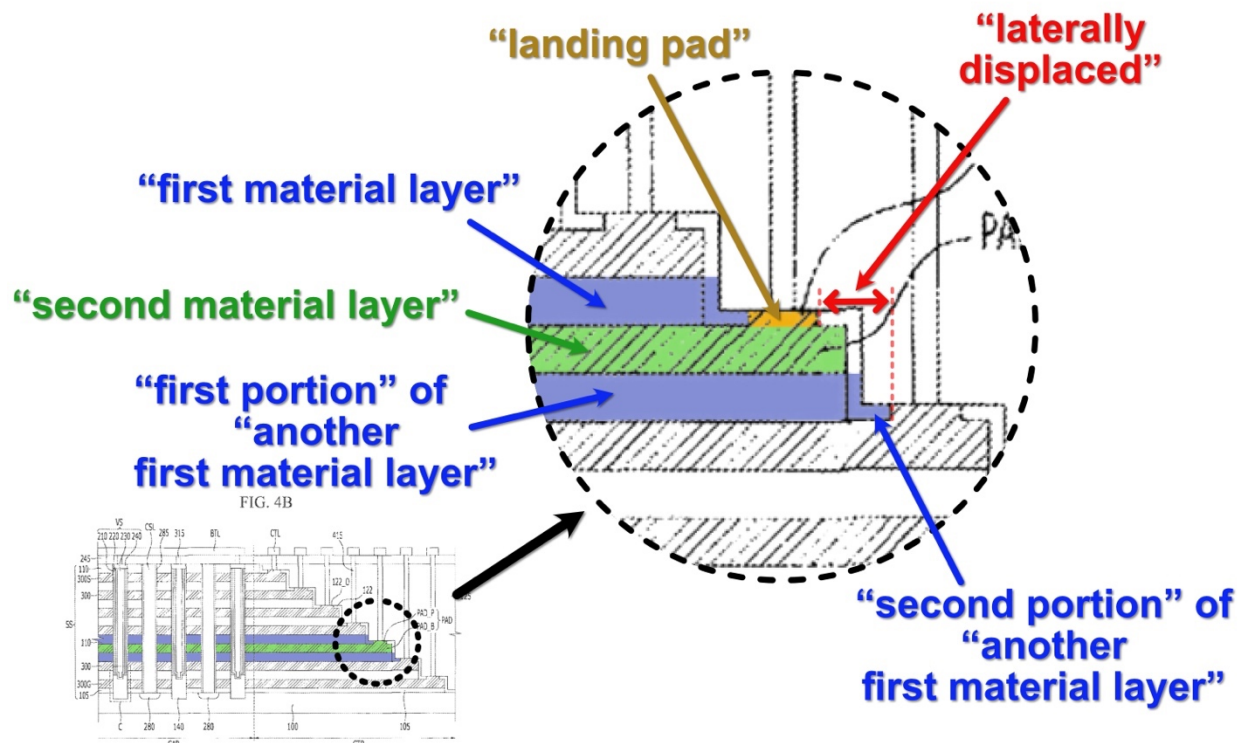


Kim, Fig. 4B (annotated).

214. Further, as I have explained above, each insulating layer 110 can be integrated with an “auxiliary insulating layer 122” such that layers 110 and 122 form “one structure.” Kim, 9:12-13, 9:29-38.

215. As shown in the annotated version of Figure 4B of Kim below, because Kim’s structure is formed as a staircase with lower steps extending out further than upper steps, and because each of its insulating layers include both layer 110 and layer 122, a ***“a side surface of a second portion of the another first material layer”*** (the portion of auxiliary insulating layer 122 adjacent to layer 110) is ***“laterally***

displaced from the second side surface of the landing pad” (the side of the pad portion PAD_P located on the upper gate electrode 300). In other words, the lower insulation layer extends beyond the edge of the conductive layer above it:



Kim, Fig. 4B (annotated).

5. Claims 7 and 17

216. Claim 7 depends on Claim 1. Claim 17 depends on Claim 12. Both claims further require:

[7]/[17] “wherein the second material layer comprises a first conductive material and the landing pad comprises a second conductive material substantially the same as the first conductive material.”

217. This, in my opinion, is taught by Kim.

218. As I explained when discussing Claim 4 above, Kim’s “gate electrode 300,” “base pad PAD_B and ... protrusion PAD_P” may all be formed from the same “common material composition” such as a “metal.” Kim, 6:31-35, 14:12-17.

219. Once again, Kim’s “gate electrode” is the claimed “*second material layer*” while its protrusion pad PAD_P is the “*landing pad*.” Both of these are made from “*substantially the same*” “*conductive material*”: metal.

6. Claim 13

220. Claim 13 depends on Claim 12 and further requires:

[13] “wherein the first side surface comprises a curved side surface.”

221. This, in my opinion, would have been obvious in view of Kim.

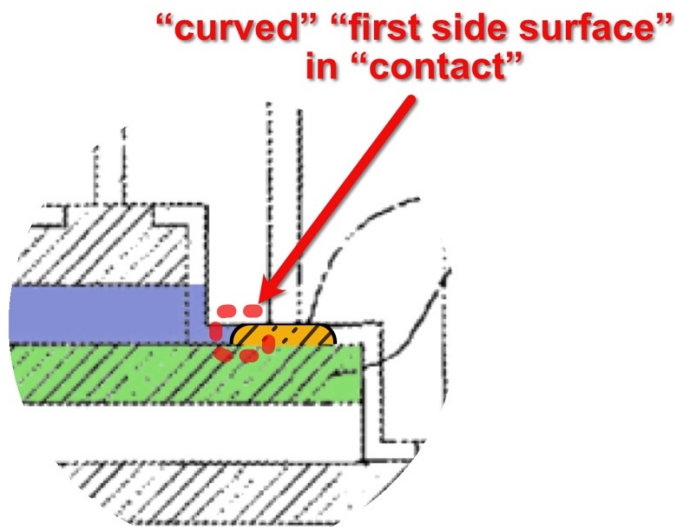
222. Kim teaches that the “*first side surface*” of its “*landing pad*” that is in “*contact*” with its “*first material layer*” is (or at the very least obviously can be) “*curved*.”

223. Kim explains that while its figures show “[e]mbodiments ... in which the protrusion pad PAD_P has a rectangular parallel[] shape[,]” “the protrusion pad PAD_P is not limited thereto and ... may have a shape including a curved surface based on a virtual rectangular parallel[] shape, a cylindrical shape, or any shape.” Kim, 8:29-34. A POSITA would have recognized that this includes configurations where the sides of the protrusion pads are curved, particularly to optimize electrical connectivity and mitigate stress at material interfaces. Such curved configurations

are routine in the fabrication of three-dimensional memory devices, as further supported by references like Park, Yun, and Nam. A POSITA also would have recognized that pads with rounded sides can be more readily manufactured than a pad with perfectly straight sides. As discussed below, ion implantation was often employed when forming contact pads. And the species implanted during this process tend to diffuse resulting in curved rather than straight contact pad sides even when straight sides are intended.

224. In my opinion, a POSITA would have understood that this teaches a variety of different protrusion pad PAD_P shapes, many of which have the type of “*curved*” side surface Claim 13 requires. This includes, for instance, pads with curved sides when viewed in cross-section or pads with curved sides when viewed above.

225. More particularly, a POSITA would have understood that when Kim references a “curved surface based on a virtual rectangular parallel[] shape,” PAD_P would obviously be shaped in the manner shown in the demonstrative below. This demonstrative was created using an expanded version of Figure 4B. The rectangular pad shown by that figure has been replaced with a pad with curved sides following Kim’s teachings:



As shown in the demonstrative, the pad continues to have a generally rectangular shape. It also continues to sit on top of Kim’s gate electrode layer. Moreover, it continues to be located in the opening in auxiliary insulation layer 122. But now, the pad’s sides are “curved” in the area where they contact auxiliary insulation layer 122. *See Kim, 8:29-34* (explaining that the protrusion pad can have a “curved” surface).

226. In my opinion, not only does Kim itself explain that its pad can have a “curved surface,” but contact pads with this type of “curved” side surfaces were well-known in the art at the time the ’838 patent was filed. Example references showing this include (1) Park (Ex. 1009), (2) Yun (Ex. 1021), and (e) Nam (Ex. 1022). Each of these will be discussed in greater detail below.

227. Park (Ex. 1009) teaches a “vertical semiconductor device” with an array of “stacked” “memory cells.” Park, 1:14-19.

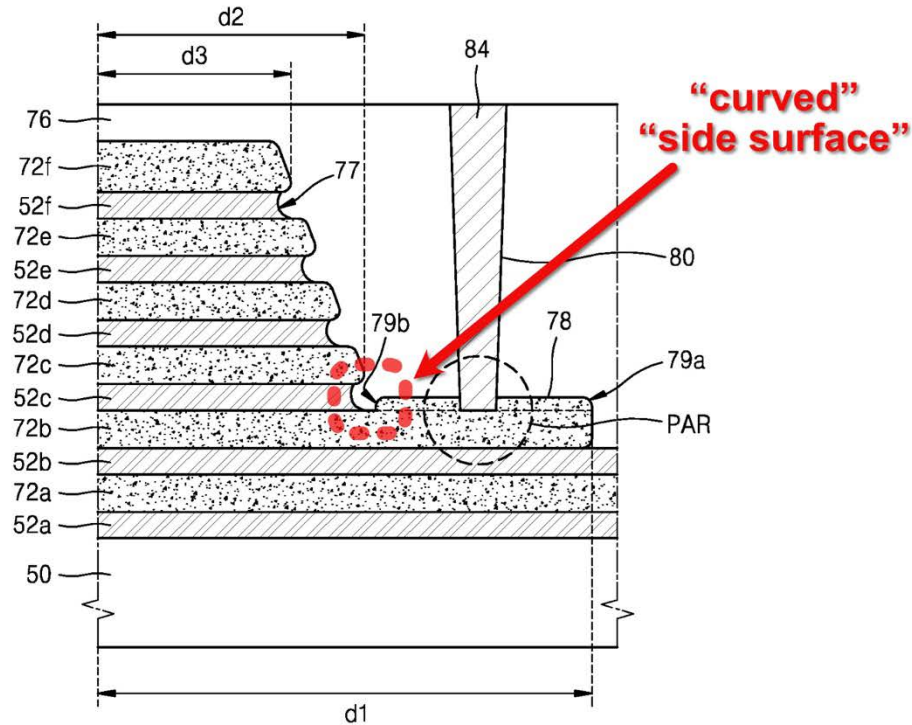
228. Park's device—like Kim's and most references teaching three-dimensional memory—includes a stepped “connection region” with “pad region[s] PAR” located on the end of gate electrodes. Park, 6:7-11, 6:36-47.

229. Each “pad region PAR” includes a “raised pad portion” 78. Park, 7:4-16.

230. Per Park, the “end 79b” of the “raised pad portion” 78 may be “rounded” to “prevent a short circuit” between the pad and an “adjacent ... conductive layer pattern 72c.” Park, 11:35-41. An example pad with a rounded end is shown in Figure 7 from Park, which is reproduced below:

FIG. 7

400



Id., Fig. 7 (annotated).

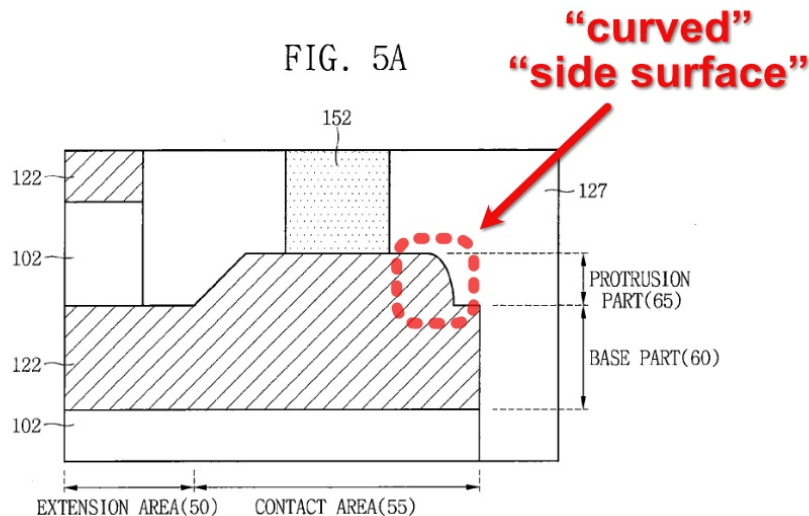
231. Yun (Ex. 1021) also relates to a “semiconductor device[] having three-dimensionally arranged memory cells...” Yun, 1:33-35.

232. Yun explains that the device, once again like most three-dimensional memory devices, has a “stepped” or “cascade structure.” Yun, 9:22-25.

233. The steps hold “contact area[s] 55” that are “co-planar with” the device’s “gate electrodes” and have both a “base part 60 and a protrusion part 65.” Yun, 8:11-20.

234. Per Yun, the “protrusion part 65” may have either “inclined” or “rounded” “side surface[s].” Yun, 8:33-40.

235. An example of this is shown in Figure 5A of Yun which is reproduced below. The “rounded” surface shown on the right side of the contact pad:



Yun, Fig. 5A (annotated).

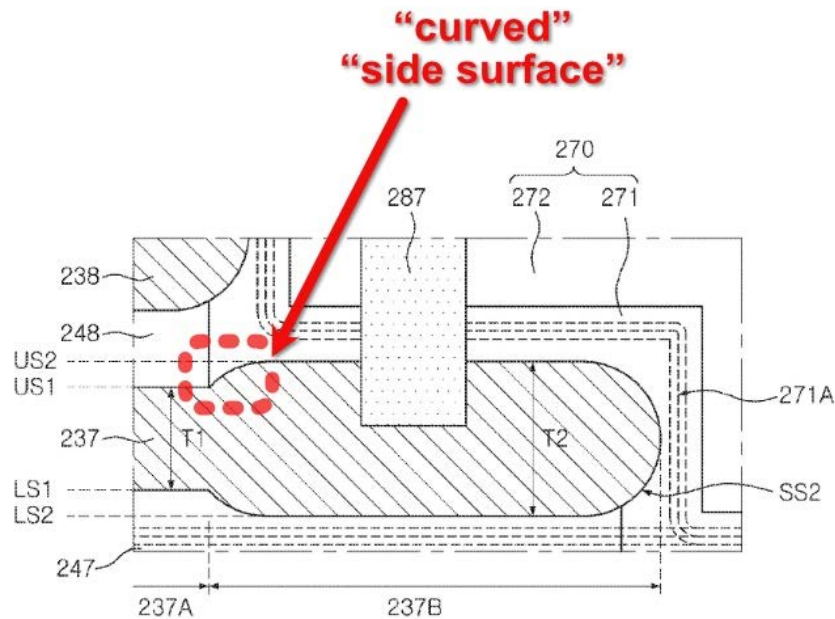
236. Nam (Ex. 1022) provides another example.

237. Nam—like the Kim, Park, and Yun references I have discussed above—teaches a “semiconductor device” formed from memory cell strings arranged in a three-dimensional array. *See* Nam, ¶¶ [0005], [0025], [0033]; Fig. 2.

238. Gate electrodes connecting to the memory cells may “have a stepped shape having step structures.” Nam, ¶ [0043]. Layers of insulation are located between the gate electrodes. *Id.*

239. Nam explains that each gate electrode includes a “pad region” at its end where “the gate electrode ... is connected to a contact 187.” Nam, ¶ [0057].

240. As shown below in Figure 8A from Nam, the “pad region” at the end of each gate electrode can have a “bull nose” or “convex” shape. Nam, ¶ [0066].



Id., Fig. 8A (annotated).

241. In my opinion, a POSITA would have been motivated to employ a contact pad with curved side surfaces when implementing Kim.

242. As I have explained, Kim itself already contemplates that its pad can have a “curved surface.” Kim, 8:29-34.

243. Moreover, this type of pad was also well known in the art as shown not only by Kim, but also by Park, Yun, and Nam. *See, e.g.*, Park, Fig. 7; Yun, Fig. 5A; Nam, Fig. 8A.

244. Because Kim itself identifies contact pads with curved surfaces as acceptable for use with its device, and because contact pads with this shape were well-known in the art, contact pads with curved side surfaces would have been among the available design choices a POSITA would have considered for use when implementing Kim. Employing this shape would have been considered a highly obvious and routine design choice.

245. Additionally, a POSITA would have recognized that using a “*curved*” side surface with Kim’s pads would have improved Kim by increasing the minimum distance between the pad and adjacent conductive layers, thereby reducing the risk of short circuit.

246. Again, Park explains that “rounded” pad side surfaces helps “prevent a short circuit” between the pad and an “adjacent ... conductive layer pattern.” Park, 11:35-41. A POSITA would have recognized that forming Kim’s pads with straight (or square) sides would have increased the possibility of short circuit with adjacent conductive layers. While also problem for equally sized pads like those shown in Figure 4B, this would have been particularly the case when Kim’s pads are made with larger widths causing the pad to occupy a larger percentage of the exposed

portion of each step in its staircase structure. *See, e.g.,* Kim, 11:57-67 (explaining that certain pads can have a “larger ... width”); Fig. 9 (showing larger protrusion pad portions near the top of Kim’s stacking structure).

247. In my opinion, the decreased risk of short circuit resulting from the use of rounded pads would have provided a strong motivation to use such a pad with Kim.

248. A POSITA would also have had every reason to believe that a curved pad could be successfully used with Kim.

249. Again, as I have explained, this is one of the shapes that Kim already contemplates and deems acceptable. *See* Kim, 8:29-34.

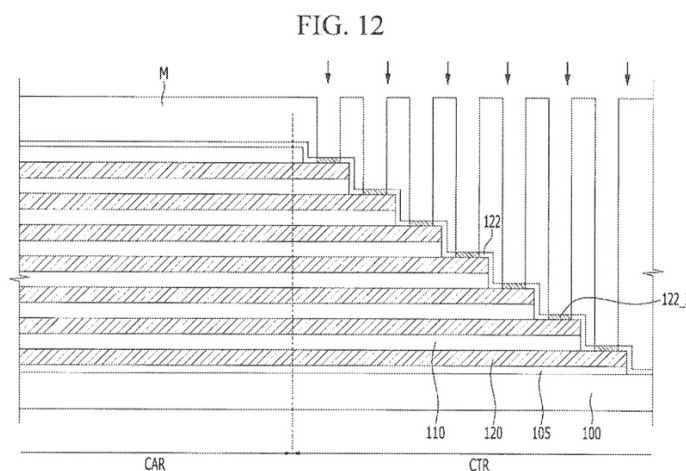
250. Further, as I have also explained, contact pads with curved side surfaces had also been successfully used in other semiconductor memory devices with stepped structures. *See, e.g.,* Park, Fig. 8; Yun, Fig. 5A.

251. Given both the fact that Kim identifies curved pads as acceptable and others similarly taught that pads of this shape can (and had) been used with three-dimensional memory devices, a POSITA would have had every reason to believe that Kim’s device would also be able to successfully employ pads of this shape. Furthermore, a POSITA would have found Park’s approach for forming such a pad to be highly applicable because it does not introduce new steps but instead optimizes

an existing manufacturing process to achieve improved reliability and performance in Kim's three-dimensional memory devices

252. Moreover, Kim explains that the opening in auxiliary insulation layer 122 that will eventually contain its protrusion pad PAD_P obtains its shape via an “ion injection process.” Kim, 13:1-11.

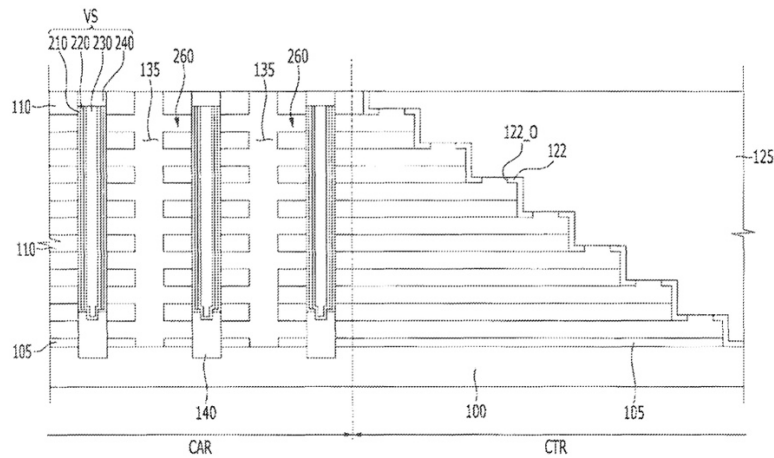
253. More particularly, in Kim, ion injection is used to form an appropriately shaped “doped region 122_I” in insulating layer 122. *See* Kim, 13:1-11. This is shown in Figure 12 below:



Id., Fig. 12.

254. This doped region is then etched away to form “opening 122_O” “simultaneously with the process of removing the sacrificial layer 120” which forms “gaps 260.” Kim, 13:55-14:8. The formed openings are shown in Figure 16 of Kim:

FIG. 16



Id., Fig. 16.

255. Then both the gaps 260 and openings 122_O are filled with conductive material to form the gate electrodes and pads. *See Kim, 14:9-17; see also Figs. 12-16.*

256. In my opinion, a POSITA would have recognized that this process could be readily adapted to form a curved opening that surrounds a curved contact pad. In particular, the ion implantation step shown in Figure 12 of Kim would simply be tailored to form a “doped region 122_I” with curved rather than straight sides. The rest of the process would proceed in the same way, resulting on contact pads located within an opening 122_O in insulation layer 122 with curved sides.

257. Showing this, numerous prior art references similarly employ ion implantation to form contact pads with rounded or curved sides using a process that is analogous to that in Kim.

258. For example, Park details how “oxidation” and “ion implantation” is used form a “raised pad portion” with “rounded” sides. *See, e.g.*, Park, 7:17-29. In particular, “an additional sacrificial layer 44” with the desired rounded shape is formed via “oxidation” by “ion implanting impurities into” an “additional insulating layer 40.” *Id.*, 8:34-49. Implanting the impurities creases a region “having a higher etching rate than” the surrounding “additional insulating layer 40” allowing this region to be removed and later replaced with a properly shaped conductive contact pad. *Id.*, 8:49-51, 9:3-11; Figs. 6D-6F.

259. Nam similarly discusses and depicts the use of “an ion implantation process” to form a “convex” contact pad. Nam, ¶¶ [0066], [0098]-[0107]; Figs. 30-39. In Nam, an “ion implantation process” is employed to form an appropriately shaped “damage region BA1” within insulating layers 272 surrounding sacrificial layers 220. *Id.*, ¶¶ [0099]-[0100]. The shape of the eventual contact pad can be controlled via the use of multiple ion-injection steps targeting different areas. *See, e.g., id.*, ¶¶ [0060], [0066], [0073]; Figs. 22, 32-34. The damaged regions have a “relatively rapid etching rate” resulting in the formation of an opening in the surrounding insulation corresponding to the contact pad. *Id.*, ¶¶ [0103]-[0104]. This opening is then replaced with conductive material. *Id.*, ¶¶ [0106]-[0107].

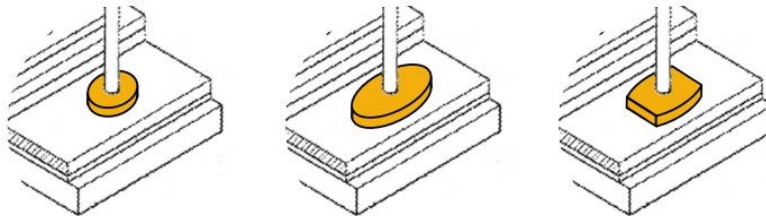
260. Again, a POSITA would have understood that ion implantation would similarly be employed to form a “doped region 122_I” in Kim’s auxiliary insulation

layer 122 with a rounded as opposed to rectangular shape. When this region is then etched to form an opening 122_O and replaced with conductive material as Kim teaches, a contact pad with rounded sides (that continue to be surrounded by and in contact with insulation) results. Alternatively, an opening with straight sides could be subjected to a further oxidation step like that taught by Park to achieve the desired rounding. The amount of rounding would be controlled by adjusting the time of application of the oxidant to the opening (the oxidant will remove exposed corners first, producing the desired rounding before it meaningfully impacts the other surfaces within the opening).

261. Next, in my opinion, a POSITA would have understood that Kim's "cylindrical[ly]"-shaped protrusion pads PAD_P also include the type of "*curved*" surface that Claim 13 requires.

262. A POSITA would have understood that a "cylindrical" contact pad can be implemented as, for instance, a right cylinder, an elliptical cylinder, or even a generally rectangular pad with two sides that follow a cylindrical pattern. While all these types of pad shapes include "curved" side surfaces, a POSITA would have understood that a generally rectangular pad with two flat sides and two sides following a cylindrical pattern is yet another way a POSITA would have considered implementing Kim's teaching that its pad can have a "curved surface based on a virtual rectangular parallel[] shape...." Kim, 8:29-34.

263. Examples of how a POSITA would have understood these pads to be shaped are shown in the demonstrative images below. Note that Kim does not include any figures showing “cylindrical” contact pads. Nonetheless, it does reference this type of pad. The below examples of what a POSITA would have understood Kim to mean when it references a “cylindrical” pad were generated using the three-dimensional view of Figure 6 as a starting point. Figure 6 shows rectangular pads. The rectangular pads in that figure have been replaced with (1) a right cylinder (left-most demonstrative), (2) elliptical cylinder (central figure), and (3) rectangular pad with two straight sides and two tides following an elliptical cylindrical shape:



264. In my opinion, employing any of these “cylindrical” contact pads also results the claimed “*landing pad*” having a “*curved*” “*first side surface*” that is in “*contact*” with Kim’s “*first material layer*.”

265. This is shown in the demonstrative below generated using Figure 6 of Kim. Again, in Figure 6, the contact pads are shown to be rectangular. In the demonstrative below, there is an expanded view—the bottom left of the demonstrative—of one such rectangular pad replaced with a pad that has two straight

267. In my opinion, a POSITA also would have been motivated to employ this shape and would have expected to succeed when doing so.

268. As I have explained, Kim itself identifies “cylindrical”-shaped contact pads as acceptable and contemplates their use.

269. Because of this, a POSITA would have considered use of cylindrical pads to be nothing more than a minor variation in design from the rectangular pads shown in Kim’s figures. Use of this shape pad—as opposed to any of the others taught by Kim—would have been a simple, straightforward design choice.

270. Further, a POSITA would have recognized that a cylindrical pad could be made following the same process and same steps Kim employs to make its rectangular pad (just with differently shaped mask patterns during the ion implantation process shown in Figure 12 to produce a cylindrical rather than rectangular pad). Thus, a POSITA would have every reason to believe that a cylindrical contact pad would be successfully employed with Kim’s device

7. Claim 14

271. Claim 14 depends on Claim 13 and further requires:

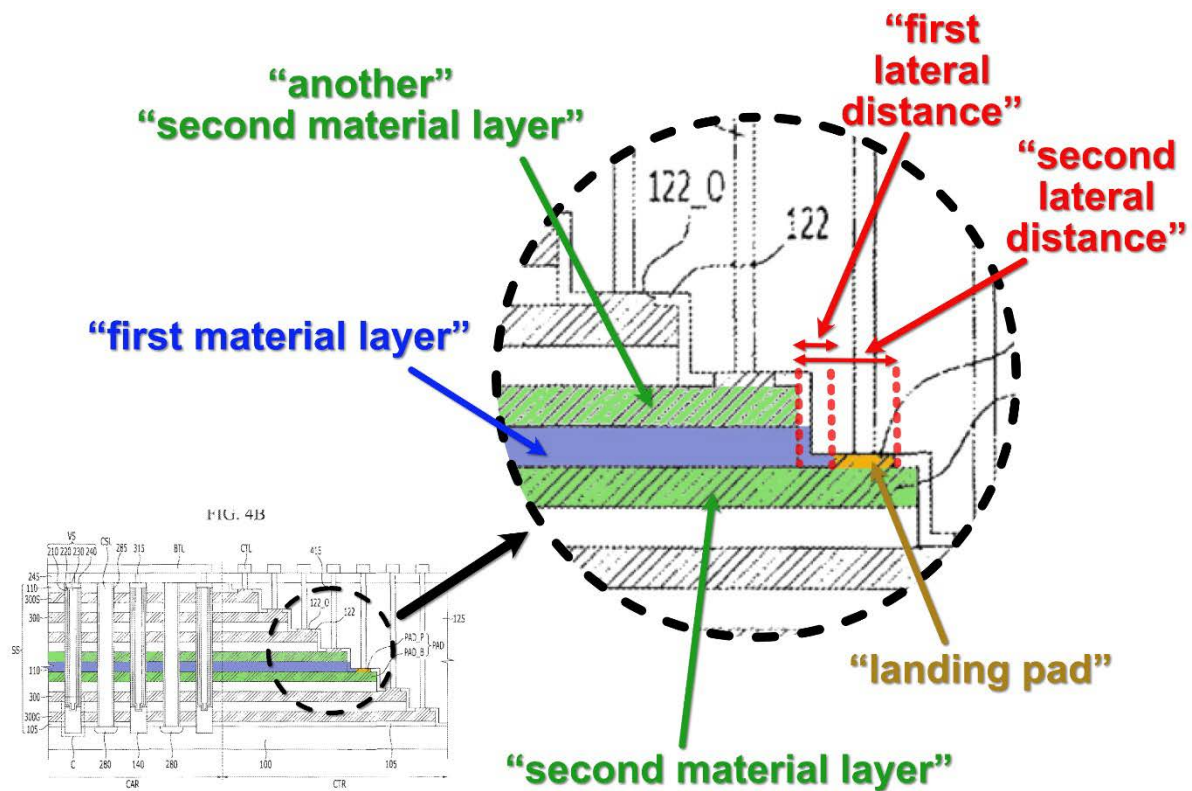
[14] “further comprising another second material layer disposed on the first material layer, wherein a first lateral distance between the first side surface and a side surface of the another second material layer is smaller than a second lateral distance between the second side surface and the side surface of the another second material layer.”

272. This, in my opinion, is taught by Kim.

273. Again, as I have explained, Kim’s “stacking structure SS” includes a “plurality” of alternating “insulating layers 110 and ... gate electrodes 300.” Kim, 5:53-55; *see also id.*, 1:41-46.

274. Because Kim’s device includes alternating conductive and insulating layers, there is **“another second material layer”** (a further gate electrode 300) that is **“disposed on the first material layer”** (the insulation layer 110 discussed in connection with Claims 1 and 12 above).

275. Further, Kim’s device has a “stepwise structure.” Kim, 1:40-47; *see also id.*, 1:15-17. This causes conductive layers higher in the stacking structure to be stepped back from lower layers. Because of this, the **“first lateral distance between the first side surface and a side surface of the another second material layer”** (the distance between a pad’s left side in Figure 4B and the side of the gate electrode in the layer above the pad) is **“smaller”** than **“second lateral distance between the second side surface and the side surface of the another second material layer”** (the distance between the same pad’s right side and the side of the gate electrode in the layer above the pad):



Id., Fig. 4B (annotated).

8. Claim 15

276. Claim 15 depends on Claim 13 and further requires:

[15] “wherein the second side surface is laterally displaced from the first side surface, and wherein a first lateral distance between the first side surface and the first portion of the second material layer is smaller than a second lateral distance between the second side surface and the first portion of the second material layer.”

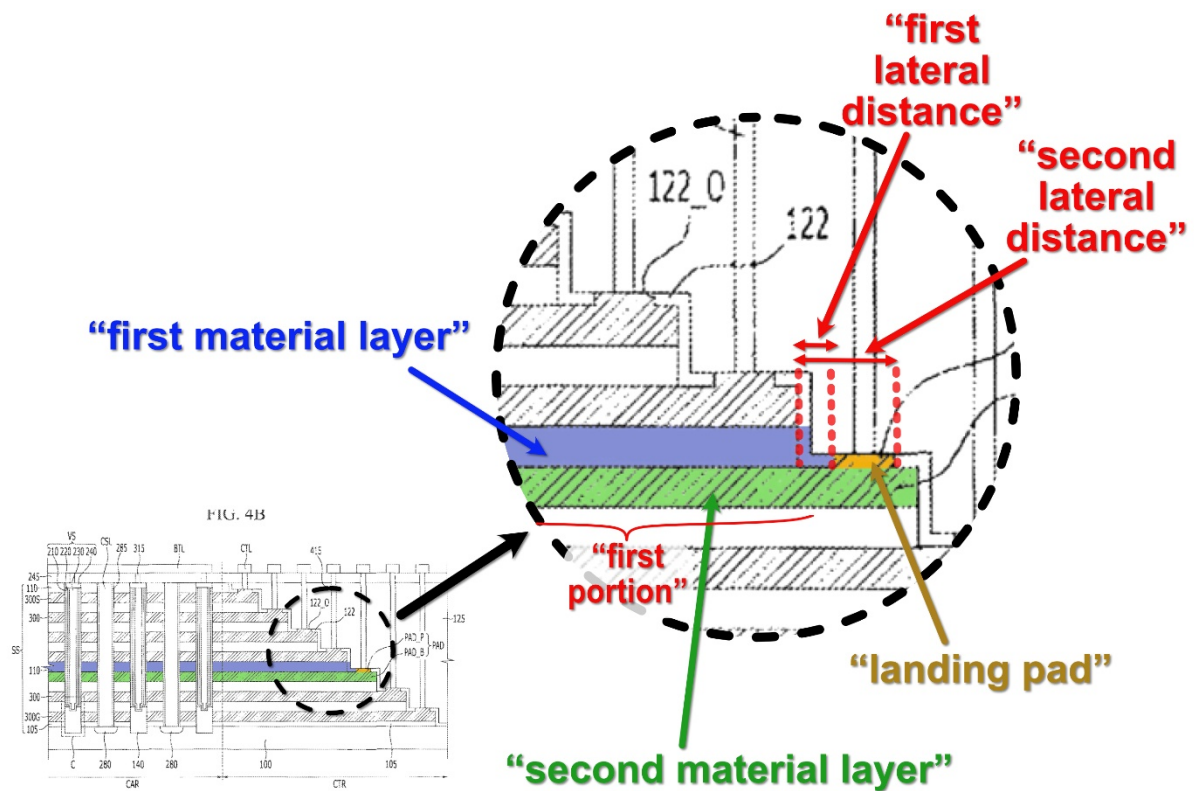
277. In my opinion, a POSITA would have considered what this claim requires obvious in view of Kim.

278. Kim explains that each of its protrusion pad has a “width.” Kim, 11:57-12:7. This can also be seen in each of Kim’s figures: the pads are always depicted as having a width from the left to right of the figure. *See, e.g., id.*, Fig. 4B.

279. Because it has a width, the “*first*” and “*second*” “*side surface[s]*” of the pad are “*laterally displaced*” from each other as this claim requires.

280. Moreover, the pad’s width and location on the underlying gate electrode causes “*a first lateral distance between the first side surface and the first portion of the second material layer*” (the distance between the leftmost edge of the protrusion pad and the gate electrode layer 300 to the left of the base pad) to be “*smaller*” than a “*second lateral distance between the second side surface and the first portion of the second material layer*” (the distance between the rightmost edge of the protrusion pad and the gate electrode layer 300 to the left of the base pad).

281. This is shown in the below annotated version of Figure 4B. Again, a portion of the figure has been expanded to better show how Kim teaches the “*lateral distance[s]*” required by this claim:



Kim, Fig. 4B (annotated).

9. Claim 16

282. Claim 16 depends on Claim 12 and further requires:

[16] “wherein the second material layer comprises tungsten, and titanium nitride.”

283. This, in my opinion, is taught by Kim.

284. Among other material options, Kim teaches that its gate electrodes 300 can be formed from “combination[s]” of materials including “metal” like “tungsten” and “metal nitride” such as “nitride titanium.” Kim, 6:31-35.

10. Claim 19

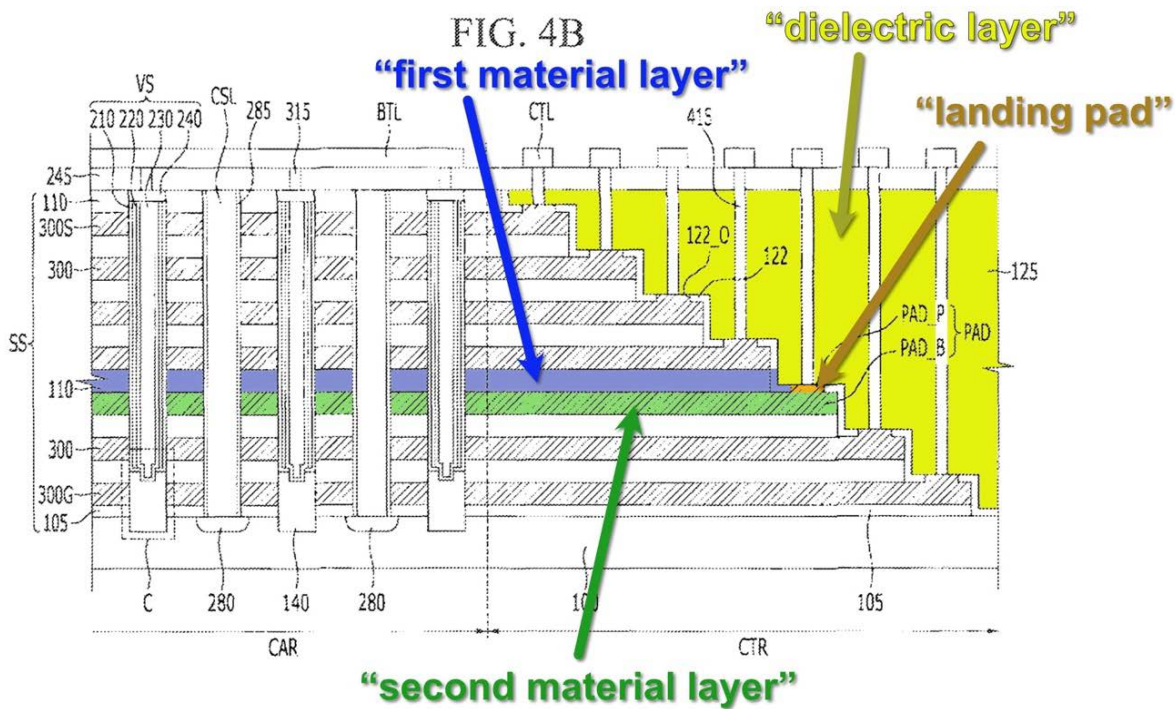
285. Claim 19 depends on Claim 12 and further requires:

[19] “a dielectric layer disposed over the first material layer and the landing pad, wherein the first material layer comprises a first dielectric material and the dielectric layer comprises a second dielectric material, wherein the first dielectric material is substantially the same as the second dielectric material, and wherein the first dielectric material comprises silicon oxide.”

286. In my opinion, Kim teaches a device that includes the claimed *“dielectric layer disposed over the first material layer and the landing pad.”*

287. Figure 4B is again reproduced below in annotated form.

288. As shown in this figure, Kim’s device includes a “buried insulating layer 125.” Kim, 9:56-57. This layer is formed over the “auxiliary insulating layer.” *Id.*, 13:12-20. This layer 125—which is annotated yellow and is Kim’s *“dielectric layer”*—is located over both the *“first material layer”* (the insulating layers 110 and 122, annotated blue) and the *“landing pad”* (the protrusion pad PAD_P, annotated orange):



Id., Fig. 4B (annotated).

289. Kim also explains that its “insulating layer 125” is formed from an “insulating material.” Kim, 13:15-17. This insulating material can be an “oxide layer.” *Id.*, 9:61-67.

290. Kim’s “insulating layer 110” and “auxiliary insulating layer 122” are also formed from an “oxide layer.” Kim, 9:29-31.

291. Kim further explains that in its device, the oxide layers can be “silicon oxide.” Kim, 12:26-29.

292. Thus, in my opinion, a POSITA would have understood (or at least considered it obvious) that Kim’s “*dielectric layer*” (layer 125) and “*first dielectric*

material” (layers 110 and 122) are formed from “*substantially the same*” material: “*silicon oxide.*”

C. **Ground 2: Claims 3 and 18 Are Obvious Over Kim and Yang**

293. In my opinion, a POSITA would have considered Kim and Yang to both be within the scope of the prior art and highly relevant to the patentability of the '838 patent's claims.

294. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Kim and Yang together render Claims 3 and 18 of the '838 patent obvious.

295. Claim 3 depends on Claim 1. Claim 18 depends on Claim 12. Both Claims further require:

[3]/[18] “wherein a lateral distance between the second side surface and the side surface of the second portion of the second material layer is between 10 nm and 300 nm.”

296. Again, in my opinion, a POSITA would have considered this claim obvious when Kim is considered in view of the knowledge of a POSITA (as shown by Yang).

297. As I explained above when discussing Ground 1, Kim teaches a three-dimensional memory device with “*landing pads*” (Kim's protrusion pad portions PAD_P) that are located within the bounds of and “*laterally displaced*” from the sides of a lower “*second material layer*” (Kim's gate electrode 300 and base pad

portion PAD_B) by a “*lateral distance.*” See *supra* discussion of Kim and limitation [1.B.2].

298. Kim does not provide a numerical example quantifying the distance between the side of its landing pad and the side of the conductive layer below it.

299. Regardless, in my opinion, a POSITA would have considered it obvious to employ a value falling within the range required by these claims: “*10 nm and 300 nm.*”

300. Yang (Ex. 1007) exemplifies this.

301. As explained in detail below, a POSITA would have understood that Kim’s device would have dimensions like those referenced in Yang due to these references’ shared purpose, structural similarities, and the predictability of applying Yang’s dimensions to Kim’s device. Both Kim and Yang aim to prevent electrical failures caused by over-etching during the manufacturing of 3D memory devices. Kim teaches protrusion pads (PAD_P) offset from the edges of lower conductive layers to improve reliability, while Yang provides specific pad dimensions that achieve the same goal by mitigating over-etching. Yang’s stair-step structure with pads embedded within each step closely resembles Kim’s structure, making Yang’s teachings directly applicable. A POSITA would view Yang’s offsets as reliable and predictable design choices that could naturally be applied to Kim’s device to ensure

stability. Additionally, both references emphasize reliability and manufacturability, confirming their compatibility.

302. Yang, like Kim, relates to “a pad structure applied to a three-dimensional (3D) memory device and a manufacturing method of the pad structure.” Yang, 1:6-10.

303. Yang’s device includes both an “array region” and a “pad region.” Yang, 4:32-39.

304. Figure 2 provides a “cross-sectional view” of the “pad region.” Yang, 4:43-48.

305. A POSITA would have recognized that Yang’s “pad region” is structurally analogous to Kim’s stepped stacking structure: it includes a stack of “material pairs 132” with a “stair step structure” located over a “substrate 100.” Yang, 4:32-36, 4:43-48. The material pairs are alternating “conductive layers” 114 and “dielectric layer[s]” 106. *Id.*, 4:56-65. Each conductive layer includes a “pad 120” at its end that allows for electrical connection to a contact “plug[] 124.” *Id.*, 4:43-51.

306. Further, as shown in Figure 2 from Yang below, like Kim’s protrusion pads PAD_P, Yang’s pads 120 are situated and sized such that they are offset from the edges of and located within the bounds of the conductive layer on which they sit. The pads are located approximately in middle of each step of the staircase structure:

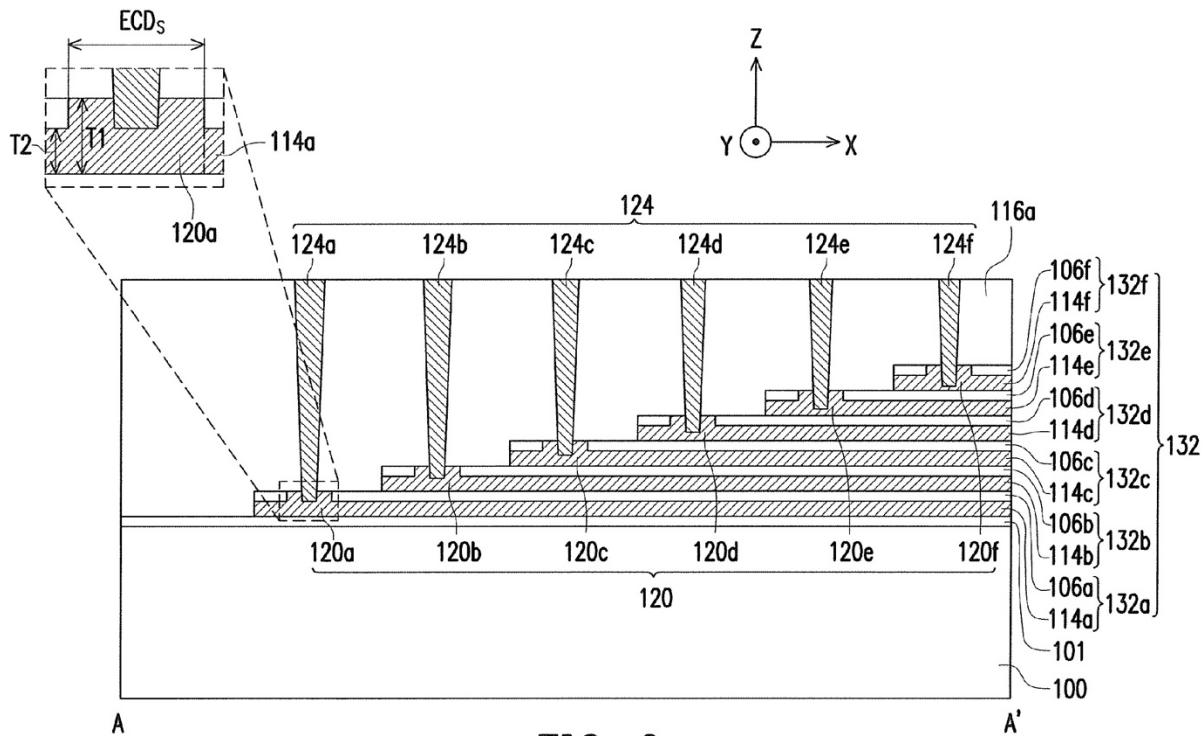


FIG. 2

Yang, Fig. 2.

307. Yang goes on to teach that its pads 120 are dimensioned to avoid “electrical failures caused by over-etching during a process of manufacturing contact openings.” Yang, 1:44-47; *see also id.*, 3:41-47; 5:45-58.

308. Yang provides example dimensions for the various components making up its device that are intended to provide this benefit.

309. According to Yang, each of the conductive layers 114 has a thickness in the range of “20 nm to 40 nm.” Yang, 6:7-28. The insulating layers 106 have thicknesses in the range of “40 nm to 60 nm.” *Id.* The portion of the conductive layer where the contact pad sits has an increased thickness of “70 nm to 90 nm.” *Id.*, 5:54-58.

310. Each of steps in Yang's staircase structure can be "400 nm to 600 nm" long. Yang, 7:22-65. Yang refers to this as either the distance D1 or D2 (both of which are employed during step formation). *Id.*; *see also id.*, Figs. 3E-3H.

311. Yang also explains that its contact pads have a "width ECDs" that "is greater than the sum of the width ECDc of the contact openings 122" connecting to the pads and "two specification values S (i.e., $ECDs > ECDc + 2S$)."

Yang, 10:7-21. Yang provides an example where the contact opening is formed using a "193 nm-ArF excimer laser stepper" with a "specification value S ... in a range of 10 nm to 20 nm, for instance." *Id.*, 10:17-21. In other words, in this example, ECDc would be 193 nm (or ~200 nm), and S would be in the range of 10-20 nm. This in turn means that ECDs (the size of the contact pad) is greater than either 200 nm + 20 nm or 200 + 40 nm, or a value in the range of ~220-240 nm.

312. Given these dimensions, a POSITA would have recognized that if the pads are located approximately in the middle of each staircase step, Yang's pad will be set back from the edge of the underlying conductive layer 114 by ~80-190 nm. This range can be determined as follows: the staircase step has a length of 400-600 nm. The contact pad has a width of 220-240 nm. The maximum amount of uncovered step space would be 600 nm – 220 nm, or 380 nm. When the contact pad is located in the middle of the step, there will be 190 nm of space between the pad and the step edges. The minimum amount of uncovered step space would be 400

nm – 240 nm, or 160 nm. When the contact pad is located in the middle of the step, there will be 80 nm of space between the pad and the step edges.

313. A POSITA would also have understood that Yang also contemplates placing the pads closer to the step edge.

314. But, as shown in Figure 2, when doing so the space between the pad edge and the end of underlying conductive layer still correspond to at least the minimum thickness of the conductive and insulating layers. *See* Yang, Fig. 2.

315. Thus, a POSITA would have understood that Yang's pads would be set back by at least 20nm (the minimum layer thickness contemplated by Yang).

316. Thus, the total range of pad offsets from the step edge contemplated by Yang would have been 20-190nm.

317. The below annotated version of Figure 2 from Yang shows all these various dimensions discussed above.

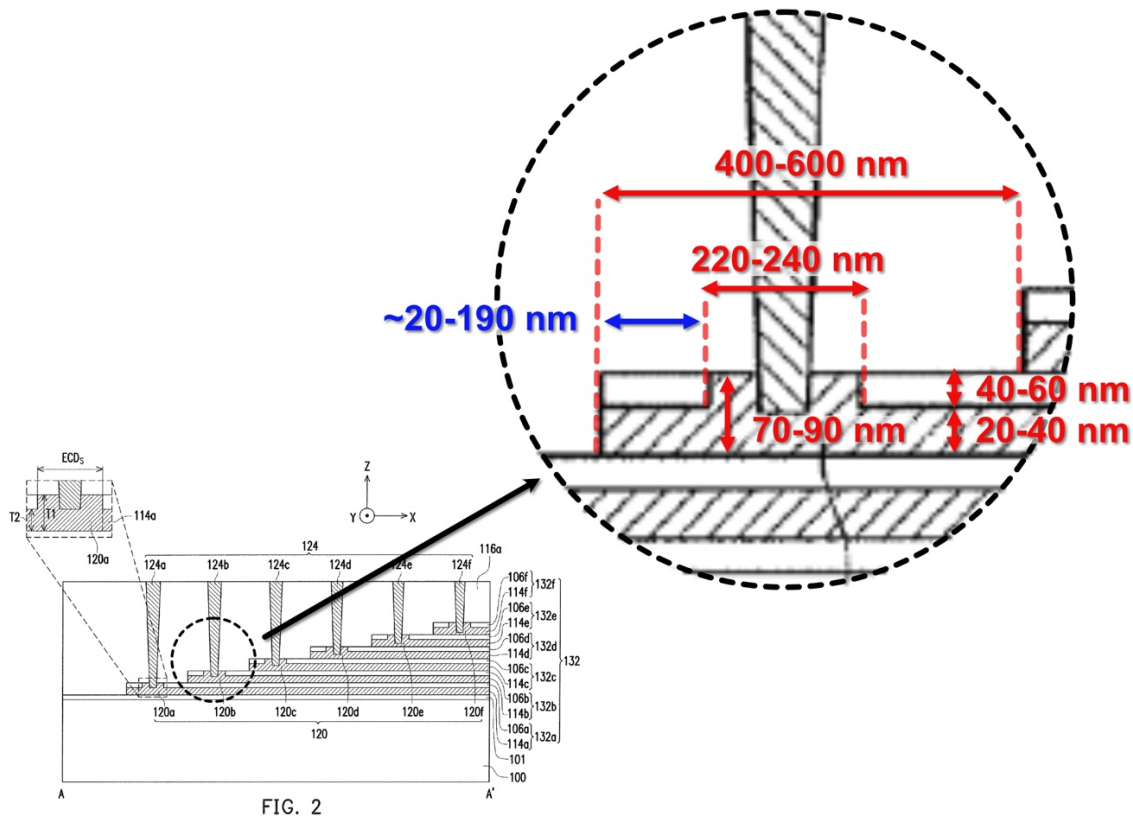


FIG. 2

Yang, Fig. 2 (annotated).

318. In my opinion, applying these example dimensions to Kim results in the claimed subject matter. This is shown in the annotated version of Figure 4B from Kim reproduced below.

319. Kim's protrusion pads would be set back—or "*laterally displaced*" by a "*lateral distance*"—from the edge of the underlying conductive layer by an amount somewhere within the range of 20-190 nm. This is within the range of "*10 nm and 300 nm*" required by Claims 3 and 18:

324. Both Kim and Yang relate to three-dimensional memory devices with a staircase-shaped contact region.

325. Both references also teach that contact pads are located on each step.

326. And in both references, the contact pads are offset from and located within the bounds of an underlying conductive layer in the same way. *Compare* Kim, Fig. 4B with Yang Fig. 2.

327. In my opinion, this similarity in design would have provided a POSITA with a strong motivation to consult Yang when implementing Kim.

328. Moreover, both Kim and Yang explain that their devices are structured to avoid “electrical failures” resulting from “over-etching.” *E.g.*, Yang, 3:39-44; Kim, 9:39-45.

329. In my opinion, this similarity in purpose would also have motivated use of Yang’s example dimensions with Kim.

330. A POSITA would also have considered use of Yang’s example dimensions to be nothing more than a routine, obvious design choice.

331. Kim already contemplates that the width of its contact pads can be adjusted. *See, e.g.*, Kim, 11:57-12:12.

332. Yang simply provides a range of different pad dimensions and offsets that would have been obvious to employ as part of this adjustment process.

333. I also note that when the '838 patent was filed, three-dimensional memory typically included steps having lengths of a few hundred nanometers. And, the layers making up a typical device's stack of conductive and insulating layers typically had thicknesses on the order of a few tens of nanometers. So, the claims here essentially embrace the full range of possible contact pad offsets that a POSITA would have considered workable, including a very small offset (i.e., 10nm) to a very large offset (i.e., 300 nm). A POSITA would have recognized that Kim would also have employed these typical stair and pad dimensions, and thus would obviously employ an offset falling squarely within the middle of the claimed range. Yang simply confirms a POSITA's understanding in this regard: as shown in Yang, a memory device with a pad structure like that in Kim positions its pads back from the underlying conductive layer by an amount somewhere towards the middle of the range required by Claims 3 and 18.

334. In my opinion, a POSITA would also have had a reasonable expectation of success.

335. Again, the similarity and purpose and design between Kim and Yang would have confirmed to a POSITA that the example dimensions set forth in Yang are not only applicable to Kim, but can be successfully employed when implementing Kim's device. Moreover, as the claimed range effectively embraces the full range of possible offsets in a typical memory device, and because the prior

art here teaches offsets within the middle of this range, a POSITA would have every reason to believe that the typical values I identify above could be successfully employed.

D. Ground 3: Claims 1, 4-7, 12, 16-17, and 19-20 Are Obvious Over Lee

336. In my opinion, a POSITA would have considered Lee to be within the scope of the prior art and highly relevant to the patentability of the '838 patent's claims.

337. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Lee renders Claims 1, 4-7, 12, 16-17, and 19-20 of the '838 patent obvious. A POSITA would have recognized that Lee's stepwise patterning and pad structure enable efficient connections in 3D memory devices while minimizing defects such as over-etching or incomplete exposure. The similar structure and function described in Lee provide clear motivation to apply its teachings to achieve the claimed staircase structure.

1. Claims 1 and 12

338. I will again assess Claims 1 and 12 together.

[1.Pre] "A staircase structure of a memory device, comprising:"

[12.Pre] "A memory device comprising":

339. To the extent this preamble language is limiting, in my opinion it is taught by Lee.

340. Lee explains that relates to “semiconductor device[s]” such as “three-dimensional (3D) non-volatile memory devices.” Lee, ¶¶ [0005], [0008]-[0009].

341. Figure 13 of Lee depicts “the configuration of a memory system according to an embodiment of the... invention.” Lee, ¶ [0017].

342. In this example figure, Lee’s “memory system 100” can include “non-volatile memory device 12 and a memory controller 110.” Lee, ¶¶ [0085]-[0090]; Fig. 13.

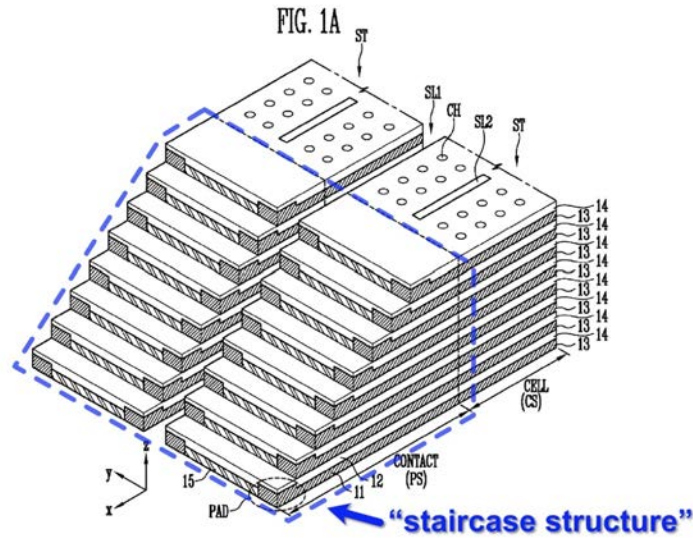
343. Lee also explains that its device includes both a “contact region CONTACT” and a “cell region CELL.” Lee, ¶ [0020].

344. The “cell region” includes the “channel layers CH” along which Lee’s memory cells (and the strings containing those cells) are formed. Lee, ¶ [0026].

345. A “stacked structure ST” formed from “conductive layers 11 and 13 and insulating layers 12 and 14” is located in both the CONTACT and CELL regions. Lee, ¶ [0020].

346. Lee explains that “[a]n end of the stacked structure may be patterned stepwise.” Lee, ¶ [0021]. Likewise, per Lee, “an end of the pad structure is patterned stepwise.” *Id.*, ¶¶ [0009].

347. Figure 1A of Lee is reproduced below. Lee’s “*staircase structure*” (the stepped portion of the CONTACT region) is encircled:



Lee, Fig. 1A (annotated).

[1.A]/[12.A] “a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and”

348. Claims 1 and 12 next require a **“first material layer”** that is **“disposed over a first portion”** of a **“second material layer.”**

349. This, in my opinion, is taught by Lee.

350. Lee’s device includes a “stacked structure ST” that is “patterned stepwise.” Lee, ¶ [0021].

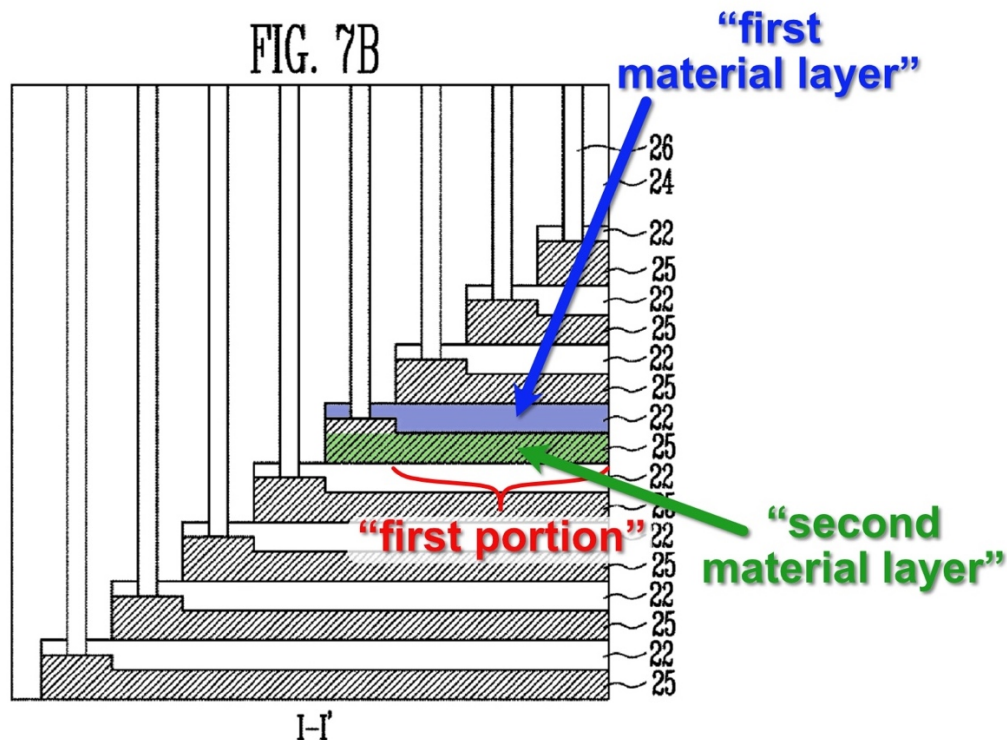
351. The “stacked structure ST” is formed from “conductive layers ... and insulating layers ... that are formed alternately with each other on the substrate.” Lee, ¶ [0021]. “Each step of the stacked structure” includes “at least one conductive layer ... and at least one insulating layer....” *Id.* The “insulating layer” is “located on” the “top surface of each step.” *Id.* Similarly, Lee explains that in its “stacked

structure[,]” “a plurality of conductive layers and a plurality of insulating layers” are “formed alternately with each other.” *Id.*, ¶ [0010].

352. Figure 7B, which is reproduced below, provides an example.

353. In this figure, layers 22 are “interlayer insulating layers.” Lee, ¶ [0046]. Layers 25 are “conductive layers.” *Id.*, ¶ [0041].

354. As shown, a “*first material layer*” (insulating layer 22, annotated blue) is “*disposed over a first portion*” of the “*second material layer*” (conductive layer 25, annotated green):



Lee, Fig. 7B (annotated). Figures 1A and 6B similarly show devices with alternating conductive and insulating layers. *See id.*, Figs. 1A, 6B.

[1.B]/[12.B] “a landing pad disposed over a second portion of the second material layer,”

355. In my opinion, Lee also teaches the claimed “*landing pad.*”

356. According to Lee, each of the “conductive layers” in its stepped stack may include a “pad portion PAD” at its end that has “a greater thickness” than other portions of “the ... conductive layer.” Lee, ¶ [0023]; *see also id.*, ¶ [0009] (Lee’s “semiconductor device” includes “pad portions” that “have a greater thickness than unexposed portions of the plurality of first conductive layers”); ¶ [0027] (similar).

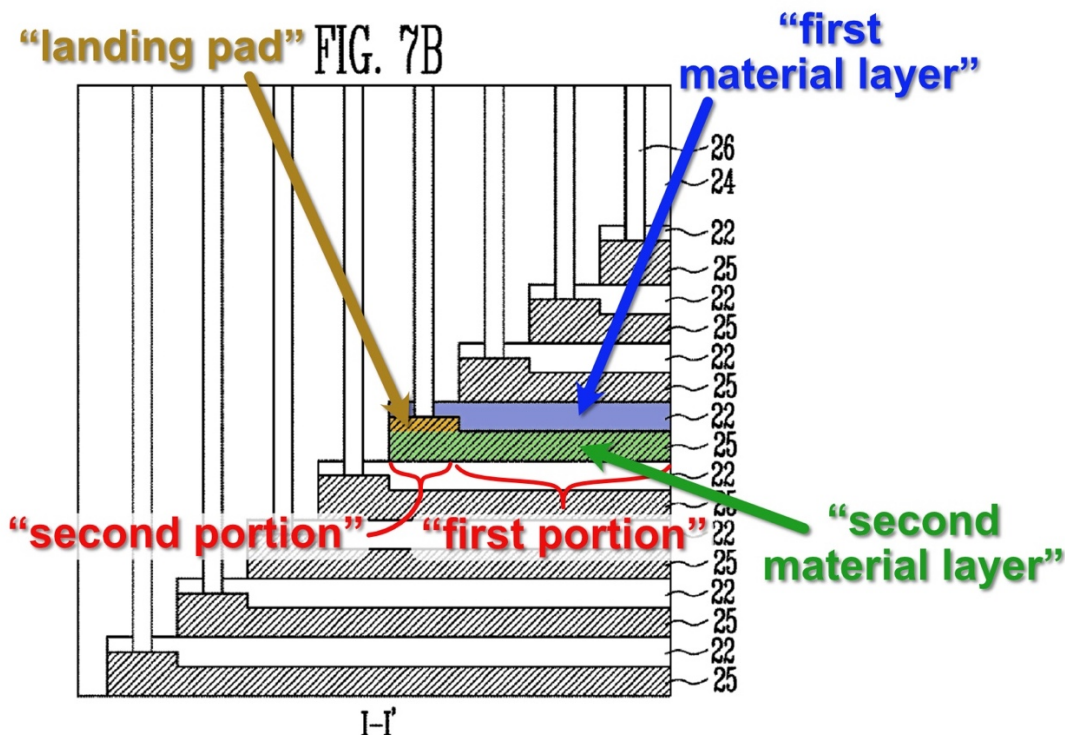
357. Lee explains that because the pad is only on the end of each conductive layer in its stack, “the thickness of the pad portion PAD may be selectively increased without increasing the height of stacked structure ST.” Lee, ¶ [0027]. In other words, the stack’s height does not increase, but the thickness of each pad does increase.

358. The “pad portions PAD” allow “contact plugs 26” to be “coupled” to each of Lee’s conductive layers. Lee, ¶ [0042].

359. According to Lee, the increased height of the pads is intended to avoid a “punch phenomenon ... due to over-etching of upper pad portions PAD” or a “not-open phenomenon” resulting from “lower pad portions PAD” which “may not be exposed along bottom surfaces of the contact holes.” Lee, ¶ [0043].

360. Figure 7B from Lee is reproduced below. In this figure, the pad portion PAD on the end of each of Lee’s conductive layer (annotated orange / brown) is the

claimed “*landing pad*.” As shown, it is located over a “*second portion*” of Lee’s “*second material layer*” (conductive layer 25, again annotated green):



Lee, Fig. 7A (annotated). Figure 1A similarly showing device with alternating insulating and conductive layers and pad portion PAD. *See id.*, Fig. 1A.

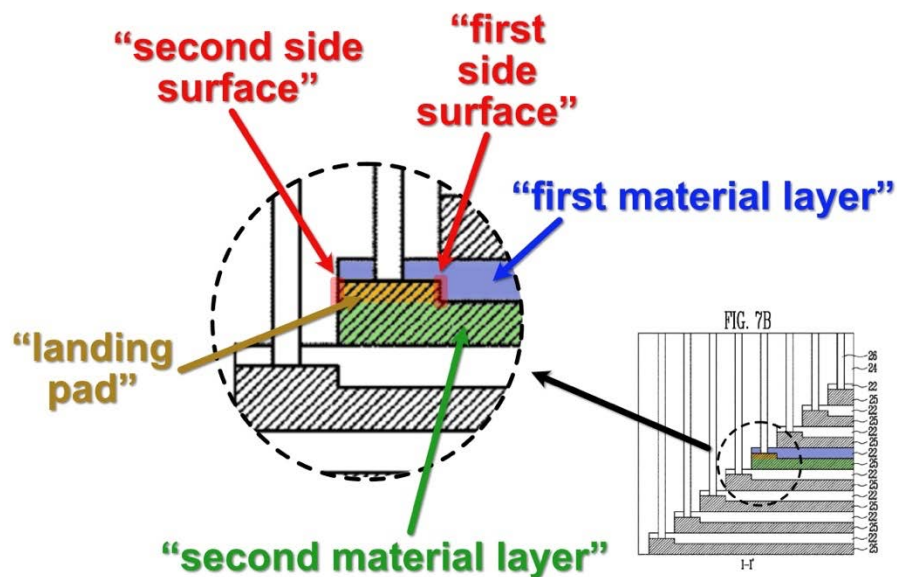
[1.B.1] / [12.B.1] “wherein the landing pad comprises a first side surface and a second side surface,”

361. This, in my opinion, is also taught by Lee.

362. Lee explains that its “pad portion PAD” has a “greater thickness” than the “conductive layer” on which it sits. Lee, ¶ [0023].

363. Lee also notes that the PAD includes “side wall[s.]” Lee, ¶ [0050].

364. Because the pad extends out of the top of the underlying conductive layer (and thus has dimension, including side walls), Lee's *"landing pad"* (the pad portion PAD) has both a *"first side surface"* (the side facing inwards towards insulation and conductive layers) and a *"second side surface"* (the side facing outwards). This is shown in the annotated version of Figure 7B for reference. The area around one pad has been expanded to better show this part of the structure:

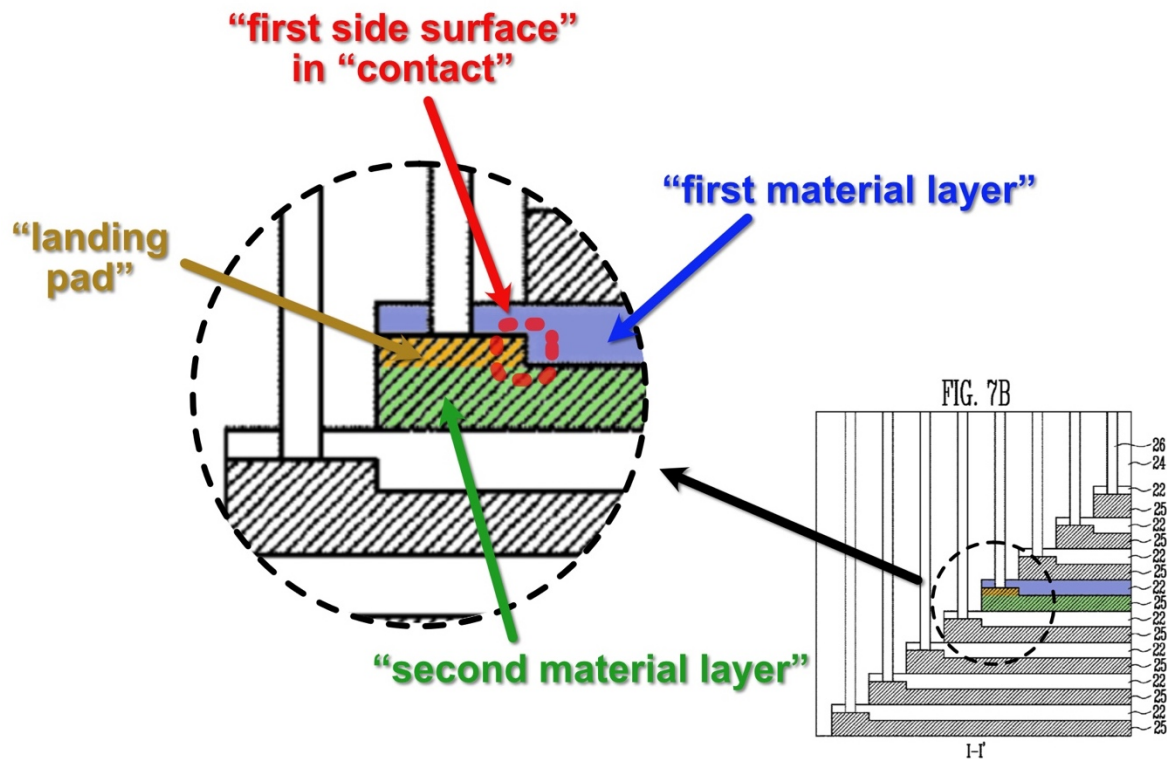


Lee, Fig. 7B.

[1.B.2] / [12.B.2] "wherein the first side surface is in contact with the first material layer and the second side surface is laterally displaced from a side surface of the second portion of the second material layer"

365. In my opinion, a POSITA would have considered this limitation obvious in view of Lee.

366. To begin, the “*first side surface*” of Lee’s “*landing pad*” (pad portion PAD) is in “*contact*” with the “*first material layer*” (insulating layer 22 in Figure 7B). This is shown in the annotated version of Figure 7B below. Once again, the area around one pad has been expanded to the left:



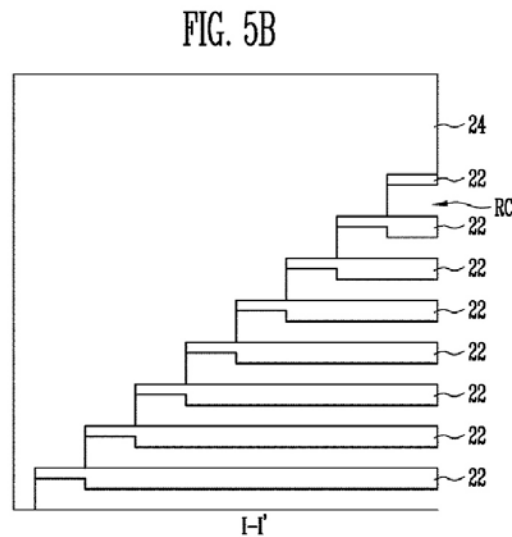
Lee, Fig. 7B (annotated).

367. A POSITA also would have understood that the process Lee employs to form its pad portion PAD confirms that there is contact between the PAD and the adjacent insulating layer.

368. Lee begins by forming “a plurality of first material layers 21 and a plurality of second material layers 22 ... alternately with each other.” Lee, ¶ [0029].

375. Then, it performs a second wet etch step to remove the impurity regions 23 to form “recessed regions RC” between the remaining portions of the insulating layers 22. Lee, ¶ [0038].

376. The formation of these openings or recessed regions RC are shown in Figure 5B



Lee, Fig. 5B.

377. Then, Lee explains that the openings formed via etching are filled with “conductive layers 25” to create the “pad portions PAD exposed at the end of stacked structure ST.” Lee, ¶ [0041].

The diagram shows a stepped profile with 12 horizontal layers. The layers are labeled on the right with values: 24, 22, 25, 22, 25, 22, 25, 22, 25, 22, 25, and 22. The horizontal axis is labeled H' .

378. Because Lee's pad portions PAD are formed within an opening in its insulating layers 22, a POSITA would have understood that the sides of the pad portions PAD contact the insulating layers.

380. Here, Lee explains that “additional processes” can be applied during the manufacture of the device shown in Figure 7B to produce a modified structure. Lee, ¶ [0047].

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at respective steps may be oxidized to thereby form a plurality of barrier layers 28.”

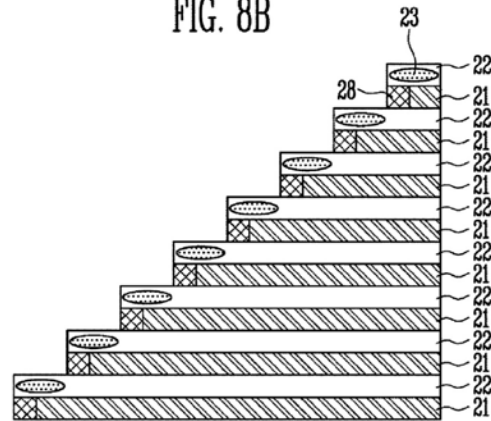
Lee, ¶ [0048].

382. Lee explains that this “barrier layer” is included “in order to ensure an etch margin when the ends of the recessed regions RC are extended.” Lee, ¶ [0049]. In particular, while the “recessed region RC” continues to “extend ... in a Z direction and thereby increase the thickness of the pad portions PAD,” extension in the “X direction” is now limited by the barrier. *Id.* This helps ensure there is “sufficient distance may be ensured between the stacked conductive layers” to prevent “deterioration” of “a breakdown voltage.” *Id.*

383. The “barrier layer” 28 remains behind in the final product. Lee, ¶ [0050].

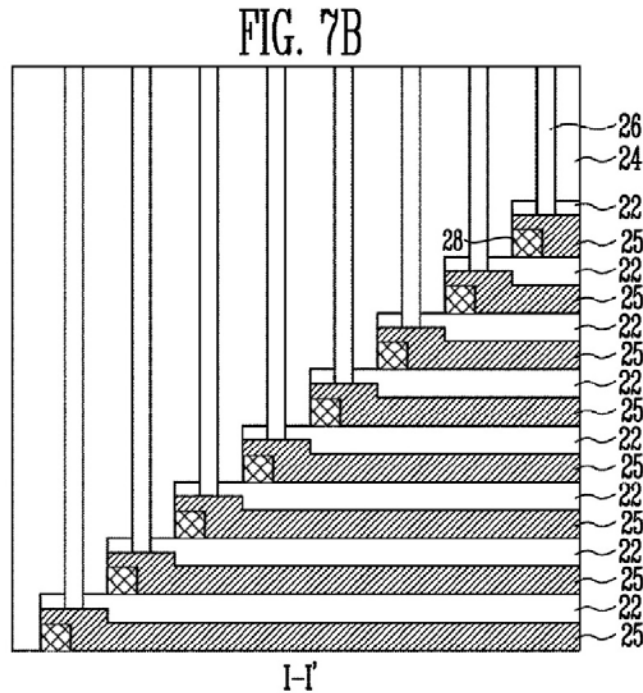
384. Figure 8B, which is reproduced below, shows this barrier layer 28 after ion implantation but before etching. The barrier layer 28 is shown with crosshatching. As Lee describes, the layer 28 is located at the end of sacrificial layer 21 shortening that layer such that it does not fully extend underneath the insulating layer 22 above it:

FIG. 8B



Lee, Fig. 8B.

385. While Lee does not include a figure showing the device after the sacrificial layers and ion implanted regions 23 in figure 8B are etched away and replaced with conductive material, the information it provides about layer 28's location and purpose provide enough information allowing a POSITA to understand how the final device will be structured. This is shown in the below modified version of Figure 7B of Lee:



Lee, Fig. 7B (modified).

386. The above figure was created by modifying Figure 7B of Lee to include barrier layer 28 from Figure 8B.

387. Following Lee's instruction, the barrier layer 28 replaced a portion of the end of sacrificial layer 21 under insulating layer 22. Again, this sacrificial layer 21 served as a precursor to conductive layer 25. Because of the presence of layer 28, etching was limited in the X direction resulting in an opening that was shorter in the X-direction. This in turn reduced the length of each of Lee's conductive layers 25 in the X-direction by an amount equal to the width of the barrier layer 28. A POSITA would have understood that this is the purpose of barrier layer 28: to serve

as an etch stop and limit the extent of conductive layer 25 in the X-direction in Figure 7B.

388. Because the ion implanted region 23 in insulating layer 22 had the same physical extent in Figure 8B as Figure 7B (albeit with the implanted region in Figure 8B partially located over the underlying barrier layer 28), Lee's pad portion PAD will continue to have the same size as shown in Figure 7B.

389. As I have explained, the only change was to layer 25 which now has reduced length in the X direction due to the presence of barrier layer 28.

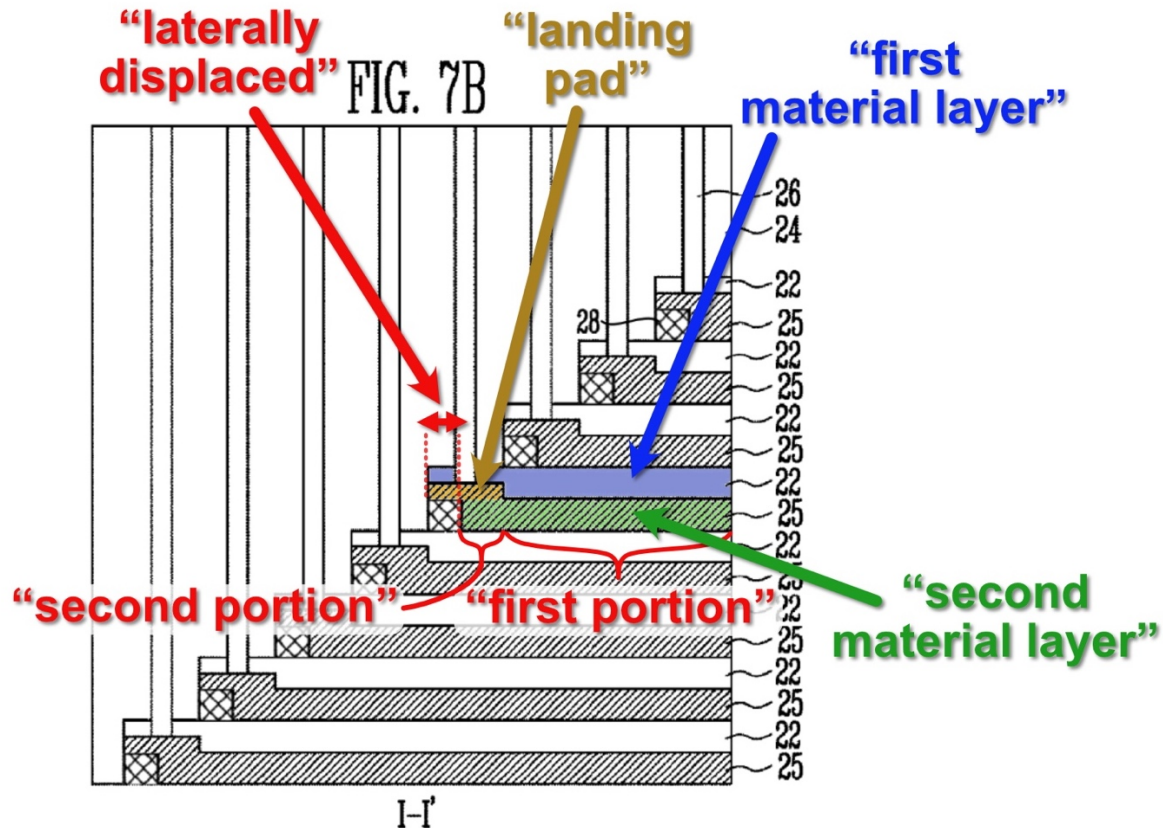
390. This causes the PAD in the finished device to extend over the barrier layer 28 that—per Lee—remains behind.

391. In my opinion, this modified structure including barrier layer 28 is what this claim requires.

392. This is shown in the below figure. This figure is the modified version of Figure 7B I discuss above (with barrier layer 28 applied following Lee's teachings). Annotations have now also been added.

393. As shown, not only is the ***“first side surface”*** of Lee's ***“landing pad”*** (pad portion PAD, annotated orange/brown) still in ***“contact”*** with the ***“first material layer”*** (insulating layer 22, annotated blue), but the pad's ***“second side surface”*** is now ***“laterally displaced”*** from the ***“side surface of the second portion***

of the second material layer” (the end of conductive layer 25, annotated green, that is adjacent to now included barrier layer 28):



Lee, Fig. 7B (modified).

2. Claim 4

394. Claim 4 depends on Claim 1 and further requires:

[4] “wherein the landing pad comprises a conductive material.”

395. This, in my opinion, is taught by Lee.

396. Here, Lee explains that layers 25 (its conductive layers) and pad portions PAD at the ends of those layers (the claimed *“landing pad”*) are formed from “conductive” material. Lee, ¶¶ [0040]-[0041].

3. Claim 5

397. Claim 5 depends on Claim 4 and further requires:

[5] “wherein the conductive material comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof.”

398. This, in my opinion, would have been obvious in view of Lee and the knowledge of one of ordinary skill in the art.

399. Lee does not indicate what specific conductive material should be used to make its layers 25 and PAD portions.

400. Lee does, however, it does identify “tungsten (W)” as an example conductive material usable in its device. Lee, ¶ [0074].

401. In my opinion, a POSITA would have considered use of this material one obvious choice when forming Lee’s conductive layers 25 and pads.

402. A POSITA would also have considered it obvious to use other well-known conductive materials known in the art at the time the ’838 patent was filed to form the conductive layers and contact pads in three-dimensional memory devices.

403. There were numerous such well-known conductive materials. Example materials included, for instance, metals such as tungsten, aluminum, copper, cobalt, nickel, hafnium, platinum, and titanium, doped silicon, metal silicides, metal nitrides, and combinations of these various materials. Park, 10:51-45; Nam, ¶ [0094]; Kim, 6:31-36.

404. In my opinion, A POSITA would have recognized that Kim was referring to—and obviously allowed the use of—any of these materials when it stated that its layers 25 and contact pads should be made “conductive.”

405. Tungsten was also the most commonly used standard gate layer material because it can be readily deposited as part of a gate replacement process and has a high conductivity and low resistivity (resulting in fast access operations). *See, e.g.*, Ex. 1011, 318, 320. Thus, this material would have been particularly obvious to employ when implementing Lee’s conductive layers.

4. Claims 6 and 20

406. Claim 6 depends on Claim 1. Claim 20 depends on Claim 12. Both claims further require:

[6]/[20] “wherein the second material layer is disposed over a first portion of another first material layer, and wherein a side surface of a second portion of the another first material layer is laterally displaced from the second side surface of the landing pad.”

407. This, in my opinion, is taught by Lee.

408. As I have explained, Lee’s device includes a “stacked structure ST” formed from alternating “conductive layers” and “insulating layers.” Lee, ¶ [0021]; *see also id.*, ¶¶ [0010], [0041], [0046]; Figs. 1A, 7A.

409. The modified version of Figure 7B of Lee is again reproduced below (as discussed above, this figure has been modified to include Lee’s barrier layer 28). As shown, because Lee’s device is formed from alternating insulating and

FIG. 7B

“landing pad”

“first material layer”

“second material layer”

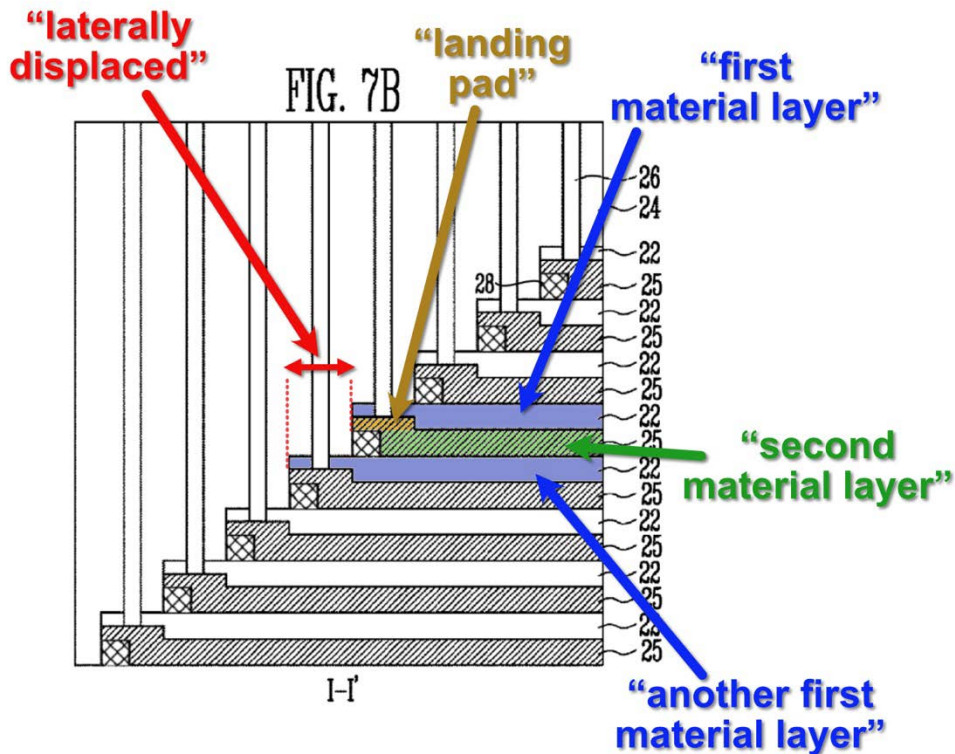
“first portion”

“another first material layer”

I-I

410. Next, Lee also explains that “[e]ach step of the stacked structure ST that is patterned stepwise” includes “one conductive layer” and “one insulating layer.” Lee, ¶ [0021].

412. As shown in the modified version of Figure 7B below, because insulating material is located on the top of each step, *“a side surface of a second portion of the another first material layer”* (the portion of a lower insulating layer 22 that extends out beyond an upper adjacent conductive layer 25 for purposes of forming a step) being *“laterally displaced”* from *“the second side surface of the landing pad”* (the leftmost side of Lee’s pad portion PAD):



Lee, Fig. 7B (annotated and modified).

5. Claims 7 and 17

413. Claim 7 depends on Claim 1. Claim 17 depends on Claim 12. Both claims further require:

[7]/[17] “wherein the second material layer comprises a first conductive material and the landing pad comprises a second conductive material substantially the same as the first conductive material.”

414. This, in my opinion, is taught by Lee.

415. Once again, according to Lee both its conductive layer 25 (the “*second material layer*”) and the pad portion PAD (the “*landing pad*”) at this layer’s end is made from the same “conductive” material. Lee, ¶¶ [0040]-[0041]. Because they are made from the same conductive material, these two components employ a “*conductive material*” that is “*substantially the same.*”

6. Claim 16

416. Claim 16 depends on Claim 12 and further requires:

[16] “wherein the second material layer comprises tungsten, and titanium nitride.”

417. In my opinion, a POSITA would have considered this obvious for the same reasons I explained in connection with Claim 5 above.

418. Again, while Lee does not identify the specific conductive materials that should be used to make its conductive layers and pads, a POSITA would have known of and considered it obvious to use any of the various, well-known conductive materials routinely employed in memory devices when implementing Lee’s conductive layers. *See supra* discussion of Claim 5.

419. Further, as I also explained, these well-known materials included “combinations” of materials such as a “metal” like “tungsten” and a “metal nitride”

like “nitride titanium.” Kim, 6:31-36; Nam, ¶ [0094] (similarly referencing “combinations” of “metal” and other materials).

7. Claim 19

420. Claim 19 depends on Claim 12 and further requires:

[19] “a dielectric layer disposed over the first material layer and the landing pad, wherein the first material layer comprises a first dielectric material and the dielectric layer comprises a second dielectric material, wherein the first dielectric material is substantially the same as the second dielectric material, and wherein the first dielectric material comprises silicon oxide.”

421. In my opinion, Lee teaches a device that includes the claimed *“dielectric layer disposed over the first material layer and the landing pad.”*

422. Lee explains that its device includes an “interlayer insulating layer 24” that is “formed on” its other “material layers...” Lee, ¶ [0036].

423. The modified version of Figure 7B is once again reproduced below in annotated form. As shown, the layer 24—which is annotated yellow and corresponds to the claimed *“dielectric layer”*—is located over both the *“first material layer”* (insulating layer 22, annotated blue) and the *“landing pad”* (the pad portion PAD, annotated orange/brown):

428. Regardless, a POSITA would have recognized that this was the most widely and commonly used insulating material in memory devices. *See, e.g.,* Kim, 6:35-46 (referencing the use of “silicon oxide” “insulating layers”); Nam, ¶ [0048] (similarly referencing the use of “silicon oxide” layers); Park, 8:1-2 (same).

429. Thus, a POSITA would have understood that Lee’s reference to “oxide layer[s]” obviously includes layers of silicon oxide.

E. Ground 4: Claims 3 and 18 Are Obvious Over Lee and Haller

430. In my opinion, a POSITA would have considered both Lee and Haller to be within the scope of the prior art and highly relevant to the patentability of the ’838 patent’s claims.

431. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Lee and Haller together render Claims 3 and 18 of the ’838 patent obvious.

432. Claim 3 depends on Claim 1. Claim 18 depends on Claim 12. Both claims further require:

[3]/[18] “wherein a lateral distance between the second side surface and the side surface of the second portion of the second material layer is between 10 nm and 300 nm.”

433. As I discussed in connection with Claim 1, Lee employs a “barrier layer 28” that operates to limit etching in the X direction during manufacture of its memory device.

434. The barrier layer 28 remains behind in Lee's final device and (1) limits the extent or length of conductive layer 25 and (2) increases the distance between Lee's pad portion PAD and adjacent conductive layers. *See* Lee, ¶ [0049].

435. Further, as I also explained when discussing Claims 1 and 12, inclusion of the barrier layer 28 at the end of each conductive layer also causes Lee's "**landing pad**" (the pad portion PAD) to be "**laterally displaced**" from its "**second material layer**" (conductive layer 25) by a distance equal to the thickness of layer 28. *See supra* discussion of limitation [1.B.2].

436. Lee does not provide an example of layer 28's thickness.

437. In my opinion, a POSITA would have considered it obvious that this layer would have a thickness falling within the range required by this claim: between "**10 nm and 300 nm.**"

438. Haller (Ex. 1008) provides an example of this.

439. Haller relates to a "3D memory device" with a "staircase structure." Haller, 4:8-12.

440. According to Haller, in prior art memory devices, problems may arise when performing an "etch process" to form contacts to the device's wordline layers. Haller, 1:30-35. The etch may either "punch[] through" the wordline (extend too far in the vertical direction) or "leak[]" over the wordline edge (extend too far in the horizontal direction) "creating an undesired short circuit." *Id.*

441. In an effort to avoid this, Haller includes an “etch stop” at the end of each conductive wordline layer in its staircase structure. Haller, 2:6-9.

442. According Haller, incorporation of the etch stop “prevent[s] ... physical or electrical contact of the wordline contact structure with an adjacent wordline of the staircase structure.” Haller, 2:19-23.

443. This etch stop includes a component labeled as “spacer 502” in Figure 9, which I have reproduced below:

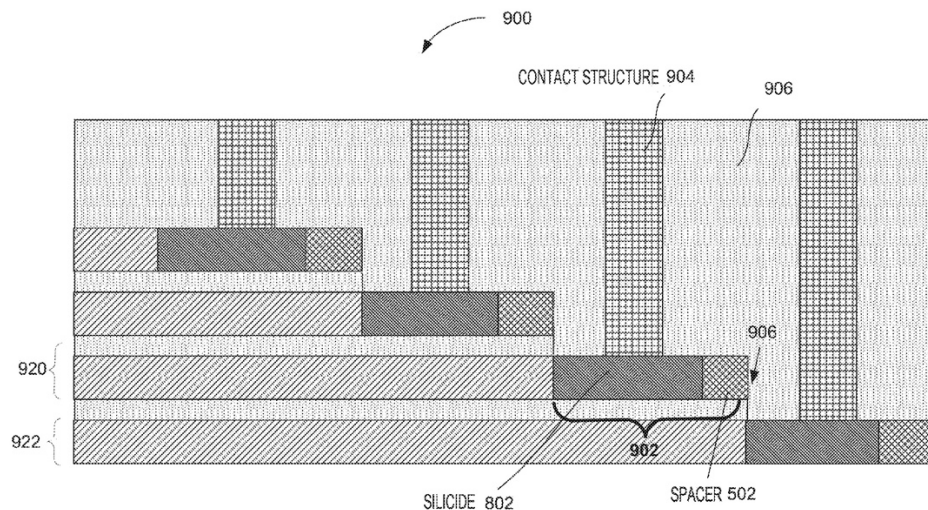


FIG. 9

Haller, Fig. 9; 6:28-63 (discussing function of spacer 502).

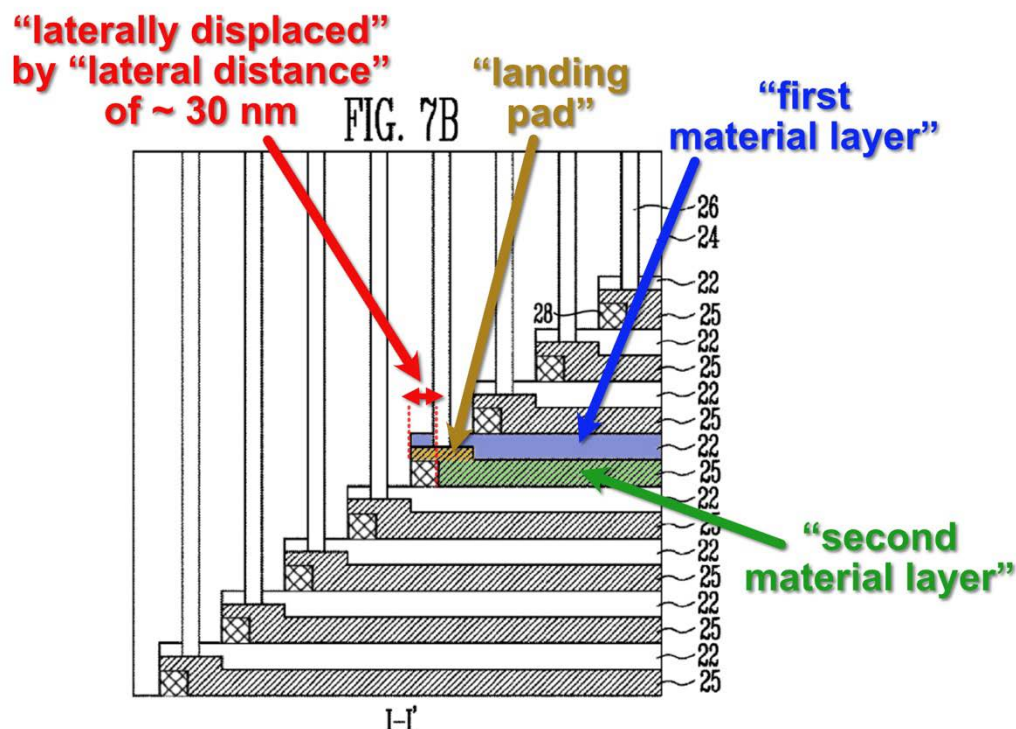
444. As shown, just like Lee’s barrier layer 28 (which also functions as an etch stop), Haller’s spacer 502 is located at the end of each of its conductive layers.

445. Haller explains that the spacer 502 is formed by depositing “insulative dielectric material” into a “recess” that is “30 nm in length.” Haller, 4:37-5:7; Figs.

3-5. Because of this, the spacer 502 will have a length of approximately 30 nm in the final device.

446. In my opinion, applying Haller's example spacer and etch stop dimension—30 nm—to Lee renders this claim obvious.

447. This is once again shown in the below modified version of Figure 7B. A POSITA would have understood and considered it obvious that Lee's layer 28 would have a thickness of 30 nm causing its "*landing pad*" (pad portion PAD, again annotated orange / brown) to overhang—or be "*laterally displaced*" by a "*lateral distance*"—from the edge of the underlying "*second material layer*" (conductive layer 25, annotated green) by approximately 30 nm. This is within the range of "*10 nm and 300 nm*" required by Claims 3 and 18:



Lee, Fig. 7B (modified and annotated).

448. In my opinion, a POSITA would have been motivated to apply Haller's example dimension to Lee and would have had a reasonable expectation of success when doing so.

449. There are, in my opinion, a number of reasons for this.

450. First, Lee does not include example dimensions for its memory device. Thus, a POSITA would out of necessity have needed to consult both their background knowledge and other references when implementing Lee.

451. A POSITA would have considered Haller to be particularly relevant in this regard. Like Lee, Haller also relates to a three-dimensional memory device with

a staircase structure. And, like Lee it also employs an etch stop at the end of each its conductive layers to avoid short circuits during manufacture.

452. This similarity in purpose and design—in particular the similarity between barrier layer 28 in Lee and spacer 502 in Haller—would have provided a strong motivation to employ Haller’s example dimension with Lee.

453. Second, a POSITA would have recognized that layers in three-dimensional memory devices routinely had thicknesses in the range of approximately 20-90 nm. *See, e.g.,* Yang, 6:7-28.

454. In my opinion, this would have confirmed to a POSITA that Haller’s example etch stop spacer thickness would not only have been obvious to employ with Lee, but that dimensioning Lee’s layer 28 this way would have been successful.

455. Moreover, as explained above in connection with Ground 2, the range of Claims 3 and 18 embraces almost all reasonable lateral displacements given typical memory staircase sizes. This would have further confirmed the obviousness of employing a layer 28 thickness and associated pad overhang of approximately 30 nm with Lee.

456. In short, a POSITA would have considered Haller to be representative of the range of dimensions appropriate for use with Lee—and would have been motivated to look to Haller—because both references address the shared challenge of preventing short circuits in 3D memory devices with staircase structures during

fabrication. Lee's barrier layer 28 and Haller's spacer 502 serve analogous functions as etch stops, and Haller explicitly provides a spacer thickness of 30 nm, which ensures precise etching control while avoiding device damage. This dimension aligns with typical industry standards for similar architectures, as disclosed in Yang (20–90 nm). The similarity in purpose and design between the two references, combined with the predictable results of employing well-known fabrication techniques, would lead a POSITA to apply Haller's example dimensions to Lee with a reasonable expectation of success.

F. Ground 5: Claims 13-15 Are Obvious Over Lee and Park

457. In my opinion, a POSITA would have considered both Lee and Park to be within the scope of the prior art and highly relevant to the patentability of the '838 patent's claims.

458. In my opinion, when Lee is modified in view of Park and the knowledge of a POSITA, Claims 13-15 of the '838 patent are rendered obvious.

1. Claim 13

459. Claim 13 depends on Claim 12 and further requires:

[13] “wherein the first side surface comprises a curved side surface.”

460. Lee depicts its pad portions PAD as having straight sides in its figures.

461. Regardless, in my opinion, a POSITA would have considered it obvious to make the “*side surface*” of Lee’s “*landing pad*” “*curved*” in view of Park’s teachings. Lee highlights the importance of maintaining sufficient spacing between

conductive layers to prevent breakdown voltages. Park's teachings on rounded pad designs directly address this issue by increasing the distance between adjacent conductive layers. A POSITA would recognize that rounding Lee's pad portions would align with Lee's stated goals and provide a straightforward design modification with predictable success.

462. Park teaches a three-dimensional memory device that includes a stepped "connection region" with "pad region[s] PAR" located on the end of gate electrodes. Park, 6:7-12, 7:36-47.

463. Each of Park's electrodes terminates with a "pad region PAR" that includes a "raised pad portion" 78 Park, 7:4-16.

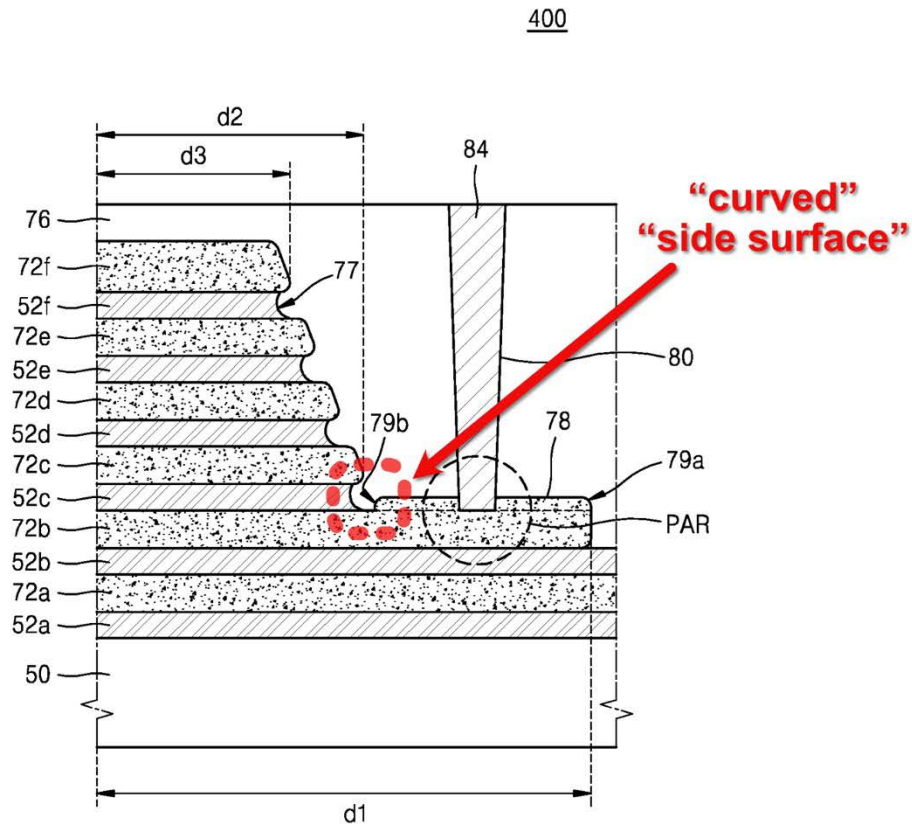
464. Park also explains that the "end 79b" of this "raised pad portion" 78 may be "rounded" to "prevent a short circuit" between the pad and an "adjacent ... conductive layer pattern 72c." Park, 11:35-41.

465. Park explains that it achieves its rounded contact pad by "ion implanting impurities" "into" an "insulating layer" and performing an "oxidation" step to create a "additional sacrificial layer" "having a higher etching rate" than the surrounding insulation. Park, 12:16-23, 39-47.

466. The sacrificial material is then removed and replaced with conductive material to form insulation surrounded electrodes and curved pads. Park, 12:48-56.

467. Figure 7 from Park below shows the eventual result of this process: a pad 78 with a curved surface 79b facing towards Park's stack of alternating conductive and insulating layers:

FIG. 7



Park, Fig. 7 (annotated).

468. Similar processes—the implantation of impurities into a layer of insulation to form an etchable region corresponding to a desired contact pad shape—was also used by other prior art to form contact pads with rounded sides surrounded by insulation.

469. For example, Nam discusses the use of multiple ion implantation steps to form a contact pad with a bullnose or a convex shape with rounded sides similar to those taught in Park. *See, e.g.*, Nam, ¶¶ [0097]-[0105]; Figs. 30-37.

470. Applying Park's teachings to Lee—and making at least the end of Lee's pad portion PAD facing its conductive layers rounded—results in what this limitation requires.

471. Again, a pad with a rounded side would have been achieved by tailoring the ion implantation steps (or ion implantation and oxidation steps like that taught by Park) to produce this particular shape.

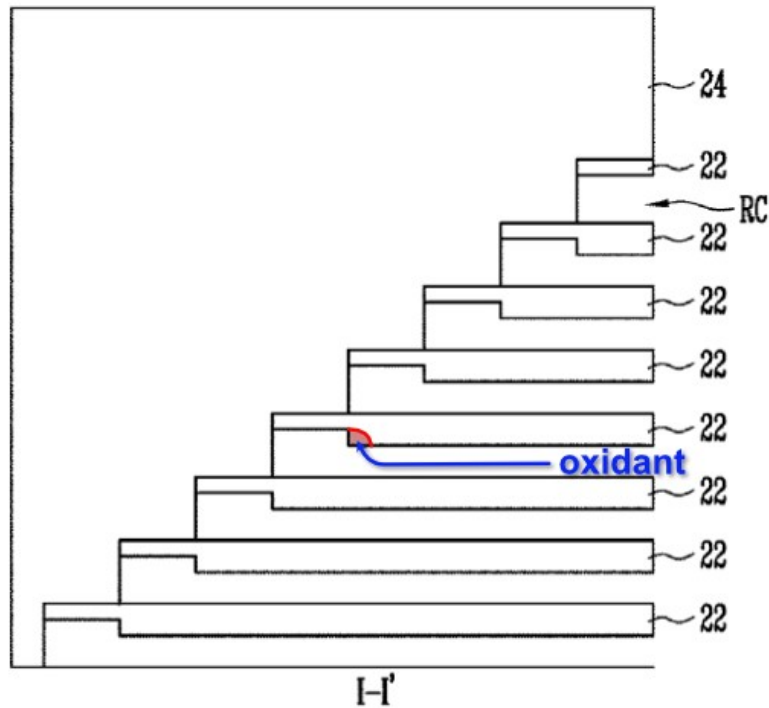
472. In particular, a POSITA would have understood that to achieve a contact pad with a curved side, the process shown in Figures 3B, 4B, and 5B of Lee could still be followed: ion implantation would be performed on the insulating layers, and then etching steps would be performed to remove the intervening sacrificial layers followed by the region where ion implantation occurred. This would then result in the same-shaped openings shown in Figure 5B of Lee. Then, to achieve a rounded rather than straight sided contact pad, oxidant would be introduced into the openings.

473. A POSITA would have recognized that oxidation rates differ at exposed corners and planar surfaces due to variations in oxidant flux and material redistribution, leading to rounded corners. The exterior corner (red below) would

be rounded via oxidation first and most aggressively. The oxidant's actions on the interior corners would be somewhat slower, while the action on the planar surfaces would be even slower. A convex (or exterior) corner like that highlighted below rounds off during oxidation because the sharp geometry increases the flux of oxidizing species and the strain energy at the tip, leading to a faster reaction rate compared to flat surfaces. As oxidation progresses, the oxide material redistributes, smoothing the sharp corner into a rounded shape. Concave (or interior) corner will also round off, albeit more slowly. The sharp geometry of the corner reduces localized stress concentrations, prompting material diffusion and redistribution to lower the strain energy. Due to the difference in geometry and mechanism of action, this produces a more gradual smoothing than experienced at a convex (or exterior) corner. Neither of these effects apply to planar surfaces.

474. The amount of rounding would be readily controllable—and confined to the depicted exterior corner with only limited impact on the interior corners and planar surfaces—by adjusting the amount of time the oxidant is permitted to remain within the opening:

FIG. 5B

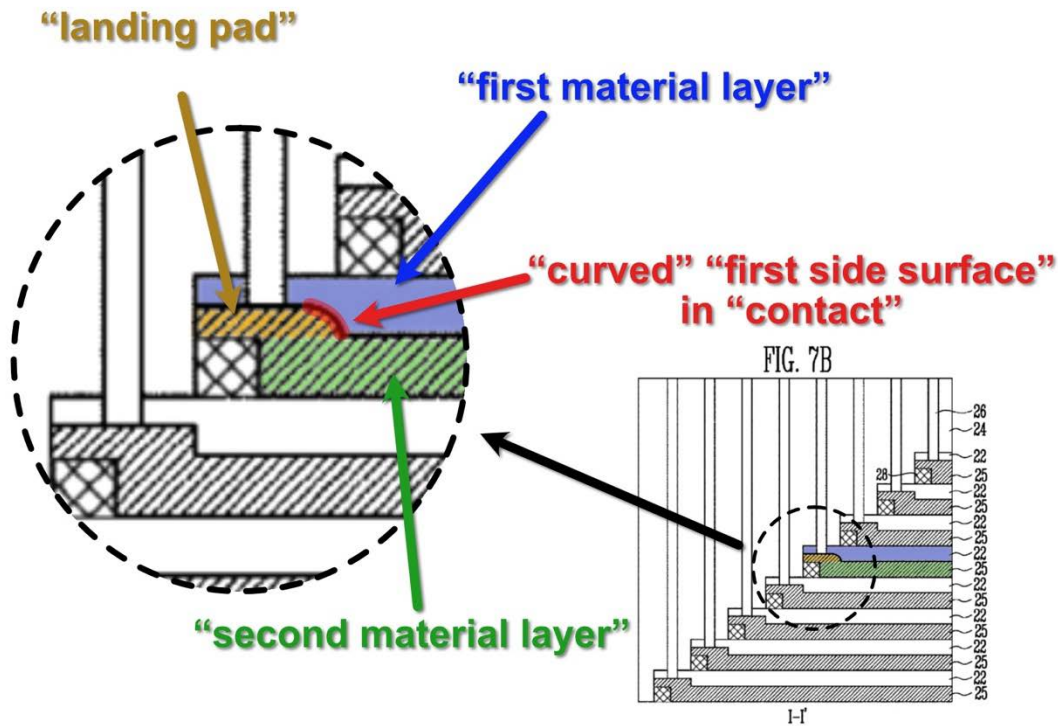


Then, when this now rounded opening is filled with conductive material, a contact pad with a rounded side results.

475. Applying Park’s teachings to Lee—and making at least the end of Lee’s pad portion PAD facing its conductive layers rounded—results in what this limitation requires.

476. This is shown in the below demonstrative. Now, the *“first side surface”* of Lee’s *“landing pad”* (pad portion PAD, annotated orange / brown) that is in *“contact”* with the *“first material layer”* (insulating layer 22, annotated blue) is *“curved.”*

477. Note that two modifications have now been made to this figure. First, barrier layer 28 (the crosshatching) has been added for the reasons discussed above. Then, this structure was further modified by following Park's teachings regarding pad rounding:



Lee, Fig. 7B (modified and annotated).

478. In my opinion, a POSITA would have been motivated to make the end of Lee's pad portion PAD facing its insulating and conductive layers rounded.

479. Again, Park explains that rounding the contact pad helps "prevent a short circuit" between the pad and an "adjacent" conductive layer. Park, 11:35-41.

480. Lee already incorporates the barrier layer 28 for purposes of ensuring that there is "sufficient distance ... between the stacked conductive layers (pad

portions).” Lee, ¶ [0049]. Increasing this distance, according to Lee, reduces the risk that the “breakdown voltage” between these layers may be “deteriorated.” *Id.*

481. In my opinion, a POSITA would have understood that applying Park’s teachings and rounding Lee’s pad portions PAD is both consistent with and supplements this goal.

482. Rounded pad corners would serve to further increase the distance between adjacent conductive layers resulting in an additional reduction in the risk of short circuit and breakdown.

483. A POSITA further would have recognized that contact pads with rounded, curved side surfaces were also a known, routinely used alternative for memory devices with staircase structures at the time the ’838 patent was filed. *See, e.g.,* Kim, 8:29-34 (noting that contact pads can have a “curved surface”); Park, 11:35-41 (contact pad can be “rounded”); Yun, 8:33-40 (contact pad can have “rounded” “side surface”; Nam, ¶ [0066] (contact pad can have “bull nose” or “convex” shape).

484. In my opinion, given the prevalence of contact pads with this type of shape in the prior art, a POSITA would have considered the use of rounded/curved pads with Lee to be nothing more than a routine, obvious design choice.

485. A POSITA would also have had every reason to believe that a curved pad could be successfully used with Lee.

486. Again, numerous prior art references identified this type of pad as acceptable for three-dimensional memory devices with staircase structures. *See, e.g.,* Kim, 8:29-34 Park, Fig. 8; Yun, Fig. 5A; Nam, Fig. 8A.

487. Moreover, Lee explains that the shape of its pad portion PAD is controlled via an “ion implantation process.” Lee, ¶¶ [0035], [0038]-[0041].

488. In my opinion, and as I discussed further above, a POSITA would have recognized that this type of process could be readily adapted to form a curved contact pad. *See, e.g.,* Park, 7:17-29 (“ion implantation” and “oxidation” to form pad with “rounded” sides); Nam, ¶¶ [0066], [0098]-[0107]; Figs. 30-39 (discussing use of “an ion implantation process” at length to form “convex” contact pad).

489. In short, a POSITA would have been motivated to combine Park’s teachings of rounded contact pads with Lee’s pad portion PAD to enhance the spacing and reduce risks of electrical short circuits and breakdown voltage. Park’s specific process steps for forming rounded pads using ion implantation and oxidation provide a clear, predictable method to achieve Lee’s objectives. Additionally, the widespread use of rounded contact pads in similar memory device structures, as demonstrated by Park, Nam, and Kim, would reinforce the obviousness of this modification. Given that Lee already employs ion implantation to control pad geometry, a POSITA would readily adapt this process to form rounded pads, further improving device performance while adhering to known design practices.

2. Claim 14

490. Claim 14 depends on claim 13 and further requires:

[14] “further comprising another second material layer disposed on the first material layer, wherein a first lateral distance between the first side surface and a side surface of the another second material layer is smaller than a second lateral distance between the second side surface and the side surface of the another second material layer.”

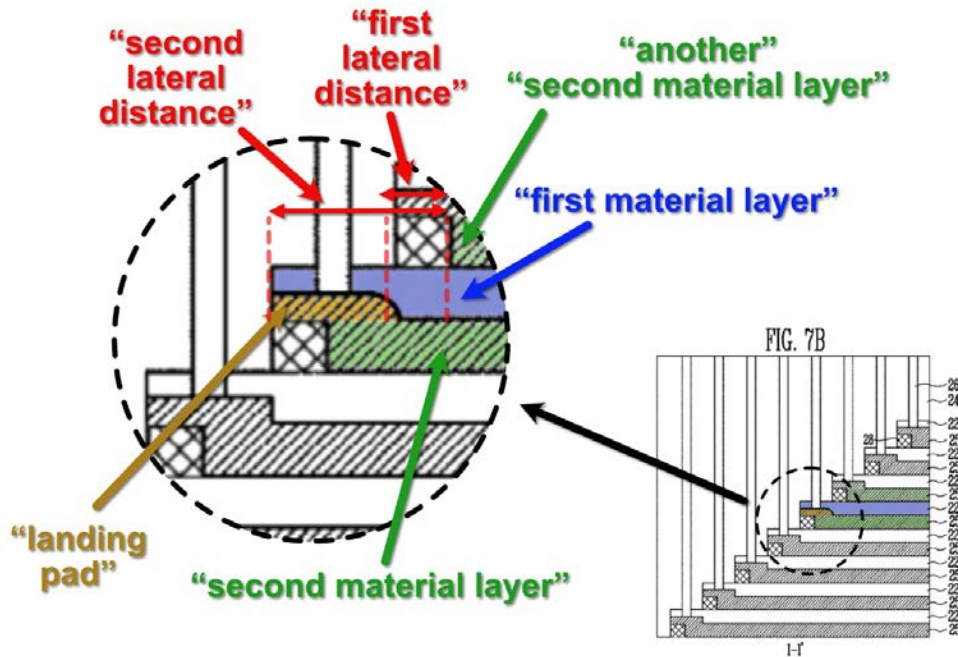
491. This, in my opinion, is taught by Lee.

492. Again, as I have repeatedly explained, Lee’s device includes alternating conductive and insulating layers. Lee, ¶ [0021]; *see also id.*, ¶¶ [0010], [0041], [0046]; Figs. 1A, 7A.

493. Because of this, there is ***“another second material layer”*** (a further conductive layer 25) that is ***“disposed on the first material layer”*** (the insulation layer 22 discussed in connection with claims 1 and 12 above).

494. Further, as I have also explained, Lee’s device is formed “stepwise.” Lee, ¶ [0021]; *see also id.*, ¶ [0009].

495. This causes upper conductive layers to be stepped back from lower layers. Because of this, the ***“first lateral distance between the first side surface and a side surface of the another second material layer”*** (the distance between a pad’s right side in Fig. 7B and the side of the conductive layer above the pad) is ***“smaller”*** than ***“second lateral distance between the second side surface and the side surface of the another second material layer”*** (the distance between the same pad’s left side and the conductive layer):



Lee, Fig. 7B (modified and annotated).

3. Claim 15

496. Claim 15 depends on Claim 13 and further requires:

[15] “wherein the second side surface is laterally displaced from the first side surface, and wherein a first lateral distance between the first side surface and the first portion of the second material layer is smaller than a second lateral distance between the second side surface and the first portion of the second material layer.”

497. This, in my opinion, is taught by Lee.

498. As shown in the figure below (once again, this is the modified version of Figure 7B from Lee that I have been discussing), because Lee’s pad portion PAD has a width, the “*first*” and “*second*” “*side surface[s]*” of the pad are “*laterally displaced*” from each other.

499. Moreover, the pad’s width and location on the underlying conductive layer 25 causes “*a first lateral distance between the first side surface and the first*

G. Secondary Considerations of Non-Obviousness

501. I am not separately aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like. Instead,

as discussed above, it is my opinion that the subject matter embraced by the '838 patent's claims was known in and obvious over the prior art. Moreover, it is also my opinion the teachings of the prior art would have been expected to successfully function as or be usable with working 3D memory devices.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: January 3, 2025

Location: Austin TX

Signature: 
DR. JACK C. LEE