US 20110031630A1

(19) **United States**

(12) **Patent Application Publication**

HASHIMOTO

(10) **Pub. No.: US 2011/0031630 A1**

(43) **Pub. Date: Feb. 10, 2011**

(54) **SEMICONDUCTOR DEVICE MANUFACTURING METHOD AND SEMICONDUCTOR DEVICE**

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(21) Appl. No.: **12/709,124**

(22) Filed: **Feb. 19, 2010**

(30) **Foreign Application Priority Data**

Aug. 4, 2009 (JP) 2009-181361

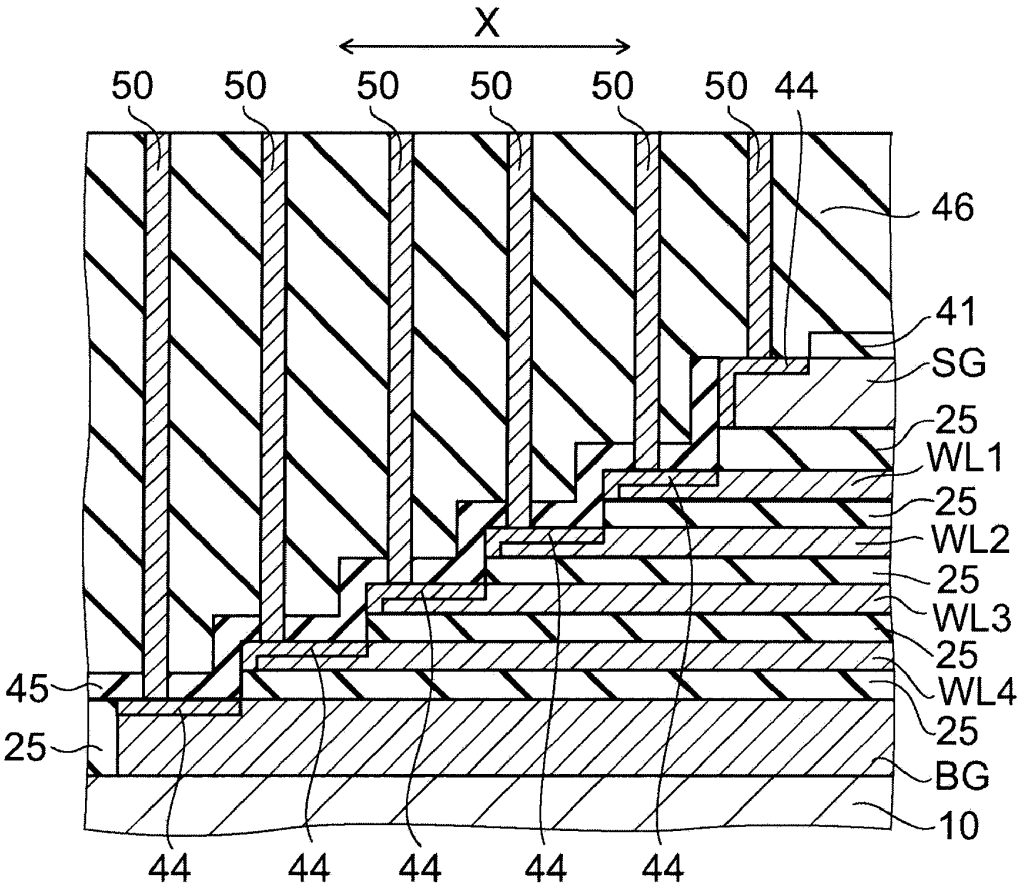
Publication Classification

(51) **Int. Cl.**
H01L 23/538 (2006.01)
H01L 21/768 (2006.01)

(52) **U.S. Cl.** **257/774**; 438/637; 257/E23.169; 257/E21.585

(57) **ABSTRACT**

A semiconductor device manufacturing method includes: stacking a plurality of electrode layers containing a semiconductor alternately with insulating layers; processing part of a multilayer body of the electrode layers and the insulating layers into a staircase shape and exposing a surface of the staircase-shaped electrode layers; forming a metal film in contact with the exposed electrode layers; reacting the semiconductor of the electrode layers with the metal film to form a metal compound in at least a portion of the electrode layers in contact with the metal film; removing an unreacted portion of the metal film; forming an interlayer insulating layer covering the staircase-shaped electrode layers after removing the unreacted portion of the metal film; forming a plurality of contact holes piercing the interlayer insulating layer, each of the contact holes reaching the metal compound of the electrode layer at a corresponding stage; and providing a plurality of contact electrodes inside the contact holes.



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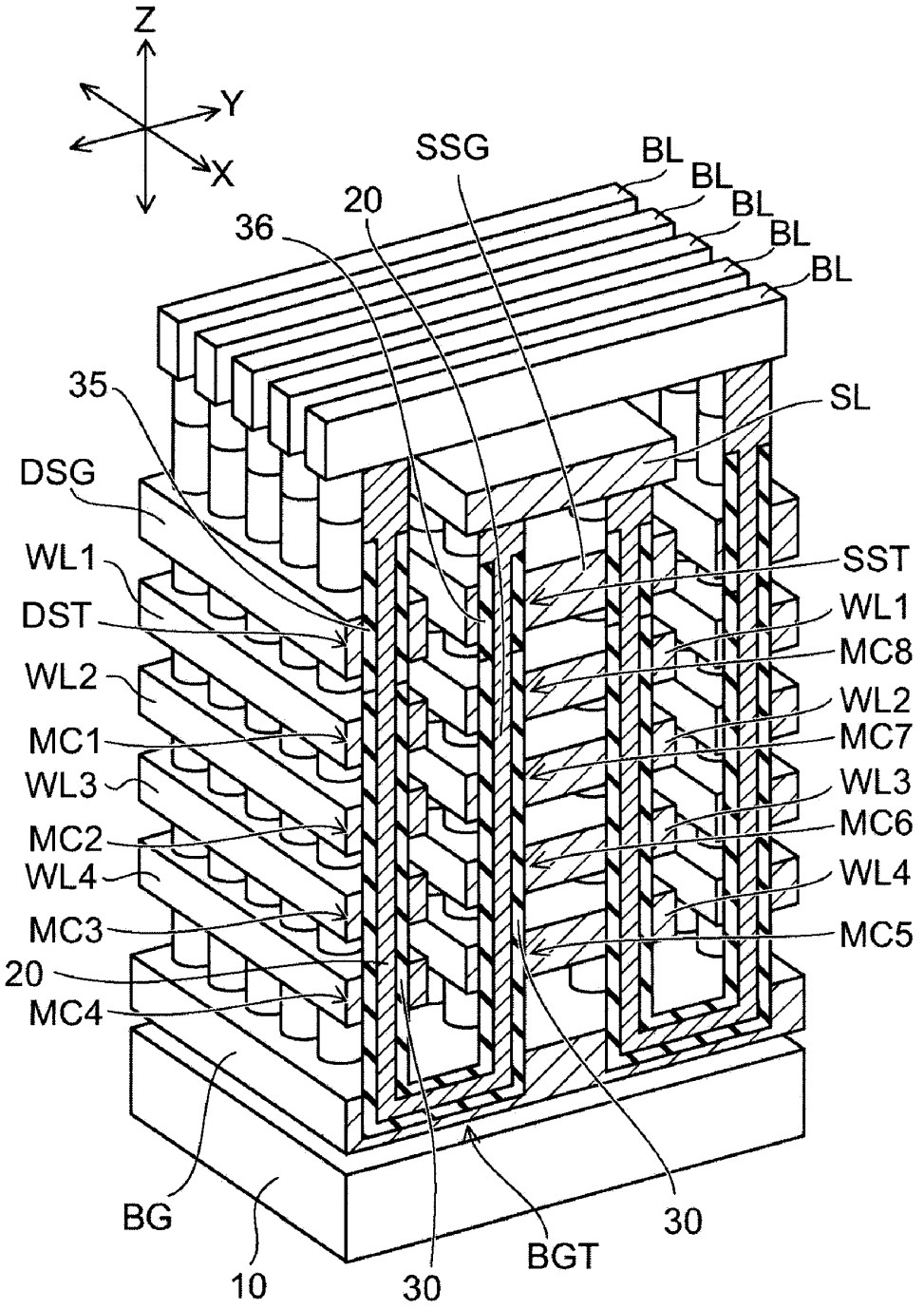

Z
Y
X
SSG
BL
BL
BL
BL
BL
20
36
35
SL
DSG
WL1
SST
DST
WL1
MC8
WL2
WL2
MC1
MC7
WL3
WL3
MC2
MC6
WL4
WL4
MC3
MC5
20
MC4
BG
10
30
BGT
30

FIG. 1

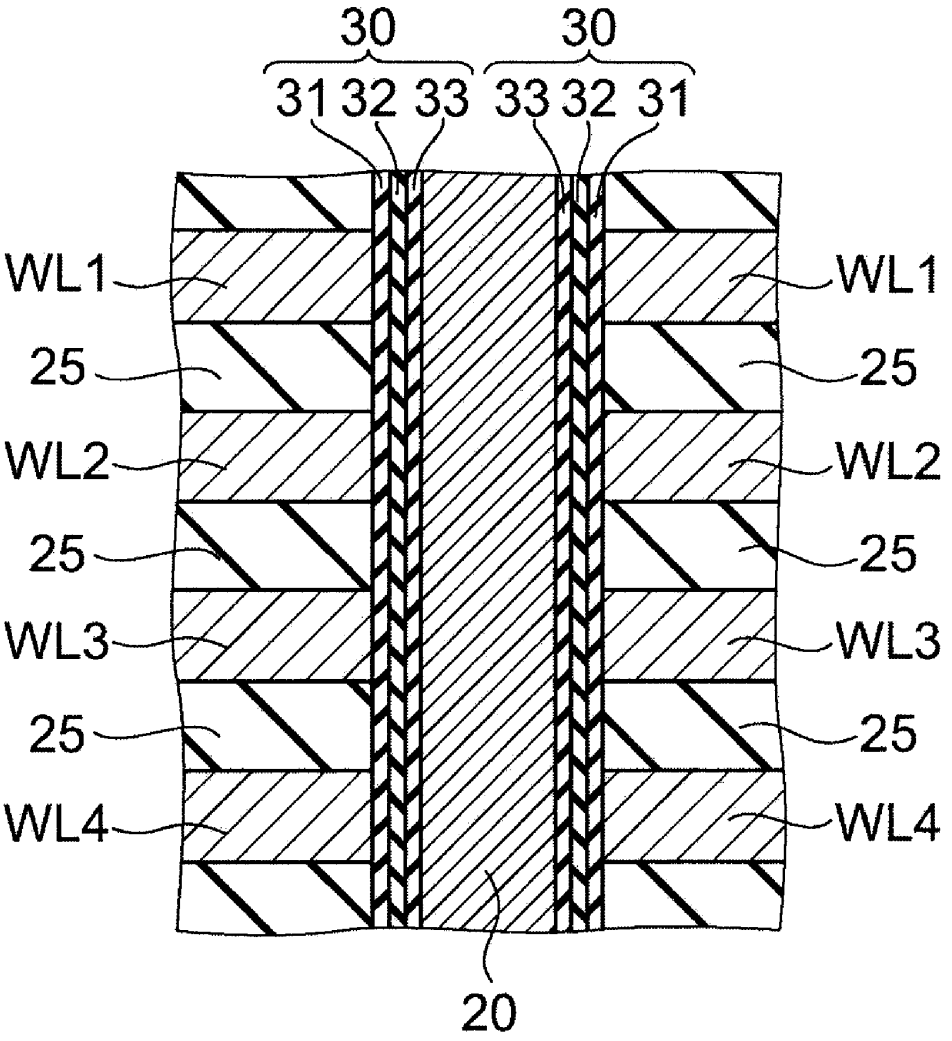

30
30
31 32 33
33 32 31
WL1
WL1
25
25
WL2
WL2
25
25
WL3
WL3
25
25
WL4
WL4
20

FIG. 2

FIG. 3A

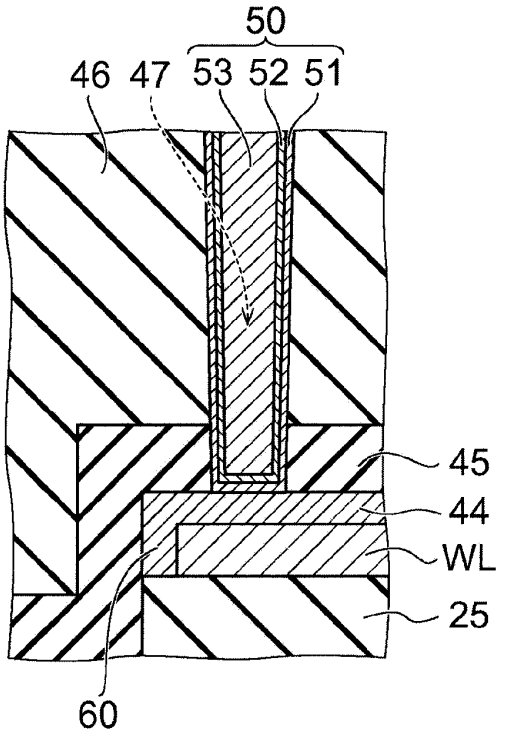
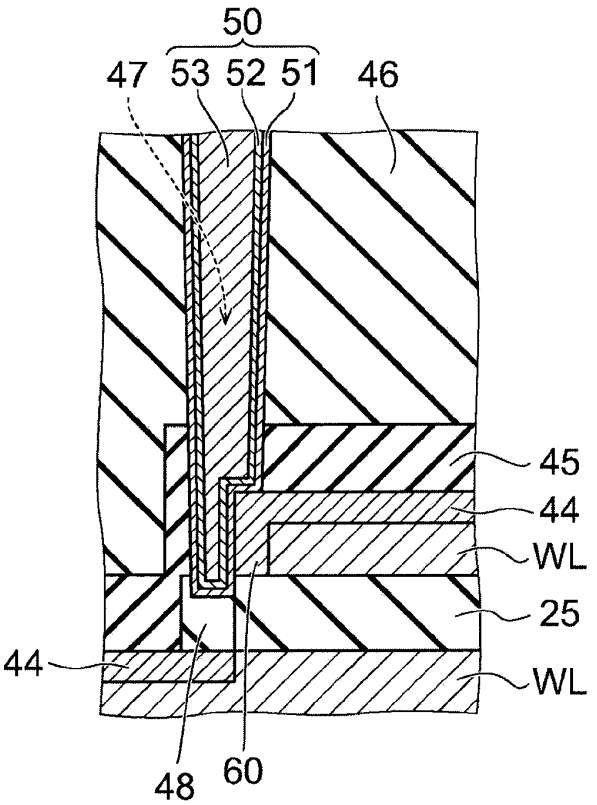

50
46
47
53
52
51
45
44
WL
25
60

FIG. 3B


50
47
53
52
51
46
45
44
WL
25
44
WL
48
60

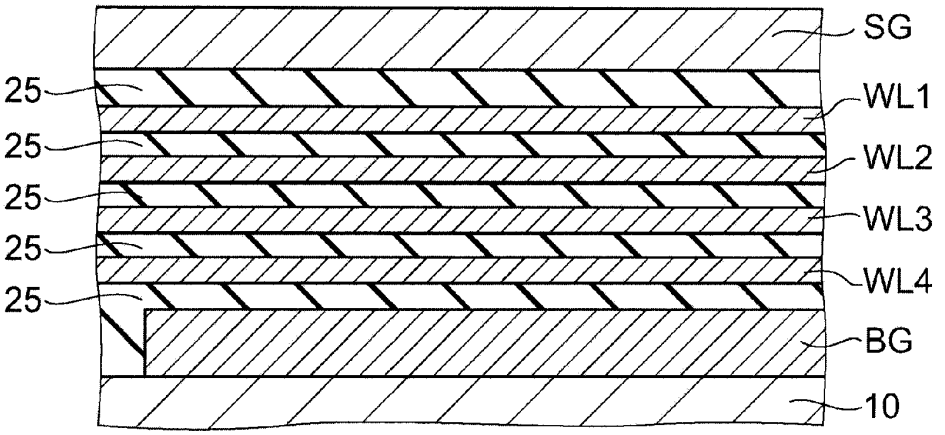

SG
25
WL1
25
WL2
25
WL3
25
WL4
25
BG
10

FIG. 4A

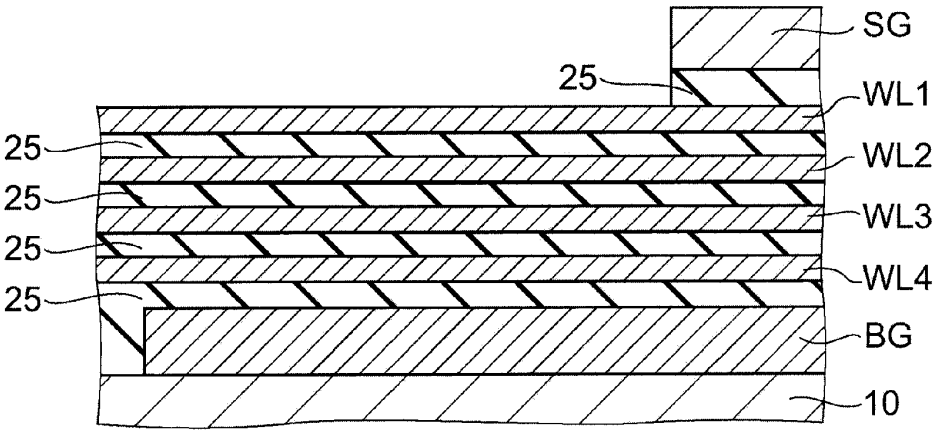

SG
25
WL1
25
WL2
25
WL3
25
WL4
25
BG
10

FIG. 4B

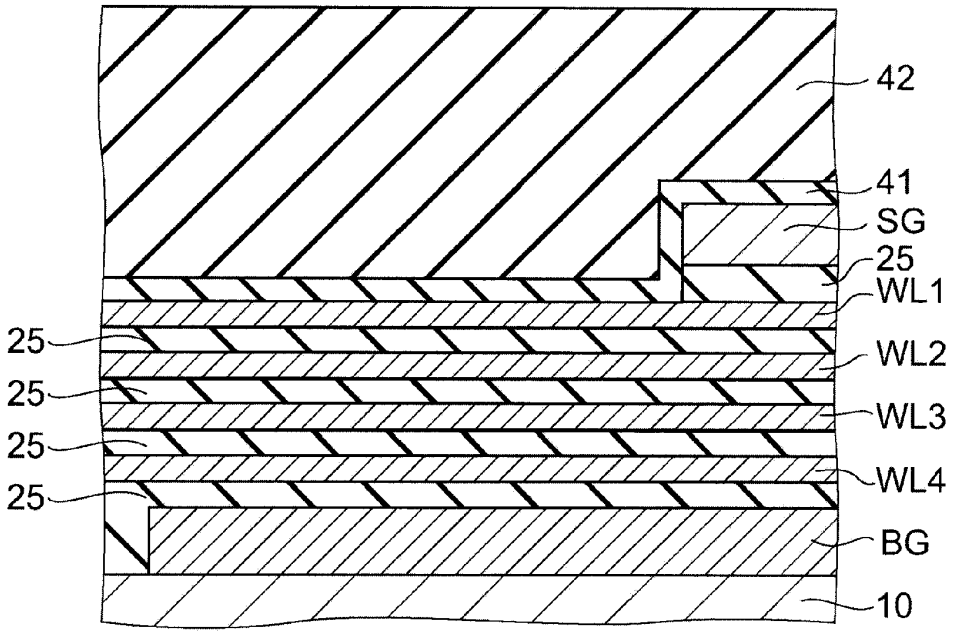

42
41
SG
25
WL1
25
WL2
25
WL3
25
WL4
BG
10

FIG. 5A

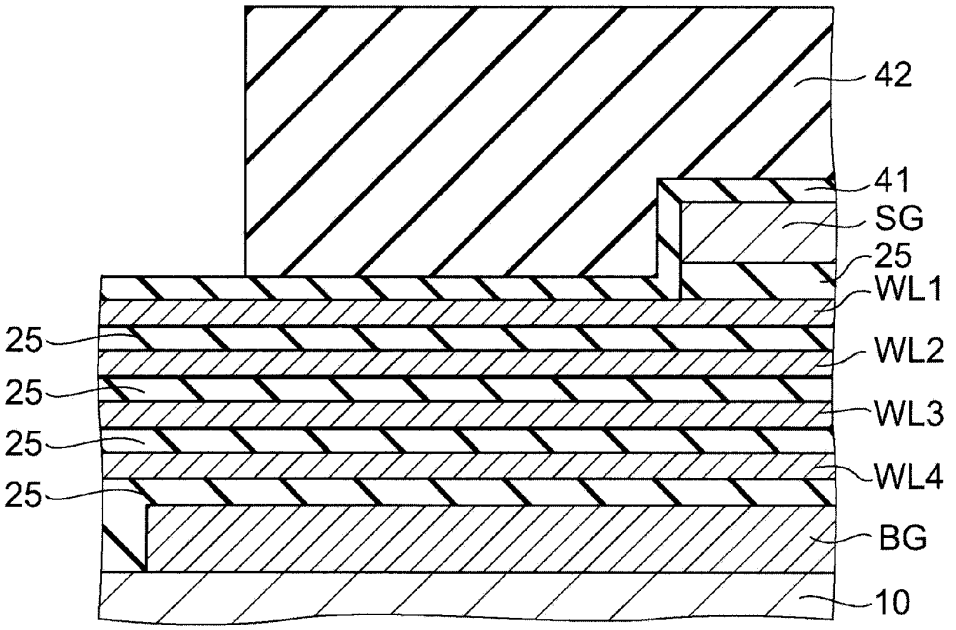

42
41
SG
25
WL1
25
WL2
25
WL3
25
WL4
BG
10

FIG. 5B

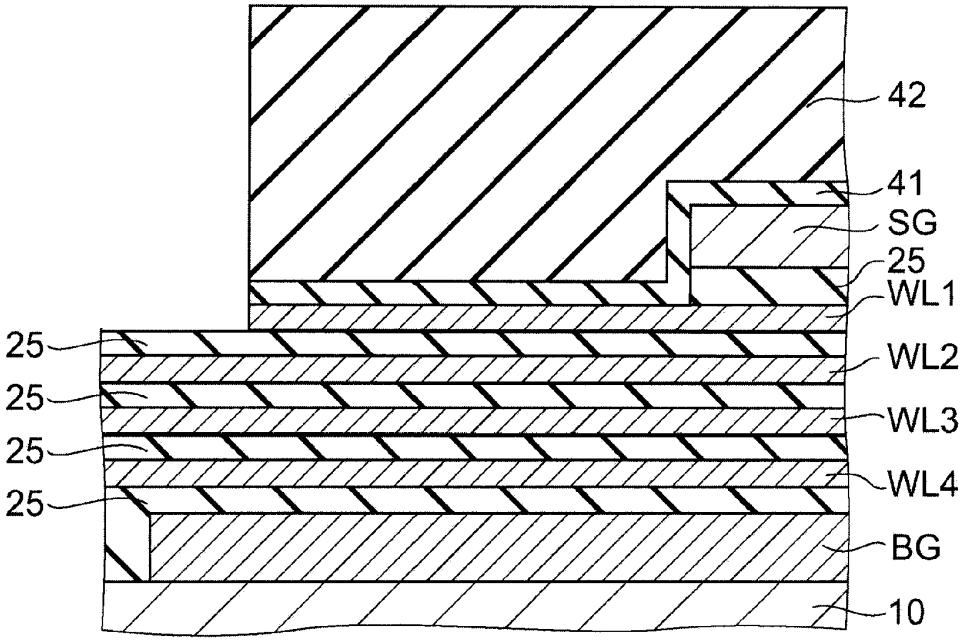

42
41
SG
25
WL1
25
WL2
25
WL3
25
WL4
BG
10

FIG. 6A

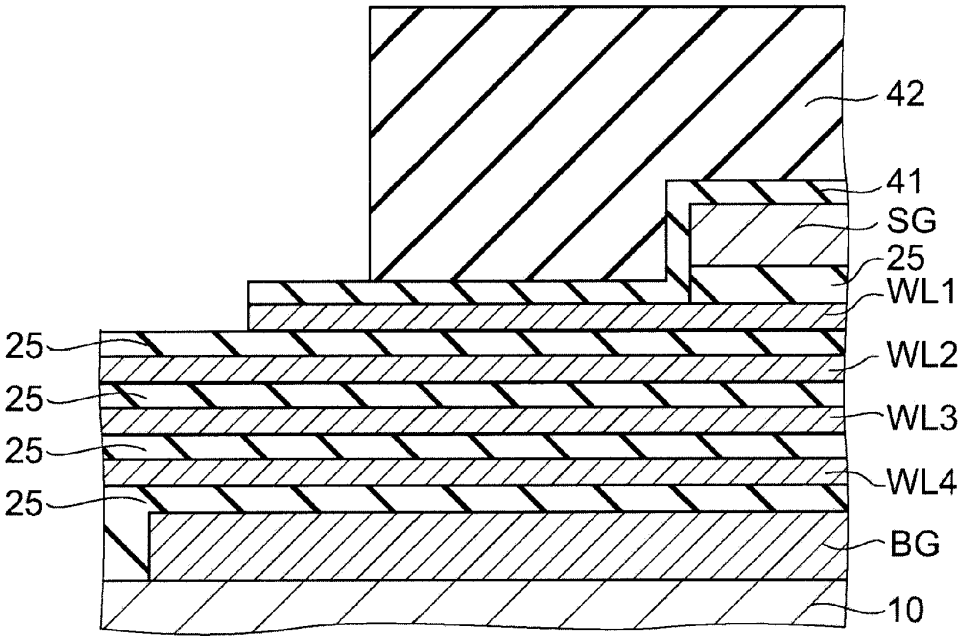

42
41
SG
25
WL1
25
WL2
25
WL3
25
WL4
BG
10

FIG. 6B

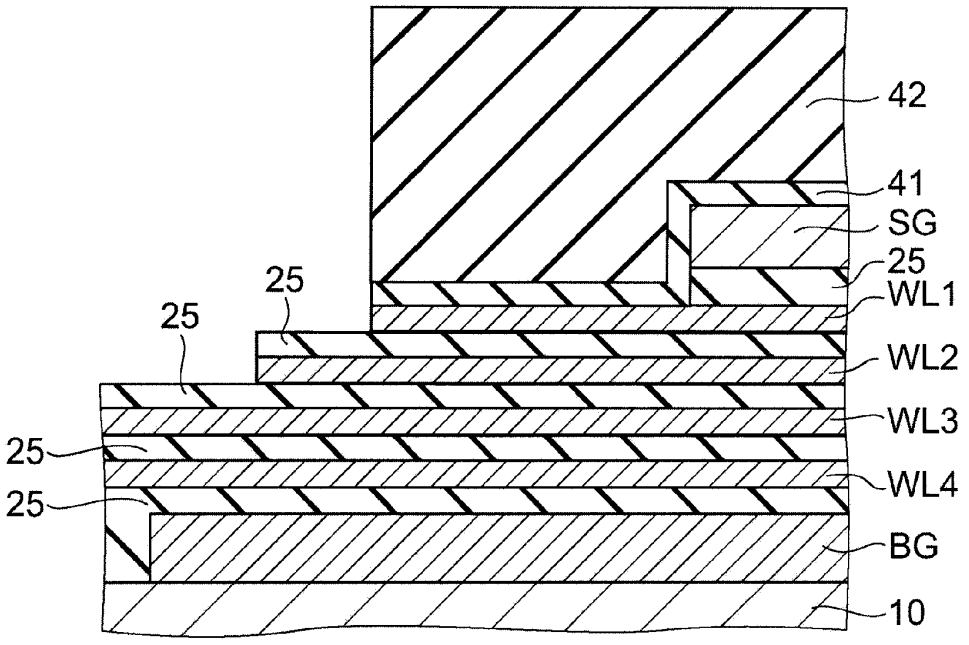

42
41
SG
25
WL1
WL2
WL3
WL4
BG
10
25
25
25
25

FIG. 7A

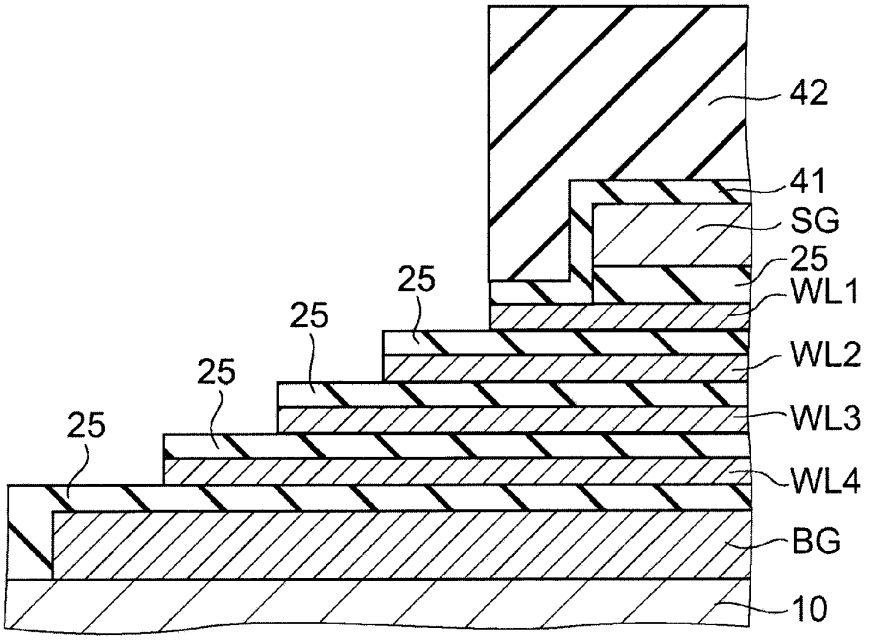

42
41
SG
25
WL1
WL2
WL3
WL4
BG
10
25
25
25
25

FIG. 7B

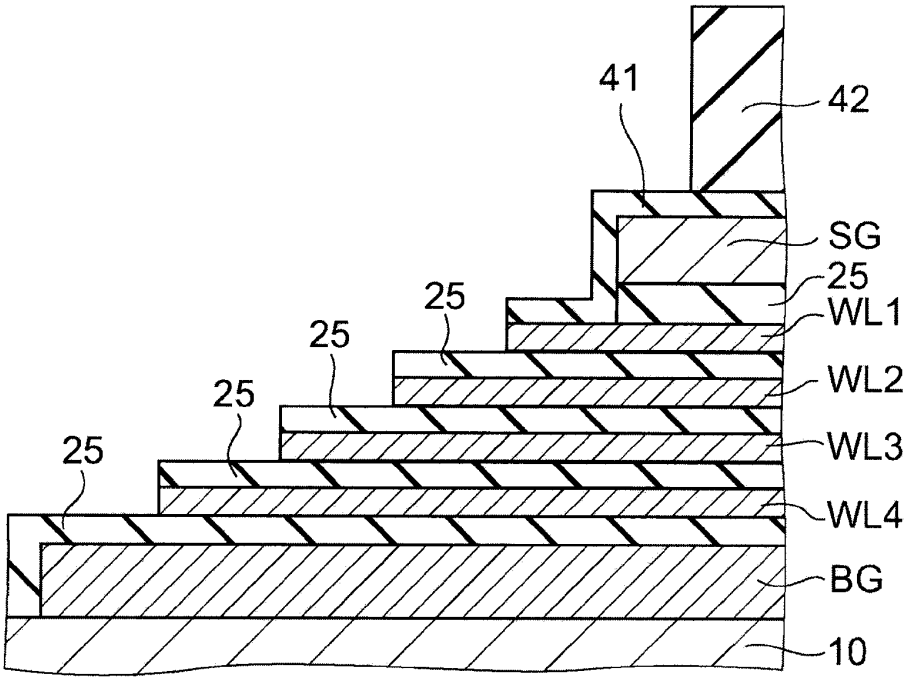

41
42
SG
25
WL1
WL2
WL3
WL4
BG
10
25
25
25
25

FIG. 8A

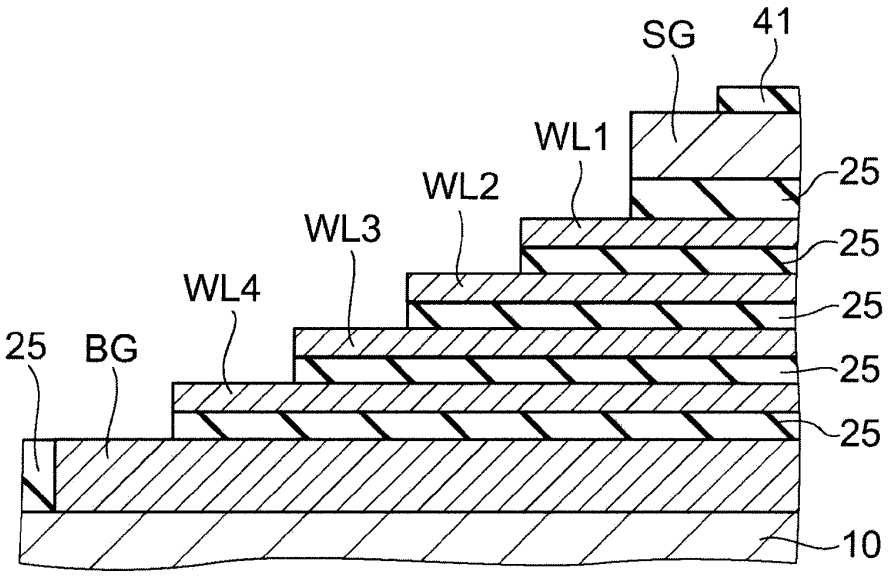

SG
41
WL1
WL2
WL3
WL4
25
BG
10
25
25
25
25
25

FIG. 8B

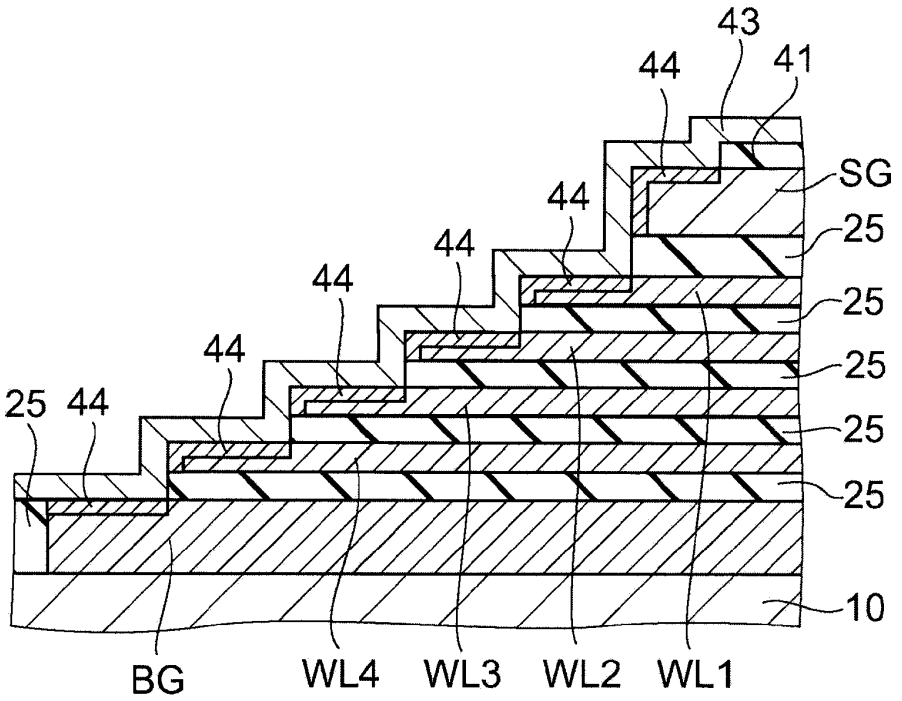

43
44
41
SG
44
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44
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44
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44
25
25
44
25
10
BG
WL4
WL3
WL2
WL1

FIG. 9A

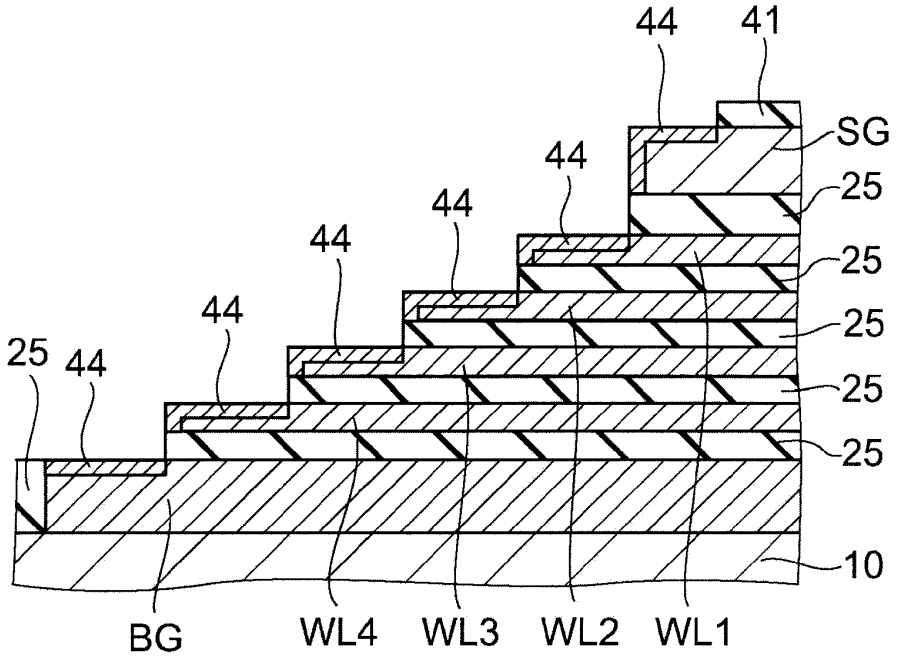

44
41
SG
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44
25
44
25
44
25
25
44
25
10
BG
WL4
WL3
WL2
WL1

FIG. 9B

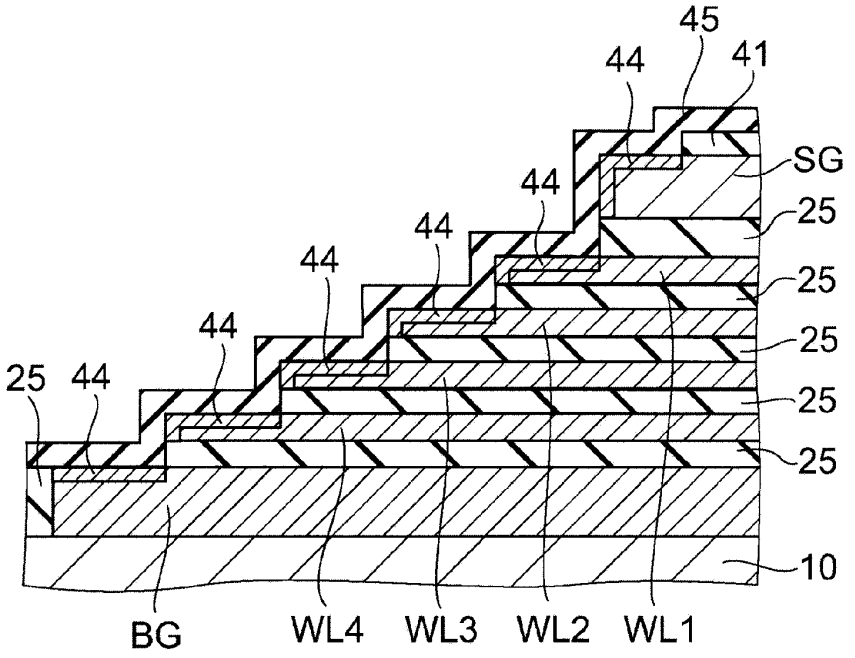


FIG. 10A

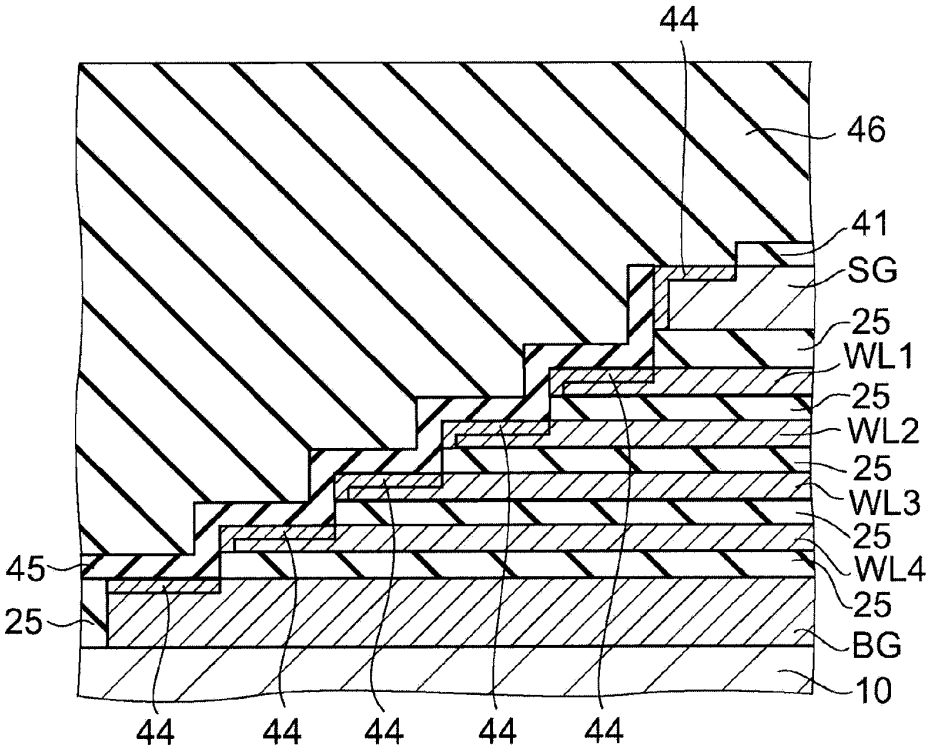


FIG. 10B

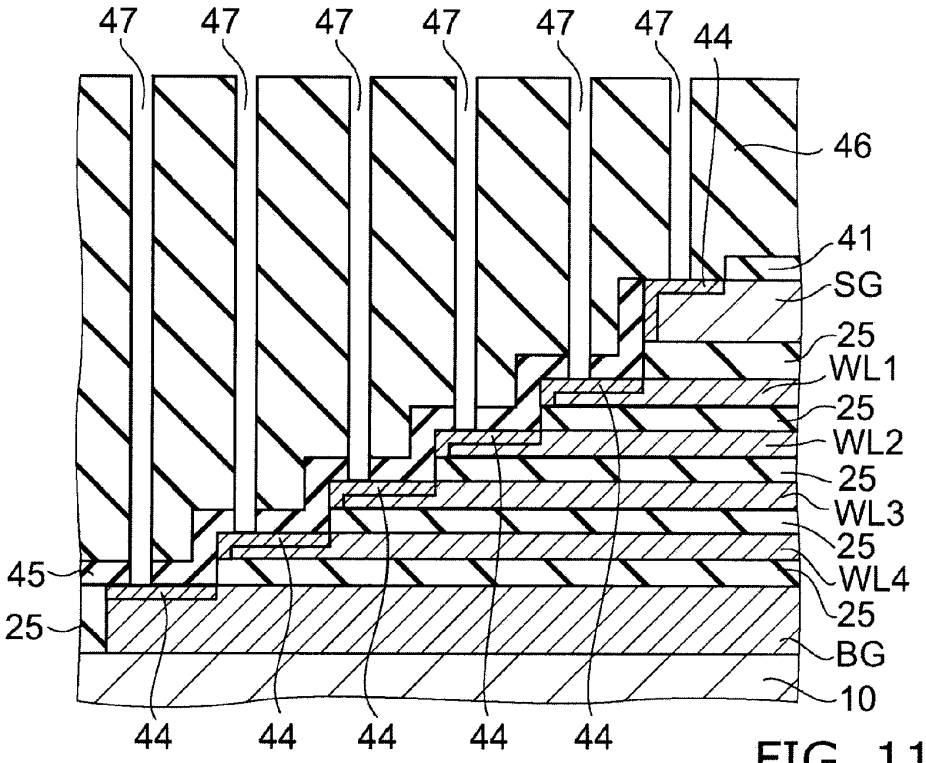


FIG. 11A

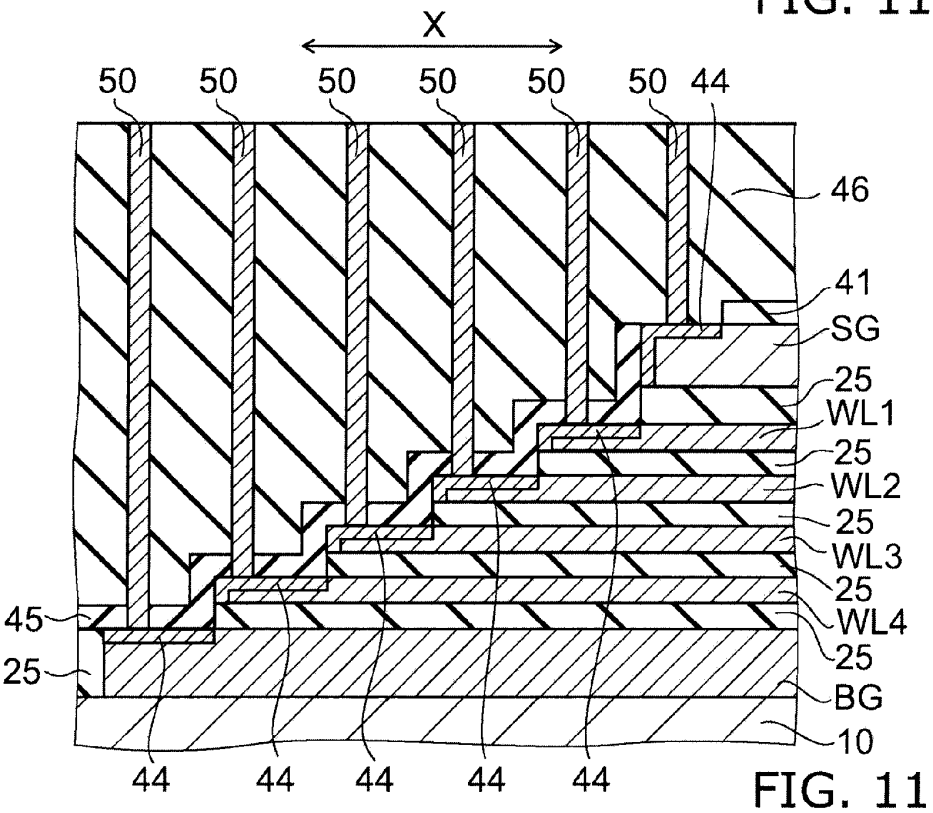


FIG. 11B

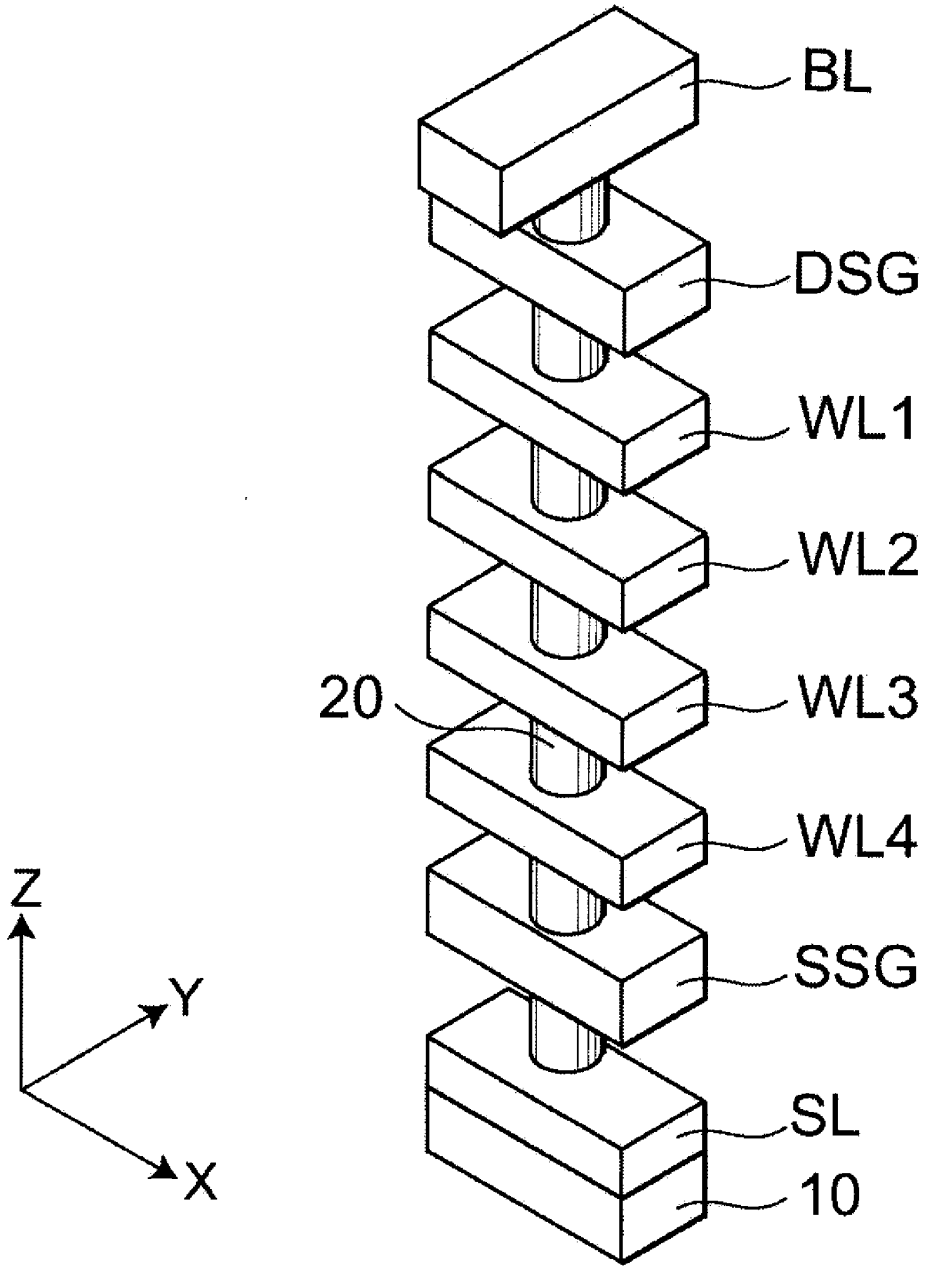


FIG. 12

SEMICONDUCTOR DEVICE MANUFACTURING METHOD AND SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2009-181361, filed on Aug. 4, 2009; the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to a semiconductor device manufacturing method and a semiconductor device.

[0004] 2. Background Art

[0005] A technique for three-dimensionally arranging memory cells is proposed in, for instance, JP-A 2007-180389 (Kokai). In this technique, a plurality of electrode layers functioning as control gates in a memory device are stacked alternately with insulating layers to form a multilayer body, in which silicon pillars are provided via a charge storage layer.

[0006] JP-A 2007-180389 (Kokai) also discloses a staircase structure of electrode layers as a structure for connecting each of a plurality of stacked electrode layers to an upper interconnect. In other words, toward the bottom, each of the electrode layers is made longer. Furthermore, a contact hole reaching each of the electrode layers is formed in an interlayer insulating layer covering the staircase structure, and a contact electrode is buried in the contact hole.

[0007] JP-A 2007-180389 (Kokai) further discloses forming a trench in a multilayer body of a memory cell array region to expose the side surface of each of the electrode layers into the trench, forming a metal film in the trench, and then performing annealing to turn the side surface of each of the electrode layers made of silicon into metal silicide. It is desired to turn also the electrode layers of the staircase-shaped contact portion into metal silicide to reduce resistance. However, the staircase-shaped contact portion is different from the memory cell array in its structure and formation process. Thus, the metal silicidation process for the memory cell array cannot be directly applied thereto.

SUMMARY OF THE INVENTION

[0008] According to an aspect of the invention, there is provided a semiconductor device manufacturing method including: stacking a plurality of electrode layers containing a semiconductor alternately with insulating layers; processing part of a multilayer body of the electrode layers and the insulating layers into a staircase shape and exposing a surface of the staircase-shaped electrode layers; forming a metal film in contact with the exposed electrode layers; reacting the semiconductor of the electrode layers with the metal film to form a metal compound in at least a portion of the electrode layers in contact with the metal film; removing an unreacted portion of the metal film; forming an interlayer insulating layer covering the staircase-shaped electrode layers after removing the unreacted portion of the metal film; forming a plurality of contact holes piercing the interlayer insulating layer, each of the contact holes reaching the metal compound of the electrode layer at a corresponding stage; and providing a plurality of contact electrodes inside the contact holes.

[0009] According to another aspect of the invention, there is provided a semiconductor device including: a multilayer body of a plurality of electrode layers containing a semiconductor stacked alternately with a plurality of insulating layers, part of the multilayer body being processed into a staircase shape, the multilayer body having a metal compound of the semiconductor and a metal formed in at least an upper surface and an end portion of the staircase-shaped electrode layers; an interlayer insulating layer covering the staircase-shaped electrode layers; and a plurality of contact electrodes provided inside a plurality of contact holes piercing the interlayer insulating layer, each of the contact holes reaching the metal compound of the electrode layer at a corresponding stage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. **1** is a schematic view illustrating the configuration of a memory cell array in a semiconductor device according to an embodiment of the invention;

[0011] FIG. **2** is an enlarged cross-sectional view of the main portion in the memory cell array;

[0012] FIGS. **3**A and **3**B are schematic cross-sectional views of the connection structure of an electrode layer and contact electrode in the semiconductor device according to the embodiment of the invention;

[0013] FIGS. **4**A to **11**B are schematic cross-sectional views illustrating a semiconductor device manufacturing method according to the embodiment of the invention; and

[0014] FIG. **12** is a schematic view illustrating another example of a memory string in the semiconductor device according to the embodiment of the invention.

DETAILED DESCRIPTION

[0015] FIG. **1** is a schematic view illustrating the configuration of a memory cell array in a semiconductor device according to an embodiment of the invention. In FIG. **1**, for clarity of illustration, insulating portions are not shown, except insulating films in a memory hole. Although a semiconductor is illustratively silicon in the following embodiments, semiconductors other than silicon may also be used.

[0016] In this specification, for convenience of description, an XYZ orthogonal coordinate system is introduced. In this coordinate system, the two directions parallel to the major surface of a substrate **10** and orthogonal to each other are referred to as X and Y directions, and the direction orthogonal to both the X and Y directions is referred to as a Z direction. A plurality of electrode layers WL**1**-WL**4** are stacked in the Z direction.

[0017] A back gate BG is provided on the substrate **10** via an insulating layer, not shown. The back gate BG is illustratively a silicon layer provided with conductivity by impurity doping. A plurality of electrode layers WL**1**-WL**4** and a plurality of insulating layers, not shown, are alternately stacked on the back gate BG. The number of electrode layers WL**1**-WL**4** is arbitrary, and the case of four layers is illustrated in this embodiment. The electrode layers WL**1**-WL**4** are illustratively silicon layers provided with conductivity by impurity doping.

[0018] The electrode layers WL**1**-WL**4** are divided into a plurality of blocks by trenches extending in the X direction. A drain-side select gate DSG is provided via an insulating layer, not shown, on the uppermost electrode layer WL**1** in one block. The drain-side select gate DSG is illustratively a silicon layer provided with conductivity by impurity doping. A

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source-side select gate SSG is provided via an insulating layer, not shown, on the uppermost electrode layer WL**1** in another block neighboring the former block. The source-side select gate SSG is illustratively a silicon layer provided with conductivity by impurity doping.

[0019] A source line SL is provided on the source-side select gate SSG via an insulating layer, not shown. The source line SL is illustratively a silicon layer provided with conductivity by impurity doping. A plurality of bit lines BL are provided via an insulating layer, not shown, on the source line SL and the drain-side select gate DSG. Each of the bit lines BL extends in the Y direction.

[0020] A plurality of U-shaped memory holes are formed in the aforementioned multilayer body on the substrate **10**. In the block including the drain-side select gate DSG, a memory hole extending in the Z direction is formed through the drain-side select gate DSG and the underlying electrode layers WL**1**-WL**4**. In the block including the source-side select gate SSG, a memory hole extending in the Z direction is formed through the source-side select gate SSG and the underlying electrode layers WL**1**-WL**4**. These memory holes are connected to each other via a memory hole formed in the back gate BG and extending in the Y direction.

[0021] A silicon body **20** is provided as a U-shaped semiconductor layer inside the memory holes. A gate insulating film **35** is formed on the inner wall of the memory hole between the drain-side select gate DSG and the silicon body **20**. A gate insulating film **36** is formed on the inner wall of the memory hole between the source-side select gate SSG and the silicon body **20**. An insulating film **30** is formed on the inner wall of the memory hole between each of the electrode layers WL**1**-WL**4** and the silicon body **20**. The insulating film **30** is formed also on the inner wall of the memory hole between the back gate BG and the silicon body **20**. The insulating film **30** illustratively has an ONO (oxide-nitride-oxide) structure in which a silicon nitride film is sandwiched between a pair of silicon oxide films.

[0022] FIG. **2** shows an enlarged cross section of the portion where the silicon body **20** pierces the electrode layers WL**1**-WL**4** and interlayer insulating layers **25**.

[0023] Between the electrode layers WL**1**-WL**4** and the silicon body **20**, a first insulating film **31**, a charge storage layer **32**, and a second insulating film **33** are provided sequentially from the electrode layers WL**1**-WL**4** side. The first insulating film **31** is in contact with the electrode layers WL**1**-WL**4**, the second insulating film **33** is in contact with the silicon body **20**, and the charge storage layer **32** is provided between the first insulating film **31** and the second insulating film **33**.

[0024] The silicon body **20** functions as a channel, the electrode layers WL**1**-WL**4** function as a control gate, and the charge storage layer **32** functions as a data storage layer for storing charge injected from the silicon body **20**. In other words, at each intersection between the silicon body **20** and the electrode layers WL**1**-WL**4**, a memory cell having a structure, which the control gate surrounds the channel, is formed.

[0025] The semiconductor device according to this embodiment is a nonvolatile semiconductor memory device in which electrical erasure/writing of data can be freely performed, and the stored content can be retained even after power off. For instance, the memory cell is one having a charge trap structure. The charge storage layer **32** includes numerous traps for confining charges (electrons) and is illustratively made of silicon nitride film. The second insulating film **33** is illustratively made of silicon oxide film and serves as a potential barrier when charge is injected from the silicon body **20** into the charge storage layer **32** or when the charge stored in the charge storage layer **32** diffuses into the silicon body **20**. The first insulating film **31** is illustratively made of silicon oxide film and prevents the charge stored in the charge storage layer **32** from diffusing into the electrode layers WL**1**-WL**4**.

[0026] Referring again to FIG. **1**, a gate insulating film **35** is provided between the drain-side select gate DSG and the silicon body **20** piercing the drain-side select gate DSG, and these constitute a drain-side select transistor DST. The upper end portion of the silicon body **20** projected upward from the drain-side select gate DSG is connected to each of the corresponding bit lines BL.

[0027] A gate insulating film **36** is provided between the source-side select gate SSG and the silicon body **20** piercing the source-side select gate SSG, and these constitute a source-side select transistor SST. The upper end portion of the silicon body **20** projected upward from the source-side select gate SSG is connected to the source line SL.

[0028] The back gate BG, the silicon body **20** provided in this back gate BG, and the insulating film **30** between the back gate BG and the silicon body **20** constitute a back gate transistor BGT.

[0029] A memory cell MC**1** with the electrode layer WL**1** serving as a control gate, a memory cell MC**2** with the electrode layer WL**2** serving as a control gate, a memory cell MC**3** with the electrode layer WL**3** serving as a control gate, and a memory cell MC**4** with the electrode layer WL**4** serving as a control gate are provided between the drain-side select transistor DST and the back gate transistor BGT.

[0030] A memory cell MC**5** with the electrode layer WL**4** serving as a control gate, a memory cell MC**6** with the electrode layer WL**3** serving as a control gate, a memory cell MC**7** with the electrode layer WL**2** serving as a control gate, and a memory cell MC**8** with the electrode layer WL**1** serving as a control gate are provided between the back gate transistor BGT and the source-side select transistor SST.

[0031] The drain-side select transistor DST, the memory cells MC**1**-MC**4**, the back gate transistor BGT, the memory cells MC**5**-MC**8**, and the source-side select transistor SST are series connected to constitute one memory string. A plurality of such memory strings are arranged in the X and Y directions, and thereby a plurality of memory cells MC**1**-MC**8** are three-dimensionally provided in the X, Y, and Z directions.

[0032] FIG. **11**B shows a cross-sectional structure of a contact region for connecting each of the silicon layers (drain-side select gate DSG, source-side select gate SSG, electrode layers WL**1**-WL**4**, and back gate BG) to an upper interconnect, not shown. As viewed in the X direction, this contact region is located outside the memory cell array region shown in FIG. **1**.

[0033] In FIG. **11**B, the interlayer insulating layer omitted in FIG. **1** is shown as insulating layers **25**. The select gate SG in FIG. **11**B corresponds to the drain-side select gate DSG or the source-side select gate SSG in FIG. **1**.

[0034] Part of the aforementioned multilayer body is processed into a staircase shape in the contact region. In other word, toward the bottom, each of the silicon layers extends farther outward in the X direction. At least the surface of each of the silicon layers in the staircase structure portion is turned into a metal compound.

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[0035] For instance, titanium silicide **44** is formed in the upper surface of the back gate BG at the lowermost stage. Titanium silicide **44** is formed in the upper surface and end surface of the electrode layer WL**4** at the next higher stage. Titanium silicide **44** is formed in the upper surface and end surface of the electrode layer WL**3** at the next higher stage. Titanium silicide **44** is formed in the upper surface and end surface of the electrode layer WL**2** at the next higher stage. Titanium silicide **44** is formed in the upper surface and end surface of the electrode layer WL**1** at the next higher stage. Titanium silicide **44** is formed in the upper surface and end surface of the select gate SG at the next higher stage.

[0036] Here, the silicon layer at each stage may be turned into titanium silicide not only in its upper surface and end surface, but also throughout the thickness.

[0037] The staircase structure portion is covered with a stopper layer **45**, and an interlayer insulating layer **46** is provided on the stopper layer **45**. For instance, the stopper layer **45** is made of silicon nitride, and the interlayer insulating layer **46** is made of silicon oxide.

[0038] A plurality of contact holes are formed in the interlayer insulating layer **46** and the stopper layer **45**, and a contact electrode **50** is provided in each of the contact holes.

[0039] FIG. **3**A is an enlarged cross-sectional view of the contact electrode **50** provided on the electrode layers WL**1**-WL**4**, for instance. In FIG. **3**A, the electrode layers WL**1**-WL**4** are generically shown as an electrode layer WL.

[0040] A contact hole **47** pierces the interlayer insulating layer **46** and the stopper layer **45** and reaches the titanium silicide **44** of the electrode layer WL. A first barrier film **51** is provided on the inner wall (sidewall and bottom) of the contact hole **47**, a second barrier film **52** is provided inside the first barrier film **51**, a conductive material **53** is buried inside the second barrier film **52**, and these constitute the contact electrode **50**. For instance, the first barrier film **51** is a titanium film, the second barrier film **52** is a titanium nitride film, and the conductive material **53** is tungsten.

[0041] The electrode layer WL is connected to an upper interconnect, not shown, via the contact electrode **50**. The electrode layer WL is illustratively a silicon layer, and titanium silicide **44** is formed in the portion of the electrode layer WL in contact with the contact electrode **50**. Hence, the contact resistance to the contact electrode **50** can be reduced.

[0042] The contact hole **47** is mostly filled with the conductive material **53**, which is a material having good filling capability, such as tungsten. Thus, the conductive material **53** can be sufficiently formed also at the bottom of the contact hole **47** particularly with high aspect ratio. Furthermore, this can avoid generation of voids and suppress the increase of resistance.

[0043] Furthermore, the first barrier film **51** and the second barrier film **52** serve to prevent the diffusion of tungsten into the interlayer insulating layer **46** and the stopper layer **45**. This can prevent short circuit between adjacent contact electrodes **50** due to diffusion of tungsten into the interlayer insulating layer **46** and the stopper layer **45**.

[0044] Here, the first barrier film **51** and the second barrier film **52** at the bottom of the contact hole **47** may be omitted. In other words, before the conductive material **53** is buried, the first barrier film **51** and the second barrier film **52** at the bottom of the contact hole **47** may be removed by RIE (Reactive Ion Etching).

[0045] The contact electrode **50** connected to the back gate BG and the contact electrode **50** connected to the select gate SG are configured likewise. The back gate BG and the select gate SG are each also electrically connected to an upper interconnect via a corresponding contact electrode **50**.

[0046] Next, a method for forming a staircase-shaped contact structure portion in the semiconductor device according to this embodiment is described with reference to FIGS. **4**A to **11**B.

[0047] First, a multilayer body shown in FIG. **4**A is formed. Specifically, a back gate BG is formed on a substrate **10** and patterned. Then, insulating layers **25** and electrode layers WL**1**-WL**4** are alternately stacked on the back gate BG. Furthermore, a select gate SG to serve as the aforementioned drain-side select gate DSG or source-side select gate SSG is formed on the uppermost insulating layer **25**.

[0048] The back gate BG, the electrode layers WL**1**-WL**4**, and the select gate SG are illustratively silicon layers provided with conductivity by impurity doping, and the insulating layer **25** is a silicon oxide layer. These are formed illustratively by the CVD (chemical vapor deposition) process.

[0049] The formation of this multilayer body is followed by processes for forming memory cells MC**1**-MC**8**, drain-side select transistor DST, source-side select transistor SST, back gate transistor BGT and the like in the memory cell array region.

[0050] Subsequently, in the region where the staircase-shaped contact structure is to be formed, a resist mask, not shown, is used to perform patterning by selectively removing the select gate SG and the underlying insulating layer **25** as shown in FIG. **4**B.

[0051] Subsequently, as shown in FIG. **5**A, an insulating layer (such as a silicon oxide layer) **41** covering the upper surface of the multilayer body is formed, and then a resist film **42** is formed on the insulating layer **41**.

[0052] Next, a mask, not shown, is used to perform lithography and development on the resist film **42**. Thus, as shown in FIG. **5**B, the resist film **42** is patterned so that its end is located at a desired position.

[0053] Next, the resist film **42** is used as a mask to perform RIE, thereby removing the portion of the insulating layer **41** and the underlying electrode layer WL**1** exposed from the resist film **42** as shown in FIG. **6**A.

[0054] Next, resist slimming for reducing the planar size of the resist film **42** is performed. By this resist slimming, as shown in FIG. **6**B, part of the surface of the insulating layer **41** is newly exposed.

[0055] Then, the slimmed resist film **42** is used as a mask to perform RIE. As shown in FIG. **7**A, this removes the insulating layer **25** and the underlying electrode layer WL**2**, which were located below the electrode layer WL**1** removed by the previous etching, and also removes the insulating layer **41** and the underlying electrode layer WL**1** exposed from the resist film **42** in the adjacent portion.

[0056] Subsequently, likewise, the process for slimming the resist film **42** and the process for etching one insulating layer and one underlying electrode layer in a portion not covered with and exposed from the slimmed resist film **42** are repeated. This results in a staircase structure shown in FIG. **7**B.

[0057] Subsequently, as shown in FIG. **8**A, the resist film **42** is further slimmed, and the remaining resist film **42** is used as a mask to perform etching. This removes the insulating layers **41** and **25** covering the surface of the staircase structure

portion. Thus, as shown in FIG. **8**B, the select gate SG, the electrode layers WL**1**-WL**4**, and the back gate BG are partly exposed.

[0058] More specifically, at the lowermost stage, the upper surface of the back gate BG is exposed. At the next higher stage, the upper surface and end surface of the electrode layer WL**4** are exposed. At the next higher stage, the upper surface and end surface of the electrode layer WL**3** are exposed. At the next higher stage, the upper surface and end surface of the electrode layer WL**2** are exposed. At the next higher stage, the upper surface and end surface of the electrode layer WL**1** are exposed. At the next higher stage, the upper surface and end surface of the select gate SG are exposed.

[0059] Next, as shown in FIG. **9**A, the staircase structure portion is covered with a metal film **43**. The metal film **43** is formed illustratively by a sputtering process. This embodiment is described by taking titanium (Ti) as an example of the material of the metal film **43**. However, besides titanium, it is also possible to use other materials such as cobalt (Co), nickel (Ni), tantalum (Ta), platinum (Pt), palladium (Pd) and tungsten (W).

[0060] After the metal film **43** is formed, annealing (heat treatment) is performed to cause silicon contained in the select gate SG, the electrode layers WL**1**-WL**4**, and the back gate BG to react with titanium contained in the metal film **43**. Thus, titanium silicide **44** is formed in the select gate SG, the electrode layers WL**1**-WL**4**, and the back gate BG, at least in the portion in contact with the metal film **43**.

[0061] Subsequently, the unreacted portion of the metal film **43** is removed by wet processing. Thus, as shown in FIG. **9**B, the titanium silicide **44** at each stage is exposed.

[0062] Next, as shown in FIG. **10**A, a stopper layer **45** is formed so as to cover the staircase structure portion. The stopper layer **45** is illustratively made of silicon nitride. Subsequently, the stopper layer **45** above the select gate SG is selectively removed. Then, as shown in FIG. **10**B, an interlayer insulating layer **46** is formed on the stopper layer **45** and the select gate SG. The interlayer insulating layer **46** is illustratively made of silicon oxide.

[0063] Subsequently, the upper surface of the interlayer insulating layer **46** is planarized. Then, a mask illustratively made of organic film, not shown, is formed thereon and used as a mask to selectively etch the interlayer insulating layer **46** and the stopper layer **45**.

[0064] Thus, as shown in FIG. **11**A, a plurality of contact holes **47** are formed in the interlayer insulating layer **46** and the stopper layer **45**. The plurality of contact holes **47** have different depths from the upper surface of the interlayer insulating layer **46**. Each of the contact holes **47** pierces the interlayer insulating layer **46** and the stopper layer **45** and reaches the titanium silicide **44** formed in the upper surface of the corresponding one of the select gate SG, the electrode layers WL**1**-WL**4**, and the back gate BG.

[0065] The plurality of contact holes **47** are formed simultaneously and collectively by RIE. Each of the silicon layers (select gate SG, electrode layers WL**1**-WL**4**, and back gate BG) in the contact region is processed into a staircase shape with the lower layers being longer. Hence, the plurality of contact holes **47** reaching the respective silicon layers can be collectively formed by the same etching process, and it achieves efficient processing.

[0066] Here, the stopper layer **45** made of silicon nitride functions as an etching stopper in etching the interlayer insulating layer **46** made of silicon oxide, and the titanium silicide **44** in the surface of each stage functions as an etching stopper in etching the stopper layer **45**.

[0067] After the contact holes **47** are formed, a contact electrode **50** is provided inside the contact hole **47** as shown in FIG. **11**B. Specifically, as shown in FIG. **3**A, a first barrier film (such as titanium film) **51** is first formed on the inner wall of the contact hole **47**, a second barrier film (such as titanium nitride film) **52** is formed inside the first barrier film **51**, and a conductive material (such as tungsten) **53** is buried inside the second barrier film **52**.

[0068] Here, as a comparative example, metal silicidation of the portion of each of the silicon layers (select gate SG, electrode layers WL**1**-WL**4**, and back gate BG) in contact with the contact electrode **50** may be performed by previously forming contact holes **47** and then turning the silicon layer surface exposed to the bottom of the contact hole **47** into metal silicide.

[0069] More specifically, after contact holes **47** are formed, a metal film is formed in the contact hole **47**, including at the bottom of the contact hole **47**, and annealed. Thus, the silicon layer surface in contact with the metal film at the bottom of the contact hole **47** is turned into metal silicide. Then, after the unreacted metal is removed, a contact electrode **50** is buried in the contact hole **47**.

[0070] However, in this case, during RIE for forming contact holes **47**, ions are implanted into the silicon layer surface exposed to the bottom of the contact hole **47**. There is concern that this may modify the surface and interfere with metal silicidation reaction. Furthermore, the metal film may fail to be formed sufficiently at the bottom of a deep contact hole **47** with high aspect ratio, as compared with a shallow contact hole **47**. This also causes concern about variation in the amount of metal silicide produced at the bottom depending on the depth of the contact hole **47**. In other words, the taller electrode layer tends to have higher contact resistance to the contact electrode **50**, which may consequently lead to variation in the characteristics of memory cells with the electrode layers WL**1**-WL**4** serving as control gates.

[0071] In contrast, in this embodiment, as described above with reference to FIG. **9**A, in the phase in which the staircase structure portion is exposed, the metal film **43** is formed, and the surface of each of the silicon layers is turned into metal silicide. Hence, a sufficient amount of metal can be supplied also to lower stages, and the thickness of the metal film **43** can be made nearly uniform between the upper stage side and the lower stage side. This can suppress the amount of produced metal silicide from varying between the upper stage side and the lower stage side. Hence, this embodiment can suppress the contact resistance to the contact electrode **50** from varying among the electrode layers WL**1**-WL**4**, and consequently suppress variation in the characteristics of memory cells with the electrode layers WL**1**-WL**4** serving as control gates.

[0072] Furthermore, in this embodiment, because the silicon layer is turned into metal silicide before undergoing RIE for forming contact holes, the metal silicidation reaction can be favorably facilitated, and it achieves lower resistance.

[0073] In the aforementioned comparative example, when the stopper layer **45** made of silicon nitride is etched, the silicon layer not yet turned into metal silicide functions as an etching stopper. However, the etching selection ratio between silicon nitride and silicon is not significantly high. Hence, particularly when the electrode layer is thinned with the increase in the number of layers, etching may proceed through an electrode layer located at a shallow position, and

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the contact hole may reach another electrode layer below the corresponding electrode layer. Then, two different electrode layers are connected to one contact electrode and short-circuited to each other.

[0074] In contrast, in this embodiment, when the stopper layer **45** is etched, the metal silicide (such as titanium silicide **44**) functions as an etching stopper. The etching selection ratio between silicon nitride and metal silicide is higher than the etching selection ratio between silicon nitride and silicon. Hence, progress of etching can be reliably stopped by the titanium silicide **44** formed in the upper surface of each of the electrode layers WL**1**-WL**4**. This can prevent the contact holes **47** from punching through the corresponding electrode layers WL**1**-WL**4**.

[0075] If each of the electrode layers WL**1**-WL**4** is etched, the contact electrodes **50** are brought into contact with the electrode layers WL**1**-WL**4** not only on the bottom surface but also on the side surface. If the amount of etching of the electrode layers WL**1**-WL**4** is varied, the contact area, or contact resistance, between each of the electrode layers WL**1**-WL**4** and the contact electrodes **50** is varied, which may lead to characteristics variation among memory cells.

[0076] In this embodiment, when the stopper layer **45** is etched, the amount of etching of each of the electrode layers WL**1**-WL**4** from the upper surface can be reduced because titanium silicide **44** is resistant to etching. Consequently, variation in the contact area, or contact resistance, between each of the electrode layers WL**1**-WL**4** and the contact electrodes **50** can be suppressed. This also contributes to the suppression of characteristics variation among memory cells.

[0077] Furthermore, as shown in FIG. **9**A, because the metal film **43** is formed in the situation where the staircase structure is yet to be covered with the stopper layer **45** and the interlayer insulating layer **46**, not only the upper surface but also the end surface of each of the electrode layers WL**1**-WL**4** is in contact with the metal film **43**. Hence, as shown in FIG. **3**A, titanium silicide **44** is formed also in the end portion **60** of the electrode layer WL.

[0078] Thus, even if the contact hole **47** is displaced from above the electrode layer WL, the side portion of the contact electrode **50** can serve to ensure contact with the end portion **60** of the electrode layer WL as shown in FIG. **3**B. This can suppress the decrease of the contact area therebetween.

[0079] In this case, by suitably controlling the etching time of the stopper layer **45**, the portion of the contact hole **47** displaced from the electrode layer WL to be connected can be prevented from reaching another electrode layer WL therebelow.

[0080] Alternatively, as shown in FIG. **3**B, it is also useful to provide, below the stopper layer **45**, a stopper layer **48** made of a material (such as silicon oxide) different from silicon nitride constituting the stopper layer **45**. This stopper layer **48** is provided near the step difference between each electrode layer WL and another electrode layer WL immediately thereabove. For instance, after the staircase structure portion is covered with the stopper layer **48**, the stopper layer **48** can be left only on the end sidewall of each stage by anisotropic etch back.

[0081] In each electrode layer WL, the contact hole **47** is aligned with the position nearer to the end portion **60** than the portion provided with the stopper layer **48**, and the stopper layer **45** is directly provided at that position without the intermediary of the stopper layer **48**. In this structure, when the stopper layer **45** is etched, even if the contact hole **47** is displaced from the target electrode layer WL as shown in FIG. **3**B, the stopper layer **48** made of a material different from that of the stopper layer **45** underlies the stopper layer **45** in the displaced portion. Hence, etching of the displaced portion can be stopped by the stopper layer **48**, and the contact hole **47** can be reliably prevented from reaching another electrode layer WL therebelow.

[0082] The embodiments of the invention have been described with reference to examples. However, the invention is not limited thereto but can be variously modified within the spirit of the invention.

[0083] The configuration of the memory string is not limited to the U-shape but may be an I-shape as shown in FIG. **12**, which shows only the conductive portions and omits the insulating portions. In this structure, a source line SL is provided on a substrate **10**, a source-side select gate (or lower select gate) SSG is provided thereon, electrode layers WL**1**-WL**4** are provided thereon, and a drain-side select gate (or upper select gate) DSG is provided between the uppermost electrode layer WL**1** and a bit line BL.

[0084] Furthermore, the insulating film structure between the electrode layer and the silicon body is not limited to the ONO structure but can illustratively be a two-layer structure of a charge storage layer and a gate insulating film.

1. A semiconductor device manufacturing method comprising:
- stacking a plurality of electrode layers containing a semiconductor alternately with insulating layers;
- processing part of a multilayer body of the electrode layers and the insulating layers into a staircase shape and exposing a surface of the staircase-shaped electrode layers;
- forming a metal film in contact with the exposed electrode layers;
- reacting the semiconductor of the electrode layers with the metal film to form a metal compound in at least a portion of the electrode layers in contact with the metal film;
- removing an unreacted portion of the metal film;
- forming an interlayer insulating layer covering the staircase-shaped electrode layers after removing the unreacted portion of the metal film;
- forming a plurality of contact holes piercing the interlayer insulating layer, each of the contact holes reaching the metal compound of the electrode layer at a corresponding stage; and
- providing a plurality of contact electrodes inside the contact holes.

2. The method according to claim **1**, wherein the processing part of the multilayer body into the staircase shape is performed by repetition of reducing planar size of a resist film formed above the multilayer body, and etching one of the insulating layers and one of the electrode layers in a portion not covered with the resist film and exposed from the resist film.

3. The method according to claim **1**, wherein
- the semiconductor is silicon, and
- the metal compound formed in the electrode layers is a metal silicide.

4. The method according to claim **1**, wherein the metal compound is formed in an upper surface and an end portion of the staircase-shaped electrode layers.

5. The method according to claim **1**, wherein the unreacted portion is removed by wet processing.

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6. The method according to claim 1, wherein the staircase-shaped electrode layers are covered with a stopper layer made of a material different from a material of the interlayer insulating layer after removing the unreacted portion of the metal film, and the interlayer insulating layer is formed on the stopper layer.

7. The method according to claim 1, wherein the plurality of contact holes having different depths from an upper surface of the interlayer insulating layer are collectively formed after planarizing the upper surface of the interlayer insulating layer.

8. The method according to claim 1, wherein the providing the contact electrodes includes:

forming a conductive barrier film on inner walls of the contact holes; and

burying a conductive material inside the barrier film in the contact holes.

9. The method according to claim 8, wherein the forming the barrier film includes:

forming a titanium film on the inner walls of the contact holes; and

forming a titanium nitride film inside the titanium film in the contact holes.

10. The method according to claim 1, further comprising:

forming a memory hole in a memory cell array region in the multilayer body, the memory hole piercing the plurality of electrode layers and insulating layers;

forming an insulating film including a charge storage layer on an inner wall of the memory hole; and

forming a semiconductor layer inside the insulating film in the memory hole.

11. The method according to claim 10, wherein the forming the insulating film includes:

forming a first silicon oxide film on the inner wall of the memory hole;

forming a silicon nitride film as the charge storage layer inside the first silicon oxide film in the memory hole; and

forming a second silicon oxide film inside the silicon nitride film in the memory hole.

12. A semiconductor device comprising:

a multilayer body of a plurality of electrode layers containing a semiconductor stacked alternately with a plurality of insulating layers, part of the multilayer body being processed into a staircase shape, the multilayer body having a metal compound of the semiconductor and a metal formed in at least an upper surface and an end portion of the staircase-shaped electrode layers;

an interlayer insulating layer covering the staircase-shaped electrode layers; and

a plurality of contact electrodes provided inside a plurality of contact holes piercing the interlayer insulating layer, each of the contact holes reaching the metal compound of the electrode layer at a corresponding stage.

13. The device according to claim 12, wherein each of the contact electrodes is in contact with the upper surface and the end portion of the electrode layer.

14. The device according to claim 12, wherein

the semiconductor is silicon, and

the metal compound is a metal silicide.

15. The device according to claim 12, further comprising:

a stopper layer interposed between the metal compound and the interlayer insulating layer and made of a material different from a material of the interlayer insulating layer.

16. The device according to claim 12, wherein each of the contact electrodes includes:

a conductive barrier film formed on an inner wall of each of the contact holes; and

a conductive material provided inside the barrier film in each of the contact holes.

17. The device according to claim 16, wherein

the barrier film includes a titanium film formed on the inner wall of each of the contact holes and a titanium nitride film formed inside the titanium film in each of the contact holes, and

the conductive material is tungsten.

18. The device according to claim 12, further comprising:

an insulating film including a charge storage layer and formed on an inner wall of a memory hole, the memory hole piercing the plurality of electrode layers and insulating layers in a memory cell array region in the multilayer body; and

a semiconductor layer provided inside the insulating film in the memory hole.

19. The device according to claim 18, wherein the insulating film includes:

a first silicon oxide film formed on the inner wall of the memory hole;

a silicon nitride film formed as the charge storage layer inside the first silicon oxide film in the memory hole; and

a second silicon oxide film formed inside the silicon nitride film in the memory hole.

20. The device according to claim 18, wherein the memory hole is formed in a U-shape to connect a pair of holes piercing the multilayer body below the multilayer body.

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