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Application Number: 16126956 Document Date: 09/10/2018

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Form Revision Date: August 26, 2013

PTO/AIA/15 (10-17)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	4123.0460002
First Named Inventor	Zhenyu LU
Title	STAIRCASE STRUCTURE FOR MEMORY DEVICE
Priority Mail Express® Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. ☐ **Applicant asserts small entity status.** See 37 CFR 1.27
3. ☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. ☑ **Specification** [*Total Pages* 20] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. ☑ **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 10]
6. **Inventor's Oath or Declaration** [*Total Pages* ____] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. ☐ Newly executed (original or copy)
   b. ☐ A copy from a prior application (37 CFR 1.63(d))
7. ☑ **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   ☐ Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PAPERS

10. ☐ **Assignment Papers** (cover sheet & document(s))
    Name of Assignee: Yangtze Memory Technologies Co., Ltd.
11. ☐ **37 CFR 3.73(c) Statement** (*when there is an assignee*) ☑ **Power of Attorney**
12. ☐ **English Translation Document** (*if applicable*)
13. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
14. ☐ **Preliminary Amendment**
15. ☐ **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. ☐ **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. ☐ **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. ☐ **Other:** ____

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 26111 **OR** ☐ Correspondence address below

Name	Donald J. Featherstone				
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Donald J. Featherstone/	Date	9/10/18
Name (Print/Type)	Donald J. Featherstone	Registration No. (Attorney/Agent)	33,876

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: LU *et al.*	Confirmation No.: *To Be Assigned*
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: *To Be Assigned*
Application No.: *To Be Assigned*	Examiner: *To Be Assigned*
(*Continuation of Appl. No. PCT/CN2018/098962; Filed: August 6, 2018*)	Atty. Docket: 4123.0460002
Filed: *Herewith*	

Title: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**

Authorization to Treat a Reply as Incorporating an Extension of Time Under 37 C.F.R. § 1.136(a)(3)

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 9/10/18

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9964817_1.docx

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0460002
	Application Number	
Title of Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Zhenyu		LU	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.
Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone

City	Wuhan, Hubei	State/Province	
Postal Code		**Country** [i]	CN

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jun		CHEN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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Inventor 3 Remove

Legal Name

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0460002
	Application Number	
Title of Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Xiaowang		DAI	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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Postal Code		**Country** [i]	CN

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jifeng		ZHU	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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Postal Code		**Country** [i]	CN

Inventor 5 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Qian		TAO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0460002
	Application Number	
Title of Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

Inventor 6 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Yu Ru		HUANG	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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City	Wuhan, Hubei	State/Province	
Postal Code		**Country** [i]	CN

Inventor 7 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Si Ping		HU	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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City	Wuhan, Hubei	State/Province	
Postal Code		**Country** [i]	CN

Inventor 8 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Lan		YAO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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	Application Number	
Title of Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

City	Wuhan, Hubei	State/Province	
Postal Code		Country [i]	CN

Inventor 9 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Li Hong		XIAO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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Postal Code		Country [i]	CN

Inventor 10 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	A Man		ZHENG	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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City	Wuhan, Hubei	State/Province	
Postal Code		Country [i]	CN

Inventor 11 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kun		BAO	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Wuhan, Hubei	Country of Residence [i]	CN

Mailing Address of Inventor:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0460002
	Application Number	
Title of Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

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Address 2	18 Gaoxin 4th Rd., East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	**State/Province**	
Postal Code		**Country**	CN

Inventor 12 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Haohao		YANG	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

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City	Wuhan, Hubei	**State/Province**	
Postal Code		**Country**	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	26111		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE		
Attorney Docket Number	4123.0460002	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	**Suggested Figure for Publication (if any)**	

Micron Ex. 1019, p. 9
Micron v. YMTC
PGR2025-00021

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0460002
	Application Number	
Title of Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	26111		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	PCT/CN2018/098962	2018-08-06

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Micron Ex. 1019, p. 10
Micron v. YMTC
PGR2025-00021

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0460002
	Application Number	
Title of Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201710750398.4	CN	2017-08-28	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Micron Ex. 1019, p. 11
Micron v. YMTC
PGR2025-00021

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0460002
	Application Number	
Title of Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0460002
	Application Number	
Title of Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

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If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

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Organization Name	Yangtze Memory Technologies Co., Ltd.

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Signature	/Donald J. Featherstone/			Date (YYYY-MM-DD)	2018-09-10
First Name	Donald	Last Name	Featherstone	Registration Number	33,876

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STAIRCASE STRUCTURE FOR MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to PCT Application No. PCT/CN2018/098962 filed on August 6, 2018, which claims priority to Chinese Patent Application No. 201710750398.4 filed on August 28, 2017, the entire content of which is incorporated herein by reference.

BACKGROUND

[0002] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As a result, memory density for planar memory cells approaches an upper limit.

[0003] A three-dimensional (3D) memory architecture can address the density limitation in planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array. The 3D memory architecture also includes a stack of word lines horizontally arranged over a substrate, with vertical semiconductor channels that intersect the word lines. The intersection of a word line and a vertical semiconductor channel forms a memory cell.

BRIEF SUMMARY

[0004] Embodiments of the present disclosure are directed to a staircase structure for a memory device (e.g., 3D memory device). The disclosed embodiments provide numerous benefits including, but not limiting to, yield and manufacturing cost improvements.

[0005] In some embodiments, a semiconductor structure includes a staircase structure disposed over a substrate. The staircase structure includes a plurality of layer stacks, where each layer stack includes a first material layer disposed over a first portion of a second material layer. The staircase structure further includes a plurality of landing pads respectively disposed on the plurality of layer stacks, where each landing pad is disposed

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over a second portion of the second material layer of a respective layer stack. Each of the landing pads is adjacent to a respective side of the first material layer and extends over a respective top surface of the second material layer. The first material layer is made of an insulating material, including silicon oxide, aluminum oxide or a combination thereof. The second material layer is made of a first conductive material. The plurality of landing pads are made of a second conductive material. The first conductive material can be the same or different from the second material. Each of the first and the second conductive materials includes tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof. The second material layer of each layer stack is disposed over a portion of the first material layer of an adjacent layer stack. One of the plurality of landing pads is thicker than the first material layer of a corresponding layer stack and is insulated from another landing pad disposed on an adjacent layer stack.

[0006] In some embodiments, a method for forming a semiconductor structure includes forming a plurality of layer stacks over a substrate, where each layer stack includes a first material layer over a portion of a second material layer. The method further includes forming a hard mask layer over the plurality of layer stacks, forming a staircase structure on the plurality of layer stacks to expose a portion of the first material layer of each layer stack, forming a landing pad over a portion of the second material layer of the each layer stack, and removing the portion of the hard mask layer. The method further includes removing the landing pad and the second material layer of the each layer stack to form a recess in each layer stack, disposing a conductive material in the recess of each layer stack, and forming a dielectric layer over the staircase structure. The formation of the landing pad includes removing a portion of the second material layer from a side of each layer stack to form a recess, disposing a material layer over the staircase structure to fill the recess in each layer stack and removing a portion of the material layer to form a spacer at the side of each layer stack and a side of the portion of the hard mask layer. The formation of the landing pad further includes removing a portion of the first material layer of each layer stack using the spacer and the portion of the hard mask layer as a mask, disposing a dielectric layer over the staircase structure and removing the spacer and a portion of the dielectric layer. The disposing of the dielectric layer over the staircase structure includes disposing the dielectric layer over a portion of the second material

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layer, a portion of a side of the first material layer and a portion of a side of the spacer. The removing of the portion of the hard mask and the portion of the top layer stack in the plurality of layer stacks includes using dry etching, wet etching or a combination thereof. The trimming the mask stack include etching the mask stack incrementally and inwardly from a boundary of the mask stack. The removing of the portion of the hard mask includes using a wet etch process with tetramethylammonium hydroxide (TMAH), potassium hydroxide (KOH), a base, or a combination thereof. The formation of each layer stack and the hard mask layer includes deposition techniques using chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma-enhanced CVD (PECVD), low pressure CVD (LPCVD), sputtering, metal-organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), or a combination thereof.

[0007] In some embodiments, a memory device includes a memory string disposed over the substrate and a staircase structure disposed adjacent to the memory string. The staircase structure includes a plurality of layer stacks, where each layer stack of the plurality of layer stacks includes an insulating layer disposed over a first portion of the a conductive layer, where a second portion of the conductive layer is in contact with a side surface of the insulating layer. The conductive layer of the each layer stack is disposed over a portion of the insulating layer of an adjacent layer stack. The second portion of the conductive layer is thicker than the first portion of the conductive material layer.

[0008] Other aspects of the present disclosure can be understood by those skilled in the art in light of the description, the claims, and the drawings of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the art to make and use the present disclosure.

[0010] FIG. 1 illustrates a cross-sectional view of a hard mask layer and a plurality of dielectric layer pairs over a substrate, according to some embodiments.

[0011] FIG. 2A illustrates a cross-sectional view of a staircase structure, according to some embodiments.

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[0012] FIG. 2B illustrates a cross-sectional view of a staircase structure, according to some embodiments.

[0013] FIG. 3 illustrates a cross-sectional view of a staircase structure with a material layer disposed therein, according to some embodiments.

[0014] FIG. 4 illustrates a cross-sectional view of a staircase structure with spacers, according to some embodiments.

[0015] FIG. 5 illustrates a cross-sectional view of a staircase structure after removal of an insulating layer, according to some embodiments.

[0016] FIG. 6 illustrates a cross-sectional view of a staircase structure with a dielectric layer disposed thereon, according to some embodiments.

[0017] FIG. 7 illustrates a cross-sectional view of a staircase structure with landing pads, according to some embodiments.

[0018] FIG. 8 illustrates a cross-sectional view of a staircase structure with a dielectric layer disposed thereon, according to some embodiments.

[0019] FIG. 9 is a flowchart of a method for forming a memory device, according to some embodiments.

DETAILED DESCRIPTION

[0020] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the art that the present disclosure can also be employed in a variety of other applications.

[0021] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment can not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

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[0022] In general, terminology can be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, can be used to describe any feature, structure, or characteristic in a singular sense or can be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, can be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term "based on" can be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0023] The meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something, but also includes the meaning of "on" something with an intermediate feature or a layer therebetween. Moreover, "above" or "over" not only means "above" or "over" something, but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

[0024] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, can be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus can be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein can likewise be interpreted accordingly.

[0025] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added. The substrate includes a top surface and a bottom surface. The top surface of the substrate is where a semiconductor device is formed, and therefore the semiconductor device is formed at a top side of the substrate. The bottom surface is opposite to the top surface and therefore a bottom side of the substrate is opposite to the top side of the substrate. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

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[0026] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer has a top side and a bottom side where the bottom side of the layer is relatively close to the substrate and the top side is relatively away from the substrate. A layer can extend over the entirety of an underlying or overlying structure, or can have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any set of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or vias are formed) and one or more dielectric layers.

[0027] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term "about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0028] In the present disclosure, the term "horizontal/horizontally/lateral/laterally" means nominally parallel to a lateral surface of a substrate.

[0029] As used herein, the term "3D memory device" refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term "vertical/vertically" means nominally perpendicular to the lateral surface of a substrate.

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[0030] In some embodiments, a NAND string or a 3D memory device includes a semiconductor channel (e.g., a silicon channel) that extends vertically through a plurality conductor/dielectric layer pairs, where the semiconductor channel is surrounded by a dielectric stack. The plurality of conductor/dielectric layer pairs are also referred to herein as an "alternating conductor/dielectric stack." The conductor layer of the alternating conductor/dielectric stack can be used as a word line (e.g., to electrically connect one or more control gates). An intersection of a word line and the semiconductor channel forms a memory cell. Vertically-oriented memory strings require an electrical connection between a word line and an access line (e.g., back end of line (BEOL) interconnection) to select a memory cell along the memory string for read and write functions, where the electrical connection is provided by forming a staircase structure at the plurality of conductor/dielectric pairs.

[0031] The 3D memory device can include a plurality of staircase structures disposed adjacent to a plurality of memory strings for word line fan-out, according to some embodiments. As the demand for higher storage capacity continues to increase, the number of vertical levels of the staircase structures also increases. As a result, when applying a BEOL process to form interconnects on the staircase structures, an upper portion of the staircase structures is exposed to the BEOL process for a longer period of time than a lower portion of the staircase structures. This differential in BEOL exposure time increases the process variation of the final 3D memory device, thus introducing challenges in balancing manufacturing yield and process complexity/cost.

[0032] In the present disclosure, a staircase structure refers to a set of surfaces that include at least two horizontal surfaces (e.g., along an x-y plane) and at least two vertical surfaces (e.g., along a z-axis). Each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is also adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface. Each of the horizontal surfaces is referred as a "step" or "stair" of the staircase structure. A horizontal direction can refer to a direction (e.g., the x-axis or the y-axis) parallel with a top surface of the substrate (e.g., the substrate that provides the fabrication platform for formation of structures over it). A vertical direction can refer to a direction (e.g., the z-axis) perpendicular to the top surface of the structure.

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[0033] The staircase structure can be formed from a plurality of layer stacks by repetitively etching and trimming the each layer stack using a mask layer, where each layer stack is also referred to as a "staircase layer" (or "SC layer") of the staircase structure in the present disclosure. A step of the staircase structure exposes a portion of a top surface of a layer stack (e.g. a SC layer) of the plurality of layer stacks. In some embodiments, the staircase structure includes a plurality of layer stacks.

[0034] FIG. 1 illustrates a structure 100 with an alternating layer stack formed over a substrate 101 and a hard mask layer 106 formed over the alternating layer stack. A layer stack within the alternating layer stack can include a dielectric layer pair with an insulating layer 102 over a sacrificial layer 104. In some embodiments, sacrificial layer 104 can be disposed over insulating layer 102. Insulating layer 102 can include silicon oxide. Sacrificial layer 104 can include silicon nitride. In some embodiments, a thickness of insulating layer 102 or sacrificial layer 104 is between 10 nm and 200 nm. In some embodiments, a thickness of hard mask layer 106 is between 10 nm and 200 nm. In some embodiments, the layers in the alternating layer stack can be different thicknesses.

[0035] In some embodiments, substrate 101 includes any suitable material for supporting a memory structure (e.g., 3D memory structure). For example, substrate 101 can include silicon, silicon germanium, silicon carbide, silicon on insulator (SOI), germanium on insulator (GOI), glass, gallium nitride, gallium arsenide, any suitable III-V compounds, any other suitable material, or combinations thereof.

[0036] In some embodiments, sacrificial layer 104 can include any suitable material different from insulating layer 102. For example, sacrificial layer 104 can include poly-crystalline silicon, silicon nitride, poly-crystalline germanium, poly-crystalline germanium-silicon, any other suitable materials, or combinations thereof. In some embodiments, sacrificial layer 104 can include silicon nitride.

[0037] Insulating layer 102 can include any suitable insulating materials, such as silicon oxide or aluminum oxide.

[0038] In some embodiments, sacrificial layer 104 can be a conductive material layer. The conductive material layer can include any suitable conductive material. In some embodiments, the conductive material layer can include poly-crystalline silicon, tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, any other suitable material, or combinations thereof.

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[0039] In some embodiments, hard mask layer 106 can be a poly-crystalline semiconductor layer including poly-crystalline silicon, poly-crystalline germanium, poly-crystalline germanium-silicon, any other suitable material, or combinations thereof. In some embodiments, hard mask layer 106 can be a metal layer, including cobalt, nickel, tungsten, copper, or silver. In some embodiments, hard mask layer 106 can be a metal silicide layer, including $CoSi_x$, $NiSi_x$, or WSi_x. In some embodiments, hard mask layer 106 can be an organic material layer formed by spin-coating or self-assembling of organic molecules.

[0040] The formation of insulating layer 102, sacrificial layer 104, and hard mask layer 106 can include any suitable deposition methods such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma-enhanced CVD (PECVD), low pressure chemical vapor deposition (LPCVD), sputtering, metal-organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), sputtering, thermal evaporation, e-beam evaporation, molecular beam-epitaxy (MBE), any other suitable deposition method, or combinations thereof. In some embodiments, insulating layer 102, sacrificial layer 104, the conductive material layer, and hard mask layer 106 are each formed by CVD. In some embodiments, the formation of hard mask layer 106 further includes applying a thermal anneal process to form a silicide layer.

[0041] FIGs. 2A-2B illustrate a cross-sectional view of staircase structures 200A and 200B, according to some embodiments. Staircase structure 200A includes a hard mask 206 and a plurality of layer stacks 202/204. Each layer stack 202/204 is also referred to herein as an "SC layer." The steps in staircase structure 200A is formed by repeating an etch-trim process on structure 100 using a mask stack (not shown). After the formation of the steps, the mask stack is removed. In some embodiments, a step exposes a portion of a top surface of an SC layer. In some embodiments, a step exposes a side of a SC layer. In some embodiments, after repeating the etch-trim process, a portion of a top-most SC layer of staircase structure 200A is exposed and another portion of the top-most SC layer is covered by hard mask layer 206. An etch process is also applied to laterally etch a portion of sacrificial layer 204 of each SC layer. As a result, each step of staircase structure 200B has a recess (e.g. recess 220, 222, 224..., etc.). In some embodiments, a lateral dimension of each recess is between 10 nm and 300 nm. In some embodiments, a lateral dimension "a" of each step is between 100 nm and 1500 nm.

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[0042] In some embodiments, the mask stack (not shown in FIG. 2A) can include a photoresist or carbon-based polymer material. In some embodiments, the mask stack is removed after forming staircase structure 200A. The etch-trim process includes an etch process and a trim process. In some embodiments, the etch process includes using any suitable etchants (e.g., wet etch and/or dry etch) to sequentially remove a portion of hard mask layer 106 and a portion of the layer stack, including a portion of insulating layer 102 and a portion of sacrificial layer 104. For example, as shown in FIG.2A, hard mask layer 206, insulating layer 202, and sacrificial layer 204 are formed after removing a portion of hard mask layer 106, a portion of insulating layer 102, and a portion of sacrificial layer 104.

[0043] In the etch process, an etchant for insulating layer 102 has a higher etching selectivity over sacrificial layer 104, and/or vice versa. In some embodiments, the etchant for hard mask layer 106 has a higher etching selectivity over insulating layer 102 and sacrificial layer 104, and/or vice versa. Accordingly, an underlying layer stack can function as an etch-stop layer so that a single layer stack is patterned/etched, according to some embodiments. In some embodiments, insulating layer 102 and sacrificial layer 104 are etched using an anisotropic etch process, such as reactive ion etch (RIE) or other dry etch process. In some embodiments, the etchant includes carbon-fluorine (CF_4) based gases or hexafluoroethane (C_2F_6) based gases. In some embodiments, an etchant includes phosphoric acid and can be used to remove both insulating layer 102 and sacrificial layer 104. The methods and etchants to remove the layer stack described herein are exemplary. Other methods and etchants are within the spirit and scope of the present disclosure.

[0044] The trim process includes applying a suitable etch process (e.g., an isotropic dry etch or a wet etch) on the mask stack at directions parallel to a surface of the substrate. The mask stack is etched incrementally and inwardly from a boundary of the mask stack. The amount of trimmed mask stack can be related to the lateral dimension "a" of each steps of staircase structure 200A.

[0045] The process for forming the recess structure (e.g. recess 220, 222, 224…, etc.) uses an etch process similar to the etching techniques for removing sacrificial layer 104 as described above. In some embodiments, the process etches sacrificial layer 204 at a higher etching rate than that of insulating layer 202 or hard mask layer 206.

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[0046] FIG. 3 illustrates a cross-sectional view of a staircase structure 300 with a material layer 310 disposed thereon, according to some embodiments. Material layer 310 is conformally disposed on staircase structure 200B, including on a top surface of hard mask layer 206, a side of hard mask layer 206, a top surface of each SC layer (e.g. each step) of staircase structure 200B, and a recess of the each SC layer. In some embodiments, material layer 310 fills each recesses of staircase structure 200B. Material layer 310 can be made of similar material as hard mask layer 106, where the formation of material layer 310 can be similar to that of hard mask layer 106. In some embodiments, a thickness of material layer 310 is thicker than that of sacrificial layer 204. In some embodiments, a thickness of material layer 310 is thinner than that of the SC layer.

[0047] FIG. 4 illustrates a cross-sectional view of a staircase structure 400 with spacers 410, according to some embodiments. Each of spacers 410 is formed at a side of each SC layer of staircase structure 300. In some embodiments, spacer 410 is formed at a side of hard mask layer 206. Spacer 410 is formed by removing a portion of material layer 310 from staircase structure 300 using similar techniques as removing hard mask layer 106. In some embodiments, material layer 310 is removed from a top surface of staircase structure 300 and a top surface of hard mask layer 206. In some embodiments, spacer 410 fills a recess (e.g. recess 220, 222, or 224) of each SC layer of staircase structure 300. In some embodiments, spacer 410 covers a side of sacrificial layer 204 of each SC layer of staircase structure 300. In some embodiments, spacer 410 covers a portion of a side of insulating layer 202 of each SC layer of staircase structure 300. In some embodiments, spacer 410 and hard mask layer 106 are made of the same material.

[0048] FIG. 5 illustrates a cross-sectional view of a staircase structure 500 after removal of a portion of insulating layer 202, according to some embodiments. In FIG. 5, the portion of insulating layer 202 of each SC layer of staircase structure 400 is removed using spacers 410 and hard mask layer 206 as masks. Insulating layer 502 is formed after removing the portion of insulating layer 202 using similar techniques as removing insulating layer 102. As illustrated in FIG. 5, each SC layer of staircase structure 500 exposes a portion of a top surface of sacrificial layer 204 and spacer 410 of each SC layer. In some embodiments, a side of insulating layer 502 of each SC layer of staircase structure 500 is exposed.

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[0049] FIG. 6 illustrates a cross-sectional view of a staircase structure 600 with a dielectric layer 620 disposed thereon, according to some embodiments. Dielectric layer 620 covers a top surface of staircase structure 500 and a portion of a side of staircase structure 500. In some embodiments, dielectric layer 620 covers a portion of each spacer 410 of staircase structure 500. In some embodiments, dielectric layer 620 covers a top surface of hard mask layer 206, a portion of a top surface of sacrificial layer 204, and a portion of a side of insulating layers 502 of each SC layer of staircase structure 500. In some embodiments, dielectric layer 620 has poor step-coverage on staircase structure 500. For example, the poor step-coverage includes a thickness of dielectric layer 620 that is substantially thinner at a side of staircase structure 600 than that at a top surface of staircase structure 600. In some embodiments, dielectric layer 620 is discontinuous between each SC layer of staircase structure 600. In some embodiments, a portion of spacer 410 or a portion of a side of insulating layer 502 of each SC layer of staircase structure 600 is exposed.

[0050] In some embodiments, dielectric layer 620 can be a nitride layer, including silicon nitride, silicon oxynitride, any suitable materials, or combinations thereof. In some embodiments, dielectric layer 620 and each sacrificial layer 204 of staircase structure 600 are made of the same material. In some embodiments, a thickness of dielectric layer 620 at a top surface of staircase structure 600 is thinner than that of insulating layer 502 of each SC layer of staircase structure 600. Dielectric layer 620 can be formed using deposition techniques including, but not limiting to plasma-enhanced CVD (PECVD), low pressure CVD (LPCVD), physical vapor deposition (PVD), high density plasma (HDP), atomic layer deposition (ALD), any suitable deposition techniques, or combinations thereof.

[0051] FIG. 7 illustrates a cross-sectional view of a staircase structure700 with landing pads 720, according to some embodiments. In FIG. 7, spacers 410 and a portion of dielectric layer 620 are removed from staircase structure 600. After removing spacers 410 and the portion of dielectric layer 620, a landing pad 720 is formed over each SC layer of staircase structure 700. As shown in FIG. 7, landing pad 720 is in contact with sacrificial layer 204 of each SC layer of staircase structure 700. Both landing pad 720 and sacrificial layer 204 of the SC layer are disposed over a portion of insulating layer 502 of another vertically adjacent SC layer. In some embodiments, landing pad 720 is formed over hard

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mask layer 206. In some embodiments, landing pad 720 of a SC layer is thicker than insulating layer 502 of the SC layer. Landing pad 720 can also be discontinuous from another landing pad 720 disposed on another vertically adjacent SC layer. In some embodiments, landing pad 720, dielectric layer 620 and sacrificial layer 204 are made of the same material.

[0052] Removal of spacers 410 and the portion of dielectric layer 620 can use an etch process similar to that which removes hard mask layer 106 and sacrificial layer 104, where the etch process has high etching selectivity to insulating layers 502 as described above. In some embodiments, more than two etch processes are applied to etch dielectric layer 620 and spacers 410, in which the etch processes have high etching selectivity to insulating layers.

[0053] FIG. 8 illustrates a cross-sectional view of a staircase structure 800 with a dielectric layer 825 disposed thereon, according to some embodiments. Staircase structure 800 is formed by removing hard mask layer 206 from staircase structure 700. Further, a wordline layer 804 for each SC layer of staircase structure 800 is formed by replacing landing pad 720 and sacrificial layer 204 of each step of staircase structure 700 with one or more conducting material layers, including poly-crystalline silicon, tungsten, silicide, nickel, tungsten, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, any other suitable material, or combinations thereof. As shown in FIG. 8, wordline layer 804 includes landing pad 820 and conductive layer 840. Wordline layer 804 of an SC layer is disposed over a portion of insulating layer 502 of another vertically adjacent SC layer. In some embodiments, a length of wordline layer 804 is shorter in a horizontal direction (e.g., x-direction) than that of insulating layer 502 of another vertically adjacent SC layer. In some embodiments, landing pad 820 is thicker than insulating layer 502 and is insulated from another landing pad 820 disposed on another vertically adjacent SC layer. A dielectric layer 825 is disposed on staircase structure 700. Each wordline layer 804, including landing pad 820 and a conductive layer 840, of staircase structure 800 can control a portion of a memory string in the stacked storage region of a memory device (e.g., 3D memory device). In some embodiments, each wordline layer 804 of staircase structure 800 is a wordline of the memory device, where conductive layer 840 contacts a portion of a memory string of a memory device, and landing pad 820 contacts a portion of a side of insulating layer 502. In some

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embodiments, a thickness of landing pad structure 820 of word line 804 is thicker than that of conductive layer 840 of wordline layer 804. In some embodiments, an edge of wordline layer 804 of each step of staircase structure 800 has landing pad structure 820, where landing pad 820 is made of the same or different conductive material as conductive layer 840.

[0054] In some embodiments, hard mask layer 206 of staircase structure 700 is removed using a wet etch process. In some embodiments, an etchant used in the wet etch process includes tetramethylammonium hydroxide (TMAH). In some embodiments, a landing pad 720 over hard mask layer 206 is lifted-off after the wet etch process. In some embodiments, hard mask layer 206 is removed using similar techniques as removing hard mask layer 106.

[0055] In some embodiments, replacement of landing pad 720 and sacrificial layer 204 of each SC layer with the conductive material includes formation of one or more recesses in each SC layer by removing landing pad 720 and sacrificial layer 204 from each SC layer, followed by filling the one or more conductive material layers in the one or more recesses. The removal of landing pad 720 or sacrificial layer 204 can be similar to the techniques of removing sacrificial layer 104. In some embodiments, the removal of landing pad 720 uses different techniques from the removal of sacrificial layer 204. The filling of the conductive material can be similar to the techniques of depositing metallic hard mask layer 106. In some embodiments, the filling of a recess formed by the removal of landing pad 720 uses different techniques and/or conductive material from the filling of another recess formed by the removal of sacrificial layer 204.

[0056] In some embodiments, the formation of dielectric layer 825 uses similar techniques as forming insulating layer 102 or sacrificial layer 104. In some embodiments, the formation of dielectric layer 825 uses a spin-coating process. In some embodiments, dielectric layer 825 includes any suitable dielectric materials, such as silicon oxide or a spin-on-dielectric material. In some embodiments, the formation of dielectric layer 825 further includes a planarization process, such as chemical-mechanical planarization (CMP). In some embodiments, dielectric layer 825 is made of the same material as insulating layer 102 or sacrificial layer 104. In some embodiments, dielectric layer 825 is disposed on each step of staircase structure 800.

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[0057] FIG. 9 is a flowchart of a method 900 for forming a memory device (e.g., 3D memory device), according to some embodiments. The operations of method 900 can be used to form memory device structures illustrated in FIGs. 1-8. The operations shown in method 900 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. In some embodiments, some operations of exemplary method 900 can be omitted or include other operations that are not described here for simplicity. In some embodiments, operations of method 900 can be performed in a different order and/or vary.

[0058] In operation 910, an alternating stack and a hard-mask layer are formed over a substrate. The substrate can include any suitable material for forming a memory structure—e.g., a 3D memory device. For example, the substrate can include silicon, silicon germanium, silicon carbide, SOI, GOI, glass, gallium nitride, gallium arsenide, plastic sheet, and/or other suitable III-V compound.

[0059] In operation 910, a layer stack in the alternatin g layer stack can include a dielectric layer pair with a first material layer and a second material layer. In some embodiments, the first material layer can be an insulating layer. The second material layer can be an sacrificial layer or a conductive material layer. The sacrificial layer can include materials such as silicon nitride, poly-crystalline silicon, poly-crystalline germanium, poly-crystalline germanium-silicon, any other suitable material, or combinations thereof. The insulating layer can include silicon oxide, aluminum oxide, or other suitable materials. The conductive material layer can include tungsten, titanium nitride, tantalum nitride, tungsten nitride, any other suitable material, or combinations thereof. Each of the insulating, sacrificial, and conductive material layers can include materials formed by one or more thin film deposition processes including, but not limiting to, CVD, PVD, ALD, or any combinations thereof.

[0060] The hard mask layer can be a poly-crystalline semiconductor layer, including poly-crystalline silicon. In some embodiments, the hard mask layer can be a metal layer, such as cobalt, nickel, tungsten, copper, or silver. In some embodiments, the hard mask layer can be a silicide layer, including $CoSi_x$, $NiSi_x$, or WSi_x . In some embodiments, the hard mask layer can be an organic material layer. The hard mask layer can be formed using similar techniques as forming the alternating layer stack. In some embodiments, the formation of the hard mask layer includes a thermal anneal process.

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[0061] In operation 920, a staircase structure is formed, where a layer of each layer stack in the staircase structure is recessed. Each step of the staircase structure can be formed by repeating an etch-trim process using a mask stack. In some embodiments, the mask stack can include a photoresist or carbon-based polymer material. The etch-trim process includes an etch process and a trim process. In some embodiments, the etch process etches a portion of the hard mask layer and a portion of the layer stack. In some embodiments, the etch process etches a portion of the hard mask layer and a portion of a plurality of layer stacks. In some embodiments, one or more etchants are used in the etch process, and each of the etchants etches the first material layer at a higher etch rate than the second material layer or the hard mask layer. In some embodiments, the one or more etchants etches one of the first material layer, the second material layer and the hard mask layer at a higher etch rate than the other two of the first material layer, the second material layer and the hard mask layer. In some embodiments, the etch process can control the formation of steps of the staircase structure because high etching selectivity between the first and the second material layer allows the etch process to stop on a surface of a layer stack of the alternating layer stack.

[0062] The trim process includes a suitable etch (e.g., an isotropic dry etch or a wet etch) of the mask stack and is performed at a direction parallel to a surface of the substrate. The amount of trimmed mask stack can be related to the lateral dimensions of the staircase structure. After the repetitive etch-trim process, the resulting staircase structure includes a plurality of layer stacks (or plurality of SC layers). In some embodiments, the staircase structure includes a plurality of steps, where each of the steps exposes a side and a portion of a top surface of each SC layer. In some embodiments, the height of each of the steps is one level, which is equal to the thickness of a SC layer.

[0063] Further, in operation 920, a layer of each SC layer is recessed. The recess process uses similar techniques as etching the alternating layer stack. In some embodiments, a sacrificial layer of each SC layer is recessed using the recess process. In some embodiments, the recess process etches a sacrificial layer of each SC layer and has higher etching selectivity to an insulating layer of each SC layer and the hard mask layer. As a result, the staircase structure includes a plurality of steps, where a SC layer exposed by a step has a lateral recess structure. The formation of the staircase structure is described above with respect to FIGs. 2A-2B.

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[0064] In operation 930, a spacer is formed at a side of each step of the staircase structure. A material layer is disposed on the staircase structure. In some embodiments, the material layer fills a recess in each of the SC layers. In some embodiments, the material layer is conformally disposed on the staircase structure. In some embodiments, the material layer is made of a similar material as the hard mask layer. In some embodiments, formation of the material layer uses similar techniques as forming the hard mask layer.

[0065] Further, in operation 930, a portion of the material layer is removed to form a spacer at a side of each of the SC layers. The removal of the material layer uses similar techniques as removing the hard mask layer. In some embodiments, the material layer is completely removed from a top of each of the SC layers. In some embodiments, the material layer is completely removed from a top of the hard mask layer. In some embodiments, the spacer fills in the recess of each of the SC layers. The spacer and the hard mask layer can be made of the same material. The formation of the spacers is described above with respect to FIGs. 3-4.

[0066] In operation 940, a portion of a layer of each of the SC layers is removed using the spacers and hard mask layer as a mask. In some embodiments, a portion of an insulating layer of each of the SC layers is removed. The removal of the portion of the layer of each of the SC layers uses similar techniques as removing the alternating layer stack. An example of operation 940 is described above with respect to FIG. 5.

[0067] In operation 950, a landing pad is formed at each layer stack of the staircase structure. A dielectric layer is disposed to cover a top surface and a portion of a side of the staircase structure, including a portion of a side of each spacer and a side of an insulating layer of each of the SC layers. The dielectric layer is substantially thinner at a side of the staircase structure than at a top surface of the staircase structure. In some embodiments, the dielectric layer is discontinuous between steps of the staircase structure. The dielectric layer can be a nitride layer. In some embodiments, the dielectric layer and the sacrificial layer are made of the same material, where forming the dielectric layer uses similar techniques as forming the sacrificial layer.

[0068] Operation 950 further includes removing a portion of the dielectric layer and the spacer to form a landing pad on each of the SC layers. The removal of the spacer and the dielectric layer uses an etch process similar to that for forming the staircase structure from

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the alternating layer stack and the hard mask layer. In some embodiments, the dielectric layer is completely removed from a side of each of the SC layers. In some embodiments, after removing the spacer and the portion of the dielectric layer, the dielectric layer remaining on each of the SC layer forms the landing pad. The landing pad and the sacrificial layer can be made of the same material. The formation of landing pads is described above with respect to FIGs 6-7.

[0069] In operation 960, a wordline layer at each layer of the staircase structure is formed. For example, the hard mask layer on a top surface of the staircase structure can be removed using an etch process. The etch process can include a wet etch process using tetramethylammonium hydroxide (TMAH). In some embodiments, the etch process lifts-off a landing pad at a top of the hard mask layer. Operation 960 further includes forming word lines of the memory device (e.g., 3D memory device) by replacing each of the landing pads and the insulating layers of each of the SC layers with one or more conductive material. This replacement starts from forming a recess at each SC layer of the staircase by removing the landing pad and the insulating layer of each SC layer. The one or more conductive material is disposed in the recess of each SC layer to form a word line in the staircase structure. After forming the word lines, a dielectric layer is disposed over the staircase structure for the BEOL interconnect process.

[0070] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the disclosure and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the disclosure and guidance.

[0071] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can

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be defined so long as the specified functions and relationships thereof are appropriately performed.

[0072] The Summary and Abstract sections can set forth one or more but not all exemplary embodiments of the present disclosure and thus are not intended to limit the present disclosure and the appended claims.

[0073] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

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WHAT IS CLAIMED IS:

1. A semiconductor structure, comprising:

a substrate; and

a staircase structure disposed over the substrate, wherein the staircase structure comprises:

a plurality of layer stacks, each layer stack comprising a first material layer disposed over a first portion of a second material layer; and

a plurality of landing pads respectively disposed on the plurality of layer stacks, each landing pad disposed over a second portion of the second material layer of a respective layer stack.

2. The semiconductor structure of claim 1, wherein each of the plurality of landing pads is adjacent to a respective side of the first material layer.

3. The semiconductor structure of claim 1, wherein each of the plurality of landing pads extends over a respective top surface of the second material layer.

4. The semiconductor structure of claim 1, wherein the first material layer comprises an insulating material, the second material layer comprises a first conductive material, and each of the plurality of landing pads comprises a second conductive material.

5. The semiconductor structure of claim 4, wherein the first conductive material is the same as or different from the second conductive material.

6. The semiconductor structure of claim 4, wherein:

the insulating material layer comprises silicon oxide, aluminum oxide, or a combination thereof; and

each of the first and the second conductive material layers comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof.

7. The semiconductor structure of claim 1, wherein the second material layer of each layer stack is disposed over a portion of the first material layer of an adjacent layer stack.

8. The semiconductor structure of claim 7, wherein one of the plurality of landing pads is thicker than the first material layer of a corresponding layer stack and is insulated from another landing pad disposed on an adjacent layer stack.

9. A method for forming a semiconductor structure, comprising:

forming a plurality of layer stacks over a substrate, wherein each layer stack comprises a first material layer disposed over a second material layer ;

forming a hard mask layer over the plurality of layer stacks;

forming a staircase structure on the plurality of layer stacks to expose a portion of the first material layer of each layer stack;

forming a landing pad over a portion of the second material layer of the each layer stack; and

removing the portion of the hard mask layer.

10. The method of claim 9, further comprising:

removing the landing pad and the second material layer of the each layer stack to form a recess in each layer stack;

disposing a conductive material in the recess of each layer stack; and

forming a dielectric layer over the staircase structure.

11. The method of claim 9, wherein forming the landing pad comprises:

removing a portion of the second material layer from a side of each layer stack to form a recess;

disposing a material layer over the staircase structure to fill the recess in each layer stack; and

removing a portion of the material layer to form a spacer at the side of each layer stack and a side of the portion of the hard mask layer.

12. The method of claim 11, wherein forming the landing pad further comprises:

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removing a portion of the first material layer of each layer stack using the spacer and the portion of the hard mask layer as a mask;

disposing a dielectric layer over the staircase structure; and

removing the spacer and a portion of the dielectric layer.

13. The method of claim 12, wherein disposing the dielectric layer over the staircase structure comprises disposing the dielectric layer over a portion of the second material layer, a portion of a side of the first material layer, and a portion of a side of the spacer.

14. The method of claim 9, wherein removing the portion of the hard mask layer and the portion of the top layer stack in the plurality of layer stacks comprise removing the portion of the hard mask layer and the portion of the top layer stack by dry etching, wet etching, or a combination thereof.

15. The method of claim 9, wherein trimming the mask stack comprises etching the mask stack incrementally and inwardly from a boundary of the mask stack.

16. The method of claim 9, wherein removing the portion of the hard mask layer comprises removing the portion of the hard mask layer by a wet etch process using tetramethylammonium hydroxide (TMAH), potassium hydroxide (KOH), a base, or a combination thereof.

17. The method of claim 9, wherein forming of each layer stack and the forming of the hard mask layer comprises deposition techniques using chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma-enhanced CVD (PECVD), low pressure CVD (LPCVD), sputtering, metal-organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), or a combination thereof.

18. A memory device, comprising:

a substrate;

a memory string disposed over the substrate; and

a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:

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a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer is in contact with a side surface of the insulating layer.

19. The memory device of claim 18, wherein the conductive layer of each layer stack is disposed over a portion of the insulating layer of an adjacent layer stack.

20. The memory device of claim 18, wherein the second portion of the conductive layer is thicker than the first portion of the conductive material layer.

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ABSTRACT

A semiconductor structure is disclosed. The semiconductor structure includes a staircase structure disposed over a substrate. The staircase structure includes a plurality of layer stacks, where each layer stack is made of a first material layer over a portion of a second material layer. The staircase structure further includes a plurality of landing pads, where each landing pad is disposed over another portion of the second material layer of a respective layer stack.

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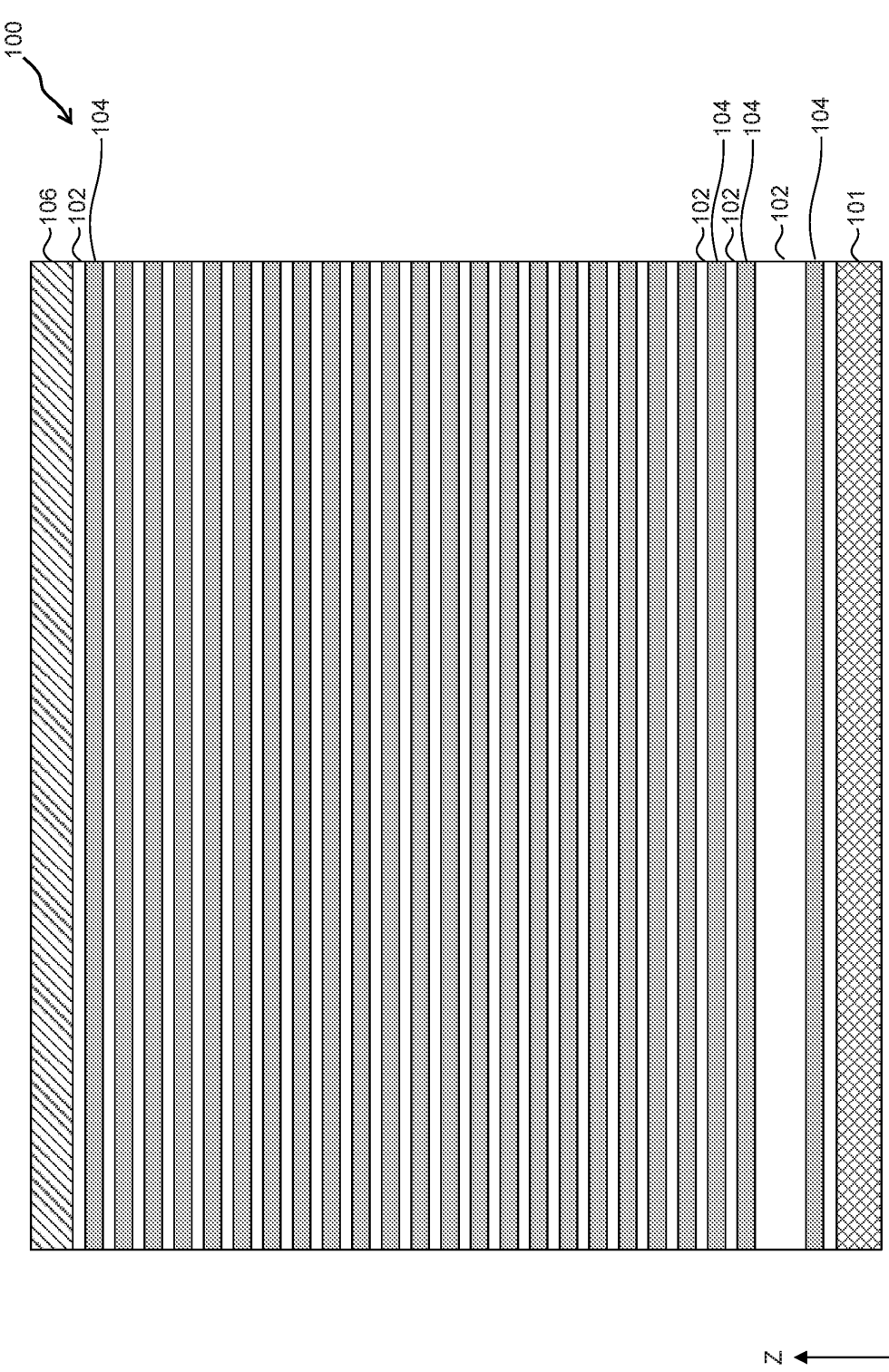


FIG. 1

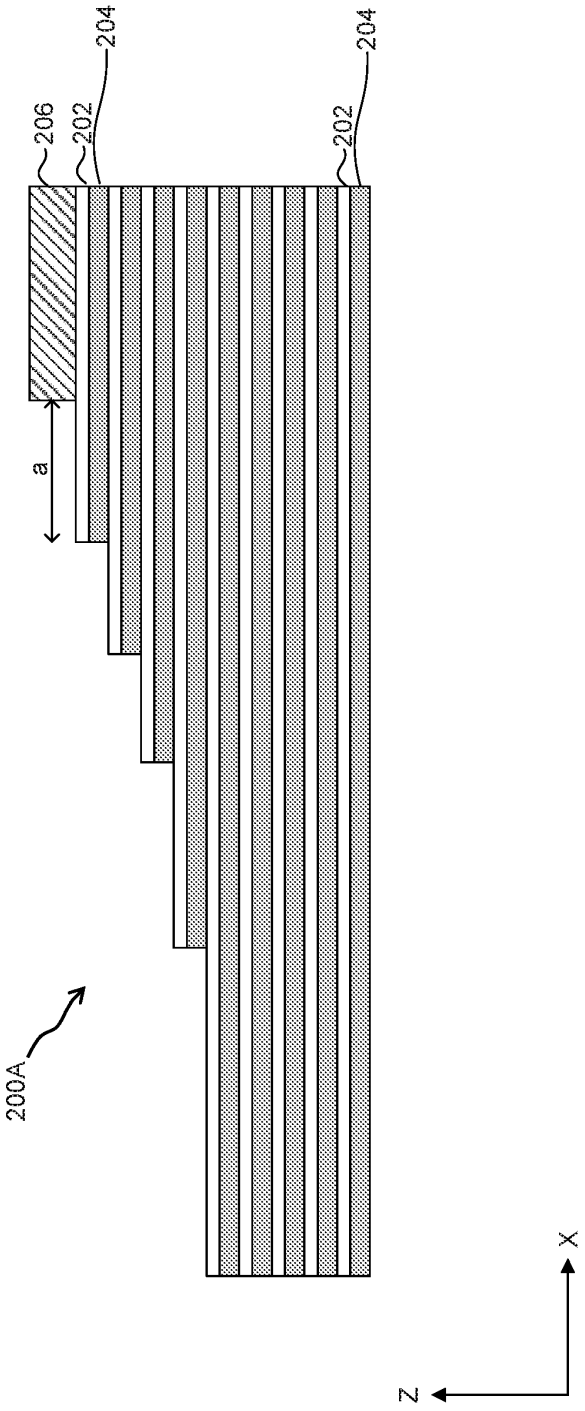


FIG. 2A

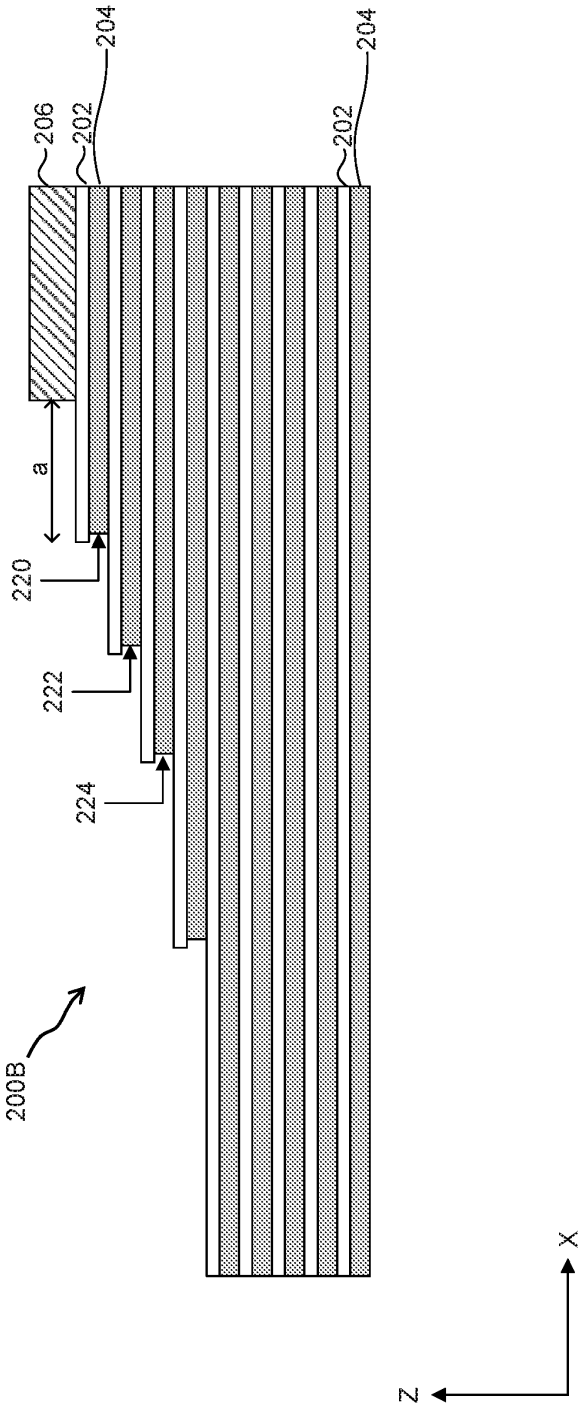


FIG. 2B

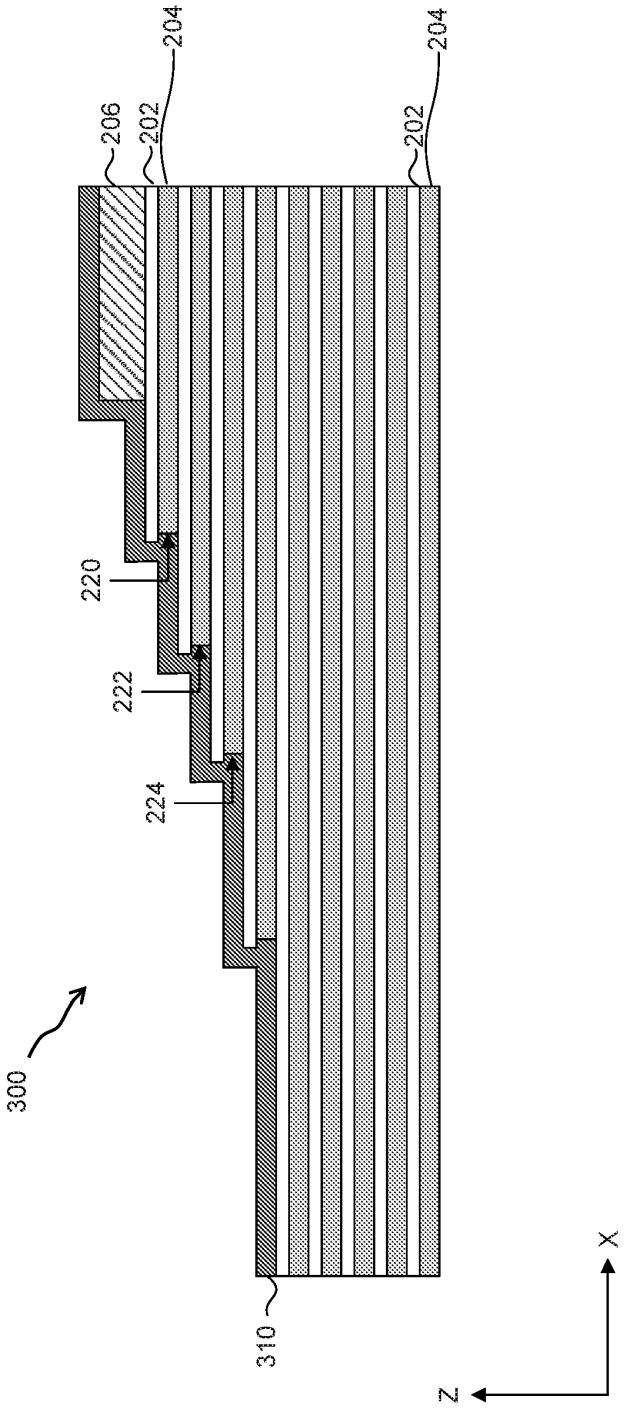


FIG. 3

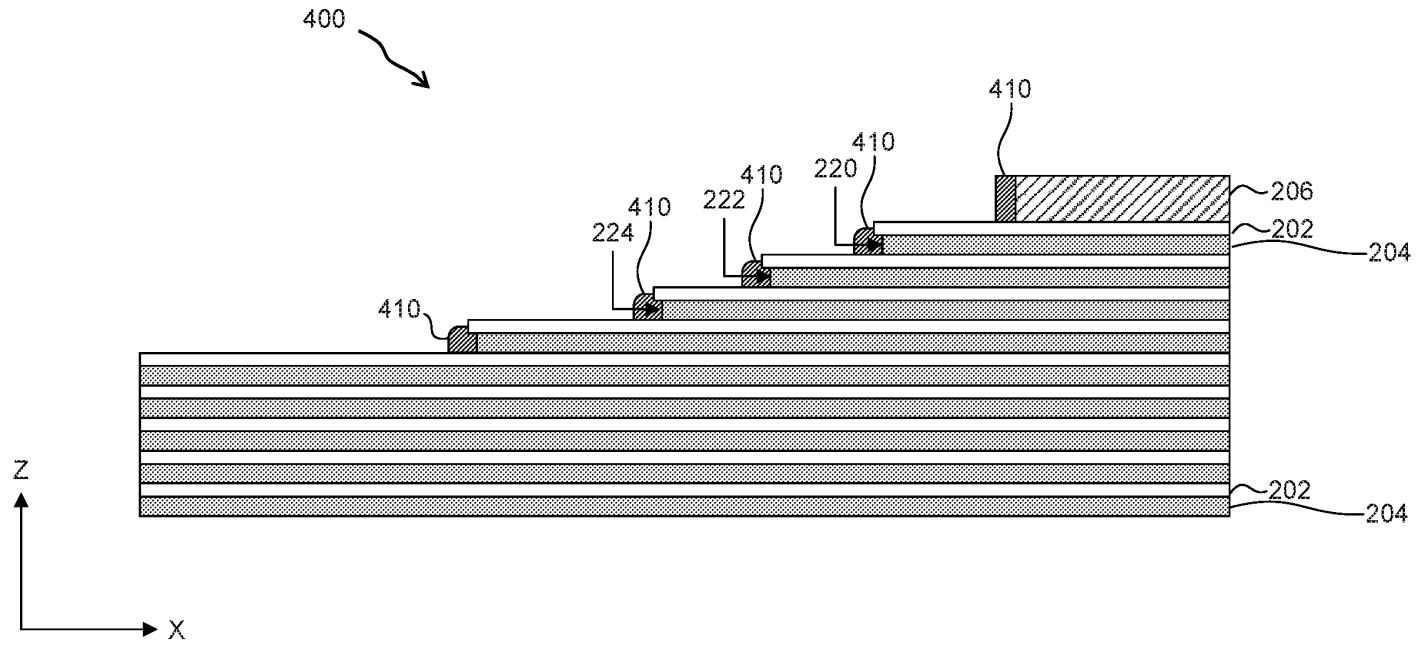


FIG. 4

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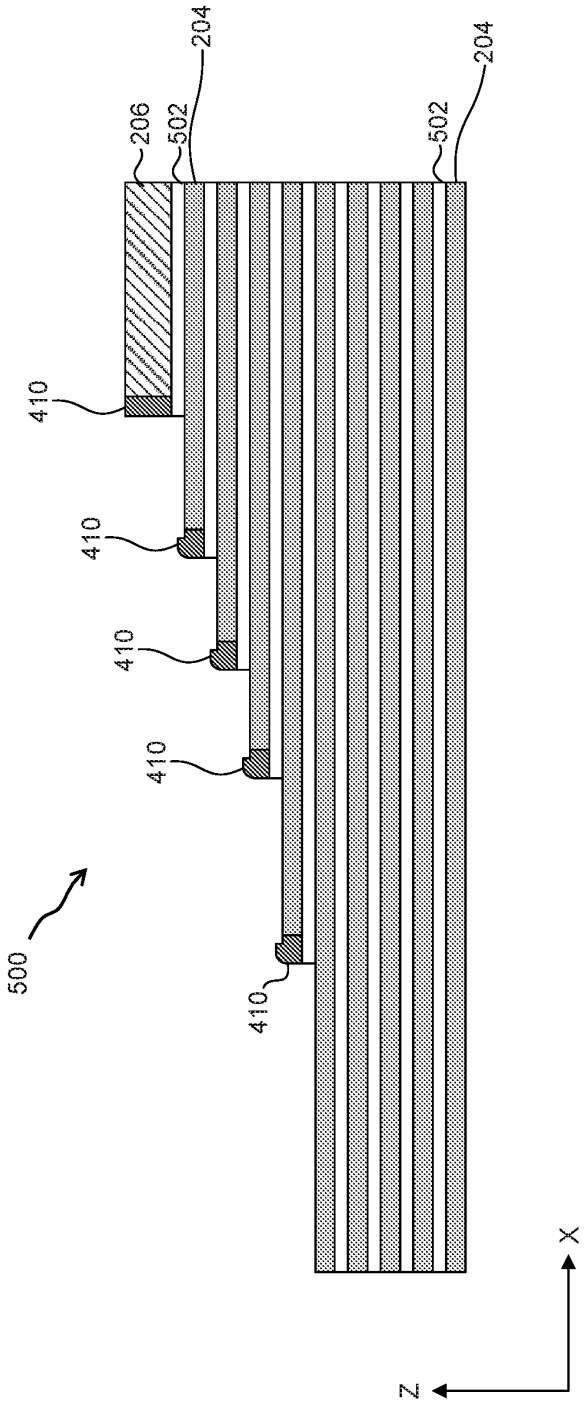


FIG. 5

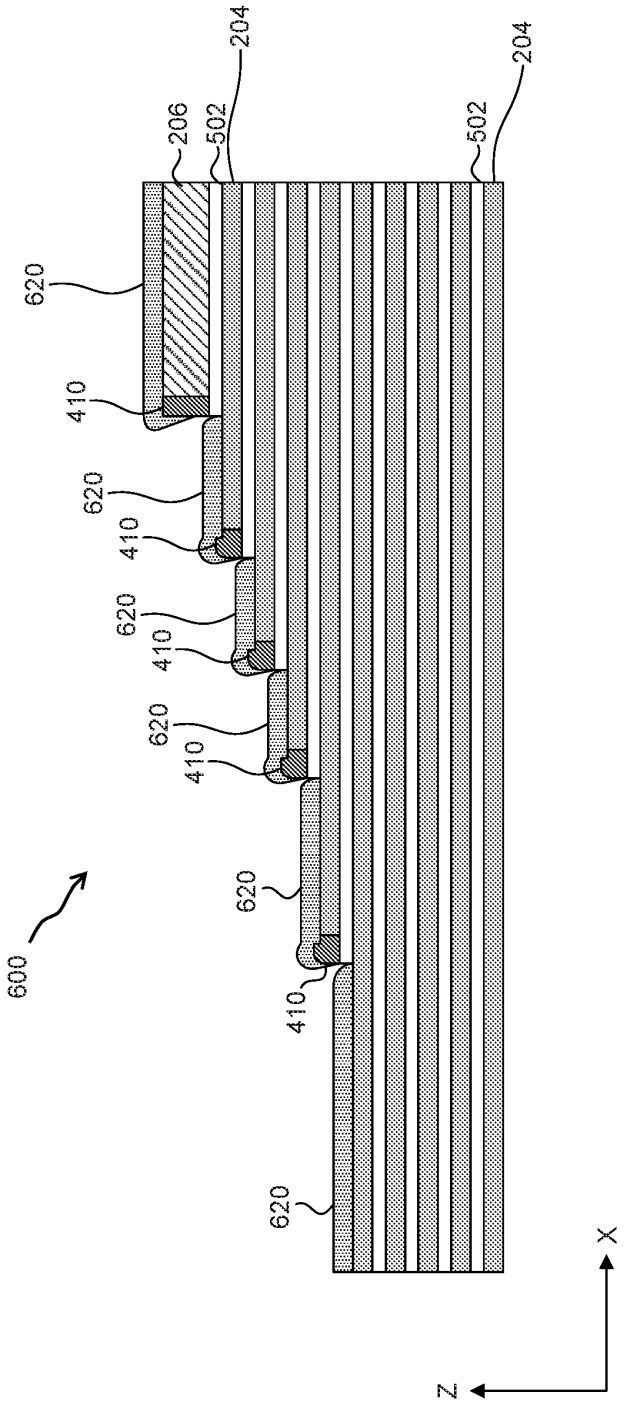

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FIG. 6

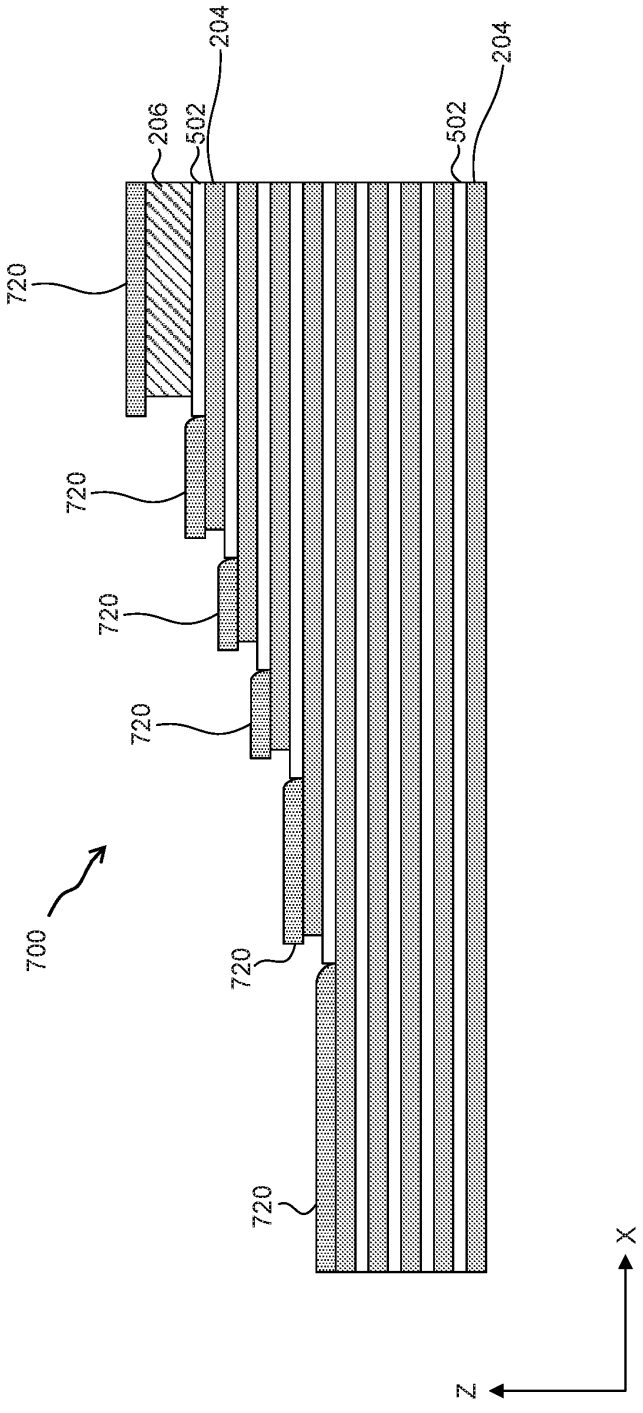


FIG. 7

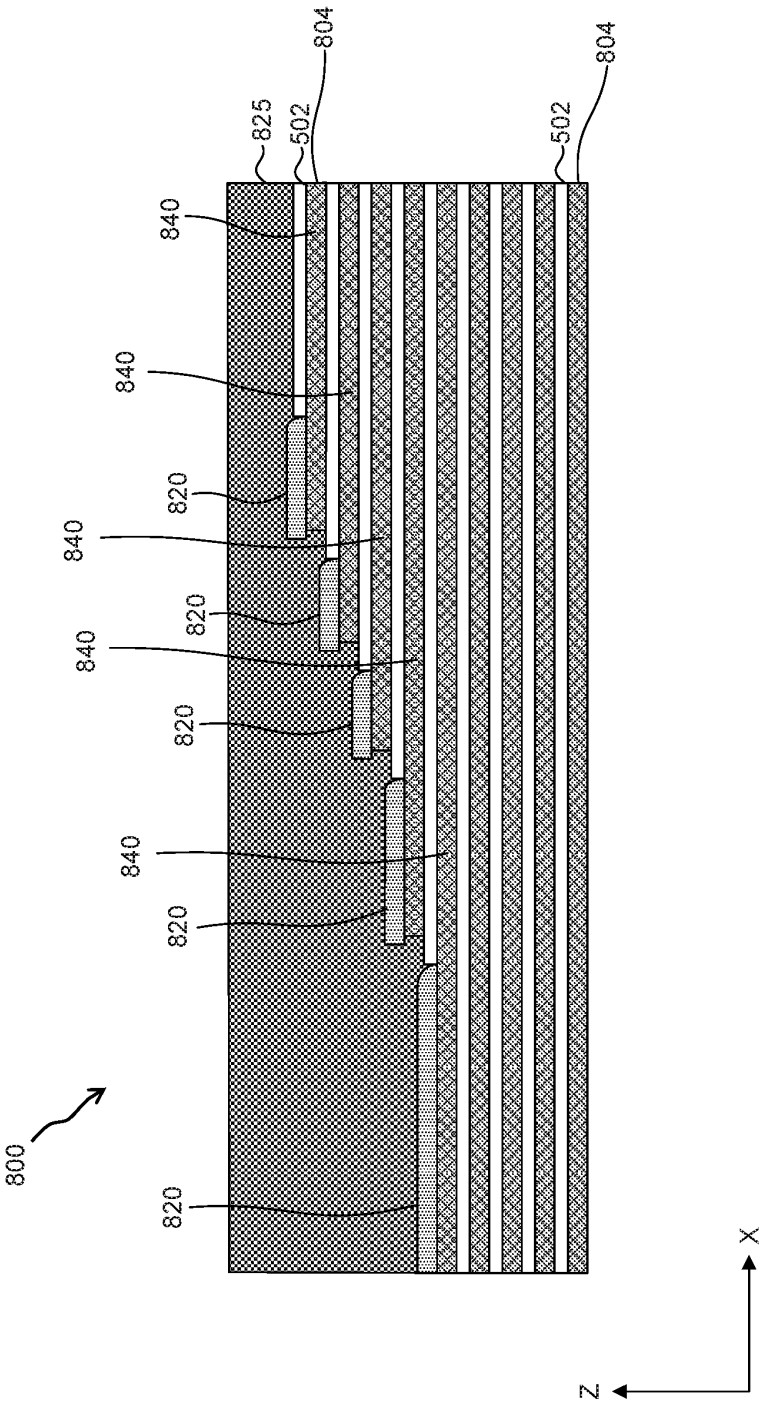

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FIG. 8

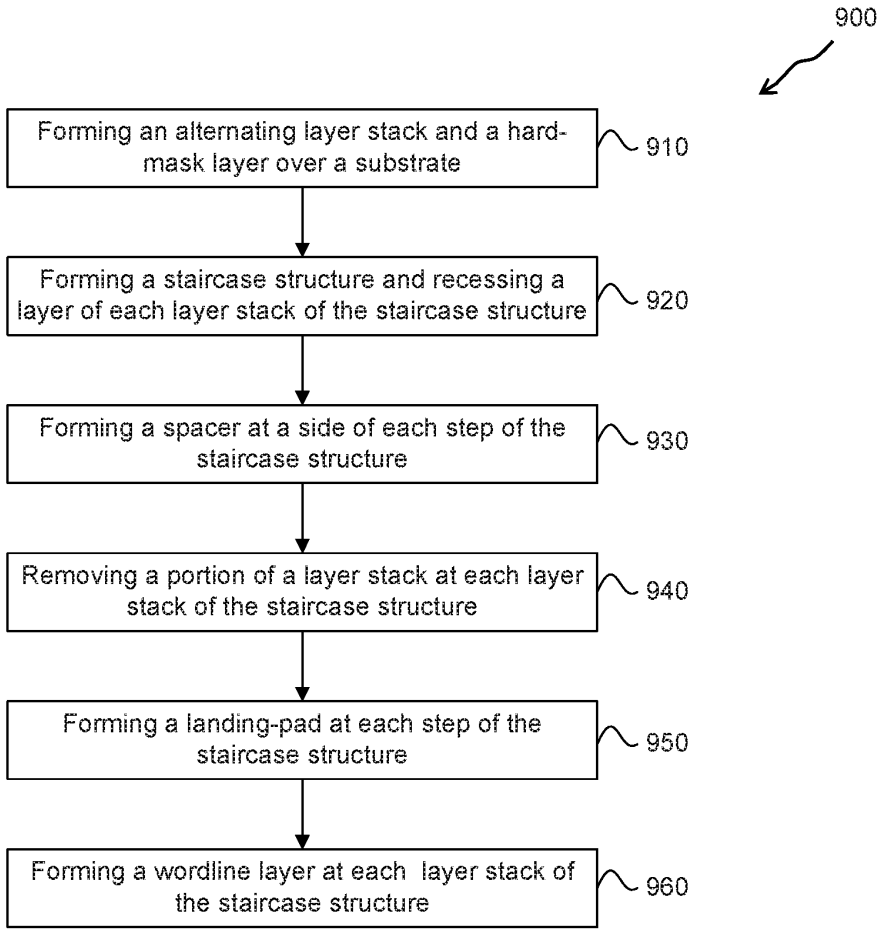


FIG. 9

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Doc Code: PA..
Document Description: Power of Attorney

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Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Zhenyu LU
Title	STAIRCASE STRUCTURE FOR MEMORY DEVICE
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0460002

SIGNATURE of Applicant or Patent Practitioner

Signature	/Donald J. Featherstone/	Date (Optional)	9/10/18
Name	Donald J. Featherstone	Registration Number	33,876
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of one (1) forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 26111

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number: 26111

OR

☐ Firm or Individual Name	
Address	
City	State / Zip
Country	
Telephone	Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

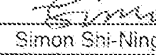
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

✓ 1 **SIGNATURE of Applicant for Patent**

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Simon Shi-Ning Yang		
Title	CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	33677487
Application Number:	16126956
International Application Number:	
Confirmation Number:	3036
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Customer Number:	26111
Filer:	Donald J. Featherstone/Tonyia Skinner
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0460002
Receipt Date:	10-SEP-2018
Filing Date:	
Time Stamp:	18:39:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		41230460002_Utility_Application_FILINGsigned.pdf	2114148 1b0dee3e9a360c30879cf6f11ed346c532a5d6bd	yes	53

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	2
	Transmittal of New Application	3	4
	Authorization for Extension of Time all replies	5	5
	Application Data Sheet	6	17
	Specification	18	36
	Claims	37	40
	Abstract	41	41
	Drawings-only black and white line drawings	42	51
	Power of Attorney	52	53
Warnings:			
Information:			
	Total Files Size (in bytes):	2114148	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Sterne Kessler
STERNE KESSLER GOLDSTEIN & FOX

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

September 10, 2018

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Patent Application under 37 C.F.R. § 1.53(b)
(*Continuation of Appl. No. PCT/CN2018/098962; Filed: August 6, 2018*)
Appl. No. *To Be Assigned*; Filed: *Herewith*
For: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**
Inventors: LU *et al.*
Our Ref: 4123.0460002

Commissioner:

The following documents are transmitted herewith for appropriate action by the U.S. Patent and Trademark Office:

1. Utility Patent Application Transmittal Form (PTO/AIA/15);

2. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);

3. U.S. Utility Patent Application entitled:

   STAIRCASE STRUCTURE FOR MEMORY DEVICE

   and naming as inventors:

   Zhenyu LU
   Jun CHEN
   Xiaowang DAI
   Jifeng ZHU
   Qian TAO
   Yu Ru HUANG
   Si Ping HU
   Lan YAO
   Li Hong XIAO
   A Man ZHENG
   Kun BAO
   Haohao YANG

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the application consisting of:

a. An Application Data Sheet (37 C.F.R. § 1.76) (PTO/AIA/14);

b. A specification containing:

i. 19 pages of description prior to the claims;

ii. 4 pages of claims (20 claims);

iii. a one (1) page abstract; and

c. 10 sheets of drawings: (*Figures 1, 2A-2B and 3-9*).

4. An executed Power of Attorney by Applicant form (PTO/AIA/82B) and the Transmittal for Power of Attorney form (PTO/AIA/82A).

The above-listed documents are filed electronically.

Correspondence should be sent to Customer Number 26111.

This patent application is being submitted under 37 C.F.R. § 1.53(b) without Declaration and without the required fees.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/KTS/tas
Enclosures

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Micron v. YMTC
PGR2025-00021

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/126,956	09/10/2018	2811	0.00	4123.0460002	20	3

CONFIRMATION NO. 3036

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT

OC000000102989333

Date Mailed: 10/15/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Zhenyu LU, Wuhan, CHINA;
Jun Chen, Wuhan, CHINA;
Xiaowang Dai, Wuhan, CHINA;
Jifeng Zhu, Wuhan, CHINA;
Qian Tao, Wuhan, CHINA;
Yu Ru Huang, Wuhan, CHINA;
Si Ping Hu, Wuhan, CHINA;
Lan Yao, Wuhan, CHINA;
Li Hong Xiao, Wuhan, CHINA;
A Man Zheng, Wuhan, CHINA;
Kun Bao, Wuhan, CHINA;
Haohao Yang, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/098962 08/06/2018

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
CHINA 201710750398.4 08/28/2017 No Access Code Provided

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Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 10/11/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/126,956**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

STAIRCASE STRUCTURE FOR MEMORY DEVICE

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

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community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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PGR2025-00021

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/126,956

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/126,956	09/10/2018	Zhenyu LU	4123.0460002

CONFIRMATION NO. 3036

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FORMALITIES LETTER

OC000000102989334

Date Mailed: 10/15/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

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Micron v. YMTC
PGR2025-00021

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Zhenyu LU
  Jun Chen
  Xiaowang Dai
  Jifeng Zhu
  Qian Tao
  Yu Ru Huang
  Si Ping Hu
  Lan Yao
  Li Hong Xiao
  A Man Zheng
  Kun Bao
  Haohao Yang

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/hachristian/

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Micron v. YMTC
PGR2025-00021

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/126,956	09/10/2018	Zhenyu LU	4123.0460002

CONFIRMATION NO. 3036

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FORMALITIES LETTER

OC000000102989334

Date Mailed: 10/15/2018

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Items Required To Avoid Processing Delays:

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Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Zhenyu LU
  Jun Chen
  Xiaowang Dai
  Jifeng Zhu
  Qian Tao
  Yu Ru Huang
  Si Ping Hu
  Lan Yao
  Li Hong Xiao
  A Man Zheng
  Kun Bao
  Haohao Yang

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/hachristian/

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Electronic Patent Application Fee Transmittal

Application Number:	16126956
Filing Date:	10-Sep-2018
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Filer:	Donald J. Featherstone/Catherine Saunders
Attorney Docket Number:	4123.0460002

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1880

Electronic Acknowledgement Receipt	
EFS ID:	34467621
Application Number:	16126956
International Application Number:	
Confirmation Number:	3036
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Customer Number:	26111
Filer:	Donald J. Featherstone/Catherine Saunders
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0460002
Receipt Date:	03-DEC-2018
Filing Date:	10-SEP-2018
Time Stamp:	17:01:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1880
RAM confirmation Number	120418INTEFSW17024101
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	Cover-Letter-4123-0460002.PDF	227541 2eb93d2bbc4b12942aacaaf2bf7c1b057de9300c	no	2
Warnings:					
Information:					
2	Oath or Declaration filed	Declaration-4123-0460002.PDF	143417 405c4fbea5c2e034c31c6d38dbdb00ee2d7a1d57	no	5
Warnings:					
Information:					
3	Applicant Response to Pre-Exam Formalities Notice	Notice-Missing-Parts-4123-0460002.PDF	86319 c14803bd47112f394080893ed026945bec82f849	no	2
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	37013 291561e12a94ee516324758c172e423c3f531fff	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	494290		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

December 3, 2018

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 3036
Mail Stop Missing Parts

Re: U.S. Patent Application
Appl. No. 16/126,956; Filed: September 10, 2018
For: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**
Inventors: LU *et al.*
Our Ref: 4123.0460002

Commissioner:

In reply to the "Notice to File Missing Parts of Non-Provisional Application," dated October 15, 2018, Applicant transmit the following documents for appropriate action by the U.S. Patent and Trademark Office:

1. Online Credit Card Payment Authorization for **$1,880.00** to cover:

   $ 1,720.00 Patent Application fee (including basic filing, search and examination fees)
   $ 160.00 Surcharge for late filing fee or late Oath or Declaration;

2. Original Combined Declaration and Assignment, executed by the inventors; and

3. Copy of Notice to File Missing Parts of Nonprovisional Application.

The above-listed documents are filed electronically.

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Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/KTS/cms
Enclosures

10373744_1.docx

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Micron v. YMTC
PGR2025-00021

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 16/126,956

filed on September 10, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **STAIRCASE STRUCTURE FOR MEMORY DEVICE** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

18A4285-0001CC7-10.18.40.58
32766-20/10/2018 17:07

Micron Ex. 1019, p. 74
Micron v. YMTC
PGR2025-00021

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Zhenyu LU** Date: 2018.10.23

Signature of Inventor: Zhenyu Lu

LEGAL NAME OF INVENTOR

Inventor: **Jun CHEN** Date: 2018.10.23

Signature of Inventor: Jun CHEN

LEGAL NAME OF INVENTOR

Inventor: **Xiaowang DAI** Date: 2018.11.3

Signature of Inventor: Xiaowang DAI

LEGAL NAME OF INVENTOR

Inventor: **Jifeng ZHU** Date: 2018.10.22

Signature of Inventor: Jifeng ZHU

18A4285-0001CC7A-10.18.40.58
32766-20/10/2018 17:07

E904117-05/11/2018 16:39

Micron Ex. 1019, p. 75
Micron v. YMTC
PGR2025-00021

LEGAL NAME OF INVENTOR

Inventor: **Qian TAO** Date: 2018.11.3

Signature of Inventor: Qian Tao

LEGAL NAME OF INVENTOR

Inventor: **Yu Ru HUANG** Date: 2018.11.5.

Signature of Inventor: Yu Ru Huang

LEGAL NAME OF INVENTOR

Inventor: **Si Ping HU** Date: 2018.11.05

Signature of Inventor: Si Ping HU

LEGAL NAME OF INVENTOR

Inventor: **Lan YAO** Date: 2018.10.22

Signature of Inventor: Lan Yao

LEGAL NAME OF INVENTOR

Inventor: **Li Hong XIAO** Date: 2018.10.22.

Signature of Inventor: Lihong Xiao

18A4285-0001CC7P-10.18.40.58
32766-20/10/2018 17:07

E904117-05/11/2018 16:44

Micron Ex. 1019, p. 76
Micron v. YMTC
PGR2025-00021

LEGAL NAME OF INVENTOR

Inventor: **A Man ZHENG** Date: 2018/10/22

Signature of Inventor: A Man ZHENG

LEGAL NAME OF INVENTOR

Inventor: **Kun BAO** Date: 2018/10/22

Signature of Inventor: Kun BAO

LEGAL NAME OF INVENTOR

Inventor: **Haohao YANG** Date: 2018/10/22

Signature of Inventor: Haohao YANG

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18A4285-0001CC7P-10.18.40.58
32766-20/10/2018 17:07

Micron Ex. 1019, p. 77
Micron v. YMTC
PGR2025-00021

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5263698

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
ZHENYU LU	10/23/2018
JUN CHEN	10/23/2018
XIAOWANG DAI	11/03/2018
JIFENG ZHU	10/22/2018
QIAN TAO	11/03/2018
YU RU HUANG	11/05/2018
SI PING HU	11/05/2018
LAN YAO	10/22/2018
LI HONG XIAO	10/22/2018
A MAN ZHENG	10/22/2018
KUN BAO	10/22/2018
HAOHAO YANG	10/22/2018

RECEIVING PARTY DATA

Name:	YANGTZE MEMORY TECHNOLOGIES CO., LTD.
Street Address:	18 GAOXIN 4TH ROAD
City:	WUHAN, HUBEI
State/Country:	CHINA

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	16126956

CORRESPONDENCE DATA

Fax Number: (202)371-2540

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 202-371-2600
Email: kshiu@sternekessler.com, ttopssecretary1@sternekessler.com
Correspondent Name: STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C
Address Line 1: 1100 NEW YORK AVENUE, N.W.
Address Line 4: WASHINGTON, D.C. 20005

ATTORNEY DOCKET NUMBER:	4123.0460002
NAME OF SUBMITTER:	DONALD J. FEATHERSTONE
SIGNATURE:	/Donald J. Featherstone/
DATE SIGNED:	12/03/2018
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 5
source=2018-12-03-Assignment-4123-0460002#page1.tif
source=2018-12-03-Assignment-4123-0460002#page2.tif
source=2018-12-03-Assignment-4123-0460002#page3.tif
source=2018-12-03-Assignment-4123-0460002#page4.tif
source=2018-12-03-Assignment-4123-0460002#page5.tif

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 16/126,956

filed on September 10, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **STAIRCASE STRUCTURE FOR MEMORY DEVICE** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

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(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

18A4285-0001CC7A-10.18.40.58
32766-20/10/2018 17:07

Micron Ex. 1019, p. 81
Micron v. YMTC
PGR2025-00021

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Zhenyu LU** Date: 2018.10.23

Signature of Inventor: Zhenyu Lu

LEGAL NAME OF INVENTOR

Inventor: **Jun CHEN** Date: 2018.10.23

Signature of Inventor: Jun CHEN

LEGAL NAME OF INVENTOR

Inventor: **Xiaowang DAI** Date: 2018.11.3

Signature of Inventor: Xiaowang DAI

LEGAL NAME OF INVENTOR

Inventor: **Jifeng ZHU** Date: 2018.10.22

Signature of Inventor: Jifeng ZHU

18A4285-0001CC7P-10.18.40.58
32766-20/10/2018 17:07

E904117-05/11/2018 16:39

Micron Ex. 1019, p. 82
Micron v. YMTC
PGR2025-00021

LEGAL NAME OF INVENTOR

Inventor: **Qian TAO** Date: 2018.11.3

Signature of Inventor: Qian Tao

LEGAL NAME OF INVENTOR

Inventor: **Yu Ru HUANG** Date: 2018.11.5.

Signature of Inventor: Yu Ru Huang

LEGAL NAME OF INVENTOR

Inventor: **Si Ping HU** Date: 2018.11.05

Signature of Inventor: Si Ping HU

LEGAL NAME OF INVENTOR

Inventor: **Lan YAO** Date: 2018.10.22

Signature of Inventor: Lan Yao

LEGAL NAME OF INVENTOR

Inventor: **Li Hong XIAO** Date: 2018.10.22.

Signature of Inventor: Lihong Xiao

18A4285-0001CC7P-10.18.40.58
32766-20/10/2018 17:07

E904117-05/11/2018 16:44

Micron Ex. 1019, p. 83
Micron v. YMTC
PGR2025-00021

LEGAL NAME OF INVENTOR

Inventor: **A Man ZHENG** Date: 2018/10/22

Signature of Inventor: A Man ZHENG

LEGAL NAME OF INVENTOR

Inventor: **Kun BAO** Date: 2018/10/22

Signature of Inventor: Kun BAO

LEGAL NAME OF INVENTOR

Inventor: **Haohao YANG** Date: 2018/10/22

Signature of Inventor: Haohao YANG

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32766-20/10/2018 17:07

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Micron v. YMTC
PGR2025-00021

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/126,956	09/10/2018	2811	1880	4123.0460002	20	3

CONFIRMATION NO. 3036

UPDATED FILING RECEIPT

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

OC000000104250491

Date Mailed: 12/06/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Zhenyu LU, Wuhan, CHINA;
Jun Chen, Wuhan, CHINA;
Xiaowang Dai, Wuhan, CHINA;
Jifeng Zhu, Wuhan, CHINA;
Qian Tao, Wuhan, CHINA;
Yu Ru Huang, Wuhan, CHINA;
Si Ping Hu, Wuhan, CHINA;
Lan Yao, Wuhan, CHINA;
Li Hong Xiao, Wuhan, CHINA;
A Man Zheng, Wuhan, CHINA;
Kun Bao, Wuhan, CHINA;
Haohao Yang, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/098962 08/06/2018

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
CHINA 201710750398.4 08/28/2017 No Access Code Provided

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Micron v. YMTC
PGR2025-00021

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 10/11/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/126,956**

Projected Publication Date: 03/14/2019

Non-Publication Request: No

Early Publication Request: No

Title

STAIRCASE STRUCTURE FOR MEMORY DEVICE

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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PGR2025-00021

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/126,956

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/126,956	09/10/2018	Zhenyu LU	4123.0460002

CONFIRMATION NO. 3036

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

PUBLICATION NOTICE

OC000000106584827

Title:STAIRCASE STRUCTURE FOR MEMORY DEVICE

Publication No.US-2019-0081070-A1
Publication Date:03/14/2019

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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PTO/SB/08a (07-09)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	16/126,956
Filing Date	September 10, 2018
First Named Inventor	Lu et al.
Art Unit	2811
Examiner Name	GURLEY, LYNNE ANN
Attorney Docket Number	4123.0460002

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 2015/0255385 A1	09-10-2015	Lee et al.	
	2	US- 2019/0081070 A1	03-14-2019	Lu et al.	
	3	US- 9,419,013 B1	08-16-2016	Lee et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	FP1	CN-106601746-A	04-26-2017	SAMSUNG ELECTRONICS CO LT		
	FP2	CN-107644876-A	01-30-2018	YANGTZE MEMORY TECH CO LT		
	FP3	KR-20110015338-A	02-15-2011	HYNIX SEMICONDUCTOR INC.		✔

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Sheet 1 of 1

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First Named Inventor	Lu et al.
Art Unit	2811
Examiner Name	GURLEY, LYNNE ANN
Attorney Docket Number	4123.0460002

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/098962, mailed November 7, 2018; 8 pages.	

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

(19)中华人民共和国国家知识产权局

(12)发明专利申请

(10)申请公布号 CN 106601746 A
(43)申请公布日 2017.04.26

(21)申请号 201610461705.2

(22)申请日 2016.06.23

(30)优先权数据
10-2015-0153303 2015.11.02 KR
62/238,881 2015.10.08 US

(71)申请人 三星电子株式会社
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(74)专利代理机构 北京铭硕知识产权代理有限公司 11286
代理人 韩明星 刘灿强

(51)Int.Cl.
H01L 27/115(2017.01)
H01L 21/8239(2006.01)
H01L 21/8234(2006.01)

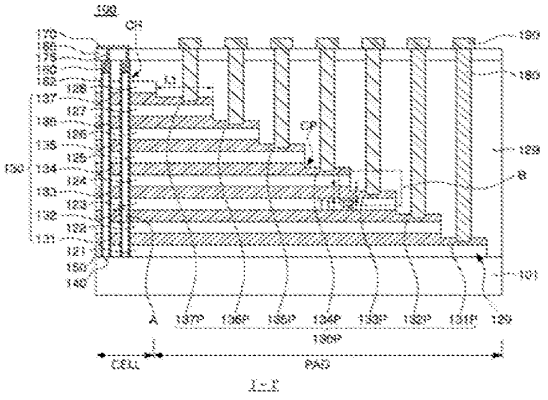
权利要求书2页 说明书16页 附图28页

(54)发明名称

半导体器件及其制造方法

(57)摘要

提供了一种半导体器件，该半导体器件包括：栅电极，垂直地堆叠在基底上；通道孔，垂直地延伸到基底，通道孔穿过栅电极，通道孔具有通道区域；栅极焊盘，以不同的长度从栅电极延伸；接触塞，连接到栅极焊盘，栅极焊盘的至少一部分具有厚度比连接到栅极焊盘的所述至少一部分的栅电极的厚度小的区域。



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1.一种半导体器件,所述半导体器件包括:

栅电极,垂直地堆叠在基底上;

通道孔,垂直地延伸到基底,所述通道孔穿过栅电极,所述通道孔具有通道区域;

栅极焊盘,以不同的长度从栅电极延伸;以及

接触塞,连接到栅极焊盘,

栅极焊盘的至少一部分具有厚度比连接到栅极焊盘的所述至少一部分的栅电极的厚度小的区域。

2.如权利要求1所述的半导体器件,其中:

栅极焊盘包括接触区域,在接触区域中,下栅极焊盘延伸得比连接到接触塞的上栅极焊盘远;以及

接触区域中的栅极焊盘的厚度比栅电极的厚度小。

3.如权利要求2所述的半导体器件,其中,在全部接触区域中,栅极焊盘具有比栅电极的厚度小的厚度。

4.如权利要求2所述的半导体器件,其中,在接触区域中,栅极焊盘具有连续地并逐渐地减小的厚度。

5.如权利要求2所述的半导体器件,其中,栅极焊盘中的每个具有在接触区域附近栅极焊盘的厚度不连续地并迅速地减小的弯曲部分,在除了弯曲部分外的区域,栅极焊盘中的每个水平地延伸。

6.如权利要求1所述的半导体器件,其中,栅极焊盘与连接到栅极焊盘的栅电极之间的厚度的差在每个栅极焊盘中不同。

7.如权利要求6所述的半导体器件,其中,栅极焊盘中厚度的差从基底的上表面沿向上的方向增加。

8.如权利要求6所述的半导体器件,其中,栅极焊盘中厚度的差在包括两个或更多个栅极焊盘的组单元中从基底的上表面沿向上的方向增加。

9.如权利要求1所述的半导体器件,所述半导体器件还包括栅极焊盘上的刻蚀停止层,

其中,接触塞穿过刻蚀停止层。

10.如权利要求9所述的半导体器件,其中,刻蚀停止层与栅极焊盘接触。

11.一种半导体器件,所述半导体器件包括:

栅电极,垂直地堆叠在基底上;

栅极焊盘,具有接触区域,所述栅极焊盘以不同的长度从栅电极延伸;以及

接触塞,在接触区域中连接到栅极焊盘,

在接触区域中,栅极焊盘的至少一部分具有减小的厚度。

12.如权利要求11所述的半导体器件,其中,接触区域包括栅极焊盘中的下栅极焊盘延伸得比栅极焊盘中的上栅极焊盘远的区域。

13.如权利要求11所述的半导体器件,其中,栅极焊盘中的每个具有台阶部分或弯曲部分,使得在接触区域中,栅极焊盘中的每个具有减小的厚度。

14.如权利要求11所述的半导体器件,其中,栅电极与连接到栅电极的栅极焊盘的厚度的差在约5Å至约100Å的范围内。

15.如权利要求11所述的半导体器件,其中,栅极焊盘的厚度的减小程度和栅极焊盘与

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基底之间的距离成正比或成反比。

16.一种制造半导体器件的方法，所述方法包括：

在基底上交替地堆叠牺牲层和层间绝缘层；

在彼此堆叠的牺牲层和层间绝缘层上形成掩模层；

通过使用掩模层去除牺牲层和层间绝缘层的部分从而以不同的长度延伸来形成焊盘区域；

在焊盘区域中形成包括氧化物基材料的焊盘绝缘层；

去除牺牲层；以及

通过用导电材料填充从其去除了牺牲层的区域来形成栅电极，

在形成焊盘绝缘层的过程中，使牺牲层在焊盘区域的至少部分被氧化以形成氧化物层。

17.如权利要求16所述的方法，其中，通过源材料从牺牲层的上表面使牺牲层的部分氧化，用于焊盘绝缘层的形成。

18.如权利要求16所述的方法，其中，在去除牺牲层的过程中，保留氧化物层不被去除。

19.如权利要求18所述的方法，其中，在氧化物层下方，栅电极中的每个具有减小的厚度。

20.如权利要求16所述的方法，其中，远离基底的上表面，增加氧化物层的厚度。

21.一种半导体器件，所述半导体器件包括：

栅电极，堆叠在基底上；以及

栅极焊盘，从栅电极中的每个延伸，栅极焊盘中的每个从栅电极中的每个延伸不同的长度；

在延伸得比栅极焊盘中的上栅极焊盘长的区域，栅极焊盘中的每个具有减小的厚度。

22.如权利要求21所述的半导体器件，其中，栅极焊盘中的至少一个具有凹进形状的弯曲部分，所述凹进形状的弯曲部分为从其延伸的栅极焊盘提供减小的厚度。

23.如权利要求22所述的半导体器件，其中，在全部区域中，从具有凹进形状的弯曲部分的栅电极中的所述至少一个延伸的栅极焊盘具有与基底平行并延伸得比上栅极焊盘长的上表面。

24.如权利要求23所述的半导体器件，其中，栅极焊盘中的每个包括接触区域。

25.如权利要求24所述的半导体器件，所述半导体器件还包括连接到接触区域中的每个的接触塞。

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半导体器件及其制造方法

[0001] 本申请要求于2015年10月8日在USPTO提交的第62/238,881号美国临时申请的优先权,出于全部目的,通过引用将其内容全部包含于此。

[0002] 通过引用,将于2015年11月2日在韩国知识产权局提交的名为“Semiconductor Device and Method of Manufacturing the Same”(半导体器件及其制造方法)的第10-2015-0153303号韩国专利申请全部包含于此。

技术领域

[0003] 实施例涉及一种半导体器件及其制造方法。

背景技术

[0004] 可能存在对于能够处理大量数据的电子产品的市场需求,同时电子产品的体积可以减小。可能需要提升在这样的电子产品中使用的半导体器件的集成程度。

发明内容

[0005] 可以通过提供一种半导体器件来实现实施例,所述半导体器件包括:栅电极,垂直地堆叠在基底上;通道孔,垂直地延伸到基底,通道孔穿过栅电极,通道孔具有通道区域;栅极焊盘,以不同的长度从栅电极延伸;接触塞,连接到栅极焊盘,栅极焊盘的至少一部分具有厚度比连接到栅极焊盘的所述至少一部分的栅电极的厚度小的区域。

[0006] 栅极焊盘可以包括下栅极焊盘延伸得比连接到接触塞的上栅极焊盘远的接触区域,接触区域中的栅极焊盘的厚度可以比栅电极的厚度小。

[0007] 在全部接触区域中,栅极焊盘可以具有比栅电极的厚度小的厚度。

[0008] 在接触区域中,栅极焊盘可以具有连续地并逐渐地减小的厚度。

[0009] 栅极焊盘中的每个可以具有在接触区域附近栅极焊盘的厚度不连续地并迅速地减小的弯曲部分,在除了弯曲部分外的区域,栅极焊盘中的每个水平地延伸。

[0010] 栅极焊盘与连接到栅极焊盘的栅电极之间的厚度的差在每个栅极焊盘中可以不同。

[0011] 栅极焊盘中厚度的差可以从基底的上表面沿向上的方向增加。

[0012] 栅极焊盘中厚度的差可以在包括两个或更多个栅极焊盘的组单元中从基底的上表面沿向上的方向增加。

[0013] 半导体器件还可以包括栅极焊盘上的刻蚀停止层。接触塞可以穿过刻蚀停止层。

[0014] 刻蚀停止层可以与栅极焊盘接触。

[0015] 可以通过提供一种半导体器件来实现实施例,所述半导体器件包括:栅电极,垂直地堆叠在基底上;栅极焊盘,具有接触区域,栅极焊盘以不同的长度从栅电极延伸;接触塞,在接触区域中连接到栅极焊盘,在接触区域中,栅极焊盘的至少一部分具有减小的厚度。

[0016] 接触区域可以包括栅极焊盘中的下栅极焊盘延伸得比栅极焊盘中的上栅极焊盘远的区域。

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[0017] 栅极焊盘中的每个可以具有台阶部分或弯曲部分，使得在接触区域中，栅极焊盘中的每个具有减小的厚度。

[0018] 栅电极与连接到栅电极的栅极焊盘的厚度的差可以在约5Å至约100Å的范围内。

[0019] 栅极焊盘的厚度的减小程度和栅极焊盘与基底之间的距离可以成正比或成反比。

[0020] 可以通过提供一种制造半导体器件的方法来实现实施例，所述制造半导体器件的方法包括：在基底上交替地堆叠牺牲层和层间绝缘层；在彼此堆叠的牺牲层和层间绝缘层上形成掩模层；通过使用掩模层去除牺牲层和层间绝缘层的部分从而以不同的长度延伸来形成焊盘区域；在焊盘区域中形成包括氧化物基材料的焊盘绝缘层；去除牺牲层；通过用导电材料填充从其去除了牺牲层的区域来形成栅电极，在形成焊盘绝缘层的过程中，使牺牲层在焊盘区域的至少部分被氧化以形成氧化物层。

[0021] 可以通过源材料从牺牲层的上表面使牺牲层的部分氧化，用于焊盘绝缘层的形成。

[0022] 在去除牺牲层的过程中，可以保留氧化物层不被去除。

[0023] 在氧化物层下方，栅电极中的每个可以具有减小的厚度。

[0024] 远离基底的上表面，可以增加氧化物层的厚度。

[0025] 可以通过提供一种半导体器件来实现实施例，所述半导体器件包括：栅电极，堆叠在基底上；栅极焊盘，从栅电极中的每个延伸，栅极焊盘中的每个从栅电极中的每个延伸不同的长度；在延伸得比栅极焊盘中的上栅极焊盘长的区域，栅极焊盘中的每个具有减小的厚度。

[0026] 栅极焊盘中的至少一个可以具有凹进形状的弯曲部分，所述凹进形状的弯曲部分为从其延伸的栅极焊盘提供减小的厚度。

[0027] 在全部区域中，从具有凹进形状的弯曲部分的栅电极中的所述至少一个延伸的栅极焊盘可以具有与基底平行并延伸得比上栅极焊盘长的上表面。

[0028] 栅极焊盘中的每个可以包括接触区域。

[0029] 半导体器件还可以包括连接到接触区域中的每个的接触塞。

附图说明

[0030] 通过参照附图详细地描述示例性实施例，对于本领域的技术人员，特征将变为清楚的，其中：

[0031] 图1示出了根据示例实施例的半导体器件的示意性框图；

[0032] 图2示出了根据示例实施例的半导体器件的存储单元阵列的等效电路图；

[0033] 图3示出了根据示例实施例的半导体器件的示意性平面图；

[0034] 图4示出了根据示例实施例的半导体器件的示意性剖视图；

[0035] 图5A至图5C示出了根据示例实施例的栅极介电层的剖视图；

[0036] 图6A至图6C示出了根据示例实施例的栅极焊盘的剖视图；

[0037] 图7至图9示出了根据示例实施例的半导体器件的示意性剖视图；

[0038] 图10A至图10K示意性地示出了根据示例实施例的制造半导体器件的方法的主要工艺的图；

[0039] 图11A至图11D示意性地示出了根据示例实施例的制造半导体器件的方法的主要

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工艺的图；

[0040] 图12示出了根据示例实施例的半导体器件的示意性透视图；

[0041] 图13示出了包括根据示例实施例的半导体器件的存储装置的框图；

[0042] 图14示出了包括根据示例实施例的半导体器件的电子设备的框图；以及

[0043] 图15示出了包括根据示例实施例的半导体器件的系统的示意图。

具体实施方式

[0044] 现在将在下文中参照附图更充分地描述示例实施例；然而，示例实施例可以以不同的形式实施而不应被解释为限于此处所阐述的实施例。相反，这些实施例被提供为使得本公开将是彻底的和完整的，并且将把示例性实施方式充分地传达给本领域的技术人员。

[0045] 在图中，为了图示的清晰起见，会夸大层和区域的尺寸。在整个说明书中，将理解的是，当诸如层、区域或晶片(基底)的元件被称为“在”另一元件“上”、“连接到”或“结合到”另一元件时，该元件可以直接“在”另一元件“上”、直接“连接到”或“结合到”另一元件，或者可以在它们之间存在其他中间元件。相反，当元件被称为“直接在”另一元件“上”、“直接连接到”或“直接结合到”另一元件时，在它们之间不会存在元件或层。此外，将理解的是，当层被称为“在”另一层“下”时，该层可以直接在另一层下，也可以存在一个或多个中间层。另外，还将理解的是，当层被称为“在”两层“之间”时，该层可以是在两层之间的唯一层，或者也可以存在一个或多个中间层。同样的标记始终表示同样的元件。如在这里使用的，术语“和/或”包括相关列出项中的一个或多个的任意和全部组合。

[0046] 将清楚的是，虽然可以在这里使用术语第一、第二、第三等来描述各种构件、组件、区域、层和/或部分，但是这些构件、组件、区域、层和/或部分不应被这些术语所限制。这些术语仅用来将一个构件、组件、区域、层或部分与另一区域、层或部分区分开来。因此，在不脱离示例实施例的教导的情况下，下面讨论的第一构件、第一组件、第一区域、第一层或第一部分可以命名为第二构件、第二组件、第二区域、第二层或第二部分。

[0047] 为了易于描述，在这里可以使用诸如“在…上方”、“上”、“在…下方”和“下”等的空间相对术语来描述如在图中所示出的一个元件与另外的元件的关系。将理解的是，空间相对术语意图包括除了在图中描绘的方位外装置在使用或操作中的不同方位。例如，如果翻转图中的装置，那么描述为“在”其他元件“上方”或“上”的元件将随后定位为“在”其他元件或特征“下方”或“下”。因此，基于图的具体方向，术语“在…上方”可以包括“在…上方”和“在…下方”两种方位。可以另外定位(旋转90度或在其他方位)所述装置，并相应地解释在这里使用的空间相对描述语。

[0048] 在这里使用的术语仅是为了描述具体实施例的目的，而不意图限制。如在这里使用的，除非上下文另外明确地指出，否则单数形式“一个(种)”和“所述(该)”也意图包括复数形式。还将理解的是，术语“包括”用在本说明书中时，说明存在所述特征、整体、步骤、操作、构件、元件和/或它们的组，但不排除存在或附加一个或多个其他特征、整体、步骤、操作、构件、元件和/或它们的组。

[0049] 在下文中，将参照示出实施例的示意性图描述实施例。在图中，例如由于制造技术和/或工差，示出的形状的修改是可以预计的。因此，实施例不应被解释为限于例如在这里示出的区域的具体形状，以包括由制造引起的形状的改变。下面的实施例也可以由一个实

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施例或实施例的组合所组成。

[0050] 下面描述的内容可以具有各种构造并在这里仅提出了一个需要的构造，但不限于此。

[0051] 在本说明书中，术语“哑”仅用作表示仅作为图案存在而不执行实际功能的构造的术语，即使该构造与其他组成元件相同或者具有与其相似的结构和形状。因此，“哑”组成元件不具有施加到其的电信号，也不执行特定的电学功能。

[0052] 图1示出了根据示例实施例的半导体器件的示意性框图。

[0053] 参照图1，根据示例实施例的半导体器件10可以包括存储单元阵列20、驱动电路30、读/写电路40和控制电路50。

[0054] 存储单元阵列20可以包括多个存储单元。多个存储单元可以按多个行和多个列布置。存储单元阵列20中包括的多个存储单元可以通过字线WL、共源线CSL、串选择线SSL、地选择线GSL等连接到驱动电路30，并可以通过位线BL连接到读/写电路40。在本公开的示例实施例中，按单行线性布置的多个存储单元可以连接到单条字线WL，按单列线性布置的多个存储单元可以连接到单条位线BL。

[0055] 存储单元阵列20中包括的多个存储单元可以分成多个存储块。各个存储块可以包括多条字线WL、多条串选择线SSL、多条地选择线GSL、多条位线BL和至少一条共源线CSL。

[0056] 驱动电路30和读/写电路40可以通过控制电路50操作。在示例实施例中，驱动电路30可以接收外部提供的地址信息ADDR，并可以将接收的地址信息ADDR解码以选择连接到存储单元阵列的字线WL、共源线CSL、串选择线SSL和地选择线GSL的至少一部分。驱动电路30可以包括用于字线WL、串选择线SSL和共源线CSL中的每个的驱动电路。

[0057] 读/写电路40可以响应于从控制电路50提供的命令来选择连接到存储单元阵列20的位线BL的至少一部分。读/写电路40可以读取已写入连接到所选择的位线BL的至少一部分的存储单元的数据或者可以向连接到所选择的位线BL的至少一部分的存储单元写入数据。读/写电路40可以包括诸如页缓冲器、输入/输出缓冲器、数据锁存等的电路。

[0058] 控制电路50可以响应于外部传输的控制信号CTRL来控制驱动电路30和读/写电路40的操作。在读取已写入存储单元阵列20中的数据的情况下，控制电路50可以控制驱动电路30的操作以向其中存储有将被读取的数据的字线WL提供电压，进行读取操作。当向特定的字线WL提供用于读取操作的电压时，控制电路50可以执行控制使得读/写电路40可以读取已写入连接到已经接收用于读取操作的电压的字线WL的存储单元的数据。

[0059] 当数据写入存储单元阵列20时，例如，控制电路50可以控制驱动电路30的操作以向将要写入数据的字线WL提供用于写入操作的电压。当用于写入操作的电压提供给特定的字线WL时，控制电路50可以控制读/写电路40以向连接到已经向其提供用于写入操作的电压的字线WL的存储单元写入数据。

[0060] 图2示出了根据示例实施例的半导体器件的存储单元阵列的等效电路图。

[0061] 图2示出了竖直半导体器件100A中包括的存储单元阵列的三维结构的等效电路图。参照图2，根据示例实施例的存储单元阵列可以包括具有彼此串联连接的n个存储单元MC1至MCn的多个存储单元串S以及分别连接到串联的n个存储单元MC1至MCn的两端的地选择晶体管GST和串选择晶体管SST。

[0062] 彼此串联连接的n个存储单元MC1至MCn可以分别连接到字线WL1至WLn，以选择n个

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存储单元MC1至MCn的至少一部分。

[0063] 地选择晶体管GST的栅极端子可以连接到地选择线GSL，其源极端子可以连接到共源线CSL。串选择晶体管SST的栅极端子可以连接到串选择线SSL，其源极端子可以连接到存储单元MCn的漏极端子。图2示出了这样的结构，在该结构中，一个地选择晶体管GST和一个串选择晶体管SST分别连接到彼此串联连接的n个存储单元MC1至MCn；按照与此不同的方式，多个地选择晶体管GST或多个串选择晶体管SST可以连接到n个存储单元MC1至MCn。

[0064] 串选择晶体管SST的漏极端子可以连接到位线BL1至BLm。当信号通过串选择线SSL施加到串选择晶体管SST的栅极端子时，通过位线BL1至BLm施加的信号可以传输到彼此串联连接的n个存储单元MC1至MCn，使得可以执行数据读取操作或数据写入操作。因为信号经过栅极选择线施加到其源极端子连接到共源线CSL的栅极选择晶体管GST的栅极端子，可以执行全部去除存储在n个存储单元MC1至MCn中的电荷的擦除操作。

[0065] 图3示出了根据示例实施例的半导体器件的示意性平面图。图3部分地示出了组成元件的结构，为了便于描述，从其省略了一些诸如焊盘绝缘层129(见图4)的构造。

[0066] 图4示出了根据示例实施例的半导体器件的示意性剖视图。图4示出了沿着图3的线I-I'截取的半导体器件的剖面。

[0067] 参照图3和图4，半导体器件100可以包括单元区域CELL和焊盘区域PAD。焊盘区域PAD可以沿x方向设置在单元区域CELL的至少一端上。单元区域CELL可以与图1的存储单元阵列20对应，焊盘区域PAD可以是将图1的存储单元阵列20与驱动电路30彼此电连接的区域。

[0068] 在单元区域CELL中，半导体器件100可以包括：栅电极131至137(栅电极130)，在沿着与基底101的上表面垂直的方向彼此分隔开的同时堆叠在基底101上；层间绝缘层121至127(层间绝缘层120)，与栅电极130交替地堆叠；通道孔CH，沿与基底101的上表面垂直的方向延伸并且其中设置有通道区域140；通道焊盘160，设置在通道孔CH的上端上；第一布线170和通道塞175，设置在通道焊盘160上。半导体器件100还可以包括通道孔CH内的通道区域140和栅极介电层150。在半导体器件100中，单个存储单元串可以基于每个通道孔CH来配置，多个存储单元串可以沿x方向和y方向按行和列布置。

[0069] 在焊盘区域PAD中，半导体器件100可以包括从栅电极131至137(栅电极130)水平延伸的栅极焊盘131P至137P(栅极焊盘130P)、连接到栅极焊盘130P的接触塞180、设置在接触塞180上的第二布线190和具有与通道孔CH相同结构的哑通道孔CHD。

[0070] 基底101可以具有沿x方向和y方向延伸的上表面。基底101可以包括半导体材料，例如IV族半导体材料、III-V族化合物半导体材料或II-VI族氧化物半导体材料。例如，IV族半导体可以包括硅、锗或硅-锗。基底101可以作为体晶片或外延层提供。

[0071] 栅电极130(例如131至137)可以沿着通道孔CH的各个侧面在与基底101的上表面垂直的方向上彼此分隔开。参照图2，栅电极130可以分别形成地选择晶体管GST的栅极、多个存储单元MC1至MCn的栅极和串选择晶体管SST的栅极。栅电极130可以在形成字线WL1至WLn的同时延伸。栅电极130可以公共地连接到通过预定单元提供并且沿x方向和y方向布置的彼此相邻的存储单元串，堆叠有栅电极130的堆叠结构可以如图3所示通过沟槽TH在y方向上彼此分离。

[0072] 在示例实施例中，在存储单元MC1至MCn的栅电极132至135的情况下，可以布置例

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如四个栅电极。例如，形成存储单元MC1至MCn的栅电极130的数量可以取决于半导体器件100的容量。例如，形成存储单元MC1至MCn的栅电极130的数量可以是2^n，其中，n是自然数。

[0073] 地选择晶体管GST的栅电极131可以沿x方向延伸以形成地选择线GSL。串选择晶体管SST的栅电极136和137可以沿x方向延伸以形成串选择线SSL。沿y方向线性设置的通道孔CH可以根据诸如通道塞175的上布线结构的设置分别连接到不同的第一布线170。在示例实施例中，串选择晶体管SST的栅电极136和137可以在沿y方向线性设置的通道孔CH之间彼此分离以形成不同的串选择线SSL。根据示例实施例，串选择晶体管SST的栅电极136和137以及地选择晶体管GST的栅电极131可以分别是一个、两个或更多个，并且可以具有与存储单元MC1至MCn的栅电极132至135的结构相同的或不同的结构。

[0074] 栅电极130的一部分，例如与地选择晶体管GST的栅电极131相邻的栅电极132或串选择晶体管SST的栅电极136和137可以是哑栅电极。例如，与地选择晶体管GST的栅电极131相邻的栅电极132可以是哑栅电极。

[0075] 栅电极130可以包括多晶硅或金属硅化物材料。金属硅化物材料可以是从例如钴(Co)、镍(Ni)、铪(Hf)、铂(Pt)、钨(W)和钛(Ti)中选择的金属的硅化物材料，或者可以是其组合。根据示例实施例，栅电极130还可以包括例如钨(W)的金属。栅电极130还可以包括扩散障碍层，例如扩散障碍层可以包括氮化钨(WN)、氮化钽(TaN)、氮化钛(TiN)或其组合。

[0076] 共源线CSL可以设置在彼此相邻的栅电极130的堆叠结构之间的沟槽TH中。

[0077] 栅极焊盘130P可以与栅电极130从单元区域CELL向焊盘区域PAD水平延伸的区域对应。因为栅电极130延伸并形成字线WL1至WLn，所以栅极焊盘130P可以称为字线或字线焊盘。栅极焊盘130P可以按不同的长度延伸以具有台阶部分。栅极焊盘130P可以提供下栅极焊盘130P比上栅极焊盘130P长的接触区域。在接触区域中，栅极焊盘130P可以分别通过接触塞180连接到设置在其上的第二布线190，通过接触塞180可以将电信号施加到栅电极130。

[0078] 栅极焊盘130P可以分别包括其厚度比栅电极130的厚度小的区域。栅极焊盘130P可以分别包括从栅电极130以特定厚度延伸并随后以减小的厚度延伸的区域。例如，栅极焊盘130P可以在接触区域具有减小的厚度。在整个接触区域中，栅极焊盘130P可以具有减小的厚度，例如，可以具有作为从第一厚度T1减小的厚度并且比第一厚度T1薄的第二厚度T2。栅极焊盘130P可以分别具有栅极焊盘130P的厚度在接触区域中竖直地减小的台阶部分CP。

[0079] 第一厚度T1与第二厚度T2之间的差可以在大约5Å至大约100Å的范围内，例如大约10Å至大约50Å，并可以在第一厚度T1的1％至35％的范围内。在示例实施例中，栅极焊盘130P与连接到其的栅电极130之间的厚度差(例如，栅极焊盘130P的厚度的减小程度)基本上彼此相等。

[0080] 最上面的栅极焊盘137P可以具有比在焊盘区域PAD中的栅电极137的厚度低的厚度，其以减小的厚度延伸的长度L1可以根据示例实施例而进行各种改变。

[0081] 层间绝缘层120可以布置在栅电极130/栅极焊盘130P之间。层间绝缘层120可以按照与栅电极130的方式相似的方式沿与基底101的上表面垂直的方向彼此分隔开并可以沿x方向延伸。在焊盘区域PAD中，层间绝缘层120还可以沿着栅极焊盘130P以不同的长度延伸。层间绝缘层120可以包括诸如氧化硅或氮化硅的绝缘材料。

[0082] 在单元区域CELL中，在基底101上形成列和行的同时，通道孔CH可以彼此分隔开，

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并可以设置为在x方向朝向彼此位移。例如，通道孔CH可以设置为形成格子图案或者可以沿单个方向以Z字形形式设置。通道孔CH可以按照其高宽比的增加具有朝向基底101成锥形的倾斜的侧表面。通道孔CH的设置可以根据示例实施例进行各种改变。

[0083] 具有柱形形状的通道区域140可以设置在沿与基底101的上表面垂直的方向延伸的通道孔CH中。虽然在通道孔CH内的通道区域140可以以环形形状形成以围绕设置在通道区域140内侧的第一绝缘层162，但是根据示例实施例，通道区域140还可以具有诸如圆柱形形状或棱柱形形状的柱形形状而其中不具有第一绝缘层162。通道区域140的下部可以连接到基底101。通道区域140可以包括诸如多晶硅或单晶硅的半导体材料，半导体材料可以是无掺杂材料或者可以是具有p型杂质或n型杂质的材料。

[0084] 哑通道孔CHD可以设置在焊盘区域PAD中的栅极焊盘130P的端部上。在实施例中，哑通道孔CHD可以沿x方向设置在接触塞180的两侧。哑通道孔CHD可以具有与通道孔CH相同的结构。诸如通道塞175的布线结构可以不设置在哑通道孔CHD的上部上。

[0085] 栅极介电层150可以设置在栅电极130与通道孔CH中的通道区域140之间。栅极介电层150可以沿通道区域140延伸以与基底101的上表面垂直。栅极介电层150可以包括在通道区域140上连续地堆叠的隧穿层、电荷储存层和阻挡层。将在下面参照图5A至5C更详细地描述栅极介电层150。

[0086] 通道焊盘160可以设置在通道区域140的上部上。通道焊盘160可以设置为覆盖第一绝缘层162的上表面并电连接到通道区域140。通道焊盘160可以包括例如掺杂的多晶硅。

[0087] 通道塞175可以穿过第二绝缘层166以连接到通道焊盘160。通道焊盘160可以通过通道塞175电连接到设置在其上的第一布线170。第一布线170可以是位线BL1至BLm(见图2)。

[0088] 第一布线170可以沿与栅电极130延伸的方向不同的方向延伸，例如，第一布线170可以在通道塞175的上部上沿y方向延伸。

[0089] 通道塞175和第一布线170可以包括导电材料，例如，诸如钨(W)、铝(Al)、铜(Cu)等的金属。

[0090] 接触塞180可以穿过第二绝缘层166和焊盘绝缘层129以连接到栅极焊盘130P。因为栅极焊盘130P的高度彼此不同，所以接触塞180可以具有不同的长度。接触塞180可以例如以栅极焊盘130P的部分凹进的方式连接到栅极焊盘130P。根据示例实施例，接触塞180还可以具有其宽度由于相对高的高宽比而向其下部减小的形式。

[0091] 第二布线190可以沿与第一布线170相同的方向延伸，例如在接触塞180上沿y方向延伸。根据示例实施例，连接到串选择晶体管SST的栅电极136和137的栅极焊盘136P和137P可以连接到沿与第二布线190不同的方向延伸的单独布线。

[0092] 接触塞180和第二布线190可以包括导电材料，例如，诸如钨(W)、铝(Al)、铜(Cu)等的金属。

[0093] 图5A至图5C是根据示例实施例的栅极介电层的剖视图，并示出了与图4的区域'A'对应的区域。

[0094] 参照图5A，示出了存储单元串的栅电极132、栅极介电层150和通道区域140。栅极介电层150可以包括在通道区域140上连续地堆叠的隧穿层152、电荷储存层154和阻挡层156。

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[0095] 隧穿层152可以允许将要经过F-N隧穿传输到电荷储存层154的电荷隧穿。隧穿层152可以包括例如二氧化硅(SiO_2)、氮化硅(Si_3N_4)、氮氧化硅(SiON)或其组合。

[0096] 电荷储存层154可以是电荷捕获层或浮栅导电层。例如，电荷储存层154可以包括介电材料、量子点或纳米晶体。量子点或纳米晶体可以由例如金属或半导体纳米颗粒的导体构成。在示例实施例中，例如，当电荷储存层154是电荷捕获层时，电荷储存层154可以包括氮化硅。

[0097] 阻挡层156可以包括二氧化硅(SiO_2)、氮化硅(Si_3N_4)、氮氧化硅(SiON)、高k介电材料或其组合。高k介电材料可以是Al_2O_3、Ta_2O_3、TiO_2、Y_2O_3、ZrO_2、$ZrSi_xO_y$、HfO_2、$HfSi_xO_y$、La_2O_3、$LaAl_xO_y$、$LaHf_xO_y$、$HfAl_xO_y$和Pr_2O_3中的任意一种。

[0098] 参照图5B，示出了存储单元串的栅电极132、栅极介电层150a和通道区域140。栅极介电层150a可以具有隧穿层152、电荷储存层154和阻挡层156a顺序堆叠在通道区域140上的结构。可以各种改变上述形成栅极介电层150a的层的相对厚度。

[0099] 详细来说，在根据示例实施例的栅极介电层150a中，隧穿层152和电荷储存层154可以沿着通道区域140竖直地延伸，而阻挡层156a可以按照与图5A的示例实施例不同的方式设置为围绕栅电极132。在示例实施例中，阻挡层156a的一部分可以沿着通道区域140竖直地延伸，其另一部分可以设置为围绕栅电极132。

[0100] 参照图5C，示出了存储单元串的栅电极132、栅极介电层150b和通道区域140。栅极介电层150b可以具有隧穿层152b、电荷储存层154b和阻挡层156b顺序堆叠在通道区域140上的结构。

[0101] 详细来说，在根据示例实施例的栅极介电层150b中，隧穿层152b、电荷储存层154b和阻挡层156b全部可以按照与图5A和图5B的示例实施例不同的方式设置为围绕栅电极132。

[0102] 图6A至图6C是根据示例实施例的栅极焊盘的剖视图并示出了与图4的区域'B'对应的区域。

[0103] 参照图6A，示出了栅极焊盘133Pa和接触塞180。栅极焊盘133Pa可以包括在连接到栅电极133的同时延伸的扩展区域PA和延伸为比上栅极焊盘134Pa长并且连接到接触塞180的接触区域PB。

[0104] 根据示例实施例的栅极焊盘133Pa可以按照与图4的示例实施例不同的方式具有逐渐地或连续地减小的厚度。当栅电极133和在扩展区域PA中的栅极焊盘133Pa的厚度为第一厚度T1时，栅极焊盘133Pa的厚度在与连接区域PA相邻的接触区域PB中可以具有比第一厚度T1低的第三厚度T3，并且在与接触区域PB的端部邻近的区域中可以具有比第三厚度T3低的第四厚度T4。

[0105] 参照图6B，栅极焊盘133Pb可以具有弯曲部分CPa，在弯曲部分CPa中，栅极焊盘133Pb的厚度在与扩展区域PA相邻的接触区域PB中按照与图4的示例实施例不同的方式迅速地或不连续地减小。通过弯曲部分CPa，栅极焊盘133Pb的厚度在形成有弯曲部分CPa的区域中可以从第一厚度T1减小到第二厚度T2，栅极焊盘133Pb可以在除了形成有弯曲部分CPa的区域之外的区域中以第二厚度T2延伸为具有例如与基底101平行的平坦的上表面。可以根据示例实施例对弯曲部分CPa的长度L2进行各种改变。

[0106] 参照图6C，栅极焊盘133Pc在与接触区域PB相邻的扩展区域PA中可以按照与图4和

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图6B的示例实施例不同的方式具有凹进形状的弯曲部分CPb。例如，可以根据示例实施例对弯曲部分CPb的位置、凹进的形式和深度进行各种改变。通过弯曲部分CPb，栅极焊盘133Pc的厚度在形成有弯曲部分CPb的区域中可以从第一厚度T1减小到第二厚度T2，栅极焊盘133Pc可以在除了形成有弯曲部分CPb的区域之外的栅极焊盘133Pc的区域中以第二厚度T2延伸为具有例如与基底101平行的平坦的上表面。

[0107] 图7至图9是根据示例实施例的半导体器件的示意性剖视图。

[0108] 参照图7，半导体器件100a可以包括栅电极130、层间绝缘层120、通道孔CH、从栅电极130水平地延伸的栅极焊盘130Pd和连接到栅极焊盘130Pd的接触塞180。

[0109] 栅极焊盘130Pd可以包括栅极焊盘分别以特定厚度从栅电极130延伸并随后以减小的厚度延伸的区域。例如，下栅极焊盘130Pd可以分别具有延伸为比上栅极焊盘130Pd的接触区域长的接触区域以连接到接触塞180并且在接触区域可以具有减小的厚度。

[0110] 栅极焊盘130Pd可以按照与图4的示例实施例不同的方式具有远离基底101的上表面进一步减小的厚度。例如，上栅极焊盘130Pd的厚度的减小程度可以比下栅极焊盘130Pd的厚度的减小程度大。例如，当栅电极130的厚度基本上彼此相同时，最上面的栅极焊盘137Pd可以在接触区域具有第五厚度T5，最下面的栅极焊盘131Pd可以在接触区域具有比第五厚度T5厚的第六厚度T6。第六厚度T6可以是等于或低于连接到栅极焊盘131Pd的栅电极131的厚度。

[0111] 根据示例实施例，栅极焊盘130Pd的厚度的减小程度还可以与在示例实施例中的厚度减小的趋势相反地远离基底101的上表面减小。例如，下栅极焊盘130Pd的厚度的减小程度可以比上栅极焊盘130Pd的厚度的减小程度大。栅极焊盘130Pd之间的厚度减小的差别的趋势可以决定于制造过程中的形成顺序，可以与其到基底101的距离成正比或成反比。

[0112] 参照图8，半导体器件100b可以包括栅电极130、层间绝缘层120、通道孔CH、从栅电极130水平地延伸的栅极焊盘130Pe和连接到栅极焊盘130Pe的接触塞180。

[0113] 栅极焊盘130Pe可以分别包括以特定厚度从栅电极130延伸并随后以减小的厚度延伸的区域。例如，下栅极焊盘130Pe可以分别具有下栅极焊盘130Pe延伸为比上栅极焊盘130Pe长的接触区域以连接到接触塞180，栅极焊盘130Pe的接触区域可以分别具有相对减小的厚度。

[0114] 栅极焊盘130Pe可以分成分别设置在较高位置和较低位置的第一组ST1和第二组ST2。第一组ST1可以包括下栅极焊盘131Pe、132Pe和133Pe，第二组ST2可以包括上栅极焊盘134Pe、135Pe、136Pe和137Pe。

[0115] 在第一组ST1和第二组ST2中，栅极焊盘130Pe的厚度的减小程度可以彼此不同。例如，在第二组ST2中的厚度的减小程度可以比第一组ST1中的厚度的减小程度大。例如，当栅电极130的厚度基本上彼此相同时，第二组ST2可以在各个接触区域具有第七厚度T7，而第一组ST1可以在各个接触区域具有比第七厚度T7大的第八厚度T8。根据示例实施例，当栅电极130的厚度彼此不同时，在第一组ST1和第二组ST2的每个中，仅栅极焊盘130Pe的厚度的减小程度可以彼此相同。

[0116] 可以根据示例实施例对诸如第一组ST1和第二组ST2的组的分类进行各种改变。例如，可以对组的数量和单个组中包括的栅极焊盘130Pe的数量进行各种改变。根据示例实施例，与本示例实施例中的厚度的减小趋势相反，在设置在较高位置的组中，厚度的减小程度

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可以相对小。在各个组中的栅极焊盘130Pd之间的厚度的减小程度的这种差别可以取决于制造过程中的形成顺序和形成方法等。

[0117] 参照图9，半导体器件100c可以包括栅电极130、层间绝缘层120、通道孔CH、从栅电极130水平地延伸的栅极焊盘130P、连接到栅极焊盘130P的接触塞180和栅极焊盘130P上的刻蚀停止层107。

[0118] 刻蚀停止层107可以设置在具有通过栅极焊盘130P形成的台阶形状的台阶部分上。刻蚀停止层107可以设置在栅极焊盘130P连接到接触塞180的区域上，接触塞180可以穿过刻蚀停止层107以连接到栅极焊盘130P。

[0119] 刻蚀停止层107可以在形成用于形成接触塞180的孔时用来停止刻蚀，使得可以稳定地形成具有不同深度的孔。刻蚀停止层107可以包括与焊盘绝缘层129和栅极焊盘130P的材料不同的材料，以具有与其不同的刻蚀选择性。例如，当焊盘绝缘层129包括氧化硅而栅极焊盘130P包括金属时，刻蚀停止层107可以包括氮化硅或碳化硅。

[0120] 根据示例实施例，刻蚀停止层107可以不与栅极焊盘130P直接接触，而可以以预设的高度与栅极焊盘130P分隔开从而设置在焊盘绝缘层129内。刻蚀停止层107可以包括诸如多晶硅的导电材料。

[0121] 图10A至图10K示意性地示出了根据示例实施例的制造半导体器件的方法的主要过程的图。图10A至图10K示出了制造图3和图4的半导体器件100的方法。

[0122] 参照图10A，可以在基底101上交替地堆叠例如层111至117的牺牲层110和例如层121至128的层间绝缘层120。可以通过后续工艺用栅电极130替代牺牲层110。

[0123] 首先可以形成层间绝缘层121，然后可以如图10A所示在基底101上交替地堆叠牺牲层110和层间绝缘层120。牺牲层110可以包括能够与层间绝缘层120被选择性刻蚀的材料。例如，牺牲层110可以由可以被刻蚀同时在刻蚀牺牲层110的过程中显著减小层间绝缘层120的刻蚀的材料形成。这样的刻蚀选择性或刻蚀选择比可以经过牺牲层110与层间绝缘层120的刻蚀速率的刻蚀速率比被量化地表示。例如，层间绝缘层120可以包括氧化硅和氮化硅中的至少一种，牺牲层110可以包括与层间绝缘层120的材料不同的材料，例如可以包括从硅、氧化硅、碳化硅和氮化硅中选择的材料。

[0124] 根据示例实施例，层间绝缘层120的厚度可以彼此不相同。例如，在层间绝缘层120中最下面的层间绝缘层121可以具有相对薄的厚度，最上面的层间绝缘层128可以具有相对厚的厚度。在示例实施例中，设置在图2的地选择晶体管GST与存储单元MC1至MCn之间的层间绝缘层122以及设置在图2的串选择晶体管SST与存储单元MC1至MCn之间的层间绝缘层126可以具有比设置在存储单元MC1至MCn之间的层间绝缘层123至125的厚度大的厚度。可以对层间绝缘层120和牺牲层110的厚度进行各种改变。还可以对构成层间绝缘层120和牺牲层110的层的数量进行各种改变。

[0125] 参照图10B，可以在彼此堆叠的层间绝缘层120和牺牲层110上形成硬掩模层HM和第一光掩模层PM1，并可以使用硬掩模层HM和第一光掩模层PM1去除牺牲层110和层间绝缘层120的部分。

[0126] 为了形成如图4所示在焊盘区域PAD中具有台阶部分的栅极焊盘130P，可以执行去除牺牲层110的部分的工艺。首先，可以在单元区域CELL中在层间绝缘层120和牺牲层110上形成硬掩模层HM，以保护单元区域CELL。硬掩模层HM可以包括与层间绝缘层120的材料不同

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的材料，并还可以由多层组成。

[0127] 然后，可以形成第一光掩模层PM1以去除最上面的第七牺牲层117的一部分。可以形成第一光掩模层PM1以与第七牺牲层117的期望的长度对应，例如，可以形成第一光掩模层PM1以与栅极焊盘137P(见图4)的期望长度对应。可以使用干法刻蚀或湿法刻蚀去除层间绝缘层120和牺牲层110的被第一光掩模层PM1暴露的部分。

[0128] 参照图10C，可以在去除第一光掩模层PM1之后形成第二光掩模层PM2，可以使用第二光掩模层PM2去除层间绝缘层120和牺牲层110的部分。

[0129] 首先，可以通过灰化和剥离工艺去除第一光掩模层PM1。还可以去除在剥离工艺过程中暴露的层间绝缘层127和128的部分。例如，当层间绝缘层120包括氧化硅并且使用氢氟酸(HF)执行剥离工艺时，可以将最上面的层间绝缘层128的厚度从第九厚度T9(见图10B)减小到比第九厚度T9低的第十厚度T10。

[0130] 然后，可以形成第二光掩模层PM2以去除第六牺牲层116的一部分。可以使用干法刻蚀或湿法刻蚀去除层间绝缘层120和牺牲层110的被第二光掩模层PM2暴露的部分。

[0131] 参照图10D，牺牲层110全部可以经历切除工艺以具有不同的长度。

[0132] 如上参照图10B和图10C所述，可以重复执行光掩模层PM1和PM2的形成、层间绝缘层120和牺牲层110的部分的去除以及光掩模层PM1和PM2的去除，使得可以通过切除工艺去除所有牺牲层110中的部分以具有台阶部分。

[0133] 在这样重复的过程中，还可以如上参照图10C所述在去除光掩模层PM1和PM2时部分地去除层间绝缘层120。层间绝缘层120可以在其暴露区域PC中分别具有减小的厚度。在剥离过程中更频繁地暴露的上层间绝缘层120可以具有比下层间绝缘层120的厚度更加减小的厚度。可以根据示例实施例对层间绝缘层120的厚度的减小进行各种改变。例如，可以在其暴露的区域完全地去除层间绝缘层120的部分以不剩余。可以暴露下牺牲层110。

[0134] 示例实施例示出了按从其上部到其下部的顺序去除牺牲层110的部分的方法。还可以使用按从下部到上部的顺序执行的牺牲层110的切除工艺。下层间绝缘层120在暴露区域PC可以分别具有比上层间绝缘层120的厚度更加减小的厚度。

[0135] 参照图10E，可以形成第一焊盘绝缘层129A和第二焊盘绝缘层129B。

[0136] 第二焊盘绝缘层129B可以包括氧化物基材料，并且例如可以是使用HDP(高密度等离子体)形成的层。在暴露区域PC中，当形成第二焊盘绝缘层129B时，可以通过提供的氧化物源部分地氧化设置在相对薄的层间绝缘层120下面的牺牲层110，因此形成氧化的层110'。在暴露区域PC中，可以减小设置在牺牲层110上的层间绝缘层120的厚度，可以不保护牺牲层110，使得可以从其上表面将牺牲层110的至少部分氧化预定深度。

[0137] 在图10E中，第一焊盘绝缘层129A被示出为分别包括通过氧化的牺牲层110形成的氧化的层110'和在暴露区域PC中保留在牺牲层110的上部上的层间绝缘层120的两层的组合。例如，这两层可以无法彼此辨别。

[0138] 例如，如在本示例实施例中所示，当保留在暴露区域PC中的层间绝缘层120的厚度相对薄以至于不能防止牺牲层110的氧化时，氧化的层110'的厚度可以彼此基本相同或相似，而不管层间绝缘层120的剩余的厚度如何。在如图7的示例实施例中，可以根据剩余的层间绝缘层120的厚度来改变通过氧化牺牲层110形成的氧化物层110'的厚度。例如，当在堆叠的层间绝缘层120的下部的层间绝缘层120的剩余的厚度相对厚时，在堆叠的层间绝缘层

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120的上部，氧化物层110'可以相对厚。在如上参照图6A至6C描述的示例实施例中，栅极焊盘层133Pa、133Pb和133Pc的形状还可以取决于在此阶段的氧化的层110'的形状。

[0139] 根据示例实施例，可以通过在彼此上直接堆叠层间绝缘层120和栅电极130/栅极焊盘130P(见图4)来制造半导体器件，而不使用牺牲层110和层间绝缘层120的堆叠结构。可以对栅极焊盘130P执行切除工艺来代替对牺牲层110使用切除工艺。

[0140] 在此阶段，当形成第二焊盘绝缘层129B时，可以在暴露区域PC中分别部分地氧化栅极焊盘130P以形成氧化物层110'，可以形成如图4所示的结构。

[0141] 参照图10F，可以通过形成第三焊盘绝缘层129C来形成覆盖焊盘区域PAD的焊盘绝缘层129。

[0142] 首先，在形成第三焊盘绝缘层129C的一部分之后，可以执行平坦化工艺，以允许硬掩模层HM被暴露。第三焊盘绝缘层129C可以是例如正硅酸乙酯(TEOS)层。

[0143] 然后，在选择性地去除硬掩模层HM之后，可以在其上另外地沉积绝缘材料以形成第三焊盘绝缘层129C。第三焊盘绝缘层129C的形成方法和工艺顺序可以是各种的。由此，可以形成包括第一至第三焊盘绝缘层129A、129B和129C的焊盘绝缘层129。构成焊盘绝缘层129的第一至第三焊盘绝缘层129A、129B和129C可以包括相同的材料，它们之间的边界可以无法辨别。第一至第三焊盘绝缘层129A、129B和129C将在下面示出为单层。

[0144] 参照图10G，可以形成通道孔CH和哑通道孔CHD(见图3)。

[0145] 首先，可以通过各向异性地刻蚀牺牲层110和层间绝缘层120来形成通道孔CH。可以刻蚀包括不同类型的层的堆叠结构，通道孔CH的侧壁可以不与基底101的上表面垂直。例如，根据示例实施例，可以朝向基底101的上表面减小通道孔CH的宽度。根据示例实施例，基底101的一部分可以被通道孔CH凹进。

[0146] 然后，可以在通道孔CH内形成栅极介电层150、通道区域140、第一绝缘层162和通道焊盘160。焊盘区域PAD的哑通道孔CHD也可以具有与通道孔CH的结构相同的结构。

[0147] 可以通过原子层沉积(ALD)或化学气相沉积(CVD)将栅极介电层150形成为具有均匀的厚度。在本工艺中，可以总体地或部分地形成栅极介电层150，可以在本工艺中形成其沿着通道孔CH的长度延伸以与基底101的上表面垂直的部分。可以在通道孔CH内在栅极介电层150上形成通道区域140。

[0148] 第一绝缘层162可以填充第一通道孔CH，并可以包括绝缘材料。根据一些实施例，导电材料而不是第一绝缘层162也可填充通道区域140之间的缝隙。通道焊盘160可以包括导电材料。通道焊盘160可以包括例如多晶硅。

[0149] 参照图10H，可以形成沟槽TH(见图3)以允许堆叠有牺牲层110和层间绝缘层120的堆叠结构沿未在图中示出的方向彼此分离，可以去除通过沟槽TH暴露的牺牲层110。

[0150] 例如，可以使用湿法刻蚀相对于层间绝缘层120选择性地去除牺牲层110以形成隧道部分TP。在去除牺牲层110之前，还可以在通道焊盘160上形成第二绝缘层166以保护通道孔CH。

[0151] 在此工艺中，可以不去除通过氧化形成第一焊盘绝缘层129A(见图10F)的一部分的牺牲层110的部分，隧道部分TP可以在其端部具有减小的宽度。

[0152] 参照图10I，可以用导电材料填充从中去除了牺牲层110的区域来形成栅电极130和栅极焊盘130P。

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[0153] 栅电极130和栅极焊盘130P可以包括金属、多晶硅或金属硅化物材料。金属硅化物材料可以是从例如钴(Co)、镍(Ni)、铪(Hf)、铂(Pt)、钨(W)和钛(Ti)中选择的金属的硅化物材料，或者是其组合。例如，当栅电极130和栅极焊盘130P包括金属硅化物材料时，硅(Si)可以填充隧道部分TP，随后可以形成另外的金属层来经历硅化工艺，从而形成栅电极130和栅极焊盘130P。

[0154] 在形成栅电极130和栅极焊盘130P之后，可以通过另外的工艺去除形成在沟槽TH(见图3)中形成的栅电极130的材料。然后，可以在沟槽TH中形成共源线CSL(见图2)。

[0155] 参照图10J，可以通过去除焊盘绝缘层129的一部分来形成接触孔H。

[0156] 可以在形成具有与将要形成接触塞180(见图4)的区域对应的开口的单独掩模图案之后使用所述单独掩模图案来形成接触孔H。可以形成接触孔H以使栅极焊盘130P被暴露。在示例实施例中，接触孔H使栅极焊盘130P凹进预定深度。

[0157] 参照图10K，可以形成接触塞180。

[0158] 首先，可以用导电材料填充接触孔H以形成接触塞180。

[0159] 然后，参照图4，可以在接触塞180上一起形成第二布线190。在单元区域CELL中，可以在通道焊盘160上形成通道塞175，然后，可以在其上形成第一布线170。在示例实施例中，第一布线170和第二布线190的设置可以如图所示。在示例实施例中，可以以不同的高度设置第一布线170和第二布线190。

[0160] 图11A至图11D示意性地示出了根据示例实施例的制造半导体器件的方法的主要工艺的图。在图11A至图11D中，示出了制造图8的半导体器件100b的方法。在下文中，将省略与图10A至图10K的描述重复的描述。

[0161] 如上参照图10A所述，可以首先形成堆叠有牺牲层110和层间绝缘层120的堆叠结构。

[0162] 然后，参照图11A，可以在彼此堆叠的层间绝缘层120和牺牲层110上形成硬掩模层HM和第一光掩模层PM1'，可以使用硬掩模层HM和第一光掩模层PM1'去除层间绝缘层120和牺牲层110的部分。

[0163] 首先，可以在其与图8的第二组ST2的栅极焊盘130Pe对应的位置执行去除牺牲层110的部分的工艺，可以将第一光掩模层PM1'形成为与第二组ST2的栅极焊盘130Pe中最下面的栅极焊盘134Pe(见图8)的长度对应。可以使用干法刻蚀或湿法刻蚀去除通过第一光掩模层PM1'暴露的牺牲层110的区域。

[0164] 参照图11B，可以通过修整第一光掩模层PM1'形成修整掩模层PM1a。

[0165] 修整工艺可以是使用干法刻蚀或湿法刻蚀减小第一光掩模层PM1'的尺寸的工艺，可以形成覆盖减小的区域使得其一端与栅极焊盘135Pe(见图8)的长度对应的第一修整掩模层PM1a。也可以通过修整工艺降低第一光掩模层PM1'的高度。

[0166] 参照图11C，可以通过切除工艺去除所有第四至第七牺牲层114至117中的将被图8的第二组ST2的栅极焊盘130Pe替代的部分。

[0167] 可以通过重复地执行如参照图11B描述的修整工艺使第四至第七牺牲层114至117经历切除工艺以具有不同的长度，然后，可以去除修整掩模层PM1a。

[0168] 在去除修整掩模层PM1a时，也可以部分地去除暴露的层间绝缘层120，在第四至第七牺牲层114至117上的暴露的层间绝缘层120可以具有以暴露的层间绝缘层120可以具有

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基本上均匀的厚度的程度减少的厚度。

[0169] 参照图11D,可以形成第二光掩模层PM2'以通过切除工艺去除设置在与图8的第一组ST1的栅极焊盘130Pe对应的位置的牺牲层110的部分。

[0170] 可以将第二光掩模层PM2'形成为与第一组ST1的栅极焊盘130Pe中的最下面的栅极焊盘131Pe(见图8)的长度对应。可以使用干法刻蚀或湿法刻蚀去除被第二光掩模层PM2'暴露的层间绝缘层120和牺牲层110。

[0171] 然后,可以通过重复地执行如上参照图11B和图11C所述的修整工艺和刻蚀工艺经过切除工艺来去除所有牺牲层110的部分。这样,可以使用修整工艺减少光掩模层的形成工艺和去除工艺的次数。在去除光掩模层时,也可以去除暴露的层间绝缘层120的部分,在牺牲层110上的经历使用单个光掩模层的切除工艺的层间绝缘层120可以具有减小了相同厚度的厚度。如上参照图10E所述,在这样的层间绝缘层120下面的牺牲层110的氧化厚度,在单个组ST1和ST2中可以相同。最后,如图8所示,基于组ST1和ST2的单位形成的栅极焊盘130Pe可以在接触区域具有不同的厚度。

[0172] 然后,可以通过执行上面参照图10E至图10K描述的工艺完成图8的半导体器件100b的制造。

[0173] 图12示出了根据示例实施例的半导体器件的示意性透视图。

[0174] 参照图12,半导体器件200可以包括单元区域CELL、焊盘区域PAD和外围电路区域PERI。

[0175] 外围电路区域PERI可以与设置有图1的存储单元阵列20的驱动电路30的区域对应。外围电路区域PERI可以设置在单元区域CELL和焊盘区域PAD下方。根据示例实施例,外围电路区域PERI也可以设置在单元区域CELL和焊盘区域PAD上面或者可以设置在单元区域CELL和焊盘区域PAD的至少一侧上。

[0176] 单元区域CELL和焊盘区域PAD可以包括栅电极130、层间绝缘层120、通道孔CH、从栅电极130水平地延伸的栅极焊盘130P和连接到栅极焊盘130P的接触塞180。

[0177] 在示例实施例中,单元区域CELL和焊盘区域PAD示出为具有与图4的示例实施例的结构相同的结构。单元区域CELL和焊盘区域PAD可以包括根据如上参照图6A至图9描述的各种示例实施例的半导体器件。

[0178] 外围电路区域PERI可以包括基体基底201、设置在基体基底201上的电路器件230、第一接触塞250和第二接触塞275以及第一布线260和第二布线270。

[0179] 基体基底201可以具有沿X方向和Y方向延伸的上表面。在基体基底201中,可以形成器件隔离层210,从而可以由此限定有源区域。包括杂质的掺杂区域205可以设置在有源区域的一部分中。基体基底201可以包括半导体材料,例如,IV族半导体材料、III-V族化合物半导体材料或II-VI族氧化物半导体材料。

[0180] 电路器件230可以包括平面晶体管。各个电路器件230可以包括电路栅极绝缘层232、间隔层234和电路栅电极235。在电路栅电极235的两侧,掺杂区域205可以设置在基体基底201内以用作电路器件230的源区或漏区。

[0181] 外围区域绝缘层240可以设置在处于基体基底201上的电路器件230上。

[0182] 第一接触塞250可以穿过外围区域绝缘层240以连接到掺杂区域205或电路栅电极235。第二接触塞275可以设置在第一布线260与第二布线270之间。可以经过第一接触塞250

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和第二接触塞275以及第一布线260和第二布线270向电路器件230施加电信号。

[0183] 半导体器件200还可以包括将焊盘区域PAD与外围电路区域PERI彼此连接的连接布线结构280和290。

[0184] 连接布线结构280和290可以设置为将第一布线260和第二布线270中的至少一个连接到例如外围电路区域PERI的电路器件230、连接到栅电极130的第一布线170与第二布线190和单元区域CELL的通道区域140，以延伸至焊盘区域PAD。

[0185] 可以首先形成外围电路区域PERI，然后，可以在外围电路区域PERI上形成单元区域CELL和焊盘区域PAD的基底101以形成单元区域CELL和焊盘区域PAD。例如，基底101可以比基体基底201小。基底101可以包括多晶硅或者可以在以非晶硅形成之后被单晶化。

[0186] 图13示出了包括根据示例实施例的半导体器件的存储装置的框图。

[0187] 参照图13，根据示例实施例的存储装置1000可以包括与主机HOST通信的控制器1010以及在其中存储数据的存储器1020-1、1020-2和1020-3。各个存储器1020-1、1020-2和1020-3可以包括根据如上参照图3至图9描述的各种示例实施例的半导体器件。

[0188] 与控制器1010通信的主机HOST可以是安装有存储装置1000的各种电子设备，例如可以是智能手机、数码相机、台式电脑、笔记本电脑、便携式媒体播放器等。控制器1010可以接收通过主机HOST传输的数据写入请求或数据读取请求以使数据能被写入存储器1020-1、1020-2和1020-3或者可以产生允许从存储器1020-1、1020-2和1020-3读取数据的命令CMD。

[0189] 如图13所示，一个或多个存储器1020-1、1020-2和1020-3可以在存储装置1000内并联连接到控制器1010。具有如在固态驱动器(SSD)中的大容量的存储装置1000可以通过将多个存储器1020-1、1020-2和1020-3并联连接到控制器1010来实施。

[0190] 图14示出了包括根据示例实施例的半导体器件的电子设备的框图。

[0191] 参照图14，根据示例实施例的电子设备2000可以包括通信单元2010、输入单元2020、输出单元2030、存储器2040和处理器2050。

[0192] 通信单元2010可以包括有线和无线通信模块，并可以包括无线因特网模块、近场通信模块、全球定位系统(GPS)模块、移动通信模块等。通信单元2010中包括的有线和无线通信模块可以经由各种通信协议连接到外部通信网络，以发送或接收数据。

[0193] 输入单元2020可以是设置为用户控制电子设备2000的操作的模块，并可以包括机械开关、触摸屏、声音识别模块等。输入单元2020也可以包括以轨迹球或激光指示器等操作的鼠标或手指鼠标装置，并且还可以包括用户可以通过其输入数据的各种传感器模块。

[0194] 输出单元2030可以以声音或视觉形式输出电子设备2000处理的信息，存储器2040可以存储处理器2050处理或控制用的程序、数据等。处理器2050可以根据要求的操作向存储器2040发送命令，以将数据写入存储器2040或者从存储器2040读取数据。

[0195] 存储器2040可以嵌入在电子设备2000中或可以经过单独接口与处理器2050通信。在经过单独接口与处理器2050通信的情况下，处理器2050可以经过诸如SD、SDHC、SDXC、MICRO SD、USB等的各种接口标准向存储器2040写入数据或从存储器2040读取数据。

[0196] 处理器2050可以控制电子设备2000中包括的各个部件的操作。处理器2050可以执行与语音通信、视频通信、数据通信等相关的控制与处理，或者还可以执行用于多媒体回放与管理的控制与处理。处理器2050可以处理用户通过输入单元2020传输的输入并可以经过输出单元2030输出其结果。处理器2050可以向存储器2040写入所需数据以控制电子装置

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2000的操作，或者可以从存储器2040读取数据。处理器2050和存储器2040中的至少一个可以包括根据如上参照图3至图9描述的各种示例实施例的半导体器件。

[0197] 图15示出了包括根据示例实施例的半导体器件的系统的示意图。

[0198] 参照图15，系统3000可以包括控制器3100、输入/输出装置3200、存储器3300和接口3400。系统3000可以是移动系统或者发送或接收信息的系统。移动系统可以是个人数字助理(PDA)、便携式电脑、网络平板、无线电话、移动电话、数字音乐播放器或存储卡。

[0199] 控制器3100可以执行程序并可以用于控制系统3000。控制器3100可以设置为例如微处理器、数字信号处理器、微控制器或与其相似的装置。

[0200] 输入/输出装置3200可以用于输入或输出系统3000的数据。系统3000可以连接到例如个人电脑或网络的外部设备，以在其间使用输入/输出装置3200交换数据。输入/输出装置3200可以设置为例如小键盘、键盘或显示器。

[0201] 存储器3300可以在其中存储用于控制器3100的操作的代码和/或数据，和/或可以在其中存储控制器3100处理的数据。存储器3300可以包括根据在示例实施例中的一个示例实施例的半导体器件。

[0202] 接口3400可以用作系统3000与外部不同的装置之间的数据传输路径。控制器3100、输入/输出装置3200、存储器3300和接口3400可以经总线3500彼此通信。

[0203] 控制器3100和存储器3300中的至少一个可以包括根据如上参照图3至图9描述的示例实施例的半导体器件。

[0204] 通过总结与回顾的方法，在垂直非易失性存储装置中，栅电极的部分可以被去除，使得栅电极在焊盘区域具有不同的长度并可以连接到上布线结构。

[0205] 在实施例中，栅电极延伸到焊盘区域的区域称作栅极焊盘，栅极焊盘可以具有厚度可以比栅电极的厚度低的区域。

[0206] 例如，栅极焊盘可以在其连接到接触塞的端部具有减小的厚度从而相对薄。可以通过当将要被栅电极替换的牺牲层经历切除工艺时，去除光掩模层的工艺来形成这样的结构。在焊盘区域中，可以部分地去除在牺牲层上的层间绝缘层以在厚度上减小，或者完全地去除层间绝缘层。牺牲层可以在后续工艺中从其上表面氧化至预定深度，以在替换工艺中当用栅电极替换牺牲层时不被去除。在对应的区域，栅电极可以具有减小的厚度。

[0207] 作为提高半导体器件集成程度的方法，半导体器件可以具有竖直晶体管结构而不是平面晶体管结构。实施例可以提供具有提高的集成度的半导体器件。例如，如上所阐述，根据示例实施例，因为各个栅极焊盘分别包括其厚度减小的区域，所以可以提供具有提高的集成度的半导体器件。

[0208] 在这里已经公开了示例实施例，虽然使用了具体的术语，但是仅以通常的和描述性的意思来使用和解释所述术语，而不是为了限制的目的。在一些情况下，正如在从本申请提交时起对本领域的技术人员清楚的是，除非另外具体地指出，否则结合具体的实施例描述的特征、特性和/或元件可以单独使用，或者可以与结合其他的实施例描述的特征、特性和/或元件组合使用。因此，本领域的技术人员将理解的是，在不脱离本发明的如在权利要求中所阐述的精神和范围的情况下，可以做出各种形式和细节上的改变。

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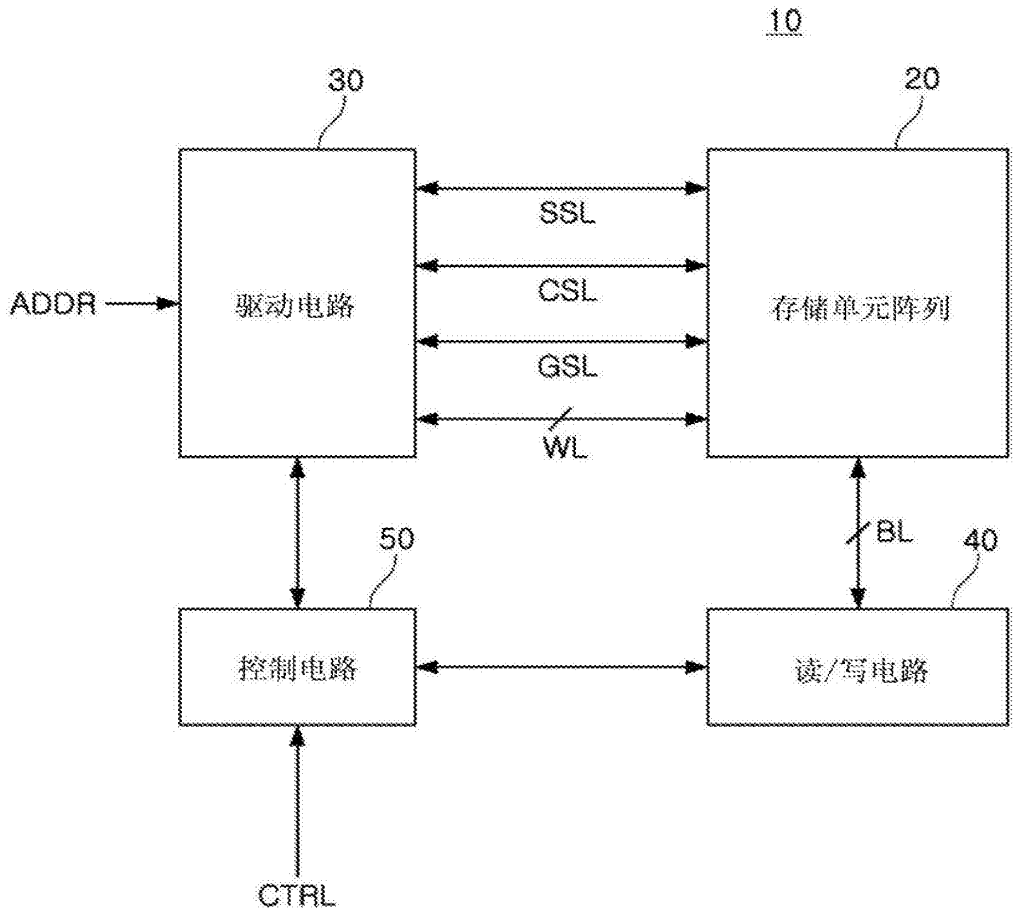


图1

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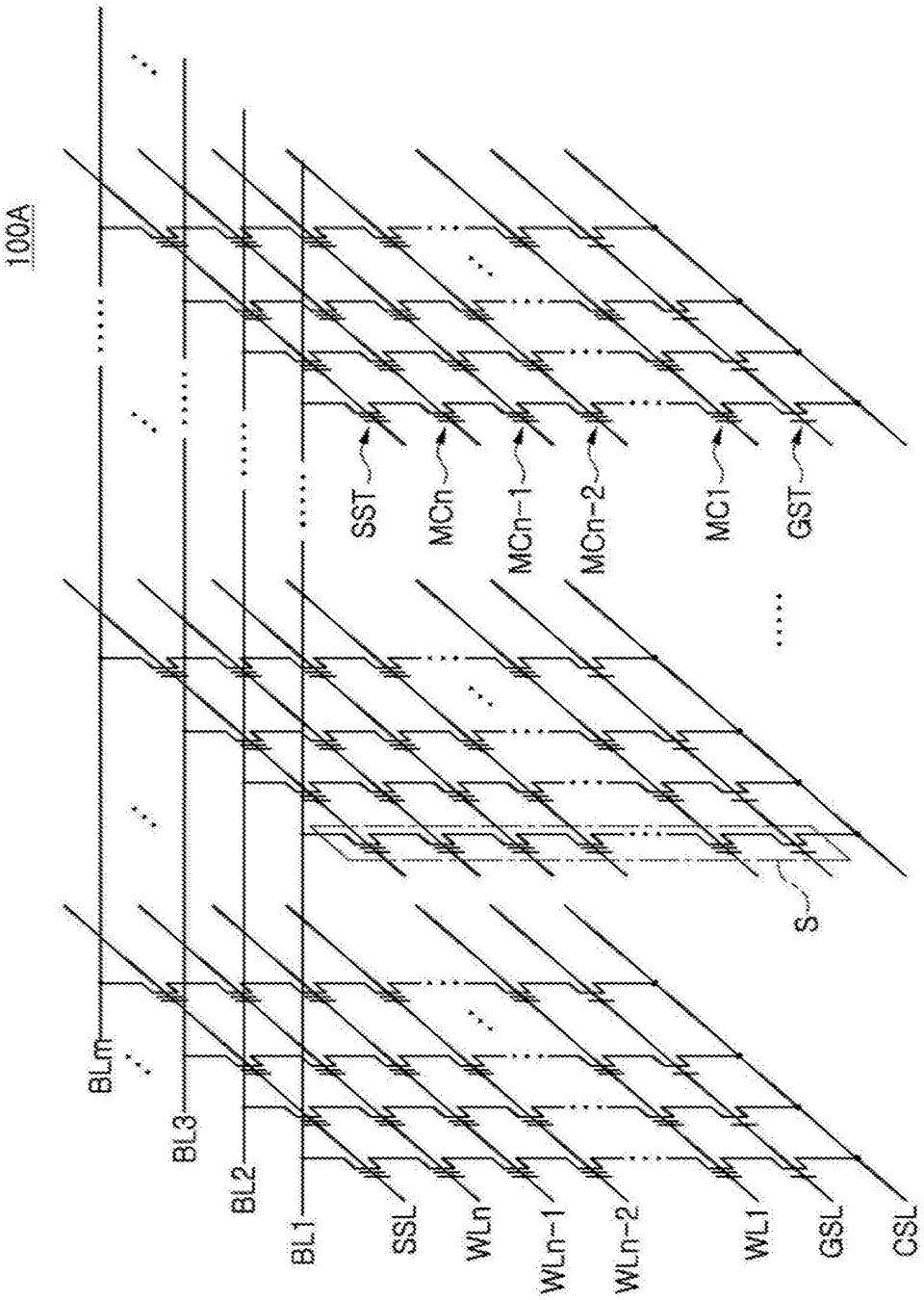


图2

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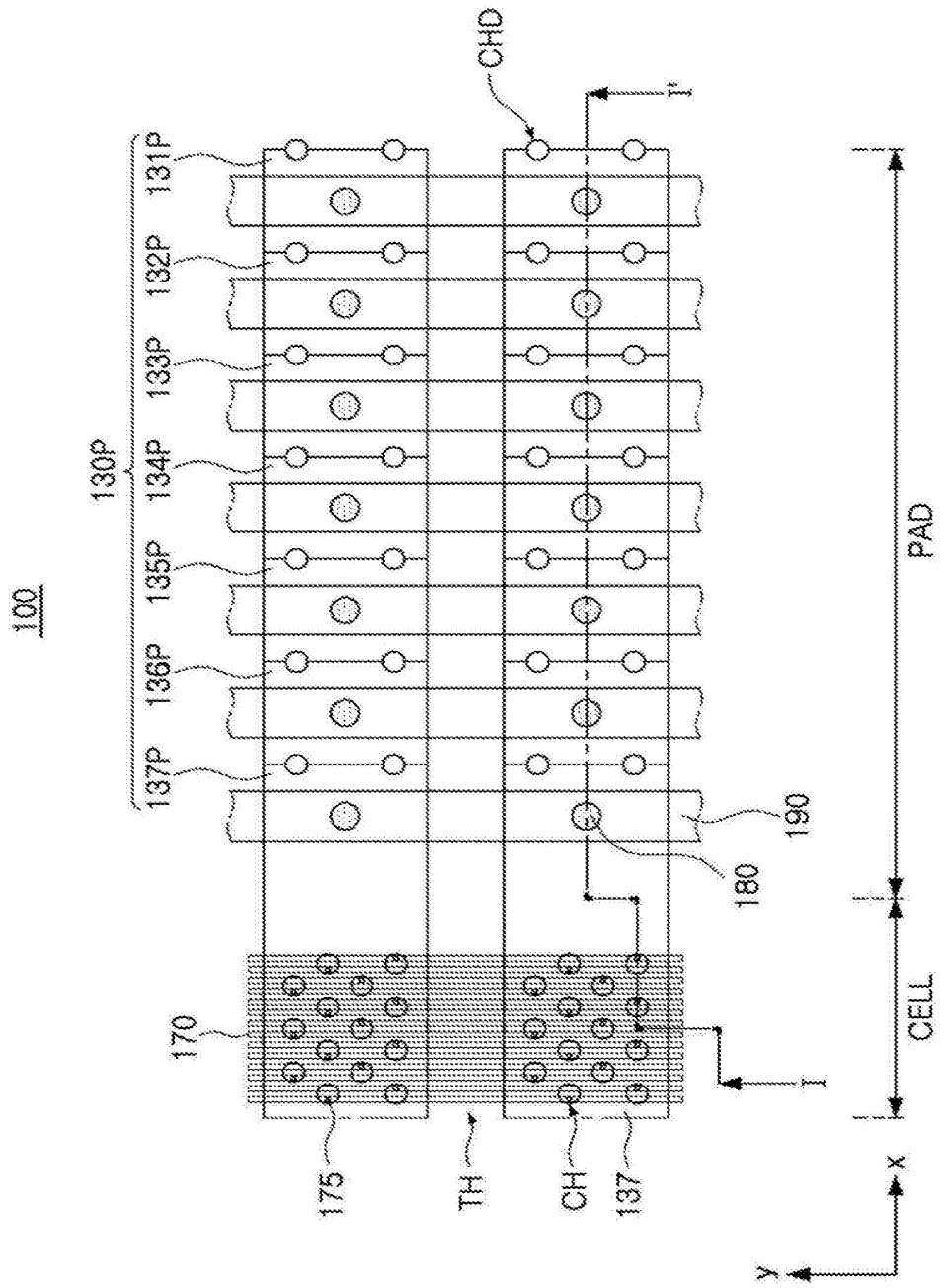


图3

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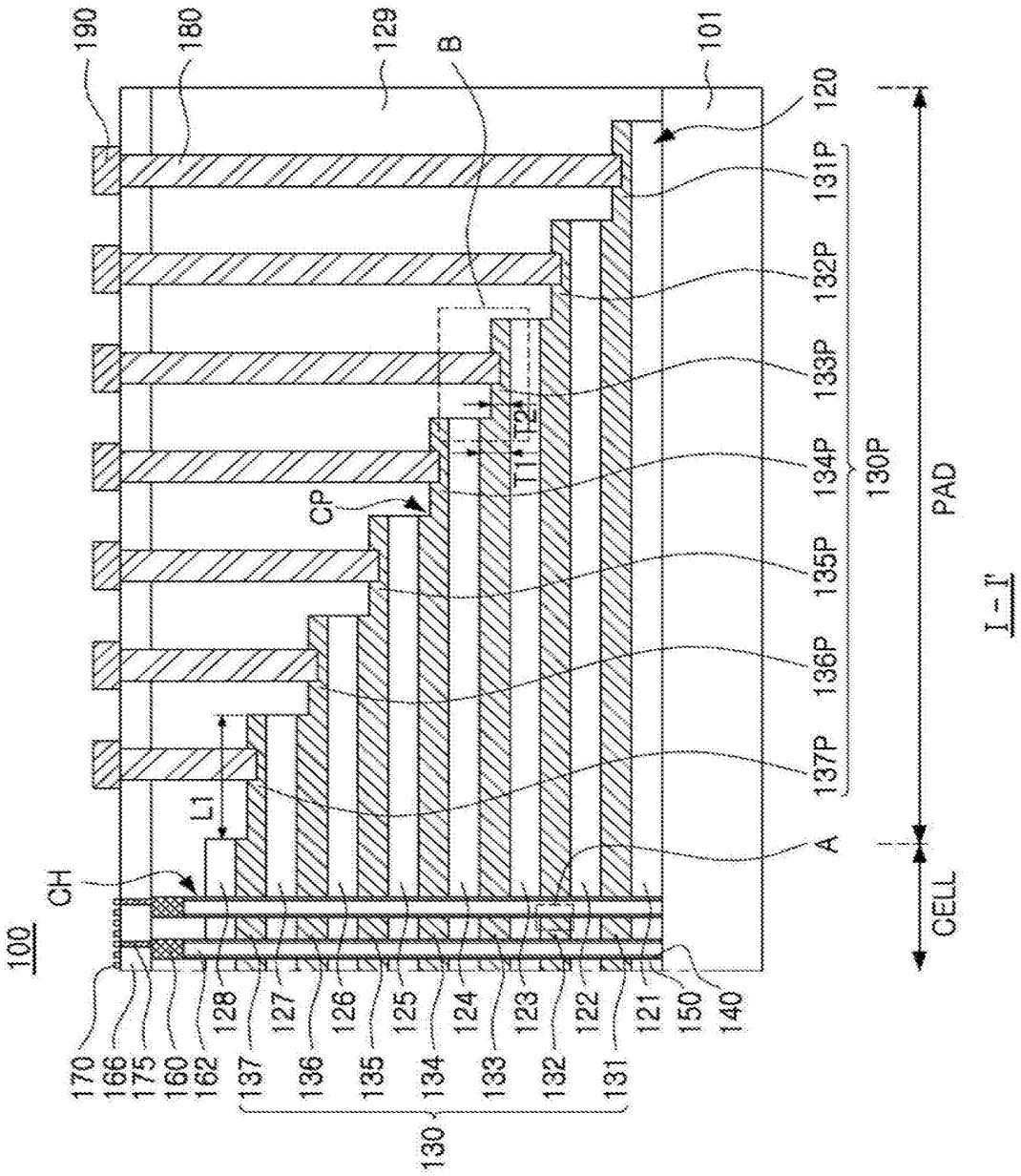


图4

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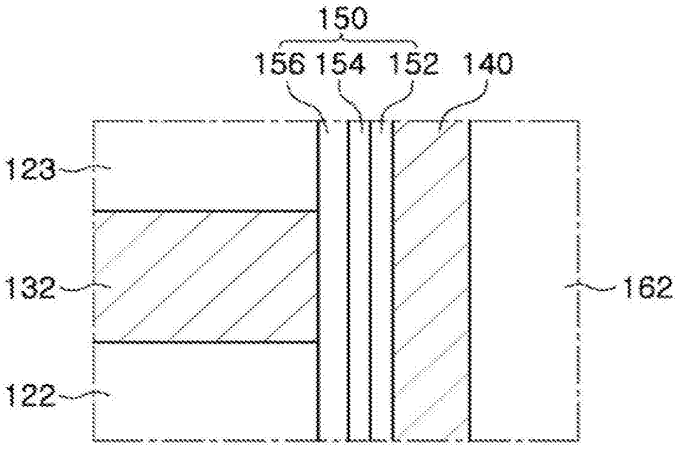


图5A

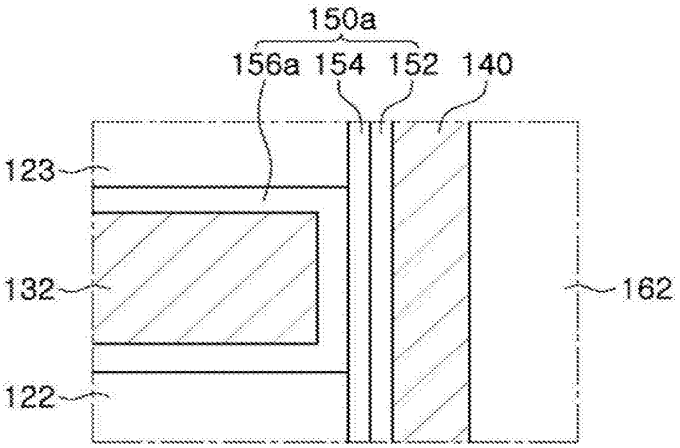


图5B

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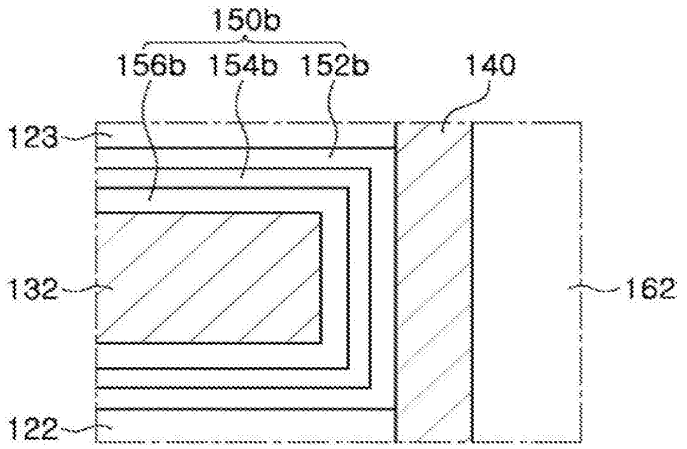


图5C

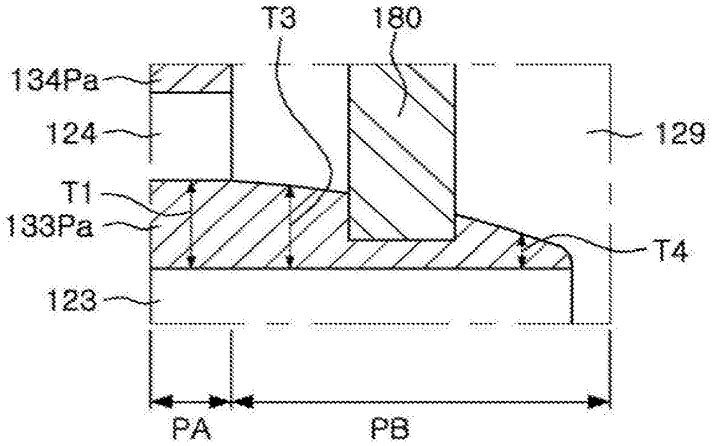


图6A

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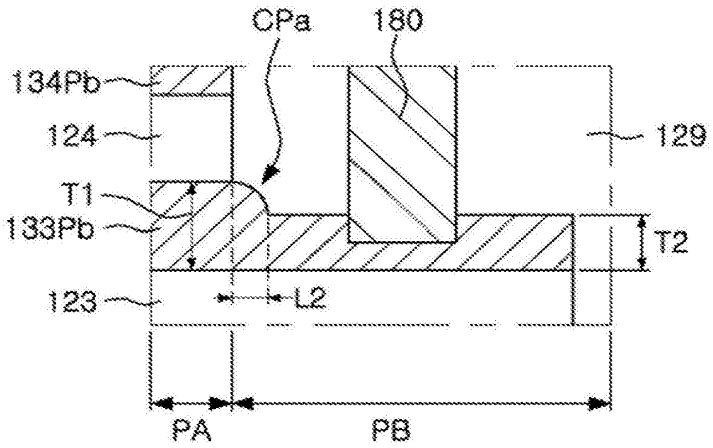


图6B

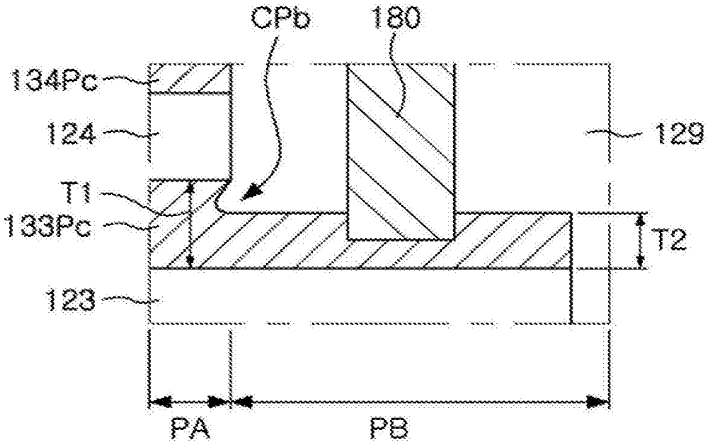


图6C

Micron Ex. 1019, p. 120
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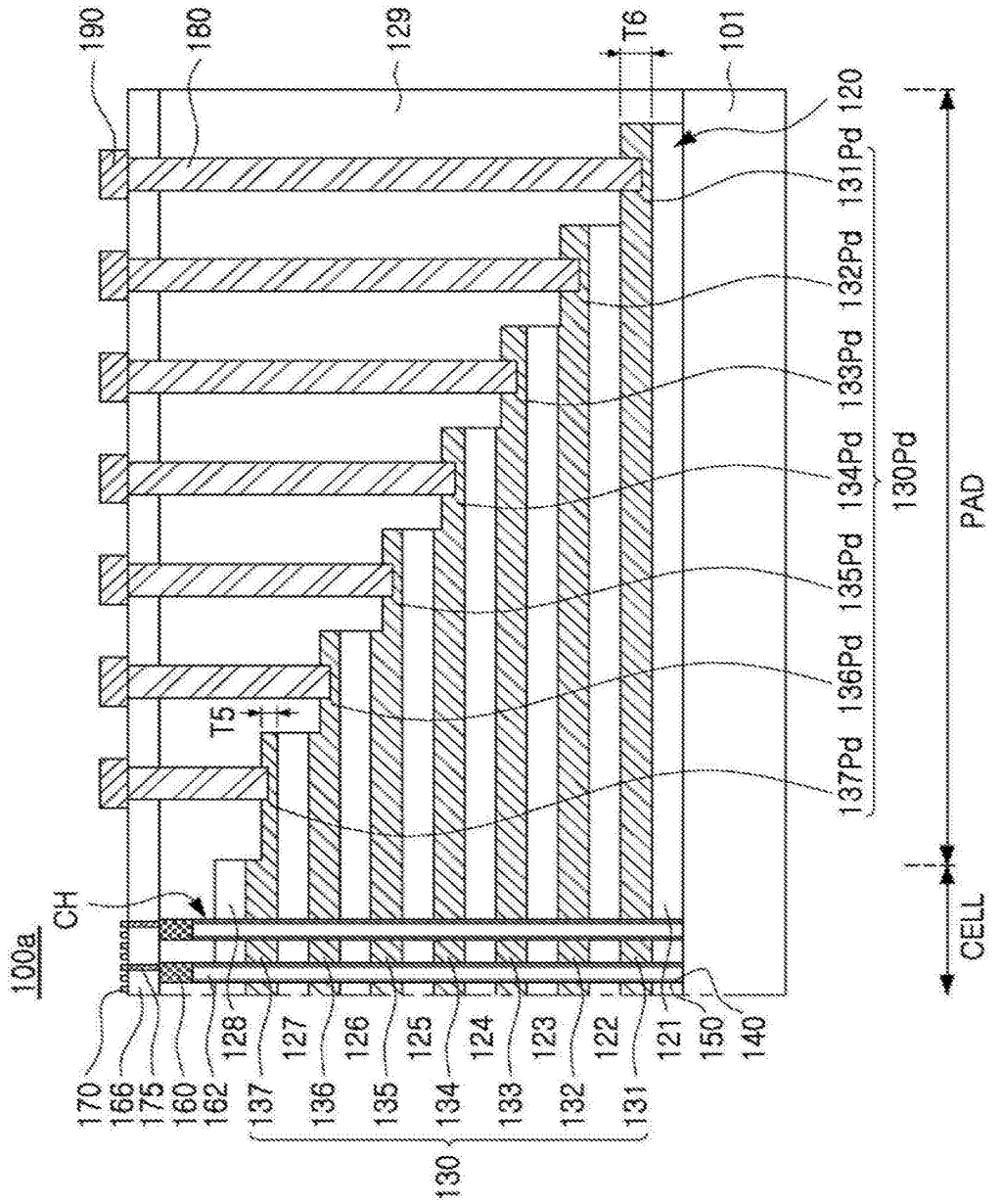


图7

Micron Ex. 1019, p. 121
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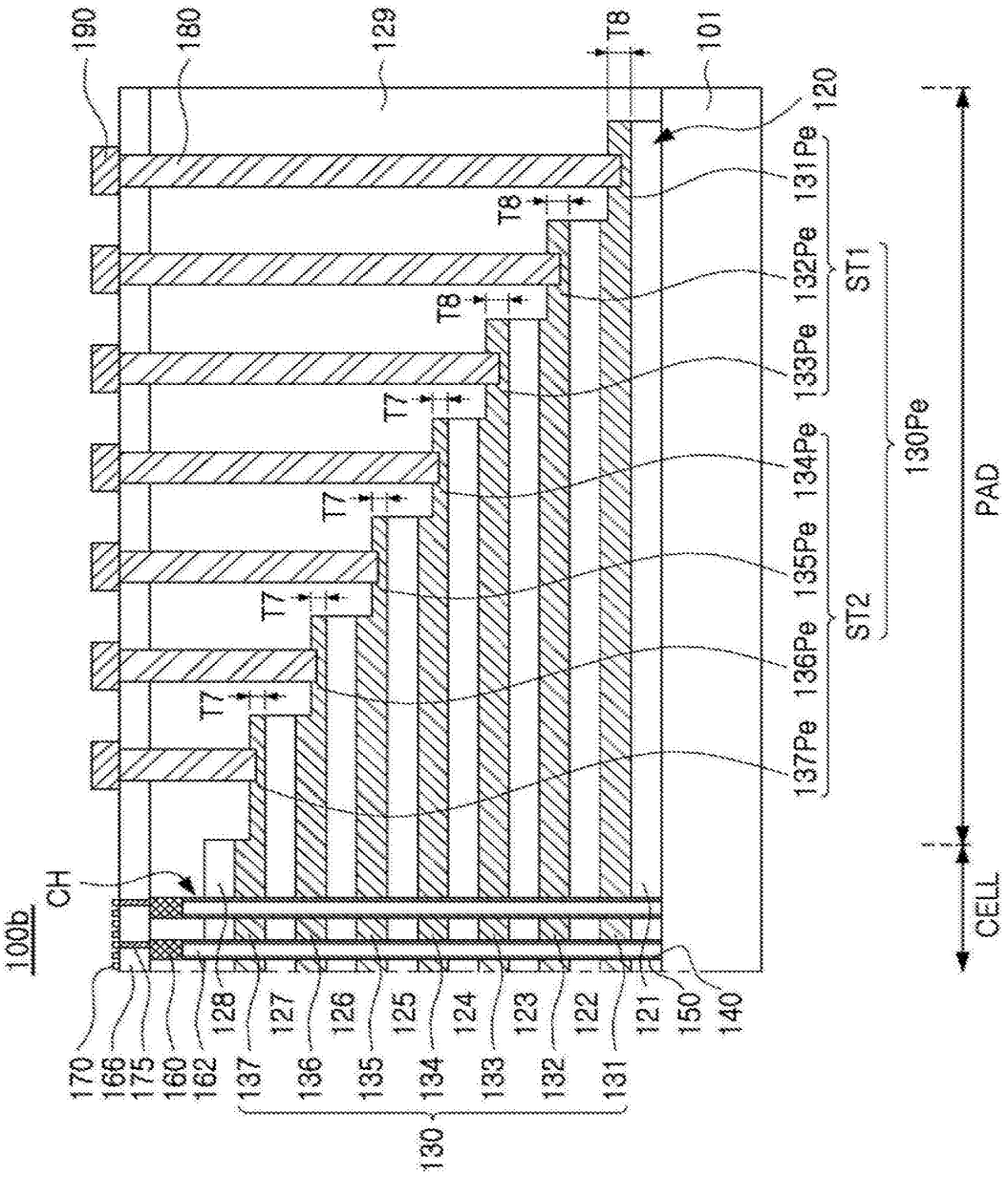


图8

Micron Ex. 1019, p. 122
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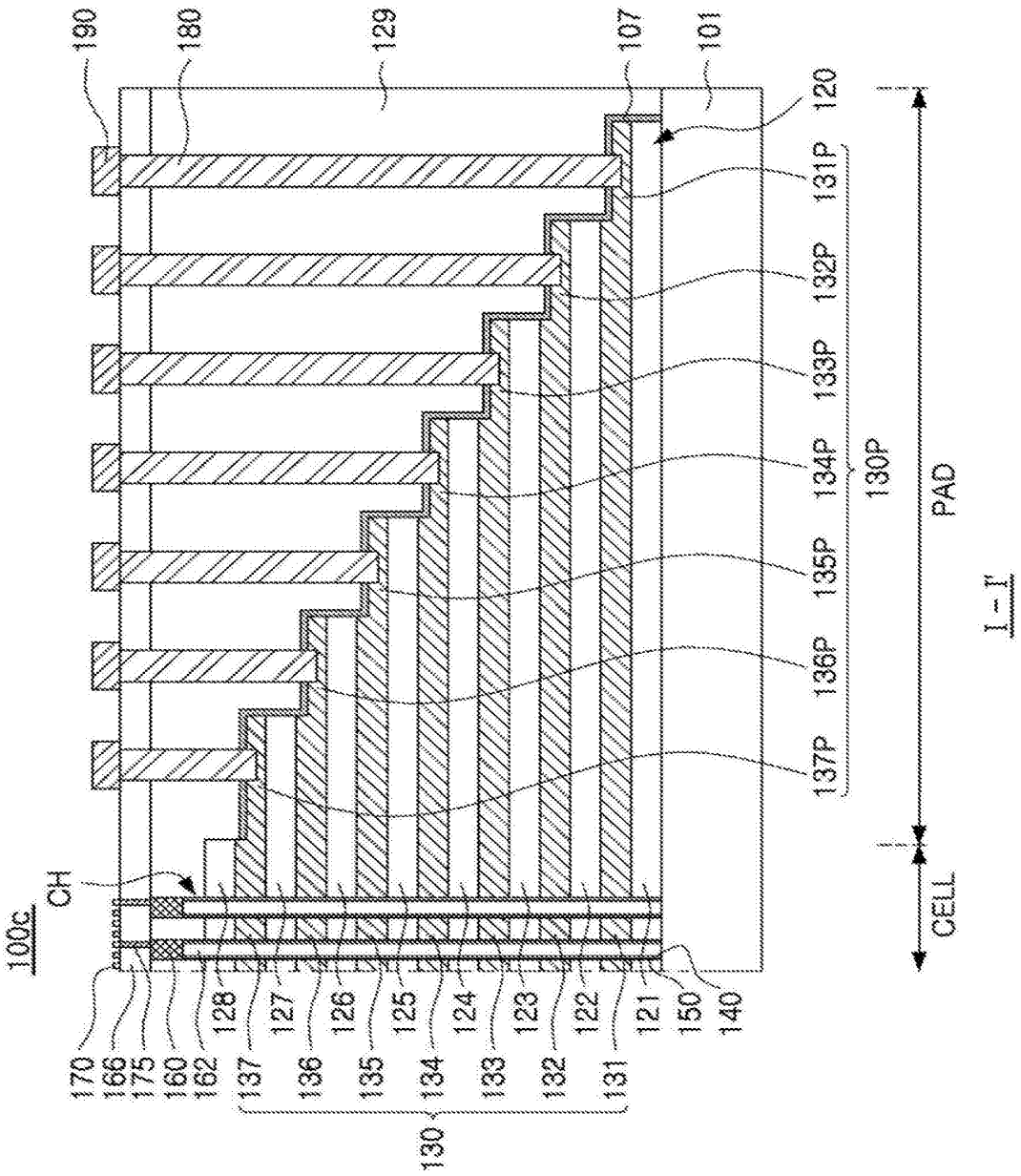


图9

Micron Ex. 1019, p. 123
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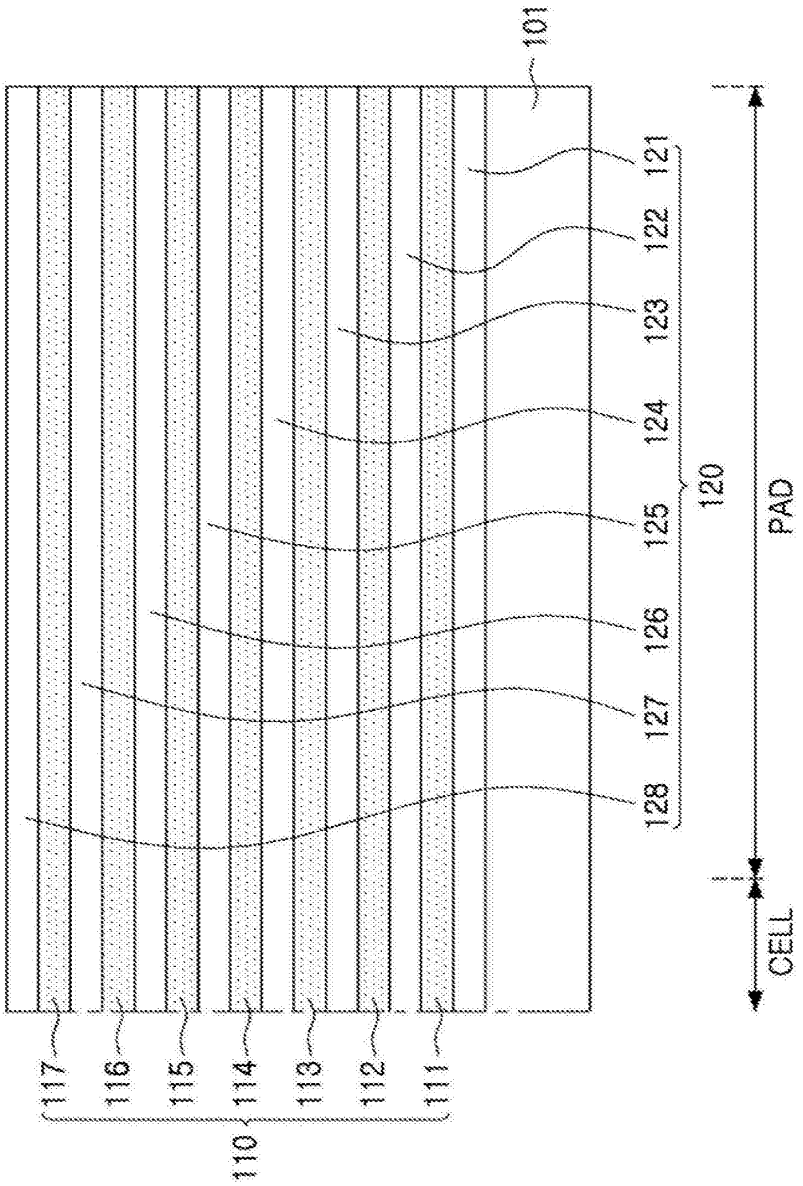


图10A

Micron Ex. 1019, p. 124
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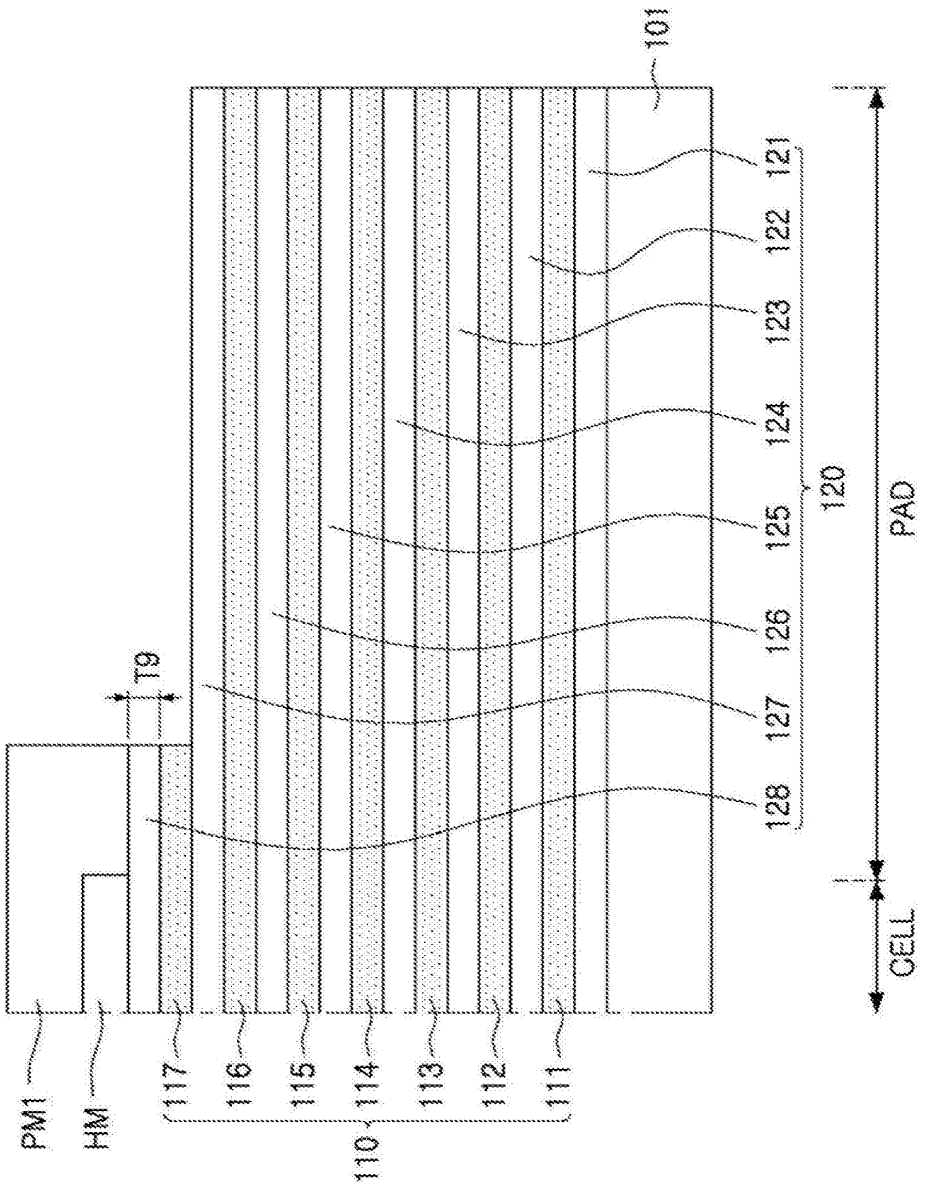


图10B

Micron Ex. 1019, p. 125
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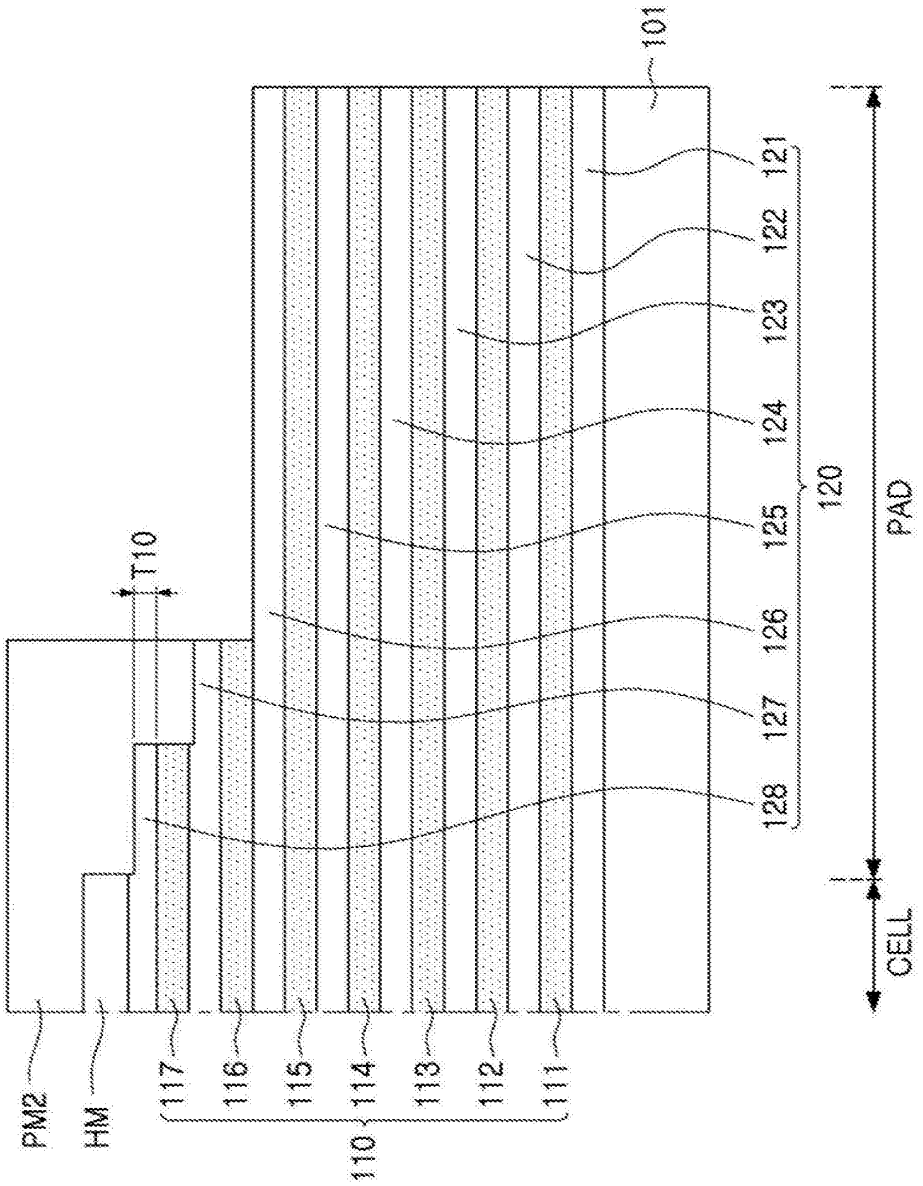


图10C

Micron Ex. 1019, p. 126
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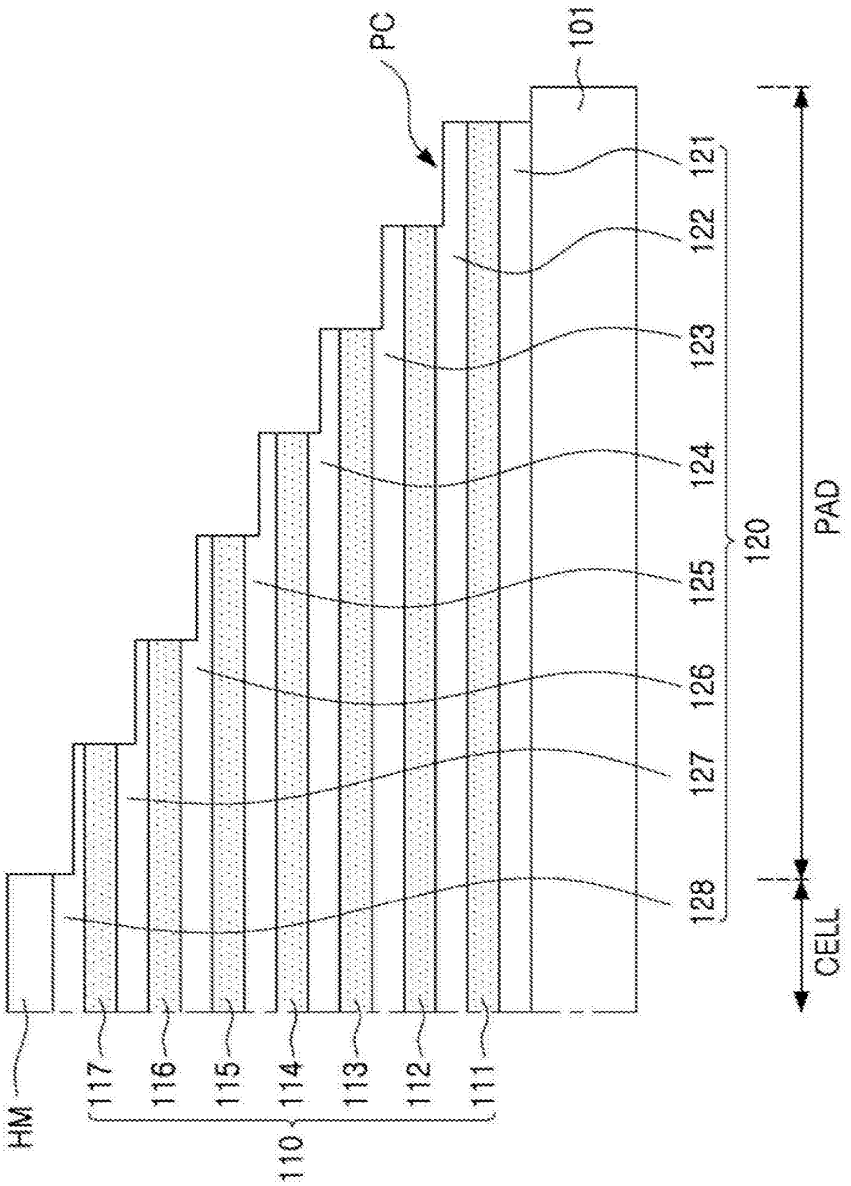


图10D

Micron Ex. 1019, p. 127
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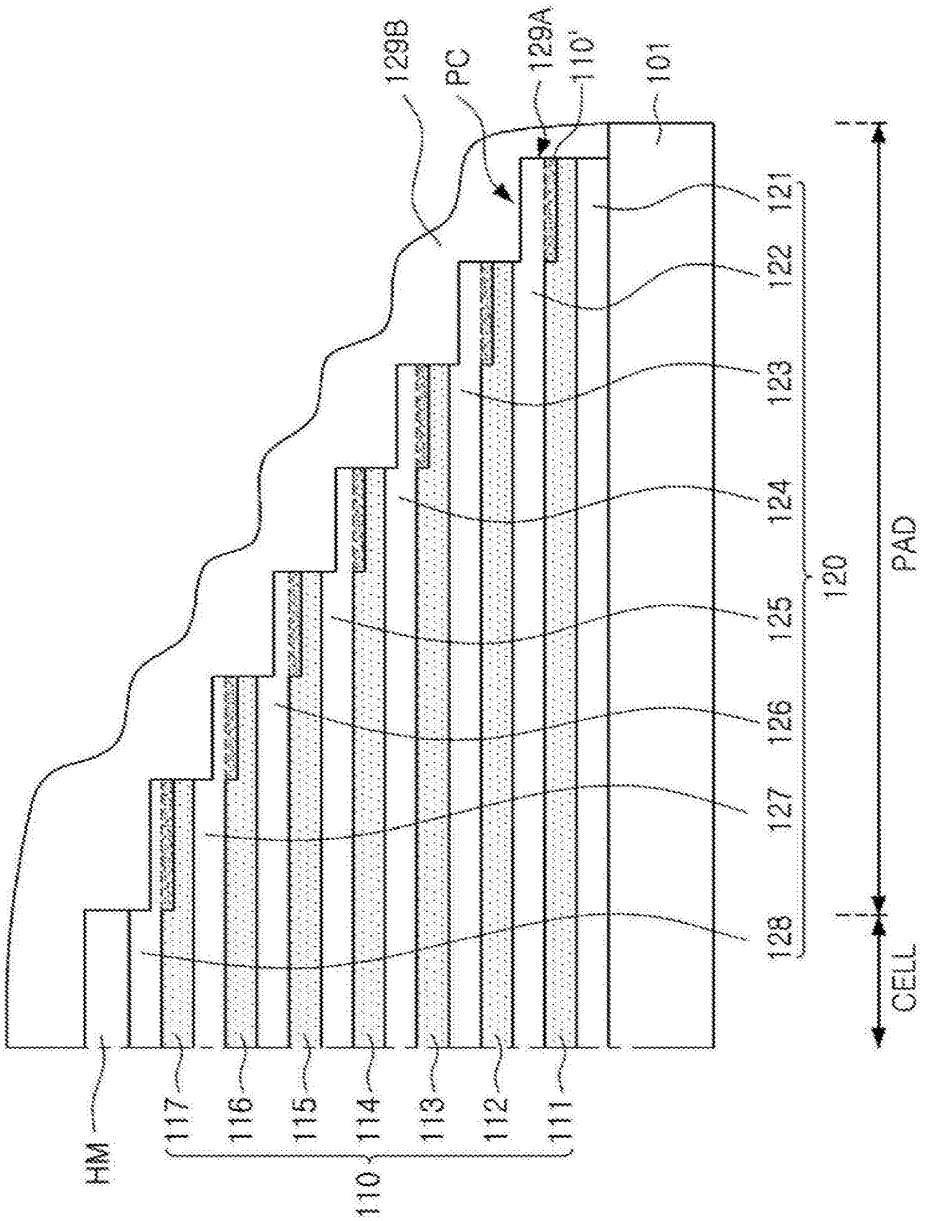


图10E

Micron Ex. 1019, p. 128
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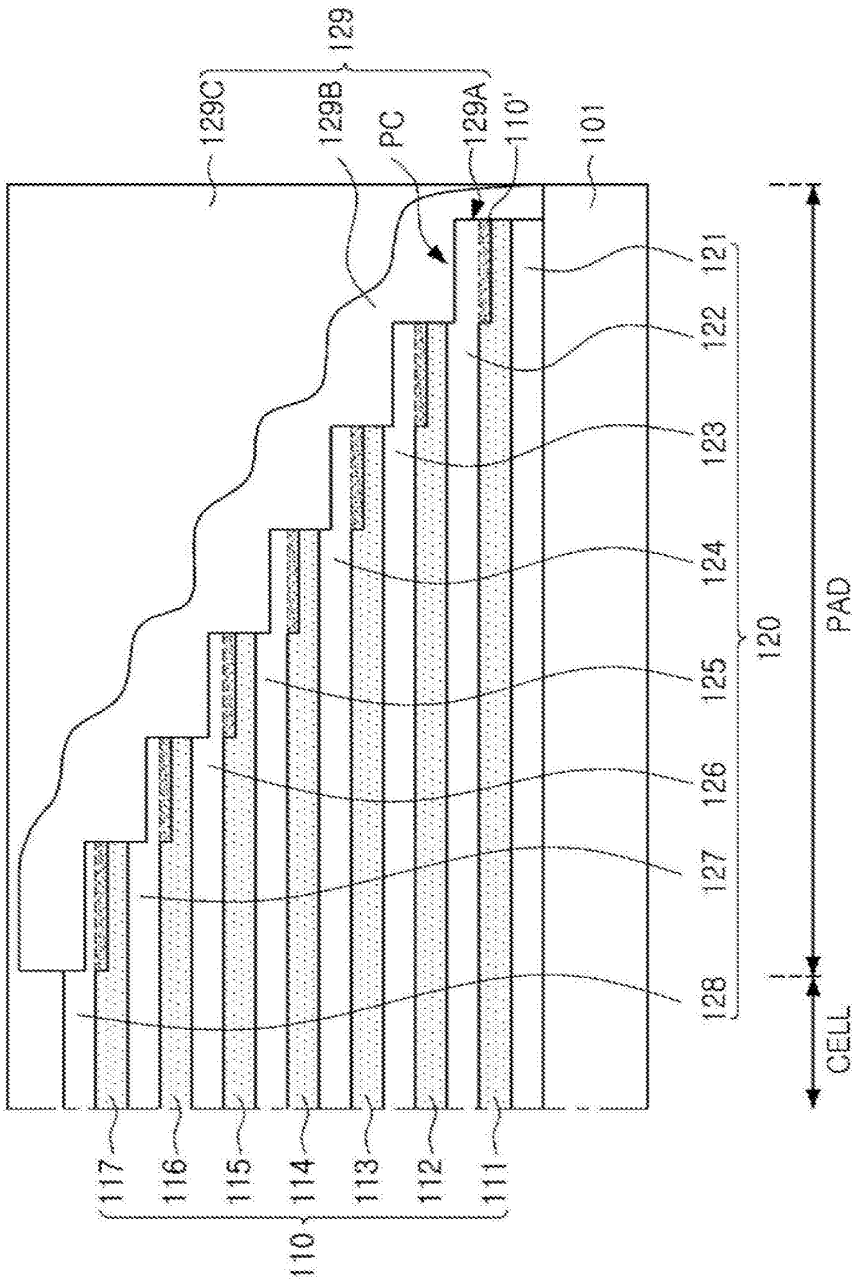


图10F

Micron Ex. 1019, p. 129
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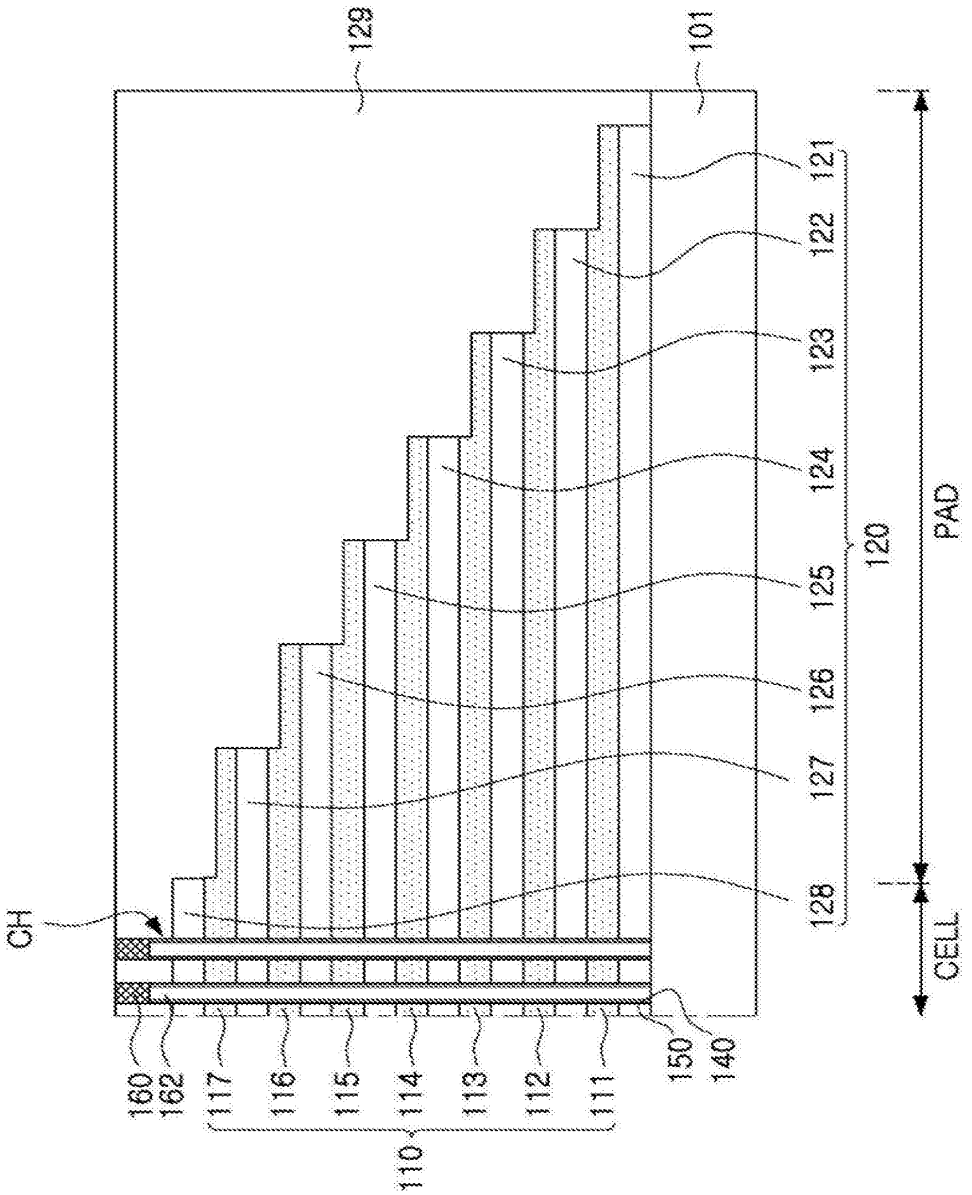


图10G

Micron Ex. 1019, p. 130
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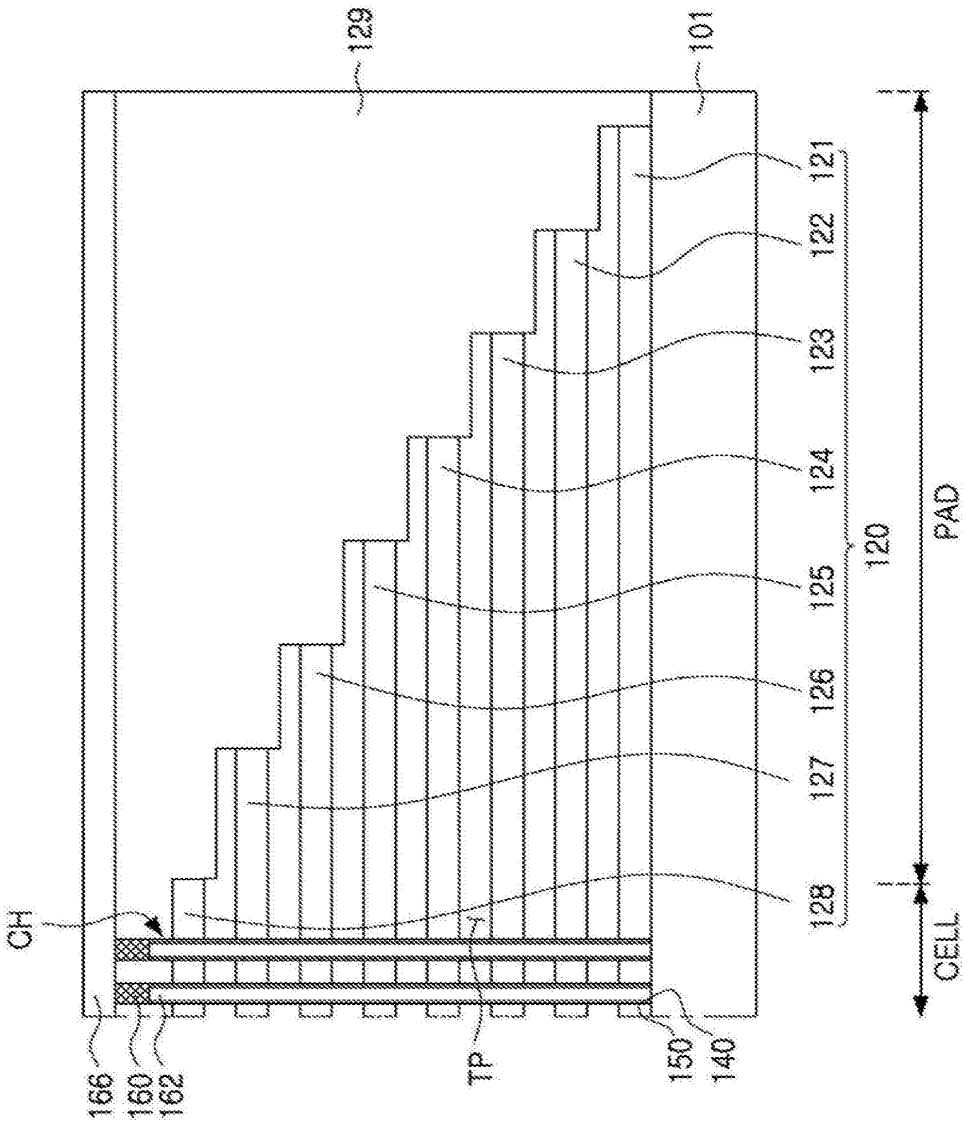


图10H

Micron Ex. 1019, p. 131
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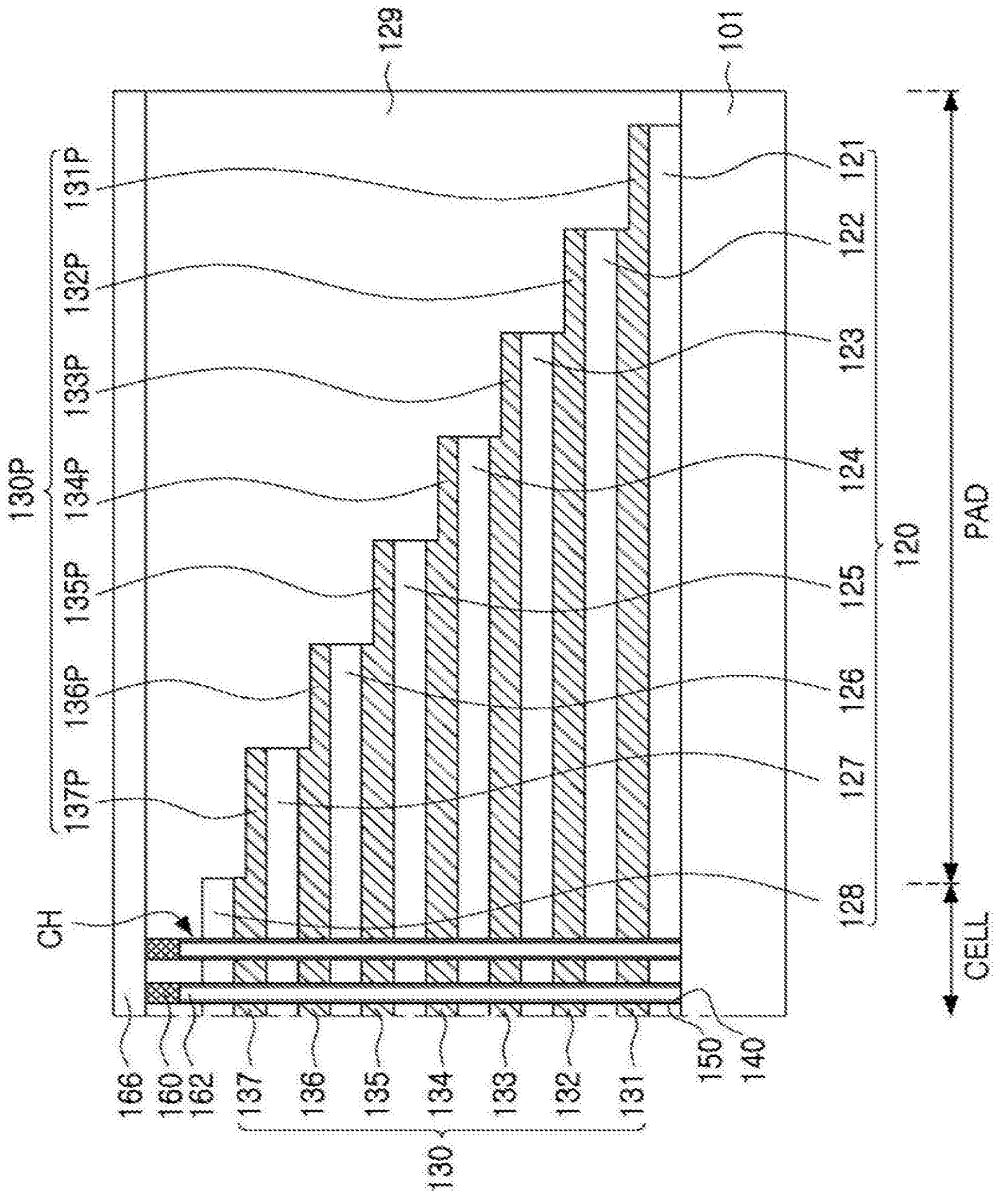


图10I

Micron Ex. 1019, p. 132
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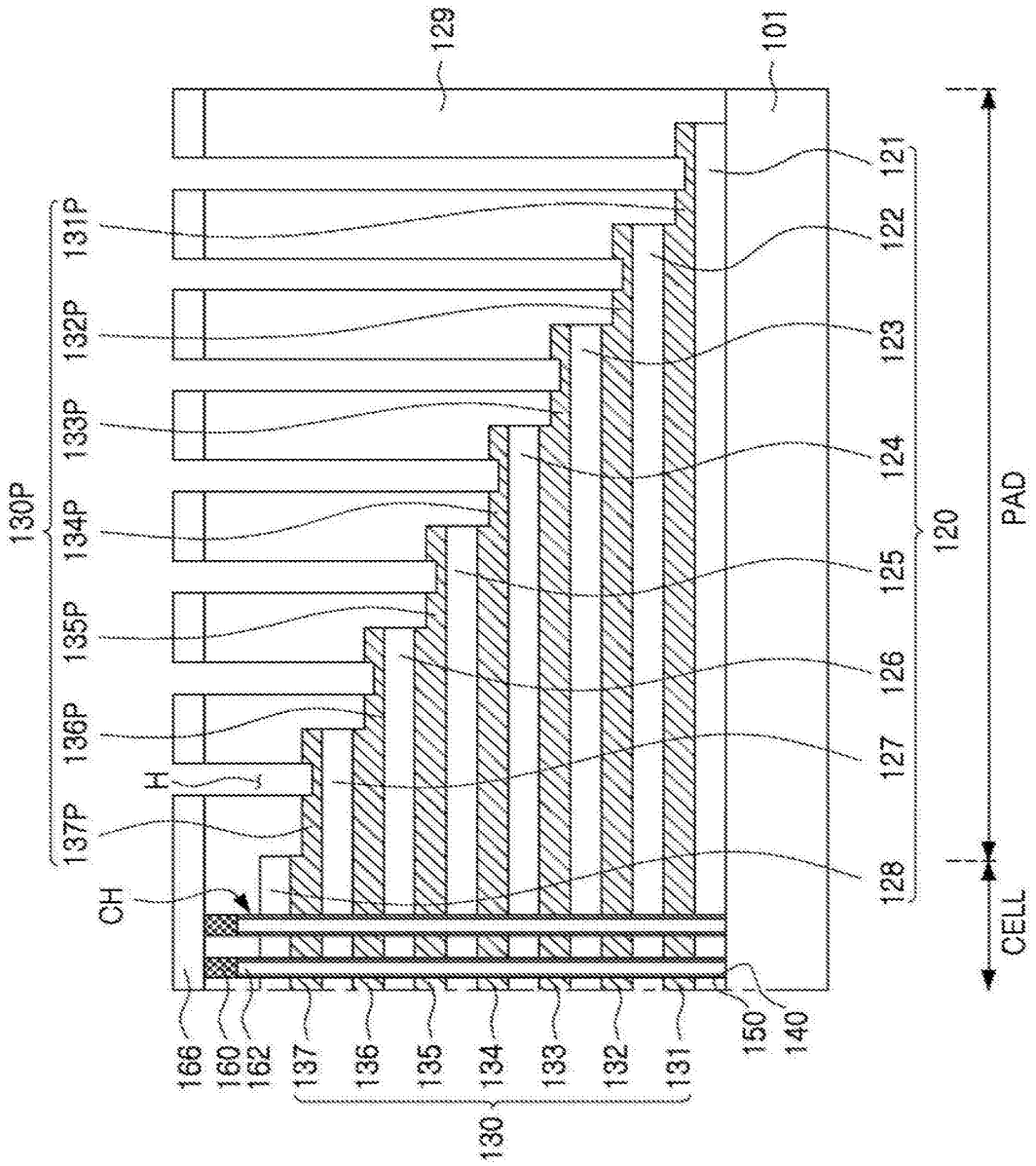


图10J

Micron Ex. 1019, p. 133
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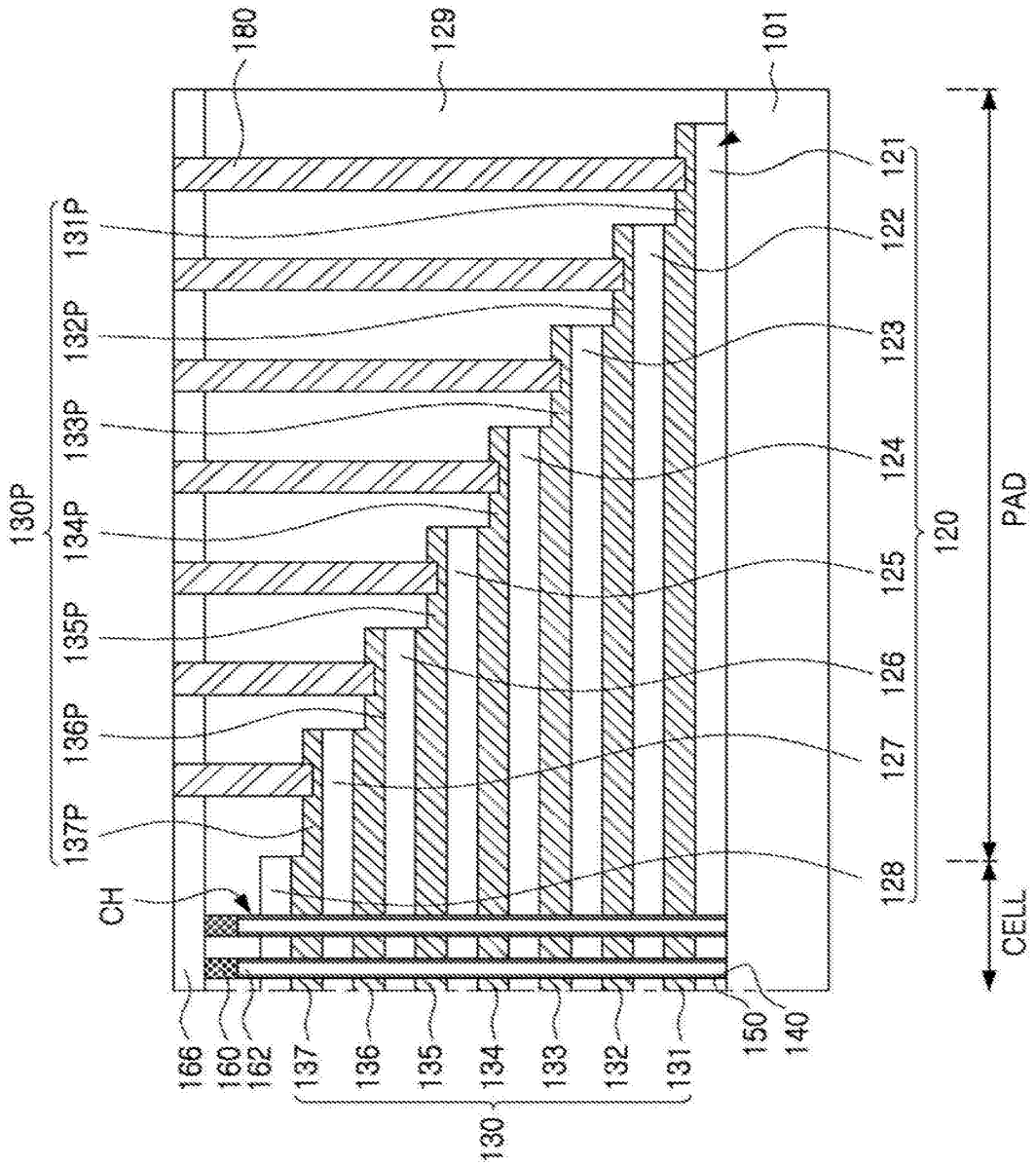


图10K

Micron Ex. 1019, p. 134
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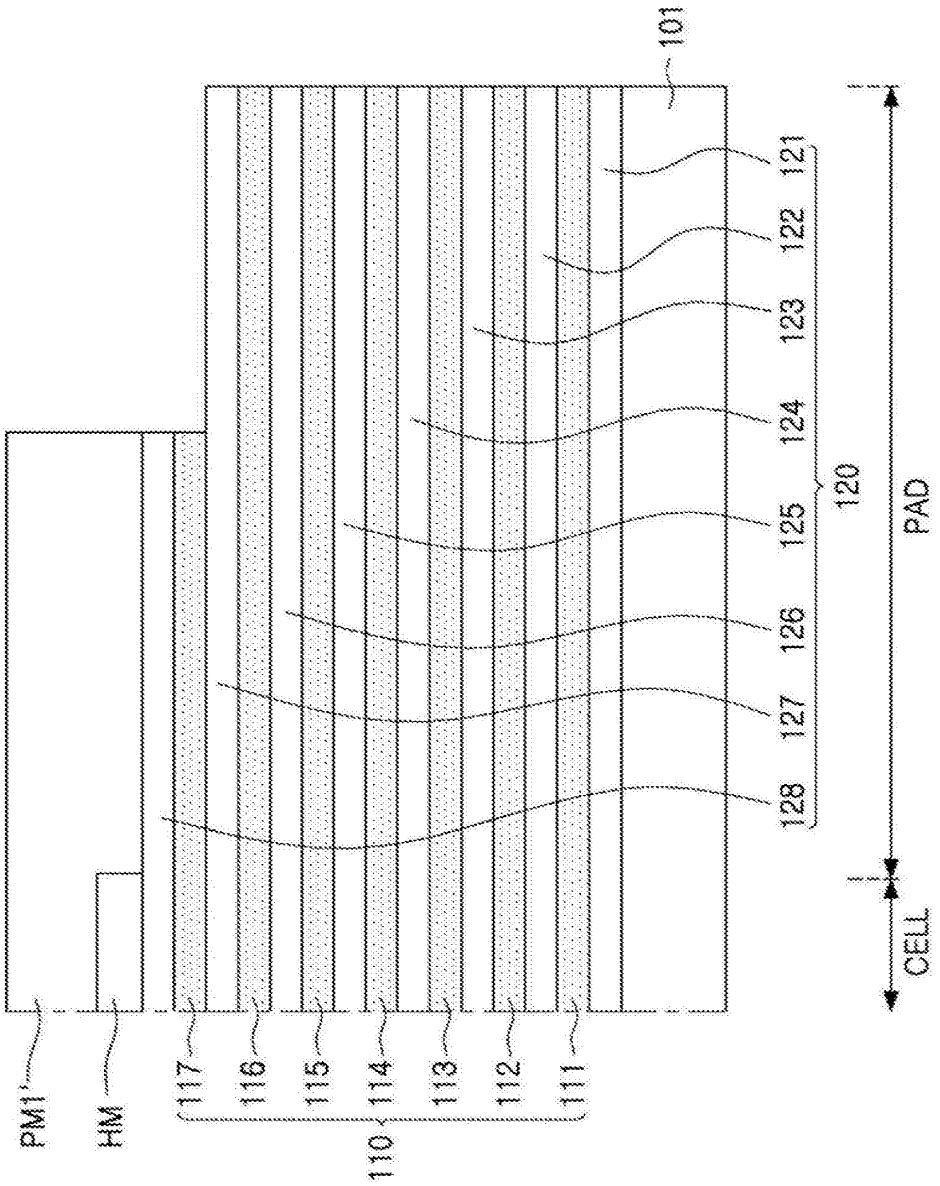


图11A

Micron Ex. 1019, p. 135
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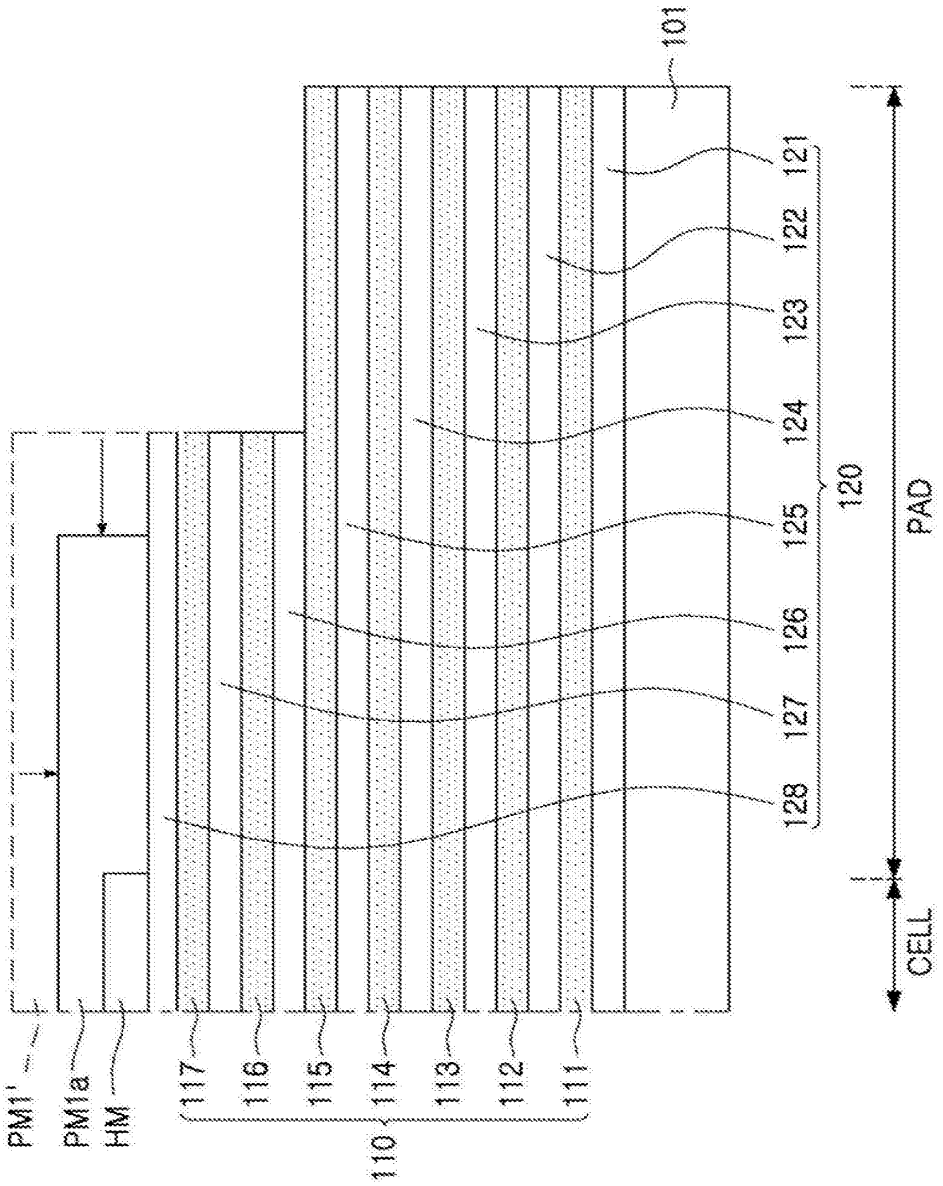


图11B

Micron Ex. 1019, p. 136
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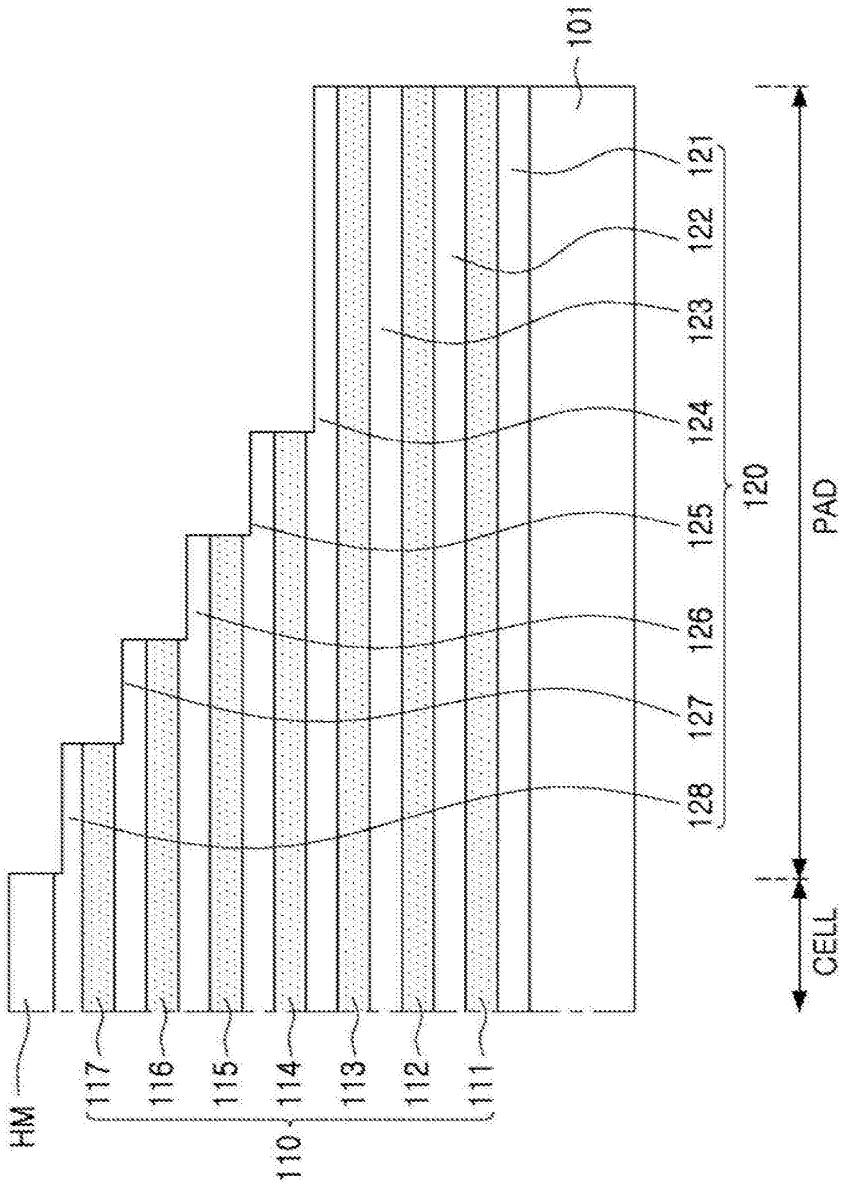


图11C

Micron Ex. 1019, p. 137
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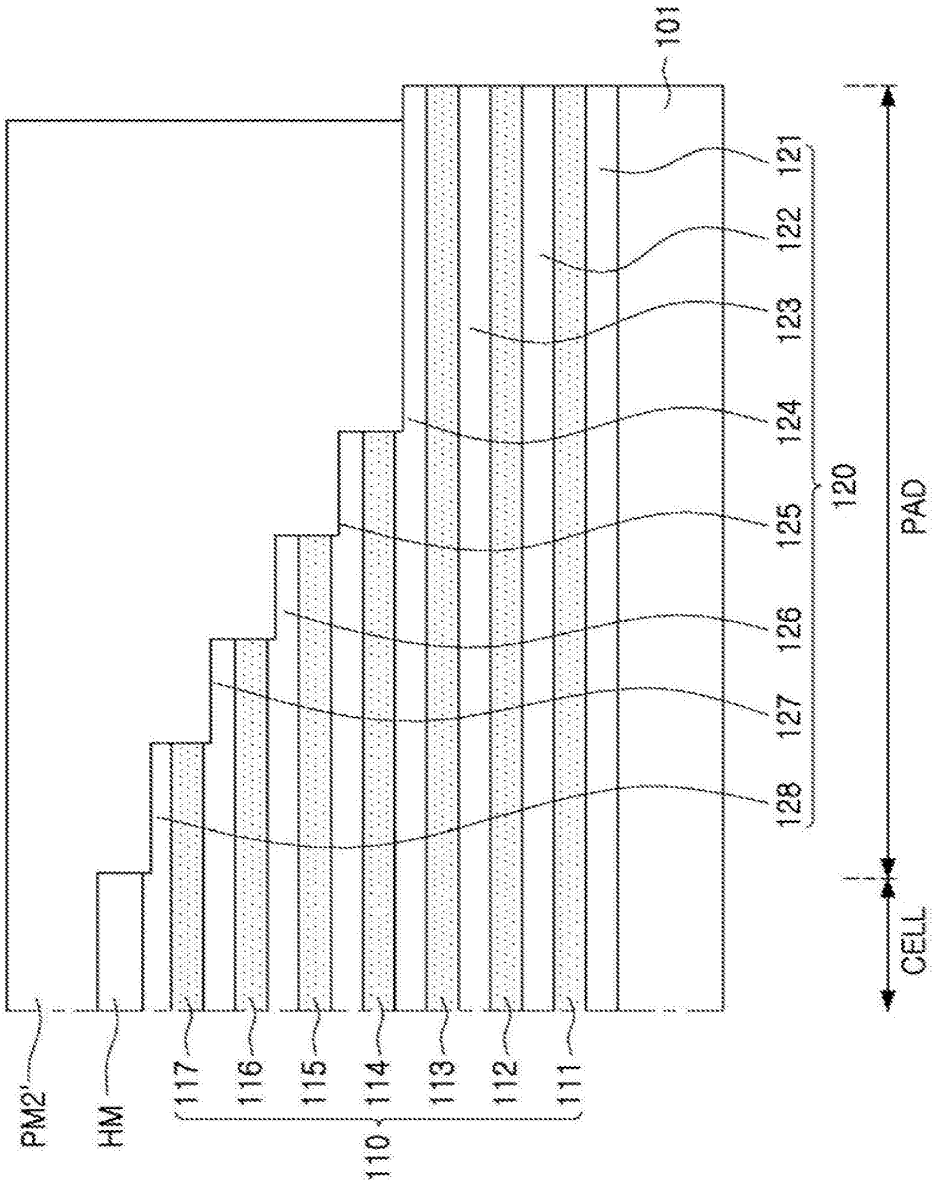


图11D

Micron Ex. 1019, p. 138
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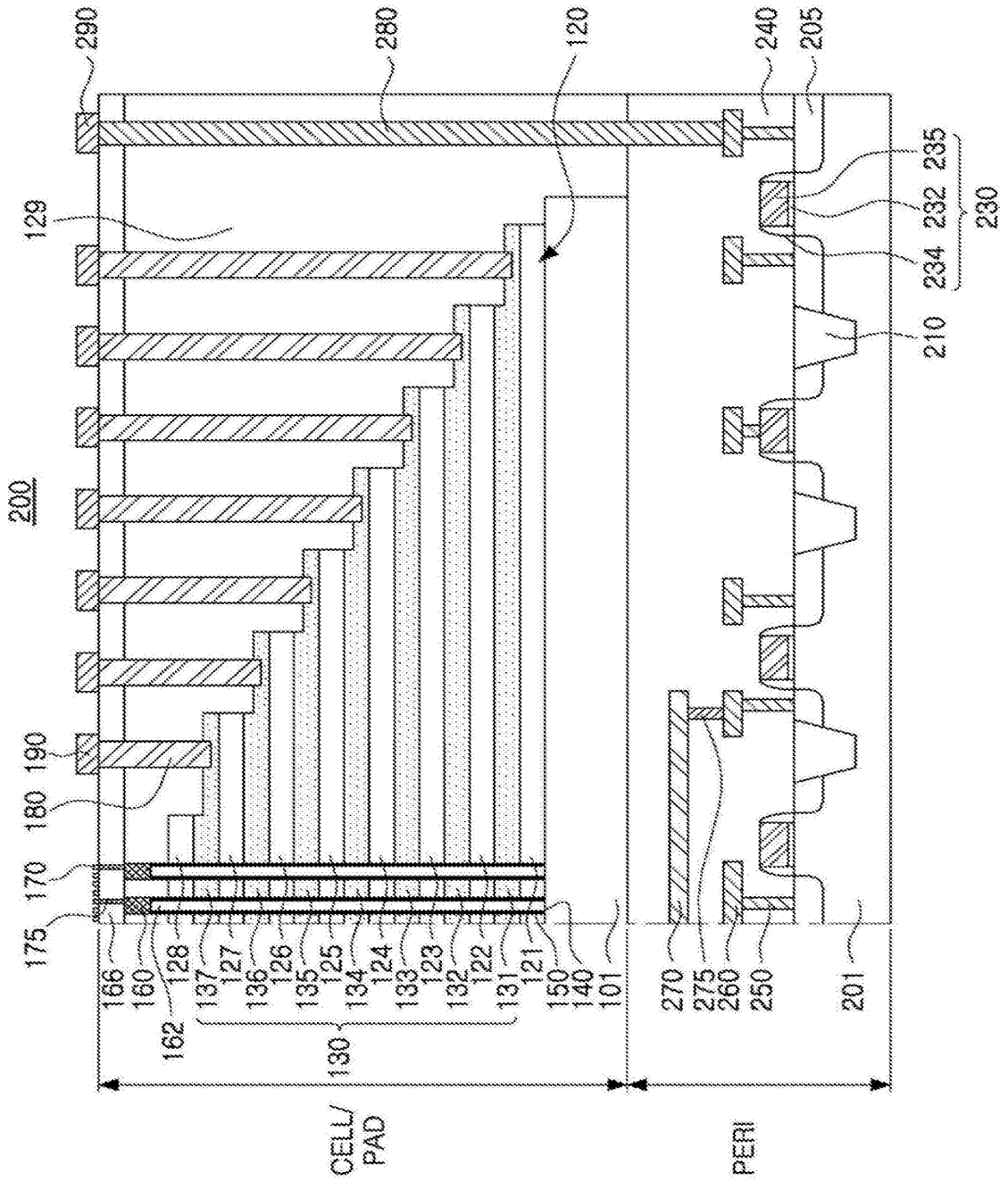


图12

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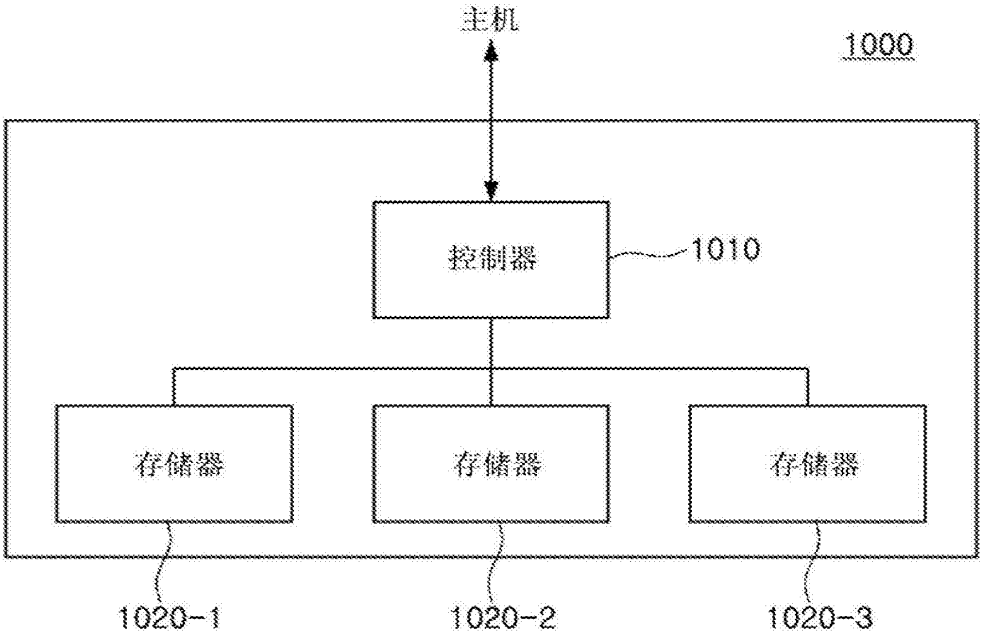


图13

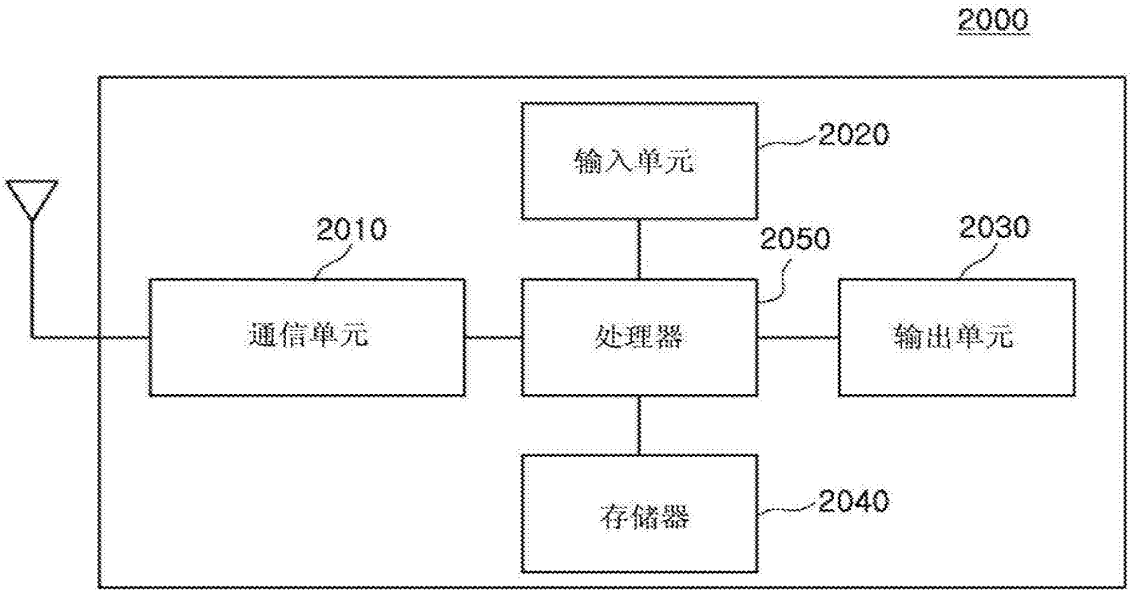


图14

Micron Ex. 1019, p. 140
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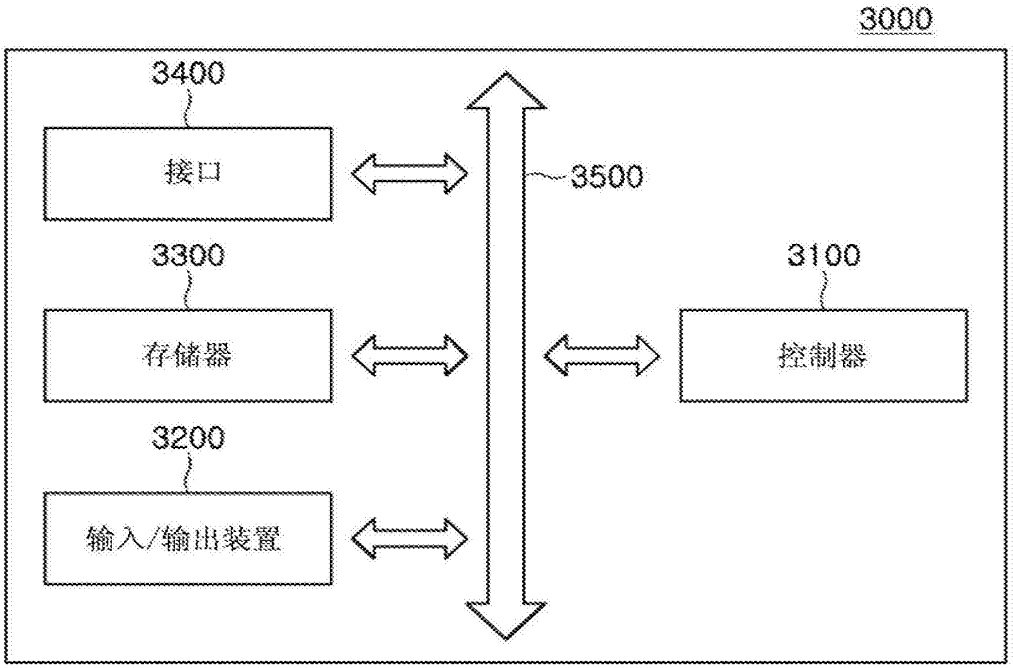


图15

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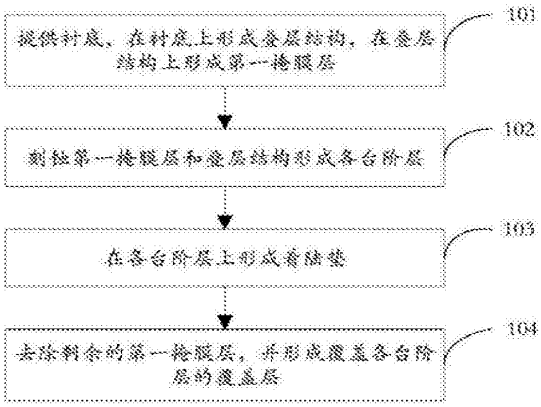
权利要求书1页 说明书4页 附图3页

(54)发明名称

台阶结构及其形成方法

(57)摘要

本发明公开了一种台阶结构及其形成方法，属于半导体技术领域。所述方法包括：提供衬底，在衬底上形成叠层结构，在叠层结构上形成第一掩膜层；刻蚀第一掩膜层和叠层结构形成各台阶层；在各台阶层上形成着陆垫；去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层。本发明中，通过在各台阶层上形成着陆垫，增加了台阶层之间互联部分的厚度，使得即使是很薄的字线需求，通过单张掩膜来形成台阶间的互连亦是可行的。



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1.一种台阶结构的形成方法，其特征在于，包括：

提供衬底，在所述衬底上形成叠层结构，在所述叠层结构上形成第一掩膜层；

刻蚀所述第一掩膜层和所述叠层结构形成各台阶层；

在各台阶层上形成着陆垫；

去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层。

2.根据权利要求1所述的方法，其特征在于，所述刻蚀所述第一掩膜层和所述叠层结构形成各台阶层，具体为：在所述第一掩膜层上旋涂光阻层，以所述光阻层为掩膜，多次刻蚀所述第一掩膜层和所述叠层结构形成各台阶层。

3.根据权利要求1所述的方法，其特征在于，

所述叠层结构，具体为多个层叠的氮氧层组，所述氮氧层组自上至下依次为氧化物层和氮化物层；

刻蚀所述第一掩膜层和所述叠层结构形成的各台阶层分别对应一个所述氮氧层组。

4.根据权利要求3所述的方法，其特征在于，所述在各台阶层上形成着陆垫，具体包括：

在除最底层台阶层外的其他台阶层中，去除部分氮化物层，使氮化物层相对于氧化物层凹陷，形成第一凹陷结构；

形成第二掩膜层，所述第二掩膜层覆盖各台阶层及剩余的第一掩膜层，并将所述第一凹陷结构完全填充；

去除第二掩膜层，并在所述第一凹陷结构中形成填充结构，所述填充结构高于所述第一凹陷结构并覆盖部分对应的氧化物层的侧面；

去除各台阶层中的氧化物层，呈现各台阶层中的氮化物层；

形成加固层，所述加固层覆盖各台阶层中的氮化物层、填充结构及剩余的第一掩膜层；

去除部分加固层、所述填充结构和部分剩余的第一掩膜层，形成各台阶层的着陆垫，使除最底层台阶层外的各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

5.根据权利要求4所述的方法，其特征在于，所述去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层，具体为：去除当前剩余的第一掩膜层及其上的加固层和其下的氧化物层，并形成覆盖层，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

6.一种台阶结构，其特征在于，包括：

衬底及衬底上的叠层结构；

形成于所述叠层结构上的各台阶层；

形成于各台阶层上的着陆垫；

覆盖各台阶层的覆盖层。

7.根据权利要求6所述的台阶结构，其特征在于，所述叠层结构，具体为多个层叠的氮氧层组，所述氮氧层组自上至下依次为氧化物层和氮化物层。

8.根据权利要求7所述的台阶结构，其特征在于，各台阶层分别对应一个氮氧层组，各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

9.根据权利要求8所述的台阶结构，其特征在于，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

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台阶结构及其形成方法

技术领域

[0001] 本发明涉及半导体技术领域，尤其涉及一种台阶结构及其形成方法。

背景技术

[0002] 闪存是一种非易变性的存储器，是电可擦除且可编程的只读存储器的一种特殊结构，其运作原理是通过改变晶体管或存储单元的临界电压来控制门极通道的开关以达到存储数据的目的，使存储在存储器中的数据不会因电源中断而消失。闪存以其便捷、存储密度高、可靠性好等优点成为非挥发性存储器研究的热点。从二十世纪八十年代第一个闪存产品问世以来，随着技术的发展和各类电子产品对存储的需求，闪存被广泛的应用于手机、笔记本、掌上电脑和U盘等移动和通讯设备中，并占据了非挥发性半导体存储器的大部分市场份额。

[0003] 如今，经历了平面型闪存存储器的发展时期，已进入了三维闪存存储器的发展热潮，其主要特色是将平面结构转换为立体结构，通过光刻工艺形成台阶结构，在台阶结构中形成多个横向和纵向的存储单元阵列，并通过在台阶结构中形成水平方向上的字线(Word line)和竖直方向的位线(Bit line)来准确定位各存储区，进而对存储区中的数据进行操作。目前的三维存储器，其台阶结构中字线的厚度是均匀的，然而，随着人们对存储器的容量及体积的要求不断提升，使形成台阶结构的堆栈会不断减小，从而字线的厚度会越来越小，进而导致用单个掩膜来创建台阶间的互连会越来越困难。

发明内容

[0004] 为解决现有技术的不足，本发明提供一种台阶结构及其形成方法。

[0005] 一方面，本发明提供一种台阶结构的形成方法，包括：

[0006] 提供衬底，在所述衬底上形成叠层结构，在所述叠层结构上形成第一掩膜层；

[0007] 刻蚀所述第一掩膜层和所述叠层结构形成各台阶层；

[0008] 在各台阶层上形成着陆垫；

[0009] 去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层。

[0010] 可选地，所述刻蚀所述第一掩膜层和所述叠层结构形成各台阶层，具体为：在所述第一掩膜层上旋涂光阻层，以所述光阻层为掩膜，多次刻蚀所述第一掩膜层和所述叠层结构形成各台阶层。

[0011] 可选地，所述叠层结构，具体为多个层叠的氮氧层组，所述氮氧层组自上至下依次为氧化物层和氮化物层；

[0012] 刻蚀所述第一掩膜层和所述叠层结构形成的各台阶层分别对应一个所述氮氧层组。

[0013] 可选地，所述在各台阶层上形成着陆垫，具体包括：

[0014] 在除最底层台阶层外的其他台阶层中，去除部分氮化物层，使氮化物层相对于氧化物层凹陷，形成第一凹陷结构；

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[0015] 形成第二掩膜层，所述第二掩膜层覆盖各台阶层及剩余的第一掩膜层，并将所述第一凹陷结构完全填充；

[0016] 去除第二掩膜层，并在所述第一凹陷结构中形成填充结构，所述填充结构高于所述第一凹陷结构并覆盖部分对应的氧化物层的侧面；

[0017] 去除各台阶层中的氧化物层，呈现各台阶层中的氮化物层；

[0018] 形成加固层，所述加固层覆盖各台阶层中的氮化物层、填充结构及剩余的第一掩膜层；

[0019] 去除部分加固层、所述填充结构和部分剩余的第一掩膜层，形成各台阶层的着陆垫，使除最底层台阶层外的各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

[0020] 可选地，所述去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层，具体为：去除当前剩余的第一掩膜层及其上的加固层和其下的氧化物层，并形成覆盖层，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

[0021] 另一方面，本发明提供一种台阶结构，包括：

[0022] 衬底及衬底上的叠层结构；

[0023] 形成于所述叠层结构上的各台阶层；

[0024] 形成于各台阶层上的着陆垫；

[0025] 覆盖各台阶层的覆盖层。

[0026] 可选地，所述叠层结构，具体为多个层叠的氮氧层组，所述氮氧层组自上至下依次为氧化物层和氮化物层。

[0027] 可选地，各台阶层分别对应一个氮氧层组，各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

[0028] 可选地，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

[0029] 本发明的优点在于：

[0030] 本发明中，通过在各台阶层上形成着陆垫，增加了台阶层之间互联部分的厚度，使得即使是很薄的字线需求，通过单张掩膜来形成台阶间的互连亦是可行的。

附图说明

[0031] 通过阅读下文优选实施方式的详细描述，各种其他的优点和益处对于本领域普通技术人员将变得清楚明了。附图仅用于示出优选实施方式的目的，而并不认为是对本发明的限制。而且在整个附图中，用相同的参考符号表示相同的部件。在附图中：

[0032] 附图1为本发明提供的一种形成台阶结构的方法流程图；

[0033] 附图2和附图3为本发明提供的形成台阶层的结构变化示意图；

[0034] 附图4至附图9为本发明提供的形成着陆垫的结构变化示意图；

[0035] 附图10为本发明提供的部分台阶结构示意图。

具体实施方式

[0036] 下面将参照附图更详细地描述本公开的示例性实施方式。虽然附图中显示了本公开的示例性实施方式，然而应当理解，可以以各种形式实现本公开而不应被这里阐述的实

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施方式所限制。相反，提供这些实施方式是为了能够更透彻地理解本公开，并且能够将本公开的范围完整的传达给本领域的技术人员。

[0037] 实施例一

[0038] 根据本发明的实施方式，提供一种台阶结构的形成方法，如图1所示，包括：

[0039] 提供衬底，在衬底上形成叠层结构，在叠层结构上形成第一掩膜层；

[0040] 刻蚀第一掩膜层和叠层结构形成各台阶层；

[0041] 在各台阶层上形成着陆垫(Landing Pad)；

[0042] 去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层。

[0043] 根据本发明的实施方式，刻蚀第一掩膜层和叠层结构形成各台阶层，具体为：在第一掩膜层上旋涂光阻层，以光阻层为掩膜，多次刻蚀第一掩膜层和叠层结构形成各台阶层。

[0044] 根据本发明的实施方式，如图2和图3所示，叠层结构，具体为多个层叠的氮氧层组，氮氧层组自上至下依次为氧化物层(图中未示出)和氮化物层(图中未示出)；

[0045] 对应地，刻蚀第一掩膜层和叠层结构形成的各台阶层分别对应一个氮氧层组。

[0046] 需要说明地，在本实施例中，对叠层结构的氮氧层组的数量及形成的台阶层的数量不作具体限定，具体依需求而定，附图仅用于示例说明。

[0047] 根据本发明的实施方式，在各台阶层上形成着陆垫，如图4至图9所示，具体包括：

[0048] 在除最底层台阶层外的其他台阶层中，去除部分氮化物层，使氮化物层相对于氧化物层凹陷，形成第一凹陷结构(Nitride Recess)；

[0049] 形成第二掩膜层，第二掩膜层覆盖各台阶层及剩余的第一掩膜层，并将第一凹陷结构完全填充(Poly Dep)；

[0050] 去除第二掩膜层，并在第一凹陷结构中形成填充结构，填充结构高于第一凹陷结构并覆盖部分对应的氧化物层的侧面(Poly Etch)；

[0051] 去除各台阶层中的氧化物层，呈现各台阶层中的氮化物层(Oxide Etch)；

[0052] 形成加固层，加固层覆盖各台阶层中的氮化物层、填充结构及剩余的第一掩膜层(Niteide Dep)；

[0053] 去除部分加固层、填充结构和部分剩余的第一掩膜层，形成各台阶层的着陆垫，使除最底层台阶层外的各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构(Nitride/Poly Recess)。

[0054] 其中，第二掩膜层具体为多晶硅，加固层具体为氮化物。

[0055] 根据本发明的实施方式，采用低压化学气相沉积(Low Pressure Chemical Vapor Deposition，简称LPCVD)的方法和/或等离子体增强化学气相沉积(Plasma Enhanced Chemical Vapor Deposition，简称PECVD)的方法形成第二掩膜层；

[0056] 根据本发明的实施方式，采用干法刻蚀(Dry Etch)工艺去除第二掩膜层，并在第一凹陷结构中形成填充结构；

[0057] 根据本发明的实施方式，采用不良梯形覆盖共形工艺(Poor Step Coverage Conformal Process)形成加固层。

[0058] 进一步地，在本实施例中，去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层，具体为：去除当前剩余的第一掩膜层及其上的加固层和其下的氧化物层，并形成覆盖层，覆盖层将第二凹陷结构完全填充，并覆盖各台阶层。

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[0059] 实施例二

[0060] 根据本发明的实施方式，提供一种台阶结构，包括：

[0061] 衬底及衬底上的叠层结构；

[0062] 形成于叠层结构上的各台阶层；

[0063] 形成于各台阶层上的着陆垫；

[0064] 覆盖各台阶层的覆盖层。

[0065] 根据本发明的实施方式，叠层结构，具体为多个层叠的氮氧层组，氮氧层组自上至下依次为氧化物层和氮化物层。

[0066] 根据本发明的实施方式，各台阶层分别对应一个氮氧层组，各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

[0067] 根据本发明的实施方式，覆盖层将第二凹陷结构完全填充，，并覆盖各台阶层。

[0068] 本发明中，通过在各台阶层上形成着陆垫，增加了台阶层之间互联部分的厚度，使得即使是很薄的字线需求，通过单张掩膜来形成台阶间的互连亦是可行的。

[0069] 以上所述，仅为本发明较佳的具体实施方式，但本发明的保护范围并不局限于此，任何熟悉本技术领域的技术人员在本发明揭露的技术范围内，可轻易想到的变化或替换，都应涵盖在本发明的保护范围之内。因此，本发明的保护范围应以所述权利要求的保护范围为准。

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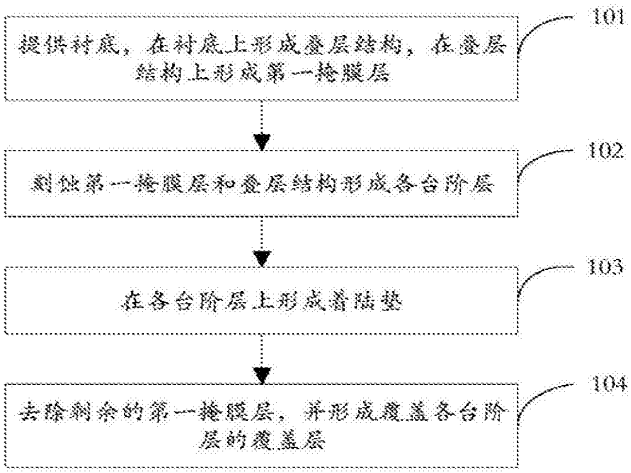


图1

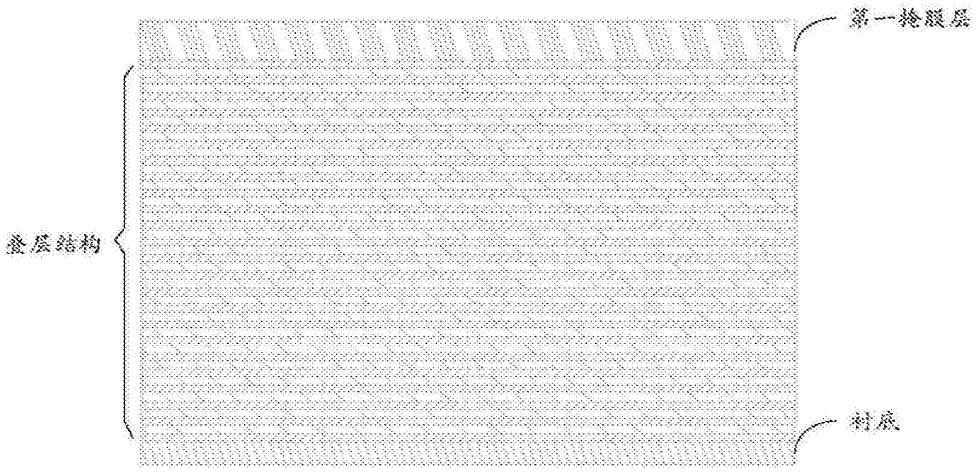


图2

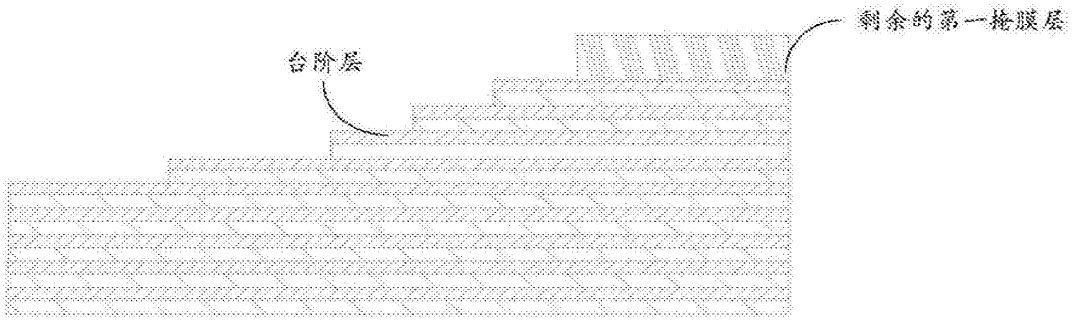


图3

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图4

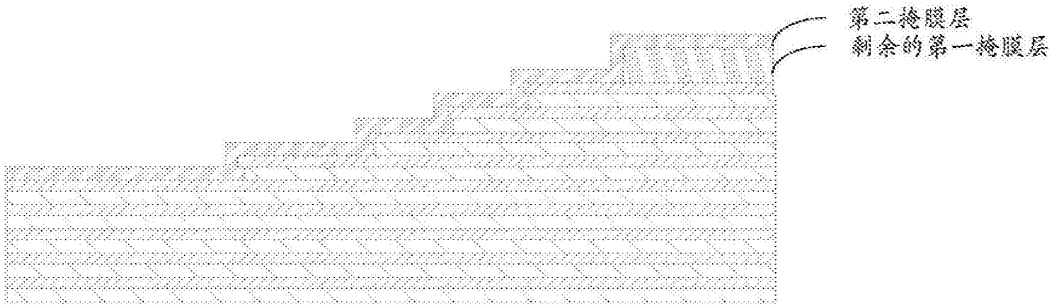


图5

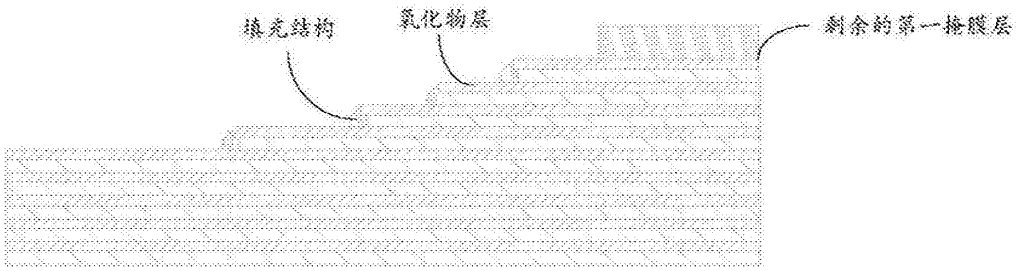


图6

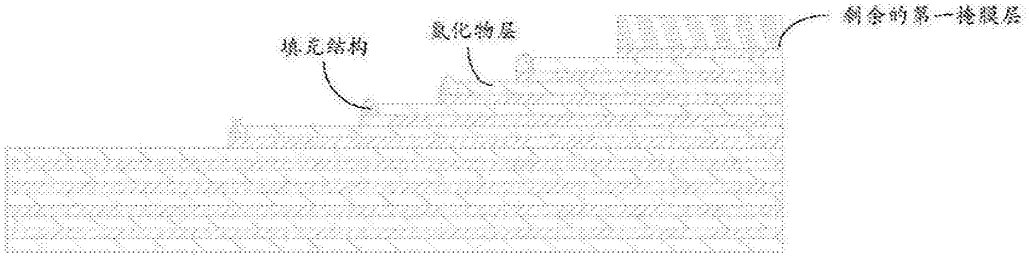


图7

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图8



图9

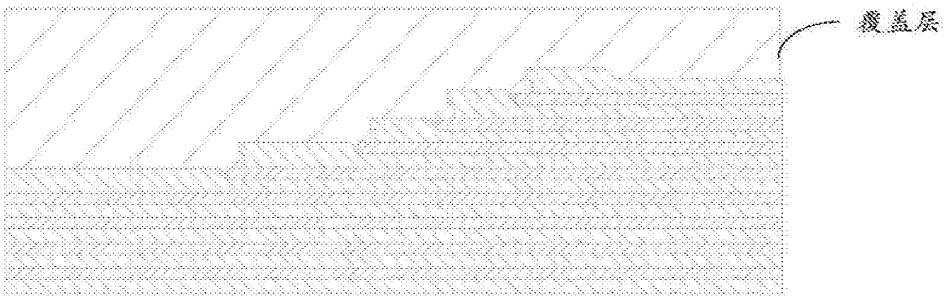


图10

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Espacenet

Bibliographic data: KR20110015338 (A) — 2011-02-15

METHOD FOR FABRICATING VERTICAL CHANNEL TYPE NON-VOLATILE MEMORY DEVICE

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Applicant(s): HYNIX SEMICONDUCTOR INC [KR] ± (HYNIX SEMICONDUCTOR INC)

Classification: - international: *H01L21/8247; H01L27/115*
- cooperative: **H01L21/28282**; **H01L21/76224**; **H01L21/76877**; **H01L21/823487**; **H01L27/11578**; **H01L27/11582**; **H01L29/78642** more

Application number: KR20090073022 20090807 Global Dossier

Priority number (s): KR20090073022 20090807

Abstract of KR20110015338 (A)

PURPOSE: A method for manufacturing a vertical channel type nonvolatile memory device is provided to prevent a layer from being damaged due to the repeated etching processes by reducing the number of etching processes in a slimming process. CONSTITUTION: A plurality of interlayer insulation layers(21) and conductive layers for a gate electrode are alternatively formed on a substrate. A mask pattern(25) is formed on the plurality of interlayer insulation layers and the conductive layer for the gate electrode. The plurality of interlayer insulation layers and the conductive layers for the gate electrode are etched. The conductive layers for the gate electrode are continuously laminated with two layers or more and are firstly etched with one unit. A spacer(26) is formed on the sidewall of the etched surface by the first etching. The plurality of interlayer insulation layers and the conductive layers for the gate electrode are secondly etched.

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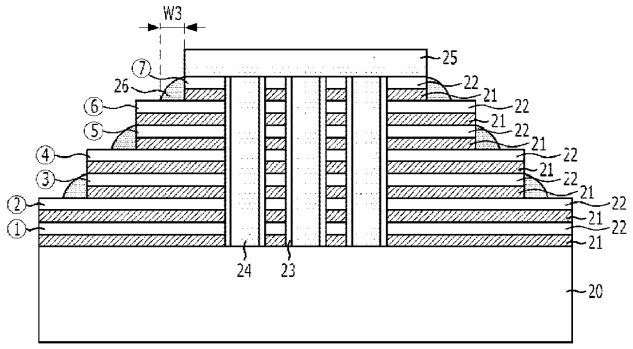
전체 청구항 수 : 총 19 항

(54) 수직채널형 비휘발성 메모리 소자 제조 방법

(57) 요 약

본 기술은 수직채널형 비휘발성 메모리 소자 제조 방법에 관한 것으로서, 기판 상에 복수의 층간절연막 및 게이트 전극용 도전막을 교대로 형성하는 단계; 상기 복수의 층간절연막 및 게이트 전극용 도전막이 형성된 결과물 상에, 메모리 셀 영역을 덮는 마스크 패턴을 형성하는 단계; 상기 마스크 패턴을 식각 베리어로 하여, 상기 게이트 전극용 도전막의 표면이 노출되도록 상기 복수의 층간절연막 및 게이트 전극용 도전막을 식각하되, 적어도 2층 이상의 연속으로 적층된 게이트 전극용 도전막을 하나의 단위로 1차식각하는 단계; 상기 1차식각에 의한 식각면 측벽에 스페이서를 형성하는 단계; 및 상기 마스크 패턴 및 스페이서를 식각베리어로 상기 복수의 층간절연막 및 게이트 전극용 도전막을 2차식각하는 단계를 포함한다. 본 기술에 따르면, 슬리밍 공정시 식각 공정의 반복 횟수를 감소시킴으로써, 식각 공정의 반복에 따른 막 손상을 방지할 수 있으며, 포토레지스트 패턴의 두께 및 폭을 용이하게 조절하여 균일한 면적의 콘택 플러그를 형성할 수 있다.

대 표 도 - 도2c



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특허청구의 범위

청구항 1

기판 상에 복수의 층간절연막 및 게이트 전극용 도전막을 교대로 형성하는 단계;

상기 복수의 층간절연막 및 게이트 전극용 도전막이 형성된 결과물 상에, 메모리 셀 영역을 덮는 마스크 패턴을 형성하는 단계;

상기 마스크 패턴을 식각 베리어로 하여, 상기 게이트 전극용 도전막의 표면이 노출되도록 상기 복수의 층간절연막 및 게이트 전극용 도전막을 식각하되, 적어도 2층 이상의 연속으로 적층된 게이트 전극용 도전막을 하나의 단위로 1차식각하는 단계;

상기 1차식각에 의한 식각면 측벽에 스페이서를 형성하는 단계; 및

상기 마스크 패턴 및 스페이서를 식각베리어로 상기 복수의 층간절연막 및 게이트 전극용 도전막을 2차식각하는 단계

를 포함하는 수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 2

제 1 항에 있어서,

상기 복수의 층간절연막 및 게이트 전극용 도전막 형성 단계 후에,

상기 복수의 층간절연막 및 게이트 전극용 도전막을 식각하여 상기 기판 표면을 노출시키는 트렌치를 형성하는 단계;

상기 트렌치의 내벽에 전하차단막, 전하포획막 및 터널절연막을 차례로 형성하는 단계; 및

상기 전하차단막, 전하포획막 및 터널절연막이 형성된 트렌치 내에 채널용 막을 매립하는 단계

를 더 포함하는 수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 3

제 1 항에 있어서,

상기 2차식각에 의해 복수의 게이트 전극용 도전막의 표면이 각각 노출된 결과물의 전체 구조 상에 층간절연막을 형성하는 단계;

상기 층간절연막을 식각하여 복수의 게이트 전극용 도전막의 표면을 각각 노출시키는 트렌치를 형성하는 단계; 및

상기 트렌치 내에 도전막을 매립하여 콘택 플러그를 형성하는 단계

를 더 포함하는 수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 4

제 1 항에 있어서,

상기 1차식각 단계는,

상기 복수의 층간절연막 및 게이트 전극용 도전막을 계단형으로 패터닝하는

수직채널형 비휘발성 메모리 소자 제조 방법.

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청구항 5

제 1 항에 있어서,

상기 1차식각 단계는,

상기 기판 또는 하부 선택 트랜지스터가 노출될 때까지 소정 횟수 반복하여 식각 공정을 수행하는

수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 6

제 5 항에 있어서,

상기 1차식각 단계는,

상기 마스크 패턴의 폭을 감소시키면서 소정 횟수 반복하여 식각 공정을 수행하는

수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 7

제 1 항에 있어서,

상기 스페이서는,

게이트 전극용 도전막 상의 콘택 플러그 예정 영역을 덮는 두께로 형성되는

수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 8

제 1 항에 있어서,

상기 스페이서는,

포토레지스터, 질화막 또는 산화막을 포함하는

수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 9

제 1 항에 있어서,

상기 스페이서 형성 단계는,

상기 1차식각이 수행된 결과물의 전면에 스페이서용 절연막을 형성하는 단계; 및

상기 1차식각에 의해 노출된 게이트 전극용 도전막의 표면이 노출될때까지 에치백 공정을 수행하는 단계

를 포함하는 수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 10

제 1 항에 있어서,

상기 2차식각 단계 후에,

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상기 스페이서를 제거하는 단계

를 더 포함하는 수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 11

제 1 항에 있어서,

상기 1차식각시, 적어도 4층 이상의 연속으로 적층된 게이트 전극용 도전막을 하나의 단위로 식각 공정을 수행하는 경우,

상기 스페이서 형성 단계 및 2차식각 단계를 상기 복수의 게이트 전극용 도전막의 표면이 전부 노출될 때까지 반복 수행하는

수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 12

제 11 항에 있어서,

상기 마스크 패턴의 폭을 감소시키면서 상기 2차식각 공정을 반복 수행하는

수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 13

기판 상에 복수의 제1물질막 및 제2물질막을 교대로 형성하는 단계;

상기 복수의 제1물질막 및 제2물질막이 형성된 결과물 상에, 메모리 셀 영역을 덮는 마스크 패턴을 형성하는 단계;

상기 마스크 패턴을 식각 베리어로하여 상기 제2물질막의 표면이 노출되도록 복수의 제1물질막 및 제2물질막을 식각하되, 적어도 2층 이상의 연속으로 적층된 제2물질막을 하나의 단위로 1차식각하는 단계;

상기 1차식각에 의한 식각면 측벽에 스페이서를 형성하는 단계; 및

상기 마스크 패턴 및 스페이서를 식각베리어로 상기 복수의 제1물질막 및 제2물질막을 2차식각하는 단계

를 포함하는 수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 14

제 13 항에 있어서,

상기 제1물질막은 층간절연막이고,

상기 제2물질막은 게이트 전극용 도전막 또는 희생막인

수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 15

제 13 항에 있어서,

상기 1차식각 단계는,

상기 복수의 제1물질막 및 제2물질막을 계단형으로 패터닝하는

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수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 16

제 13 항에 있어서,

상기 1차식각 단계는,

상기 기판 또는 하부 선택 트랜지스터가 노출될 때까지 소정 횟수 반복하여 식각 공정을 수행하는

수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 17

제 16 항에 있어서,

상기 1차식각 단계는,

상기 마스크 패턴의 폭을 감소시키면서 반복하여 식각 공정을 수행하는

수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 18

제 13 항에 있어서,

상기 1차식각시, 적어도 4층 이상의 연속으로 적층된 제2물질막을 하나의 단위로 식각 공정을 수행하는 경우,

상기 스페이서 형성 단계 및 2차식각 단계를 상기 복수의 제2물질막의 표면이 전부 노출될 때까지 반복 수행하는

수직채널형 비휘발성 메모리 소자 제조 방법.

청구항 19

제 18 항에 있어서,

상기 마스크 패턴의 폭을 감소시키면서 상기 2차식각 공정을 반복 수행하는

수직채널형 비휘발성 메모리 소자 제조 방법.

명 세 서

발명의 상세한 설명

기 술 분 야

[0001] 본 발명은 반도체 소자 제조 방법에 관한 것으로, 보다 상세하는 수직채널형 비휘발성 메모리 소자 제조 방법에 관한 것이다.

배 경 기 술

[0002] 비휘발성 메모리 소자는 전원공급이 차단되더라도 저장된 데이터가 그대로 유지되는 메모리 소자이다. 최근 실리콘 기판 상에 단층으로 메모리 소자를 제조하는 2차원 구조의 메모리 소자의 집적도 향상이 한계에 도달함에 따라, 실리콘 기판으로부터 수직으로 메모리 셀을 적층하는 3차원 구조의 비휘발성 메모리 소자가 제안되고 있

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다.

[0003] 이하, 도면을 참조하여 종래기술에 따른 3차원 구조의 비휘발성 메모리 소자 제조 방법을 상세히 살펴보도록 한다.

[0004] 도 1a 내지 도 1e는 종래기술에 따른 3차원 구조의 비휘발성 메모리 소자 제조 공정을 설명하기 위한 공정 단면도이다.

[0005] 도 1a에 도시된 바와 같이, 기판(10) 상에 복수의 층간절연막(11) 및 게이트 전극용 도전막(12)을 교대로 형성한 후, 이를 식각하여 기판(10)을 노출시키는 트렌치를 형성한다.

[0006] 이어서, 트렌치의 내벽에 전하차단막, 전하포획막 및 터널절연막(13)을 차례로 형성한 후, 트렌치 내에 채널용 막(14)을 매립한다. 이로써, 기판(10)으로부터 수직으로 돌출되는 채널을 따라 적층되는 복수의 메모리 셀들이 형성된다. 본 도면에서는 설명의 편의를 위하여, 전하차단막, 전하포획막 및 터널절연막을 하나의 막으로 도시하였으며, 도면 부호 "13"으로 표시하였다.

[0007] 도 1b에 도시된 바와 같이, 메모리 셀이 형성된 결과물 상에 메모리 셀 예정영역을 덮으면서, 콘택 플러그 예정영역을 노출시키는 마스크 패턴(15)을 형성한다.

[0008] 여기서, 마스크 패턴(15)은 복수의 게이트 전극용 도전막의 표면을 노출시키기 위한 복수회의 식각 공정에서 식각 베리어로서 사용하기 위한 것으로, 이와 같은 식각 공정을 이하 슬리밍(slimming) 공정이라 한다.

[0009] 최초에 형성되는 마스크 패턴(15)의 폭(W)은 최하층 즉, 기판(10)상에 첫번째로 형성된 게이트 전극용 도전막(12)의 콘택 플러그 예정 영역을 노출시킬 수 있는 값으로 결정된다. 또한, 최초에 형성되는 마스크 패턴(15)의 두께(D)는 복수회에 걸친 식각 공정에서의 손실을 감안하여 충분한 두께로 형성된다.

[0010] 이어서, 마스크 패턴(15)을 식각 베리어로 최상부에 형성된 층간절연막(11) 및 게이트 전극용 도전막(12)을 식각한다.

[0011] 도 1c에 도시된 바와 같이, 마스크 패턴(15A)의 폭(W1)을 소정값 감소시키는데, 마스크 패턴(15A)의 폭(W1)은 기판(10)으로부터 두번째로 형성된 게이트 전극용 도전막(12)의 콘택 플러그 예정 영역을 노출시킬 수 있는 값으로 결정된다.

[0012] 이어서, 마스크 패턴(15A)을 식각베리어로 최상부에 형성된 층간절연막(11) 및 게이트 전극용 도전막(12)을 식각한다. 이때, 최상부에 형성된 층간절연막(11) 및 게이트 전극용 도전막(12)을 식각하는 과정에서, 단차가 유지되면서 하부의 층간절연막(11) 및 게이트 전극용 도전막(12)이 함께 식각된다.

[0013] 도 1d에 도시된 바와 같이, 마스크 패턴(15B)의 폭(W2)을 점차 감소시키면서 층간절연막(11) 및 게이트 전극용 도전막(12) 식각 공정을 반복 수행한다. 이와 같은 슬리밍 공정을 통해, 복수의 게이트 전극용 도전막(12)의 표면을 각각 노출시키는 계단형의 구조물이 형성된다. 여기서, 각 층에 노출된 복수의 게이트 전극용 도전막(12)의 표면은 콘택 플러그 예정 영역으로서 후속 공정에 의해 콘택 플러그가 형성된다.

[0014] 도 1e에 도시된 바와 같이, 슬리밍 공정이 수행된 결과물의 전체 구조 상에 절연막(16)을 형성한 후, 복수의 게이트 전극용 도전막(12)의 표면을 각각 노출시키는 콘택홀을 형성한다.

[0015] 이어서, 콘택홀 내에 도전막을 매립하여, 복수의 게이트 전극용 도전막(12)으로 각각 연결되는 복수의 콘택 플러그(17)을 형성한다. 이어서, 본 도면에서는 도시되지 않았으나, 콘택 플러그(17)와 연결되는 워드라인을 형성하는 후속 공정이 진행된다.

[0016] 그러나, 전술한 바와 같은 종래기술에 따르면, 슬리밍 공정을 수행함에 있어서 복수의 게이트 전극용 도전막(12) 표면을 노출시키기 위한 식각 공정을 반복 수행함에 따라 문제점이 발생한다.

[0017] 첫째, 슬리밍 공정을 수행하는 과정에서, 막들이 손상되는 문제점이 발생한다. 예를 들어, 도 1a 내지 도 1e에 도시된 바와 같이 총 7개의 메모리 셀을 적층시키는 경우, 각 메모리 셀의 게이트 전극 표면을 각각 노출시키기 위하여 총 6번의 식각 공정을 반복 수행하게 된다. 이와 같이, 식각 공정을 수회 반복 수행하는 경우, 반복되는 식각 공정에서 막들이 손상되는 문제점이 발생한다.

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[0018] 또한, 포토레지스트 패턴(15)의 폭을 감소시키면서 식각 공정을 반복하기 때문에, 포토레지스트 패턴(15)의 LER(line edge roughness)로 인해 균일한 면적의 콘택 플러그 영역을 확보하는데 어려움이 있다.

[0019] 둘째, 슬리밍 공정을 수행하는 과정에서 포토레지스트 패턴(15)의 두께(D) 및 폭(W) 조절이 용이하지 않다. 포토레지스트 패턴(15)은 식각 공정을 반복 수행하는 과정에서 식각 베리어로서의 역할을 충실히 수행하기 위해 충분한 두께로 형성되어야함과 동시에, 폭을 일정 값씩 균일하게 감소시키면서 식각 공정을 반복 수행하여야 한다. 따라서, 식각 과정에서의 손실을 감안하여 포토레지스트 패턴(15)의 두께(D)를 증가시킬수록, 폭(W)을 콘트롤하는 것이 어려워지는 문제점이 발생하게 된다.

[0020] 특히, 전술한 바와 같은 문제점은 메모리 소자의 집적도가 향상될수록 더욱 심화된다. 3차원 구조의 비휘발성 메모리 소자의 경우, 기판으로부터 돌출되는 채널을 따라 적층되는 메모리 셀의 개수를 증가시킴으로써 메모리 소자의 집적도를 향상시키게 되는데, 적층되는 메모리 셀의 개수가 증가될수록 슬리밍 공정을 수행함에 있어서 게이트 전극용 도전막(12)의 표면을 노출시키기 위한 식각 공정의 횟수가 더욱 증가하게 된다. 따라서, 메모리 소자의 집적도가 향상될수록 식각 공정 횟수 증가에 따른 문제점이 더욱 심화된다.

발명의 내용

해결 하고자하는 과제

[0021] 본 발명은 상기 문제점을 해결하기 위해 제안된 것으로, 슬리밍 공정 수행시 식각 공정의 반복 횟수를 감소시킬 수 있는 수직채널형 비휘발성 메모리 소자 제조 방법을 제공하는 것을 목적으로 한다.

과제 해결수단

[0022] 상기 목적을 달성하기 위해 제안된 본 발명은 수직채널형 비휘발성 메모리 소자 제조 방법에 있어서, 기판 상에 복수의 층간절연막 및 게이트 전극용 도전막을 교대로 형성하는 단계; 상기 복수의 층간절연막 및 게이트 전극용 도전막이 형성된 결과물 상에, 메모리 셀 영역을 덮는 마스크 패턴을 형성하는 단계; 상기 마스크 패턴을 식각 베리어로 하여, 상기 게이트 전극용 도전막의 표면이 노출되도록 상기 복수의 층간절연막 및 게이트 전극용 도전막을 식각하되, 적어도 2층 이상의 연속으로 적층된 게이트 전극용 도전막을 하나의 단위로 1차식각하는 단계; 상기 1차식각에 의한 식각면 측벽에 스페이서를 형성하는 단계; 및 상기 마스크 패턴 및 스페이서를 식각베리어로 상기 복수의 층간절연막 및 게이트 전극용 도전막을 2차식각하는 단계를 포함하는 것을 일 특징으로 한다.

[0023] 또한, 본 발명은 수직채널형 비휘발성 메모리 소자 제조 방법에 있어서, 기판 상에 복수의 제1물질막 및 제2물질막을 교대로 형성하는 단계; 상기 복수의 제1물질막 및 제2물질막이 형성된 결과물 상에, 메모리 셀 영역을 덮는 마스크 패턴을 형성하는 단계; 상기 마스크 패턴을 식각 베리어로하여 상기 제2물질막의 표면이 노출되도록 복수의 제1물질막 및 제2물질막을 식각하되, 적어도 2층 이상의 연속으로 적층된 제2물질막을 하나의 단위로 1차식각하는 단계; 상기 1차식각에 의한 식각면 측벽에 스페이서를 형성하는 단계; 및 상기 마스크 패턴 및 스페이서를 식각베리어로 상기 복수의 제1물질막 및 제2물질막을 2차식각하는 단계를 포함하는 것을 다른 특징으로 한다.

효 과

[0024] 본 발명에 따르면, 1차식각, 스페이서 형성 및 2차식각 단계로 이루어지는 슬리밍 공정을 수행하는데, 특히, 적어도 2층 이상의 연속으로 적층된 게이트 전극용 도전막을 하나의 단위로 1차식각을 수행함으로써, 슬리밍 공정시 식각 공정의 반복 횟수를 감소시킬 수 있다. 따라서, 식각 공정의 반복에 따른 막 손상을 방지할 수 있으며, 포토레지스트 패턴의 두께 및 폭을 용이하게 조절하여 균일한 면적의 콘택 플러그를 형성할 수 있다.

발명의 실시를 위한 구체적인 내용

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[0025] 이하에서는, 본 발명의 가장 바람직한 실시예가 설명된다. 도면에 있어서, 두께와 간격은 설명의 편의를 위하여 표현된 것이며, 실제 물리적 두께에 비해 과장되어 도시될 수 있다. 본 발명을 설명함에 있어서, 본 발명의 요지와 무관한 공지의 구성은 생략될 수 있다. 각 도면의 구성요소들에 참조 번호를 부가함에 있어서, 동일한 구성 요소들에 한해서는 비록 다른 도면상에 표시되더라도 가능한 한 동일한 번호를 가지도록 하고 있음에 유의하여야 한다.

[0026] 본 발명은 반도체 소자의 슬리밍 공정에 관한 것으로서, 특히, 슬리밍 공정을 1차 식각, 스페이서 형성 및 2차 식각으로 진행하는 방법에 관한 것이다.

[0027] 단, 슬리밍 공정을 수행하기에 앞서, 기판으로부터 돌출된 채널을 따라 적층된 복수의 메모리 셀을 형성하는데, 기판 상에 복수의 제1물질막 및 제2물질막을 형성한 후, 소정 공정들을 통해 메모리 셀들을 형성할 수 있다.

[0028] 여기서, 제1물질막 및 제2물질막은 메모리 셀을 형성하는 방법에 따라 다양한 물질로 이루어질 수 있다. 예를 들어, 제1물질막은 층간절연막일 수 있다. 또한, 제2물질막은 복수의 메모리 셀들의 게이트 전극 형성을 위한 게이트 전극용 도전막이거나, 후속 공정에서 터널절연막, 전하트랩막, 전하차단막 및 콘트롤 게이트 전극의 형성 공간을 확보하기 위한 희생막일 수 있다.

[0029] 이하, 본 발명의 일 실시예로서, 제1물질막이 층간절연막이고, 제2물질막이 게이트 전극용 도전막인 경우의 수직채널형 비휘발성 메모리 소자 제조 방법에 대하여 설명하도록 한다.

[0030] 도 2a 내지 도 2e는 본 발명의 제1 실시예에 따른 수직채널형 비휘발성 메모리 소자의 제조 방법을 설명하기 위한 공정 단면도이다. 제1 실시예에서는 복수의 층간절연막 및 게이트 전극용 도전막을 식각하되, 적어도 2층 이상의 연속으로 적층된 게이트 전극용 도전막을 하나의 단위로 식각하는 경우에 대해 설명하도록 한다.

[0031] 도 2a에 도시된 바와 같이, 기판(20)상에 층간절연막(21) 및 게이트 전극용 도전막(22)을 교대로 형성한 후, 이를 식각하여 기판(20)을 노출시키는 트렌치를 형성한다.

[0032] 이어서, 트렌치의 내벽에 전하차단막, 전하포획막 및 터널절연막(23)을 차례로 형성한 후, 트렌치 내에 채널용 막(24)을 매립한다. 본 도면에서는 설명의 편의를 위하여, 전하차단막, 전하포획막 및 터널절연막을 하나의 막으로 도시하였으며, 도면 부호 "23"으로 표시하였다.

[0033] 이로써, 기판(20)으로부터 수직으로 돌출되는 채널을 따라 적층되는 복수의 메모리 셀들이 형성된다.

[0034] 이어서, 복수의 메모리 셀이 형성된 결과물에 대하여, 콘택 플러그 형성을 위해 복수의 게이트 전극용 도전막(22)의 표면을 각각 노출시키는 슬리밍 공정을 수행한다.

[0035] 도 2b에 도시된 바와 같이, 1차 식각 공정을 수행하기 위해, 메모리 셀이 형성된 결과물 상에 메모리 셀 영역을 덮는 마스크 패턴(25)을 형성한다. 이어서, 마스크 패턴(25)을 식각 베리어로 복수의 층간절연막(21) 및 게이트 전극용 도전막(22)을 식각하는데, 적어도 2층 이상의 연속으로 적층된 게이트 전극용 도전막(22)을 하나의 단위로 식각한다.

[0036] 본 도면에서는 1차식각 공정이 수행되는 한 단위의 층들을 도면 부호 "A"로 표시하였으며, 특히, 2층의 연속으로 적층된 게이트 전극용 도전막(22)을 하나의 단위(A)로 식각하는 경우에 대해 도시하고 있다.

[0037] 여기서, 1차식각 단계는 종래기술에 따른 슬리밍 공정과 마찬가지로 마스크 패턴(25)의 폭을 감소시키면서 소정 횟수 반복하여 식각 공정을 수행하는데, 적어도 2층 이상의 게이트 전극용 도전막(22)을 하나의 단위(A)로 하여 기판(20) 또는 하부 선택 트랜지스터(미도시됨)가 노출될 때까지 소정 횟수 반복하여 식각 공정을 수행하는 것이 바람직하다.

[0038] 즉, 마스크 패턴(25)의 폭을 감소시키면서 복수의 층간절연막(21) 및 게이트 전극용 도전막(22)을 계단형으로 패터닝하여, 연속으로 적층된 적어도 2층의 게이트 전극용 도전막(22)이 하나의 층을 이루는 계단형 구조물을 형성한다.

[0039] 이와 같이 소정 개수 단위(A)로 복수의 층간절연막(21) 및 게이트 전극용 도전막(22)을 식각하는 경우, 1차식각

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단계에 의해, 복수의 게이트 전극용 도전막(22) 중 일부의 표면을 노출시키게 된다.

[0040] 예를 들어, 본 도면에서는 총 7개의 메모리 셀을 적층한 경우에 대해 도시하고 있으며, 설명의 편의를 위하여 기판(20)상에 적층된 순서에 따라 총 7개의 게이트 전극용 도전막을 도면 부호 "①~⑦"로 각각 표시하였다.

[0041] 제1 실시예에서는 연속으로 적층된 2개(①②/③④/⑤⑥/⑦)의 게이트 전극용 도전막(22)을 단위(A)로 하여 1차 식각 공정을 수행함으로써, 4개의 막(층간절연막 포함)으로 하나의 층이 이루어지는 계단형 구조물을 형성한다. 따라서, 기판(20)상에 적층된 총 6개의 게이트 전극용 도전막(22) 중 기판(20)으로부터 두번째(②), 네번째(④), 여섯번째(⑥) 적층된 게이트 전극용 도전막(22)의 표면 즉, 콘택 플러그 예정 영역이 노출된다.

[0042] 여기서, 1차식각에 의해 노출되는 게이트 전극용 도전막(22)의 표면 면적은 한단위로 식각된 게이트 전극용 도전막(22)들의 콘택 플러그 예정 영역을 고려하여 결정되어야 하는데, 적어도 두 개 이상의 콘택플러그 예정 영역의 면적을 합친 값 이상이 되어야 한다. 예를 들어, 1차식각에 의해 노출되는 두번째(②) 게이트 전극용 도전막(22)의 표면 면적은, 두번째(②) 게이트 전극용 도전막(22) 뿐만 아니라 첫번째(①) 게이트 전극용 도전막(22)의 콘택플러그 예정영역을 포함하도록 형성되어야 한다.

[0043] 이와 같은, 제1 실시예에 따르면, 1차 식각은 총 6개의 게이트 전극용 도전막(22) 중 일부인 두번째(②), 네번째(④), 여섯번째(⑥) 게이트 전극용 도전막(22)의 표면을 노출시키도록, 총 3번의 식각 공정으로 이루어지게 된다.

[0044] 도 2c에 도시된 바와 같이, 1차식각에 의한 식각면 측벽에 스페이서(26)를 형성한다.

[0045] 여기서, 스페이서(26)는 2차식각 공정시 마스크 패턴(25)과 함께 식각베리어로서 사용하기 위한 것으로서, 특히, 하나의 단위로 함께 식각된 게이트 전극용 도전막(22)을 식각하여 1차식각 단계에서 노출되지 않은 게이트 전극용 도전막들의 표면을 노출시키기 위한 것이다.

[0046] 스페이서(26)는 1차식각 공정이 수행된 결과물의 전면에 스페이서용 절연막을 형성한 후, 1차식각 공정에 의해 노출된 게이트 전극용 도전막(22)의 표면이 노출될때까지 스페이서용 절연막을 에치백함으로써 형성하는 것이 바람직하다.

[0047] 또한, 스페이서(26)는 층간절연막(21) 및 게이트 전극용 도전막(22)과 식각 선택비가 큰 물질로 이루어지는 것이 바람직하며, 특히, 포토레지스트, 질화막 또는 산화막을 포함하는 것이 더욱 바람직하다.

[0048] 또한, 스페이서(26)의 폭은 콘택 플러그 예정 영역의 폭과 동일한 것이 바람직하다.

[0049] 도 2d에 도시된 바와 같이, 마스크 패턴(25) 및 스페이서(26)를 식각베리어로 복수의 층간절연막(21) 및 게이트 전극용 도전막(22)을 2차식각하여, 복수의 게이트 전극용 도전막(22)을 각각 노출시킨다.

[0050] 본 도면을 참조하면, 스페이서(26)를 식각베리어로 두번째(②), 네번째(④), 여섯번째(⑥) 게이트 전극용 도전막(22) 및 층간절연막(21)을 식각함으로써, 첫번째(①), 세번째(③), 다섯번째(⑤) 게이트 전극용 도전막(22)의 표면 즉, 콘택 플러그 예정 영역을 노출시키게 된다.

[0051] 이와 같은, 제1 실시예에 따르면, 2차 식각은 한번의 식각 공정으로 이루어지며, 이로써, 복수의 게이트 전극용 도전막(22)들의 표면 즉, 콘택 플러그 예정 영역이 모두 노출된다.

[0052] 도 2e에 도시된 바와 같이, 복수의 게이트 전극용 도전막(22)들의 표면이 각각 노출된 결과물의 전체 구조상에 층간절연막(27)을 형성한다. 이때, 스페이서(26)가 포토레지스트를 포함하는 경우에는 층간절연막(27)의 형성에 앞서, 스페이서(26)를 제거하는 것이 바람직하다. 본 도면에서는 스페이서(26)를 제거하지 않는 경우에 대해 도시하고 있다.

[0053] 이어서, 층간절연막(27)을 식각하여 복수의 게이트 전극용 도전막(22)의 표면 즉, 복수의 콘택 플러그 예정 영역을 각각 노출시키는 트렌치를 형성한다. 이어서, 트렌치 내에 도전막을 매립하여 콘택 플러그(28)를 형성한다.

[0054] 전술한 바와 같은 본 발명에 따르면, 1차식각 공정 및 2차식각 공정으로 나누어 슬리밍 공정을 수행함으로써, 슬리밍 공정 수행시 반복되는 식각 공정 횟수를 감소시킬 수 있다. 즉, 7개의 메모리 셀을 적층시킨 경우, 종래에는 총 6번의 식각 공정이 수행되는데 비해, 본 발명에 따르면, 총 4번(1차식각시 3번+2차식각시 1번)의 식각 공정으로 슬리밍 공정을 완료할 수 있다. 즉, 슬리밍 공정시 식각 공정의 반복 횟수를 약 50% 감소시킬 수

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있다.

[0055] 따라서, 슬리밍 공정에서의 식각 공정 반복에 따른 막들의 손상을 감소시킬 수 있다. 또한, 종래에 비해 마스크 패턴(25)의 두께를 감소시킬 수 있으므로, 마스크 패턴(25)의 LER에 따른 콘택 플러그 영역 면적의 불균일을 최소화할 수 있다.

[0056] 도 3a 내지 도 3e는 본 발명의 제2 실시예에 따른 수직채널형 비휘발성 메모리 소자의 제조 방법을 설명하기 위한 공정 단면도이다. 제2 실시예에서는 복수의 층간절연막 및 게이트 전극용 도전막을 식각하되, 적어도 4층 이상의 연속으로 적층된 게이트 전극용 도전막을 하나의 단위로 식각하는 경우에 대해 설명하도록 한다. 단, 앞서 제1 실시예에서 설명한 내용과 중복되는 내용은 생략하도록 한다.

[0057] 도 3a에 도시된 바와 같이, 기판(30)으로부터 수직으로 돌출되는 채널을 따라 적층되는 복수의 메모리 셀들을 형성한다. 여기서, 메모리 셀들의 형성 과정은 앞서 제1 실시예에서 설명한 바와 동일하므로, 상세한 설명은 생략하도록 한다.

[0058] 이어서, 메모리 셀이 형성된 결과물 상에 메모리 셀 영역을 덮는 마스크 패턴(35)을 형성한 후, 마스크 패턴(35)을 식각 베리어로 복수의 층간절연막(31) 및 게이트 전극용 도전막(32)을 적어도 4층 이상의 연속으로 적층된 게이트 전극용 도전막을 하나의 단위로 1차식각한다. 본 도면에서는 1차식각 공정이 수행되는 하나의 단위를 도면 부호 "B"로 표시하였다.

[0059] 특히, 연속으로 적층된 4층의 게이트 전극용 도전막(32)을 하나의 단위(B)로 식각하는 경우를 나타낸다. 즉, 연속으로 적층된 4개(①②③④/⑤⑥⑦⑧/⑨⑩)의 게이트 전극용 도전막(32)이 하나의 층을 이루도록 1차식각 공정을 수행한다.

[0060] 이와 같은 1차식각 공정에 의해, 기판(30)상에 적층된 총 10개의 게이트 전극용 도전막(32) 중 기판(30)으로부터 네번째(④), 여덟번째(⑧) 적층된 게이트 전극용 도전막(32)의 표면 즉, 콘택 플러그 예정 영역이 노출된다.

[0061] 여기서, 1차식각에 의해 노출되는 게이트 전극용 도전막(32)의 표면 면적은 하나의 단위(B)로 식각된 게이트 전극용 도전막(32)들의 콘택 플러그 예정 영역을 고려하여 결정되어야 한다. 예를 들어, 1차식각에 의해 노출되는 네번째(④) 게이트 전극용 도전막(32)의 표면 면적은, 네번째(④) 게이트 전극용 도전막(32) 뿐만 아니라 첫번째(①), 두번째(②), 세번째(③) 게이트 전극용 도전막(32)의 콘택플러그 예정영역을 포함하도록 형성되어야 한다.

[0062] 이와 같은, 제2 실시예에 따르면, 1차 식각은 총 10개의 게이트 전극용 도전막(32) 중 일부인 네번째(④), 여덟번째(⑧) 게이트 전극용 도전막(32)의 표면을 노출시키도록, 총 2번의 식각 공정으로 이루어지게 된다.

[0063] 도 3b에 도시된 바와 같이, 1차식각에 의한 식각면 측벽에 제1스페이서(36)를 형성한 후, 마스크 패턴(35) 및 제1스페이서(36)를 식각베리어로 복수의 층간절연막(31) 및 게이트 전극용 도전막(32)을 2차식각한다.

[0064] 단, 1차식각 단계에서 연속으로 증착된 4층 이상의 게이트 전극용 도전막(32)을 한 단위로 식각한 경우, 2차식각 단계는 1차식각 단계와 마찬가지로 적어도 2층 이상의 연속으로 적층된 게이트 전극용 도전막을 하나의 단위(C)로 식각한다.

[0065] 본 도면을 참조하면, 1차식각 단계에서 연속으로 적층된 4층의 게이트 전극용 도전막(32)을 하나의 단위(B)로 식각 공정을 수행하였으므로, 2차식각 단계에서는 연속으로 적층된 2층의 게이트 전극용 도전막(32)을 하나의 단위(C)로 식각 공정을 수행하는 것이 바람직하다. 즉, 제1스페이서(36)를 식각 베리어로 세번째(③), 네번째(④), 일곱번째(⑦), 여덟번째(⑧) 게이트 전극용 도전막 및 층간절연막(31)을 식각함으로써, 두번째(②), 여섯번째(⑥) 게이트 전극용 도전막(32)의 표면을 추가로 노출시킨다.

[0066] 여기서, 적어도 2층 이상의 연속으로 적층된 게이트 전극용 도전막(32)을 하나의 단위(C)로 2차식각하는 경우, 제1스페이서(36)의 폭은 상기 식각 단위(C)를 고려하여 결정되는 것이 바람직하다. 본 도면을 참조하면, 연속으로 적층된 2층의 게이트 전극용 도전막(32)을 하나의 단위(C)로 2차식각을 수행하므로, 제1스페이서의 폭은 2개의 콘택 플러그 예정영역 면적과 동일한 값을 갖는 것이 바람직하다.

[0067] 이와 같은 스페이서 형성 및 2차식각 단계는 복수의 게이트 전극용 도전막(32)의 표면이 전부 노출될 때까지 반복적으로 수행된다.

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[0068] 도 3c에 도시된 바와 같이, 제1스페이서(36)를 제거한 후, 2차식각에 의한 식각면 측벽에 제2스페이서(37)를 형성한다. 여기서, 제2스페이서(37)는 콘택 플러그 예정 영역을 덮는 두께로 형성되는 것이 바람직하다.

[0069] 또한, 10번째(⑩) 게이트 전극용 도전막(32) 및 층간절연막(31)을 식각하기 위하여 마스크 패턴(35A)의 폭을 일정 값 감소시키는 것이 바람직하다. 즉, 스페이스 형성 및 2차식각 단계를 반복하여 수행하는 경우, 마스크 패턴(35A)의 폭을 점차 감소시키면서 2차식각 단계를 반복 수행하는 것이 바람직하다.

[0070] 도 3d에 도시된 바와 같이, 마스크 패턴(35A) 및 제2스페이서(37)를 식각베리어로 층간절연막(31) 및 게이트 전극용 도전막(32)을 식각한다.

[0071] 이와 같은, 제2 실시예에 따르면, 스페이서 형성 및 2차 식각 공정이 두번 반복 수행되며, 이로써, 복수의 게이트 전극용 도전막(32)들의 표면 즉, 콘택 플러그 예정 영역이 모두 노출된다.

[0072] 도 3e에 도시된 바와 같이, 복수의 게이트 전극용 도전막(32)들의 표면이 각각 노출된 결과물의 전체 구조상에 층간절연막(37)을 형성한다. 이어서, 층간절연막(37)을 식각하여 복수의 게이트 전극용 도전막(32)의 표면 즉, 복수의 콘택 플러그 예정 영역을 각각 노출시키는 트렌치를 형성한다. 이어서, 트렌치 내에 도전막을 매립하여 콘택 플러그(38)를 형성한다.

[0073] 전술한 바와 같은 본 발명의 제2 실시예에 따르면, 10개의 메모리 셀을 적층시킨 경우, 총 4번(1차식각시 2번+2차식각 2번 반복)의 식각 공정으로 슬리밍 공정을 완료할 수 있다. 즉, 총 9번의 식각 공정이 요구되는 종래의 슬리밍 공정 기술에 비해, 식각 공정의 반복 횟수를 약 50% 감소시킬 수 있다.

[0074] 본 명세서에서는 수직채널형 비휘발성 메모리 소자 제조 방법에 있어서, 기판상에 복수의 층간절연막 및 게이트 전극용 도전막을 형성한 후, 후속 공정들에 의해 기판으로부터 돌출된 채널을 따라 적층된 복수의 메모리 셀들을 형성하는 방법에 대해 설명하고 있으나, 이는 설명의 편의를 위한 것일 뿐, 본 발명이 이에 한정되는 것은 아니다.

[0075] 본 발명은 슬리밍 공정이 요구되는 모든 반도체 소자 제조 방법에 적용이 가능하다. 예를 들어, 기판상에 메모리 셀을 적층하는 3차원 구조의 비휘발성 메모리 소자 제조 방법에 적용이 가능한데, 이를 보다 상세히 살펴보면 다음과 같다.

[0076] 먼저, 기판상에 복수의 층간절연막 및 희생막을 교대로 형성한 후, 복수의 층간절연막 및 희생막을 식각하여 기판을 노출시키는 트렌치를 형성한다. 이어서, 트렌치 내에 채널용 막을 매립하여 채널을 형성한다. 이어서, 희생막만을 선택적으로 제거한 후, 희생막이 제거된 영역 내에 터널절연막, 전하트랩막, 전하차단막 및 게이트 전극용 도전막을 차례로 형성함으로써, 채널을 따라 적층된 복수의 메모리 셀을 형성한다.

[0077] 이어서, 복수의 층간절연막 및 게이트 전극용 도전막을 식각하여, 복수의 게이트 전극용 도전막의 표면을 노출시키도록 슬리밍 공정을 수행하는데, 이와같은 슬리밍 공정 수행시 본 발명의 적용이 가능하다.

[0078] 이어서, 콘택 플러그를 형성하는 등의 공정이 수행된다.

[0079] 본 발명의 기술 사상은 상기 바람직한 실시예들에 따라 구체적으로 기록되었으나, 상기한 실시예는 그 설명을 위한 것이며 그 제한을 위한 것이 아님을 주의하여야 한다. 또한, 본 발명의 기술 분야의 통상의 전문가라면 본 발명의 기술 사상의 범위내에서 다양한 실시예가 가능함을 이해할 수 있을 것이다.

도면의 간단한 설명

[0080] 도 1a 내지 도 1e는 종래기술에 따른 수직채널형 비휘발성 메모리 소자 제조 방법을 설명하기 위한 공정 단면도.

[0081] 도 2a 내지 도 2e는 본 발명의 제1 실시예에 따른 수직채널형 비휘발성 메모리 소자 제조 방법을 설명하기 위한 공정 단면도.

[0082] 도 3a 내지 도 3e는 본 발명의 제2 실시예에 따른 수직채널형 비휘발성 메모리 소자 제조 방법을 설명하기 위

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한 공정 단면도.

[0083] [도면의 주요 부분에 대한 부호의 설명]

[0084] 20: 기판 21: 층간절연막

[0085] 22: 게이트 전극용 도전막 23: 전하차단막, 전하포획막 및 터널절연막

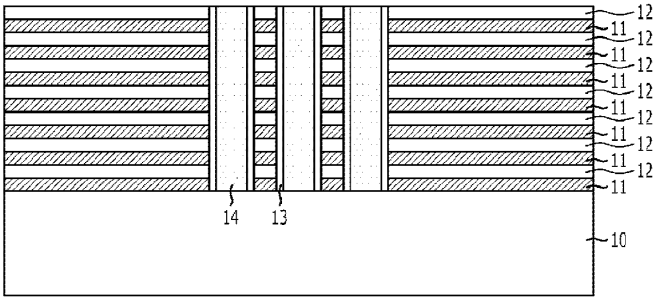
[0086] 24: 채널 25: 마스크 패턴

[0087] 26: 스페이서 27: 층간절연막

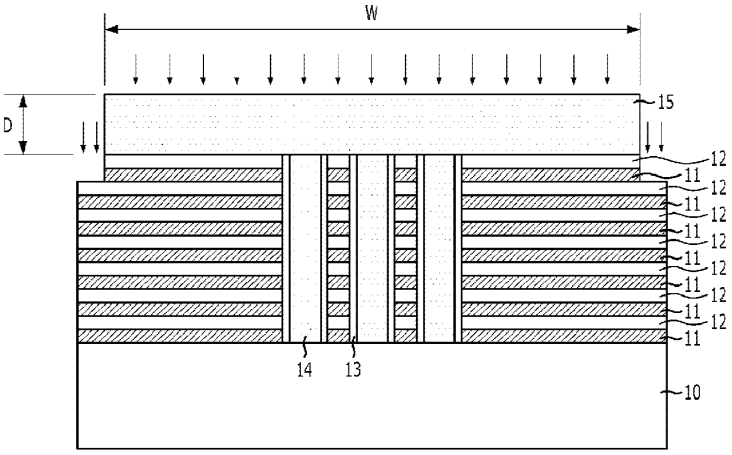
[0088] 28: 콘택 플러그

도면

도면1a

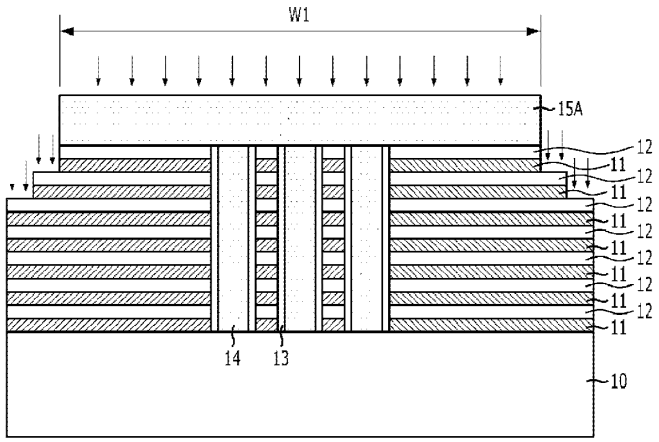


도면1b

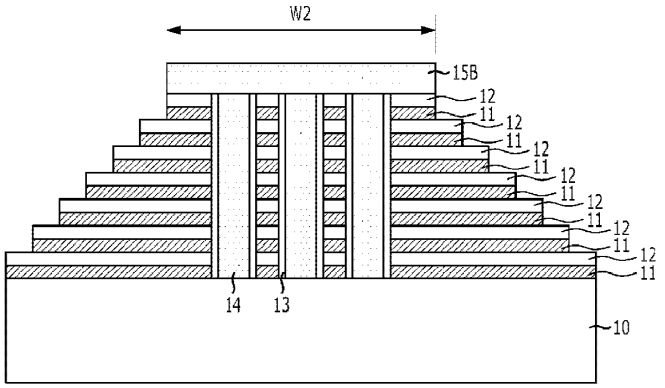


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도면1c

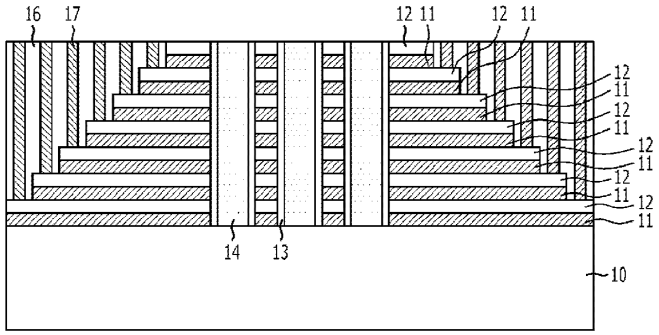


도면1d

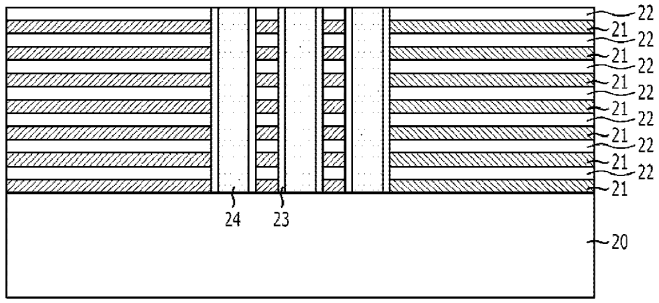


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Micron v. YMTC
PGR2025-00021

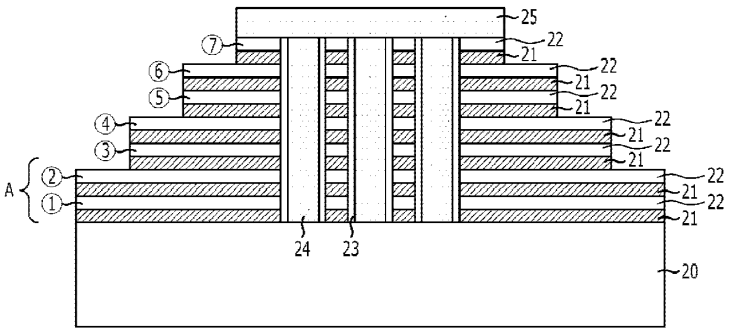
도면1e



도면2a

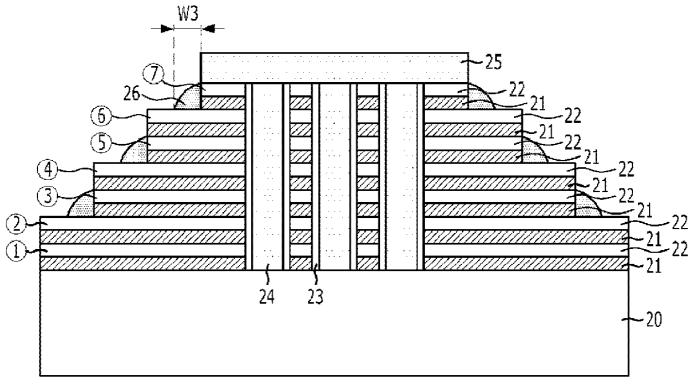


도면2b

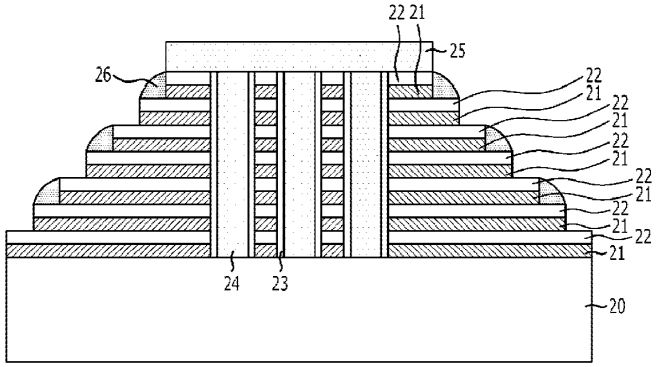


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Micron v. YMTC
PGR2025-00021

도면2c

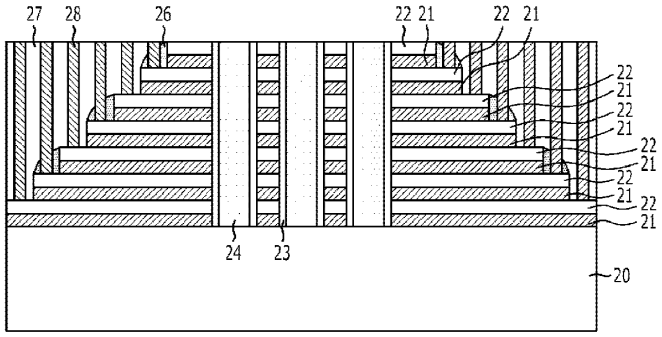


도면2d

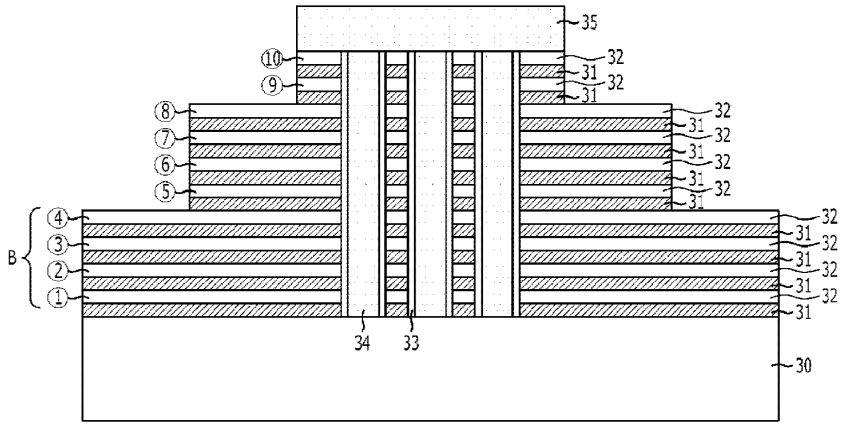


Micron Ex. 1019, p. 166
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도면2e

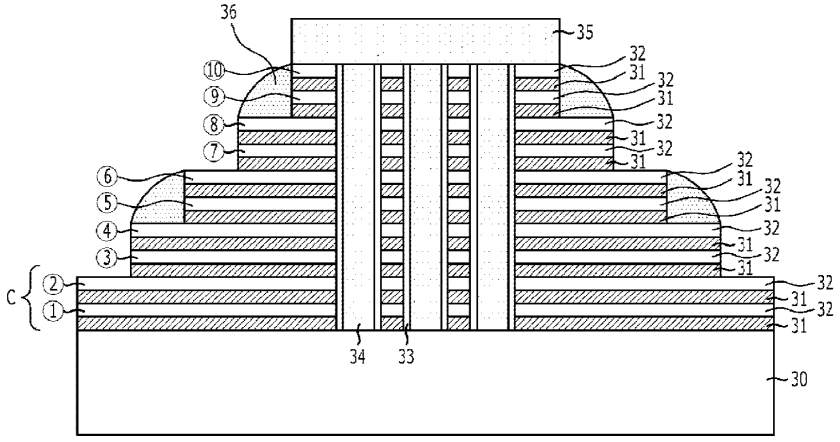


도면3a

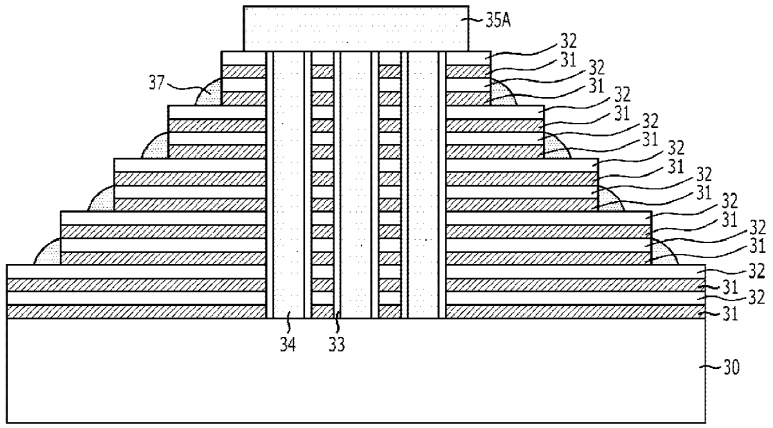


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도면3b

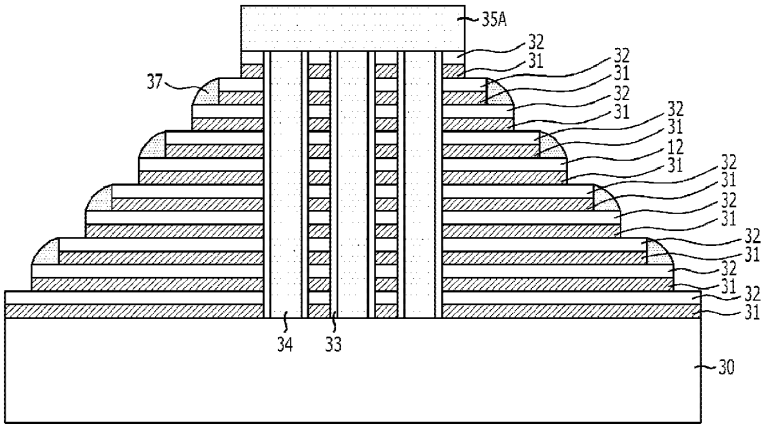


도면3c

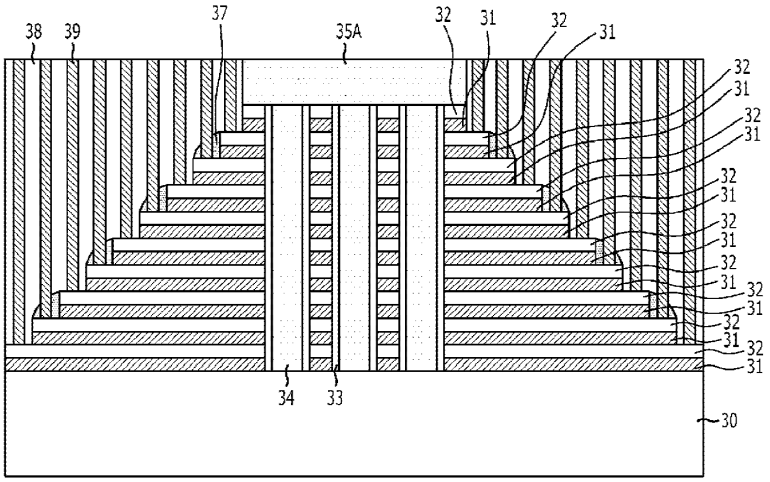


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도면3d



도면3e



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PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference **P2018TC556**	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. **PCT/CN2018/098962**	International filing date *(day/month/year)* **06 August 2018**	(Earliest) Priority Date *(day/month/year)* **28 August 2017**
Applicant **Yangtze Memory Technologies Co., Ltd.**		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of **4** sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of:

   ☑ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

   ☑ the text is approved as submitted by the applicant.

   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

   ☐ the text is approved as submitted by the applicant.

   ☑ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

   a. the figure of the **drawings** to be published with the abstract is Figure No. **8**

   ☑ as suggested by the applicant.

   ☐ as selected by this Authority, because the applicant failed to suggest a figure.

   ☐ as selected by this Authority, because this figure better characterizes the invention.

   b. ☐ none of the figures is to be published with the abstract.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2018/098962

Box No. IV Text of the abstract (Continuation of item 5 of the first sheet)

A semiconductor structure is disclosed. The semiconductor structure includes a staircase structure (800) disposed over a substrate (101). The staircase structure (800) includes a plurality of layer stacks, where each layer stack is made of a first material layer (502) over a portion of a second material layer (840). The staircase structure (800) further includes a plurality of landing pads (820), where each landing pad (820) is disposed over another portion of the second material layer (840) of a respective layer stack.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2018/098962

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/11551(2017.01)i; H01L 27/11578(2017.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,WPI,EPODOC,CNKI,IEEE:memory,storage,3D,vertical,stack,step,stair,staircase,stagger,pad,recess

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2015255385 A1 (SK HYNIX INC.) 10 September 2015 (2015-09-10) description, paragraphs [0022]-[0115], figures 1A-9	1-10,14-20
X	KR 20110015338 A (HYNIX SEMICONDUCTOR INC.) 15 February 2011 (2011-02-15) description, paragraphs [0025]-[0055], figures 2a-2e	1-9,14-20
PX	CN 107644876 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 30 January 2018 (2018-01-30) description, paragraphs [0037]-[0068], figures 1-10	1-20
A	CN 106601746 A (SAMSUNG ELECTRONICS CO., LTD.) 26 April 2017 (2017-04-26) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 October 2018	**07 November 2018**

Name and mailing address of the ISA/CN	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088** **China**	**HUANG,Lina**
Facsimile No. **(86-10)62019451**	Telephone No. **86-(10)-53961458**

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2018/098962

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2015255385 A1	10 September 2015	US 9356038 B2	31 May 2016
		KR 20150104817 A	16 September 2015
KR 20110015338 A	15 February 2011	None	
CN 107644876 A	30 January 2018	None	
CN 106601746 A	26 April 2017	US 9419013 B1	16 August 2016
		KR 20170042449 A	19 April 2017

Form PCT/ISA/210 (patent family annex) (January 2015)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
100013
China 10th Floor, Tower C, Beijing Global Trade Center, 36 North Third Ring Road East, Dongcheng District, Beijing

NTD UNIVATION INTELLECTUAL PROPERTY AGENCY LTD.

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	**07 November 2018**
Applicant's or agent's file reference	**FOR FURTHER ACTION** See paragraph 2 below
P2018TC556	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CN2018/098962	**06 August 2018**	**28 August 2017**

International Patent Classification (IPC) or both national classification and IPC
H01L 27/11551(2017.01)i; H01L 27/11578(2017.01)i

Applicant
Yangtze Memory Technologies Co., Ltd.

1. This opinion contains indications relating to the following items:
   - ☑ Box No. I Basis of the opinion
   - ☑ Box No. II Priority
   - ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - ☐ Box No. IV Lack of unity of invention
   - ☑ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
   - ☐ Box No. VI Certain documents cited
   - ☐ Box No. VII Certain defects in the international application
   - ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

   If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

   If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

   For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/	Date of completion of this opinion	Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA **China 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088**	**01 November 2018**	**HUANG,Lina**
Facsimile No. **(86—10) 62019451**		Telephone No. **86-(10)-53961458**

Form PCT/ISA/237 (Cover sheet) (January 2015)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2018/098962

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:
   - [✓] the international application in the language in which it was filed.
   - [ ] a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a)).

3. [ ] With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:
   - a. [ ] forming part of the international application as filed:
     - [ ] in the form of an Annex C/ST.25 text file.
     - [ ] on paper or in the form of an image file.
   - b. [ ] furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
   - c. [ ] furnished subsequent to the international filing date for the purposes of international search only:
     - [ ] in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
     - [ ] on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. [ ] In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
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Box No. II Priority

1. ☐ The validity of the priority claim has not been considered because the International Searching Authority does not have in its possession a copy of the earlier application whose priority has been claimed or, where required, a translation of that earlier application. This opinion has nevertheless been established on the assumption that the relevant date (Rules 43*bis*.1 and 64.1) is the claimed priority date.

2. ☐ This opinion has been established as if no priority had been claimed due to the fact that the priority claim has been found invalid (Rules 43*bis*.1 and 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. Additional observations, if necessary:

[1] The priority of the application is valid after verified.

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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

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PCT/CN2018/098962

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	None	NO
Inventive step (IS)	Claims	11-13	YES
	Claims	1-10, 14-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	None	NO

2. Citations and explanations :

[1] Cited document

[2] D1: US2015255385A1, 10 Sep. 2015

[3] I. Novelty and Inventive step

[4] D1 discloses a memory device, a semiconductor structure and a method for forming the semiconductor structure(see description, paragraphs [0022]-[0115], figures 1A-9): the semiconductor structure comprises a staircase structure, wherein the staircase structure comprises: a plurality of layer stacks ST, each layer stack comprising a first material layer 12 disposed over a first portion 11A of a second material layer 11; and a plurality of landing pads A respectively disposed on the plurality of layer stacks ST, each landing pad A disposed over a second portion 11B of the second material layer 11 of a respective layer stack; the memory device comprises a memory string and a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises: a plurality of layer stacks ST, each layer stack comprising an insulating layer 12 disposed over a first portion 11A of a conductive layer 11, wherein a second portion 11B of the conductive layer 11 is in contact with a side surface of the insulating layer 12; the method comprises: forming a plurality of layer stacks ST, wherein each layer stack comprises a first material layer 22 disposed over a second material layer 21; forming a staircase structure on the plurality of layer stacks ST to expose a portion of the first material layer 22 of each layer stack; forming a landing pad over a portion of the second material layer 21 of the each layer stack.

[5] The difference between claim 1 and D1 is that: the staircase structure is disposed over a substrate.

[6] The differences between claim 9 and D1 are that: forming the layer stacks over a substrate; forming a hard mask layer over the plurality of layer stacks and finally removing the portion of the hard mask layer.

[7] The difference between claim 18 and D1 is that: the memory string is disposed over a substrate.

[8] Therefore, claims 1,9,18 are new in the sense of PCT Article 33(2). Claims 2-8,10-17,19-20 are respectively dependent on claims 1,9,18 directly or indirectly and as such also meet the requirement of PCT Article 33(2).

[9] However, the above differences come within the scope of the customary practice followed by a person skilled in the art. Therefore, claims 1,9,18 do not involve an inventive step in the sense of PCT Article 33(3).

[10] As for claims 2-8,10-17,19-20, the additional features of claims 2-5,7-8,10,19-20 are disclosed by D1(see description, paragraphs [0022]-[0115], figures 1A-9), the additional features of claims 6,14-17 are not disclosed by D1 but come within the scope of the customary practice followed by a person skilled in the art, the additional features of claims 11-13 are not disclosed by D1 and are neither indicated nor obviously rendered from the available prior art. Hence, claims 2-8,10,14-17,19-20 do not involve an inventive step in the sense of PCT Article 33(3), and claims 11-13 involve an inventive step in the sense of PCT Article 33(3).

[11] II. Industrial applicability

[12] The technical solutions of claims 1-20 are industrially applicable in the technical field of memory technology, and thus said claims meet the criteria set out in PCT Article 33(4).

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PGR2025-00021

Electronic Acknowledgement Receipt

EFS ID:	36220343
Application Number:	16126956
International Application Number:	
Confirmation Number:	3036
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Customer Number:	26111
Filer:	Donald J. Featherstone/Tonyia Skinner
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0460002
Receipt Date:	06-JUN-2019
Filing Date:	10-SEP-2018
Time Stamp:	15:15:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2019-06-06-Cover-Letter-4123-0460002.pdf	293971 498ab2136bd3e3d67bfaf3c7f3de460de6497261	no	1
Warnings:					

Information:					
2	Transmittal Letter	2019-06-06-IDS-Pleading-4123-0460002.pdf	145731 bf3093c8cb7bb9ccccbc41683efd421a8aef5fea	no	6
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	2019-06-06-IDS-Form-SB08A-4123-0460002.PDF	260011 156f6286848ecf9926f4a4433801e048ae9b1245	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
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Warnings:					
Information:					
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5	Foreign Reference	FP1_CN106601746A.PDF	3517109 bee060e8236f9240787ce18519fe7f6f6e45bf23	no	47
Warnings:					
Information:					
6	Foreign Reference	FP2_CN107644876A.PDF	631801 f90f7b05d875f4b7e386320db7ec7d2a2ffce39f	no	9
Warnings:					
Information:					
7	Foreign Reference	FP3_KR20110015338A.PDF	815267 8b3903074ae9e58e0c0cda91a7558c6881af1e72	no	19
Warnings:					
Information:					
8	Non Patent Literature	NPL1_ISRWO.PDF	311325 6412ef3fdeff5c944826dcb8752e57143e693a80	no	8
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Information:	
Total Files Size (in bytes):	6207306

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Sterne Kessler
STERNE KESSLER GOLDSTEIN & FOX

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

June 6, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 3036
Art Unit 2811
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 16/126,956; Filing Date: September 10, 2018
For: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**
Inventors: LU *et al.*
Our Ref: 4123.0460002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Information Disclosure Statement;

2. Form PTO/SB/08a (1 sheet) listing 6 documents (**US1-US3** and **FP1-FP3**);

3. Form PTO/SB/08b (1 sheet) listing 1 document (**NPL1**); and

4. Copies of cited documents (**FP1-FP3** and **NPL1**).

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/KTS/jcb
Enclosures

13277886_1.docx

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PGR2025-00021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: LU *et al.*	Confirmation No.: 3036
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: 2811
Application No.: 16/126,956	Examiner: GURLEY, LYNNE ANN
Filing Date: September 10, 2018	Atty. Docket: 4123.0460002

Title: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**

Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Forms PTO/SB/08a equivalent and PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart[1] foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action

---

[1] The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

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after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of $240.00 in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or

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Micron v. YMTC
PGR2025-00021

Notice of Allowance, but on or before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of $240.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or

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other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).

☒ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **US2** (2019/0081070 A1) is submitted herewith as the English-language counterpart of document **FP2** (CN 107644876 A).

Document **US3** (9,419,013 B1) is submitted herewith as the English-language counterpart of document **FP1** (CN 106601746 A).

☒ 8. Copies of documents **FP1-FP3** and **NPL1** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of the U.S. patent and patent application publications cited as documents **US1-US3** on the attached IDS Form are submitted.

☐ 9. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☐ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No(s). _____ in accordance with MPEP 2001.06(b), and

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indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

☐ 11. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No._____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: June 6, 2019

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

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Atty. Dkt. No. 4123.0460002

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4123.0460002
	Application Number	16/126,956
Title of Invention	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201710750398.4	CN	2017-08-28	38A6

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Donald J. Featherstone/			**Date (YYYY-MM-DD)**	2019-08-07
First Name	Donald	**Last Name**	Featherstone	**Registration Number**	33,876

13539000_1.docx

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Micron v. YMTC
PGR2025-00021

Electronic Acknowledgement Receipt

EFS ID:	36806939
Application Number:	16126956
International Application Number:	
Confirmation Number:	3036
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Customer Number:	26111
Filer:	Donald J. Featherstone/Kim Perry
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0460002
Receipt Date:	07-AUG-2019
Filing Date:	10-SEP-2018
Time Stamp:	17:58:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2019-08-07-Corrected-ADS-4123-0460002.pdf	104603 c405ae713afe5abff353c99022f51aa52208fdb0	no	1

Warnings:

Information:	
This is not an USPTO supplied ADS fillable form	
Total Files Size (in bytes):	104603

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,956	09/10/2018	Zhenyu LU	4123.0460002	3036

26111 7590 09/18/2019

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
GEYER, SCOTT B	

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
09/18/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

Micron Ex. 1019, p. 191
Micron v. YMTC
PGR2025-00021

Office Action Summary	Application No. 16/126,956	Applicant(s) LU et al.	
	Examiner Scott B Geyer	Art Unit 2812	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 07 August 2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☐ Claim(s) _____ is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☑ Claim(s) 1-20 are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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PGR2025-00021

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-8 and 18-20, drawn to a device, classified in H01L 27/105+.

II. Claims 9-17, drawn to a method, classified in H01L 21/027+.

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the process as claimed can be used to make another and materially different product since the process requires formation of a recess within each layer stack whereas the product claims do not require this feature.

Restriction for examination purposes as indicated is proper because all the inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because one or more of the following reasons apply: the inventions require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search strategies or search queries).

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement

may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer (telephone: 571-272-1958). The examiner can normally be reached on Monday to Friday, 10AM - 4PM. Examiner interviews are available via telephone, in-person, and video conferencing using a

USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at: http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles D Garber (telephone: 571-272-2194). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in U.S.A. or Canada) or 571-272-1000.

/SCOTT B GEYER/
Primary Examiner, Art Unit 2812

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: LU *et al.*	Confirmation No.: 3036
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: 2812
Application No.: 16/126,956	Examiner: Geyer, Scott B.
Filing Date: September 10, 2018	Atty. Docket: 4123.0460002

Title: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**

Reply to Restriction Requirement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the office action dated September 18, 2019, requesting an election of one group of claims to prosecute in the above-referenced patent application, Applicant hereby provisionally elects to prosecute Group I, represented by claims 1-8 and 18-20. This election is made without prejudice to or disclaimer of the other claims or inventions disclosed.

This election is made without traverse.

Reconsideration and withdrawal of the Restriction Requirement, and consideration and allowance of all pending claims, are respectfully requested.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue

prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: October 2, 2019

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Micron Ex. 1019, p. 197
Micron v. YMTC
PGR2025-00021

Electronic Acknowledgement Receipt

EFS ID:	37342442
Application Number:	16126956
International Application Number:	
Confirmation Number:	3036
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Customer Number:	26111
Filer:	Donald J. Featherstone/Maya Bennett
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0460002
Receipt Date:	02-OCT-2019
Filing Date:	10-SEP-2018
Time Stamp:	12:52:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2019-10-02-Cover-Letter-4123-0460002.PDF	211158 716ce1cc12f9db97f917cd90f1cefe2ec1bda1b5	no	1
Warnings:					

Information:					
2	Response to Election / Restriction Filed	2019-10-02-Reply-Restriction-Requirement-4123-0460002.PDF	83889 a2771ac2609a1f43618b2094c1ce79568dc27b10	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	295047	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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October 2, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 3036

Re: U.S. Utility Patent Application
Appl. No. 16/126,956; Filed: September 10, 2018
For: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**
Inventors: LU *et al.*
Our Ref: 4123.0460002

Commissioner:

Transmitted herewith for appropriate action is a ***Reply to Restriction Requirement***, which is submitted electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/mlb
Enclosure

13927048_1.docx

Micron Ex. 1019, p. 200
Micron v. YMTC
PGR2025-00021

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,956	09/10/2018	Zhenyu LU	4123.0460002	3036

26111 7590 10/22/2019

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
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EXAMINER	
GEYER, SCOTT B	

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
10/22/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

Micron Ex. 1019, p. 201
Micron v. YMTC
PGR2025-00021

Office Action Summary	Application No. 16/126,956	Applicant(s) LU et al.	
	Examiner Scott B Geyer	Art Unit 2812	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 02 October 2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) 9-17 is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-7 and 18-20 is/are rejected.

8) ☑ Claim(s) 8 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 10 September 2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☑ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 20190606 (2 documents).

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-8 and 18-20 in the reply filed on October 2, 2019 is acknowledged.

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in China on August 28, 2017. It is noted, however, that applicant has not filed a certified copy of the foreign priority application as required by 37 CFR 1.55.

Information Disclosure Statement

The references cited within the IDS documents submitted on June 6, 2019 (two documents) have been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claims 1-7 and 18-20 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Hyun (US 9,373,540 B2).

As to **claim 1**, Hyun teaches a semiconductor structure in figure 2H (see also figures 2A-2G). The semiconductor structure of Hyun has:

a substrate (not shown, see column 5, lines 17-30); and

a staircase structure (see figure 2H) disposed over the substrate, wherein the staircase structure comprises:

a plurality of layer stacks (203/235), each layer stack comprising a first material layer (203) disposed over a first portion of a second material layer (235, which is 231+233); and

a plurality of landing pads (217P) respectively disposed on the plurality of layer stacks, each landing pad disposed over a second portion of the second material layer (235) of a respective layer stack.

As to **claim 2**, Hyun teaches each of the plurality of landing pads (217P) is adjacent to a respective side of the first material layer (203). See figure 2H.

As to **claim 3**, Hyun teaches each of the plurality of landing pads (217P) extends over a respective top surface of the second material layer (235).

As to **claim 4**, Hyun teaches the first material layer (203) comprises an insulating material, the second material layer (235) comprises a first conductive material, and each of the plurality of landing pads (217P) comprises a second conductive material.

As to **claim 5**, Hyun teaches the first conductive material is the same as or different from the second conductive material. First conductive material can be tungsten (see column 7, lines 64-65) and second conductive material can be tungsten as well (see column 6, lines 50-52). See also figures 2C and 2G.

As to **claim 6**, Hyun teaches the insulating material can be silicon oxide (column 5, lines 31-45) and each of the first and the second conductive material layers comprises tungsten (column 7, lines 64-65; column 6, lines 50-52).

As to **claim 7**, Hyun teaches the second material layer (235) of each layer stack is disposed over a portion of the first material layer (203) of an adjacent layer stack. See also figure 2H.

As to **claim 18**, Hyun teaches a memory device in figure 2H (see also figures 2A-2G). The memory device of Hyun has:

a substrate (not shown, see column 5, lines 17-30); and

a memory string (see also figure 1) disposed over the substrate; and

a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:

a plurality of layer stacks (see figure 2H), each layer stack comprising an insulating layer (203) disposed over a first portion of a conductive layer (235/231+233), wherein a second portion of the conductive layer (217P) is in contact with a side surface of the insulating layer (see figure 2H).

As to **claim 19**, Hyun teaches the conductive layer of each layer stack is disposed over a portion of the insulating layer of an adjacent layer stack. See figure 2H.

As to **claim 20**, Hyun teaches the second portion of the conductive layer is thicker than the first portion of the conductive material layer. Regarding figure 2H, the "second portion" is the area of the conductive 'track' that includes 217P, the landing

pad. The overall thickness of 217P and 231/233 in this area is thicker than the area to the right side (the "first portion" area), which is only 231/233.

//

//

Claims 1-3 and 7 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Hashimoto (US 2011/0031630 A1).

As to **claim 1**, Hashimoto teaches a semiconductor structure in figure 11B. The semiconductor structure of Hashimoto has:

a substrate (10); and

a staircase structure (see figure 11B) disposed over the substrate, wherein the staircase structure comprises:

a plurality of layer stacks (e.g. WL4/25), each layer stack comprising a first material layer (WL4) disposed over a first portion of a second material layer (25); and

a plurality of landing pads (44) respectively disposed on the plurality of layer stacks, each landing pad disposed over a second portion of the second material layer (25) of a respective layer stack.

As to **claim 2**, Hashimoto teaches each of the plurality of landing pads (44) is adjacent to a respective side of the first material layer (WL4). See figure 11B.

As to **claim 3**, Hashimoto teaches each of the plurality of landing pads (44) extends over a respective top surface of the second material layer (25).

As to **claim 7**, Hashimoto teaches the second material layer (25) of each layer stack is disposed over a portion of the first material layer (e.g. WL4, WL3, WL2) of an adjacent layer stack. See also figure 11B.

Allowable Subject Matter

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: see the attached form PTO-892 for pertinent cited art.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer (telephone: 571-272-1958). The examiner can normally be reached on Monday to Friday, 10AM - 4PM. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at: http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles D Garber (telephone: 571-272-2194). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in U.S.A. or Canada) or 571-272-1000.

/SCOTT B GEYER/
Primary Examiner, Art Unit 2812

Notice of References Cited	Application/Control No. 16/126,956	Applicant(s)/Patent Under Reexamination LU et al.	
	Examiner Scott B Geyer	Art Unit 2812	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20170084532-A1	03-2017	SON; Yong-Hoon	H01L23/5226	1/1
*	B	US-10403641-B2	09-2019	Kim; Sung-Gil	H01L27/11575	1/1
*	C	US-10002880-B1	06-2018	Nagashima; Satoshi	H01L27/11582	1/1
*	D	US-9478487-B2	10-2016	Yang; Byeong-Wan	H01L23/49838	1/1
*	E	US-9373540-B2	06-2016	Hyun; Chan Sun	H01L21/76843	1/1
*	F	US-9343452-B2	05-2016	Yun; Tae-Hwan	H01L27/1157	1/1
*	G	US-9331082-B2	05-2016	Lee; Ki Hong	H01L27/11548	1/1
*	H	US-9006884-B2	04-2015	Lee; Ki Hong	H01L21/7685	257/314
*	I	US-20150255386-A1	09-2015	LEE; JAEGOO	H01L23/5226	257/774
*	J	US-20130270714-A1	10-2013	Lee; Ho-Ki	H01L21/76802	257/774
*	K	US-20110031630-A1	02-2011	HASHIMOTO; Junichi	H01L27/11578	257/774
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Micron Ex. 1019, p. 209
Micron v. YMTC
PGR2025-00021

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/126,956	LU et al.
	Examiner	Art Unit
	Scott B Geyer	2812

CPC - Searched*		
Symbol	Date	Examiner
H01L27/11582, H01L27/1157, H01L27/11575	10/16/2019	SBG
H01L27/11514, H01L27/11521, H01L27/11551, H01L27/11568, H01L27/11578, H01L27/11597	10/16/2019	SBG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Text searches utilizing above-noted CPC areas	10/16/2019	SBG
EAST search notes attached	10/16/2019	SBG

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

Micron Ex. 1019, p. 210
Micron v. YMTC
PGR2025-00021

Receipt date: 06/06/2019

PTO/SB/08b (07-09)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	16/126,956
Filing Date	September 10, 2018
First Named Inventor	Lu et al.
Art Unit	~~2811~~ 2812
Examiner Name	~~GURLEY, LYNNE ANN~~ S. Geyer
Attorney Docket Number	4123.0460002

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/SG/	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/098962, mailed November 7, 2018; 8 pages.	

Examiner Signature	/SCOTT B GEYER/	Date Considered	10/15/2019

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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BIB DATA SHEET

CONFIRMATION NO. 3036

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
16/126,956	09/10/2018 RULE	257	2812	4123.0460002

APPLICANTS

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

INVENTORS

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Li Hong Xiao, Wuhan, CHINA;
A Man Zheng, Wuhan, CHINA;
Kun Bao, Wuhan, CHINA;
Haohao Yang, Wuhan, CHINA;

/SBG/

**** CONTINUING DATA ***************************

This application is a CON of PCT/CN2018/098962 08/06/2018

**** FOREIGN APPLICATIONS ***************************

CHINA 201710750398.4 08/28/2017

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

10/11/2018

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☑ Yes ☐ No	☐ Yes ☑ No	/SCOTT B GEYER/ Examiner's Signature	☐ Initials	CHINA	10	20	3

ADDRESS

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1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005
UNITED STATES

TITLE

STAIRCASE STRUCTURE FOR MEMORY DEVICE

FILING FEE RECEIVED		
1880	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____

BIB (Rev. 05/07).

Receipt date: 06/06/2019

PTO/SB/08a (07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 1

Complete if Known	
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First Named Inventor	Lu et al.
Art Unit	~~2811~~ 2812
Examiner Name	~~GURLEY, LYNNE ANN~~
Attorney Docket Number	4123.0460002

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/SG/	1	US- 2015/0255385 A1	09-10-2015	Lee et al.	
/SG/	2	US- 2019/0081070 A1	03-14-2019	Lu et al.	
/SG/	3	US- 9,419,013 B1	08-16-2016	Lee et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
/SG/	FP1	CN-106601746-A	04-26-2017	SAMSUNG ELECTRONICS CO LT		
/SG/	FP2	CN-107644876-A	01-30-2018	YANGTZE MEMORY TECH CO LT		
/SG/	FP3	KR-20110015338-A	02-15-2011	HYNIX SEMICONDUCTOR INC.		✔

Examiner Signature	/SCOTT B GEYER/	Date Considered	10/15/2019

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	(("9373540") or ("20110031630") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 10:55
L2	1	("9373540").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 11:19
L3	1	2 and string	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/16 12:35
L4	1	("20110031630").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 12:45
L5	11	(("10403641") or ("20170084532") or ("9478487") or ("9373540") or ("20150255386") or ("20110031630") or ("10002880") or ("9343452") or ("20130270714") or ("9006884") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 13:01
S1	47	((Yangtze adj Memory).as. (Zhenyu with LU).in. (Jun with Chen).in. (Xiaowang with Dai).in. (Jifeng with Zhu).in. (Qian with Tao).in. (Yu with Huang).in. (Si with Hu).in. (Lan with Yao).in. (Li with Xiao).in. (Man with Zheng).in. (Kun with Bao).in. (Haohao with Yang).in.) and ((staircase stair-case (stair adj case)) SAME (substrate memory semiconductor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 11:21
S2	770	(H01L27/11582 H01L21/0273 H01L21/31144 H01L27/1157 H01L27/11575).cpc. and ((staircase stair-case (stair adj case)) SAME (substrate memory semiconductor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 11:21
S3	3	(("20150255385") or ("20190081070") or ("9419013")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 11:37
S4	1	(14/465573).APP.	USPAT; USOCR	OR	OFF	2019/10/15 11:40
S5	3	("20080073635" | "20130234232").PN. OR ("9356038").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 11:40
S6	29	("20100207195" | "20120061743" | "20130056818" | "20140162420" | "20140191389" | "20140199815" |	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 11:40

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		"20140225183" | "20140264934" | "20140293703" | "20140306279" | "20140367759" | "20150035065" | "20150064900" | "20150187789" | "20150255468" | "20150263029" | "8728889" | "8822285" | "8828884" | "8871591" | "8928149").PN. OR ("9419013").URPN.				
S7	2123	(staircase stair-case (stair adj case)) SAME memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 12:36
S8	1076	(staircase stair-case (stair adj case)) with memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 12:36
S9	9	("20160336330" | "20170084532" | "20180366453" | "9202780" | "9331082" | "9343452" | "9356038" | "9373540" | "9478487").PN. OR ("10403641").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 12:52
S10	6	("20110031630" | "20130127011" | "20150255386" | "8304348").PN. OR ("9373540").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 12:59
S11	1	(12/709124).APP.	USPAT; USOCR	OR	OFF	2019/10/15 13:02
S12	15	("20070134817" | "20080121953" | "20090317978").PN. OR ("8304348").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 13:02
S13	8	("20120119283" | "20130270714" | "20130334589" | "8304348" | "8395190" | "9006884").PN. OR ("9343452").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 13:09
S14	383	(H01L27/11514 H01L27/11521 H01L27/11551 H01L27/11568 H01L27/11578 H01L27/11597).cpc. and (staircase stair-case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/15 17:17
S15	123	S14 and (stack layer tier) with pad	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/15 17:17
S16	11	(("10403641") or ("20170084532") or ("9478487") or ("9373540") or ("20150255386") or ("20110031630") or ("10002880") or ("9343452") or ("20130270714") or ("9006884") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 17:26
S17	3	(("9373540") or ("20110031630") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 17:39

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10/ 16/ 2019 1:04:03 PM
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PTO/SB/08a (07-09)
Approved for use through 11/30/2020. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	16/126,956
Filing Date	September 10, 2018
First Named Inventor	Zhenyu LU
Art Unit	2812
Examiner Name	GEYER, SCOTT B
Attorney Docket Number	4123.0460002

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 9,741,563 B2	08-22-2017	Xiang et al.	
		US-			
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		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	16126956
Filing Date:	10-Sep-2018
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Filer:	Donald J. Featherstone/Jon Baitlon
Attorney Docket Number:	4123.0460002

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	37597750
Application Number:	16126956
International Application Number:	
Confirmation Number:	3036
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Customer Number:	26111
Filer:	Donald J. Featherstone/Jon Baitlon
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0460002
Receipt Date:	29-OCT-2019
Filing Date:	10-SEP-2018
Time Stamp:	17:59:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$240
RAM confirmation Number	E20190SI00279947
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	4123-0460002-1SIDS-CoverLetter.pdf	234872 d0c261fb295a86eb84d34bdf7fce366b71a41e3b	no	1
Warnings:					
Information:					
2	Transmittal Letter	4123-0460002-1SIDS-Pleading.pdf	115354 bbe436272da4f748eb3e5377b7d2736942ac0784	no	6
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	4123-0460002-1SIDSPTOFormb0008a.pdf	142451 e00f441215cba34dbfb5cdac3c7df113dbb7dda5	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Fee Worksheet (SB06)	fee-info.pdf	30353 c002270737cca19184f10c7461e9d99a00ae9b0e	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	523030		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Sterne Kessler
STERNE KESSLER GOLDSTEIN & FOX

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

October 29, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 3036
Art Unit 2812
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 16/126,956; Filing Date: September 10, 2018
For: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**
Inventors: LU *et al.*
Our Ref: 4123.0460002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Online Credit Card Payment Authorization in the amount of **$240.00** in payment of the fee under 37 C.F.R. § 1.17(p);

2. First Supplemental Information Disclosure Statement;

3. Form PTO/SB/08a (1 sheet) listing 1 document (**US1**);

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/K-S/jcb
Enclosures

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PGR2025-00021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: LU *et al.*	Confirmation No.: 3036
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: 2812
Application No.: 16/126,956	Examiner: GEYER, SCOTT B
Filing Date: September 10, 2018	Atty. Docket: 4123.0460002

Title: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**

First Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Form PTO/SB/08a equivalent is a document that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Form based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart[1] foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.

☐ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

☒ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office

---

[1] The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

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PGR2025-00021

Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☒ c. The required fee is provided through online credit card payment authorization in the amount of **$240.00** in payment of the fee under 37 C.F.R. § 1.17(p).

☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of $240.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

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☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).

☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

☐ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

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☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).

☐ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

☒ 8. In accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copy of the U.S. patent cited as document **US1** on the attached IDS Form is submitted.

☐ 9. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No._____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).

☐ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No(s). _____ in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

☐ 11. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No._____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the

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Micron v. YMTC
PGR2025-00021

present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: October 29, 2019

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
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Micron Ex. 1019, p. 229
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/126,956	Filing Date 09/10/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	01/16/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 13	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/NICOLE LOVE HENSLEY/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: LU *et al.*	Confirmation No.: 3036
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: 2812
Application No.: 16/126,956	Examiner: GEYER, Scott B.
Filing Date: September 10, 2018	Atty. Docket: 4123.0460002

Title: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated October 22, 2019 ("Office Action"), Applicant submits the following Amendment and Remarks.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Doc Code: PD.REQ.RETR
Document Description: Request for USPTO to retrieve priority docs

PTO/SB/38 (12-18)
Approved for use through 12/31/2021. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Request to Retrieve Electronic Priority Application(s)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

COMPLETE IF KNOWN	
Application Number	16/126,956
Filing Date	September 10, 2018
First Named Inventor	Zhenyu LU
Art Unit	2812
Examiner Name	GEYER, Scott B.
Attorney Docket Number	4123.0460002

Pursuant to 37 CFR 1.55(i), the undersigned hereby requests that the USPTO retrieve an electronic copy of each of the following foreign applications for which priority has been claimed under 35 U.S.C. 119(a)-(d) from a foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement. This Request must be submitted:

- within the later of sixteen months from the filing date of the prior foreign application or four months from the actual filing date of an application under 35 U.S.C. 111(a),
- within four months from the later of the date of commencement (37 CFR 1.491(a)) or the date of the initial submission under 35 U.S.C. 371 of an application entering the national stage under 35 U.S.C. 371, or
- with a petition under 37 CFR 1.55(e) or (f).

☐ **OPTION A**

Please retrieve the priority application identified in Column C, a certified copy of which is contained in the EP or JP application identified in Columns A and B:

	A	B			C	
	Code for Participating Office (EP or JP only)	Application containing the non-participating priority application			Non-participating priority application to be retrieved	
		App. No.	Filing Date	Access Code (for JP only)	Country Code	App. No.
1						

■ **OPTION B**

This Request may be used for the infrequent circumstance when a claim for priority to an application filed in a participating foreign intellectual property office was made prior to that foreign intellectual property office becoming a participating foreign intellectual property office.

Please retrieve the priority application identified in Columns A and B:

	A	B		
	Code for Participating Office (e.g., EP) or WIPO DAS Depositing Office (e.g., AU, BR, CN, DK, EA, EE, ES, FI, GB, IB, IN, JP, KR, MA, NL, NZ, SE)	Application to be retrieved		
		App. No.	Filing Date	Access Code (for WIPO DAS Depositing Office)
1	CN	201710750398.4	08-28-2017	38A6
2				

The USPTO will not attempt to retrieve the identified priority application(s) unless an identical claim for foreign priority to the application identified above is made pursuant to 37 CFR 1.55(d) or a petition is granted under 37 CFR 1.55(e) or (f). Applicants are advised to consult Private PAIR (accessed through www.uspto.gov) to assure that the retrieval has been successful. The applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period set forth in 37 CFR 1.55(g)(1).

I hereby declare that I have the authority to grant access to the above-identified foreign application(s).

/Donald J. Featherstone/	1/16/20
Signature	Date
Donald J. Featherstone	(202) 371-2600
Printed or Typed Name	Telephone Number
Attorney for Applicant	33,876
Title	Registration Number, if applicable

This collection of information is required by 37 CFR 1.55(d). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	38314739
Application Number:	16126956
International Application Number:	
Confirmation Number:	3036
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Customer Number:	26111
Filer:	Donald J. Featherstone/Tonyia Skinner
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0460002
Receipt Date:	16-JAN-2020
Filing Date:	10-SEP-2018
Time Stamp:	15:25:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2020-01-16-Cover-Letter-4123-0460002.pdf	299107 82472ca88a895e8c86ab70dbbccfa14220c2fee3	no	1
Warnings:					

Information:					
2		2020-01-16-Amendment-Reply-111-4123-0460002.pdf	304258 bec250cab5b7e6f05866ce9d0b2765a18a64fb98	yes	8
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Applicant Arguments/Remarks Made in an Amendment		5	8	
	Claims		2	4	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
Warnings:					
Information:					
3	Request for USPTO to retrieve priority docs	2020-01-16-Request-Retrieve-Priority-Application-4123-0460002.pdf	240088 bb24537e08a1c61265478f6a9bfcaa6cb949966a	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	843453		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

January 16, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 3036
Art Unit 2812
Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 16/126,956; Filing Date: September 10, 2018
For: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**
Inventors: LU *et al.*
Our Ref: 4123.0460002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Amendment and Reply Under 37 C.F.R. § 1.111; and

2. Request to Retrieve Electronic Priority Application(s) (PTO/SB/38).

The above-listed documents are filed electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/KTS/tas/cms
Enclosures

14152858_1.docx

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Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-8 and 18-22 are pending in the application, with claims 1 and 18 being the independent claims. Claims 1-3, 5, 7, 8, and 18-20 are sought to be amended. New claims 21 and 22 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

The Office Action presents the following rejections:

- Claims 1-7 and 18-20 are rejected under 35 U.S.C. § 102(a)(1) as allegedly being anticipated by U.S. Patent No. US 9,373,540 to Hyun ("Hyun").
- Claims 1-3 and 7 are rejected under 35 U.S.C. § 102(a)(1) as allegedly being anticipated by U.S. Patent Application Publication No. 2011/0031630 to Hashimoto ("Hashimoto").

Applicant respectfully traverses.

Without acquiescing to the propriety of the rejection, independent claims 1 and 18 have been amended to further clarify their distinguishing features. For example, claim 1 has been amended to recite "wherein the each landing pad comprises a first side surface and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface." Independent claim 18 has been amended to include similar distinguishing features. Hyun and Hashimoto do not disclose these distinguishing features.

Hyun discloses a memory device that has a stair structure with alternated interlayer insulating patterns and conductive patterns, and pad patterns connected to the end portions of the respective conductive patterns (Hyun, Abstract). Each of the pad patterns exhibits a straight vertical sidewall between its top surface and the bottom surface. For example, in Fig. 2H of Hyun (illustrated below), the pad pattern 217P (the alleged "the second portion of the conductive layer") only exhibits a straight vertical side surface that connects pad pattern 217's top surface and bottom

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surface. The straight vertical side surface of pad pattern 217P results from an etching process using protective pattern 215P as a top etch mask (Hyun, ¶¶ 7: 15-21.) Therefore, Hyun does not disclose or suggest the above-noted distinguishing features "wherein the each landing pad comprises a first side surface and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface," as recited in claim 1 and similarly in claim 18.

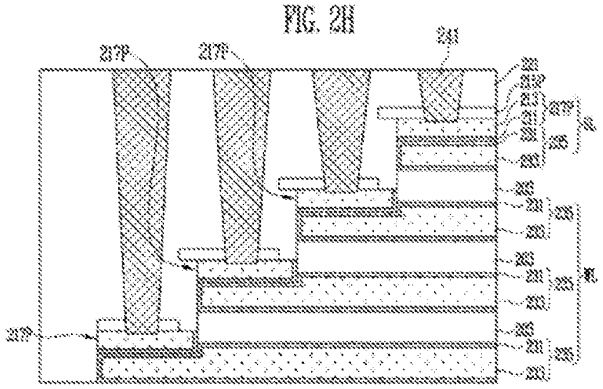


Fig. 2H of Hyun

Hashimoto has similar deficiencies as Hyun. Therefore, Hashimoto does not disclose or suggest the above-noted distinguishing features "wherein the each landing pad comprises a first side surface and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface," as recited in claim 1.

In view of above, independent claims 1 and 18 is patentable over the applied references. At least based on their dependencies from independent claim 1 and 18, claims 2-7, 19, and 20 are patentable over the applied references, in addition to their own distinguishing features. Applicant respectfully requests the Examiner to reconsider and withdraw the rejection under 35 U.S.C. § 102 and to pass claims 1-7 and 18-20 to allowance.

New Claims 21 and 22

Claim 21 depends from independent claim 1, and claim 22 depends from claim 21. Exemplary support for the amendments may be found in at least Fig. 8 and paragraphs [0046]-[0056] of the present application. At least based on their respective dependency from claim 1, claims 21

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and 22 are also patentable over the applied references, in addition to their own distinguishing features.

Applicant respectfully requests that claims 21 and 22 be passed to allowance.

Allowable Subject Matter

The Office Action objects claim 8 as allegedly being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Without acquiescing to the propriety of the rejection, claim 8 has been amended to change its dependency to independent claim 1 for antecedent basis reasons. At least based on its dependency from claim 1, claim 8 is also patentable over the applied references, in addition to its own distinguishing features.

Applicant respectfully requests that claim 8 be passed to allowance.

Priority

The Office Action alleges that this application fails to file a certified copy of the foreign priority application as required by 37 CFR 1.55 (see Office Action, p.2). It is believed that Applicant has authorized the Office to retrieve the certified copy of the foreign priority application upon the filing of this application. To move forward this prosecution, the Applicant hereby encloses the Request to Retrieve Electronic Priority Application form to authorize the Office to retrieve the certified copy of the foreign priority application associated with this application.

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Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 1/16/20

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Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A semiconductor structure, comprising:

a substrate; and

a staircase structure disposed over the substrate, wherein the staircase structure comprises:

a plurality of layer stacks, each layer stack comprising a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of [[a]] the second material layer; and

a plurality of landing pads respectively disposed on the plurality of layer stacks, each landing pad disposed over a second portion of the second material layer of a respective layer stack of the plurality of layer stacks, wherein the each landing pad comprises a first side surface and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface.

2. (Currently Amended) The semiconductor structure of claim 1, wherein each of the plurality of landing pads is adjacent to a ~~respective~~ side surface of the first material layer of the respective layer stack.

3. (Currently Amended) The semiconductor structure of claim 1, wherein a first portion of a landing pad [[each]] of the plurality of landing pads ~~extends over~~ is in contact with ~~a respective top surface of~~ the second material layer of the respective layer stack, and a second portion of the landing pad is laterally displaced from the second material layer of the respective layer stack.

4. (Original) The semiconductor structure of claim 1, wherein the first material layer comprises an insulating material, the second material layer comprises a first conductive material, and each of the plurality of landing pads comprises a second conductive material.

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5. (Currently Amended) The semiconductor structure of claim 4, wherein the first conductive material is ~~the same as or~~ different from the second conductive material.

6. (Original) The semiconductor structure of claim 4, wherein:

the insulating material layer comprises silicon oxide, aluminum oxide, or a combination thereof; and

each of the first and the second conductive material layers comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof.

7. (Currently Amended) The semiconductor structure of claim 1, wherein the second material layer of [[each]] a layer stack of the plurality of layer stacks is disposed over a first portion of the first material layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the first material layer of the adjacent layer stack is laterally displaced from the second material layer of the layer stack.

8. (Currently Amended) The semiconductor structure of claim [[7]] 1, wherein one of the plurality of landing pads is thicker than the first material layer of ~~a corresponding~~ the respective layer stack of the plurality of layer stacks and is insulated from another landing pad disposed on an adjacent layer stack of the plurality of layer stacks.

9-17. (Canceled)

18. (Currently Amended) A memory device, comprising:

a substrate;

a memory string disposed over the substrate; and

a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:

a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer is in contact with a side surface of the insulating layer, wherein the second portion of the

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conductive layer comprises a first side surface and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface.

19. (Currently Amended) The memory device of claim 18, wherein the conductive layer of [[each]] a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack.

20. (Currently Amended) The memory device of claim 18, wherein the second portion of the conductive layer ~~is thicker than the first portion of the conductive material layer~~ comprises a layer of conductive material and a landing pad disposed over the layer of conductive material, wherein the layer of conductive material comprises the second side surface, wherein the landing pad comprises the first side surface.

21. (New) The semiconductor structure of claim 1, wherein each landing pad comprises a bottom surface substantially coplanar with another bottom surface of the first material layer of the respective layer stack.

22. (New) The semiconductor structure of claim 21, wherein each landing pad is laterally displaced from the first material layer of the respective layer stack.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/126,956	09/10/2018	2812	1880	4123.0460002	20	3

CONFIRMATION NO. 3036

REPLACEMENT FILING RECEIPT

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

OC000000114087038

Date Mailed: 01/22/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Zhenyu LU, Wuhan, CHINA;
Jun Chen, Wuhan, CHINA;
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Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2018/098962 08/06/2018

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Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
CHINA 201710750398.4 08/28/2017 Access Code Provided

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 01/21/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/126,956**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

STAIRCASE STRUCTURE FOR MEMORY DEVICE

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application

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serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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PGR2025-00021

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证　　明

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申　请　类　型：发明专利

发明 创造 名称：台阶结构及其形成方法

申　　请　　日：2017 年 08 月 28 日

申　　请　　人：长江存储科技有限责任公司

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局长

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2019 年 06 月 26 日

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权利要求书

1、一种台阶结构的形成方法，其特征在于，包括：

提供衬底，在所述衬底上形成叠层结构，在所述叠层结构上形成第一掩膜层；

刻蚀所述第一掩膜层和所述叠层结构形成各台阶层；

在各台阶层上形成着陆垫；

去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层。

2、根据权利要求1所述的方法，其特征在于，所述刻蚀所述第一掩膜层和所述叠层结构形成各台阶层，具体为：在所述第一掩膜层上旋涂光阻层，以所述光阻层为掩膜，多次刻蚀所述第一掩膜层和所述叠层结构形成各台阶层。

3、根据权利要求1所述的方法，其特征在于，

所述叠层结构，具体为多个层叠的氮氧层组，所述氮氧层组自上至下依次为氧化物层和氮化物层；

刻蚀所述第一掩膜层和所述叠层结构形成的各台阶层分别对应一个所述氮氧层组。

4、根据权利要求3所述的方法，其特征在于，所述在各台阶层上形成着陆垫，具体包括：

在除最底层台阶层外的其他台阶层中，去除部分氮化物层，使氮化物层相对于氧化物层凹陷，形成第一凹陷结构；

形成第二掩膜层，所述第二掩膜层覆盖各台阶层及剩余的第一掩膜层，并将所述第一凹陷结构完全填充；

去除第二掩膜层，并在所述第一凹陷结构中形成填充结构，所述填充结构高于所述第一凹陷结构并覆盖部分对应的氧化物层的侧面；

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去除各台阶层中的氧化物层，呈现各台阶层中的氮化物层；

形成加固层，所述加固层覆盖各台阶层中的氮化物层、填充结构及剩余的第一掩膜层；

去除部分加固层、所述填充结构和部分剩余的第一掩膜层，形成各台阶层的着陆垫，使除最底层台阶层外的各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

5、根据权利要求4所述的方法，其特征在于，所述去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层，具体为：去除当前剩余的第一掩膜层及其上的加固层和其下的氧化物层，并形成覆盖层，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

6、一种台阶结构，其特征在于，包括：

衬底及衬底上的叠层结构；

形成于所述叠层结构上的各台阶层；

形成于各台阶层上的着陆垫；

覆盖各台阶层的覆盖层。

7、根据权利要求6所述的台阶结构，其特征在于，所述叠层结构，具体为多个层叠的氮氧层组，所述氮氧层组自上至下依次为氧化物层和氮化物层。

8、根据权利要求7所述的台阶结构，其特征在于，各台阶层分别对应一个氮氧层组，各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

9、根据权利要求8所述的台阶结构，其特征在于，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

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1、一种台阶结构的形成方法，其特征在于，包括：

提供衬底，在所述衬底上形成叠层结构，在所述叠层结构上形成第一掩膜层；

刻蚀所述第一掩膜层和所述叠层结构形成各台阶层；

在各台阶层上形成着陆垫；其中，各着陆垫所在层相对于对应的着陆垫形成有凹陷结构；

去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层。

2、根据权利要求 1 所述的方法，其特征在于，所述刻蚀所述第一掩膜层和所述叠层结构形成各台阶层，具体为：在所述第一掩膜层上旋涂光阻层，以所述光阻层为掩膜，多次刻蚀所述第一掩膜层和所述叠层结构形成各台阶层。

3、根据权利要求 1 所述的方法，其特征在于，

所述叠层结构，具体为多个层叠的氮氧层组，所述氮氧层组自上至下依次为氧化物层和氮化物层；

刻蚀所述第一掩膜层和所述叠层结构形成的各台阶层分别对应一个所述氮氧层组。

4、根据权利要求 3 所述的方法，其特征在于，所述在各台阶层上形成着陆垫，具体包括：

在除最底层台阶层外的其他台阶层中，去除部分氮化物层，使氮化物层相对于氧化物层凹陷，形成第一凹陷结构；

形成第二掩膜层，所述第二掩膜层覆盖各台阶层及剩余的第一掩膜层，并将所述第一凹陷结构完全填充；

去除第二掩膜层，并在所述第一凹陷结构中形成填充结构，所述填充结构高于所述第一凹陷结构并覆盖部分对应的氧化物层的侧面；

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去除各台阶层中的氧化物层，呈现各台阶层中的氮化物层；

形成加固层，所述加固层覆盖各台阶层中的氮化物层、填充结构及剩余的第一掩膜层；

去除部分加固层、所述填充结构和部分剩余的第一掩膜层，形成各台阶层的着陆垫，使除最底层台阶层外的各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

5、根据权利要求4所述的方法，其特征在于，所述去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层，具体为：去除当前剩余的第一掩膜层及其上的加固层和其下的氧化物层，并形成覆盖层，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

6、一种台阶结构，其特征在于，包括：

衬底及衬底上的叠层结构；

形成于所述叠层结构上的各台阶层；

形成于各台阶层上的着陆垫；

覆盖各台阶层的覆盖层。

7、根据权利要求6所述的台阶结构，其特征在于，所述叠层结构，具体为多个层叠的氮氧层组，所述氮氧层组自上至下依次为氧化物层和氮化物层。

8、根据权利要求7所述的台阶结构，其特征在于，各台阶层分别对应一个氮氧层组，各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

9、根据权利要求8所述的台阶结构，其特征在于，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

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1、一种台阶结构的形成方法，其特征在于，包括：

提供衬底，在所述衬底上形成含有多个氮氧层组的叠层结构，所述氮氧层组自上至下依次为氧化物层和氮化物层；

在所述叠层结构上形成第一掩膜层；

刻蚀所述第一掩膜层和所述叠层结构形成各台阶层；

在除最底层台阶层外的其他台阶层中，去除部分氮化物层，使氮化物层相对于氧化物层凹陷，形成第一凹陷结构；

形成第二掩膜层，所述第二掩膜层覆盖各台阶层及剩余的第一掩膜层，并将所述第一凹陷结构完全填充；

去除第二掩膜层，并在所述第一凹陷结构中形成填充结构，所述填充结构高于所述第一凹陷结构并覆盖部分对应的氧化物层的侧面；

去除各台阶层中的氧化物层，呈现各台阶层中的氮化物层；

形成加固层，所述加固层覆盖各台阶层中的氮化物层、填充结构及剩余的第一掩膜层；

去除部分加固层、所述填充结构和部分剩余的第一掩膜层，形成各台阶层的着陆垫，使除最底层台阶层外的各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构；

去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层。

2、根据权利要求 1 所述的方法，其特征在于，所述刻蚀所述第一掩膜层和所述叠层结构形成各台阶层，具体为：在所述第一掩膜层上旋涂光阻层，以所述光阻层为掩膜，多次刻蚀所述第一掩膜层和所述叠层结构形成各台阶层。

3、根据权利要求 1 所述的方法，其特征在于，所述去除剩余的第一掩膜层，

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并形成覆盖各台阶层的覆盖层，具体为：去除当前剩余的第一掩膜层及其上的加固层和其下的氧化物层，并形成覆盖层，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

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说明书

台阶结构及其形成方法

技术领域

本发明涉及半导体技术领域，尤其涉及一种台阶结构及其形成方法。

背景技术

闪存是一种非易变性的存储器，是电可擦除且可编程的只读存储器的一种特殊结构，其运作原理是通过改变晶体管或存储单元的临界电压来控制门极通道的开关以达到存储数据的目的，使存储在存储器中的数据不会因电源中断而消失。闪存以其便捷、存储密度高、可靠性好等优点成为非挥发性存储器研究的热点。从二十世纪八十年代第一个闪存产品问世以来，随着技术的发展和各类电子产品对存储的需求，闪存被广泛的应用于手机、笔记本、掌上电脑和U盘等移动和通讯设备中，并占据了非挥发性半导体存储器的大部分市场份额。

如今，经历了平面型闪存存储器的发展时期，已进入了三维闪存存储器的发展热潮，其主要特色是将平面结构转换为立体结构，通过光刻工艺形成台阶结构，在台阶结构中形成多个横向和纵向的存储单元阵列，并通过在台阶结构中形成水平方向上的字线（Word line）和竖直方向的位线（Bit line）来准确定位各存储区，进而对存储区中的数据进行操作。目前的三维存储器，其台阶结构中字线的厚度是均匀的，然而，随着人们对存储器的容量及体积的要求不断提升，使形成台阶结构的堆栈会不断减小，从而字线的厚度会越来越小，进而导致用单个掩膜来创建台阶间的互连会越来越困难。

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发明内容

为解决现有技术的不足，本发明提供一种台阶结构及其形成方法。

一方面，本发明提供一种台阶结构的形成方法，包括：

提供衬底，在所述衬底上形成叠层结构，在所述叠层结构上形成第一掩膜层；

刻蚀所述第一掩膜层和所述叠层结构形成各台阶层；

在各台阶层上形成着陆垫；

去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层。

可选地，所述刻蚀所述第一掩膜层和所述叠层结构形成各台阶层，具体为：在所述第一掩膜层上旋涂光阻层，以所述光阻层为掩膜，多次刻蚀所述第一掩膜层和所述叠层结构形成各台阶层。

可选地，所述叠层结构，具体为多个层叠的氮氧层组，所述氮氧层组自上至下依次为氧化物层和氮化物层；

刻蚀所述第一掩膜层和所述叠层结构形成的各台阶层分别对应一个所述氮氧层组。

可选地，所述在各台阶层上形成着陆垫，具体包括：

在除最底层台阶层外的其他台阶层中，去除部分氮化物层，使氮化物层相对于氧化物层凹陷，形成第一凹陷结构；

形成第二掩膜层，所述第二掩膜层覆盖各台阶层及剩余的第一掩膜层，并将所述第一凹陷结构完全填充；

去除第二掩膜层，并在所述第一凹陷结构中形成填充结构，所述填充结构高于所述第一凹陷结构并覆盖部分对应的氧化物层的侧面；

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去除各台阶层中的氧化物层，呈现各台阶层中的氮化物层；

形成加固层，所述加固层覆盖各台阶层中的氮化物层、填充结构及剩余的第一掩膜层；

去除部分加固层、所述填充结构和部分剩余的第一掩膜层，形成各台阶层的着陆垫，使除最底层台阶层外的各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

可选地，所述去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层，具体为：去除当前剩余的第一掩膜层及其上的加固层和其下的氧化物层，并形成覆盖层，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

另一方面，本发明提供一种台阶结构，包括：

衬底及衬底上的叠层结构；

形成于所述叠层结构上的各台阶层；

形成于各台阶层上的着陆垫；

覆盖各台阶层的覆盖层。

可选地，所述叠层结构，具体为多个层叠的氮氧层组，所述氮氧层组自上至下依次为氧化物层和氮化物层。

可选地，各台阶层分别对应一个氮氧层组，各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

可选地，所述覆盖层将所述第二凹陷结构完全填充，并覆盖各台阶层。

本发明的优点在于：

本发明中，通过在各台阶层上形成着陆垫，增加了台阶层之间互联部分的厚度，使得即使是很薄的字线需求，通过单张掩膜来形成台阶间的互连亦是可

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行的。

附图说明

通过阅读下文优选实施方式的详细描述，各种其他的优点和益处对于本领域普通技术人员将变得清楚明了。附图仅用于示出优选实施方式的目的，而并不认为是对本发明的限制。而且在整个附图中，用相同的参考符号表示相同的部件。在附图中：

附图 1 为本发明提供的一种形成台阶结构的方法流程图；

附图 2 和附图 3 为本发明提供的形成台阶层的结构变化示意图；

附图 4 至附图 9 为本发明提供的形成着陆垫的结构变化示意图；

附图 10 为本发明提供的部分台阶结构示意图。

具体实施方式

下面将参照附图更详细地描述本公开的示例性实施方式。虽然附图中显示了本公开的示例性实施方式，然而应当理解，可以以各种形式实现本公开而不应被这里阐述的实施方式所限制。相反，提供这些实施方式是为了能够更透彻地理解本公开，并且能够将本公开的范围完整的传达给本领域的技术人员。

实施例一

根据本发明的实施方式，提供一种台阶结构的形成方法，如图 1 所示，包括：

提供衬底，在衬底上形成叠层结构，在叠层结构上形成第一掩膜层；

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刻蚀第一掩膜层和叠层结构形成各台阶层；

在各台阶层上形成着陆垫（Landing Pad）；

去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层。

根据本发明的实施方式，刻蚀第一掩膜层和叠层结构形成各台阶层，具体为：在第一掩膜层上旋涂光阻层，以光阻层为掩膜，多次刻蚀第一掩膜层和叠层结构形成各台阶层。

根据本发明的实施方式，如图 2 和图 3 所示，叠层结构，具体为多个层叠的氮氧层组，氮氧层组自上至下依次为氧化物层（图中未示出）和氮化物层（图中未示出）；

对应地，刻蚀第一掩膜层和叠层结构形成的各台阶层分别对应一个氮氧层组。

需要说明地，在本实施例中，对叠层结构的氮氧层组的数量及形成的台阶层的数量不作具体限定，具体依需求而定，附图仅用于示例说明。

根据本发明的实施方式，在各台阶层上形成着陆垫，如图 4 至图 9 所示，具体包括：

在除最底层台阶层外的其他台阶层中，去除部分氮化物层，使氮化物层相对于氧化物层凹陷，形成第一凹陷结构（Nitride Recess）；

形成第二掩膜层，第二掩膜层覆盖各台阶层及剩余的第一掩膜层，并将第一凹陷结构完全填充（Poly Dep）；

去除第二掩膜层，并在第一凹陷结构中形成填充结构，填充结构高于第一凹陷结构并覆盖部分对应的氧化物层的侧面（Poly Etch）；

去除各台阶层中的氧化物层，呈现各台阶层中的氮化物层（Oxide Etch）；

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形成加固层，加固层覆盖各台阶层中的氮化物层、填充结构及剩余的第一掩膜层（Niteide Dep）；

去除部分加固层、填充结构和部分剩余的第一掩膜层，形成各台阶层的着陆垫，使除最底层台阶层外的各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构（Nitride/Poly Recess）。

其中，第二掩膜层具体为多晶硅，加固层具体为氮化物。

根据本发明的实施方式，采用低压化学气相沉积（Low Pressure Chemical Vapor Deposition，简称LPCVD）的方法和/或等离子体增强化学气相沉积（Plasma Enhanced Chemical Vapor Deposition，简称PECVD）的方法形成第二掩膜层；

根据本发明的实施方式，采用干法刻蚀（Dry Etch）工艺去除第二掩膜层，并在第一凹陷结构中形成填充结构；

根据本发明的实施方式，采用不良梯形覆盖共形工艺（Poor Step Coverage Conformal Process）形成加固层。

进一步地，在本实施例中，去除剩余的第一掩膜层，并形成覆盖各台阶层的覆盖层，具体为：去除当前剩余的第一掩膜层及其上的加固层和其下的氧化物层，并形成覆盖层，覆盖层将第二凹陷结构完全填充，并覆盖各台阶层。

实施例二

根据本发明的实施方式，提供一种台阶结构，包括：

衬底及衬底上的叠层结构；

形成于叠层结构上的各台阶层；

形成于各台阶层上的着陆垫；

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覆盖各台阶层的覆盖层。

根据本发明的实施方式，叠层结构，具体为多个层叠的氮氧层组，氮氧层组自上至下依次为氧化物层和氮化物层。

根据本发明的实施方式，各台阶层分别对应一个氮氧层组，各台阶层的氮化物层相对于对应的着陆垫凹陷，形成第二凹陷结构。

根据本发明的实施方式，覆盖层将第二凹陷结构完全填充，，并覆盖各台阶层。

本发明中，通过在各台阶层上形成着陆垫，增加了台阶层之间互联部分的厚度，使得即使是很薄的字线需求，通过单张掩膜来形成台阶间的互连亦是可行的。

以上所述，仅为本发明较佳的具体实施方式，但本发明的保护范围并不局限于此，任何熟悉本技术领域的技术人员在本发明揭露的技术范围内，可轻易想到的变化或替换，都应涵盖在本发明的保护范围之内。因此，本发明的保护范围应以所述权利要求的保护范围为准。

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2017107503984

说明书附图

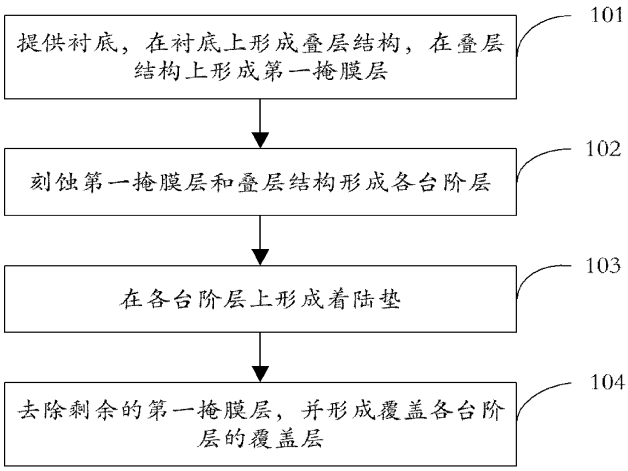


图 1



图 2

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2017107503984

说明书附图

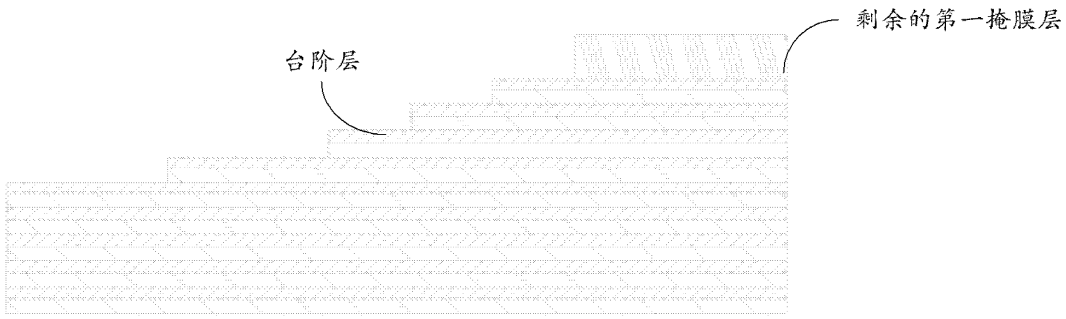


图 3



图 4

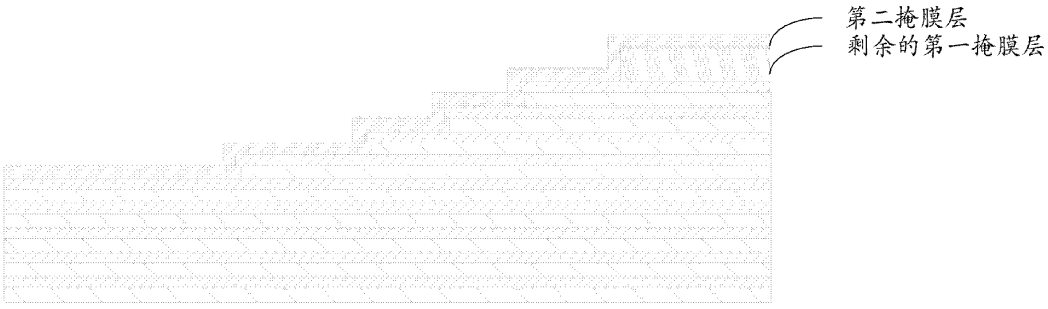


图 5

Micron Ex. 1019, p. 263
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2017107503984

说明书附图

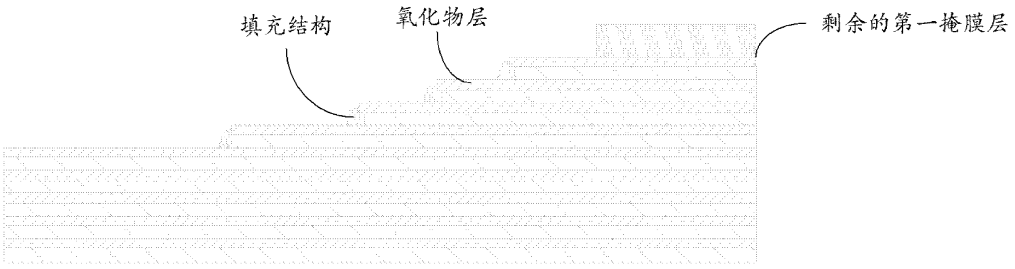


图 6

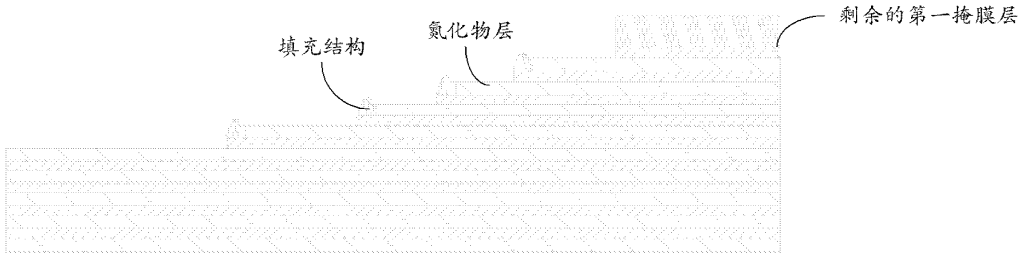


图 7

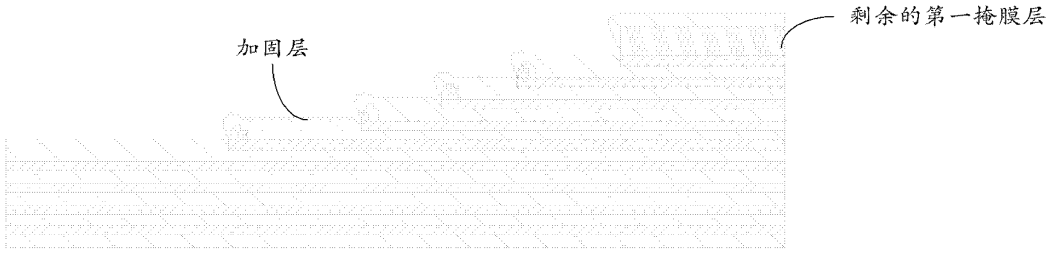


图 8

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说明书附图



图 9

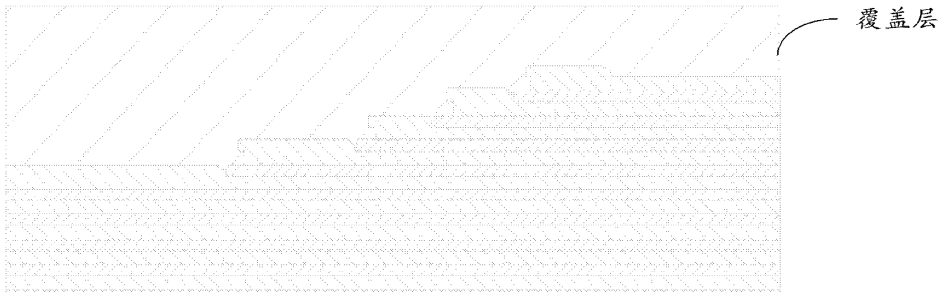


图 10

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,956	09/10/2018	Zhenyu LU	4123.0460002	3036

26111 7590 01/31/2020

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
GEYER, SCOTT B	

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
01/31/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

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Office Action Summary	Application No. 16/126,956	Applicant(s) LU et al.	
	Examiner Scott B Geyer	Art Unit 2812	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 16 January 2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-8 and 18-22 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-2,4,6 and 18 is/are rejected.

8) ☑ Claim(s) 3,5,7-8 and 19-22 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 10 September 2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 20191029.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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DETAILED ACTION

Priority

Receipt is acknowledged of certified copies of papers required by 37 CFR 1.55.

Information Disclosure Statement

The reference cited within the IDS document submitted on October 29, 2019 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claims 1, 2, 4, 6, and 18 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Hyun (US 9,373,540 B2).

As to **claim 1**, Hyun teaches a semiconductor structure in figure 2H (see also figures 2A-2G). The semiconductor structure of Hyun has:

a substrate (not shown, see column 5, lines 17-30); and

a staircase structure (see figure 2H) disposed over the substrate, wherein the staircase structure comprises:

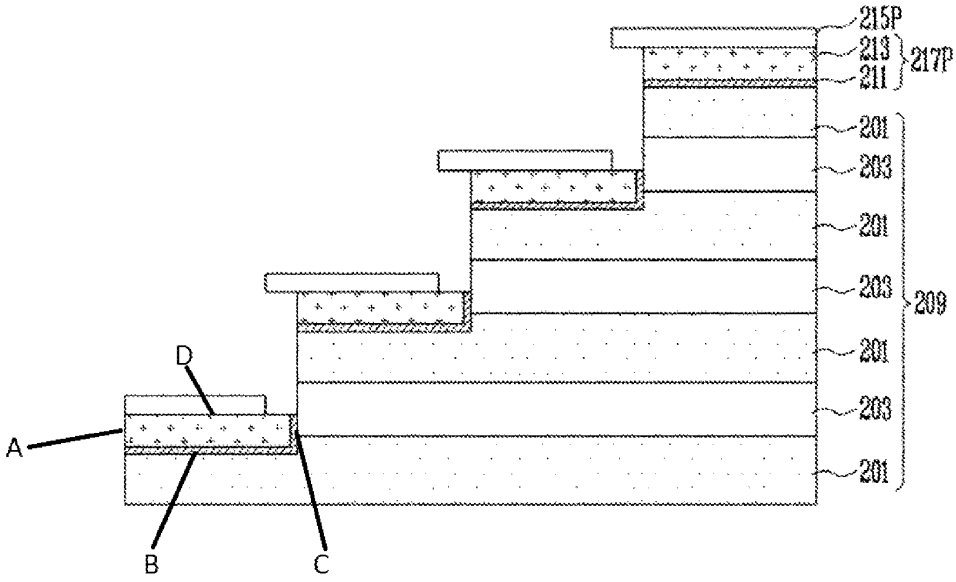
a plurality of layer stacks (203/235), each layer stack comprising a first material layer (203) and a second material layer (235, which is 231+233), wherein the first material layer (203) is disposed over a first portion of the second material layer (235); and

a plurality of landing pads (217P) respectively disposed on the plurality of layer stacks, each landing pad disposed over a second portion of the second material layer (235) of a respective layer stack of the plurality of layer stacks.

Hyun also teaches wherein the each landing pad comprises a first side surface and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface. See for example the annotated figure 2E from Hyun, below. An example landing pad has 4 side surfaces: A, B, C, and D. Sides B and D can be viewed as first and second side surfaces, wherein side B is vertically below (and thus laterally displaced) from side D.

(In addition, sides A and C of Hyun would also be side surfaces, side A would also be laterally displaced from side C, and sides A and C would be adjacent one another – though not in an above/below relationship as B and D are).

FIG. 2E



As to **claim 2**, Hyun teaches each of the plurality of landing pads is adjacent to a side surface of the first material layer of the respective layer stack. See figure 2H.

As to **claim 4**, Hyun teaches the first material layer (203) comprises an insulating material, the second material layer (235) comprises a first conductive material, and each of the plurality of landing pads (217P) comprises a second conductive material.

As to **claim 6**, Hyun teaches the insulating material can be silicon oxide (column 5, lines 31-45) and each of the first and second conductive material layers comprise tungsten (column 7, lines 64-65; column 6, lines 50-52).

As to **claim 18**, Hyun teaches a memory device in figure 2H (see also figures 2A-2G). The memory device of Hyun has:

a memory string (see also figure 1) disposed over the substrate; and

a staircase structure (see figure 2H) disposed adjacent to the memory string, wherein the staircase structure comprises:

a plurality of layer stacks (203/235), each layer stack comprising an insulating layer (203) disposed over a first portion of a conductive layer (235/231+233), wherein a second portion of the conductive layer (217P) is in contact with a side surface of the insulating layer (see figure 2H). Hyun also teaches wherein the second portion of the conductive layer comprises a first side surface and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface (see above explanation for side surfaces within the rejection of claim 1, and annotated figure 2E).

Allowable Subject Matter

Claims 3, 5, 7, 8, and 19-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. (Claim 22 is also objected to as being dependent upon an objected claim.)

Response to Arguments

Applicant's arguments filed January 16, 2020 have been fully considered but they are not persuasive. The applicant has argued that Hyun did not teach the added limitations to claim 1 regarding the side surfaces.

Specifically, the applicant has stated: "*For example, in Fig. 2H of Hyun (illustrated below), the pad pattern 217P (the alleged "the second portion of the conductive layer") only exhibits a straight vertical side surface that connects pad pattern 217's top surface and bottom surface. The straight vertical side surface of pad pattern 217P results from an etching process using protective pattern 215P as a top etch mask (Hyun, 7: 15-21.) Therefore, Hyun does not disclose or suggest the above-noted distinguishing features "wherein the each landing pad comprises a first side surface and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface," as recited in claim 1 and similarly in claim 18.*"

However, the examiner would draw attention to the rejection of claims 1 and 18 above, and note that neither independent claim explicitly details which "side" surfaces are being referred to in the claim. The arguments of the applicant appear to be drawn to the curved feature indicated on one of the 4 sides of the landing pads (e.g. applicant's figure 7). The claims do not currently have enough detail to describe and claim this feature. As such, the Hyun reference still applies to the claims as detailed on previous pages of this instant office action.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer (telephone: 571-272-1958). The examiner can normally be reached on Monday to Friday, 10AM - 4PM. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at: http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles D Garber (telephone: 571-272-2194). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in U.S.A. or Canada) or 571-272-1000.

/SCOTT B GEYER/
Primary Examiner, Art Unit 2812

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/126,956	LU et al.
	Examiner	Art Unit
	Scott B Geyer	2812

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L27/11582, H01L27/1157, H01L27/11575	10/16/2019	SBG
H01L27/11514, H01L27/11521, H01L27/11551, H01L27/11568, H01L27/11578, H01L27/11597	10/16/2019	SBG

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Text searches utilizing above-noted CPC areas	10/16/2019	SBG
EAST search notes attached	10/16/2019	SBG
EAST search updated	01/28/2020	SBG

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

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Receipt date: 10/29/2019

PTO/SB/08a (07-09)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	16/126,956
Filing Date	September 10, 2018
First Named Inventor	Zhenyu LU
Art Unit	2812
Examiner Name	GEYER, SCOTT B
Attorney Docket Number	4123.0460002

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/SG/	1	US- 9,741,563 B2	08-22-2017	Xiang et al.	
		US-			
		US-			
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/SCOTT B GEYER/	Date Considered	01/28/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	47	((Yangtze adj Memory).as. (Zhenyu with LU).in. (Jun with Chen).in. (Xiaowang with Dai).in. (Jifeng with Zhu).in. (Qian with Tao).in. (Yu with Huang).in. (Si with Hu).in. (Lan with Yao).in. (Li with Xiao).in. (Man with Zheng).in. (Kun with Bao).in. (Haohao with Yang).in.) and ((staircase stair-case (stair adj case)) SAME (substrate memory semiconductor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 11:21
S2	770	(H01L27/11582 H01L21/0273 H01L21/31144 H01L27/1157 H01L27/11575).cpc. and ((staircase stair-case (stair adj case)) SAME (substrate memory semiconductor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 11:21
S3	3	(("20150255385") or ("20190081070") or ("9419013")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 11:37
S4	1	(14/465573).APP.	USPAT; USOCR	OR	OFF	2019/10/15 11:40
S5	3	("20080073635" | "20130234232").PN. OR ("9356038").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 11:40
S6	29	("20100207195" | "20120061743" | "20130056818" | "20140162420" | "20140191389" | "20140199815" | "20140225183" | "20140264934" | "20140293703" | "20140306279" | "20140367759" | "20150035065" | "20150064900" | "20150187789" | "20150255468" | "20150263029" | "8728889" | "8822285" | "8828884" | "8871591" | "8928149").PN. OR ("9419013").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 11:40
S7	2123	(staircase stair-case (stair adj case)) SAME memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 12:36
S8	1076	(staircase stair-case (stair adj case)) with memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 12:36
S9	9	("20160336330" | "20170084532" |	US-PGPUB;	OR	OFF	2019/10/15

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		"20180366453" | "9202780" | "9331082" | "9343452" | "9356038" | "9373540" | "9478487").PN. OR ("10403641").URPN.	USPAT; USOCR			12:52
S10	6	("20110031630" | "20130127011" | "20150255386" | "8304348").PN. OR ("9373540").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 12:59
S11	1	(12/709124).APP.	USPAT; USOCR	OR	OFF	2019/10/15 13:02
S12	15	("20070134817" | "20080121953" | "20090317978").PN. OR ("8304348").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 13:02
S13	8	("20120119283" | "20130270714" | "20130334589" | "8304348" | "8395190" | "9006884").PN. OR ("9343452").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 13:09
S14	383	(H01L27/11514 H01L27/11521 H01L27/11551 H01L27/11568 H01L27/11578 H01L27/11597).cpc. and (staircase stair-case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/15 17:17
S15	123	S14 and (stack layer tier) with pad	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/15 17:17
S16	11	(("10403641") or ("20170084532") or ("9478487") or ("9373540") or ("20150255386") or ("20110031630") or ("10002880") or ("9343452") or ("20130270714") or ("9006884") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 17:26
S17	3	(("9373540") or ("20110031630") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 17:39
S19	3	(("9373540") or ("20110031630") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 10:55
S20	1	("9373540").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 11:19
S21	1	S20 and string	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/16 12:35
S22	1	("20110031630").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 12:45
S23	11	(("10403641") or ("20170084532") or ("9478487") or ("9373540") or ("20150255386") or ("20110031630") or ("10002880") or ("9343452") or ("20130270714") or ("9006884") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 13:01

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S24	419	(H01L27/11514 H01L27/11521 H01L27/11551 H01L27/11568 H01L27/11578 H01L27/11597).cpc. and (staircase stair-case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/01/28 10:40
S26	363	S24 and ((stack layer tier) with (land landing pad contact electrode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/01/28 10:41
S27	347	S26 not ("2020" "2019").ay.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/01/28 10:41
S28	1	("9741563").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/01/28 11:16
S29	11	(("10403641") or ("20170084532") or ("9478487") or ("9373540") or ("20150255386") or ("20110031630") or ("10002880") or ("9343452") or ("20130270714") or ("9006884") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/01/28 11:32
S30	2	(("9373540") or ("20110031630")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/01/28 14:43

1/ 28/ 2020 4:42:54 PM
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Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
4123.0460002	16/126,956	September 10, 2018
First Named Inventor:	**Title:**	
Zhenyu LU	STAIRCASE STRUCTURE FOR MEMORY DEVICE	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:

- Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
- The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
  - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
  - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
    - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
    - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	Date
/Donald J. Featherstone/	3/13/2020
Name (Print/Typed) Donald J. Featherstone	**Practitioner Registration No.** 33,876

***Note**: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

[✓] * Total of one (1) forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: LU *et al.*	Confirmation No.: 3036
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: 2812
Application No.: 16/126,956	Examiner: GEYER, Scott B.
Filing Date: September 10, 2018	Atty. Docket: 4123.0460002

Title: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**

Amendment and Reply Under 37 C.F.R. § 1.116

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop AF

Commissioner:

In reply to the Office Action dated January 31, 2020 ("Final Office Action"), Applicant submits the following Amendment and Remarks, and concurrently files a Request for Consideration under After Final Consideration Pilot Program 2.0 (AFCP 2.0) herewith in the captioned application.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A semiconductor structure, comprising:

a substrate; and

a staircase structure disposed over the substrate, wherein the staircase structure comprises:

a plurality of layer stacks, each layer stack comprising a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and

a plurality of landing pads respectively disposed on the plurality of layer stacks, each landing pad disposed over a second portion of the second material layer of a respective layer stack of the plurality of layer stacks, wherein the each landing pad comprises a bottom surface, a first side surface, and a second side surface, wherein the second side surface is vertically below and laterally displaced from the first side surface, wherein the bottom surface is substantially coplanar with another bottom surface of the first material layer of the respective layer stack.

2. (Previously Presented) The semiconductor structure of claim 1, wherein each of the plurality of landing pads is adjacent to a side surface of the first material layer of the respective layer stack.

3. (Previously Presented) The semiconductor structure of claim 1, wherein a first portion of a landing pad of the plurality of landing pads is in contact with the second material layer of the respective layer stack, and a second portion of the landing pad is laterally displaced from the second material layer of the respective layer stack.

4. (Original) The semiconductor structure of claim 1, wherein the first material layer comprises an insulating material, the second material layer comprises a first conductive material, and each of the plurality of landing pads comprises a second conductive material.

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5. (Previously Presented) The semiconductor structure of claim 4, wherein the first conductive material is different from the second conductive material.

6. (Original) The semiconductor structure of claim 4, wherein:

the insulating material layer comprises silicon oxide, aluminum oxide, or a combination thereof; and

each of the first and the second conductive material layers comprises tungsten, silicide, nickel, titanium, platinum, aluminum, titanium nitride, tantalum nitride, tungsten nitride, or a combination thereof.

7. (Previously Presented) The semiconductor structure of claim 1, wherein the second material layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the first material layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the first material layer of the adjacent layer stack is laterally displaced from the second material layer of the layer stack.

8. (Previously Presented) The semiconductor structure of claim 1, wherein one of the plurality of landing pads is thicker than the first material layer of the respective layer stack of the plurality of layer stacks and is insulated from another landing pad disposed on an adjacent layer stack of the plurality of layer stacks.

9-17. (Canceled)

18. (Currently Amended) A memory device, comprising:

a substrate, wherein the substrate comprises a top surface;

a memory string disposed over the substrate; and

a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:

a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer, wherein a second portion of the conductive layer is in contact with a side surface of the insulating layer, wherein the second portion of the

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conductive layer comprises a first side surface and a second side surface, wherein the first side surface and the second side surface are substantially perpendicular to the top surface, wherein the second side surface is vertically below and laterally displaced from the first side surface.

19. (Previously Presented) The memory device of claim 18, wherein the conductive layer of a layer stack of the plurality of layer stacks is disposed over a first portion of the insulating layer of an adjacent layer stack of the plurality of layer stacks, wherein a second portion of the insulating layer of the adjacent layer stack is laterally displaced from the conductive layer of the layer stack.

20. (Previously Presented) The memory device of claim 18, wherein the second portion of the conductive layer comprises a layer of conductive material and a landing pad disposed over the layer of conductive material, wherein the layer of conductive material comprises the second side surface, wherein the landing pad comprises the first side surface.

21. (Canceled)

22. (Currently Amended) The semiconductor structure of claim [[21]] 1, wherein each landing pad is laterally displaced from the first material layer of the respective layer stack.

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Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-8, 18-20, and 22 are pending in the application, with claims 1 and 18 being the independent claims. Claims 1, 18 and 22 are sought to be amended. Claim 21 is sought to be canceled without prejudice to or disclaimer of the subject matter therein. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Under 37 C.F.R. §1.116, the amendments set forth above should be entered as they (i) satisfy a requirement of form expressly set forth in a previous Office Action; (ii) place the claims in better form for consideration on appeal, should such an appeal be necessary; or (iii) are necessary and were not presented earlier for the good and sufficient reason that they are being made in response to the grounds of rejection set forth in the Final Office Action.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Objections to the Claims/Allowable Subject Matter

Applicant thanks the Examiner indicating the allowability of claims 3, 5, 7, 8, and 19-22 if rewritten in independent form including all of the limitations of the base claim and any intervening claims (see Final Office Action, P. 5). Without acquiescing to the propriety of the rejections below, Applicant has amended the independent claim 1 to incorporate the allowable subject matter of claim 21. Thus, independent claim 1 is in condition for allowance. Dependent claims 3, 5, 7, 8, and 22

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should also be found allowable at least based on their dependencies from the independent claim 1, as well as for their additional distinguishing features.

Rejections under 35 U.S.C. § 102

Claims 1, 2, 4, 6, and 18 were rejected under 35 U.S.C. § 102(a)(1) as allegedly being anticipated by U.S. Patent No. 9,373,540 B2 to Hyun ("Hyun"). Applicant respectively traverse these rejections.

Claims 1, 2, 4, and 6

Without acquiescing to the propriety of the rejections and reserving the right to argue additional or different distinguishing features in the future, independent claim 1 has been amended to incorporate allowable subject matter from claim 21. For example, claim 1 has been amended to include the feature of "wherein each landing pad comprises a bottom surface substantially coplanar with another bottom surface of the first material layer of the respective layer stack" as recited in claim 21, which is allowable subject matter (see Final Office Action, p. 5) and patentable over Hyun. Thus, claim 1 is in condition for allowance. Dependent claims 2, 4, and 6 should also be found allowable at least based on their dependencies from the independent claim 1, as well as for their additional distinguishing features.

Accordingly, Applicant respectfully requests the Examiner to reconsider and withdraw the rejection under 35 U.S.C. § 102 and to pass claims 1, 2, 4, and 6 to allowance.

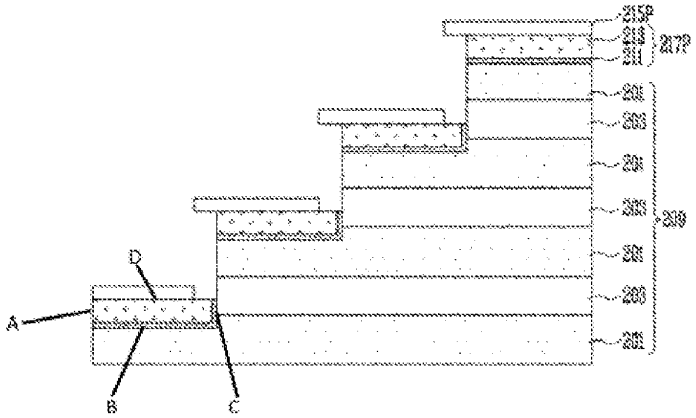
Claim 18

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Without acquiescing to the propriety of the rejections, independent claim 18 has been amended to further clarify its distinguishing features. For example, claim 18 has been amended to recite "wherein the first side surface and the second side surface are substantially perpendicular to the top surface." Hyun does not disclose these distinguishing features.

Referring to the annotated Fig. 2E of Hyun (see Final Office Action, p. 4), the Office concedes that "sides A and C…would not in an above/below relationship B and D are." (see Final Office Action, p. 3). Thus, Hyun does disclose or suggest the above-noted distinguishing feature "wherein the first side surface and the second side surface are substantially perpendicular to the top surface," as recited in claim 18.

FIG. 2E



Annotated Fig. 2E of Hyun

In view of above, independent claim 18 is patentable over Hyun. Dependent claims 19 and 20 should also be found allowable at least based on their dependencies from independent claim 18, as well as for their additional distinguishing features. Accordingly, Applicant respectfully requests

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that the rejection under 35 U.S.C. § 102 be reconsidered and withdrawn and the claims passed to allowance.

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Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 3/13/2020

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Electronic Acknowledgement Receipt

EFS ID:	38860798
Application Number:	16126956
International Application Number:	
Confirmation Number:	3036
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Customer Number:	26111
Filer:	Donald J. Featherstone/Tonyia Skinner
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0460002
Receipt Date:	13-MAR-2020
Filing Date:	10-SEP-2018
Time Stamp:	15:58:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2020-03-13-Cover-Letter-4123-0460002.pdf	300042 f61c67b0a651a5ee65846e7078079071eb31a390	no	1
Warnings:					

Information:					
2	After Final Consideration Program Request	2020-03-13-AFCP-Request-4123-0460002.PDF	226760 1c03f1c461a271fa5f4754f2a94336707fdac5d0	no	2
Warnings:					
Information:					
3		2020-03-13-Amendment-Reply-116-4123-0460002.pdf	169821 b0c86662f78ffd11879e9a9dbee9a6e69a8a8dd6	yes	9

Multipart Description/PDF files in .zip description

Document Description	Start	End
Response After Final Action	1	1
Claims	2	4
Applicant Arguments/Remarks Made in an Amendment	5	9

Warnings:	
Information:	
Total Files Size (in bytes):	696623

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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March 13, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 3036
Art Unit 2812
Attn: Mail Stop AF

Re: U.S. Utility Patent Application
Appl. No. 16/126,956; Filing Date: September 10, 2018
For: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**
Inventors: LU *et al.*
Our Ref: 4123.0460002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Certification and Request for Consideration Under the After Final Consideration Pilot Program 2.0 (PTO/SB/434); and

2. Amendment and Reply Under 37 C.F.R. § 1.116.

The above-listed documents are filed electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/KTS/tas
Enclosures

14531512_1.docx

Micron Ex. 1019, p. 293
Micron v. YMTC
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/126,956	Filing Date 09/10/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	03/13/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/SULONDA D STEVENSON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 03/25/2020

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER
GEYER, SCOTT B

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/25/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,956	09/10/2018	Zhenyu LU	4123.0460002	3036

TITLE OF INVENTION: STAIRCASE STRUCTURE FOR MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	06/25/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

Micron Ex. 1019, p. 295
Micron v. YMTC
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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 03/25/2020

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,956	09/10/2018	Zhenyu LU	4123.0460002	3036

TITLE OF INVENTION: STAIRCASE STRUCTURE FOR MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	06/25/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
GEYER, SCOTT B	2812	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Micron Ex. 1019, p. 296
Micron v. YMTC
PGR2025-00021

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,956	09/10/2018	Zhenyu LU	4123.0460002	3036

26111 7590 03/25/2020

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
GEYER, SCOTT B	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/25/2020

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/126,956	Applicant(s) LU et al.	
	Examiner Scott B Geyer	Art Unit 2812	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to papers filed by the applicant on March 13, 2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-8,18-20 and 22 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some *c) ☐ None of the:

   1. ☑ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/SCOTT B GEYER/
Primary Examiner, Art Unit 2812

Micron Ex. 1019, p. 299
Micron v. YMTC
PGR2025-00021

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/126,956	LU et al.
	Examiner	Art Unit
	Scott B Geyer	2812

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L27/11582, H01L27/1157, H01L27/11575	10/16/2019	SBG
H01L27/11514, H01L27/11521, H01L27/11551, H01L27/11568, H01L27/11578, H01L27/11597	10/16/2019	SBG

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Text searches utilizing above-noted CPC areas	10/16/2019	SBG
EAST search notes attached	10/16/2019	SBG
EAST search updated	01/28/2020	SBG
EAST search updated	03/18/2020	SBG

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
	Interference Search	03/18/2020	SBG

Micron Ex. 1019, p. 300
Micron v. YMTC
PGR2025-00021

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/126,956	LU et al.
	Examiner	**Art Unit**
	Scott B Geyer	2812

CPC						
Symbol					**Type**	**Version**
H01L	/	27	/	11524	F	2013-01-01
H01L	/	27	/	11582	I	2013-01-01
H01L	/	21	/	0273	I	2013-01-01
H01L	/	27	/	1157	I	2013-01-01
H01L	/	27	/	11575	I	2013-01-01
H01L	/	21	/	31144	I	2013-01-01
H01L	/	27	/	11529	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	12	
/SCOTT B GEYER/ Primary Examiner, Art Unit 2812	18 March 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7

U.S. Patent and Trademark Office — Part of Paper No.: 20200318

Micron Ex. 1019, p. 301
Micron v. YMTC
PGR2025-00021

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/126,956	LU et al.
	Examiner	**Art Unit**
	Scott B Geyer	2812

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L	/	27	/	11524

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/SCOTT B GEYER/ Primary Examiner, Art Unit 2812	18 March 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7

U.S. Patent and Trademark Office — Part of Paper No.: 20200318

Micron Ex. 1019, p. 302
Micron v. YMTC
PGR2025-00021

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/126,956	LU et al.
	Examiner	**Art Unit**
	Scott B Geyer	2812

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		10	11	19										
2	2		11	12	20										
3	3		12		21										
4	4		13	9	22										
5	5		14												
6	6		15												
7	7		16												
8	8		17												
	9	10	18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	12	
/SCOTT B GEYER/ Primary Examiner, Art Unit 2812	18 March 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7

U.S. Patent and Trademark Office — Part of Paper No.: 20200318

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Amendment Under 37 C.F.R. § 1.116
Expedited Procedure – Art Unit 2812

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: LU *et al.*	Confirmation No.: 3036
Applicant: Yangtze Memory Technologies Co., Ltd.	Art Unit: 2812
Application No.: 16/126,956	Examiner: GEYER, Scott B.
Filing Date: September 10, 2018	Atty. Docket: 4123.0460002

Title: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**

Amendment and Reply Under 37 C.F.R. § 1.116

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop AF

OK TO ENTER: /S.B.G/

Commissioner:

In reply to the Office Action dated January 31, 2020 ("Final Office Action"), Applicant submits the following Amendment and Remarks, and concurrently files a Request for Consideration under After Final Consideration Pilot Program 2.0 (AFCP 2.0) herewith in the captioned application.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	672	(H01L27/11514 H01L27/11521 H01L27/11551 H01L27/11568 H01L27/11578 H01L27/11597).cpc. and (staircase stair-case (stair adj case) stairstep stair-step (stair adj step))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:16
L3	566	1 and ((stack$3 layer$3 tier$2) with (land landing pad contact electrode))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:18
L4	541	3 not ("2020" "2019").ay.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:18
L5	1676	(staircase stair-case (stair adj case) stairstep stair-step (stair adj step)) with memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:28
L6	79	(H01L23/522 H01L23/5226).cpc. and (H01L27/11514 H01L27/11521 H01L27/11551 H01L27/11568 H01L27/11578 H01L27/11597).cpc. and (staircase stair-case (stair adj case) stairstep stair-step (stair adj step))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:31
L7	631	(H01L23/522 H01L23/5226).cpc. and (H01L27/11514 H01L27/11521 H01L27/11551 H01L27/11568 H01L27/11578 H01L27/11597).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:31
L8	74	6 not ("2020" "2019").ay.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:31
L9	83	(H01L23/522 H01L23/5226	US-PGPUB;	OR	ON	2020/03/18

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		H01L23/5283).cpc. and (H01L27/11514 H01L27/11521 H01L27/11551 H01L27/11568 H01L27/11578 H01L27/11597).cpc. and (staircase stair-case (stair adj case) stairstep stair-step (stair adj step))	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			14:33
L10	393	1 and ((land landing pad contact electrode) with (wordline word-line (word adj line)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:42
L11	930	(H01L27/11514 H01L27/11521 H01L27/11524 H01L27/11551 H01L27/11568 H01L27/11578 H01L27/11597).cpc. and (staircase stair-case (stair adj case) stairstep stair-step (stair adj step))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:44
L12	2020	(H01L27/105-11597).cpc. and (staircase stair-case (stair adj case) stairstep stair-step (stair adj step))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:45
L13	1085	12 and ((land landing pad contact electrode) with (wordline word-line (word adj line)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:45
L14	1014	13 not ("2020" "2019").ay.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:45
L15	432	(H01L27/11524 H01L27/11529).cpc. and (staircase stair-case (stair adj case) stairstep stair-step (stair adj step))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:55
L16	241	15 and ((land landing pad contact electrode) with (wordline word-line (word adj line)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/03/18 14:56
L17	224	16 not ("2020" "2019").ay.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2020/03/18 14:56

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			IBM_TDB			
S1	47	((Yangtze adj Memory).as. (Zhenyu with LU).in. (Jun with Chen).in. (Xiaowang with Dai).in. (Jifeng with Zhu).in. (Qian with Tao).in. (Yu with Huang).in. (Si with Hu).in. (Lan with Yao).in. (Li with Xiao).in. (Man with Zheng).in. (Kun with Bao).in. (Haohao with Yang).in.) and ((staircase stair-case (stair adj case)) SAME (substrate memory semiconductor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 11:21
S2	770	(H01L27/11582 H01L21/0273 H01L21/31144 H01L27/1157 H01L27/11575).cpc. and ((staircase stair-case (stair adj case)) SAME (substrate memory semiconductor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 11:21
S3	3	(("20150255385") or ("20190081070") or ("9419013")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 11:37
S4	1	(14/465573).APP.	USPAT; USOCR	OR	OFF	2019/10/15 11:40
S5	3	("20080073635" | "20130234232").PN. OR ("9356038").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 11:40
S6	29	("20100207195" | "20120061743" | "20130056818" | "20140162420" | "20140191389" | "20140199815" | "20140225183" | "20140264934" | "20140293703" | "20140306279" | "20140367759" | "20150035065" | "20150064900" | "20150187789" | "20150255468" | "20150263029" | "8728889" | "8822285" | "8828884" | "8871591" | "8928149").PN. OR ("9419013").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 11:40
S7	2123	(staircase stair-case (stair adj case)) SAME memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 12:36
S8	1076	(staircase stair-case (stair adj case)) with memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/15 12:36
S9	9	("20160336330" | "20170084532" | "20180366453" | "9202780" | "9331082" | "9343452" | "9356038" | "9373540" | "9478487").PN. OR ("10403641").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 12:52
S10	6	("20110031630" | "20130127011" | "20150255386" | "8304348").PN. OR ("9373540").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 12:59
S11	1	(12/709124).APP.	USPAT; USOCR	OR	OFF	2019/10/15 13:02
S12	15	("20070134817" | "20080121953" |	US-PGPUB;	OR	OFF	2019/10/15

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		"20090317978").PN. OR ("8304348").URPN.	USPAT; USOCR			13:02
S13	8	("20120119283" | "20130270714" | "20130334589" | "8304348" | "8395190" | "9006884").PN. OR ("9343452").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 13:09
S14	383	(H01L27/11514 H01L27/11521 H01L27/11551 H01L27/11568 H01L27/11578 H01L27/11597).cpc. and (staircase stair-case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/15 17:17
S15	123	S14 and (stack layer tier) with pad	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/10/15 17:17
S16	11	(("10403641") or ("20170084532") or ("9478487") or ("9373540") or ("20150255386") or ("20110031630") or ("10002880") or ("9343452") or ("20130270714") or ("9006884") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 17:26
S17	3	(("9373540") or ("20110031630") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/15 17:39
S19	3	(("9373540") or ("20110031630") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 10:55
S20	1	("9373540").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 11:19
S21	1	S20 and string	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2019/10/16 12:35
S22	1	("20110031630").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 12:45
S23	11	(("10403641") or ("20170084532") or ("9478487") or ("9373540") or ("20150255386") or ("20110031630") or ("10002880") or ("9343452") or ("20130270714") or ("9006884") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/10/16 13:01
S24	419	(H01L27/11514 H01L27/11521 H01L27/11551 H01L27/11568 H01L27/11578 H01L27/11597).cpc. and (staircase stair-case (stair adj case))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/01/28 10:40
S26	363	S24 and ((stack layer tier) with (land landing pad contact electrode))	US-PGPUB; USPAT; USOCR;	OR	ON	2020/01/28 10:41

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S27	347	S26 not ("2020" "2019").ay.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/01/28 10:41
S28	1	("9741563").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/01/28 11:16
S29	11	(("10403641") or ("20170084532") or ("9478487") or ("9373540") or ("20150255386") or ("20110031630") or ("10002880") or ("9343452") or ("20130270714") or ("9006884") or ("9331082")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/01/28 11:32
S30	2	(("9373540") or ("20110031630")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2020/01/28 14:43

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L18		((staircase stair-case (stair adj case) stairstep stair-step (stair adj step)) with memory).clm. and (landing land pad contact electrode).clm.	US-PGPUB; USPAT	OR	ON	2020/03/18 15:05

3/18/2020 3:09:11 PM
C:\Users\sgeyer\Documents\EAST\Workspaces\16 126956.wsp

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Sterne Kessler
STERNE KESSLER GOLDSTEIN & FOX

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DIRECTOR
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DONF@STERNEKESSLER.COM

April 28, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 3036
Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 16/126,956; Filed: September 10, 2018
For: **STAIRCASE STRUCTURE FOR MEMORY DEVICE**
Inventors: LU *et al.*
Our Ref: 4123.0460002

Commissioner:

In response to the **Notice of Allowance and Fee(s) Due** dated March 25, 2020, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark Office:

1. Online Credit Card Payment Authorization for **$1,000.00** to cover the Issue Fee; and

2. Issue Fee Transmittal (Form PTOL-85).

The above-listed documents are filed electronically.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/KTS/tas
Enclosures

14849588.1

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7598 03/25/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,956	09/10/2018	Zhenyu LU	4123.0460002	3036

TITLE OF INVENTION: STAIRCASE STRUCTURE FOR MEMORY DEVICE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	06/25/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
GEYER, SCOTT B	2812	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sterne, Kessler, Goldstein &
2 Fox P.L.L.C.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Yangtze Memory Technologies Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Wuhan, Hubei, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 19-0036

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Donald J. Featherstone/ Date 4/28/2020

Typed or printed name Donald J. Featherstone Registration No. 33,876

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Electronic Patent Application Fee Transmittal

Application Number:	16126956
Filing Date:	10-Sep-2018
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Filer:	Donald J. Featherstone/Tonyia Skinner
Attorney Docket Number:	4123.0460002

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt	
EFS ID:	39288022
Application Number:	16126956
International Application Number:	
Confirmation Number:	3036
Title of Invention:	STAIRCASE STRUCTURE FOR MEMORY DEVICE
First Named Inventor/Applicant Name:	Zhenyu LU
Customer Number:	26111
Filer:	Donald J. Featherstone/Tonyia Skinner
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0460002
Receipt Date:	28-APR-2020
Filing Date:	10-SEP-2018
Time Stamp:	15:15:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	E20204RF15356554
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2020-04-28-Filing-Bundle-4123-0460002.pdf	36549 a3effccf41204185ab30ad53d195e60b698da2b4	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Issue Fee Payment (PTO-85B)	2	2

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30155 cfbdd480b0ecfdc24d0d28e7dfedb2f2933bdd5b	no	2

Warnings:

Information:

Total Files Size (in bytes):	66704

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,956	06/09/2020	10680003	4123.0460002	3036

26111 7590 05/20/2020

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
16/126,956	**07/03/2024 03:18:05 PM Z ET**	**4123.0460002**

Title of Invention

STAIRCASE STRUCTURE FOR MEMORY DEVICE

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	10680003
CONFIRMATION #	3036	FILED BY	Hillary White
PATENT CENTER #	66232521	FILING DATE	09/10/2018
CUSTOMER #	26111	FIRST NAMED INVENTOR	Zhenyu LU
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Mark Zimmerman

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2017-00295-YMTC-PCT-US_POA.pdf	3	Power of Attorney	402 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2017-00295-YMTC-PCT-US_POA.pdf	5967A695221D7546238EFB1E1C7E38F9BC2672EF80DA4563330BC08A13AD74B97082D459104B6D204C0FE8E8CDE8F5DE0DA01DFF446B570D3D6CD27FC7E1CB83

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Application Number	16126956
Filing Date	September 10, 2018
First Named Inventor	Zhenyu LU
Title	STAIRCASE STRUCTURE FOR MEMORY DEVICE
Art Unit	2812
Examiner Name	SCOTT GEYER
Attorney Docket Number	2017-00295-YMTC-PCT-US

SIGNATURE of Applicant or Patent Practitioner

Signature	/Mark C. Zimmerman /	Date (Optional)	July 3, 2024
Name	Mark C. Zimmerman	Registration Number	44006
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

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I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

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I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	Tuenlap Daniel Chan		
Title	Deputy General Counsel, Head of Intellectual Property Department		

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PGR2025-00021

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