

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: June 6, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case PGR2025-00021
Patent 12,010,838

**DECLARATION OF KONSTANTINOS GIAPIS
IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE**

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I. Introduction and Qualifications

1. I have been retained by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) to provide my opinions concerning the validity of certain claims of U.S. Patent No. 12,010,838 (Ex. 1001).

2. I am a professor of chemical engineering at the California Institute of Technology (“Caltech”). I have held a professorial position at Caltech since 1993.

3. My primary research relates to the processing of semiconductors, dielectrics, and metals, as performed in the fabrication of semiconductor devices, including microprocessors and digital memories. In particular, my work has focused upon experimental and computational studies of various aspects of depositing and patterning of layers of electronic materials to fabricate sub-micron features such as transistor gates, vias, and interconnect channels found in VLSI circuits and digital storage. My research group has contributed to the understanding of the evolution of such features (profiles) in single-crystalline silicon, poly-silicon, metal, and dielectric layers subjected to plasma processing (etching, deposition, ion implantation). Since the start of my graduate career in 1985, I have accumulated over 40 years of experience on most aspects of processing of semiconductor materials and devices.

4. In my professorial duties at Caltech, I have developed and taught new undergraduate and graduate level courses on semiconductor device physics, processing, and fabrication. These innovative courses combined solid state physics and electronic materials processing technologies with the more traditional chemical engineering subjects of transport phenomena and chemical thermodynamics. The courses have prepared several generations of students for successful careers in the semiconductor industry.

5. During my research career, I have authored or co-authored 100 peer-reviewed papers, 12 refereed conference proceedings, and two book chapters. Most of my publications relate to basic aspects of semiconductor processing and, in particular, the interaction dynamics of plasma ions with patterned and unpatterned surfaces of materials used in semiconductor manufacturing. My papers on charging damage during plasma-processing of VLSI devices are highly cited. The latter work includes studies of charging effects and surface breakdown during directional (plasma) deposition of interlevel dielectrics on patterned metal interconnects. My laboratory has also extensively used and studied plasma-deposited silicon oxide layers from silane and TEOS precursors.

6. Additional information regarding my education, technical experience and publications, including a list of 14 U.S. patents I have co-

invented, is included in my *Curriculum Vitae*, which I understand is attached at Exhibit 2007.

II. Summary Of Materials Reviewed And Considered

7. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor fabrication, I reviewed the following documents, and other documents cited herein:

Ex.	Description
1001	United States Patent No. 12,010,838 (“the ’838 patent”)
1002	File History for the ’838 patent (“’838 FH”)
1003	Declaration of Dr. Jack C. Lee
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent No. 10,229,929 to Kim et al. (“Kim”)
1006	U.S. Patent Publication No. 2014/0191389 A1 to Lee et al. (“Lee”)
1007	U.S. Patent No. 9,941,153 to Yang (“Yang”)
1008	U.S. Patent No. 9,520,402 to Haller et al. (“Haller”)
1009	U.S. Patent No. 10,297,543 to Park et al. (“Park”)
1011	Aritome, “Nand Flash Memory Technologies” (2016)
1012	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1014	U.S. Patent Publication No. 2016/0218107 A1 to Lee et al. (“Lee 107”)

8. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the ’838

patent at the time of the alleged invention, which I have been asked to assume is August 28, 2017.

III. Understanding of Legal Standards

9. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

10. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

A. Claim construction

11. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim

construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary. I also have been informed by Counsel that it is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.

12. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office ("USPTO"). I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Obviousness

13. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While

such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

14. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

15. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the

pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

16. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

17. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated

to make a combination includes whether he/she would select particular references in order to combine their elements.

18. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

19. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

20. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not

to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness.

IV. Person Having Ordinary Skill in the Art

21. Petitioner's expert defines a person having ordinary skill in the art ("POSITA") as a person having "a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) 3D memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may substitute for professional experience)." Ex. 1003 ¶ 36. Petitioner's expert further notes that "this POSITA would also have been aware of and generally knowledgeable about 3D memory's structure, its component parts, and how it operates." Ex. 1003 ¶ 37.

22. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art. In view of my educational

background and work experience, I surpass Petitioner's expert's definition of a POSITA, and did so before August 28, 2017. Regardless of the precise definition of a POSITA, none of the Grounds in the Petition show that the challenged claims are obvious. I reserve the right to opine as to an alternative level of a POSITA in other proceedings or if the Board institutes review in this proceeding.

V. Overview of 3D NAND Memories

23. 3D NAND memory is an assembly of discrete memory cells in three dimensions, developed to increase digital memory density. While the process has matured over the years, it is not a simple or straightforward technology.

24. 3D NAND memory devices include “a stack of word lines horizontally arranged over a substrate, with vertical semiconductor channels that intersect the word lines.” ’838 patent at 1:33-36. “The intersection of a word line and a vertical semiconductor channel forms a memory cell.” ’838 patent at 1:36-37. Memory cells can be written or read by applying a voltage to the “word lines,” which are made of an electrically conductive material and run horizontally across the memory array. *E.g.*, ’838 patent at 5:27-33; Ex. 1014 at [0006]. For example, the figure below, from Exhibit 1012, shows vertically stacked memory cells on the left hand side, each controlled by a Control Gate (CG) accessible

electrically by means of word lines. Ex. 1012 at 134; *see also* Ex. 1011 at 62, Fig. 3.4 (equating “Control Gate” with “Word Line”).¹

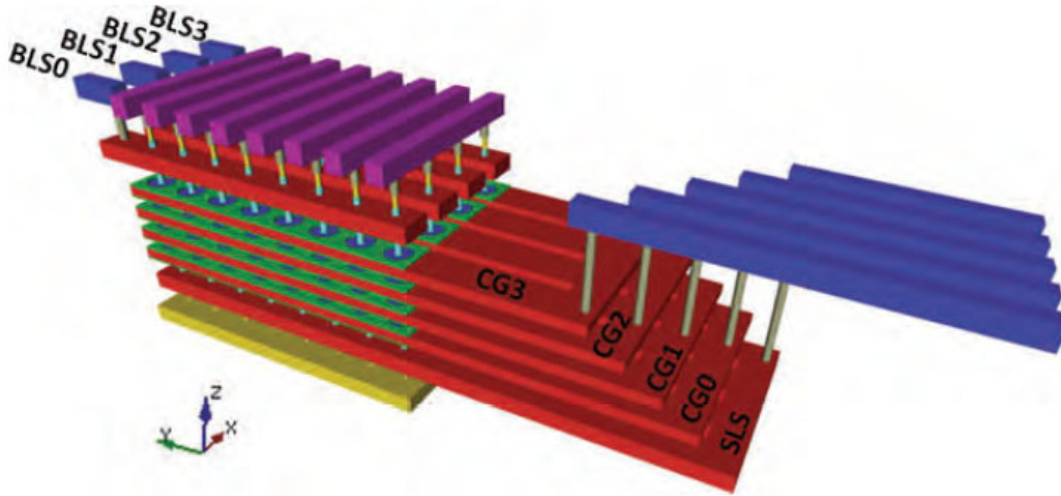


Fig. 5.20 C-FG NAND Flash array with fan-out

25. The word lines (CG0, CG1, CG2, and CG3) themselves need to be accessed externally to the memory device in order to control the memory. To enable such access, word lines can be “fanned out” in an area adjacent to the memory array ending in conductive portions similar to stair steps arranged in a staircase pattern, as shown above. Ex. 1012 at 134; ’838 patent at 5:34-43. That way, the word lines can then be separately accessed through vertical metal columns (tan) connecting the conductive steps electrically to external conductive

¹ My citations to Ex. 1002, Ex. 1011, and Ex. 1012 are to page numbers in captions added by the parties to the exhibits.

lines (blue). Ex. 1012 at 134. The metal columns are formed by first drilling channels, called “vias,” in the interlevel dielectric material covering the steps, then filling the vias with metal.

26. A potential problem with the staircase structure is the possibility of a device malfunction by way of a short-circuit “[a]s the demand for higher storage capacity continues to increase [and] the number of vertical levels of the staircase structures also increases.” *E.g.*, ’838 patent at 5:36-39. “As a result, when applying a BEOL process to form interconnects on the staircase structures, an upper portion of the staircase structures is exposed to the BEOL process for a longer period of time than a lower portion of the staircase structures. This differential in BEOL exposure time increases the process variation of the final 3D memory device, thus introducing challenges in balancing manufacturing yield and process complexity/cost.” ’838 patent at 5:39-46.

27. For example, when upper stair steps are exposed to a BEOL (Back End Of Line) process longer during the formation of the interconnects (vertical metal columns), there is a possibility of breaking through the stair step material and forming an interconnect that extends to one or more word lines lying underneath, thereby risking electrically shorting the word lines. One way to prevent this is to increase the thickness of each stair step, which however brings the step closer to the upper word line creating the potential for electrical

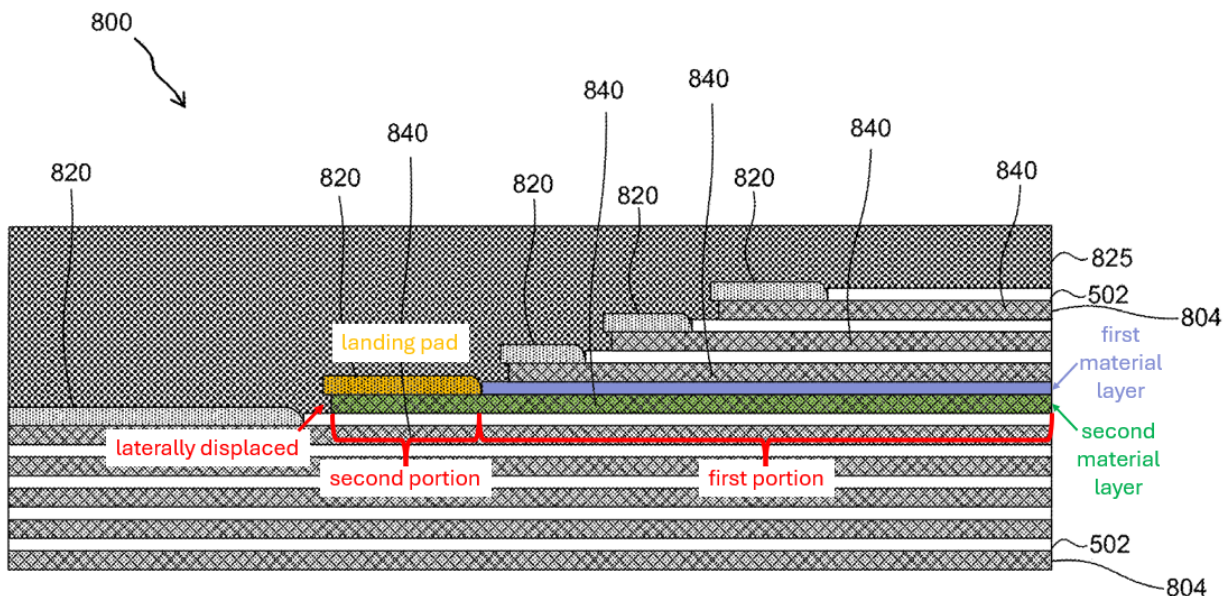
breakdown (i.e., a short-circuit), even in the presence of insulating material between the word lines.

28. The semiconductor process must account for this problem to ensure short-circuits do not occur. The process and structure disclosed in the '838 patent provides a way to address this problem.

VI. Overview of the '838 Patent

29. The '838 patent discloses a process for making “a staircase structure for a memory device” and claims specific structures. '838 patent at 1:39-43, 6:4-13:13, Figs. 1-9. Aside from Figure 9, the figures show cross-sectional views showing only the x-z plane. *See* '838 patent at Figs. 1-8 (showing axes labels). The structures formed by the process “provide numerous benefits including, but not limited to, yield and manufacturing cost improvements.” '838 patent at 1:43-45. A specific structure disclosed and claimed includes a “staircase structure [that] includes a plurality of layer stacks, where each layer stack includes a first material layer disposed over a first portion of a second material layer.” '838 patent at 1:47-50, Fig. 8. Further, “[t]he staircase structure further includes a plurality of landing pads respectively disposed on the plurality of layer stacks, where each landing pad is disposed over a second portion of the second material layer of a respective layer stack.” '838 patent at 1:50-54, Fig. 8. Additionally, “[e]ach of the landing pads is adjacent to a respective side of the first material

layer” and is laterally displaced from the end of the second material layer below it. ’838 patent at 1:54-57, Fig. 8. These features are shown in Figure 8, annotated below. The first material layer is shown in blue, the second material layer is shown in green, and the landing pad is shown in orange. The first portion of the second material layer and the second portion of the second material layer are labeled. As can be seen, the first portion and the second portion are distinct from one another. They are separate, non-overlapping portions of the second material layer. While not labeled, the lateral displacement of the left side of the landing pad can also be seen in the figure below, extending beyond the left side of the second material layer.

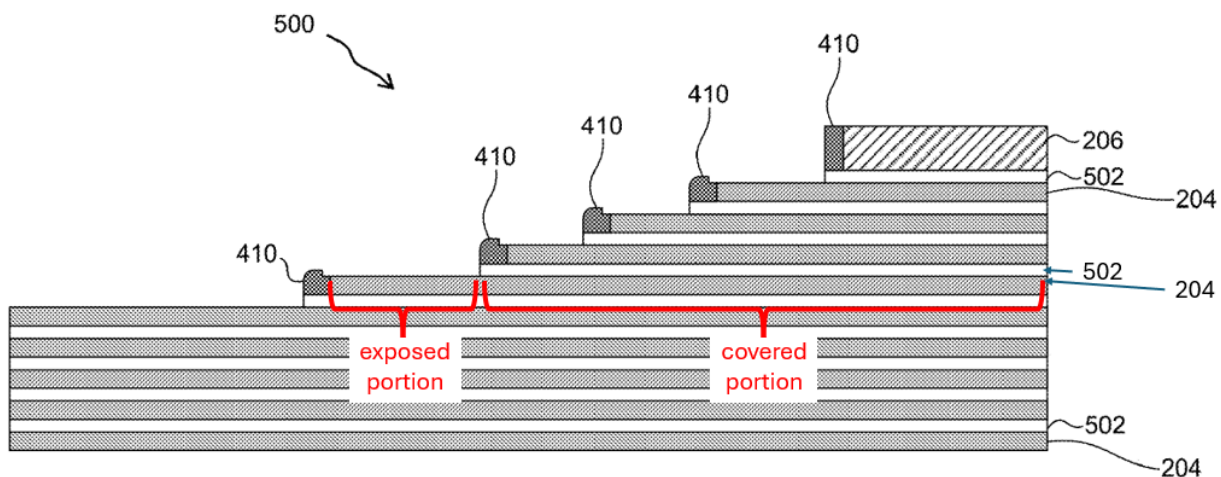


30. As described above, contacts must be formed to the word lines. In the '838 patent's structure, the landing pads are where the contacts are made by means of vertical metal columns (not shown). '838 patent at 1:50-54, 1:60-61, 9:42-61, Fig. 8. In the final memory device, the landing pad and the second material layer are made of conductive material or materials to form word lines, while the first material layer is made of insulating or dielectric material. '838 patent at 1:57-60, Fig. 8. The second material layer is also disposed over a first portion of the first material layer of an adjacent layer of the staircase structure while a second portion of the first material layer of the adjacent layer is laterally displaced from the second material layer (not annotated above). '838 patent at 1:66-2:1, Fig. 8.

31. The process of forming the structure is described throughout the specification using the accompanying figures. To form the structure, the process begins with an alternating layer stack formed over a substrate. '838 patent at 6:4-67, 10:61-11:28, Fig. 1. At this stage, the alternating layer stack includes a plurality of layers, with each layer having an insulating layer over a sacrificial layer. '838 patent at 6:4-67, 10:61-11:28, Fig. 1. The alternating layer stack is formed into a staircase structure by repeating an etch-trim process using a mask stack. '838 patent at 7:1-67, 11:29-12:8, Figs. 2A-2B. After stairs have been formed, spacers are formed at a side of each layer of the staircase by conformally

depositing a material on the staircase structure and then removing a portion of that material. '838 patent at 8:1-33, 12:9-28, Figs. 3-4.

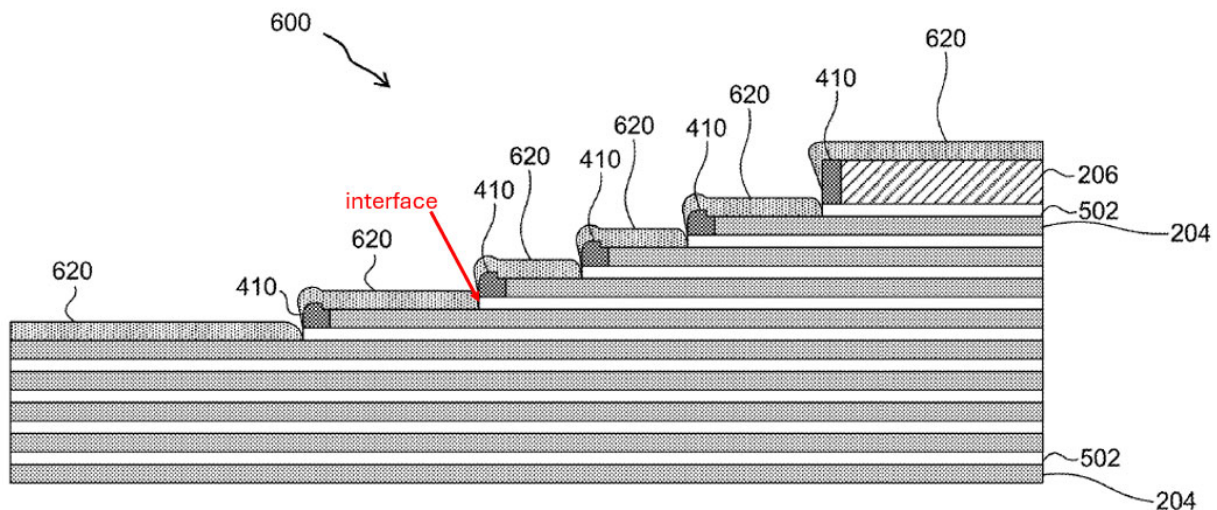
32. The exposed portion of the insulating layer of each step is then removed to expose a top portion of sacrificial layer underneath. '838 patent 8:34-45, 12:29-36, Fig. 5. Specifically, Figure 5 is described as “a cross-sectional view of a staircase structure 500 after removal of a portion of insulating layer 202.” '838 patent at 8:34-36. It goes on to explain that “each SC layer of staircase structure 500 exposes a portion of a top surface of sacrificial layer 204 and spacer 410 of each SC layer.” '838 patent at 8:41-44. This is shown below in annotated Figure 5, which annotates the exposed portion, the covered portion, and adds labels 502 and 204 to the annotated layer, consistent with the '838 patent's description.



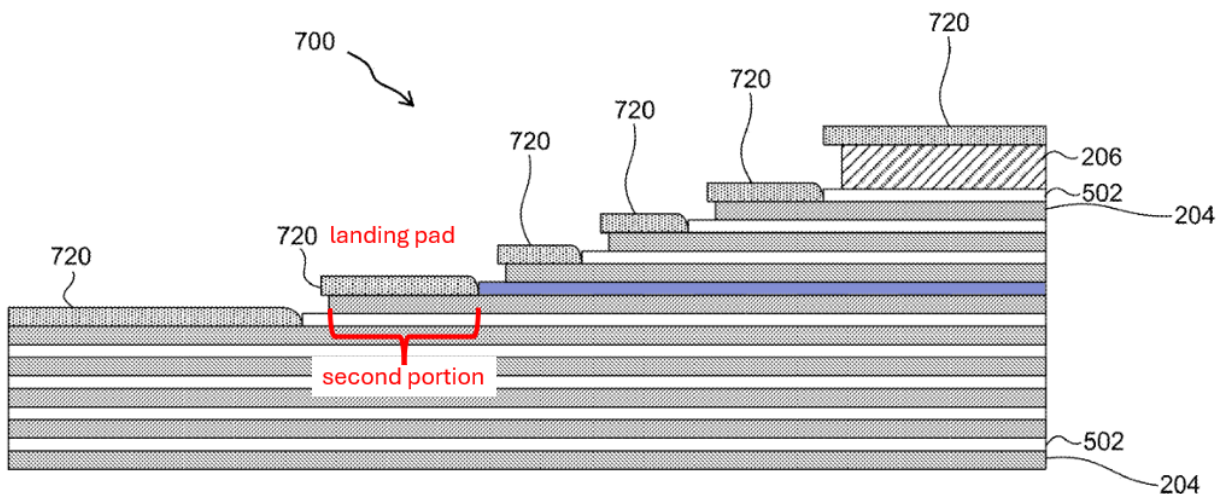
Compared to Figure 4, which depicts the previous step, it can be seen that any insulating material 502 (which was labeled 202 in Figure 4) that was not covered

(when looking down on the structure in the z-direction) extending along the x-direction to the spacers 410 is removed. This creates two distinct and separate portions of the sacrificial layer 204: (i) a first portion that is still covered by insulating material 502 and (ii) a second portion that is the exposed portion shown above. These parts of the sacrificial layer 204 are ultimately the “first portion” and “second portion” of the second material layer as claimed in claims 1 and 12 of the '838 patent.

33. A dielectric material is then deposited onto the staircase structure. '838 patent at 8:46-9:12, 12:37-49, Fig. 6. The '838 patent describes this as a deposition process and does not describe formation of the structures 620 depicted in Figure 6 as made or shaped by a lithographic process. This creates an interface between each of the structures 620 and a respective insulating material 502. This is shown below in annotated Figure 6.

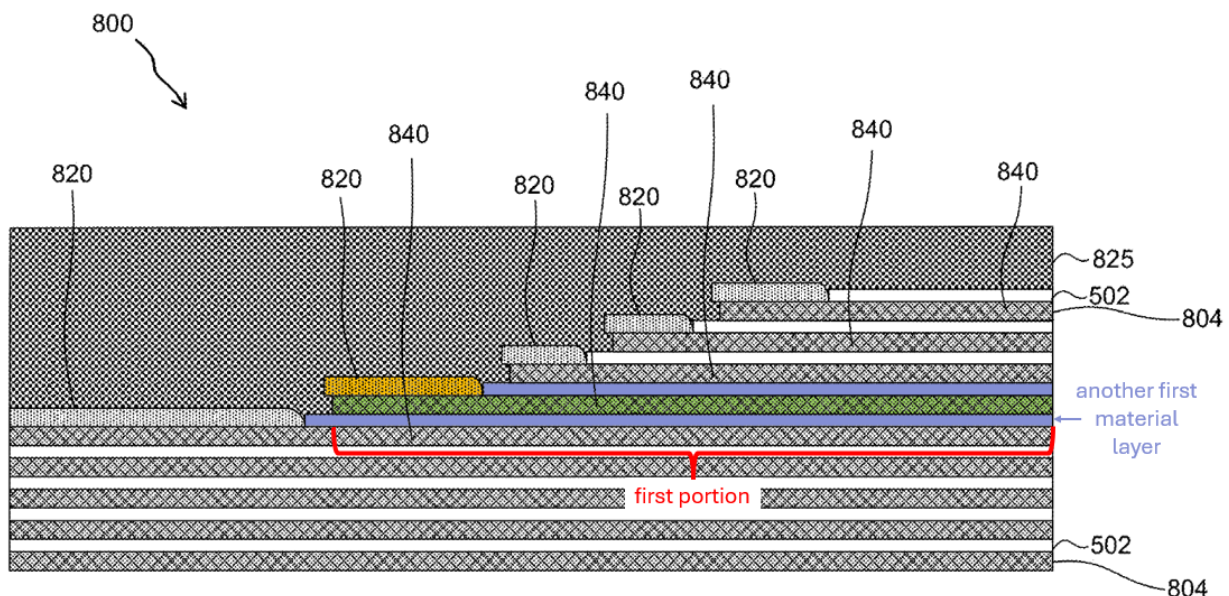


Then, the spacers 410 and a portion of the dielectric layer 620 are removed to form landing pads 720 such that landing pads 720 remain in contact with the sacrificial layer 204. '838 patent at 9:13-39, 12:50-62, Fig. 7. This is shown in annotated Figure 7 below. An insulating layer 502 is colored blue and the landing pad is identified over the “second portion” of the second material layer, which was the “exposed portion” discussed above, which terminates on one end at the interface between the landing pad and the insulating material 502. This is the “second portion” as claimed in claims 1 and 12.



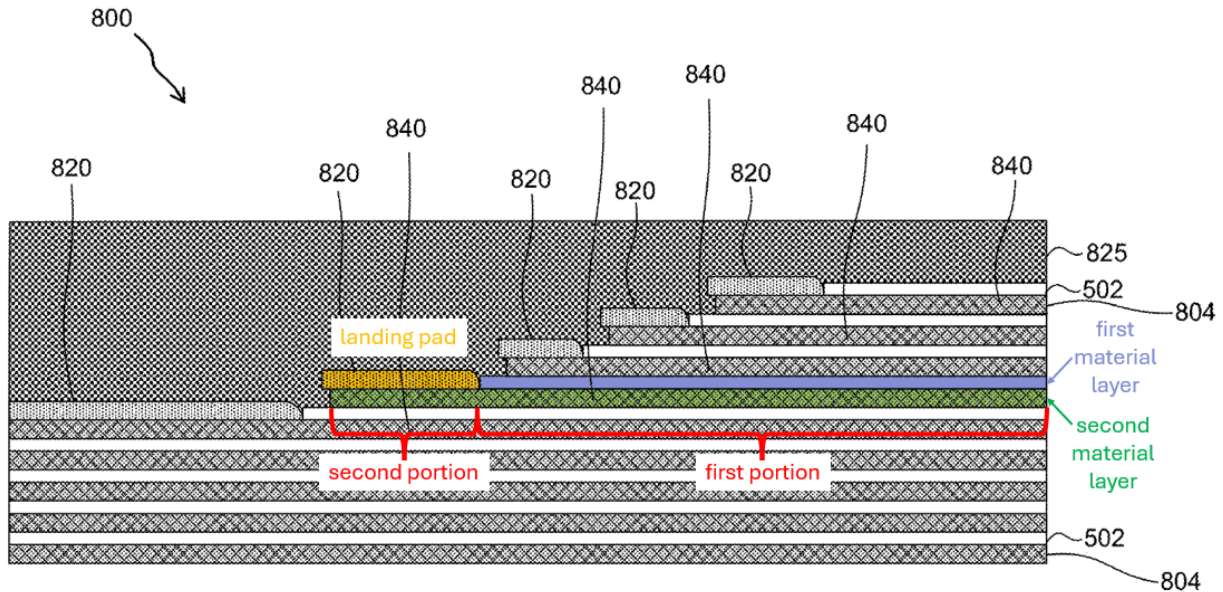
34. Then, an insulating dielectric layer is formed over the entire structure and word lines are formed in the staircase structure by removing the sacrificial layer and the remaining dielectric layer 620/landing pads 720 to form recesses and then filling the recesses with one or more conducting material layers. '838 patent at 9:40-10:48, 12:63-13:13, Fig. 8.

35. The specification also notes that “[b]oth landing pad 720 and sacrificial layer 204 of the SC layer are disposed over a portion of insulating layer 502 of another vertically adjacent SC layer.” ’838 patent at 9:21-24; *see also id.* at 1:66-2:1. This is shown in annotated Figure 8 below, where the “first portion” labeled is not of the second material layer, as in claims 1 and 12, but of the “another first material layer” as recited in claims 6 and 20, which is the lower blue layer.



36. At the end of this process, a structure is formed as depicted in Figure 8 below, in accordance with claims 1, 12, and dependent claims. The “first material layer,” annotated in blue, is over a “first portion” of the “second material layer,” annotated in green. The “landing pad,” annotated in orange, is over a “second portion” of the “second material layer.” As explained above, the process

described in the specification results in the “first portion” and the “second portion” being distinct, separate, and non-overlapping.



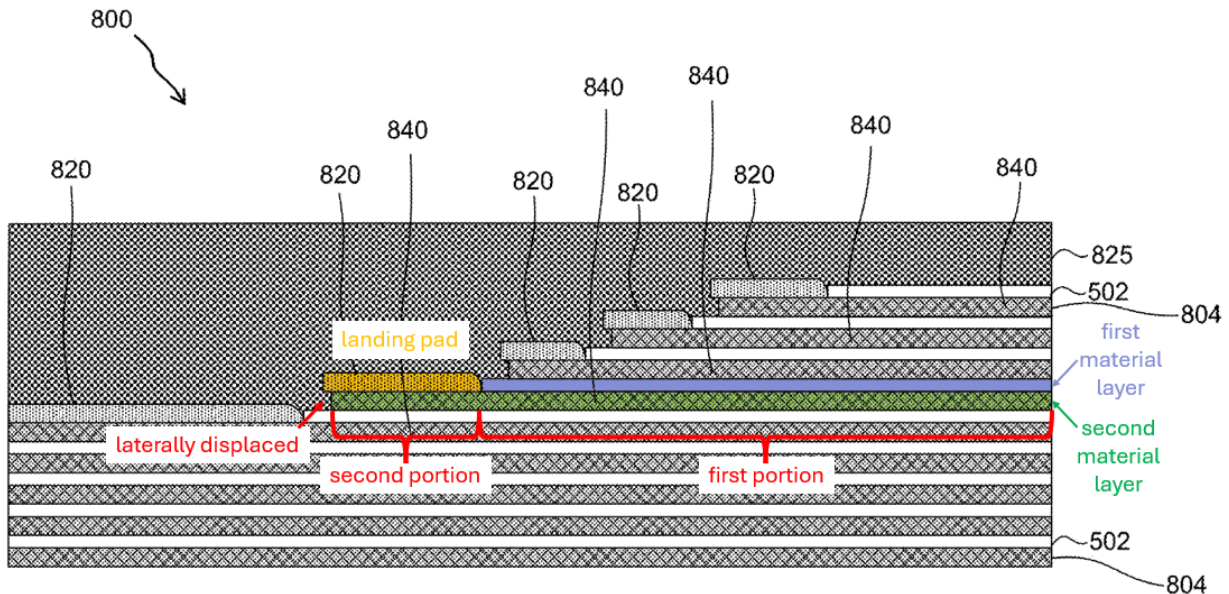
37. Figure 8 notes that it is depicting the x-z plane of the staircase structure. See '838 patent at Fig. 8. The y-axis is into and coming out of the page. To avoid confusion, I note that the axes in Figure 8 (and other figures of the '838 patent) are different from the axes in the figure from page 134 of Ex. 1012, discussed earlier in my declaration. In the '838 patent, the x-axis runs along the steps toward the memory cells, where as in the figure from page 134 of Ex. 1012 shown earlier, the x-axis runs along the steps, but perpendicular to the direction from the end of the steps toward the memory cells. In other words, the x-axis and y-axis are inverted when comparing the figures of the '838 patent and the figure from page 134 of Ex. 1012.

38. The Petition says that “the specification explains that the terms ‘on,’ ‘above,’ and ‘over’ ‘should be interpreted in the broadest manner such that ‘on’ not only means ‘directly on’ something, but also includes the meaning of ‘on’ something with an intermediate feature or a layer therebetween.” Pet. 20 (quoting ’838 patent at 4:4-12). That same part of the specification also states, “Moreover, ‘above’ or ‘over’ not only means ‘above’ or ‘over’ something, but can also include the meaning it is ‘above’ or ‘over’ something with no intermediate feature or layer therebetween (i.e., directly on something).” ’838 patent at 4:8-12. A POSITA would understand this to mean that, for example, feature 1 is over feature 2 regardless of whether feature 1 is directly on and in physical contact with feature 2, or is separated from feature 2 by an intermediate feature or layer.

VII. The Claimed Structural Arrangement

39. In relevant part, claims 1 and 12 both recite the following limitations: “a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and a landing pad disposed over a second portion of the second material layer, wherein the landing pad comprises a first side surface and a second side surface, and wherein the first side surface is in contact with the first material layer and the second side surface is laterally displaced from a side surface of the second

portion of the second material layer.” As explained in the previous section, the process described in the specification results in the “first portion” and the “second portion” being distinct, separate, and non-overlapping. Figure 8 of the '838 patent depicts the recited structure in this regard, as annotated below.

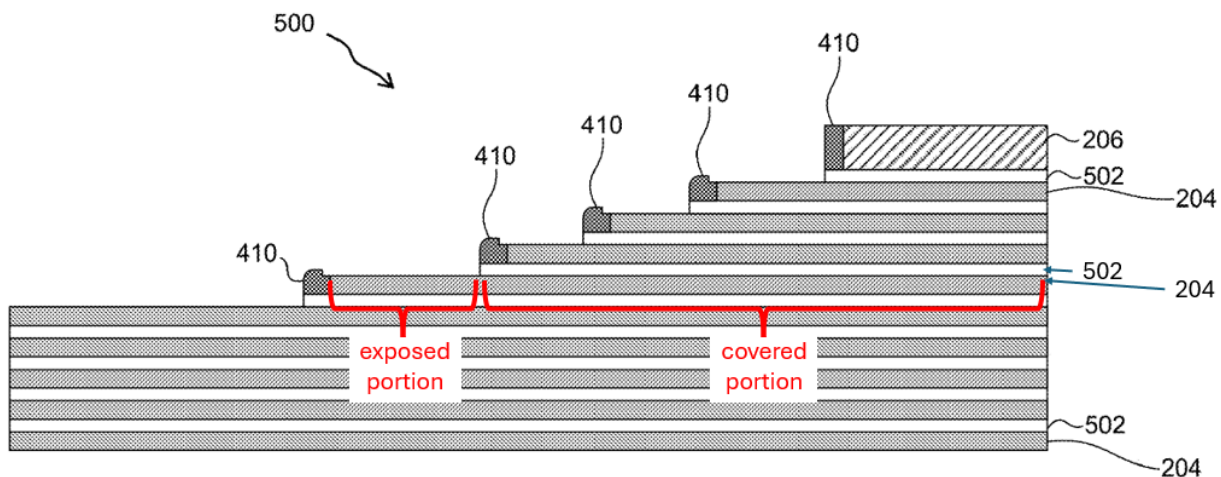


40. I note that the claims recite a “first portion,” and separately recite a “second portion,” which signifies to a POSITA that these are two distinct portions of the “second material layer.” For example, the claims do not use generic language regarding these portions, but instead they use ordinal language that signifies separateness. In addition to the labels “first” and “second,” the rest of the claimed structure reinforces this understanding because there are different structures over the distinct portions and a defined interface between those structures signifying the boundary between the first portion and the second

portion. Thus, the way the claims are written implies that the “first portion” is distinct and separate from, and not overlapping with the “second portion.”

Nothing in the claims suggests a different understanding.

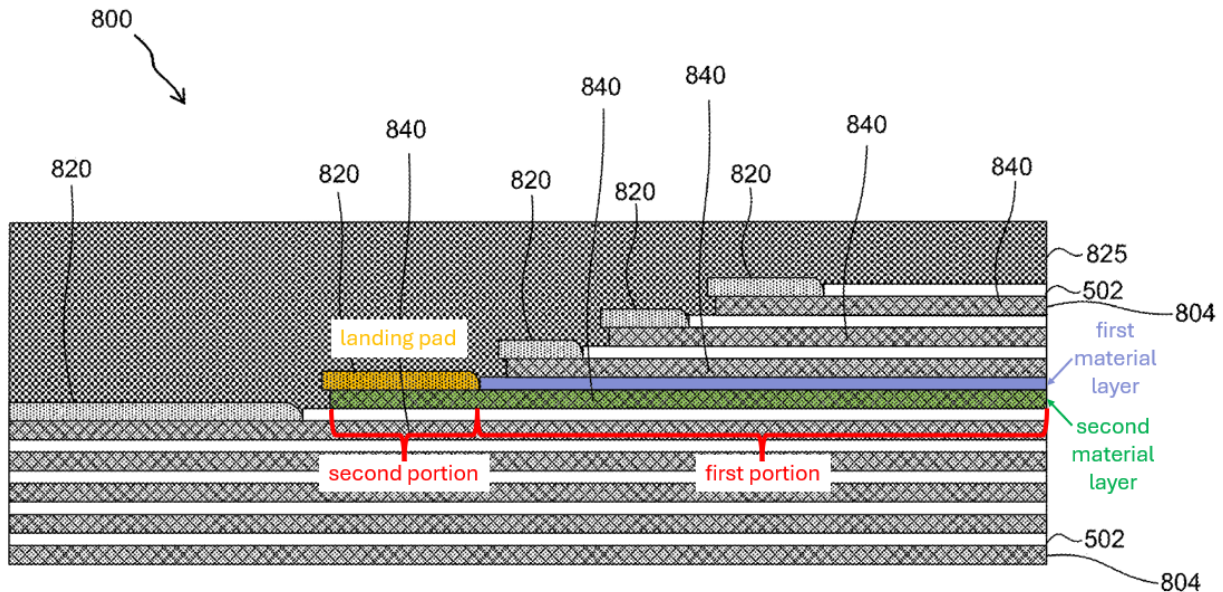
41. This is also consistent with the description of the claimed structures and their formation in the specification, which I detailed in the previous section. In particular, during the described process, an exposed portion of the insulating layer of each step is removed to expose a top portion of sacrificial layer underneath, as shown in annotated Figure 5 below. '838 patent 8:34-45, 12:29-36, Fig. 5.



This creates two distinct and separate portions of the sacrificial layer 204: (i) a first portion that is still covered by insulating material 502 and (ii) a second portion that is the exposed portion shown above. These two portions are separate, distinct, and non-overlapping for the entirety of their extents in the x-direction (left-right in the above figure and the other figures of the '838 patent).

These parts of the sacrificial layer 204 are ultimately the “first portion” and “second portion” of the second material layer as claimed in claims 1 and 12 of the '838 patent. As this ultimately results in distinct, separate, and non-overlapping “first portion” and “second portion” parts of the second material layer, this further confirms to a POSITA that the “first portion” and “second portion” in claims 1 and 12 are separate and distinct portions of the second material layer that do not overlap.

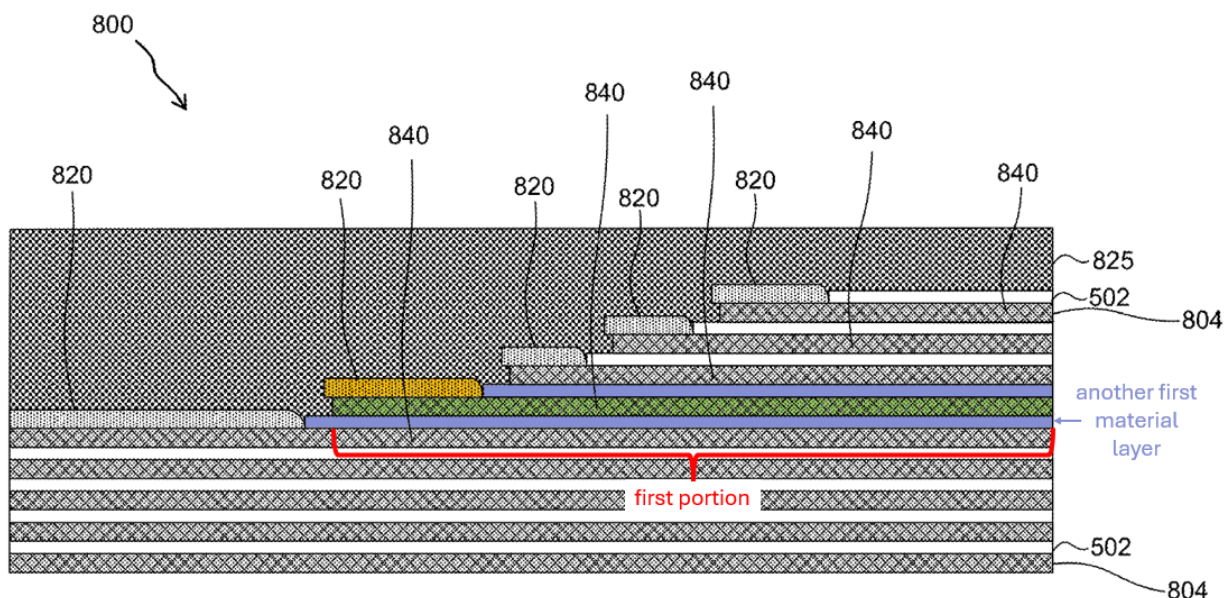
42. After further steps described in the previous section, landing pads are formed only over the previously exposed portion (now labeled “second portion”) of the sacrificial layer, as depicted in annotated Figure 7 below. Notably, the portion of the underlying layer 204 that the landing pad is formed over is distinct and separate from the portion over which the insulating layer 502, annotated in blue, is disposed. These correspond to the claimed “second portion” and “first portion” respectively, and with the interface of the landing pad 720 and the insulating layer 502 delineating the two portions underneath.



44. This is also how the patent itself describes the resulting structure.

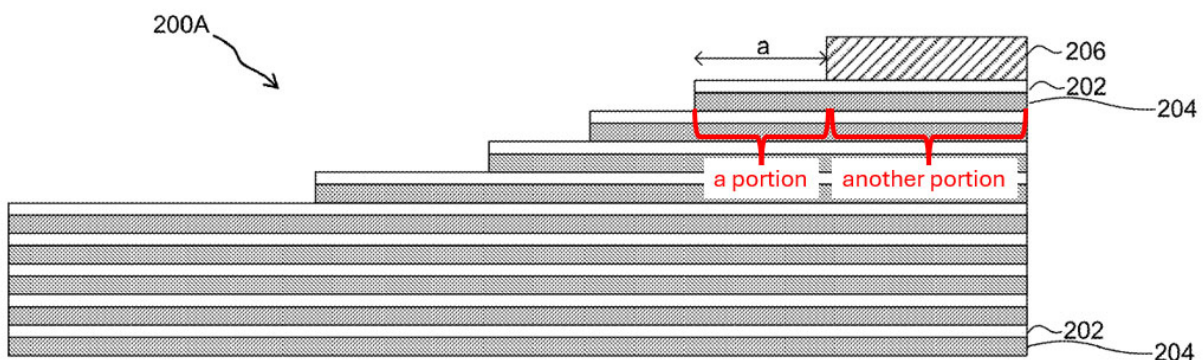
The specification explains that “[t]he staircase structure includes a plurality of layer stacks, where each layer stack includes a first material layer disposed *over a first portion* of the second material layer.” ’838 patent at 1:47-50 (emphasis added). That is one feature of the staircase structure. But the specification continues, stating that “[t]he staircase structure *further includes* a plurality of landing pads respectively disposed on the plurality of layer stacks, where each landing pad is disposed *over a second portion* of the second material layer of a respective layer stack.” ’838 patent at 1:50-54 (emphasis added). So, in addition to the “first portion,” the staircase structure “further includes” the “second portion.” This mirrors the claims, which also recite specifically identified portions of the “second material layer.”

45. A POSITA would also recognize a consistent usage of distinct “portions” of layers throughout the ’838 patent. Other claims, such as claims 6, 8, 9, 15, and 20 all discuss separate and distinct portions of layers. Claims 6 and 20 recite that “the second material layer is disposed over *a first portion* of another first material layer.” ’838 patent at 14:5-7, 15:17-19 (emphasis added). This is shown below in annotated Figure 8, with the “first portion” of the lower first material layer identified. A POSITA would understand the meaning of “first portion” in claims 6 and 20 consistent with the use of “first portion” and “second portion” in claims 1 and 12: that they refer to distinct portions of the referenced material layer. Thus, the second material layer, annotated in green below, is over a portion of the first material layer below it, annotated in blue, and is not over the entirety of the lower first material layer.



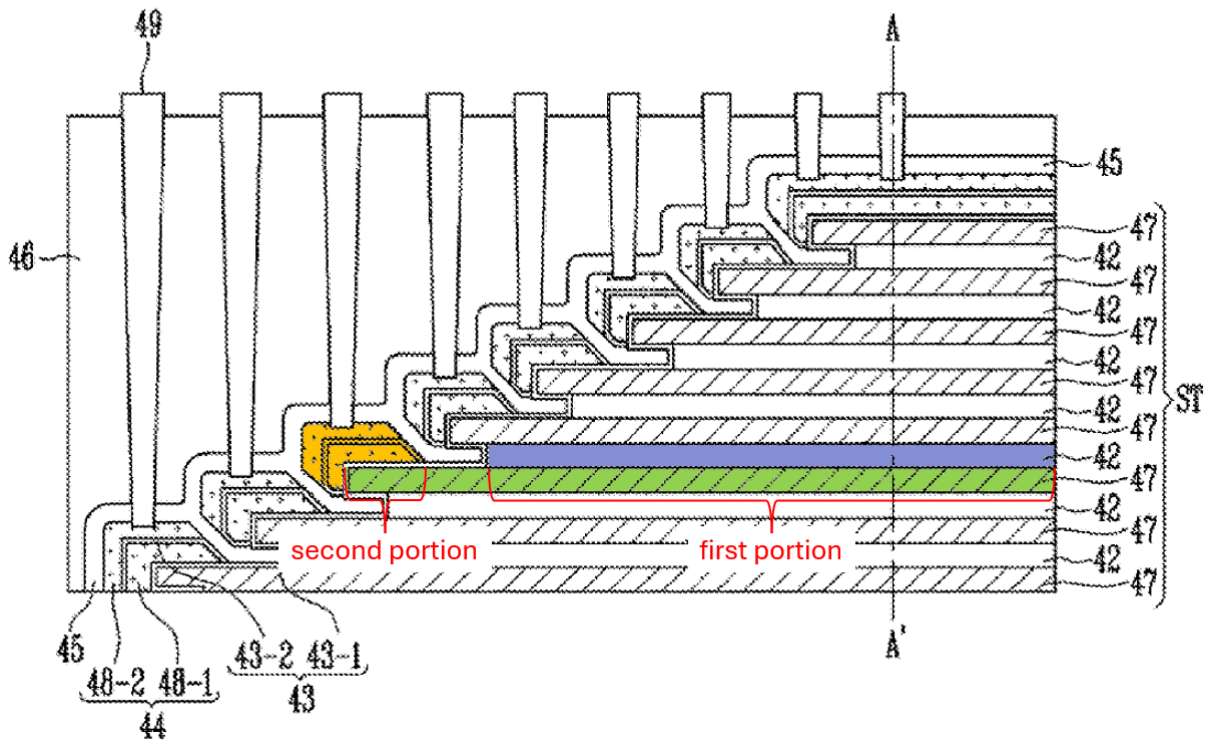
46. The specification describes this arrangement in a similar and consistent way. The specification states that “[w]ordline layer 804 of an SC layer is disposed over ***a portion*** of insulating layer 502 of another vertically adjacent SC layer.” ’838 patent at 9:53-55 (emphasis added); *see also id.* at 1:66-2:1, 9:21-24.

47. As another example, in describing a part of the process of forming the claimed structure, the specification describes that “***a portion*** of a top-most SC layer of staircase structure 200A is exposed and ***another portion*** of the top-most SC layer is covered by hard mask layer 206.” ’838 patent at 7:12-15 (emphasis added). The hard mask layer 206 is shown over the “another portion” while the “a portion” is exposed. This is shown in annotated Figure 2A below. Again, the patent describes two distinct and non-overlapping portions of the structure with an extension in the x-direction. This would also signal to a POSITA that that is the correct understanding of “first portion” and “second portion” in claims 1 and 12.

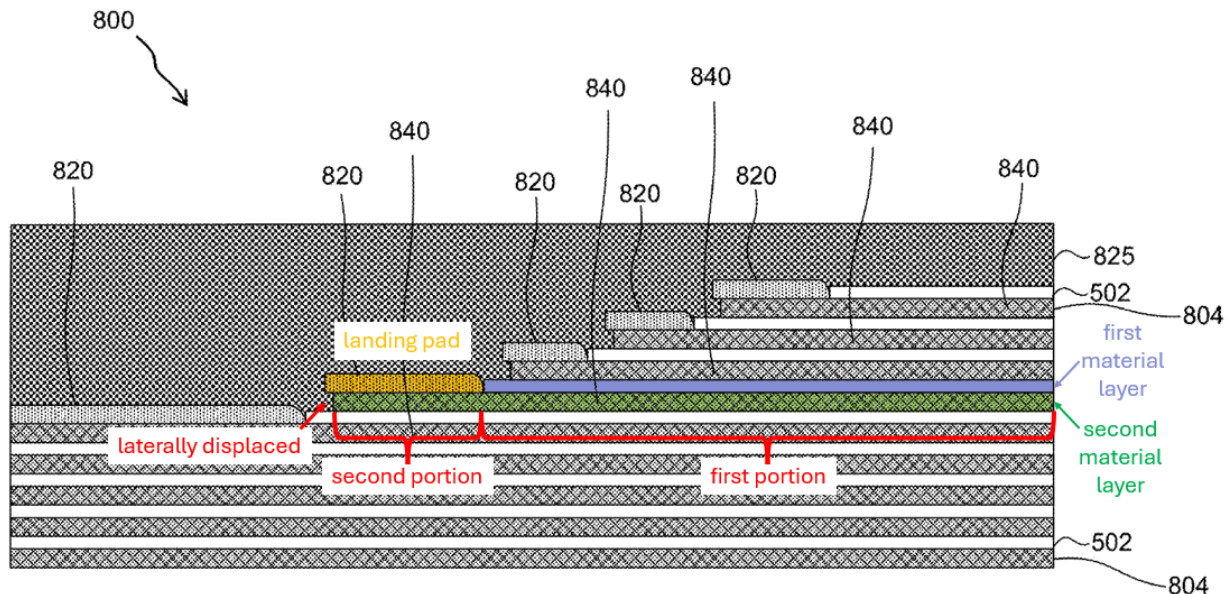


48. I have also reviewed the file history of the '838 patent in Ex. 1002. When originally filed, claim 1 was similar to issued claims 1 and 12 in the sense that it recited an arrangement between the first material layer, the landing pad, and first and second portions of the second material layer. Ex. 1002 at 39. The originally-filed claim 1 was initially rejected as anticipated by US 2016/02180107 ("Lee-107" (Ex. 1014)). Ex. 1002 at 153-54. The examiner relied on Figure 4C of Lee-107, which is annotated below. The annotations show how the examiner applied the structure shown below against the originally-filed claim 1. Importantly, the examiner identified the structures of the prior art such that there were distinct, separate, and non-overlapping "first portion" and "second portion" of the second material layer, annotated in green below. Thus, a POSITA would understand that the examiner understood the claims such that the "first portion" and the "second portion" were distinct and separate from each other.

FIG. 4C



49. Thus, in light of the above and the description of the process in the previous section, in my opinion, a POSITA would understand claims 1 and 12 to be consistent with the annotated Figure 8 below, including that the “first portion” and “second portion” have their plain and ordinary meaning of distinct and separate portions of the “second material layer” that do not overlap.



VIII. Ground 1: Claims 1 and 12 Are Not Obvious In View of Kim

A. Overview of Kim (Ex. 1005)

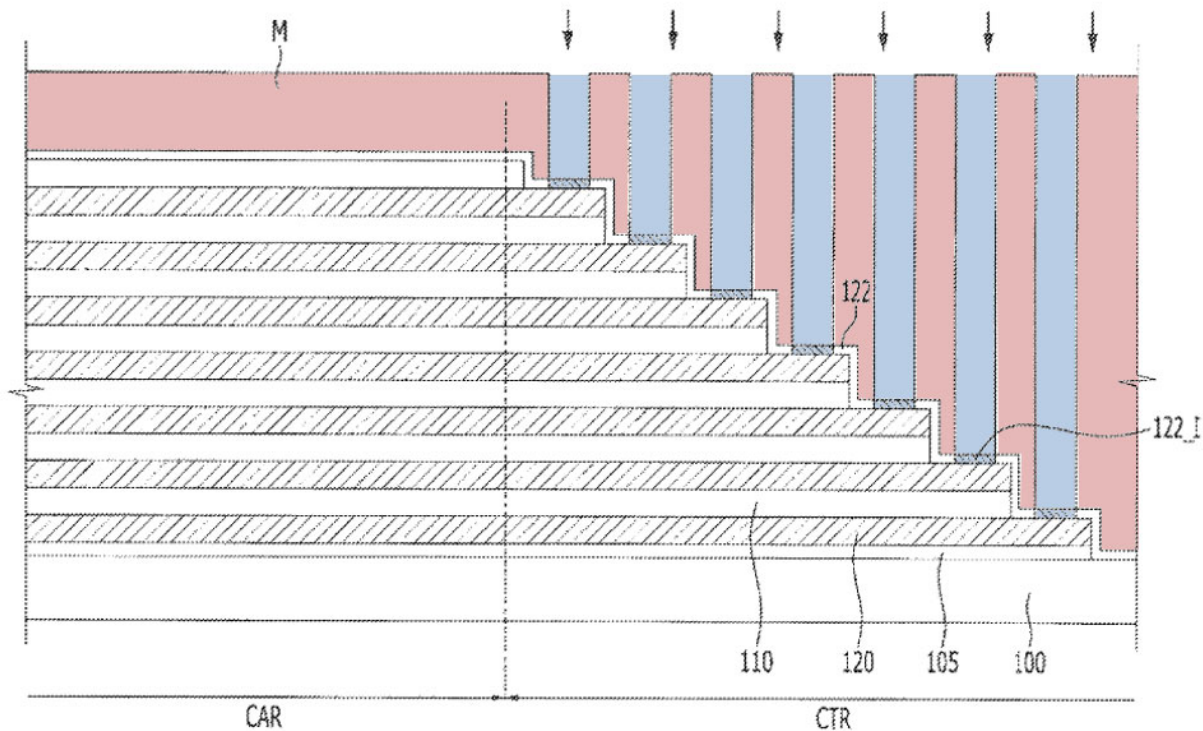
50. Kim describes 3D semiconductor memory devices with a “stepwise” “stacking structure” in the contact region. Kim at 1:13-35, 1:40-53, Fig. 4B. “Ones of the plurality of gate electrodes, may include a respective pad unit that comprises a step of the stepwise structure. At least one of the pad units may include a base pad and a protrusion pad on the base pad.” Kim at 1:47-50. The pad units are where contact plugs are formed for electrical connection to word lines in upper layers. Kim at 9:64-10:4, Fig. 4B. Kim describes the process by which its complete stepwise stacking structure is formed, including the pad units. Steps described include the formation of the memory cells, but I omit those details here to focus on the contact region.

51. A set of alternating layers of insulating layers 110 and sacrificial layers 120 are formed on a lower insulating layer 105. Kim at 12:20-25, Fig. 10. The stepwise structure is formed by using a mask pattern to etch some material, then the mask pattern itself is etched so that more of the alternating layer structure is exposed and etched further. This process is repeated until the stepwise structure is formed. Kim at 12:43-56, Fig. 11. An auxiliary insulating layer 122 is then formed over the stepwise structure conformally covering the top and side surfaces of the stepwise structure. Kim at 9:12-20, 12:57-60, Fig. 11.

52. A photosensitive resin pattern M is then formed on the structure over the auxiliary insulating layer 122. Kim at 12:61-67, Fig. 12. The photosensitive resin pattern M is formed so that predetermined regions of auxiliary insulating layer 122 are exposed. Kim at 12:61-67, Fig. 12. The predetermined regions are referred to as region 122_I, and are for forming the protrusion pad. Kim at 12:61-67, Fig. 12. To better show this, in the figure below, I have colored in light blue the openings made in photosensitive resin pattern M, extending all the way down to and including the corresponding exposed regions 122_I. The portion in pink is the solid photosensitive resin pattern M that remains in place during this step. Once the openings are made, predetermined ions are injected from above, as indicated by the arrows. The ions can travel freely only in the openings made in the photosensitive resin pattern M and are thus able to reach

the exposed regions 122_I of the auxiliary insulating layer only at these locations. Through this process, the regions 122_I become “doped region[s]” and therefore have a different etching ratio as compared to the rest of the auxiliary insulating layer 122 that was not exposed to the ions through the mask pattern but remained covered by the solid portion of the mask pattern (pink below) and thus it was not injected with ions. Kim at 12:61-13:11, Fig. 12. A POSITA would understand this from these disclosures in Kim.

FIG. 12



53. After the ion injection, remaining material of the mask pattern (pink above) is removed and an insulating layer 125 is placed over the stepwise structure. Kim at 13:12-20, Fig. 13. Thereafter, the sacrificial layers 120 can be

removed. As a POSITA would understand from Kim, because the regions 122_I have the different etching ratio compared to the rest of auxiliary insulating layer 122, the regions 122_I can be removed either together with the sacrificial layers 120 or separately, such that there is an opening in the auxiliary insulating layer 122 only at those implanted locations termed openings 122_O in Kim. Kim at 13:51-67, Fig. 16.

54. The area where the sacrificial layers 120 were and the openings 122_O, which Kim refers to as “gaps 260,” are then filled with conductive material to form gate electrodes 300. Kim at 13:55-67, 14:6-7. Kim refers to the area defined by the openings 122_O and subsequently filled by conductive material as the “protrusion pad PAD_P.”

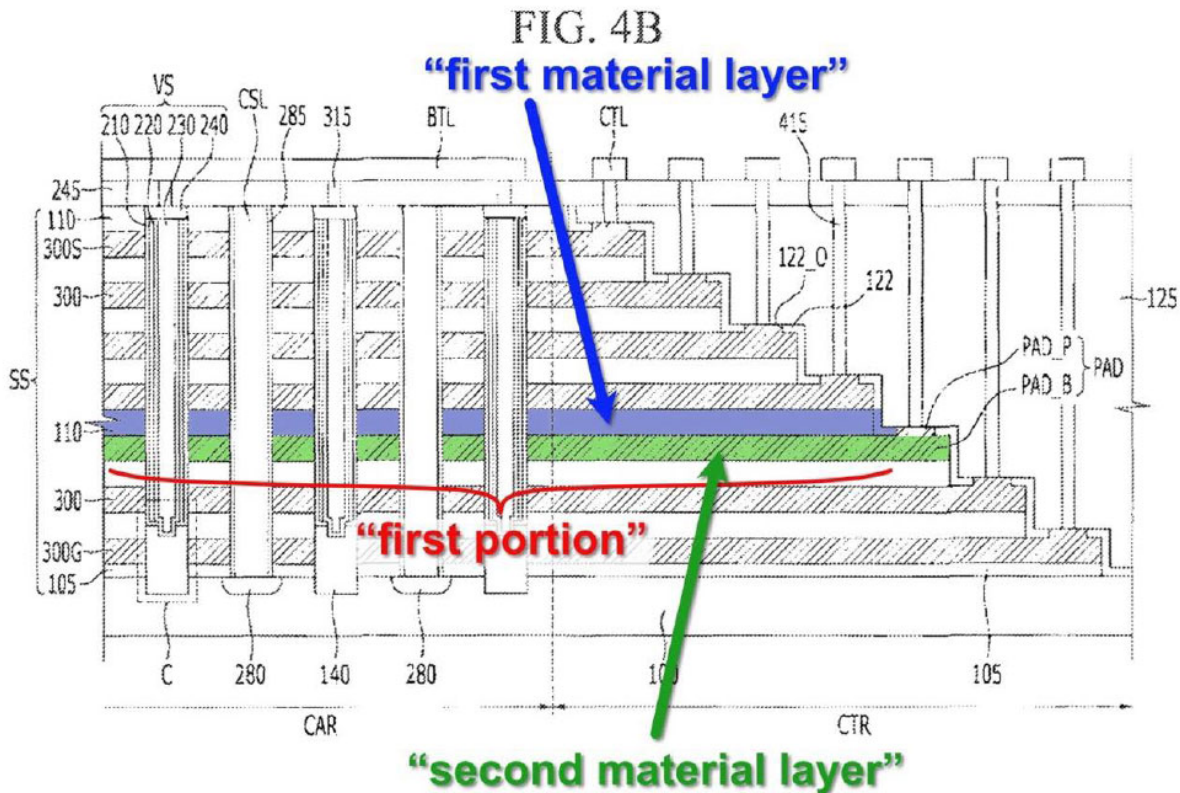
B. Petitioner’s Expert Misunderstands or Misrepresents Kim and Kim’s Mapping to Claims 1 and 12 and Does Not Show Obviousness

55. I have reviewed Petitioner’s expert’s mapping of Kim to the limitations of claims 1 and 12 of the ’838 patent. *See* Ex. 1003 ¶¶ 144-202. In his analysis, Petitioner’s expert relies only on Figures 4B and 6 of Kim. *See id.* The Petition then relies on the same annotated Figures 4B and 6. *See* Pet. 27-38.

56. Petitioner’s expert states that “Kim’s insulating layer 110 and the adjacent portion of auxiliary insulation layer 122 together constitute the claimed ‘first material layer.’” Ex. 1003 ¶154 (emphasis removed); *see also id.* ¶160. He

also states that “the gate electrode 300” is the “second material layer.” *Id.* ¶167.

He uses the figure below to illustrate his opinions:



57. Petitioner’s expert labels a “first portion” that extends along the second material layer, annotated in green, to where his first material layer, annotated in blue, (mistakenly) ends at the PAD_P.² As noted above, Petitioner’s

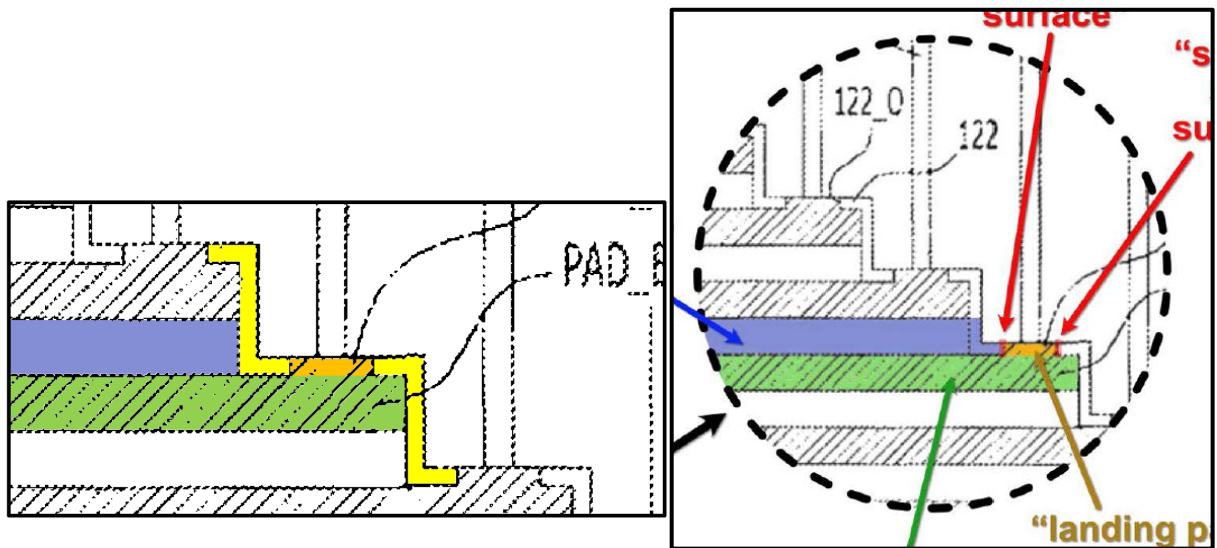
² Petitioner’s expert has identified the “first portion” as extending through both the CAR and CTR regions of Kim’s stacking structure in Kim Figure 4B.

However, Kim explains that these are not contiguous in one direction: “FIG. 4B is a cross-sectional view taken along line b-b’ of FIG. 4A.” Kim at 5:27-28. The

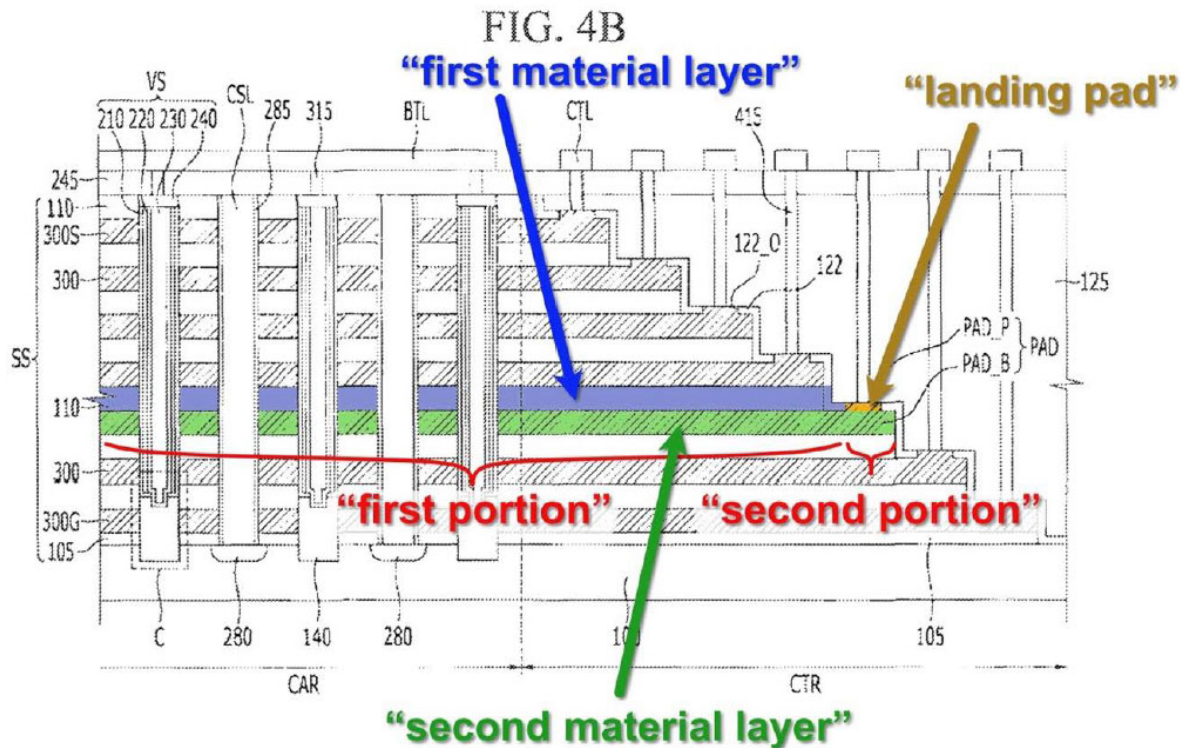
expert asserts that, for purposes of mapping Kim to the claims of the '838 patent, that “Kim’s insulating layer 110 **and** the adjacent portion of auxiliary insulation layer 122 **together** constitute the claimed ‘first material layer.’” Ex. 1003 ¶154 (emphasis modified). To illustrate his opinion, the figure below on the left annotates Kim’s layer 110 in blue, Kim’s gate electrode 300 in green, Kim’s PAD_P in orange, and Kim’s auxiliary layer 122 in yellow, following the descriptions of these structures in Kim. *See* Kim at 5:53-55, 6:15-19, 7:50-8:10, 9:12-20, Fig. 4B. The figure below on the right is a cropped version of the figure from paragraph 182 of Petitioner’s expert’s declaration. *See* Ex. 1003 ¶ 182. As can be seen, Petitioner’s expert colors in blue just part of the auxiliary layer seen in yellow on the left. Notably, he does not include any other part of the yellow auxiliary layer, but does not explain why. In my opinion, this is incorrect and is

line b-b’ in Figure 4A is not straight, but instead extends from b in the y-direction, and then makes a 90 degree turn to extend in the x-direction to b’. *See* Kim at Fig. 4A. Thus, the CAR and CTR regions depicted in Kim Figure 4B extend in the y-direction and x-direction respectively. In this way, Petitioner’s expert’s labeling of figures is confusing. Regardless, I disagree with his analysis as explained herein, but note this because it also indicates that Petitioner’s expert may not fully understand or appreciate what is described in Kim.

an arbitrary label flawed by hindsight, as I explain further below after discussing Petitioner's expert's opinions first.

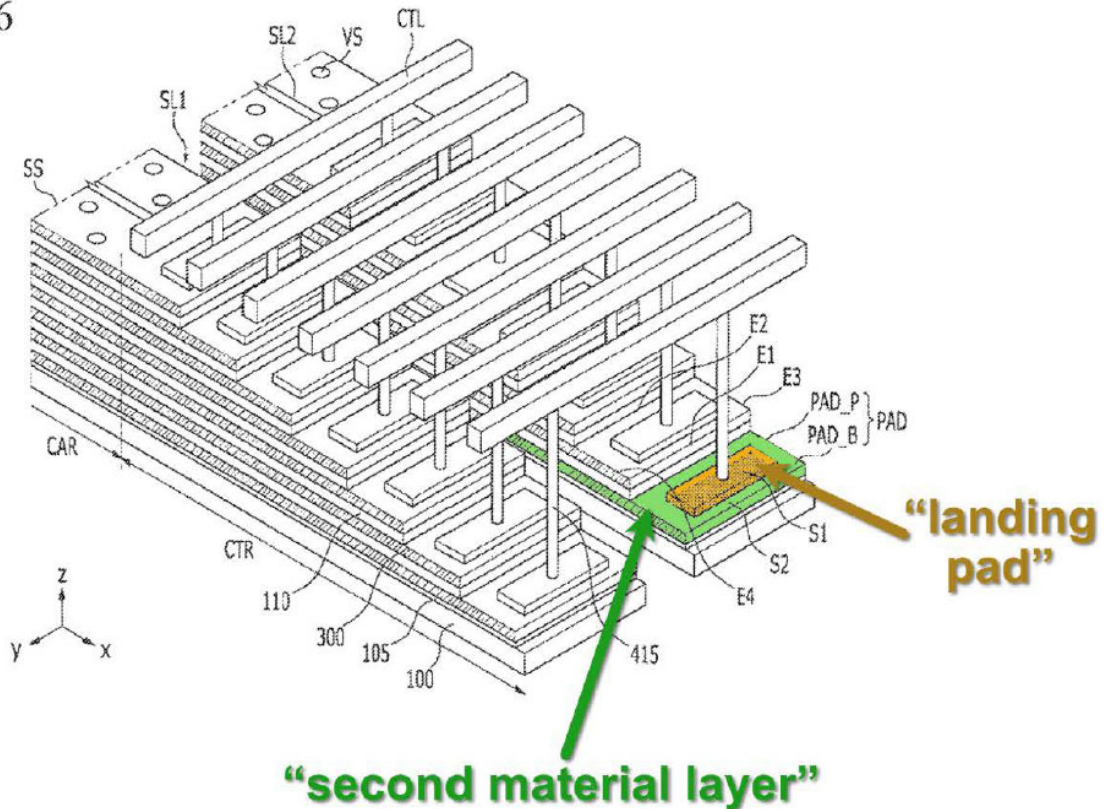


58. Continuing with Petitioner's expert's opinions, he provides the below figure where he maps Kim's PAD_P to the claimed landing pad. Ex. 1003 ¶ 175. He provides a "second portion" label, but does not explain why it is the claimed "second portion" or how it relates to the rest of Kim's structure. Again, it is just an arbitrary label driven by hindsight.



59. Furthermore, in describing the PAD_P “landing pad,” Petitioner’s expert makes clear that he relies on a PAD_P where “the shape of this protrusion pad” “has an ‘island shape.’” Ex. 1003 ¶ 180. He further explains that “Kim teaches a protrusion pad PAD_P that is smaller than the conductive layer on which it sits and thus has sides that are offset from the sides of that conductive layer.” Ex. 1003 ¶ 192. Because Kim’s Figure 4B only shows the CTR region in the x-z plane, *see* Kim at 2:39-42, 5:22-28, 5:58-67, 6:15-19, Fig. 4A, Fig. 4B, Petitioner’s expert points to Kim Figure 6 as showing the PAD_P used in his opinions, *see* Ex. 1003 ¶¶ 193-194. His annotated Figure 6 is shown below.

FIG. 6

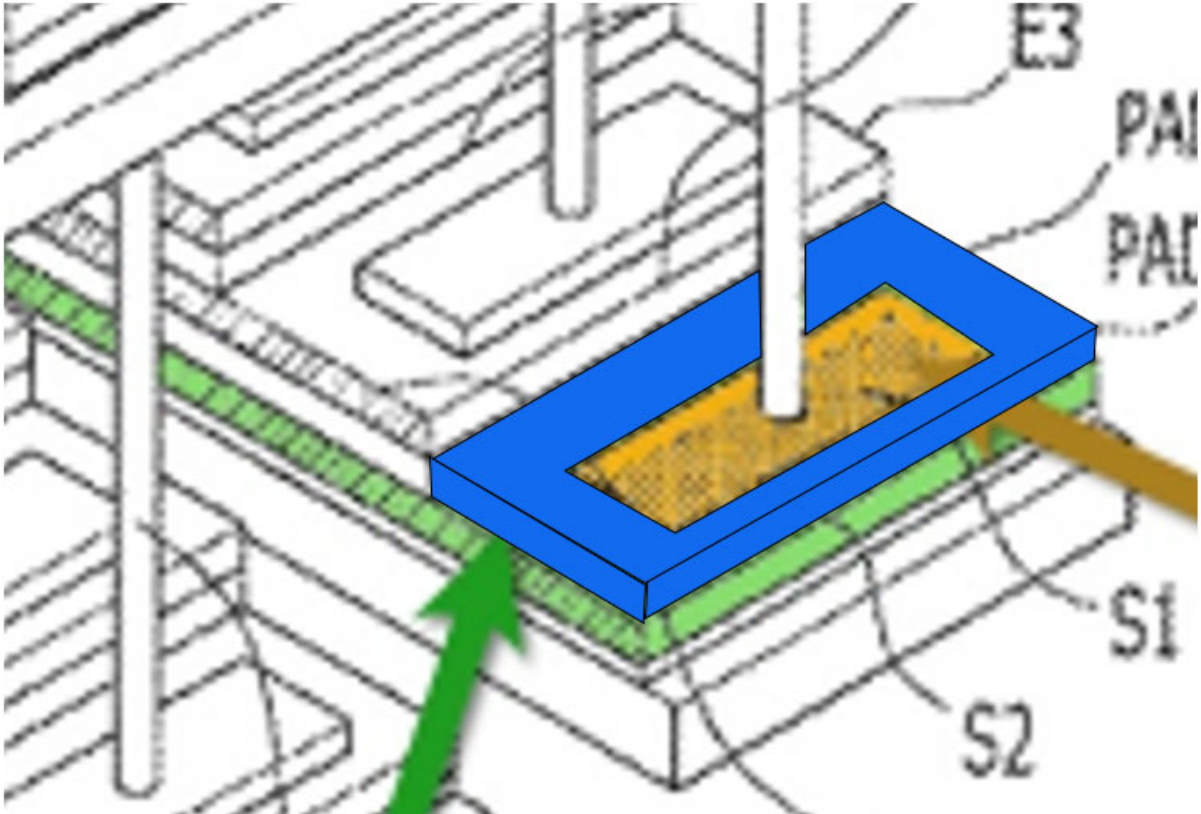


With the Figure 6 three-dimensional figure, one can see the “island shape” that Petitioner’s expert described as offset from the sides of the conductive structure beneath it (the green second material layer that he has annotated).

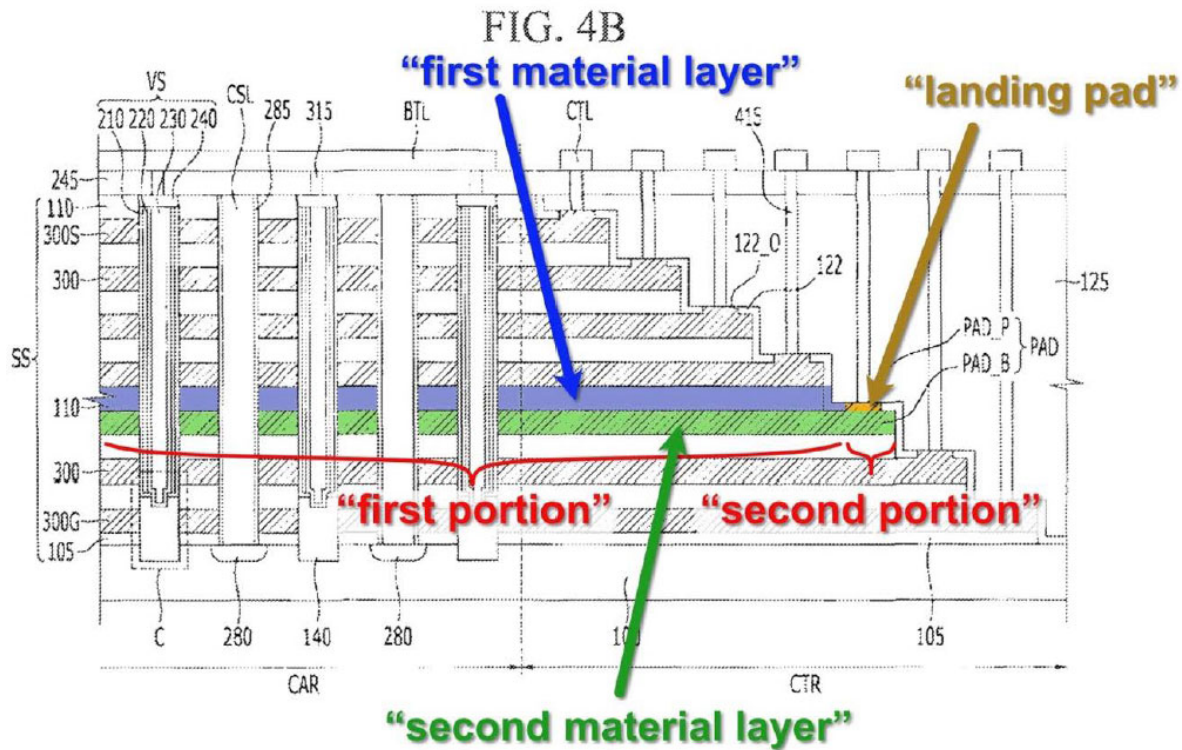
60. Petitioner’s expert continues to rely on the island shaped PAD_P in his opinions about dependent claims, albeit with different shapes. *See* Ex. 1003 ¶ 263. Assuming, without necessarily agreeing, that the shapes shown in paragraph 263 of Petitioner’s expert’s declaration are feasible, those shapes and the island PAD_P shown in the annotated Figure 6 above are formed by shaping the openings in the photosensitive resin pattern M that I described above in Paragraph 52. As I explained there, the openings in the photosensitive resin

pattern M allow for the auxiliary insulating layer 122 to be injected with ions so that the part of the auxiliary insulating layer 122 that was exposed in the openings of the photosensitive resin pattern M are the locations of the PAD_P when formed. *See supra* Paragraphs 52-54. Petitioner's expert acknowledges this when he states that "auxiliary layer 122 is applied ***before*** Kim's contact pads are formed. In particular, after 'the plurality of insulating layers 110' are 'patterned in the stepwise structure in the contact region CTR,' then the auxiliary insulating layer 122: is 'formed thereon.'" Ex. 1003 ¶ 157. A POSITA would understand from Kim's description that, aside from the opening 122_O, the rest of auxiliary insulating layer 122 remains in Kim's final structure, as it is described as in place when "buried insulating layer 125" is placed over the top of the entire structure and "covering the auxiliary insulating layer 122." *See* Kim at 9:12-63, Fig. 4B. For this same reason, a POSITA would understand that, while Kim's Figure 6 above does not show auxiliary insulating layer 122, it would be there. Kim explicitly states, in describing Figure 6, that "[t]he auxiliary insulating layer 122 may contact the second region S2 of the surface of the base pad PAD_B and the side of the base pad PAD_B in the contact region CTR." Kim at 10:49-51. As shown in Figure 6 above, "S2" is the region on top of the identified second material layer, annotated in green, that surrounds the island PAD_P.

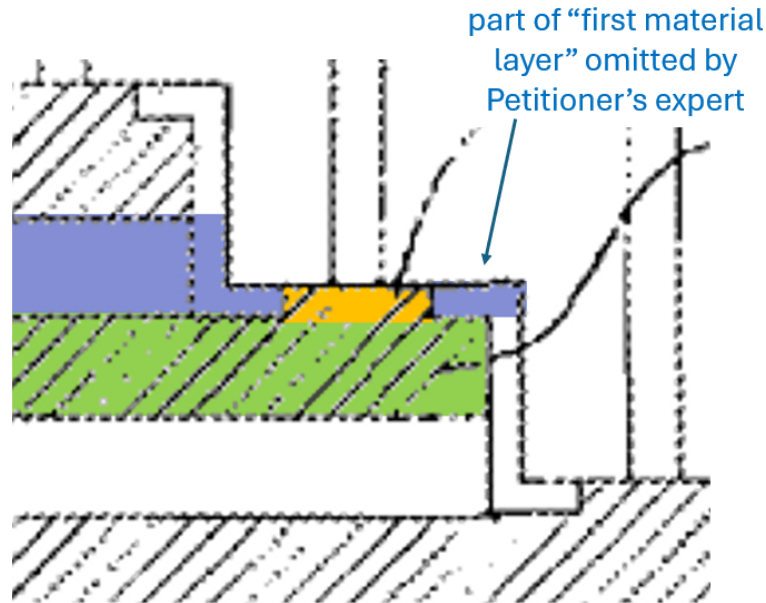
61. Thus, from Kim's explicit teachings, a POSITA would understand that auxiliary insulating layer 122 would be present and surround the PAD_P in Kim's Figure 6. This is shown in the figure below, which takes Petitioner's expert's annotated Figure 6, zooms in to the step, and annotates the auxiliary insulating layer 122 that surrounds the PAD_P. The illustration below just shows the auxiliary insulating layer 122 (blue) that surrounds the PAD_P, but a POSITA would understand that the auxiliary insulating layer 122 follows the path of the stairs and covers all the stairs, as shown in the figure on the left below Paragraph 57 above. Petitioner's expert states that "because layers 110 and 122 are formed from the same material such that they 'form one structure' as Kim itself states." Ex. 1003 ¶ 160. Assuming that is what is understood by a POSITA, then a POSITA would understand that one structure is formed all the way around the PAD_P.



62. As can be seen in Petitioner's expert's annotated figures, such as the one reproduced below, he does not account for the fact that the auxiliary insulating layer 122 surrounds the PAD_P. Instead, he simply ignores the auxiliary layer 122 on the other side of the PAD_P, assumedly because of the hindsight need to label the "first portion" and "second portion" of the second material layer as he does below.

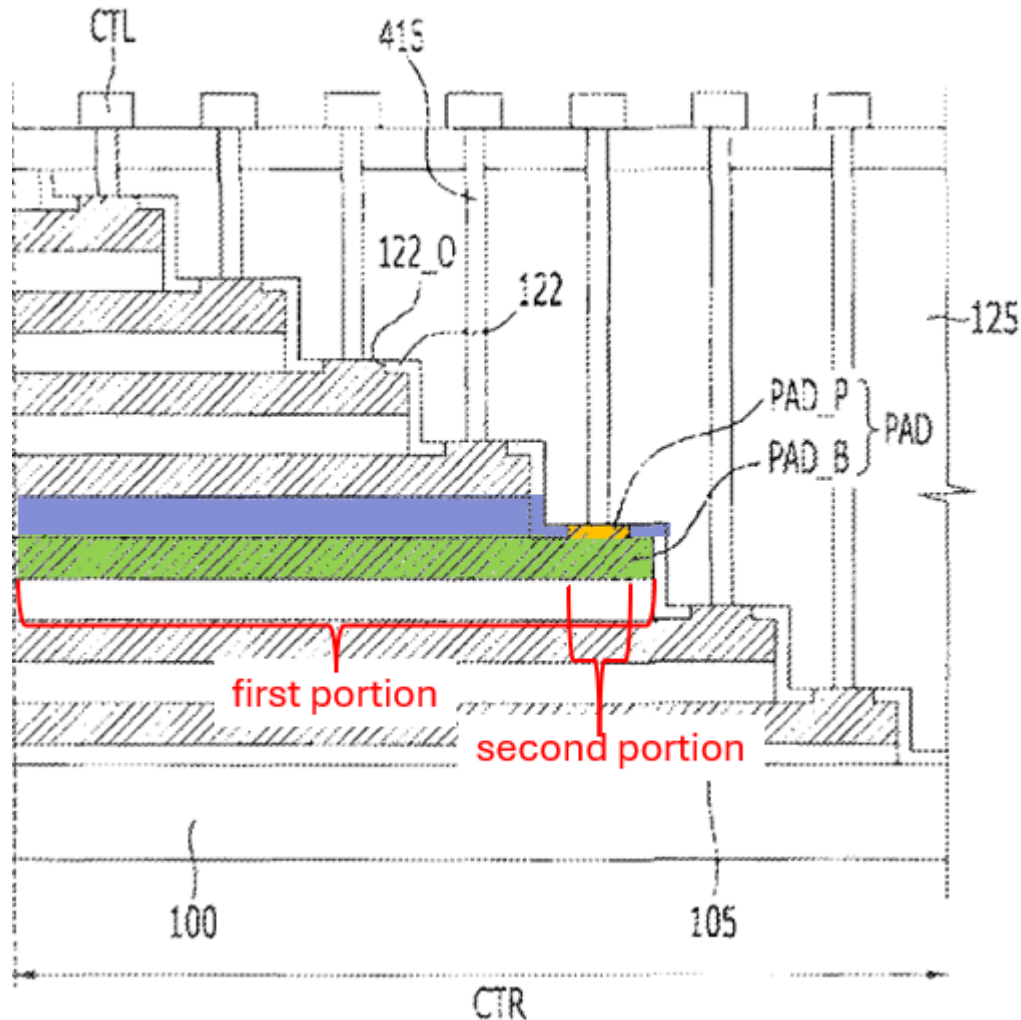


63. The figure below is a zoomed in, cropped version of Kim’s Figure 4B, annotated similarly to the above figure from Petitioner’s expert, except the auxiliary layer 122 on the right side of the PAD_P, which is connected and contiguous with the portion on the left side for the reasons already explained, is also annotated in blue. Petitioner’s expert incorrectly omits this part of auxiliary insulating layer 122 from his analysis and annotated figures without any explanation.



64. Properly identifying the full extent of the first material layer, rather than just arbitrarily picking a hindsight-driven partial extent, the first material layer, annotated in blue, extends across the entire second material layer, annotated in green, which is labeled “first portion” in the figure below. As can be seen, this overlaps with what Petitioner’s expert identifies as the “second portion” in his figure that is between Paragraphs 62 and 63 above. But in three dimensions, the “second portion” below is only under the PAD_P (assuming that can satisfy the “second portion” limitation). Because the first material layer completely surrounds the island shaped landing pad, the “second portion of the second material layer” is also an island shaped portion underneath the landing pad. With the first material layer completely surrounding the landing pad, the interface between the first material layer and the landing pad is on all sides of the

landing pad. That interface also defines the boundary between the “first portion” and the “second portion” of the second material layer below.



65. By ignoring Kim’s express teachings, Petitioner’s expert’s labels are entirely arbitrary and hindsight-driven. As claims 1 and 12 require, there is a correspondence between the “first material layer” and the “first portion of the second material layer.” Likewise, there is a correspondence between the “landing pad” and the “second portion of the second material layer.” Thus, in light of Kim’s teachings, the “second portion” is an island shaped portion in the

second material layer just below the PAD_P landing pad. But an island shaped “second portion” does not render claims 1 and 12 obvious because it does not show “the second side surface [of the landing pad] is laterally displaced from a side surface of the second portion of the second material layer” as required. Instead, they are coterminous when viewed from above and there is no lateral displacement.

66. Thus, in my opinion, claims 1 and 12 are not obvious in view of Kim as argued by Petitioner’s expert. As the remainder of Ground 1 discusses dependent claims, obviousness of those claims also has not been shown.

IX. Ground 3: Claims 1 and 12 Are Not Obvious In View of Lee

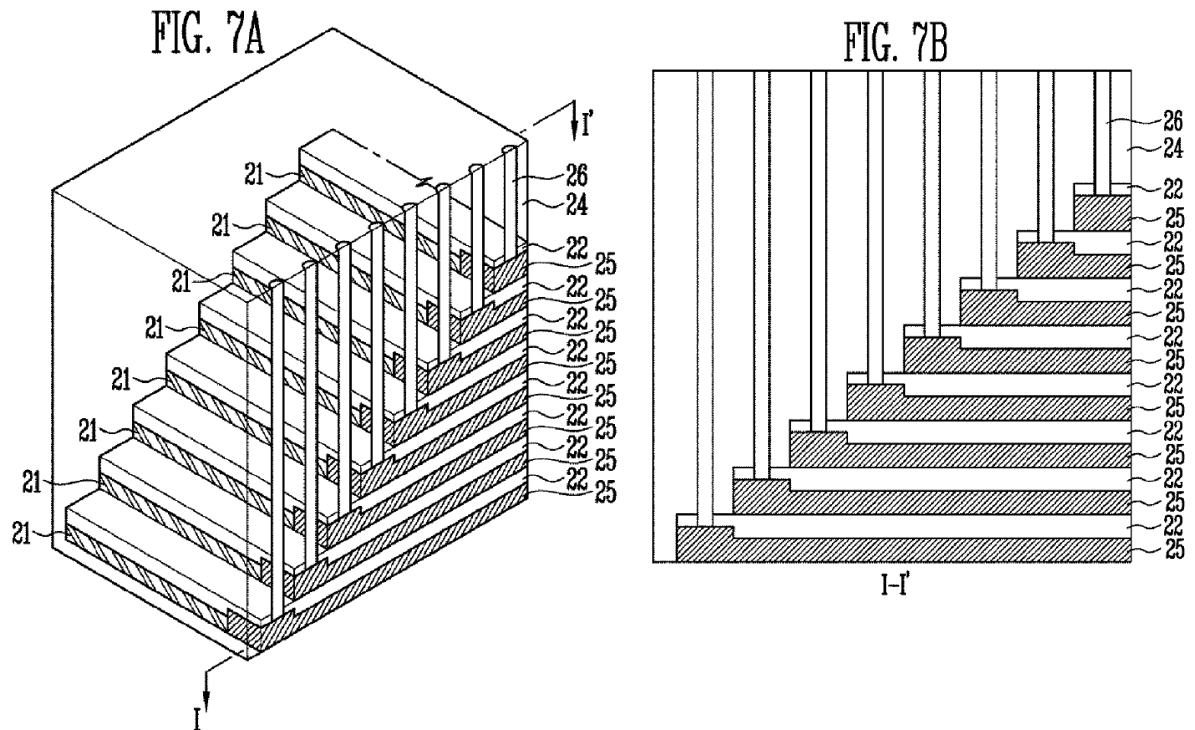
A. Overview of Lee (Ex. 1006)

67. Lee describes 3D semiconductor memory devices with “a plurality of stacked structures is patterned stepwise” in the contact region. Lee at [0005]-[0006], [0009]-[0010]. The conductive parts of the stepwise structure are described as having “a pad structure,” and where the conductive parts are not covered by the layer above, the “pad portions have a greater thickness than unexposed portions of the plurality of first conductive layers.” Lee at [0009]. The pad portions are where “contact plugs” make electrical connections to conductive word lines. Lee at [0006], [0042], Figs. 7A-7B.

68. A set of alternating layers of “first material layers 21” and “second material layers 22” are formed. Lee at [0029], Figs. 2A-2B. The “first material layers 21” may be a sacrificial layer to start. Lee at [0030]-[0031]. The “second material layers 22” are insulating layers. Lee at [0030]. I note that “first” and “second” layers in Lee are reversed in name compared to those in claims 1 and 12 as described in the '838 patent. These are then “patterned stepwise.” Lee at [0032], Figs. 2A-2B.

69. Impurities are then implanted into the exposed portions of second material layers 22 of the stacked structure. Lee at [0034]-[0035], Figs. 3A-3B. Then, recessed regions are formed by removing part of the first material layers 21 by first forming an interlayer insulating layer 24 over the structure, and then introducing an etchant through a slit formed in the stacked structures. Lee at [0036], Figs. 4A-4B. “As illustrated in FIGS. 5A and 5B, the thickness of ends of the recessed regions RC may be increased. For example, the second material layers 22 exposed by the recessed regions RC may be etched to a predetermined thickness by using a wet etch process. Since an etch rate of the impurity region 23 is higher than that of a region implanted with no impurities, an etch amount of the impurity region 23 may be greater than that of a non-implanted region. Therefore, the ends of the recessed regions RC may be extended.” Lee at [0038], Figs. 5A-5B.

70. Subsequently, conductive layers 25 are formed in the recessed regions. Lee at [0040], Figs. 6A-6B. “As a result, the conductive layers 25 may be formed in which the pad portions PAD exposed at the end of the stacked structure ST may have a greater thickness than unexposed portions of the conductive layers 25.” Lee at [0041]. Then, contact holes can be formed through the interlayer insulating layer 24 to expose the pad portions PAD, which holes then can be filled with a conductive material to become contact plugs 26 to the pad portions PAD. Lee at [0042], Figs. 7A-7B. Lee Figures 7A and 7B are reproduced below. As can be seen, in Lee’s structure, the insulating “second material layers 22” extend over the entirety of the conductive layers 25 below on each step. The contact plugs 26 are formed through the insulating “second material layers 22” to reach the pad portions PAD of the conductive layers 25 beneath.



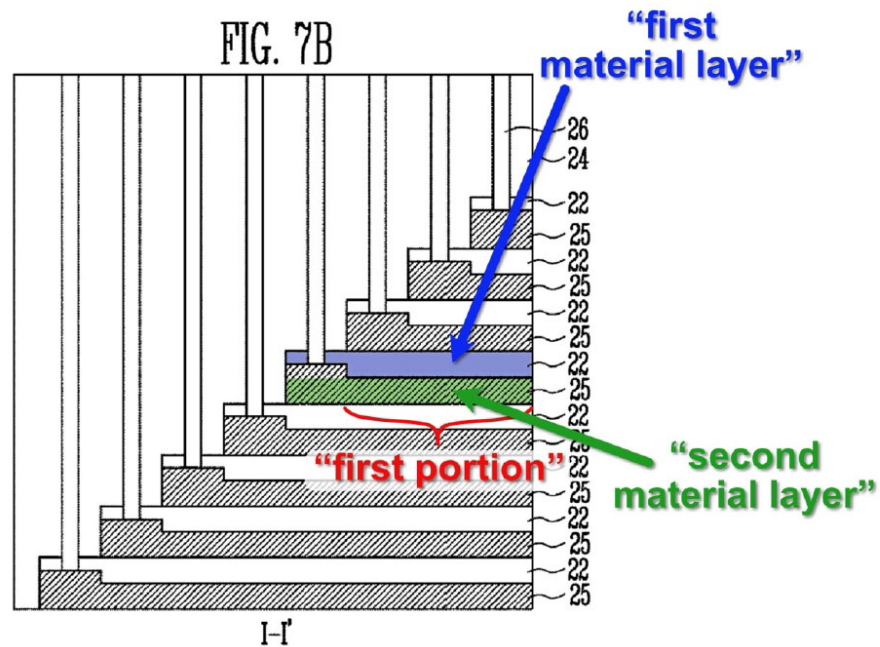
71. Other embodiments are also described, including some relied on by Petitioner's expert. But they are not germane to the discussion below, so I have omitted those details here.

B. Petitioner's Expert Does Not Show Obviousness of Claims 1 and 12 in View of Lee

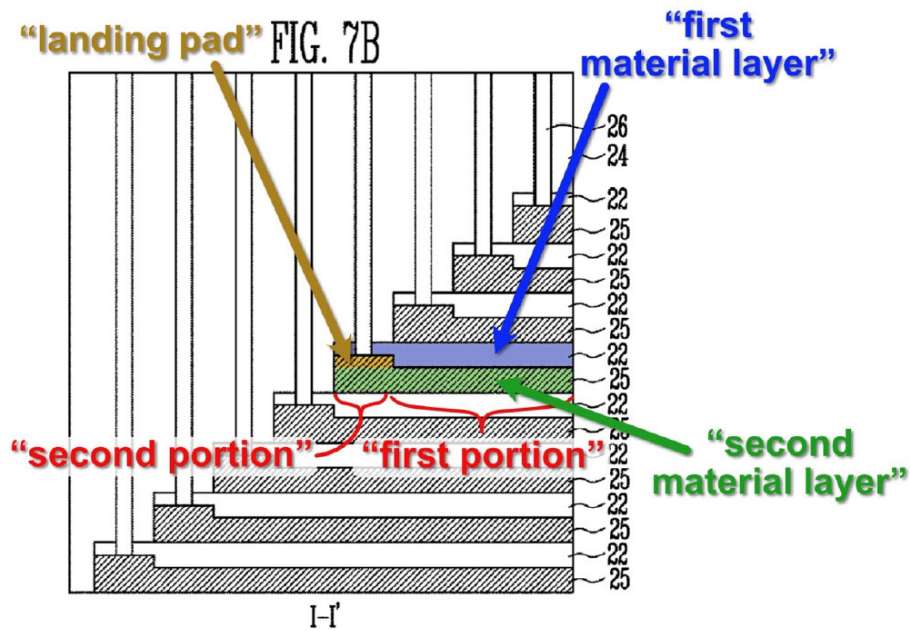
72. I have reviewed Petitioner's expert's mapping of Lee to the limitations of claims 1 and 12 of the '838 patent, and specifically the mapping to the claimed "first material layer," "landing pad," "second material layer," and the "first portion" and "second portion" of the "second material layer." *See* Ex. 1003 ¶¶ 348-393. As explained in Sections VI and VII above, claims 1 and 12 of the '838 patent describe a specific arrangement and relationship between the "first

material layer,” the “landing pad,” and first and second portions of the “second material layer.”

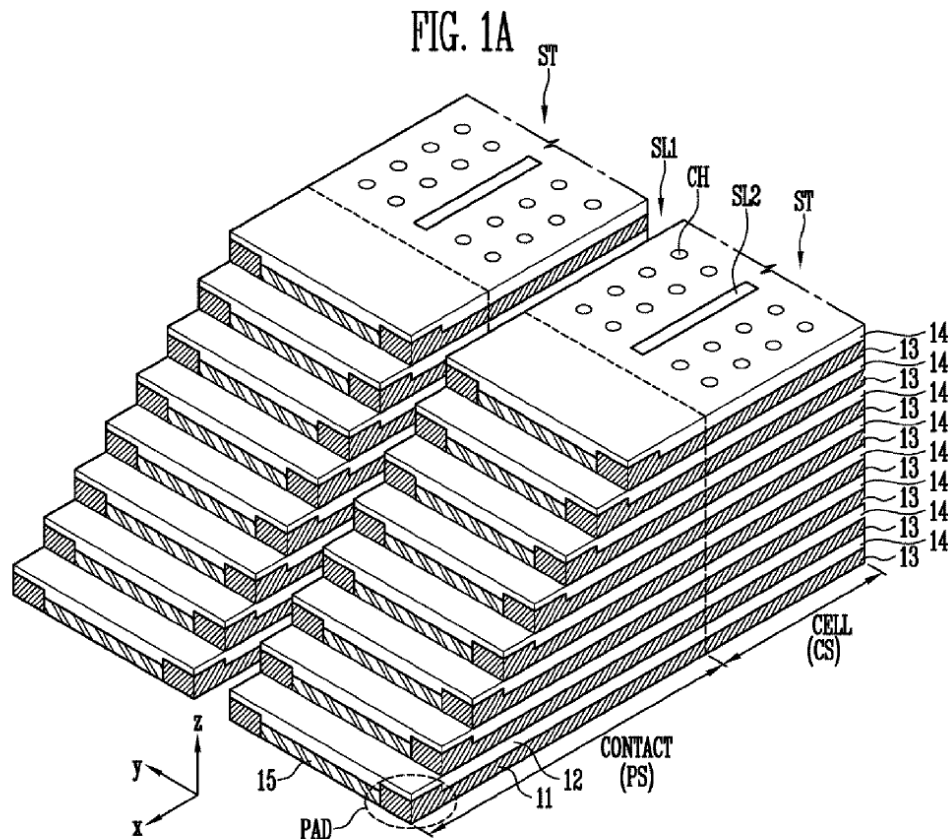
73. Petitioner’s expert starts with Lee Figure 7B as annotated below. *See* Ex. 1003 ¶¶ 351-354. Notably, Petitioner’s expert annotates that the “first material layer” extends over the entirety of the “second material layer.” Yet, he arbitrarily designates a “first portion” of the second material layer without explaining why. In my opinion, this arbitrary and unexplained selection is due to a hindsight reconstruction of the challenged claims. As Petitioner’s expert acknowledges, Lee’s layer 22, which Petitioner’s expert maps to the “first material layer” of the claims, extends over the entirety of the identified “second material layer.” Thus, there is no identifiable “portion” at all that layer 22 is “disposed over” because it is over the entirety of it. This fails to show the structure of claims 1 and 12 of the ’838 patent, which describe a correspondence between the “first material layer” and the “first portion of the second material layer.”



74. Despite the lack of explanation for the arbitrary “first portion” label, Petitioner’s expert identifies part of conductive layer 25 as the “landing pad,” annotated in orange below. *See* Ex. 1003 ¶¶ 356-360. This is also is unexplained.



75. In his analysis, Petitioner's expert states that "the pad portion PAD on the end of each of Lee's conductive layer (annotated orange / brown) is the claimed "landing pad." Ex. 1003 ¶ 360 (emphasis removed). However, what Petitioner's expert annotates in orange above is not what Lee refers to as "the pad portion PAD" as he states. Instead, Lee explains, referring to Lee Figure 1A, that "[p]ortions of the first conductive layers 11 that are exposed along the stepped end of the pad structure PS may be defined as pad portions PAD." Lee at [0023], Fig. 1A. A POSITA would understand that the pad portions PAD are all of the conductive material that is not covered by a step above. Lee indicates this in Figure 1A by circling all of the end of the conductive material 11 and labeling it "PAD."



76. After two arbitrary labels inconsistent with the teachings of Lee itself, Petitioner's expert then labels a "second portion." In my opinion, this series of arbitrary labels that are not associated with the structures described in Lee evidences the hindsight reconstruction of Petitioner's expert's mapping of Lee to the requirements of claims 1 and 12. As claims 1 and 12 require, there is a correspondence between the "first material layer" and the "first portion of the second material layer." Likewise, there is a correspondence between the "landing pad" and the "second portion of the second material layer." Like with Ground 1, Petitioner's expert simply ignores the claimed relationships. But for

the reasons I have given, these relationships describe the claimed structure, identifying the relationships between the claimed features in the claimed structures. To ignore those relationships is to omit them from the claims. Again, one can see this if one considers the claims with “a first portion of” and “a second portion of” (and “the second portion of”) removed. Then there is no defined relationship and no distinct and separate portions claimed. The “landing pad” and the “first material layer” just need to be over the “second material layer.” That is essentially all that Petitioner’s expert shows with Lee. That would also be inconsistent with the discussion above in Sections VI and VII regarding the specification and how the “first portion” and “second portion” are described as separate and distinct as extents in the x-direction.

77. The Petition states that “[t]he claims require only that an insulating layer be ‘disposed over a first portion’ of an underlying conductive layer. They do not prohibit the insulating layer from also covering other portions of the same conductive layer.” Pet. 62. For the reasons explained above, I disagree with this interpretation. In my opinion, it ignores the claimed relationships of the features, renders “first portion” and “second portion” meaningless, and is contrary to the plain language of the claims.

78. Thus, in my opinion, claims 1 and 12 are not obvious in view of Lee as argued by Petitioner's expert. As the remainder of Ground 1 discusses dependent claims, obviousness of those claims also has not been shown.

X. Grounds 2, 4, and 5 Do Not Show Obviousness of the '838 Patent

79. As I have explained above, Petitioner's expert has not demonstrated obviousness of claims 1 and 12 over Kim or Lee. Ground 2 discusses claims 3 and 18 of the '838 patent, based on Kim and Yang. But Petitioner's expert does not discuss claims 1 and 12 in his analysis. *See* Ex. 1003 ¶¶ 293-335. Thus, in my opinion, claims 3 and 18 have not been shown to be obvious as in Ground 2.

80. Ground 4 discusses claims 3 and 18 of the '838 patent, based on Lee and Haller. But Petitioner's expert does not discuss claims 1 and 12 in his analysis. *See* Ex. 1003 ¶¶ 430-456. Thus, in my opinion, claims 3 and 18 have not been shown to be obvious as in Ground 4.

81. Ground 5 discusses claims 13-15, based on Lee and Park. But Petitioner's expert does not discuss claims 1 and 12 in his analysis. *See* Ex. 1003 ¶¶ 457-499. Thus, in my opinion, claims 13-15 have not been shown to be obvious as in Ground 5.

XI. Conclusion

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on June 06, 2025, in Pasadena, CA.

A handwritten signature in black ink, appearing to read 'Konstantinos Giapis', written over a horizontal line.

Konstantinos Giapis