



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/126,956	09/10/2018	Zhenyu LU	4123.0460002	3036
26111	7590	10/22/2019	EXAMINER	
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.			GEYER, SCOTT B	
1100 NEW YORK AVENUE, N.W.			ART UNIT	PAPER NUMBER
WASHINGTON, DC 20005			2812	
			NOTIFICATION DATE	DELIVERY MODE
			10/22/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-8 and 18-20 in the reply filed on October 2, 2019 is acknowledged.

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in China on August 28, 2017. It is noted, however, that applicant has not filed a certified copy of the foreign priority application as required by 37 CFR 1.55.

Information Disclosure Statement

The references cited within the IDS documents submitted on June 6, 2019 (two documents) have been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claims 1-7 and 18-20 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Hyun (US 9,373,540 B2).

As to **claim 1**, Hyun teaches a semiconductor structure in figure 2H (see also figures 2A-2G). The semiconductor structure of Hyun has:

a substrate (not shown, see column 5, lines 17-30); and

a staircase structure (see figure 2H) disposed over the substrate, wherein the staircase structure comprises:

a plurality of layer stacks (203/235), each layer stack comprising a first material layer (203) disposed over a first portion of a second material layer (235, which is 231+233); and

a plurality of landing pads (217P) respectively disposed on the plurality of layer stacks, each landing pad disposed over a second portion of the second material layer (235) of a respective layer stack.

As to **claim 2**, Hyun teaches each of the plurality of landing pads (217P) is adjacent to a respective side of the first material layer (203). See figure 2H.

As to **claim 3**, Hyun teaches each of the plurality of landing pads (217P) extends over a respective top surface of the second material layer (235).

As to **claim 4**, Hyun teaches the first material layer (203) comprises an insulating material, the second material layer (235) comprises a first conductive material, and each of the plurality of landing pads (217P) comprises a second conductive material.

As to **claim 5**, Hyun teaches the first conductive material is the same as or different from the second conductive material. First conductive material can be tungsten (see column 7, lines 64-65) and second conductive material can be tungsten as well (see column 6, lines 50-52). See also figures 2C and 2G.

As to **claim 6**, Hyun teaches the insulating material can be silicon oxide (column 5, lines 31-45) and each of the first and the second conductive material layers comprises tungsten (column 7, lines 64-65; column 6, lines 50-52).

As to **claim 7**, Hyun teaches the second material layer (235) of each layer stack is disposed over a portion of the first material layer (203) of an adjacent layer stack. See also figure 2H.

As to **claim 18**, Hyun teaches a memory device in figure 2H (see also figures 2A-2G). The memory device of Hyun has:

- a substrate (not shown, see column 5, lines 17-30); and
- a memory string (see also figure 1) disposed over the substrate; and
- a staircase structure disposed adjacent to the memory string, wherein the staircase structure comprises:

- a plurality of layer stacks (see figure 2H), each layer stack comprising an insulating layer (203) disposed over a first portion of a conductive layer (235/231+233), wherein a second portion of the conductive layer (217P) is in contact with a side surface of the insulating layer (see figure 2H).

As to **claim 19**, Hyun teaches the conductive layer of each layer stack is disposed over a portion of the insulating layer of an adjacent layer stack. See figure 2H.

As to **claim 20**, Hyun teaches the second portion of the conductive layer is thicker than the first portion of the conductive material layer. Regarding figure 2H, the "second portion" is the area of the conductive 'track' that includes 217P, the landing

pad. The overall thickness of 217P and 231/233 in this area is thicker than the area to the right side (the "first portion" area), which is only 231/233.

//

//

Claims 1-3 and 7 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Hashimoto (US 2011/0031630 A1).

As to **claim 1**, Hashimoto teaches a semiconductor structure in figure 11B. The semiconductor structure of Hashimoto has:

a substrate (10); and

a staircase structure (see figure 11B) disposed over the substrate, wherein the staircase structure comprises:

a plurality of layer stacks (e.g. WL4/25), each layer stack comprising a first material layer (WL4) disposed over a first portion of a second material layer (25); and

a plurality of landing pads (44) respectively disposed on the plurality of layer stacks, each landing pad disposed over a second portion of the second material layer (25) of a respective layer stack.

As to **claim 2**, Hashimoto teaches each of the plurality of landing pads (44) is adjacent to a respective side of the first material layer (WL4). See figure 11B.

As to **claim 3**, Hashimoto teaches each of the plurality of landing pads (44) extends over a respective top surface of the second material layer (25).

As to **claim 7**, Hashimoto teaches the second material layer (25) of each layer stack is disposed over a portion of the first material layer (e.g. WL4, WL3, WL2) of an adjacent layer stack. See also figure 11B.

Allowable Subject Matter

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: see the attached form PTO-892 for pertinent cited art.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott B. Geyer (telephone: 571-272-1958). The examiner can normally be reached on Monday to Friday, 10AM - 4PM. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at: <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles D Garber (telephone: 571-272-2194). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in U.S.A. or Canada) or 571-272-1000.

/SCOTT B GEYER/
Primary Examiner, Art Unit 2812