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"At 20nm, chips have features sized ten times smaller than the wavelength of laser used in lithography"

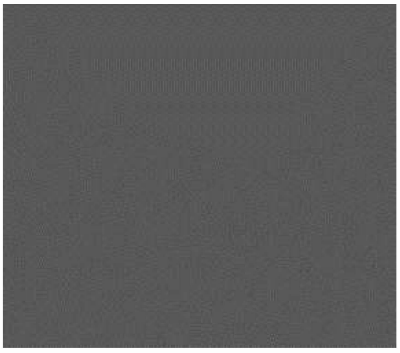
By **EFY Bureau**

December 4, 2014

While EDA has not been traditionally valued as highly as apps and online networking companies, the scenario is changing thanks to the rapid pace of innovation. A new breed of firms is embracing the value of EDA, IP, and semiconductor design ecosystem as systems companies build their own components and subsystems.

Jaswinder Ahuja, Corporate Vice President and Managing Director, Cadence India speaks to Dilin Anand where he shares his perspective on the rapid pace of development in electronics and the challenges involved in ensuring constant innovation.

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Q. What according to you are the innovations driving our semiconductor industry?

YMTC
Exhibit 2025
Micron v. YMTC
PGR2025-00021
Ex. 2025-001



Jaswinder Ahuja, Corporate Vice President and Managing Director, Cadence India

A. Semiconductor and Electronics Design Automation (EDA) companies have had to innovate rapidly to keep up with the market demand for even more bandwidth, memory, and longer lasting power requirements. The fact that in the last few years we have moved from 90nm to 28nm and even 16/14nm is a testament to the innovation that is happening. Advanced process nodes promise tremendous advantages in power, performance, and design capacity, but they also introduce some tough design challenges, such as increased timing and power variability, more complex layout rules, and incredibly large designs with massive amounts of Intellectual Property (IP).

Q. Could you elaborate on the kind of manufacturing challenges introduced by advanced process nodes?

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A. Manufacturing issues take centre stage for design flows at the 20nm technology node, and no wonder: at 20nm, chips have feature sizes ten times smaller than the wavelength of the laser light typically used in lithography. Designers need automated solutions that deal with the manufacturing requirements of 20nm chip designs and, specifically, with their new lithography techniques. One technique in particular—double-patterning technology—has such a pervasive impact on the silicon that nearly every step in the design flow must anticipate and prevent double-patterning problems.

Q. It's interesting how the effects are seen all the way back to design too. What are the other challenges faced while designing products for advanced nodes?

A. Each new technology node brings design and integration complexity to a new level. Decreasing metal pitch leads to coupling effects and signal integrity issues. Increasing wire and via resistance requires more advanced and variable wire sizing and tapering techniques. Extraction, timing, signal integrity analysis, and modelling must take a multitude of variation issues into account to achieve accuracy without compromising performance. Lithography limitations at 20nm often require a great deal of fixing to achieve signoff. Moreover, there are multiple chip and IP integration challenges, packaging issues, and the complexity of all these issues interacting.

Q. We have seen 3D architecture in semiconductors and memory these last couple of years. What was the biggest design challenge back when this was introduced to research & development (R&D) centres, and what EDA features helped solve them?

A. Many 3D stacks will combine digital and analogue or RF circuitry, requiring a strong analogue or mixed-signal capability. Because of the unique packaging requirements of a stacked die, an integrated circuit (IC) or package co-design capability is a must. Additionally, fitting 3D-ICs on a board is challenging, requiring a capable printed circuit board (PCB) layout system with appropriate analysis tools. Thus, anyone who presents a complete solution must provide expertise in digital, analogue, IC, package, and PCB design. Moving on to 3D-IC will require design engineers, who have historically worked in isolated domains, to collaborate and essentially co-design the IC.

Q. What is driving the changing trend where EDA tools solve more than just immediate hardware problems?

A. As electronic products across all market segments become more sophisticated, developing their underlying hardware and software and integrating the two sides continues to grow more complex. Early software development, hardware verification, hardware/software integration, and integrated system validation have become primary challenges, increasing development costs, project schedules, and risks. From the electronic system level (ESL) design perspective, the high-level abstraction of software is eclipsing hardware as the main driver of system development cost, schedule, and risk. As software applications have become the primary product differentiator, systems and semiconductor companies must provide not only silicon, but also complete hardware/software systems ready for apps deployment. EDA companies must provide solutions for both.

Q. Could you share an example of a recent complex device brought to market faster using these solutions?

A. The last five years in the history of EDA have been significant. Electronics devices manufactured today are far more complex than they were five years ago in terms of processing power, power consumption, memory, area, and performance. Take just one ubiquitous example—the mobile phone.

Five years ago, in June 2009, we were impressed with the state-of-the-art iPhone 3GS which had a three megapixel camera, full HTML web browsing, 256MB RAM and a 600MHz ARM® Cortex®-A8 CPU. Compare that with today's iPhone 6, which has an eight megapixel camera, 1GB RAM, and a dual-core 1.4GHz (ARM V8-based) Cyclone CPU.

Q. What are the new technologies that EDA firms have brought to the table, to enable system design firms to meet the challenges of the modern world?

A. With this surge in the scale of features, the growth of the app ecosystem, and the increasing consumption of media on mobile devices, the fundamental manner in which electronic design is developed has had to scale up rapidly. Systems companies look towards EDA and chip suppliers to keep up with consumers' demands for faster, smaller, and more functional devices. Hardware/software co-verification, advanced node design, 3D-ICs, FinFETs, double patterning, and IP use and re-use are some of the new technologies and design techniques that have helped EDA and the semiconductor industry continue to meet the demands of mobile world.

Q. Why is ecosystem collaboration so important in solving modern challenges, even with the availability of those technologies mentioned above?

A. Many of today's design challenges are interdependent. To deal with this interdependency, EDA companies must not only address specific technical issues, but also collaborate closely with ecosystem partners to develop practical and reliable solutions in a reasonable timeframe. Close collaboration among designers, EDA vendors, IP providers, foundries, and other ecosystem players will help mitigate some of the design challenges posed by sophisticated electronic devices.

Q. Could you elaborate on these interdependent challenges?

A. There are several examples. In the case of IP, a semiconductor company will buy it from an IP company like Cadence. The challenge thereafter is integrating the IP into their designs, which requires collaboration with EDA vendors and with foundries. EDA tools

need to be certified by foundries like Taiwan Semiconductor Manufacturing Company (TSMC) for instance. Cadence recently won a TSMC Partner of the Year award for joint development of 16FF+ design infrastructure based on the early, in-depth collaboration between TSMC and Cadence for FinFET enablement and the development of this latest advanced node technology for next-generation system-on-chip (SoC) designs. In the case of double patterning that we discussed earlier, close collaboration is required between the semiconductor and EDA companies with the foundries to ensure manufacturability.
