

Filed on behalf of: Yangtze Memory Technologies Company, Ltd.

Entered: November 26, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

PGR2025-00021
Patent 12,010,838

**DECLARATION OF KONSTANTINOS GIAPIS
IN SUPPORT OF
PATENT OWNER'S RESPONSE**

Table of Contents

I.	Introduction and Qualifications	1
II.	Summary Of Materials Reviewed And Considered	3
III.	Understanding of Legal Standards.....	7
A.	Claim Construction.....	7
B.	Obviousness	8
IV.	Person Having Ordinary Skill in the Art.....	12
V.	Overview of 3D NAND Memories.....	13
VI.	Overview of the '838 Patent (Ex. 1001)	16
VII.	Claim Construction	30
A.	Terms involving “first” and “second portion” “of the second material layer”.....	30
B.	“curved side surface”	42
VIII.	Ground 1: Claims 1, 4-7, 12-17, and 19-20 Are Not Obvious In View of Kim.....	59
A.	Overview of Kim (Ex. 1005).....	59
B.	Petitioner’s Expert Misunderstands or Misrepresents Kim and Kim’s Mapping to Claims 1 and 12 and Does Not Show Obviousness	70
C.	A POSITA Would Not Have Found Claims 13-15 Obvious Based on Kim.....	82
1.	Kim, Alone or in Combination, Does Not Teach nor Render Obvious a “first side surface comprises a curved side surface”	91
IX.	Ground 2: Claims 3 and 18 Are Not Obvious In View of Kim and Yang (Ex. 1007)	107
X.	Ground 3: Claims 1, 4-7, 12, 16-17, and 19-20 Are Not Obvious In View of Lee.....	117
A.	Overview of Lee (Ex. 1006)	117

B. Petitioner’s Expert Does Not Show Obviousness of Claims 1
 and 12 in View of Lee 120

XI. Ground 4: Claims 3 and 18 Are Not Obvious In View of Lee and
 Haller..... 125

XII. Ground 5: Claim 13-15 Are Not Obvious In View of Lee and Park
 131

XIII. Conclusion..... 144

I. Introduction and Qualifications

1. I have been retained by Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Patent Owner”) to provide my opinions concerning the validity of certain claims of U.S. Patent No. 12,010,838 (“838 patent”) (Ex. 1001).

2. I am a professor of chemical engineering at the California Institute of Technology (“Caltech”). I have held a professorial position at Caltech since 1993.

3. My primary research relates to the processing of semiconductors, dielectrics, and metals, as performed in the fabrication of semiconductor devices, including microprocessors and digital memories. In particular, my work has focused upon experimental and computational studies of various aspects of depositing and patterning of layers of electronic materials to fabricate sub-micron features such as transistor gates, vias, and interconnect channels found in VLSI circuits and digital storage. My research group has contributed to the understanding of the evolution of such features (profiles) in single-crystalline silicon, poly-silicon, metal, and dielectric layers subjected to plasma processing (etching, deposition, ion implantation). Since the start of my graduate career in 1985, I have accumulated over 40 years of experience on most aspects of processing of semiconductor materials and devices.

4. In my professorial duties at Caltech, I have developed and taught new undergraduate and graduate level courses on semiconductor device physics, processing, and fabrication. These innovative courses combined solid state physics and electronic materials processing technologies with the more traditional chemical engineering subjects of transport phenomena and chemical thermodynamics. The courses have prepared several generations of students for successful careers in the semiconductor industry.

5. During my research career, I have authored or co-authored 100 peer-reviewed papers, 12 refereed conference proceedings, and two book chapters. Most of my publications relate to basic aspects of semiconductor processing and, in particular, the interaction dynamics of plasma ions with patterned and unpatterned surfaces of materials used in semiconductor manufacturing. My papers on charging damage during plasma-processing of VLSI devices are highly cited. The latter work includes studies of charging effects and surface breakdown during directional (plasma) deposition of interlevel dielectrics on patterned metal interconnects. My laboratory has also extensively used and studied plasma-deposited silicon oxide layers from silane and TEOS precursors.

6. Additional information regarding my education, technical experience and publications, including a list of 14 U.S. patents I have co-

invented, is included in my *Curriculum Vitae*, which I understand is Exhibit 2007.

II. Summary Of Materials Reviewed And Considered

7. All of the opinions contained in this Declaration are based on the documents I reviewed and my knowledge and professional judgment. In forming the opinions expressed in this Declaration, while drawing on my experience in the field of semiconductor fabrication, I reviewed the following documents, and other documents cited herein:

Ex.	Description
1001	United States Patent No. 12,010,838 (“the ’838 patent”)
1002	File History for the ’838 patent (“’838 FH”)
1003	Declaration of Dr. Jack C. Lee
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent No. 10,229,929 to Kim et al. (“Kim”)
1006	U.S. Patent Publication No. 2014/0191389 A1 to Lee et al. (“Lee”)
1007	U.S. Patent No. 9,941,153 to Yang (“Yang”)
1008	U.S. Patent No. 9,520,402 to Haller et al. (“Haller”)
1009	U.S. Patent No. 10,297,543 to Park et al. (“Park”)
1010	U.S. Patent No. 9,589,978 to Yip (“Yip”)
1011	Aritome, “Nand Flash Memory Technologies” (2016)
1012	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2nd Ed. 2018)
1013	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017
1014	U.S. Patent Publication No. 2016/0218107 A1 to Lee et al. (“Lee 107”)

Ex.	Description
1015	U.S. Patent Publication No. 2015/255385 to Lee
1016	U.S. Patent No. 9,373,540 to Hyun
1017	U.S. Patent Publication No. 2011/0031630 A1 to Hashimoto
1018	Excerpts from the File History of PCT/CN2018/098962
1019	File History of U.S. Patent Application No. 16/126,956
1020	File History of U.S. Patent Application No. 16/885,858
1021	U.S. Patent No. 9,343,452 B2 (“Yun”)
1022	U.S. Patent Application Publication No. 2018/0026046 A1 (“Nam”)
2020	U.S. Patent No. 9,006,884 B2 (“’884 Patent”)
2021	U.S. Patent No. 11,145,666 B2 (“’666 Patent”)
2022	Excerpt of File History U.S. Patent Application No. 16/126,956
2023	Counterpoint Tech. Mkt. Rsch., <i>Scaling to 1,000-Layer 3D NAND in the AI Era</i> (July 2024), https://filecache.mediaroom.com/mr5mr_lamresearch/182770/Counterpoint_Research_Paper_Scaling_to_1000-Layer_3D_NAND_in_the_AI_Era.pdf (“Counterpoint”)
2024	3D FLASH MEMORIES (Roni Micheloni ed. 2016) (“Micheloni”) (excerpt)
2025	EFY Bureau, <i>At 20nm, Chips Have Features Sized Ten Times Smaller Than the Wavelength of Laser Used in Lithography</i> , Electronicsforu.com (Dec. 4, 2014), https://www.electronicsforu.com/technology-trends/interviews/20nm-chips-features-sized-ten-times-smaller-wavelength-laser-used-lithography
2026	Press Release, ASML, ASML Extends ArF Leadership (Dec. 6, 2006), https://www.asml.com/en/news/press-releases/2006/asml-extends-arf-leadership (last visited Nov. 17, 2025)
2027	ASML, <i>Light and Lasers</i> , https://www.asml.com/en/technology/lithography-principles/light-and-lasers (last visited Nov. 17, 2025)

Ex.	Description
2028	James D. Plummer et al., SILICON VLSI TECHNOLOGY: FUNDAMENTALS, PRACTICE AND MODELING (Prentice Hall Elecs. & VLSI Series) (Charles Sodini ed. 2000) (“Plummer”) (excerpts)
2029	Steven S. Zumdahl et al., CHEMISTRY: AN ATOMS FIRST APPROACH (3d ed. 2021) (“Zumdahl”) (excerpt)
2030	Transcript of the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , PGR2025-00021 (P.T.A.B. Oct. 30, 2025) (“Lee ’838 Dep.”)
2031	Transcript of the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00189 (P.T.A.B. Aug. 13, 2025) (“Lee ’666 Dep.”)
2032	Exhibit 1 entered in the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00189 (P.T.A.B. Aug. 13, 2025) (Ex. 2031) (“Lee ’666 Dep. Ex. 1”)
2033	Exhibit 2 entered in the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00189 (P.T.A.B. Aug. 13, 2025) (Ex. 2031) (“Lee ’666 Dep. Ex. 2”)
2034	Exhibit 3 entered in the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00189 (P.T.A.B. Aug. 13, 2025) (Ex. 2031) (“Lee ’666 Dep. Ex. 3”)
2035	Exhibit 4 entered in the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00189 (P.T.A.B. Aug. 13, 2025) (Ex. 2031) (“Lee ’666 Dep. Ex. 4”)
2036	Exhibit 5 entered in the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00189 (P.T.A.B. Aug. 13, 2025) (Ex. 2031) (“Lee ’666 Dep. Ex. 5”)

Ex.	Description
2037	Exhibit 6 entered in the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00189 (P.T.A.B. Aug. 13, 2025) (Ex. 2031) (“Lee ’666 Dep. Ex. 6”)
2038	Exhibit 7 entered in the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00189 (P.T.A.B. Aug. 13, 2025) (Ex. 2031) (“Lee ’666 Dep. Ex. 7”)
2039	Exhibit 8 entered in the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00189 (P.T.A.B. Aug. 13, 2025) (Ex. 2031) (“Lee ’666 Dep. Ex. 8”)
2040	Exhibit 9 entered in the Deposition of Jack C. Lee, Ph.D., <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , IPR2025-00189 (P.T.A.B. Aug. 13, 2025) (Ex. 2031) (“Lee ’666 Dep. Ex. 9”)
2041	U.S. Patent Application Publication No. 2018/0301460 A1 (“Yoo”)
2042	A.E.T. Kuiper et al., <i>Oxidation Behaviour of LPCVD Silicon Oxynitride Films</i> , 33/34 APPLIED SURFACE SCI. 757 (1988) (“Kuiper”)
2043	Yen-Po Lin & Jenn-Gwo Hwu, <i>Quality Improvement in LPCVD Silicon Nitrides by Anodic and Rapid Thermal Oxidations</i> , 7 ELECTROCHEMICAL SOLID-STATE LETTERS G87 (2004) (“Lin”)
2044	X. Y. Chen et al., <i>Annealing and Oxidation of Silicon Oxide Films Prepared By Plasma-Enhanced Chemical Vapor Deposition</i> , 97 J. APPLIED PHYSICS 014913 (2005) (“Chen”)
2045	A. Barranco et al., <i>Electronic State Characterization of SiO_x Thin Films Prepared by Evaporation</i> , 97 J. APPLIED PHYSICS 113714 (2005) (“Barranco”)

8. My opinions are additionally guided by my appreciation of how a person of ordinary skill in the art would have understood the claims of the ’838

patent at the time of the alleged invention, which I have been asked to assume is August 28, 2017.

III. Understanding of Legal Standards

9. I am not an attorney, and in this Declaration, I do not opine on matters of law. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis and opinions. My understanding of these principles is set forth below.

10. I have been informed by Counsel that the validity analysis is a two-step process. First, the patent claims are construed to ascertain their proper scope. Second, the construed claims are compared to the identified prior art to determine if the claims are valid over the prior art.

A. Claim Construction

11. I have been informed by Counsel that the claims of a patent define the limits of the patentee's exclusive rights. I have been informed by Counsel that to determine the scope of the claimed invention, courts typically construe claim terms, the meaning of which the parties may dispute. I have been informed by Counsel that claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of filing of the patent application, after reading the patent and its prosecution history. I also have been informed by Counsel that a basic tenet of claim

construction presumes that different words in a claim have different meanings, unless there is evidence to the contrary. I also have been informed by Counsel that it is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.

12. I have been informed by Counsel that claims must be construed in light of, and consistent with, the intrinsic evidence. In this context, I have been informed by Counsel that intrinsic evidence includes the claims themselves, the written disclosure in the specification, and the patent's prosecution history, including prior art that was considered by the United States Patent and Trademark Office ("USPTO"). I have been informed by Counsel that the specification is always highly relevant to the claim construction analysis and often is the single best guide to the meaning of a disputed term. I have been informed by Counsel that extrinsic evidence may also be considered when construing claims and may include, for example, technical dictionaries, technical publications and books, treatises, and expert testimony.

B. Obviousness

13. I have been informed by Counsel that patent claims can be deemed invalid if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. While

such conclusions are often based on more than one piece of prior art, only one is required. It is not sufficient that a collection of prior art references merely recites the various elements of a challenged patent claim. Rather, as I have been informed by Counsel, the prior art must present the elements in a manner that is consistent with their arrangement or use in the challenged claims. I have been informed by Counsel that obviousness cannot be based on the hindsight combination of components selectively culled from the prior art.

14. I have been informed by Counsel that a person having ordinary skill in the art (i.e., a POSITA) is a hypothetical person who is presumed to have known the relevant art at the time the invention was made. I have been informed by Counsel that the condition “at the time the invention was made” is imposed to rule out impermissible hindsight. I also have been informed by Counsel that an expert is to analyze the prior art from the perspective of a person of ordinary skill in the art at the time the invention was made, and not simply to provide his/her own personal conclusions.

15. I also have been informed by Counsel that an obviousness determination includes several factual inquiries, including (1) determining the scope and content of the prior art; (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the

pertinent art; and (4) taking into consideration any objective indicia of nonobviousness.

16. I have been informed by Counsel that obviousness must be determined as of the date of the invention (i.e., the effective filing date or priority date of the patent). Thus, in considering the reason or motivation to combine references, it is essential to avoid using hindsight. For example, the problem examined when considering obviousness is the general problem that confronted the inventor before the invention was made, not the specific problem solved by the invention. Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness. Further, an overly narrow statement of the problem can represent a form of hindsight, because often the inventive contribution lies in defining the problem in a new revelatory way. Similarly, an assertion that a person of ordinary skill could combine the references, rather than that they would have been motivated to do so, is an impermissible form of hindsight. Moreover, knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed invention.

17. I have been informed by Counsel that a motivation to solve a problem (or issue) is not the same as a motivation to have combined references. I have been informed by Counsel that whether a skilled artisan would be motivated

to make a combination includes whether he/she would select particular references in order to combine their elements.

18. I have been informed by Counsel that the analysis of the motivation to combine should be explicit. Additionally, it must include articulated reasoning with rational underpinnings to support the conclusion of obviousness. Providing a full explanation of the motivation to combine the references and the reasonable expectation of success is a necessary component of the obviousness inquiry, as inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. However, conclusory statements fail to adequately explain why a person of ordinary skill would have a motivation to combine the potential prior art references.

19. I have been informed by Counsel that common sense, common wisdom, and common knowledge may be used to support a motivation to combine, so long as the use of common sense in the analysis is explained with sufficient reasoning. But, common sense can only be used to supply a limitation missing from the prior art where the technology is unusually simple and straightforward.

20. I also have been informed by Counsel that evidence suggesting reasons to combine cannot be viewed apart from evidence suggesting reasons not

to combine. In analyzing motivation, both advantages and disadvantages must be considered. Teaching away, for example, is a statement in the prior art that either (i) discourages one from following the path of the claimed invention, or (ii) encourages one to follow a path that diverges from the path of the claimed invention. The concept of teaching away bears directly on whether there was a reason to combine prior art. Known disadvantages in prior art technology or devices which would naturally discourage a search for new inventions may also be taken into account in determining obviousness.

21. I also have been informed by Counsel that patent drawings do not define the precise proportions of the elements in prior art patents and publications and may not be relied on to show particular sizes if the specification is completely silent on the issue.

IV. Person Having Ordinary Skill in the Art

22. Petitioner's expert defines a person having ordinary skill in the art ("POSITA") as a person having "a bachelor's degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) 3D memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may substitute for professional experience)." Ex. 1003 (Lee Decl.) ¶36. Petitioner's expert further notes that "this POSITA would also have been aware of and

generally knowledgeable about 3D memory's structure, its component parts, and how it operates.” *Id.* ¶37.

23. For the purposes of this declaration, I have not been asked to provide an opinion on the level of ordinary skill in the art. In view of my educational background and work experience, I surpass Petitioner's expert's definition of a POSITA, and did so before August 28, 2017. Regardless of the precise definition of a POSITA, none of the Grounds in the Petition show that the challenged claims are obvious. I reserve the right to opine as to an alternative level of a POSITA in other proceedings.

V. Overview of 3D NAND Memories

24. 3D NAND memory is an assembly of discrete memory cells in three dimensions, developed to increase digital memory density. While the process has matured over the years, it is not a simple or straightforward technology.

25. Even as late as 2024, NAND technology had been described as a “complex technology that presents some major manufacturing challenges” and as having a “not trivial” process complexity. Ex. 2023 6; Ex. 2024 199. It certainly was complex and not straightforward back on August 28, 2017.

26. 3D NAND memory devices include “a stack of word lines horizontally arranged over a substrate, with vertical semiconductor channels that intersect the word lines.” '838 patent (Ex. 1001) 1:33-36. “The intersection of a

word line and a vertical semiconductor channel forms a memory cell.” *Id.* 1:36-37. Memory cells can be written or read by applying a voltage to the “word lines,” which are made of an electrically conductive material and run horizontally across the memory array. *E.g., id.* 5:27-33; Ex. 1014 [0006]. For example, the figure below, from Exhibit 1012, shows vertically stacked memory cells on the left hand side, each controlled by a Control Gate (CG) accessible electrically by means of word lines. Ex. 1012 134; *see also* Ex. 1011 62, Fig. 3.4 (equating “Control Gate” with “Word Line”).¹

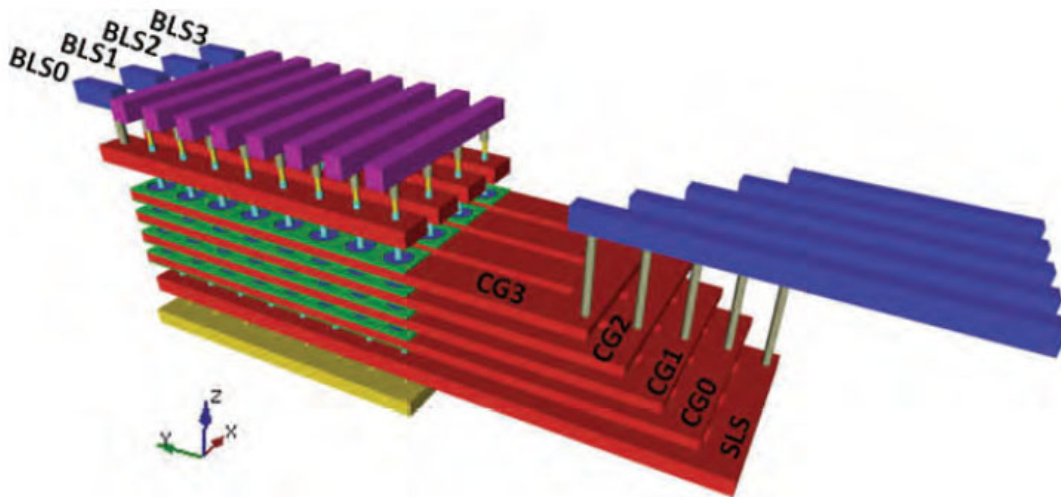


Fig. 5.20 C-FG NAND Flash array with fan-out

¹ My citations to Ex. 1002, Ex. 1011, and Ex. 1012 are to page numbers in captions added by the parties to the exhibits.

27. The word lines (CG0, CG1, CG2, and CG3) themselves need to be accessed externally to the memory device in order to control the memory. To enable such access, word lines can be “fan[ned] out” in an area adjacent to the memory array ending in conductive portions similar to stair steps arranged in a staircase pattern, as shown above. Ex. 1012 134; '838 patent 5:34-43. That way, the word lines can then be separately accessed through vertical metal columns (tan) connecting the conductive steps electrically to external conductive lines (blue). Ex. 1012 134. The metal columns are formed by first drilling channels, called “vias,” in the interlevel dielectric material covering the steps, then filling the vias with metal.

28. A potential problem with the staircase structure is the possibility of a device malfunction by way of a short-circuit “[a]s the demand for higher storage capacity continues to increase [and] the number of vertical levels of the staircase structures also increases.” *E.g.*, '838 patent 5:36-39. “As a result, when applying a BEOL process to form interconnects on the staircase structures, an upper portion of the staircase structures is exposed to the BEOL process for a longer period of time than a lower portion of the staircase structures. This differential in BEOL exposure time increases the process variation of the final 3D memory device, thus introducing challenges in balancing manufacturing yield and process complexity/cost.” '838 patent 5:39-46.

29. For example, when upper stair steps are exposed to a BEOL (Back End Of Line) process longer during the formation of the interconnects (vertical metal columns), there is a possibility of breaking through the stair step material and forming an interconnect that extends to one or more word lines lying underneath, thereby risking electrically shorting the word lines. One way to prevent this is to increase the thickness of each stair step, which however brings the step closer to the upper word line creating the potential for electrical breakdown (i.e., a short-circuit), even in the presence of insulating material between the word lines.

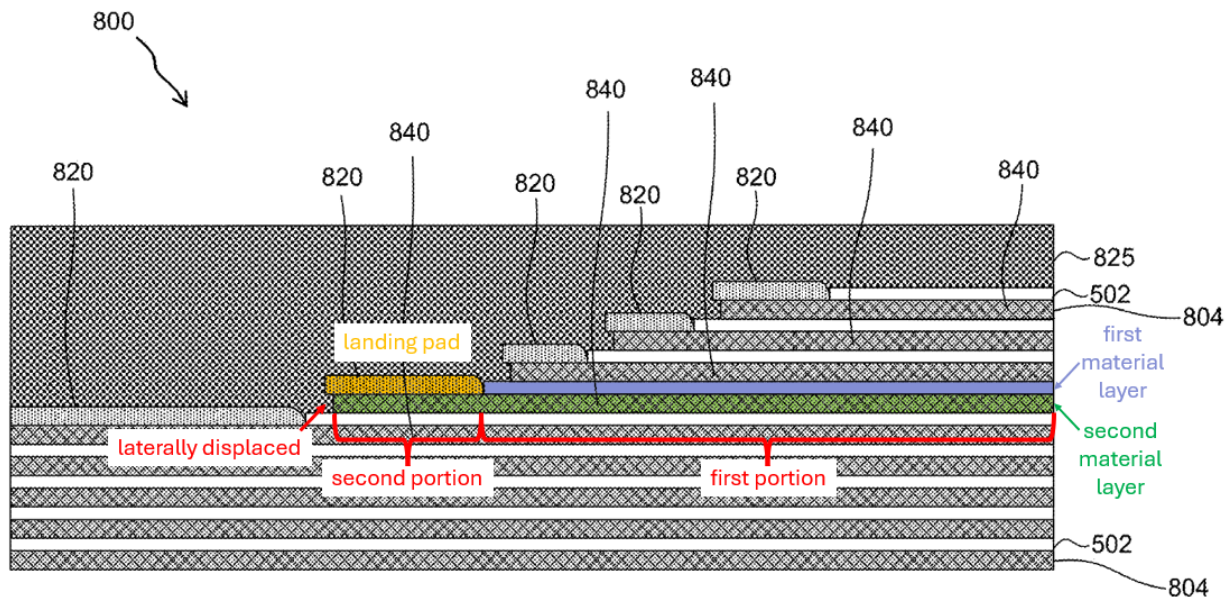
30. The semiconductor process must account for this problem to ensure short-circuits do not occur. The process and structure disclosed in the '838 patent provides a novel way to address this known problem.

VI. Overview of the '838 Patent (Ex. 1001)

31. The '838 patent discloses a process for making “a staircase structure for a memory device” and claims specific structures. '838 patent 1:39-43, 6:4-13:13, Figs. 1-9. Aside from Figure 9, the figures show cross-sectional views showing only the x-z plane. *See* '838 patent Figs. 1-8 (showing axes labels). The structures formed by the process “provide numerous benefits including, but not limited to, yield and manufacturing cost improvements.” *Id.* 1:43-45. A specific structure disclosed and claimed includes a “staircase structure [that] includes a

plurality of layer stacks, where each layer stack includes a first material layer disposed over a first portion of a second material layer.” *Id.* 1:47-50, Fig. 8.

Further, “[t]he staircase structure further includes a plurality of landing pads respectively disposed on the plurality of layer stacks, where each landing pad is disposed over a second portion of the second material layer of a respective layer stack.” *Id.* 1:50-54, Fig. 8. Additionally, “[e]ach of the landing pads is adjacent to a respective side of the first material layer” and is laterally displaced from the end of the second material layer below it. *Id.* 1:54-57, Fig. 8. These features are shown in Figure 8, annotated below. The first material layer is shown in blue, the second material layer is shown in green, and the landing pad is shown in orange. The first portion of the second material layer and the second portion of the second material layer are labeled. As can be seen, the first portion and the second portion are distinct from one another. They are separate, non-overlapping portions of the second material layer. While not labeled, the lateral displacement of the left side of the landing pad can also be seen in the figure below, extending beyond the left side of the second material layer.



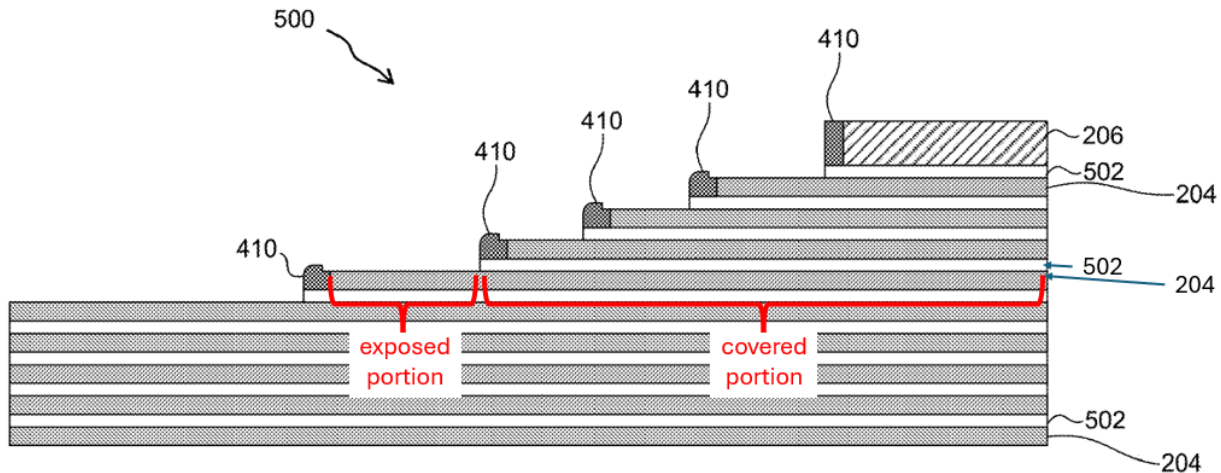
32. As described above, contacts must be formed to the word lines. In the '838 patent's structure, the landing pads are where the contacts are made by means of vertical metal columns (not shown). '838 patent 1:50-54, 1:60-61, 9:42-61, Fig. 8. In the final memory device, the landing pad and the second material layer are made of conductive material or materials to form word lines, while the first material layer is made of insulating or dielectric material. *Id.* 1:57-60, Fig. 8. The second material layer is also disposed over a first portion of the first material layer of an adjacent layer of the staircase structure while a second portion of the first material layer of the adjacent layer is laterally displaced from the second material layer (not annotated above). *Id.* 1:66-2:1, Fig. 8. The side

surface of the landing pad in contact with the first material layer includes a curved side surface. '838 patent Fig. 8.

33. The process of forming the structure is described throughout the specification using the accompanying figures. To form the structure, the process begins with an alternating layer stack formed over a substrate. *Id.* 6:4-67, 10:61-11:28, Fig. 1. At this stage, the alternating layer stack includes a plurality of layers, with each layer having an insulating layer over a sacrificial layer. *Id.* 6:4-67, 10:61-11:28, Fig. 1. The alternating layer stack is formed into a staircase structure by repeating an etch-trim process using a mask stack. *Id.* 7:1-67, 11:29-12:8, Figs. 2A-2B. After stairs have been formed, spacers are formed at a side of each layer of the staircase by conformally depositing a material on the staircase structure and then removing a portion of that material. *Id.* 8:1-33, 12:9-28, Figs. 3-4.

34. The exposed portion of the insulating layer of each step is then removed to expose a top portion of sacrificial layer underneath. *Id.* 8:34-45, 12:29-36, Fig. 5. Specifically, Figure 5 is described as “a cross-sectional view of a staircase structure 500 after removal of a portion of insulating layer 202.” *Id.* 8:34-36. It goes on to explain that “each SC layer of staircase structure 500 exposes a portion of a top surface of sacrificial layer 204 and spacer 410 of each SC layer.” *Id.* 8:41-44. This is shown below in annotated Figure 5, which

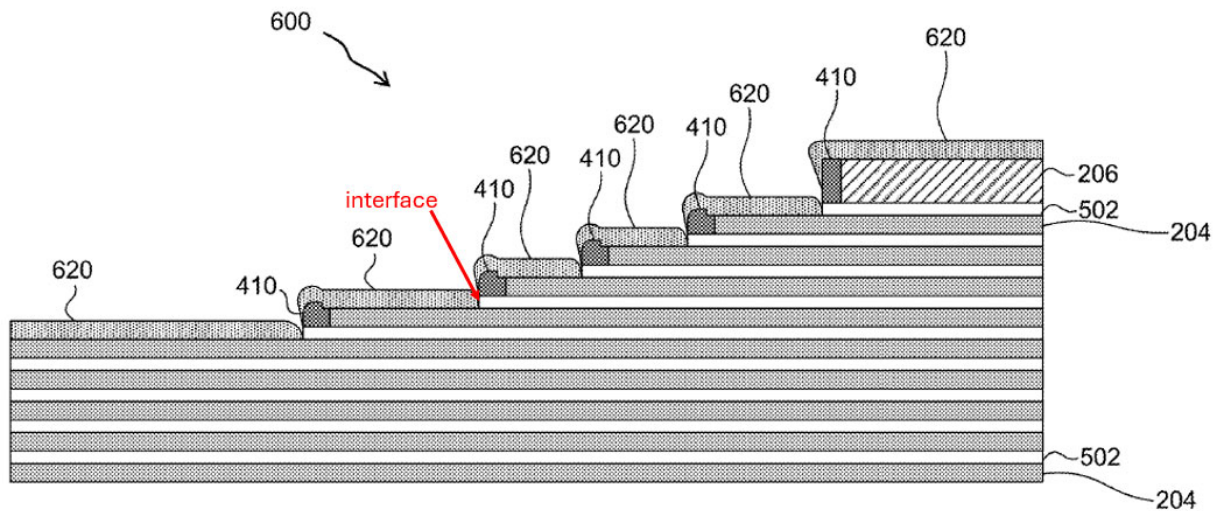
annotates the exposed portion, the covered portion, and adds labels 502 and 204 to the annotated layer, consistent with the '838 patent's description.



Compared to Figure 4, which depicts the previous step, it can be seen that any insulating material 502 (which was labeled 202 in Figure 4) that was not covered (when looking down on the structure in the z-direction) extending along the x-direction to the spacers 410 is removed. This creates two distinct and separate portions of the sacrificial layer 204: (i) a first portion that is still covered by insulating material 502 and (ii) a second portion that is the exposed portion shown above. These parts of the sacrificial layer 204 are ultimately the “first portion” and “second portion” of the second material layer as claimed in claims 1 and 12 of the '838 patent.

35. A dielectric material is then deposited onto the staircase structure. '838 patent 8:46-9:12, 12:37-49, Fig. 6. The '838 patent describes this as a deposition process and does not describe formation of the structures 620 depicted

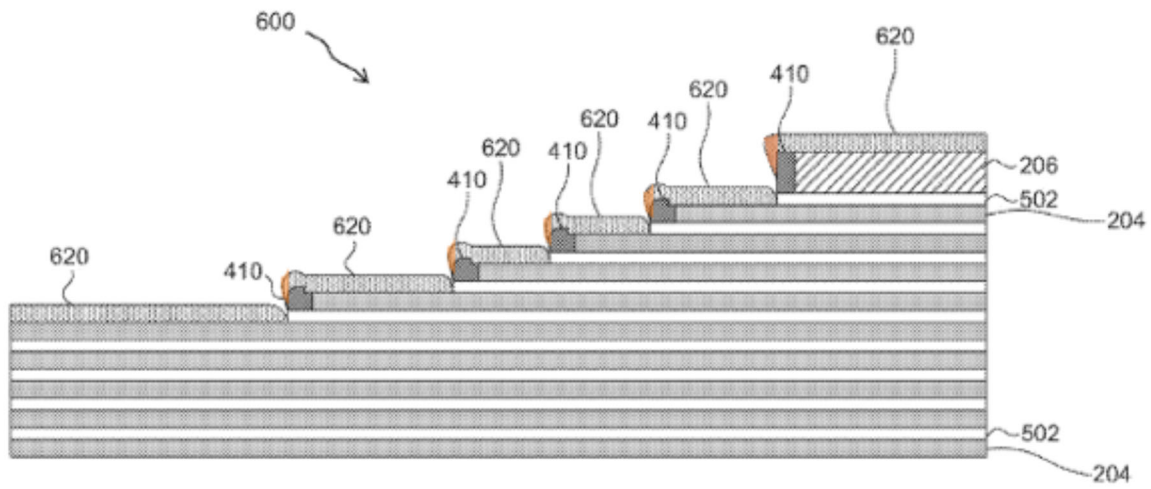
in Figure 6 as made or shaped by a lithographic process. This creates an interface between each of the structures 620 and a respective insulating material 502. This is shown below in annotated Figure 6.



36. A dielectric material is deposited onto the staircase structure so that the ensuing “layer 620 has poor step coverage on staircase structure 500.” ’838 patent 8:56-57. A POSITA would have understood what the ’838 patent meant by “poor step coverage.” *See, e.g.,* Plummer (Ex. 2028) 509-510. The term describes the non-conformal profile of the layer deposited on patterned surfaces when the flux of reactive gas-phase molecules arriving at the patterned surface has both a directional and an isotropic component. *Id.* 544, 552, 577; *see also* Ex. 1021 (Yun) 9:41-65. Under such deposition conditions, a stair step shadows the step below it thus limiting the flux of depositing molecules arriving there from the gas phase. This is particularly acute at the sidewall of all the steps. As

a result, the vertical sidewall surfaces of the steps accumulate less material than the horizontal flat surfaces. Depending on the balance of fluxes (directional vs. isotropic), the sidewalls may be covered by a non-uniform or even discontinuous layer of dielectric material, with excess thickness at the upper portion of the sidewalls, thus creating an overhang. The '838 patent shows that clearly in Figure 6, where I highlighted the overhang in orange color. '838 patent 8:46-9:12, 12:37-49, Fig. 6. Note that before the deposition of dielectric layer 620, the steps leading up to Figure 6 consist of a composite of materials 410 and 204 stacked on top of layer 502. In short, this approach relies on employing a (gas-phase) vapor deposition technique with both directional and isotropic flux components, where the two flux components can be carefully balanced (optimized) to tune the deposited layer surface curvature in the vertical direction. Plummer 552. The '838 patent contemplates multiple embodiments of the profile shape and continuity of the dielectric layer 620 to be deposited, all resulting in a dielectric layer with a curved surface at the bottom corner of each step. '838 patent 8:46-9:12. To obtain such profiles, a POSITA must select and optimize specific gas-phase deposition techniques capable of supplying both directional and isotropic fluxes of depositing molecules to the staircase structure, such as plasma-enhanced CVD and directional sputter deposition (PVD) among others.

Plummer 547-554, 590-600.

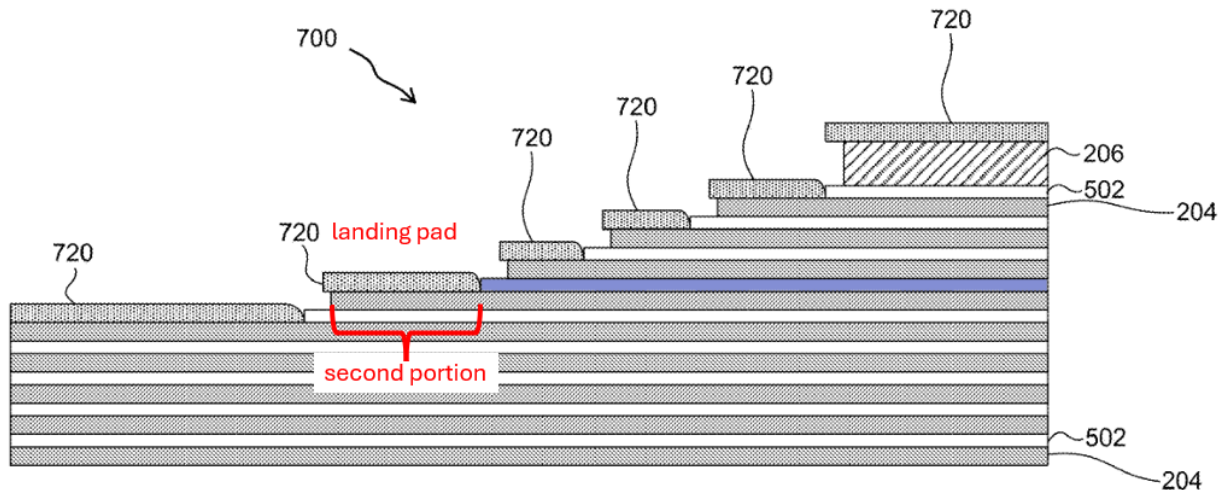


'838 patent Fig. 6 (annotated).

37. The overhang reduces (shadows) further the delivery of additional depositing molecules to the bottom corner of each step from the space above the structure. As the overhang grows out, progressively less-and-less material is deposited directly below it, resulting in a layer (620) with a surface that curves into the corner by the step sidewall, precisely where layer 620 meets the insulating layer 502 of the respective layer stack. '838 patent 8:46-9:12, 12:37-49, Fig. 6.

38. Then, the spacers 410 and a portion of the dielectric layer 620 are removed to form landing pads 720 such that landing pads 720 remain in contact with the sacrificial layer 204. '838 patent 9:13-39, 12:50-62, Fig. 7. This is shown in annotated Figure 7 below. An insulating layer 502 is colored blue and

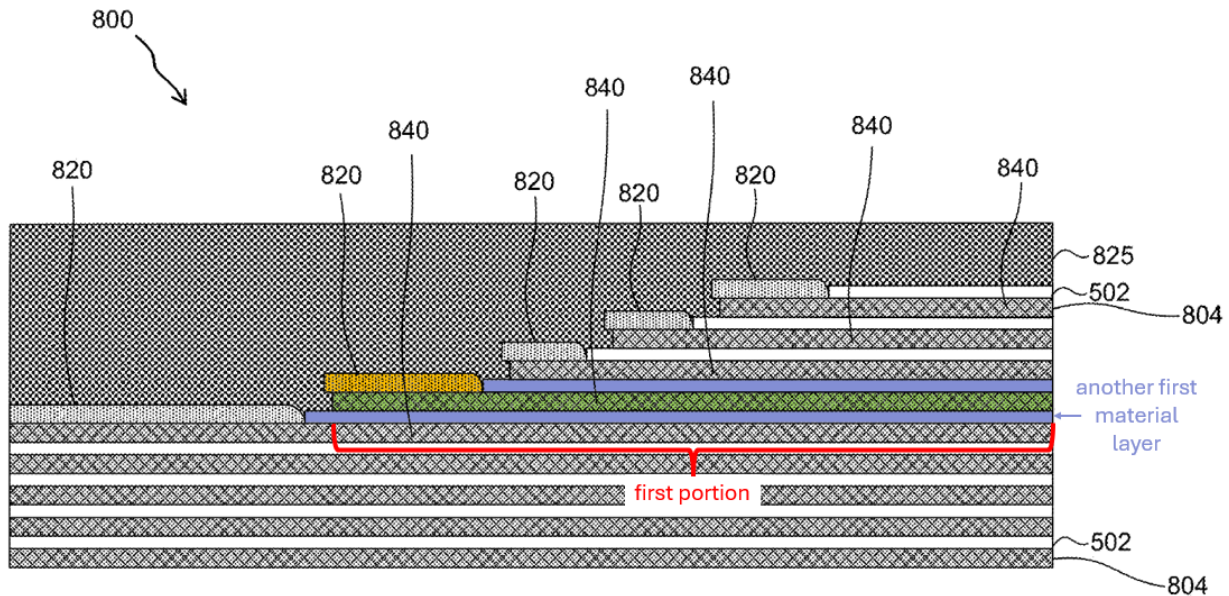
the landing pad is identified over the “second portion” of the second material layer, which was the “exposed portion” discussed above, which terminates on one end at the interface between the landing pad and the insulating material 502. This is the “second portion” as claimed in claims 1 and 12.



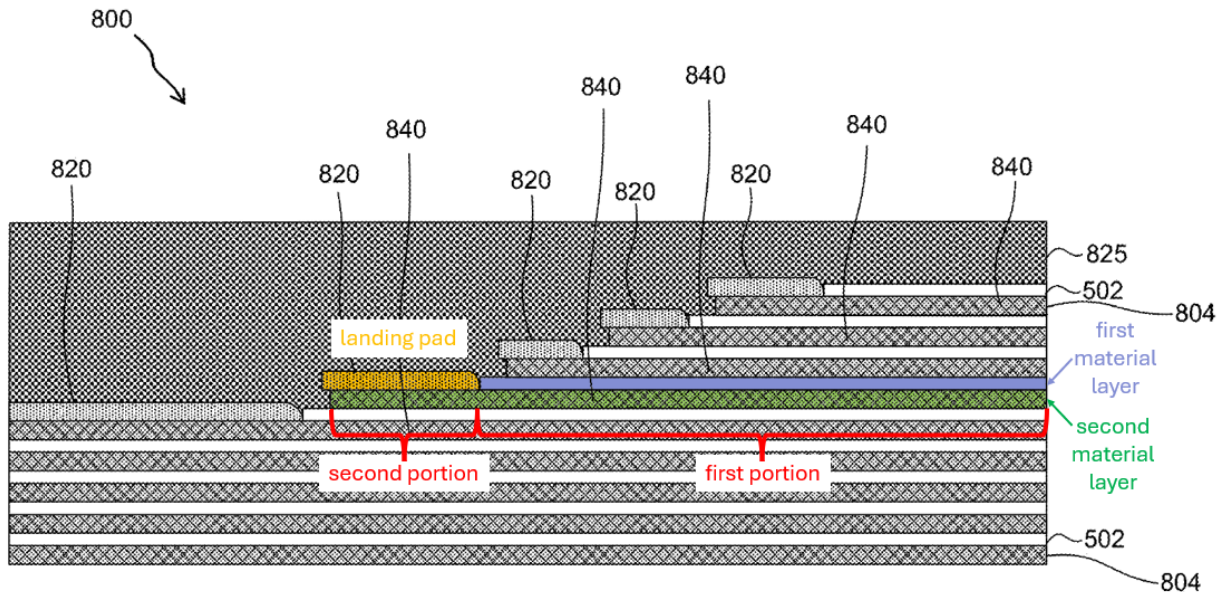
39. Then, an insulating dielectric layer is formed over the entire structure and word lines are formed in the staircase structure by removing the sacrificial layer and the remaining dielectric layer 620/landing pads 720 to form recesses and then filling the recesses with one or more conducting material layers. '838 patent 9:40-10:48, 12:63-13:13, Fig. 8.

40. The specification also notes that “[b]oth landing pad 720 and sacrificial layer 204 of the SC layer are disposed over a portion of insulating layer 502 of another vertically adjacent SC layer.” *Id.* 9:21-24; *see also id.* 1:66-2:1. This is shown in annotated Figure 8 below, where the “first portion” labeled

is not of the second material layer, as in claims 1 and 12, but of the “another first material layer” as recited in claims 6 and 20, which is the lower blue layer.



41. At the end of this process, a structure is formed as depicted in Figure 8 below, in accordance with claims 1, 12, and dependent claims. The “first material layer,” annotated in blue, is over a “first portion” of the “second material layer,” annotated in green. The “landing pad,” annotated in orange, is over a “second portion” of the “second material layer.” As explained above, the process described in the specification results in the “first portion” and the “second portion” being distinct, separate, and non-overlapping.



42. Figure 8 notes that it is depicting the x-z plane of the staircase structure. *See* '838 patent Fig. 8. The y-axis is into and coming out of the page. To avoid confusion, I note that the axes in Figure 8 (and other figures of the '838 patent) are different from the axes in the figure from page 134 of Ex. 1012, discussed earlier in my declaration. In the '838 patent, the x-axis runs along the steps toward the memory cells, whereas in the figure from page 134 of Ex. 1012 shown earlier, the x-axis runs along the steps, but perpendicular to the direction from the end of the steps toward the memory cells. In other words, the x-axis and y-axis are inverted when comparing the figures of the '838 patent and the figure from page 134 of Ex. 1012.

43. Of particular note, Figure 8 of the '838 patent shows that the landing pads have a curved side surface in the x-z plane, which is in contact with each respective insulating layer 502. As can be seen, the curvature in the x-z plane

provides further separation between consecutive conductive material layers as compared to a structure where there was no curvature. This is depicted below, by zooming into one step. The colors used in these figures match those in the Petition and Dr. Lee's declaration, with the "first material layer" colored blue, "second material layer" in green, and the landing pad in orange. On the left is shown a zoom-in portion from Figure 8 of the '838 patent, while on the right I have edited the figure such that 820 has no curvature. The arrows in both Figures mark the physical separation of the landing pad from the upper word line. The corresponding distances are shorter in the picture on the right, which indicates a heightened risk of electrical shorting between the word lines in the absence of curvature. Thus, the curved side surface of the landing pad 820 illustrates an additional benefit of the '838 patent. This additional margin leads to yield and manufacturing cost improvements because of fewer short-circuit defects. *See* '838 patent 1:39-46. The Petition argues this as well. *See* Pet. 45, 83-84; Ex. 1003 ¶¶247, 482.

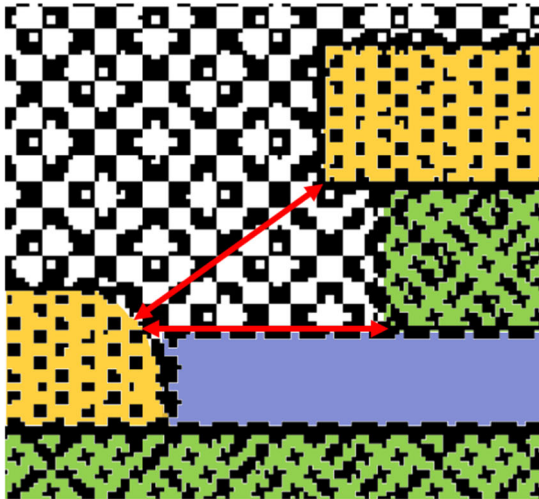
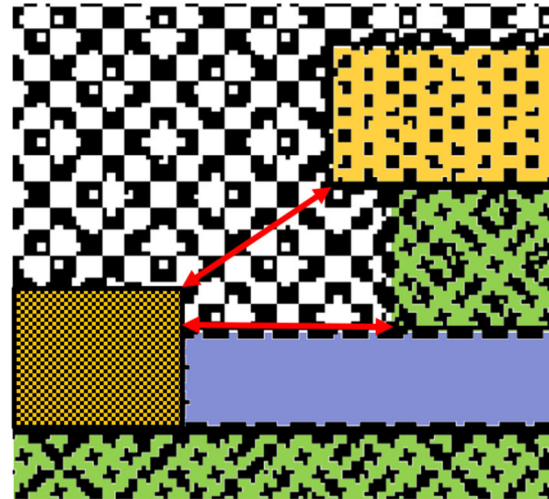
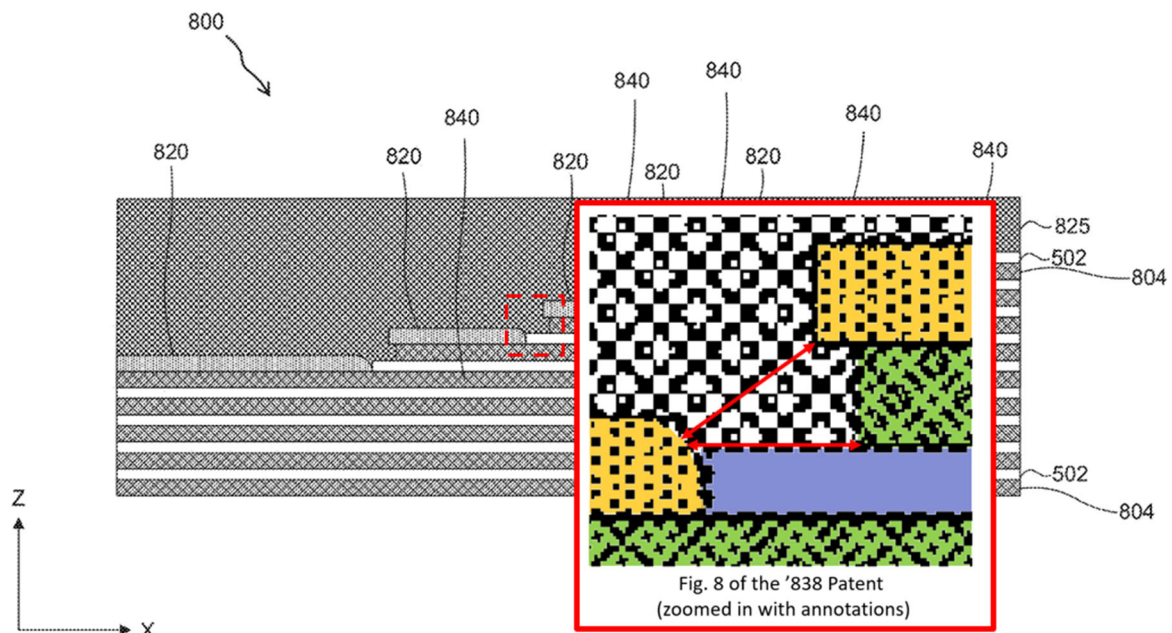


Fig. 8 of the '838 Patent
(zoomed in with annotations)



Other Structures

44. As shown in Figure 8 (zoomed in and annotated below), the claimed invention maintains distances (shown in red) between adjacent conductive layers which include the landing pad (conductive layers in green and orange), thereby preventing short-circuits between adjacent layers.



45. Additionally, in the area of landing pads 820, the combination of the conductive material(s) produces a thicker layer. This thicker portion helps prevent punch-through during the fabrication of the pad contacts thus avoiding short-circuits to word lines underneath the pads. *See* '838 patent 5:19-48; Ex. 1003 ¶¶119, 440.

46. I note that Dr. Lee agreed that the thicker pads prevent damage to the pad during the manufacturing process.

Q. Does increasing the thickness of the pad help prevent damage to the pad during the manufacturing process?

A. Yes. Of course.

Q. Okay.

A. Because those pads are eventually used to form the conductive veer, meaning the vertical conduit. And if the pad is thin, that it can -- you know, first you do an oxide etch of the field oxide, and then you deposit the -- the content material, conductive material. Those process, if the contact pad is thin, can easily damage the contact region and such that the -- **you would have a potential shorting issues.** Ex. 2031 (Lee '666 Dep.) 168:17-169:10.

47. The Petition says that “the specification explains that the terms ‘on,’ ‘above,’ and ‘over’ ‘should be interpreted in the broadest manner such that ‘on’ not only means ‘directly on’ something, but also includes the meaning of ‘on’

something with an intermediate feature or a layer therebetween.” Pet. 20 (quoting '838 patent 4:4-12). That same part of the specification also states, “Moreover, ‘above’ or ‘over’ not only means ‘above’ or ‘over’ something, but can also include the meaning it is ‘above’ or ‘over’ something with no intermediate feature or layer therebetween (i.e., directly on something).” '838 patent 4:8-12. A POSITA would understand this to mean that, for example, feature 1 is over feature 2 regardless of whether feature 1 is directly on and in physical contact with feature 2, or is separated from feature 2 by an intermediate feature or layer.

VII. Claim Construction

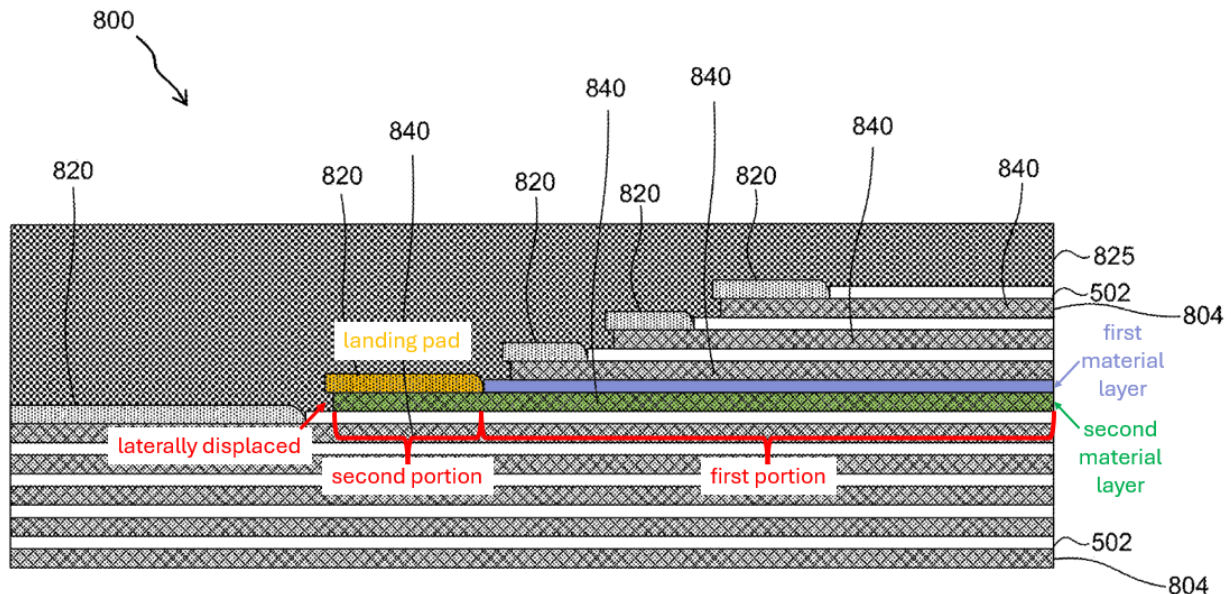
A. Terms involving “first” and “second portion” “of the second material layer”

48. I have been asked to opine on how a POSITA would construe the term “first portion of the second material layer” when read in the context of the claims, specification, and prosecution history. It is my opinion that a POSITA would construe the term “first portion of the second material layer” to mean “a portion of the second material layer beneath the first material layer that is separate and distinct from the second portion of the second material layer.”

49. I have also been asked to opine, in the alternative, how a POSITA would construe the terms “wherein the first material layer is disposed over a first portion of the second material layer” and “a landing pad disposed over a second

portion of the second material layer” when read in the context of the claims, specification, and prosecution history. It is my opinion that a POSITA would construe the term “wherein the first material layer is disposed over a first portion of the second material layer” as “wherein the first material layer is disposed over a first portion of the second material layer but not a second portion of the second material layer” and the phrase “a landing pad disposed over a second portion of the second material layer” as “a landing pad disposed over the second portion of the second material layer but not the first portion of the second material layer.”

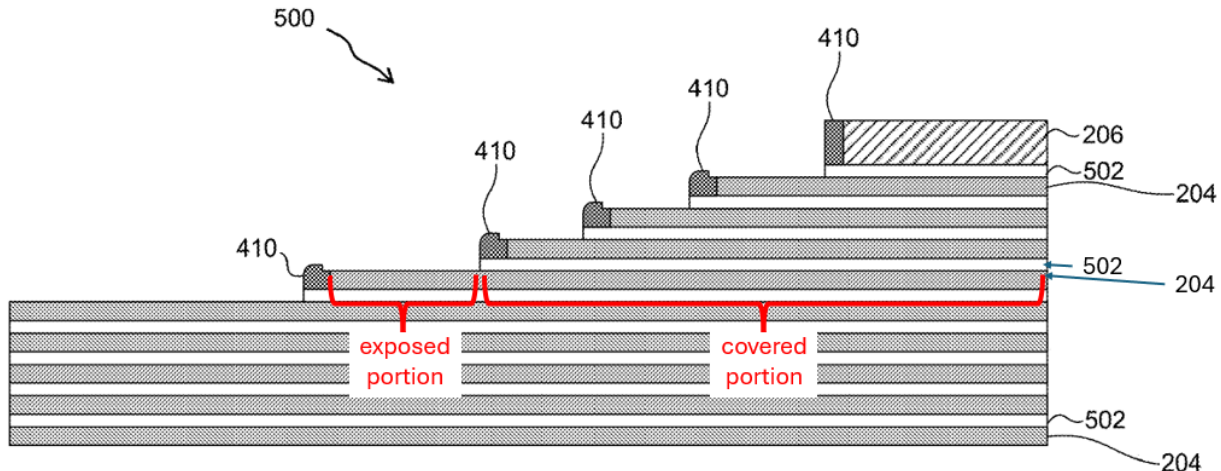
50. The claim language itself supports my construction. In relevant part, claims 1 and 12 both recite the following limitations: “a first material layer and a second material layer, wherein the first material layer is disposed over a first portion of the second material layer; and a landing pad disposed over a second portion of the second material layer, wherein the landing pad comprises a first side surface and a second side surface, and wherein the first side surface is in contact with the first material layer and the second side surface is laterally displaced from a side surface of the second portion of the second material layer.” As explained in the previous section, the process described in the specification results in the “first portion” and the “second portion” being distinct, separate, and non-overlapping. Figure 8 of the '838 patent depicts the recited structure in this regard, as annotated below.



51. I note that the claims recite a “first portion,” and separately recite a “second portion,” which signifies to a POSITA that these are two distinct portions of the “second material layer.” For example, the claims do not use generic language regarding these portions, but instead they use ordinal language that signifies separateness. In addition to the labels “first” and “second,” the rest of the claimed structure reinforces this understanding because there are different structures over the distinct portions and a defined interface between those structures signifying the boundary between the first portion and the second portion. Thus, the way the claims are written implies that the “first portion” is distinct and separate from, and not overlapping with the “second portion.” Nothing in the claims suggests a different understanding.

52. If the “first” and “second portions” could overlap, then the requirement of a “first” and “second” portion would become meaningless and redundant. The claims provide a specific position of the (1) “first portion” as under the “first material layer and (2) “second portion” as under the “landing pad.” If a “first portion” was able to be beneath the landing pad, then it would be redundant with the second portion. Likewise, if the second portion can be under the first material layer, then it becomes the same as the “first” portion. In short, the “first portion of the second material layer” must be separate and distinct from the second portion of the second material layer as otherwise, the limitation would be rendered optional and nonexistent.

53. This is also consistent with the description of the claimed structures and their formation in the specification, which I detailed in the previous section. In particular, during the described process, an exposed portion of the insulating layer of each step is removed to expose a top portion of sacrificial layer underneath, as shown in annotated Figure 5 below. '838 patent 8:34-45, 12:29-36, Fig. 5.

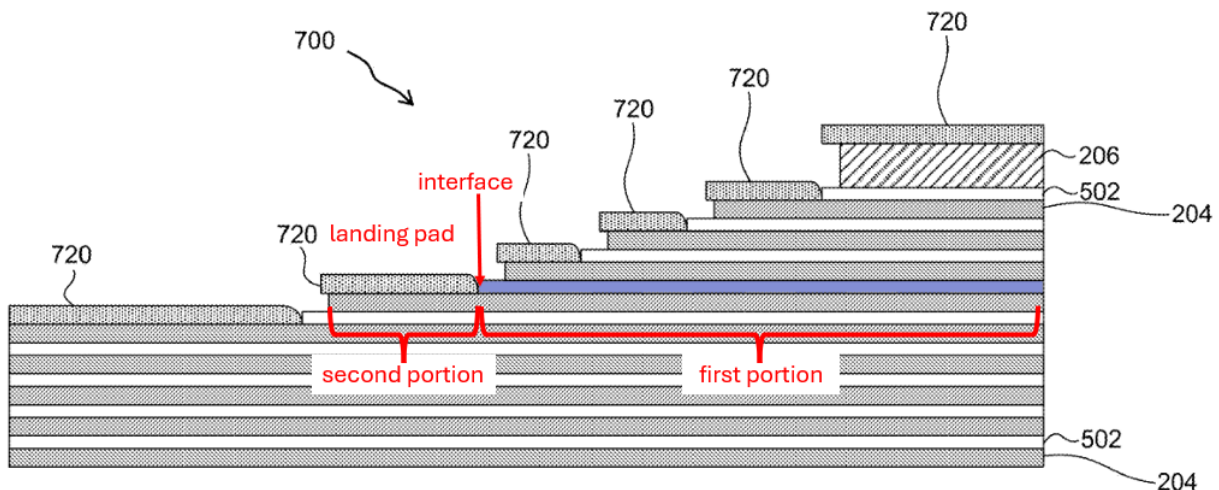


This creates two distinct and separate portions of the sacrificial layer 204: (i) a first portion that is still covered by insulating material 502 and (ii) a second portion that is the exposed portion shown above. These two portions are separate, distinct, and non-overlapping for the entirety of their extents in the x-direction (left-right in the above figure and the other figures of the '838 patent). These parts of the sacrificial layer 204 are ultimately the “first portion” and “second portion” of the second material layer as claimed in claims 1 and 12 of the '838 patent. As this ultimately results in distinct, separate, and non-overlapping “first portion” and “second portion” parts of the second material layer, this further confirms to a POSITA that the “first portion” and “second portion” in claims 1 and 12 are separate and distinct portions of the second material layer that do not overlap.

54. After further steps described in the previous section, landing pads are formed only over the previously exposed portion (now labeled “second

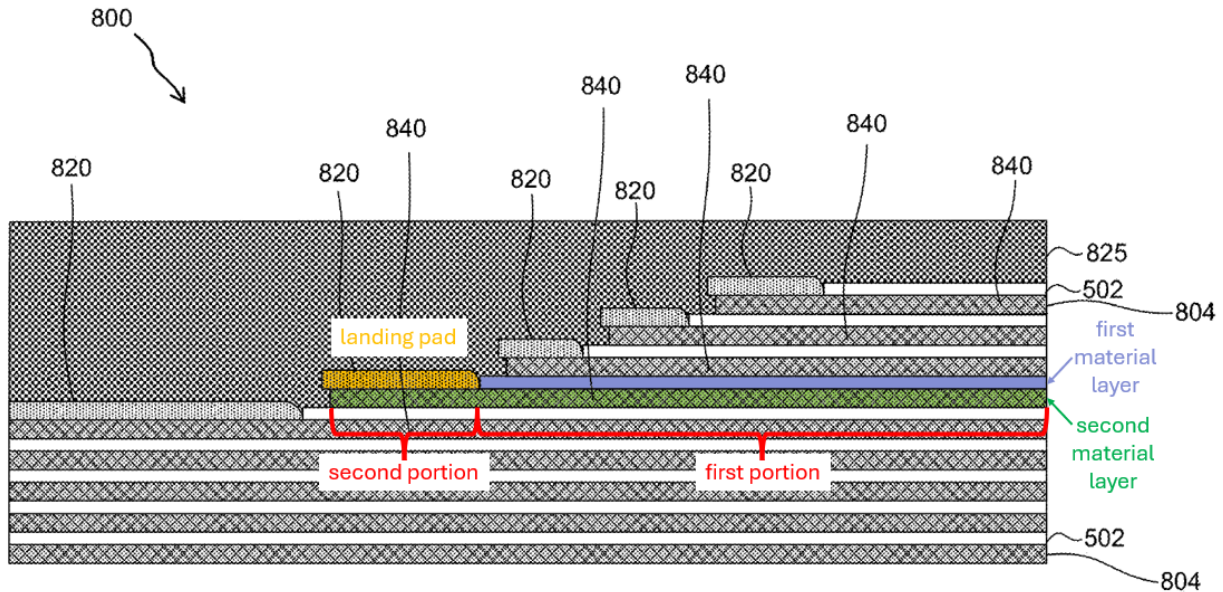
portion”) of the sacrificial layer, as depicted in annotated Figure 7 below.

Notably, the portion of the underlying layer 204 over which the landing pad is formed is distinct and separate from the portion over which the insulating layer 502, annotated in blue, is disposed. These correspond to the claimed “second portion” and “first portion” respectively, and with the interface of the landing pad 720 and the insulating layer 502 delineating the two portions underneath.



55. After further steps described in the previous section, the resulting structure is formed, as shown in Figure 8 annotated below. Consistent with its formation, there are two distinct and separate portions of the second material layer, which are non-overlapping. There is no description of forming the structure in a way where the “first portion” and “second portion” would overlap or otherwise not be distinct and separate, or where the “first material layer” and the “landing pad” overlap. In short, the manufacturing process described in the

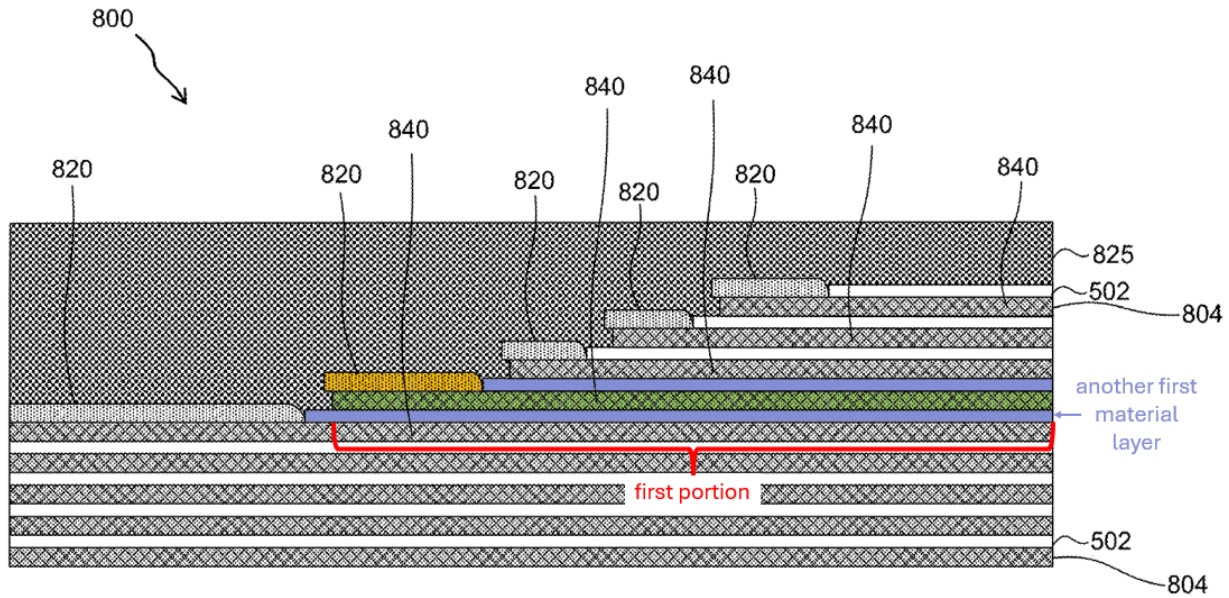
'838 patent can only result in “a first portion of a second material layer” that is separate and distinct from the “second portion.”



56. This is also how the patent itself describes the resulting structure. The specification explains that “[t]he staircase structure includes a plurality of layer stacks, where each layer stack includes a first material layer disposed ***over a first portion*** of the second material layer.” ’838 patent 1:47-50 (emphasis added). That is one feature of the staircase structure. But the specification continues, stating that “[t]he staircase structure ***further includes*** a plurality of landing pads respectively disposed on the plurality of layer stacks, where each landing pad is disposed ***over a second portion*** of the second material layer of a respective layer stack.” *Id.* 1:50-54 (emphasis added). So, in addition to the “first portion,” the staircase structure “further includes” the “second portion.”

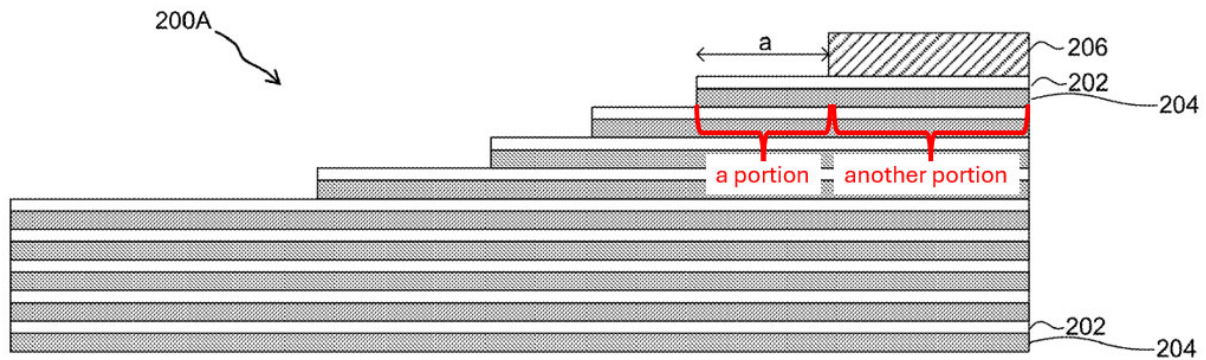
This mirrors the claims, which also recite specifically identified portions of the “second material layer.”

57. A POSITA would also recognize a consistent usage of distinct “portions” of layers throughout the '838 patent. Other claims, such as claims 6, 8, 9, 15, and 20 all discuss separate and distinct portions of layers. Claims 6 and 20 recite that “the second material layer is disposed over *a first portion* of another first material layer.” '838 patent 14:5-7, 15:17-19 (emphasis added). This is shown below in annotated Figure 8, with the “first portion” of the lower first material layer identified. A POSITA would understand the meaning of “first portion” in claims 6 and 20 consistent with the use of “first portion” and “second portion” in claims 1 and 12: that they refer to distinct portions of the referenced material layer. Thus, the second material layer, annotated in green below, is over a portion of the first material layer below it, annotated in blue, and is not over the entirety of the lower first material layer.



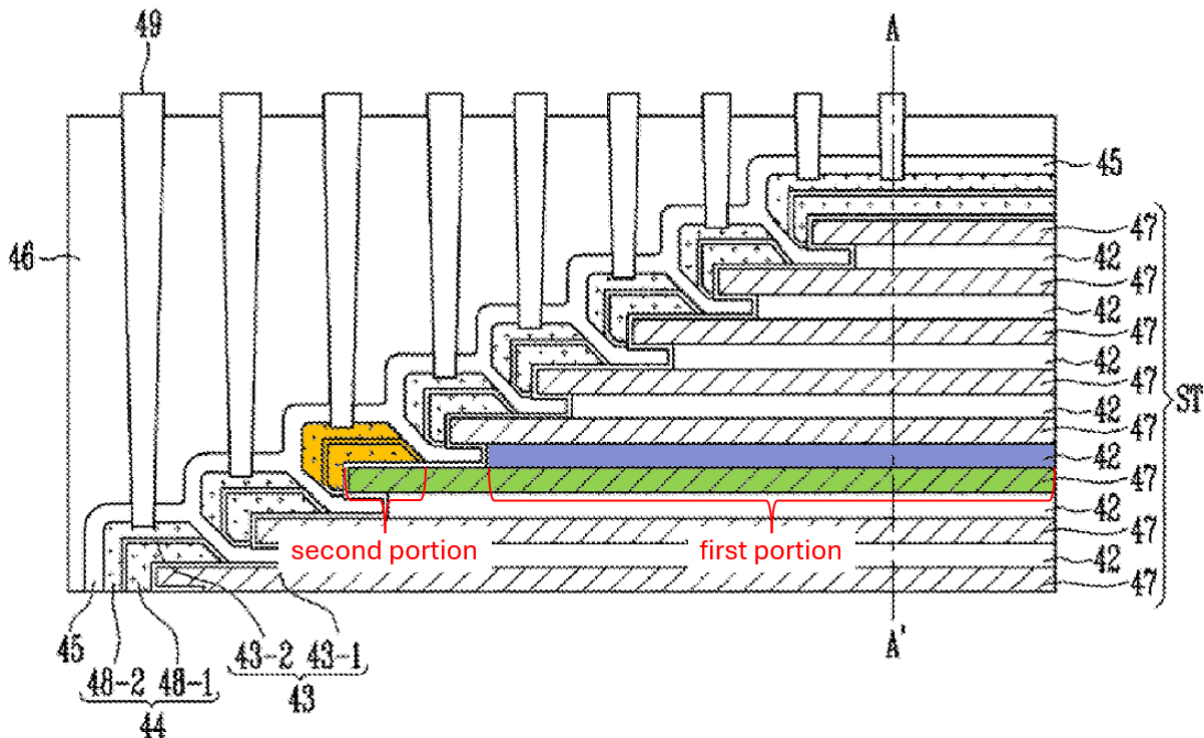
58. The specification describes this arrangement in a similar and consistent way. The specification states that “[w]ordline layer 804 of an SC layer is disposed over *a portion* of insulating layer 502 of another vertically adjacent SC layer.” ’838 patent 9:53-55 (emphasis added); *see also id.* 1:66-2:1, 9:21-24.

59. As another example, in describing a part of the process of forming the claimed structure, the specification describes that “*a portion* of a top-most SC layer of staircase structure 200A is exposed and *another portion* of the top-most SC layer is covered by hard mask layer 206.” *Id.* 7:12-15 (emphasis added). The hard mask layer 206 is shown over the “another portion” while the “a portion” is exposed. This is shown in annotated Figure 2A below. Again, the patent describes two distinct and non-overlapping portions of the structure with an extension in the x-direction. This would also signal to a POSITA that that is the correct understanding of “first portion” and “second portion” in claims 1 and 12.



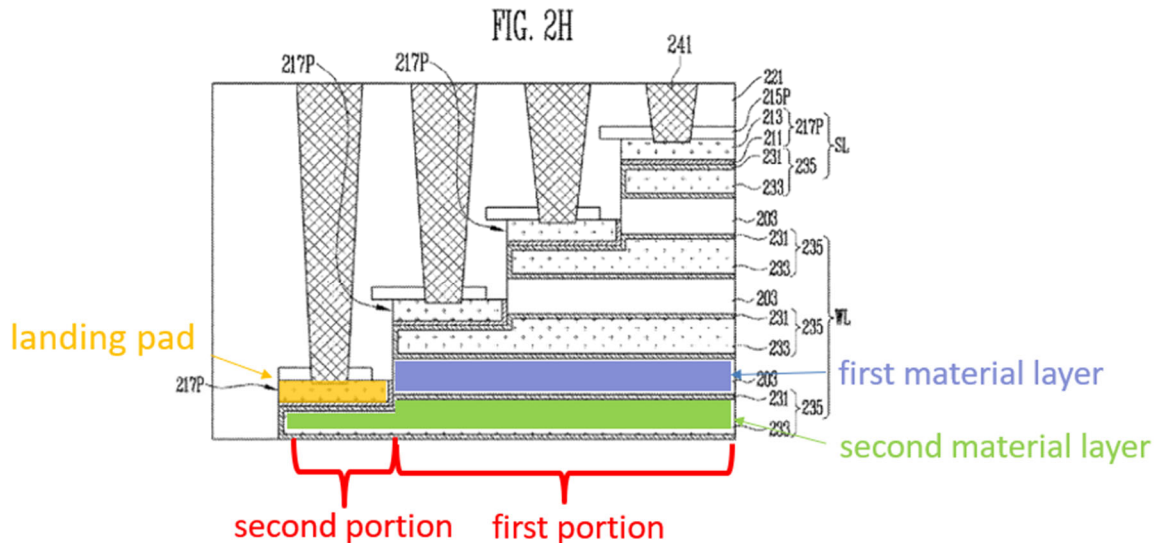
60. I have also reviewed the file history of the '838 patent in Exhibit 1002. When originally filed, claim 1 was similar to issued claims 1 and 12 in the sense that it recited an arrangement between the first material layer, the landing pad, and first and second portions of the second material layer. Ex. 1002 39. The originally-filed claim 1 was initially rejected as anticipated by US 2016/02180107 ("Lee-107" (Ex. 1014)). Ex. 1002 153-54. The examiner relied on Figure 4C of Lee-107, which is annotated below. The annotations show how the examiner applied the structure shown below against the originally-filed claim 1. Importantly, the examiner identified the structures of the prior art such that there were distinct, separate, and non-overlapping "first portion" and "second portion" of the second material layer, annotated in green below. Thus, a POSITA would understand that the examiner understood the claims such that the "first portion" and the "second portion" were distinct and separate from each other.

FIG. 4C



61. During prosecution of a related patent application, U.S. Application No. 16/126,956, the claims recited “a first material layer disposed over a first portion of a second material layer” and “each landing pad disposed over a second portion of the second material layer.” Ex. 2022 (’16/126,956 FH) 4. During examination, the Examiner rejected the claims based on US 9,373,540 B2, issued to Hyun (Ex.1016) (“Hyun”). The Examiner found that Hyun taught “a first material layer (203) disposed over a first portion of a second material layer (235, which is 231+233); and a plurality of landing pads (217P) respectively disposed on the plurality of layer stacks, each landing pad disposed over a second portion of the second material layer (235).” Ex. 2022 4. I have identified below how the

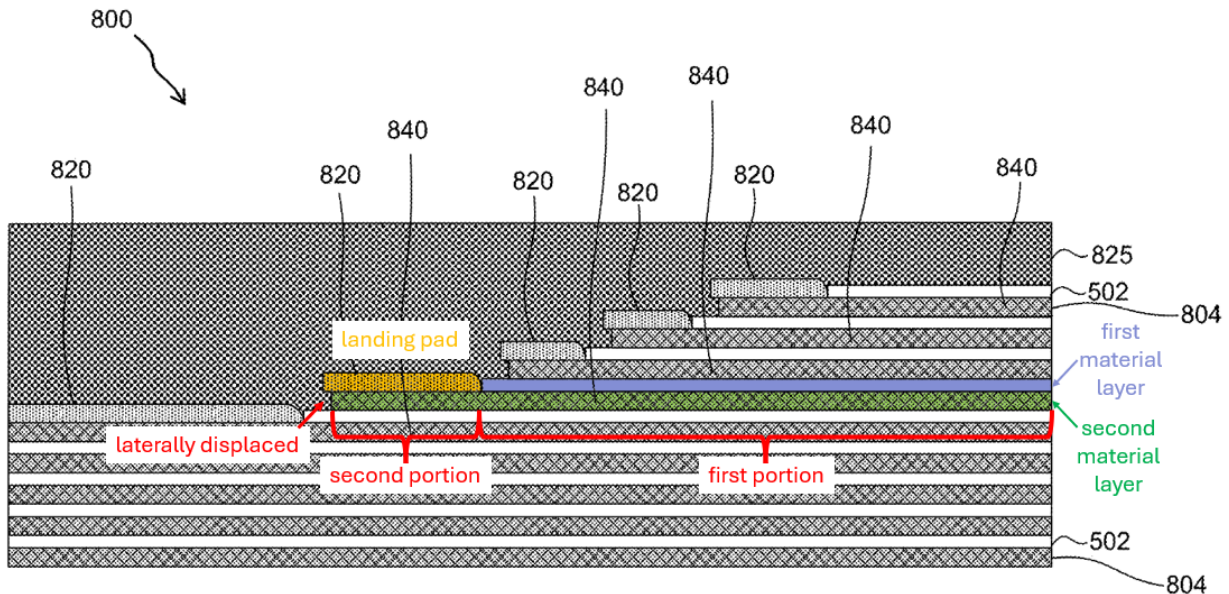
Examiner matched Hyun to those pending claims. The Examiner's rejection of these claims in view of Hyun further confirms that a POSITA would have understood the claimed "first" and "second" portions are separate and distinct.



Ex.1016 Fig. 2H (annotated).

62. Thus, in light of the above and the description of the process in the previous section, in my opinion, a POSITA would understand claims 1 and 12 to be consistent with the annotated Figure 8 below, including that the term "first portion of the second material layer" to mean "a portion of the second material layer beneath the first material layer that is separate and distinct from the second portion of the second material layer." And in the alternative, that the term "wherein the first material layer is disposed over a first portion of the second material layer" should be construed as "wherein the first material layer is disposed over a first portion of the second material layer but not a second portion

of the second material layer” and the phrase “a landing pad disposed over a second portion of the second material layer” as “a landing pad disposed over the second portion of the second material layer but not the first portion of the second material layer.”



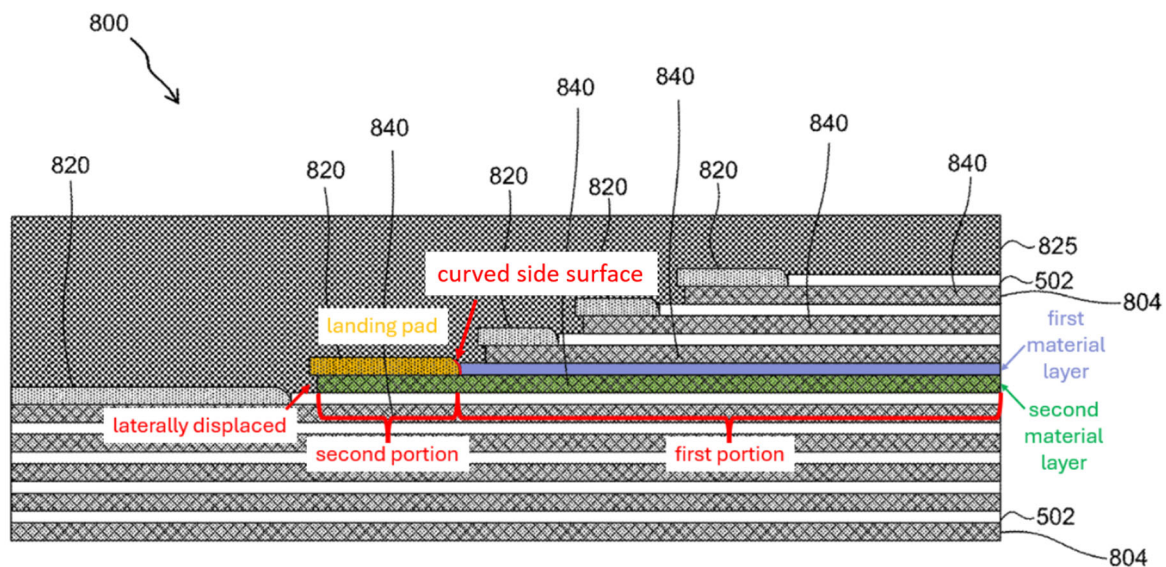
B. “curved side surface”

63. I have been asked to opine on how a POSITA would understand the term “curved side surface” when read in the context of the claims, specification, and prosecution history. It is my opinion that a POSITA would understand the term “curved side surface” to mean a “vertical surface curved along a direction (e.g., the z-axis) perpendicular to the top surface of the structure.”

64. Looking at the claims first, a POSITA would understand that a “curved side surface” is a vertical surface. In particular, the claims of the ’838

patent use the term “bottom” when describing a horizontal surface and “side” when describing a vertical surface.

65. Claim 12, (which claim 13 depends on), claims a landing pad having a “first **side surface**” and a “second **side surface**.” That “first **side surface**” is “in contact with the first material layer,” and in claim 13 “comprises a curved **side surface**.” The landing pad the first material layer contact at the landing pad’s “first **side surface**,” and both the landing pad and first material layer are “disposed over ... the second material layer.” A POSITA would have understood this means the landing pad and first material layer are in contact at a vertical surface because it is a side surface. Figure 8 depicts this claimed arrangement below as I have annotated below.



66. Claims 1, 2, and 11 further confirm that the “curved side surface” is vertical and not horizontal as they contrast “side surfaces” from “bottom surface.” Claim 1 states “the landing pad comprises **a first side surface** and **a second side surface**,” surfaces a POSITA would understand to be vertical surfaces. Claim 2 depends from claim 1 and states “a dielectric layer in contact with **a bottom surface** of the landing pad, **the second side surface** of the landing pad, and **the side surface** of the second portion of the second material layer.” As such, the claims themselves show that a “bottom surface” is a horizontal surface, and a first and second “side surface” are vertical. Claim 11 makes a similar distinction, claiming “a dielectric layer in contact with **a bottom surface** of the landing pad, **a side surface** of the landing pad, and **a side surface** of the second portion of the conductive layer.” As claim 13 uses similar language to these claims, a POSITA would interpret the use of the similar terms the same across the claims.

67. The specification supports my opinion as well. In particular, the patent references a “top surface” or “bottom surface” 28 times. Every reference to a “top” or “bottom” surface would have been understood to refer to a horizontal surface. Meanwhile, the '838 patent refers to a “side” surface (without the modifier “top” or “bottom”) 60 times, each time referring to a vertical

surface. This is detailed in my discussion below and reflects consistent usage throughout the specification of any “side surface” being a vertical surface.

68. Only one section (found in column 4) of the specification refers to a “side” (not “side surface”) as a horizontal surface. However, in each of those instances, a modifier “top” or “bottom” is also used, further reflecting that a “side surface” without one of those modifiers is a vertical surface. Moreover, in context, that passage is discussing a “top surface” and a “bottom surface,” further confirming that the “top side” and “bottom side” are referring to the “top surface” and “bottom surface” being described.

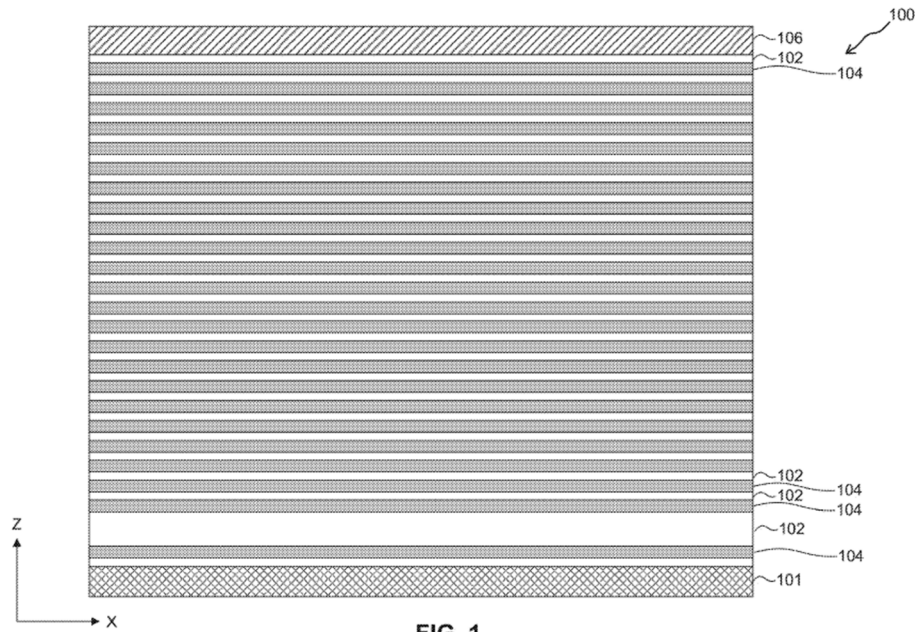
The top surface of the substrate is where a semiconductor device is formed, and therefore the semiconductor device is formed at a **top side** of the substrate. The bottom surface is opposite to the top surface and therefore a **bottom side** of the substrate is opposite to the **top side** of the substrate....

As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer has a **top side** and a **bottom side** where the **bottom side** of the layer is relatively close to the substrate and the **top side** is relatively away from the substrate. '838 patent, 4:26-43.

69. The '838 patent distinguishes between horizontal and vertical surfaces, defining the surfaces in the vertical direction as those in “a direction (e.g., the z-axis) **perpendicular to the top surface** of the structure.”

[i]n the present disclosure, a staircase structure refers to a set of surfaces that include at least **two horizontal surfaces (e.g., along an x-y plane)** and at least **two vertical surfaces (e.g., along a z-axis)**. Each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is also adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface. Each of the horizontal surfaces is referred to as a ‘step’ or ‘stair’ of the staircase structure. A horizontal direction can refer to a direction (e.g., the x-axis or the y-axis) **parallel with a top surface** of the substrate (e.g., the substrate that provides the fabrication platform for formation of structure over it). A vertical direction can refer to a direction (e.g., the z-axis) **perpendicular to the top surface** of the structure. ’838 patent 4:47-61.

70. The ’838 patent teaches “[t]he substrate includes a **top surface** and a **bottom surface**.” ’838 patent 4:27-33. And as the ’838 patent shows in Figure 1, consistent with other parts of the specification, the “top surface” of the substrate 101 is “parallel” to “the x-axis.” *Id.* 5:56-62.



71. “FIGS. 2A-2B illustrate a cross-sectional view of staircase structures 200A and 200B” that “includes a hard mask 206 and a plurality of layer stacks 202/204.” *Id.* 7:1-4. In Figure 2A, each layer stack 202/204, called an “SC layer,” has an exposed “a top surface” (shown as a horizontal surface in green color) and an exposed “side” (shown as a vertical surface in red color inside the dashed box) as labeled below. *Id.* 7:4-11, Fig. 2A.

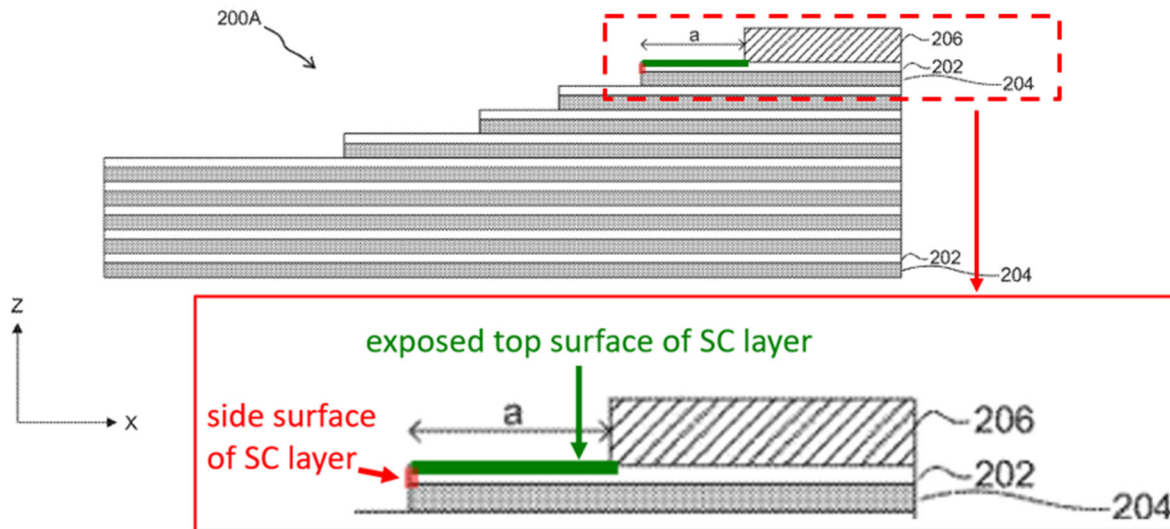


FIG. 2A

72. The '838 patent's description and depiction of Figure 3 is similarly consistent with referring to "side" surfaces as vertical surfaces while referring to "top" and "bottom" surfaces as horizontal surfaces.

FIG. 3 illustrates a cross-sectional view of a staircase structure 300 with a material layer 310 disposed thereon, according to some embodiments. Material layer 310 is conformally disposed on staircase structure 200B, including on a **top surface** of hard mask layer 206, **a side** of hard mask layer 206, **a top surface** of each SC layer (e.g. each step) of staircase structure 200B, and a recess of the each SC layer. '838 patent 8:1-7.

As I understand Dr. Lee admitted in his deposition regarding the '666 patent (which shares the same disclosures as the '838 patent) and as is shown below, the "top surface of hard mask layer 206" is a horizontal surface (green below), while the "side of hard mask layer 206" is a vertical surface (red below). Ex. 2031

62:10-63:7; '838 patent 8:1-7. The “top surface of each SC layer” 202/204 is also shown to be a horizontal surface.

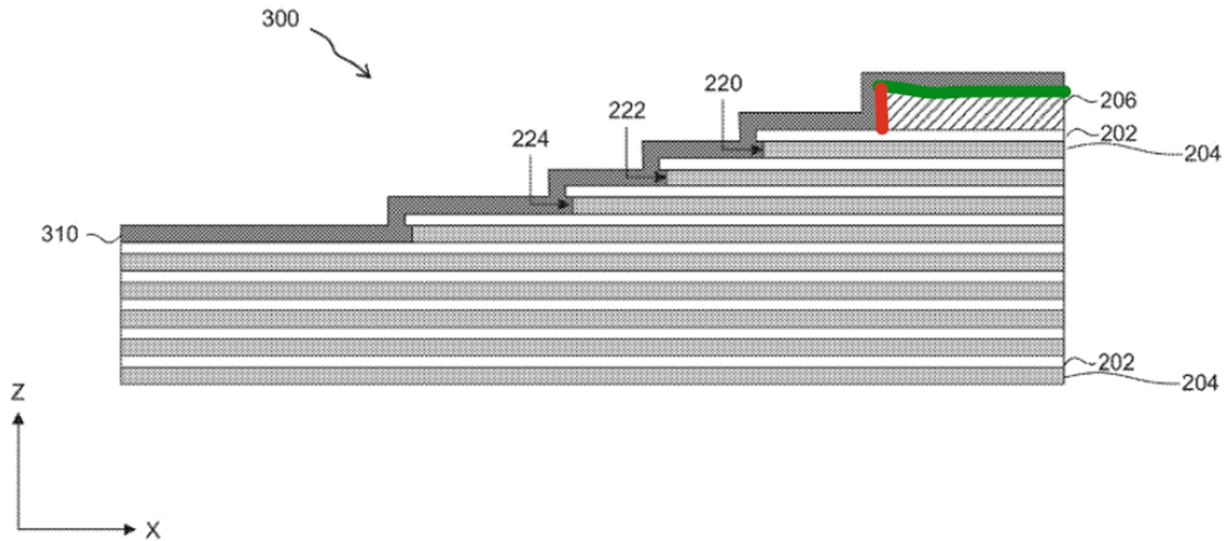


FIG. 3

Ex. 2032 (Lee '666 Dep. Ex. 1).

73. Figure 4 describes and depicts the same distinction between “side” and “top” surfaces as the rest of the '838 patent.

FIG. 4 illustrates a cross-sectional view of a staircase structure 400 with spacers 410, according to some embodiments. Each of spacers 410 is formed at a **side** of each SC layer of staircase structure 300. In some embodiments, spacer 410 is formed at a **side** of hard mask layer 206.... In some embodiments, material layer 310 is removed from a **top surface** of staircase structure 300 and a **top surface** of hard mask layer 206.... In some embodiments, spacer 410 covers a

side of sacrificial layer 204 of each SC layer of staircase structure 300. In some embodiments, spacer 410 covers a portion of a **side** of insulating layer 202 of each SC layer of staircase structure 300.”
'838 patent 8:16-33.

As I depict below, the “side of hard mask layer” (in red) is a vertical surface while the “top surface of hard mask layer” (in green) is a horizontal surface. The usage of the word “side,” specifically of sacrificial layer 204 and insulating layer 202, also refers to a vertical surface.

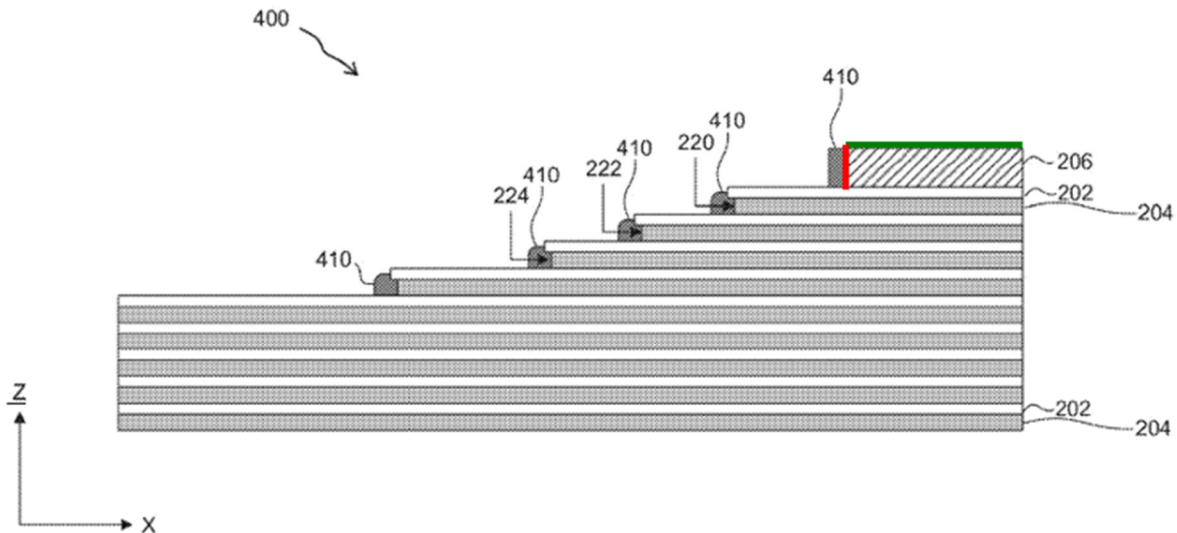


FIG. 4

74. Figure 5 also describes and depicts the same distinction between “side” and “top” surfaces as the rest of the ’838 patent.

As illustrated in FIG. 5, each SC layer of staircase structure 500 exposes a portion of a **top surface** of sacrificial layer 204 and spacer 410 of each SC layer. In some embodiments, a **side** of insulating

layer 502 of each SC layer of staircase structure 500 is exposed. '838 patent 8:41-45.

As I label below, the side of insulating layer 502 (red) is a vertical surface while the “top surface” of sacrificial layer 204 (green) is a horizontal surface.

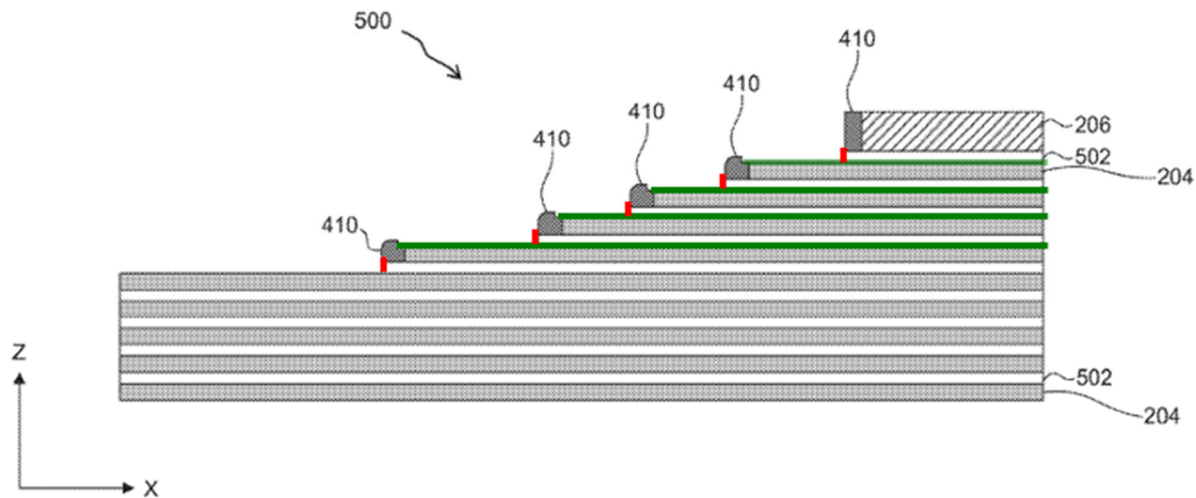


FIG. 5

75. Figure 6 also describes and depicts the same distinction between “side” and “top” surfaces as the rest of the '838 patent.

Dielectric layer 620 covers a **top surface** of staircase structure 500 and a portion of a **side** of staircase structure 500.... In some embodiments, dielectric layer 620 covers a **top surface** of hard mask layer 206, a portion of a **top surface** of sacrificial layer 204, and a portion of a **side** of insulating layers 502 of each SC layer of staircase structure 500.... The poor step-coverage includes a thickness of dielectric layer 620 that is substantially thinner at a **side** of staircase structure 600 than that at a **top surface** of staircase

structure 600. In some embodiments, a portion of spacer 410 or a portion of a **side** of insulating layer 502 of each SC layer of staircase structure 600 is exposed.... In some embodiments, a thickness of dielectric layer 620 at a **top surface** of staircase structure 600 is thinner than that of insulating layer 502 of each SC layer of staircase structure 600. '838 patent 8:46-9:7.

As I label below, the “top surface” of staircase structure 600 (green) is a horizontal surface while the “side of staircase structure 500” (red) is a vertical surface. Likewise, the “side of insulating layer 502” is a vertical surface that is covered by a “thinner” dielectric layer 620 than the “top surface.” '838 patent 8:46-9:7.

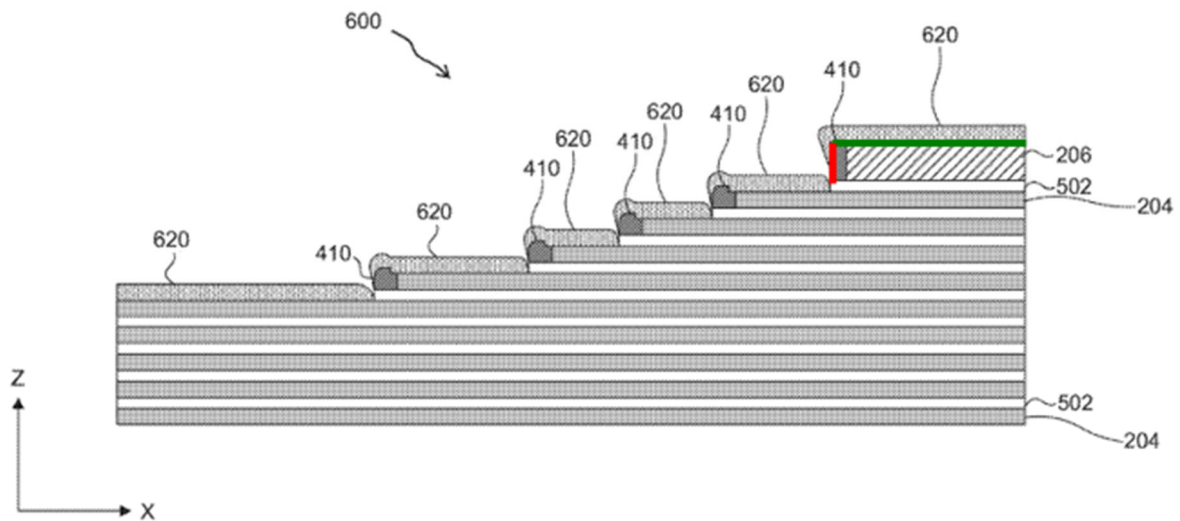
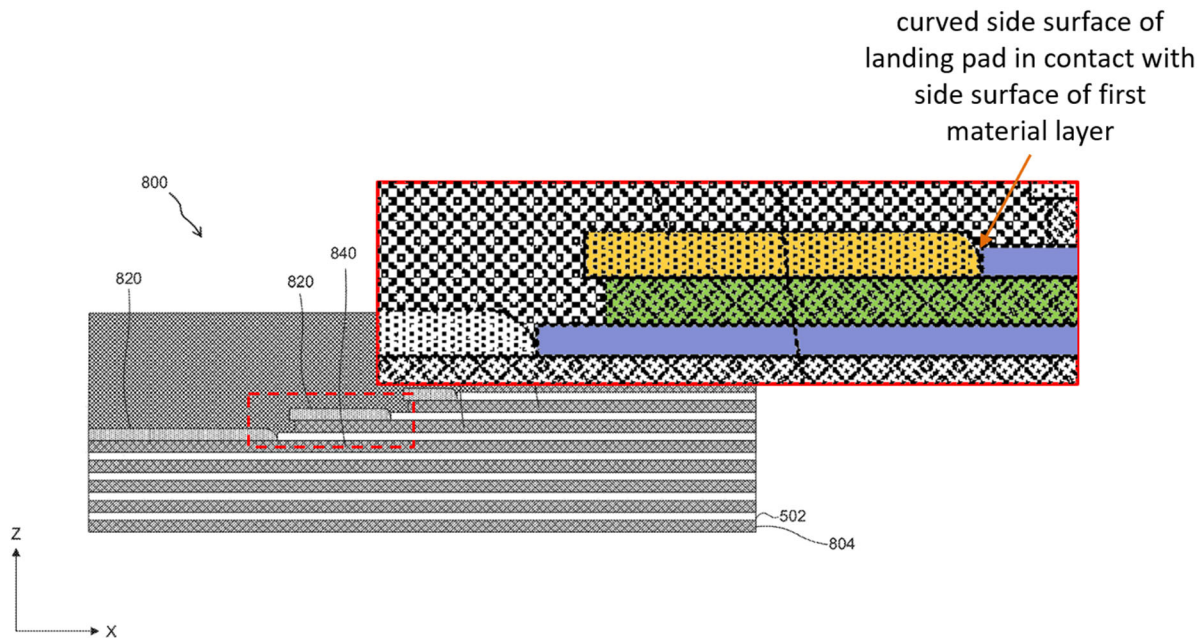


FIG. 6

76. Figure 8 is the only embodiment of the claimed “curved side surface,” as I show below. As depicted, the curved side surface is a vertical

surface that is curved away from the nominal vertical direction. The structure otherwise has a top surface, bottom surface, and other side surface.



77. Further, the '838 patent states “landing pad 820 contacts a portion of a **side** of insulating layer 502.” ’838 patent 9:66-10:3. That “side of insulating layer 502” is shown in Figure 8 to be a vertical surface in contact with the curved surface of the landing pad.

78. Figure 9 is a flowchart of method 900 for forming “memory device structures illustrated in Figs 1-8.” ’838 patent 10:49-53. Thus, the descriptions regarding Figure 9 of “top surface” and “side” surface are consistent with the descriptions of “top” and “side” surfaces I have already discussed.

- “In some embodiments, the staircase structure includes a plurality of steps, where each of the steps exposes a **side** and a portion of a **top surface** of each SC layer” *Id.* 11:60-62. That “side” is a vertical surface and “top surface” is a horizontal portion as shown in Figure 2A.
- “In operation 930, a spacer is formed at a **side** of each step of the staircase structure.” ’838 patent 12:9-10. That “side” is a vertical surface as shown in Figure 6.
- “A dielectric layer is disposed to cover a **top surface** and a portion of a **side** of the staircase structure, including a portion of a **side** of each spacer and a **side** of an insulating layer of each of the SC layers. The dielectric layer is substantially thinner at a **side** of the staircase structure than at a **top surface** of the staircase structure.” ’838 patent 12:37-44. Those “side” of “each spacer,” “an insulating layer” and “staircase structure” are all shown as vertical surfaces in Figure 8. Meanwhile, the top surface of the staircase structure is shown to be a horizontal surface.
- “In some embodiments, the dielectric layer is completely removed from a **side** of each of the SC layers.” ’838 patent 12:55-56. A POSITA would have understood “a side of each of the SC layers”

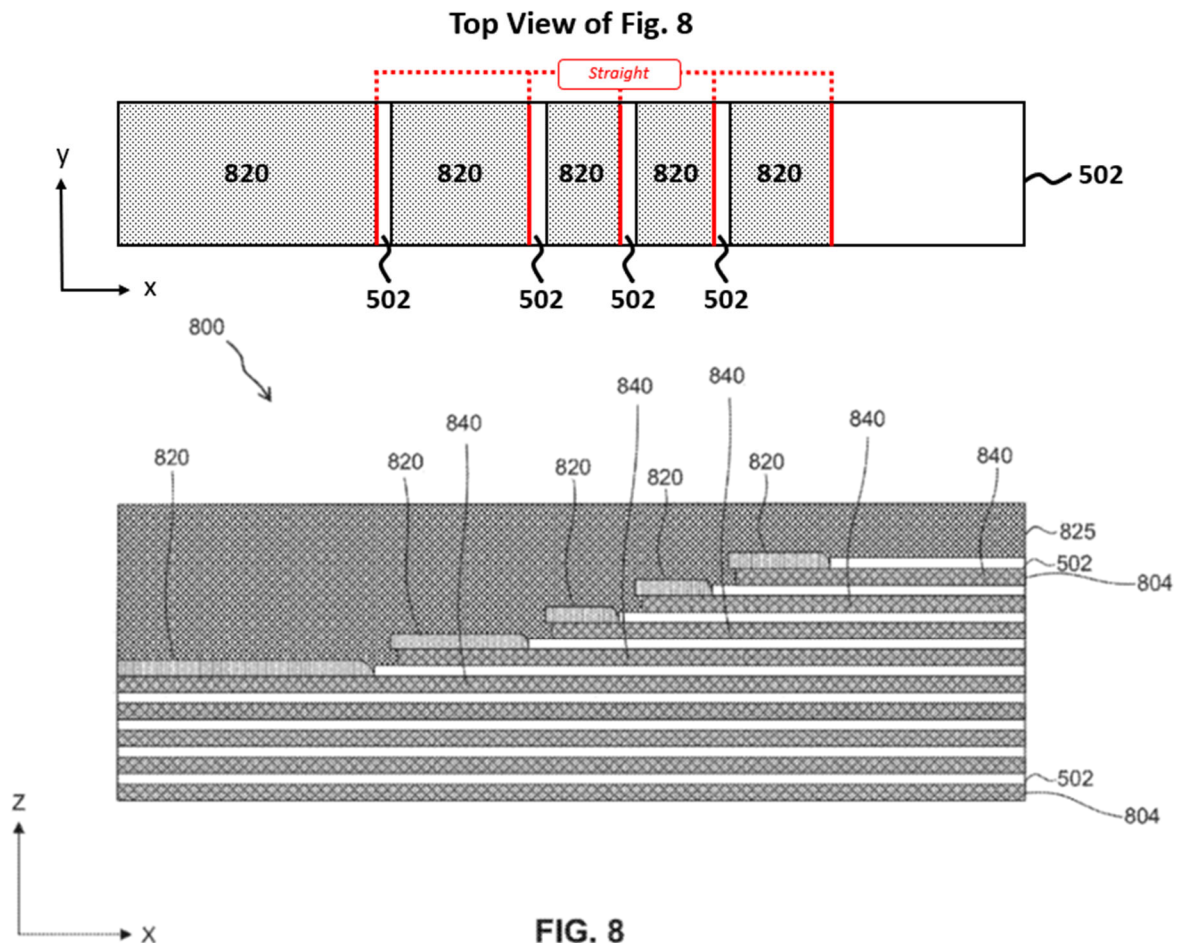
refers to a vertical surfaces shown on the left portion of each SC layer shown in Figure 6.

- “For example, the hard mask layer on a **top surface** of the staircase structure can be removed using an etch process.” ’838 patent 12:63-66. This “top surface” is a horizontal surface, as I indicated in Figure 3.

79. The methods of manufacturing taught by the ’838 patent form a curved side surface that is a “vertical surface curved along a direction (e.g., the z-axis) perpendicular to the top surface of the structure.” They cannot form a “curved side surface” in the plane parallel to the top surface of the structure (x-y), which further supports that a POSITA would understand “curved side surface” to be a “vertical surface curved along a direction (e.g., the z-axis) perpendicular to the top surface of the structure.”

80. Gas-phase deposition techniques, capable of supplying both directional and isotropic fluxes of depositing molecules, offer control of the curvature of the deposited side surface. Such techniques include plasma-enhanced CVD and directional sputter deposition (PVD). Plummer 547-554, 590-600. The resulting structure, shown in Figure 8 of the patent, includes a landing pad that has a vertical surface curved along the z-axis. But, as I show below, that same Figure 8 shown from above in the x-y plane will not have any

curved horizontal surface, because there is no process described in the '838 patent for curving the surfaces of the landing pads in contact with the insulating layer in the x-y plane.



Nor could the process taught in the '838 patent result in a landing pad having surface that is curved in the x-y plane. This would have been understood by a POSITA.

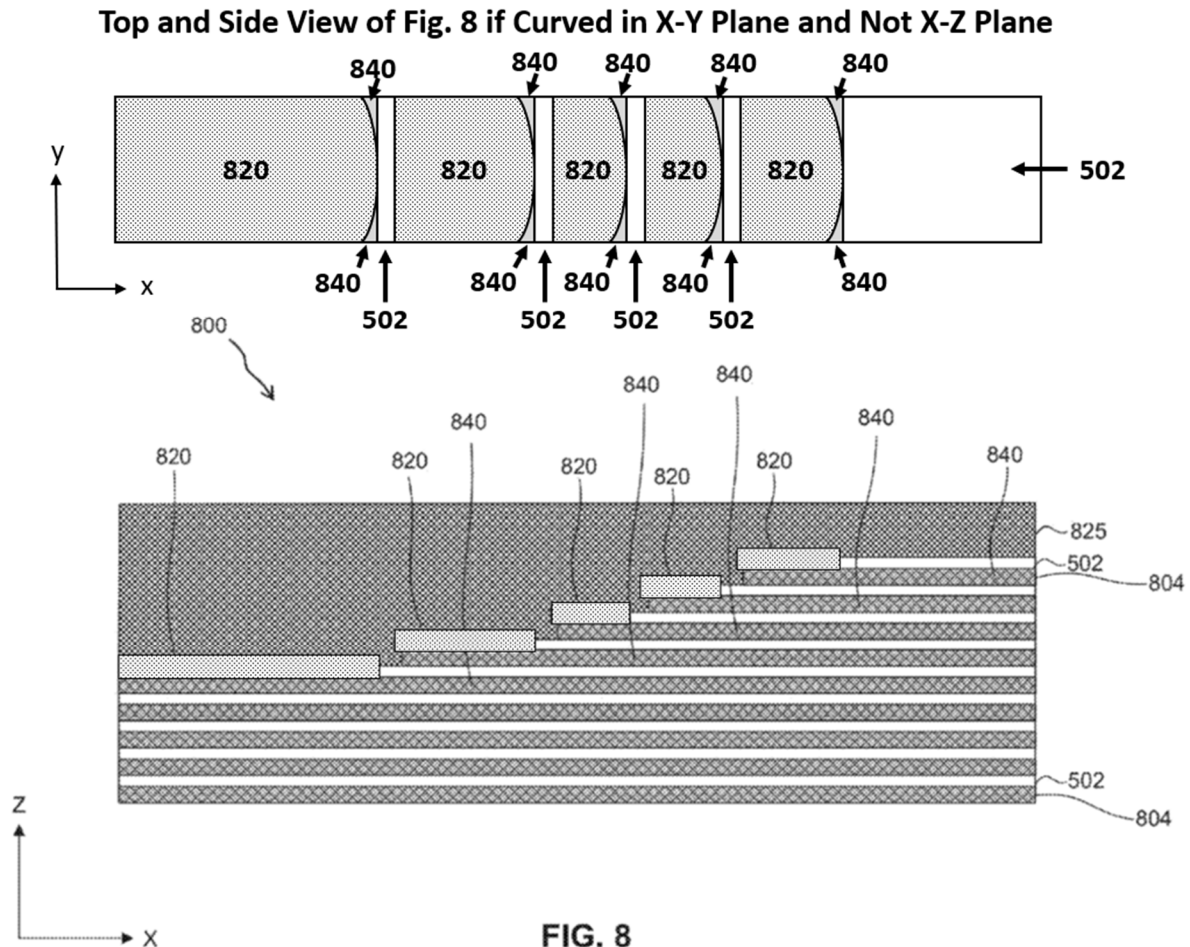
81. The landing pad is formed by replacing dielectric layer 620/720. '838 patent 8:46-9:12. And that dielectric layer is deposited to ensure it "is

substantially thinner at the side of staircase structure 600 than that at a top surface of staircase structure 600.” *Id.* 8:46-9:12. In other words, the dielectric layer 620/720 and then the resulting landing pad are formed to change the curvature along the z-axis, not in the x-y plane. There is no teaching in the '838 patent for depositing the dielectric so that it curves in the x-y plane.

82. I understand that the purpose of the invention also informs claim construction. Here, the '838 patent describes “a staircase structure for a memory device” that “provide[s] numerous benefits including, but not limiting to, yield and manufacturing cost improvements.” *Id.* 1:42-46. As I have explained in my patent overview, a POSITA would have understood one of those improvements as a “curved side surface” that reduces the risk of short-circuit by increasing the distance between adjacent conductive layers. But that benefit only occurs by forming a curve along the vertical direction.

83. Below I show what Figure 8 would look like if the landing pads in Figure 8 were curved in the x-y direction and not the z-direction, recognizing that the '838 patent does not provide any method for forming such landing pads. As shown, the distance between conductive layers will be unchanged versus conventional approaches if curved along the x-y axis, because the vertical separation of the conductive layers will not be increased. Thus, a purpose of a “curved side surface” in the '838 patent, specifically to reduce the risk of short-

circuit by increasing the distance between adjacent conductive layers, is only achieved with the landing pad having a vertical surface curved along the z-direction.



84. I have reviewed the prosecution history and saw nothing that would change my opinions. During prosecution of the application that would become the '838 patent, claim 13 included a "curved side surface" and the Examiner "agreed that cited prior art (Lee et al., US 2016/0218107) would not read on language regarding 'curved' structural feature." Ex.1002 109, 177, 195.

Meanwhile, there was no discussion in either the prosecution of the '838 patent nor prosecution in related patents about the “curved side surface.”

VIII. Ground 1: Claims 1, 4-7, 12-17, and 19-20 Are Not Obvious In View of Kim

A. Overview of Kim (Ex. 1005)

85. Kim describes 3D semiconductor memory devices with a “stepwise” “stacking structure” in the contact region. Kim (Ex. 1006) 1:13-35, 1:40-53, Fig. 4B. “Ones of the plurality of gate electrodes, may include a respective pad unit that comprises a step of the stepwise structure. At least one of the pad units may include a base pad and a protrusion pad on the base pad.” *Id.* 1:47-50. The pad units are where contact plugs are formed for electrical connection to word lines in upper layers. *Id.* 9:64-10:4, Fig. 4B. Kim describes the process by which its complete stepwise stacking structure is formed, including the pad units. Steps described include the formation of the memory cells, but I omit those details here to focus on the contact region.

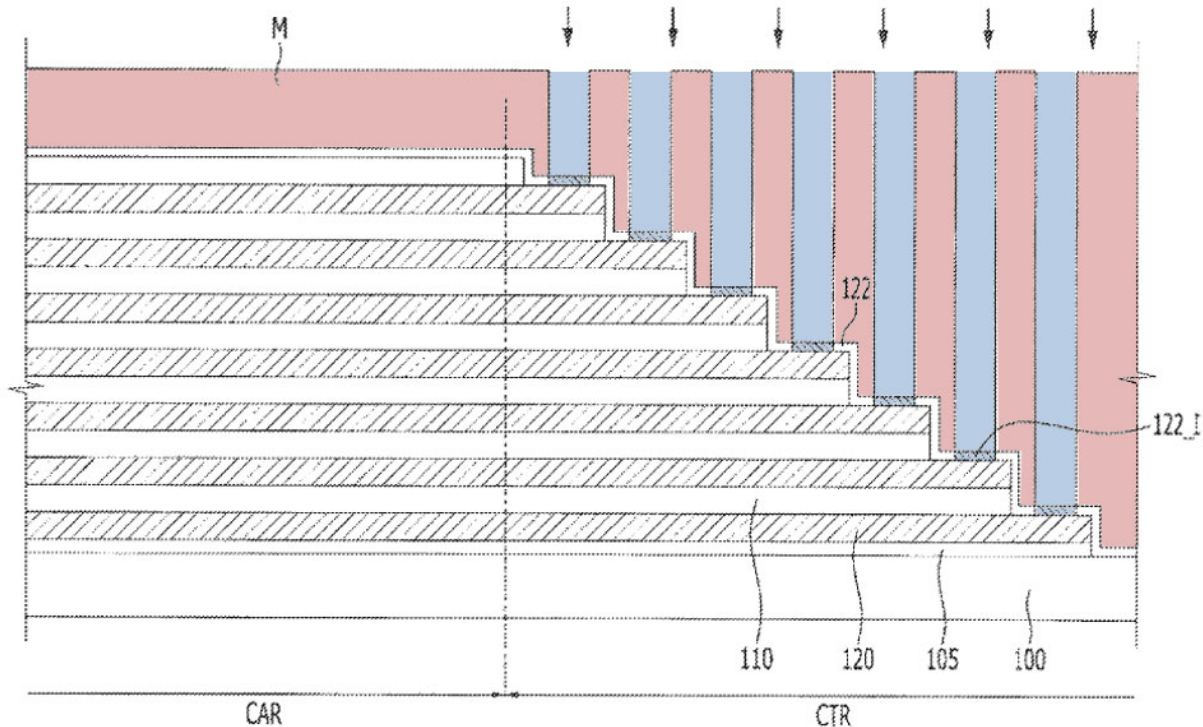
86. A set of alternating layers of insulating layers 110 and sacrificial layers 120 are formed on a lower insulating layer 105. *Id.* 12:20-25, Fig. 10. The stepwise structure is formed by using a mask pattern to etch some material, then the mask pattern itself is etched so that more of the alternating layer structure is exposed and etched further. This process is repeated until the stepwise structure is formed. *Id.* 12:43-56, Fig. 11. An auxiliary insulating layer 122 is then

formed over the stepwise structure conformally covering the top and side surfaces of the stepwise structure. Kim 9:12-20, 12:57-60, Fig. 11.

87. A photosensitive resin pattern M is then formed on the structure over the auxiliary insulating layer 122. *Id.* 12:61-67, Fig. 12. The photosensitive resin pattern M is formed so that predetermined regions of auxiliary insulating layer 122 are exposed. *Id.* 12:61-67, Fig. 12. The predetermined regions are referred to as region 122_I, and are for forming the protrusion pad. *Id.* 12:61-67, Fig. 12. To better show this, in the figure below, I have colored in light blue the openings made in photosensitive resin pattern M, extending all the way down to and including the corresponding exposed regions 122_I. The portion in pink is the solid photosensitive resin pattern M that remains in place during this step. Once the openings are made, predetermined ions are injected from above, as indicated by the arrows. The ions can travel freely only in the openings made in the photosensitive resin pattern M and are thus able to reach the exposed regions 122_I of the auxiliary insulating layer only at these locations. Through this process, the regions 122_I become “doped region[s]” and therefore have a different etching ratio as compared to the rest of the auxiliary insulating layer 122 that was not exposed to the ions through the mask pattern but remained covered by the solid portion of the mask pattern (pink below) and thus it was not injected

with ions. Kim 12:61-13:11, Fig. 12. A POSITA would understand this from these disclosures in Kim.

FIG. 12



88. Indeed, Dr. Lee agreed in his '666 patent deposition that the x-y surface is determined by the shape of the mask and that the shape of the mask is a horizontal shape, not a vertical one.

Q. So the shape of the exposed – of the x-y surface in the exposed region of 122 is determined by the shape of the openings in the photosensitive pattern M?

A. Yeah, let me explain how the photoresist work. You put on the photoresist and you expose the photoresist with UV light. And then you develop the photoresist such that the exposed photoresist region

will dissolve and so you left behind an opening. And that opening, of course, is determined by your mask that is used to define the photoresist pattern. **And so, yeah, the exposed region is determined by the pattern of the mas[k] defining the photoresist pattern.** Does that make sense? Ex. 2031 150:20-151:15 (emphasis added).

Q. But the top of the mask is some shape in the horizontal direction, correct?

A. **The top of the mask is a shape defined by the process engineer and is defined by the shape on the mask.** It could be a rectangle. It could be a square. It could be an oval shape. But all we see here is a cross-section in the -- in a particular -- all we see here is a cross-section in the z-x plane. We don't know what's the other perspective in the -- into the board. In fact, it could be a circle. It could be an oval shape.

Q. But the shape that it is, is a shape along the horizontal direction, correct? **It's not a vertical shape?**

A. **Yeah.** From the top view you see the opening defined by the mask. And, yeah, you could say that this is a horizontal top view of the opening. But even the opening, like I said, is a three-dimensional structure. The whole is not a two-dimensional structure. It's a three-dimensional structure. All we see in Figure 12, it's just a cross-section. Ex. 2031 153:20-155:15 (emphasis added).

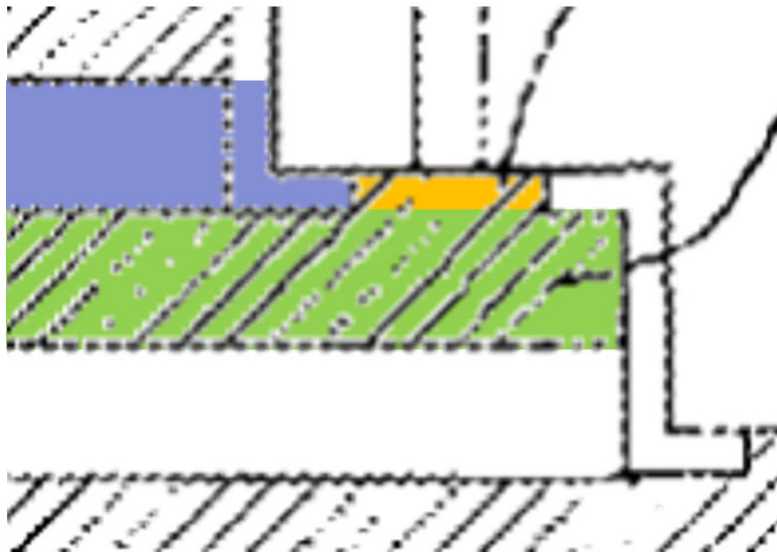
89. After the ion injection, remaining material of the mask pattern (pink above) is removed and an insulating layer 125 is placed over the stepwise structure. Kim 13:12-20, Fig. 13. Thereafter, the sacrificial layers 120 can be removed. As a POSITA would understand from Kim, because the regions 122_I have the different etching ratio compared to the rest of auxiliary insulating layer 122, the regions 122_I can be removed either together with the sacrificial layers 120 or separately, such that there is an opening in the auxiliary insulating layer 122 only at those implanted locations termed openings 122_O in Kim. Kim 13:51-67, Fig. 16. Furthermore, a POSITA would understand that the entirety of each exposed region 122_I would be removed during that etching process because the ion injection process alters the etching ratio everywhere within each exposed region 122_I. This is what Kim depicts and Kim never says otherwise and a POSITA would not expect otherwise. *E.g., id.* 13:55-60, Fig. 4B, Figs. 16-18. The rest of the auxiliary insulating layer 122 (i.e., the portion not exposed through the mask pattern) is not etched in this process and remains in place.

90. The area where the sacrificial layers 120 were and the openings 122_O, which Kim refers to as “gaps 260,” are then filled with conductive material to form gate electrodes 300. *Id.* 13:55-67, 14:6-7. Kim refers to the area defined by the openings 122_O and subsequently filled by conductive material as the “protrusion pad PAD_P.”

91. The longer portion below that, which is not covered by insulating layer 120, is referred to as the “base pad PAD_B.” Kim 9:21-28, 14:6-17, Fig. 6, Fig. 17. In this way, Kim’s pad unit PAD combines base pad PAD_B with protrusion pad PAD_P, thus increasing the thickness of the PAD in the vertical z-direction, which helps prevent damage to the PAD during the manufacturing process. Kim 9:39-45, 11:48-52. As Kim explains, this may occur when forming the word line contact plugs 415, which can result in the contact punching through the pad region causing a short-circuit between different steps. *Id.* 9:39-45, 11:48-52, Fig. 18. Furthermore, by using the mask pattern to form the PAD_P in precise locations, Kim can ensure that “the protrusion pad PAD_P [is] inside from the edge of a surface of the base pad PAD_B to prevent the short-circuit between the pad units PAD positioned at different rows.” *Id.* 9:46-49, Fig. 4B, Fig. 18; *see also id.* 8:1-22, 8:35-59, 10:19-48, Fig. 5, Fig. 6. Kim further notes that short-circuits are “effectively prevented” because the auxiliary insulating layer 122 remains in place. *Id.* 9:50-55, Fig. 4B, Fig. 18.

92. The below figure is a zoomed in and annotated version of Kim’s Figure 4B. The colored annotations match those used in the Petition. Pet. 43-45. While Kim’s Figure 4B does not provide axes, it is clear from the axes provided on Kim’s Figures 4A, 5, 6, and 7, in the stepwise region, which Kim also calls the contact region or CTR, that the below figure zooms in on, a POSITA would

readily understand it to be the x-z plane. Kim 5:22-39, Fig. 4A, Figs. 5-7. This matches the plane of Figure 8 of the '838 patent. As can be seen, in the x-z plane, there is no curvature depicted—it is a straight vertical surface. This is precisely what a POSITA would expect in light of the process described in Kim, which I have detailed above. The vertical (z-direction), straight contact between the annotated blue and orange occurs because the entirety of the regions 122_I are removed and the openings 122_O are filled with conductive material.



93. Kim notes that what is illustrated is “the protrusion pad PAD_P has a rectangular parallele [sic] shape.” Kim 8:29-31. Kim explains that “[t]he protrusion pad PAD_P may have an island shape with respect to the one surface of the base pad PAD_B.” Kim 8:23-26. This is shown in Kim’s Figure 6, where “the protrusion pad PAD_P ... [is] positioned inside from four edges E1, E2, E3, and E4 of the surface of the base pad PAD_B.” *Id.* 10:19-48, Fig. 6. Regardless

of whether PAD_P is an island or not, Kim's Figure 4B would look the same because the cut is taken where contact plug 415 contacts PAD_P. Kim 9:64-10:4, Fig. 4B, Figs. 5-6. A POSITA would understand from Kim's disclosure that the difference in forming PAD_P as in Figure 5 versus forming PAD_P as in Figure 6 would be a change to the shape of the openings in the photosensitive resin pattern M. I illustrate this using a cropped version of Kim's Figure 4A, below. Employing the same colors as in Paragraph 87 above where I illustrated this in the x-z plane using Kim's Figure 4B, the solid part of photosensitive resin pattern M is shown in pink while the openings are shown in light blue. Figure 4A and the colored figures below are in the x-y plane, looking from above, down onto the stepwise structure. On the left, the openings extend the full width of the steps in the y-direction and would result in PAD_Ps that extend the full width of the steps in the y-direction, as in Kim's Figure 5. On the right, the openings are shorter in the y-direction and would result in PAD_Ps that are islands on stair steps (PAD_B) as in Kim's Figure 6. I have included Figures 5 and 6 below the annotated figures, but note that Figures 5 and 6 each show two sets of steps, whereas I have only depicted one set of steps in the colored drawings as indicated by the dotted lines annotated on Figures 5 and 6.

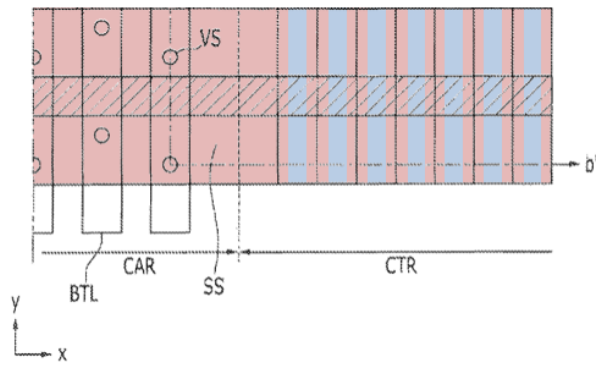


FIG. 5

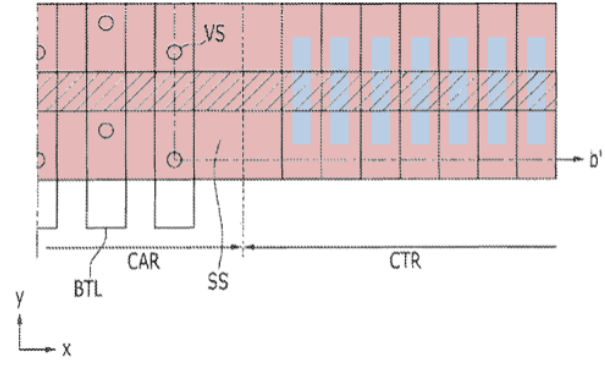
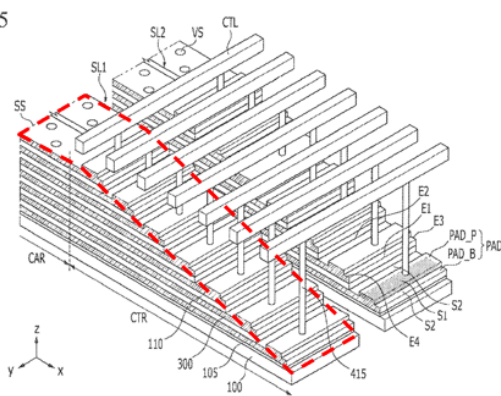
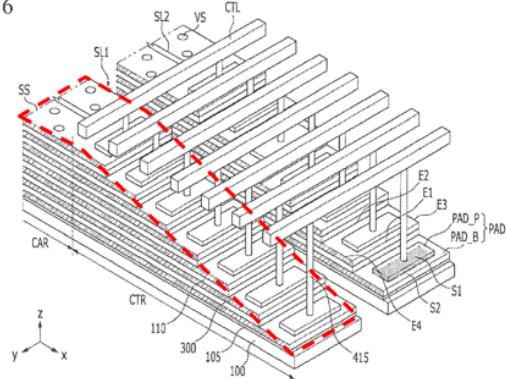
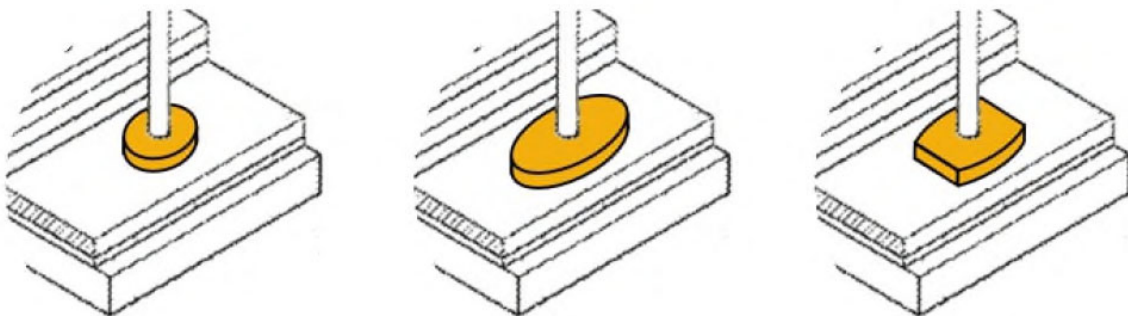


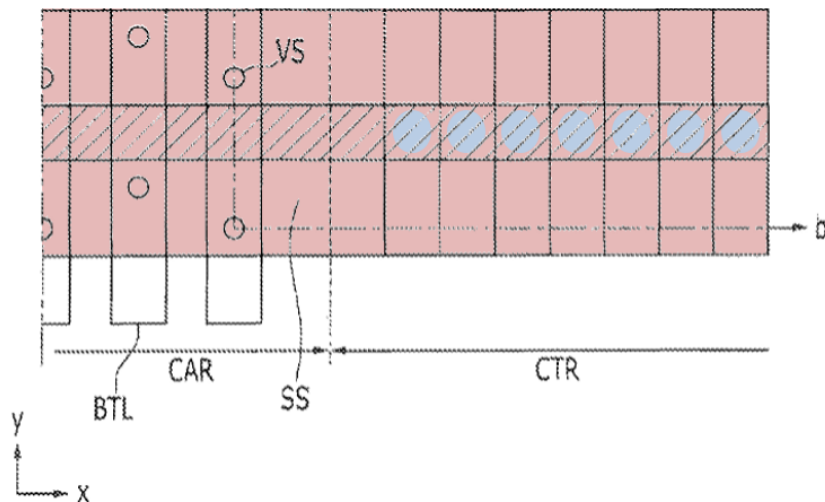
FIG. 6



94. Kim also explains that, “in some embodiments,” PAD_P “may have a shape including a curved surface based on a virtual rectangular parallelepiped shape, a cylindrical shape, or any shape.” Kim 8:32-34. The Petition and Dr. Lee provide the below figures as depicting such shaped PAD_Ps. Pet. 47-49; Ex. 1003 ¶¶263-266. But neither explains whether or why a POSITA would want to use any of these shaped PAD_Ps.

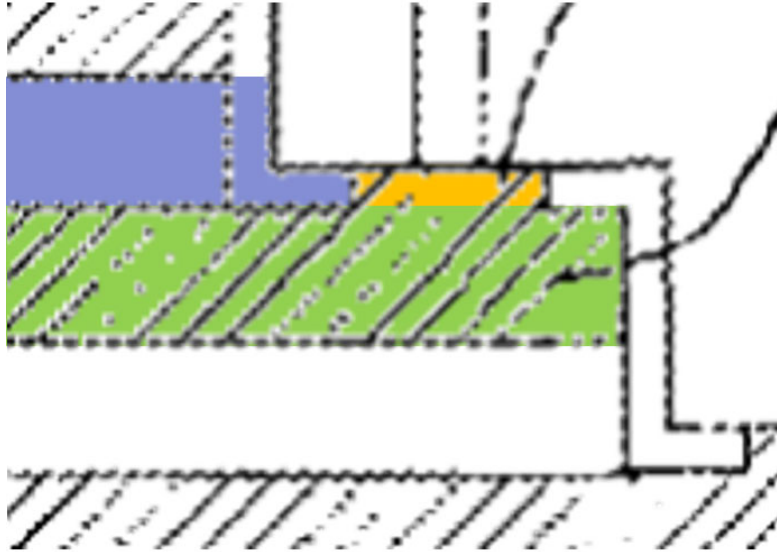


95. Assuming the above shapes would be used by a POSITA, the PAD_P would be formed by changing the photosensitive resin pattern M such that openings were not rectangular, but instead had the shapes above in top view. See Ex. 1003 ¶270. As I did above in Paragraph 93, I depict this again with the solid part of photosensitive resin pattern M is shown in pink while the openings are shown in light blue, to form the smaller circular pad on the left in the Petition's figures.



96. Regardless of the shape of the openings formed in the photosensitive resin pattern M, the resulting structure will look the same in the x-z plane of Kim's Figure 4B, which I again depict below (same as in the discussion of Paragraph 92). The only difference would be the width of the orange portion in the x-direction (left to right in the figure below). There will always be vertical (z-direction), straight contact between the annotated blue and orange because the

entirety of the regions 122_I are removed and the openings 122_O filled with conductive material.

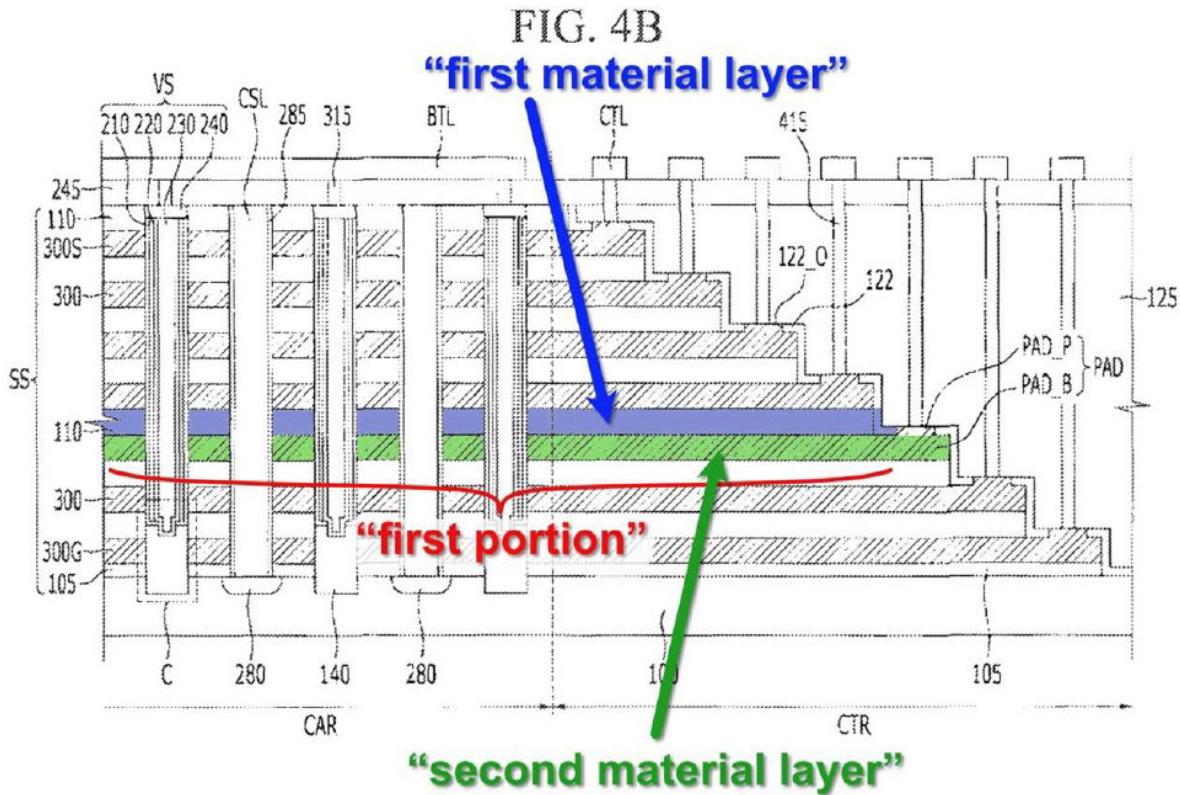


97. While Kim refers to PAD_P “including a curved surface,” Kim 8:29-34, a POSITA would understand that there is no curvature in the x-z plane, because in cross-sectional view the pad will always look as it does above, i.e., with straight vertical sidewalls. In one explanation, the Petition and Dr. Lee appear to treat the curved areas of the cylindrical PAD_Ps in top view, depicted above in connection with my Paragraph 94, as the “curved side surface” in the ’838 patent. If that is what Kim refers to, then there will not be a curvature in the x-z plane to the contact between the annotated blue and orange in the above figure. This does not satisfy the claimed “curved side surface.”

B. Petitioner's Expert Misunderstands or Misrepresents Kim and Kim's Mapping to Claims 1 and 12 and Does Not Show Obviousness

98. I have reviewed Petitioner's expert's mapping of Kim to the limitations of claims 1 and 12 of the '838 patent. *See* Ex. 1003 ¶¶144-202. In his analysis, Petitioner's expert relies only on Figures 4B and 6 of Kim. *See id.* The Petition then relies on the same annotated Figures 4B and 6. *See* Pet. 27-38.

99. Petitioner's expert states that "Kim's insulating layer 110 and the adjacent portion of auxiliary insulation layer 122 together constitute the claimed 'first material layer.'" Ex. 1003 ¶154 (emphasis removed); *see also id.* ¶160. He also states that "the gate electrode 300" is the "second material layer." *Id.* ¶167. He uses the figure below to illustrate his opinions:



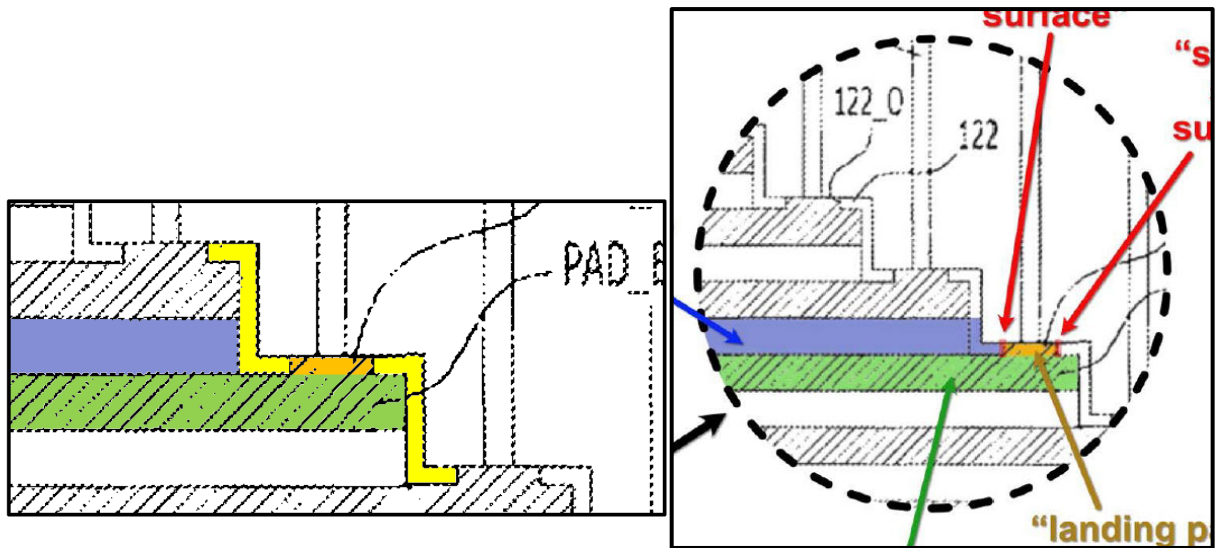
100. Petitioner’s expert labels a “first portion” that extends along the second material layer, annotated in green, to where his first material layer, annotated in blue, (mistakenly) ends at the PAD_P.² As noted above, Petitioner’s

² Petitioner’s expert has identified the “first portion” as extending through both the CAR and CTR regions of Kim’s stacking structure in Kim Figure 4B.

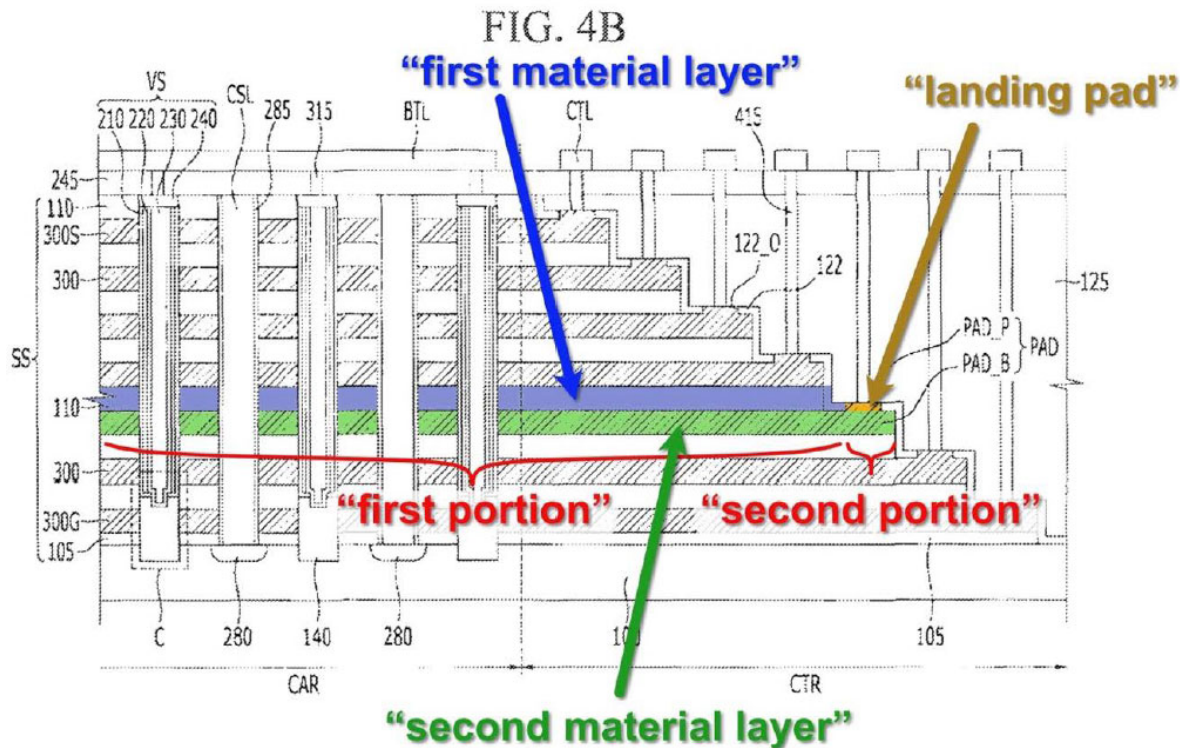
However, Kim explains that these are not contiguous in one direction: “FIG. 4B is a cross-sectional view taken along line b-b’ of FIG. 4A.” Kim at 5:27-28. The line b-b’ in Figure 4A is not straight, but instead extends from b in the y-direction, and then makes a 90 degree turn to extend in the x-direction to b’. See

expert asserts that, for purposes of mapping Kim to the claims of the '838 patent, that “Kim’s insulating layer 110 **and** the adjacent portion of auxiliary insulation layer 122 **together** constitute the claimed ‘first material layer.’” Ex. 1003 ¶154 (emphasis modified). To illustrate his opinion, the figure below on the left annotates Kim’s layer 110 in blue, Kim’s gate electrode 300 in green, Kim’s PAD_P in orange, and Kim’s auxiliary layer 122 in yellow, following the descriptions of these structures in Kim. *See* Kim 5:53-55, 6:15-19, 7:50-8:10, 9:12-20, Fig. 4B. The figure below on the right is a cropped version of the figure from paragraph 182 of Petitioner’s expert’s declaration. *See* Ex. 1003 ¶182. As can be seen, Petitioner’s expert colors in blue just part of the auxiliary layer seen in yellow on the left. Notably, he does not include any other part of the yellow auxiliary layer, but does not explain why. In my opinion, this is incorrect and is an arbitrary label flawed by hindsight, as I explain further below after discussing Petitioner’s expert’s opinions first.

Kim at Fig. 4A. Thus, the CAR and CTR regions depicted in Kim Figure 4B extend in the y-direction and x-direction respectively. In this way, Petitioner’s expert’s labeling of figures is confusing. Regardless, I disagree with his analysis as explained herein, but note this because it also indicates that Petitioner’s expert may not fully understand or appreciate what is described in Kim.

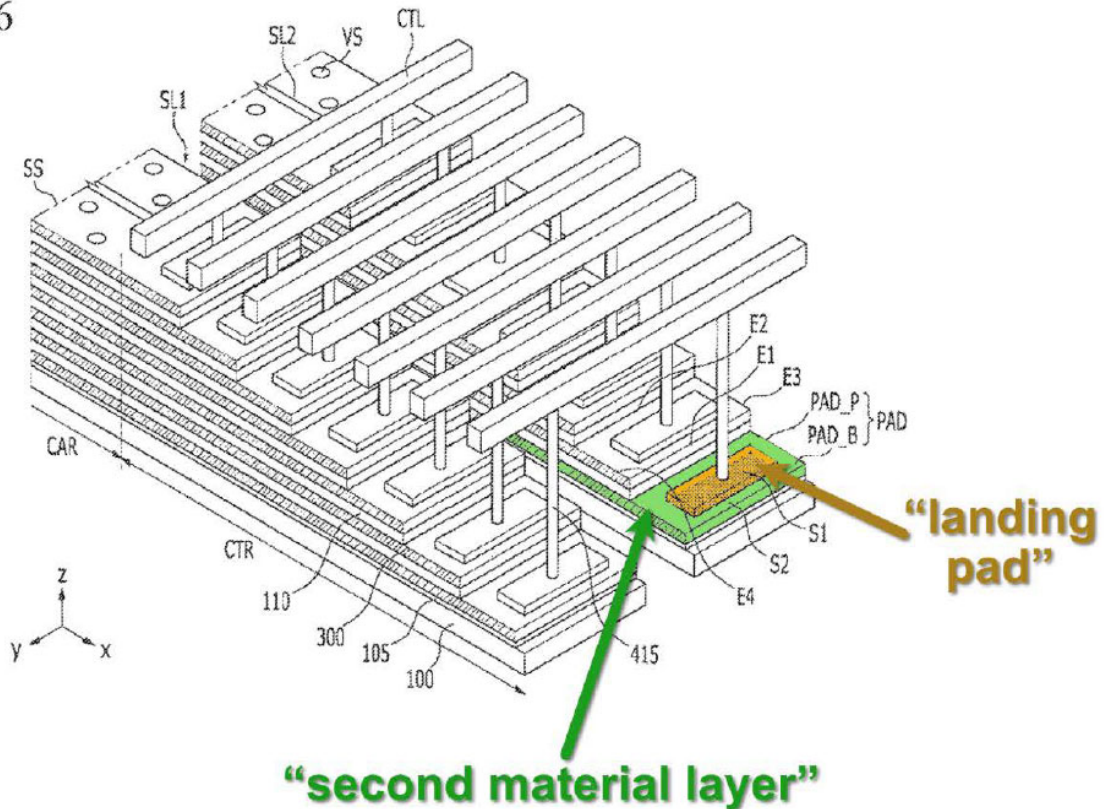


101. Continuing with Petitioner's expert's opinions, he provides the below figure where he maps Kim's PAD_P to the claimed landing pad. Ex. 1003 ¶175. He provides a "second portion" label, but does not explain why it is the claimed "second portion" or how it relates to the rest of Kim's structure. Again, it is just an arbitrary label driven by hindsight.



102. Furthermore, in describing the PAD_P “landing pad,” Petitioner’s expert makes clear that he relies on a PAD_P where “the shape of this protrusion pad” “has an ‘island shape.’” Ex. 1003 ¶180. He further explains that “Kim teaches a protrusion pad PAD_P that is smaller than the conductive layer on which it sits and thus has sides that are offset from the sides of that conductive layer.” Ex. 1003 ¶192. Because Kim’s Figure 4B only shows the CTR region in the x-z plane, *see* Kim 2:39-42, 5:22-28, 5:58-67, 6:15-19, Fig. 4A, Fig. 4B, Petitioner’s expert points to Kim Figure 6 as showing the PAD_P used in his opinions, *see* Ex. 1003 ¶¶193-194. His annotated Figure 6 is shown below.

FIG. 6

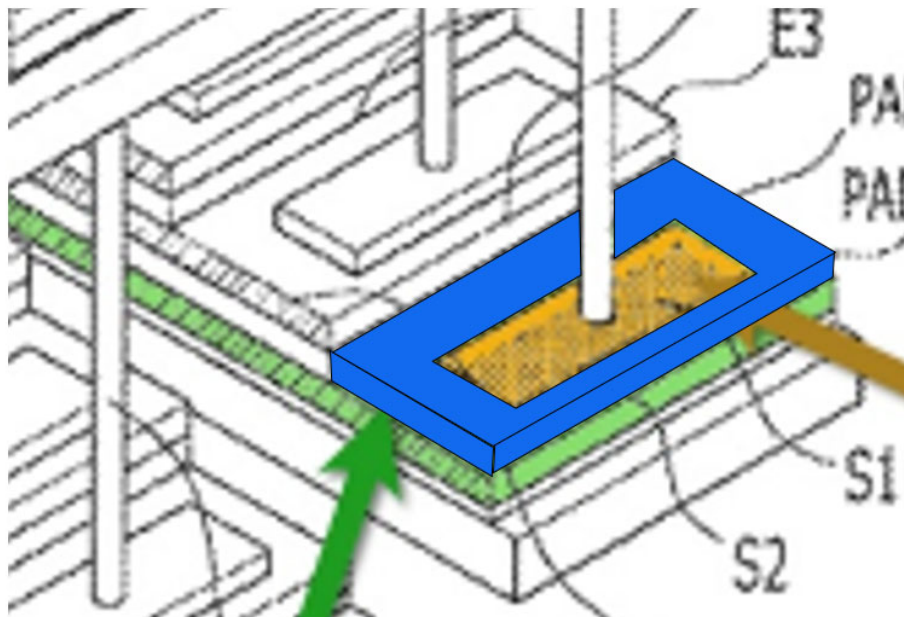


With the Figure 6 three-dimensional figure, one can see the “island shape” that Petitioner’s expert described as offset from the sides of the conductive structure beneath it (the green second material layer that he has annotated).

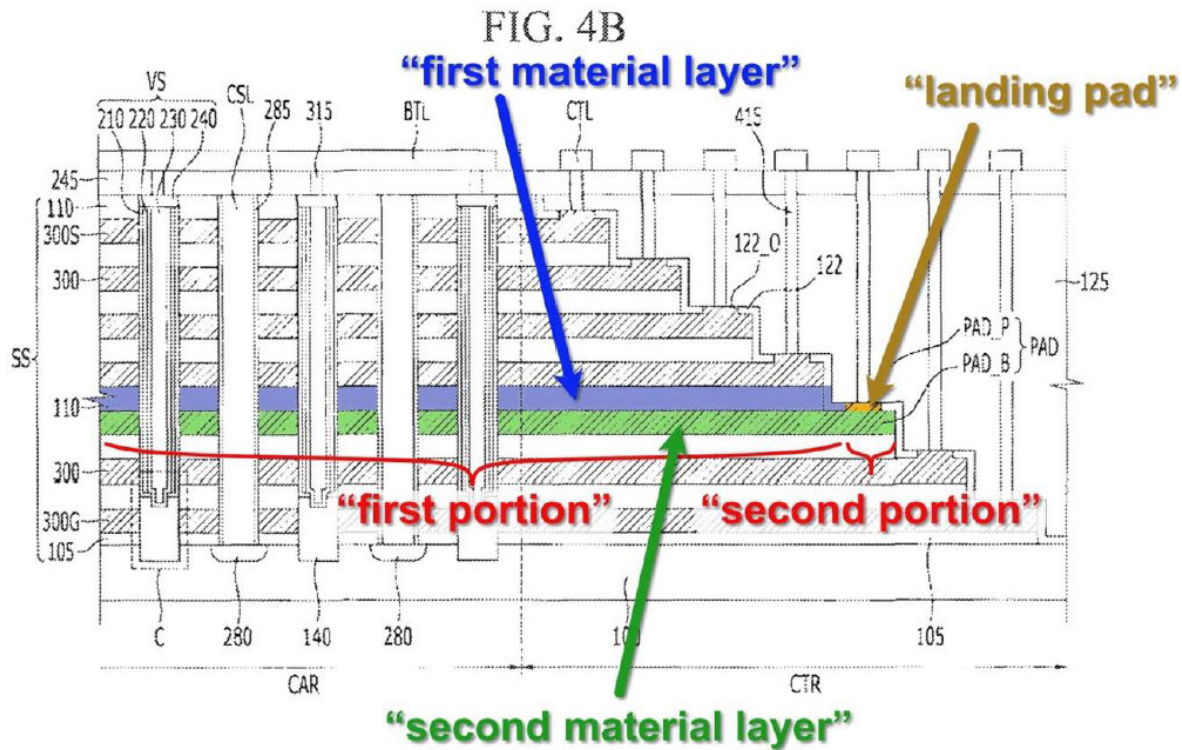
103. Petitioner’s expert continues to rely on the island shaped PAD_P in his opinions about dependent claims, albeit with different shapes. *See* Ex. 1003 ¶263. Assuming, without necessarily agreeing, that the shapes shown in paragraph 263 of Petitioner’s expert’s declaration are feasible, those shapes and the island PAD_P shown in the annotated Figure 6 above are formed by shaping the openings in the photosensitive resin pattern M that I described above in Paragraph 87. As I explained there, the openings in the photosensitive resin

pattern M allow for the auxiliary insulating layer 122 to be injected with ions so that the part of the auxiliary insulating layer 122 that was exposed in the openings of the photosensitive resin pattern M are the locations of the PAD_P when formed. *See supra* Paragraphs 87-90. Petitioner's expert acknowledges this when he states that "auxiliary layer 122 is applied ***before*** Kim's contact pads are formed. In particular, after 'the plurality of insulating layers 110' are 'patterned in the stepwise structure in the contact region CTR,' then the auxiliary insulating layer 122: is 'formed thereon.'" Ex. 1003 ¶157. A POSITA would understand from Kim's description that, aside from the opening 122_O, the rest of auxiliary insulating layer 122 remains in Kim's final structure, as it is described as in place when "buried insulating layer 125" is placed over the top of the entire structure and "covering the auxiliary insulating layer 122." *See* Kim 9:12-63, Fig. 4B. For this same reason, a POSITA would understand that, while Kim's Figure 6 above does not show auxiliary insulating layer 122, it would be there. Kim explicitly states, in describing Figure 6, that "[the] auxiliary insulating layer 122 may contact the second region S2 of the surface of the base pad PAD_B and the side of the base pad PAD_B in the contact region CTR." *Id.* 10:49-51. As shown in Figure 6 above, "S2" is the region on top of the identified second material layer, annotated in green, that surrounds the island PAD_P.

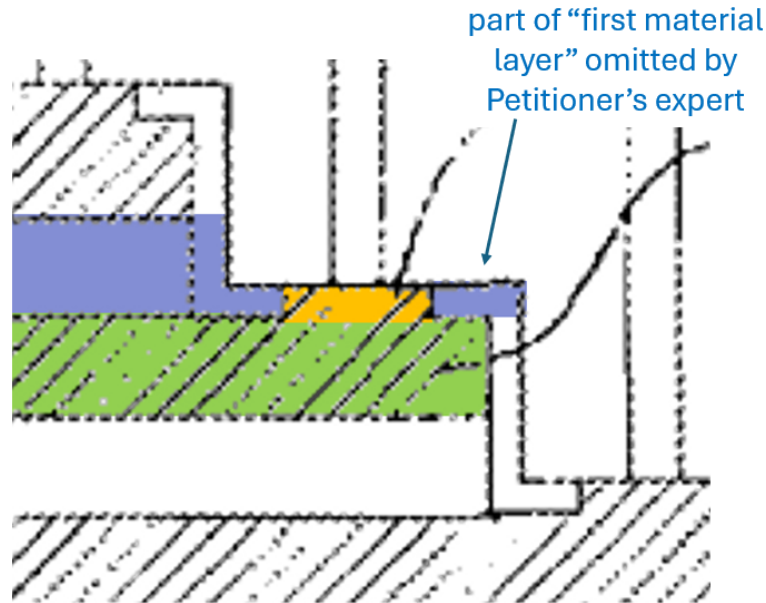
104. Thus, from Kim's explicit teachings, a POSITA would understand that auxiliary insulating layer 122 would be present and surround the PAD_P in Kim's Figure 6. This is shown in the figure below, which takes Petitioner's expert's annotated Figure 6, zooms in to the step, and annotates the auxiliary insulating layer 122 that surrounds the PAD_P. The illustration below just shows the auxiliary insulating layer 122 (blue) that surrounds the PAD_P, but a POSITA would understand that the auxiliary insulating layer 122 follows the path of the stairs and covers all the stairs, as shown in the figure on the left in Paragraph 100 above. Petitioner's expert states that "because layers 110 and 122 are formed from the same material such that they 'form one structure' as Kim itself states." Ex. 1003 ¶160. Assuming that is what is understood by a POSITA, then a POSITA would understand that one structure is formed all the way around the PAD_P.



105. As can be seen in Petitioner's expert's annotated figures, such as the one reproduced below, he does not account for the fact that the auxiliary insulating layer 122 surrounds the PAD_P. Instead, he simply ignores the auxiliary layer 122 on the other side of the PAD_P, assumedly because of the hindsight need to label the "first portion" and "second portion" of the second material layer as he does below.

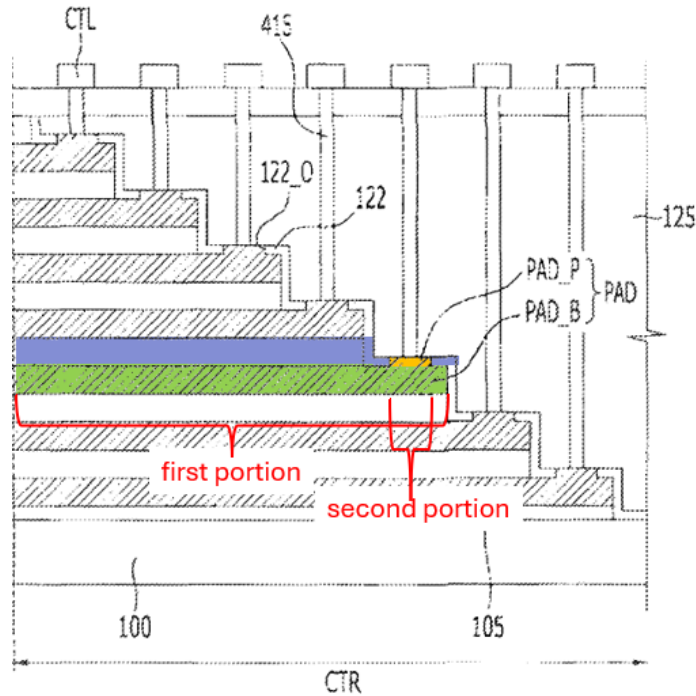


106. The figure below is a zoomed in, cropped version of Kim’s Figure 4B, annotated similarly to the above figure from Petitioner’s expert, except the auxiliary layer 122 on the right side of the PAD_P, which is connected and contiguous with the portion on the left side for the reasons already explained, is also annotated in blue. Petitioner’s expert incorrectly omits this part of auxiliary insulating layer 122 from his analysis and annotated figures without any explanation.



107. Properly identifying the full extent of the first material layer, rather than just arbitrarily picking a hindsight-driven partial extent, the first material layer, annotated in blue, extends across the entire second material layer, annotated in green, which is labeled “first portion” in the figure below. As can be seen, this overlaps with what Petitioner’s expert identifies as the “second portion” in his figure that is between Paragraphs 105 and 106 above. But in three dimensions, the “second portion” below is only under the PAD_P (assuming that can satisfy the “second portion” limitation). Because the first material layer completely surrounds the island shaped landing pad, the “second portion of the second material layer” is also an island shaped portion underneath the landing pad. With the first material layer completely surrounding the landing pad, the interface between the first material layer and the landing pad exists on all sides of

the landing pad. That interface also defines the boundary between the “first portion” and the “second portion” of the second material layer below. Thus when properly understood, Kim’s “first portion” and the “second portion” of the second material layer overlap (as shown below).



108. By ignoring Kim’s express teachings, Petitioner’s expert’s labels are entirely arbitrary and hindsight-driven. As claims 1 and 12 require, there is a correspondence between the “first material layer” and the “first portion of the second material layer.” Likewise, there is a correspondence between the “landing pad” and the “second portion of the second material layer.” Thus, in light of Kim’s teachings, the “second portion” is an island shaped portion in the second material layer just below the PAD_P landing pad. But an island shaped

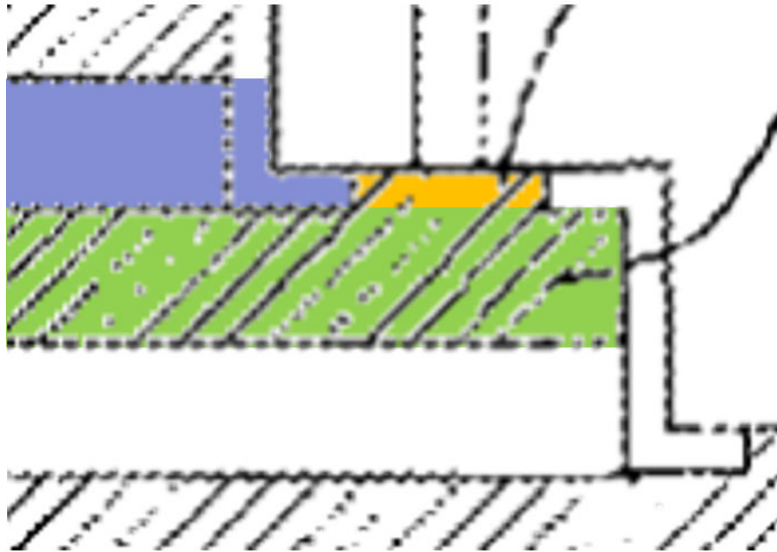
“second portion” does not render claims 1 and 12 obvious because it does not show “the second side surface [of the landing pad] is laterally displaced from a side surface of the second portion of the second material layer” as required. Instead, they are coterminous when viewed from above and there is no lateral displacement.

109. Thus, in my opinion, claims 1 and 12 are not obvious in view of Kim as argued by Petitioner’s expert. As the remainder of Ground 1 discusses dependent claims, obviousness of those claims also has not been shown.

C. A POSITA Would Not Have Found Claims 13-15 Obvious Based on Kim

110. In my opinion, Kim does not teach nor render obvious claim 13. Specifically, a POSITA would not arrive at “the first side surface comprises a curved side surface,” as recited in claim 13, based on Kim. Since claims 14-15 depend on claim 13, they are not obvious in view of Kim either.

111. As explained above, Kim does not show a “curved side surface” in its figures. Instead, there will always be vertical straight contact between the annotated blue and orange regions because the entirety of the regions 122_I are removed and the openings 122_O are filled with conductive material, as depicted again below. Dr. Lee depicts this straight contact the same as I do, just with different annotations. Ex. 1003 ¶275.



112. While Dr. Lee asserted in his declaration that “Kim teaches that the *‘first side surface’* of its *‘landing pad’* that is in *‘contact’* with its *‘first material layer’* is (or at the very least obviously can be) *‘curved’*” (Ex. 1003 ¶222), at deposition regarding the ’666 patent, he agreed it is not shown by Kim. When discussing limitations 17.C.1 (“a plurality of layer stacks, each layer stack comprising an insulating layer disposed over a first portion of a conductive layer”) and 17.C.2 (“wherein a second portion of the conductive layer comprises a curved side surface in contact with a side surface of the insulating layer”) of the ’666 patent, Dr. Lee stated:

Q. Where does it mean that the limitation is taught by Kim?

A. I’m sorry. I’m trying to search word -- I think that what I meant is that Kim expressly or inherently disclose that limitation 17.C.1. And because each layer stack comprises an insulating layer disposed over the first portion of the conductive layer. So it is clearly shown

in Figure 4B and clearly discuss in the specifications of Kim. And, at worse, would make it obvious. **But 17.C.2, Kim does not expressly or inherently disclose the curved side surface.** But a person of ordinary skill in the art reading Kim in view of his knowledge would render this limitation obvious. Ex. 2031 130:8-131:7.

Q. Kim alone does not expressly or inherently disclose limitation 17.C.2, correct?

A. I think I answered that, that **Kim alone does not expressly or inherently disclose every element of that limitation 17.C.2.**

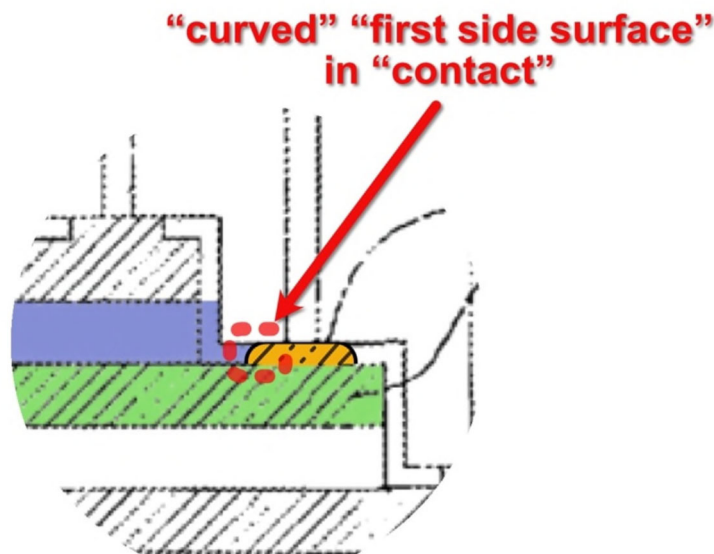
Q. Okay.

A. –exactly as claimed. *Id.* 132:17-133:3.

I note that while the limitations differ slightly between claim limitation 17.C.2 of the '666 patent and claim 13 of the '838 patent, Dr. Lee made clear his opinion that “Kim does not expressly or inherently disclose the curved side surface.”

113. Dr. Lee points to the discussion of the shape of Kim's PAD_P, which I thoroughly discussed above, as something a POSITA would recognize as including “configurations where the sides of the protrusion pads are curved, particularly to optimize electrical connectivity and mitigate stress at material interfaces.” Ex. 1003 ¶223. He also asserts that “[s]uch curved configurations

are routine in the fabrication of three-dimensional memory devices, as further supported by references like Park, Yun, and Nam.” *Id.* ¶224. He then asserts that “a POSITA would have understood that this teaches a variety of different protrusion pad PAD_P shapes, many of which have the type of ‘curved’ side surface Claim 13 requires. This includes, for instance, pads with curved sides when viewed in cross-section or pads with curved sides when viewed above.” *Id.* ¶224. Finally, he asserts that “a POSITA would have understood that when Kim references a ‘curved surface based on a virtual rectangular parallel[] shape,’ PAD_P would obviously be shaped in the manner shown in the demonstrative below,” which he says would be formed “following Kim’s teachings.” *Id.* ¶225. I have reproduced Dr. Lee’s demonstrative below, showing a curvature in the x-z plane, which he also refers to as “when viewed in cross-section.”



114. Dr. Lee is wrong that the above shaped PAD_P could result from following Kim's process. For the reasons I have already explained, there will always be vertical (z-direction), straight contact between the annotated blue and orange regions in the x-z plane (or as Dr. Lee says, "when viewed in cross-section") because the entirety of the regions 122_I are removed leaving behind openings 122_O with straight vertical sidewalls. These openings 122_O are filled subsequently with conductive material retaining the straight vertical sidewall shape. Dr. Lee provides no explanation at all for how sidewall curvature in the z-direction could be formed following Kim's process. And for all the reasons I have already provided, it could not be formed as Dr. Lee depicts. Furthermore, this is not the "curved surface" that Kim refers to, as noted above in Paragraph 97.

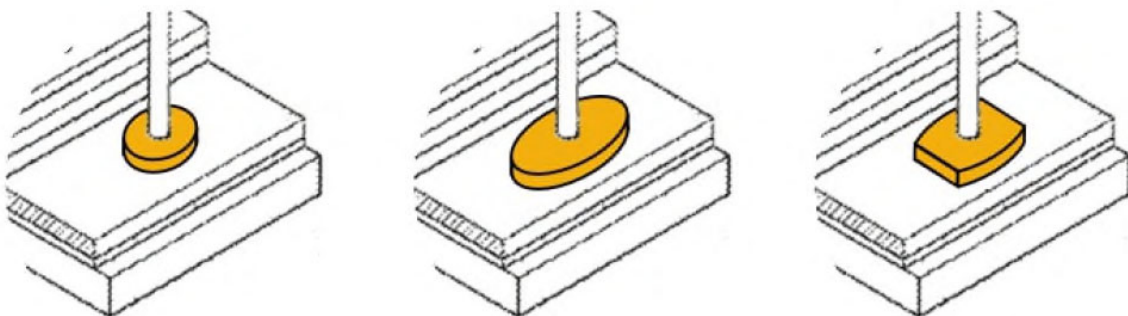
115. With nothing in Kim showing the made-up shape that Dr. Lee draws, Dr. Lee asserts that "a POSITA would have been motivated to employ a contact pad with curved side surfaces when implementing Kim." Ex. 1003 ¶241. Dr. Lee provides three purported reasons why. *Id.* ¶¶241-247. In brief, Dr. Lee asserts (1) Kim already contemplates a curved side surface (*id.* ¶242); (2) this type of pad was well known in the art (*id.* ¶¶243-244); and (3) doing so would reduce the risk of short-circuit in Kim (*id.* ¶¶245-247). I disagree with all three

assertions. I address (1) below in this section, (2) in Section VIII.C.1.b, and (3) in Section VIII.C.1.a.

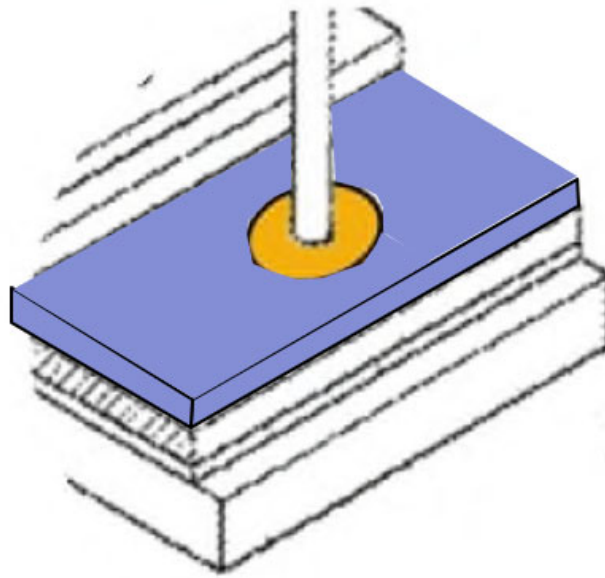
116. Dr. Lee asserts that “Kim itself already contemplates that its pad can have a “curved surface.” *Id.* ¶242; *see also id.* ¶226. But as I explained in Paragraphs 110-115, a POSITA would not understand Kim to be referring to a curved surface in the x-z plane as in the claimed structure. Nor does Kim describe a process for injecting ions resulting in a curved side surface in the vertical direction, as I explained above.

117. Dr. Lee states that “a POSITA would have understood that Kim’s ‘cylindrical[ly]’-shaped protrusion pads PAD_P also include the type of ‘curved’ surface that Claim 13 requires.” Ex. 1003 ¶261. I disagree.

118. As described above, Dr. Lee relies on the below figure as showing the “cylindrical” contact pads that he asserts could be used. Ex. 1003 ¶¶263-264. What Dr. Lee fails to depict is what happens to the auxiliary insulating layer 122 when a PAD_P like the ones below is formed.

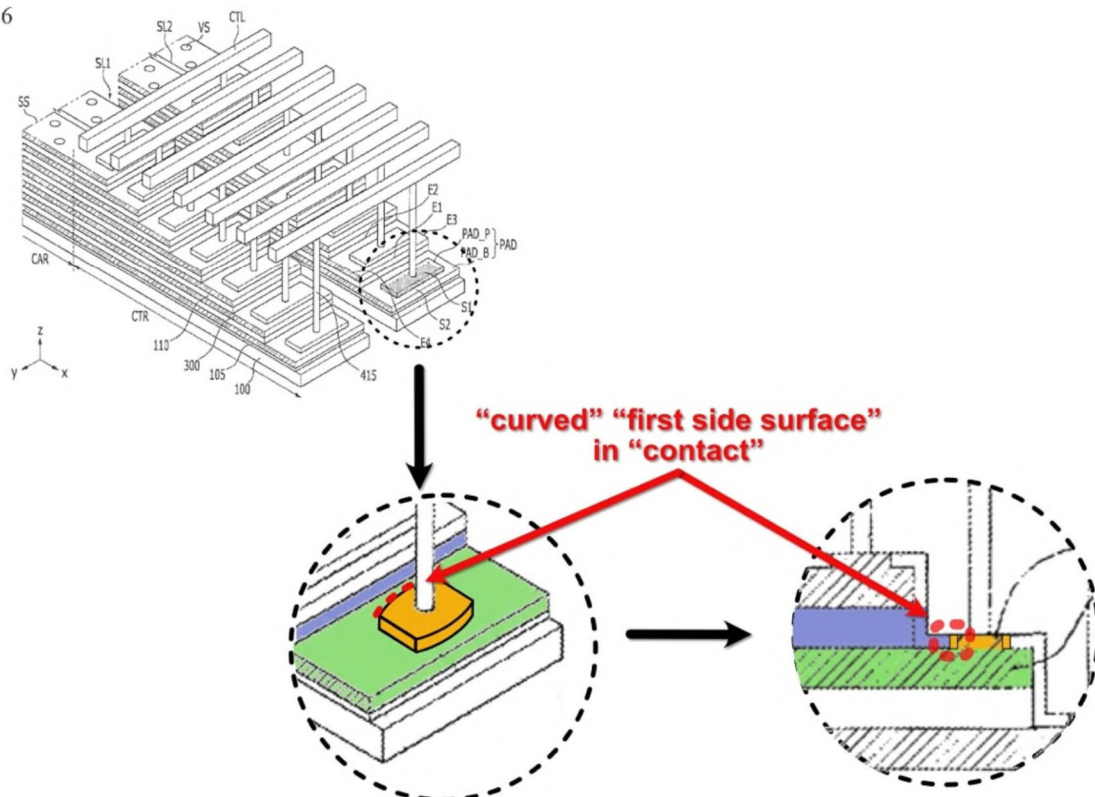


119. Using the PAD_P on the left in the above figures as an example, and focusing just in the area of one of Kim's PADs, the auxiliary insulating layer 122 would entirely surround the PAD_P as shown below. I have used the blue color to show this because the Petition relies on auxiliary insulating layer 122 as part of the claimed "first material layer" and depicts it in the same blue. Pet. 28-30. Kim explicitly describes this when discussing Figure 6, which the above figures are based on (Ex. 1003 ¶263). Kim explains that PAD_B has "the first region S1 contacting the protrusion pad PAD_P," meaning the portion of PAD_B underneath PAD_P, and has "the second region S2 other than the first region S1," meaning everywhere on the step surface not covered by PAD_P. Kim 10:30-32, Fig. 6. Kim then explains that "[t]he auxiliary insulating layer 122 may contact the second region S2 of the surface of the base pad PAD_B" *Id.* 10:49-51. A POSITA would understand this description to look as below. The same is generally true for each of the PAD_P shapes depicted above.

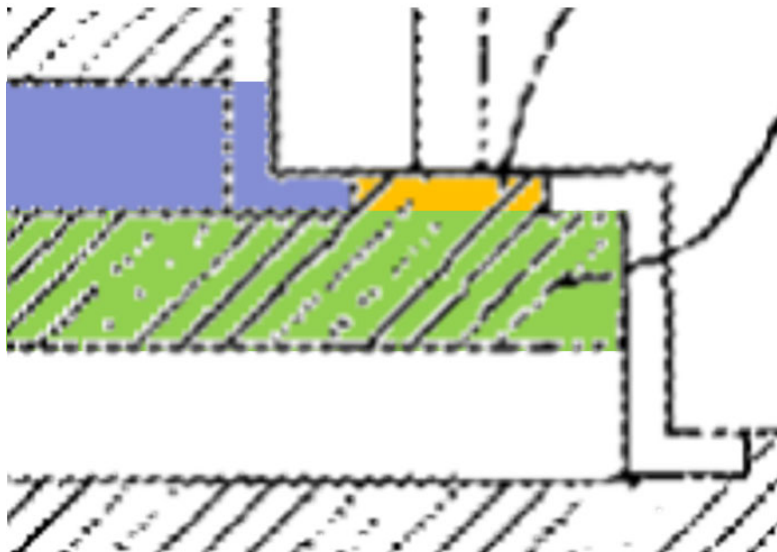


120. I note however that in the demonstrative Dr. Lee provides between paragraphs 266 and 267 of his declaration (reproduced below), the PAD_P in the far right image showing the side view has an unexplained shape.

FIG. 6



It is unclear to me what the small rectangles on either side are meant to be. Further, when I zoom in, there appears to be a curvature shown in the x-z plane, but it is unclear if this is intentional or not as it is unexplained. As I explained above in Paragraph 96, regardless of the shape of the openings formed in the photosensitive resin pattern M, the resulting structure will look the same in the x-z plane of Kim's Figure 4B, which I again depict below. The only difference would be the width of the orange portion in the x-direction (left to right in the figure below). There will always be vertical (z-direction), straight contact between the annotated blue and orange regions because the entirety of the injected regions 122_I are removed and the openings 122_O are filled with conductive material. This does not satisfy the claimed "curved side surface."



121. While Dr. Lee states that "a POSITA also would have been motivated to employ this shape [the one shown above his paragraph 267] and

would have expected to succeed when doing so,” Ex. 1003 ¶267, he provides no explanation for why a POSITA would obtain these shapes. The shape of PAD_P in Kim is a function of Kim’s photosensitive resin pattern M and would be selected depending on margins associated with landing contacts and contact shape. The shape of PAD_P will not further improve the short-circuit problem beyond what Kim’s offset from the edges of PAD_B already does, which I explain in the next section.

122. Further, neither Kim nor Dr. Lee describe what the appropriate sizing would be for these shapes Dr. Lee shows in paragraphs 263 and 266 of his declaration. The size of each shape could affect the performance of the memory device, but Dr. Lee never discusses these sizing parameters when arguing that a POSITA would be motivated to form such a shape.

1. Kim, Alone or in Combination, Does Not Teach nor Render Obvious a “first side surface comprises a curved side surface”

a. A POSITA Would Not Have Been Motivated to Modify Kim to Reduce the Risk of Short-Circuit

123. Dr. Lee asserts that “a POSITA would have recognized that using a ‘curved’ side surface with Kim’s pads would have improved Kim by increasing the minimum distance between the pad and adjacent conductive layers, thereby reducing the risk of short circuit.” Ex. 1003 ¶245. This is the only reason given for why a POSITA would change Kim’s process. But a POSITA would not have

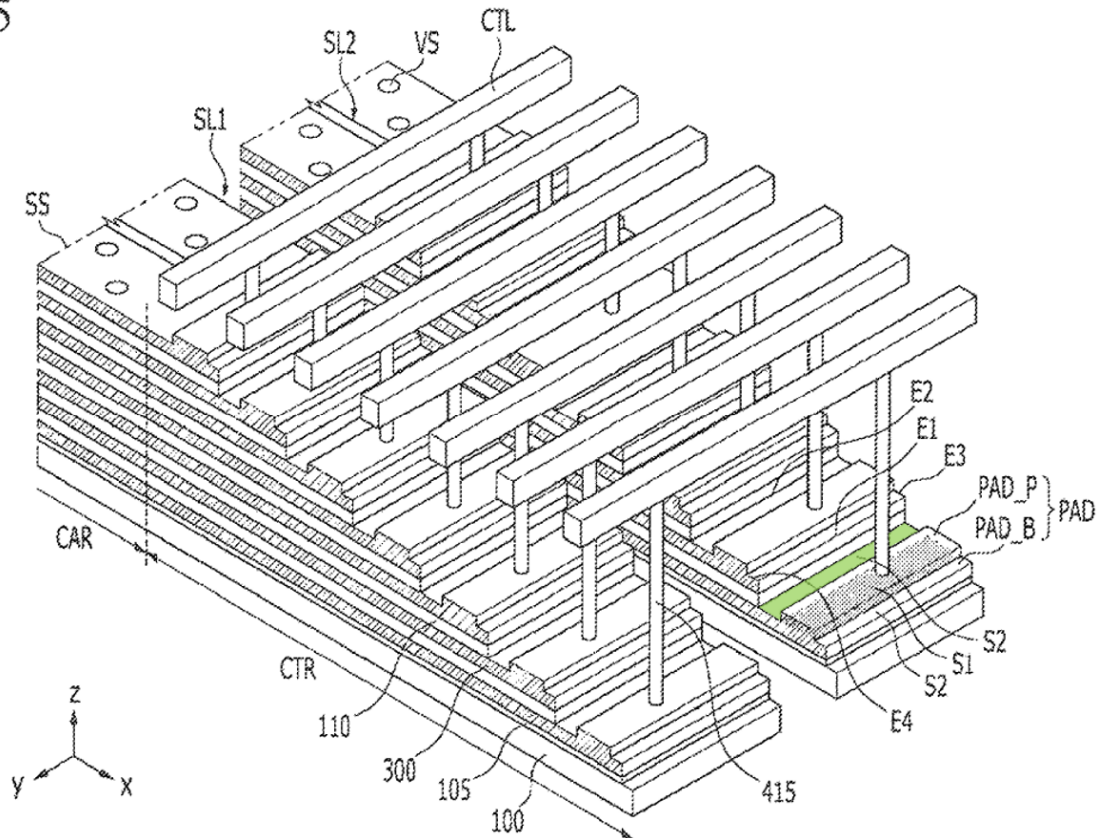
been motivated to change Kim's process to reduce the risk of short-circuit because Kim already accounts for the risk of short-circuit in multiple but different ways. Thus, Dr. Lee and the Petition provide no reasons at all for why a POSITA would modify Kim's process to have the claimed "curved side surface."

124. In my opinion, a POSITA would not be motivated to modify Kim "by increasing the minimum distance between the pad and adjacent conductive layers, thereby reducing the risk of short circuit." *Id.* This is because Kim already has numerous features that address and solve this very same short-circuit problem.

125. I explained Kim's process above. As part of its process, Kim explains that the protrusion pad PAD_P is formed "inside from the edge of a surface of the base pad PAD_B to prevent the short-circuit between the pad units PAD positioned as different rows." Kim 9:46-49, Figs. 5-9. What would be apparent to a POSITA from this process, and what is depicted in Kim, is that Kim's process ensures that the PAD_P is set off from the adjacent conducting layer in the step direction (x-direction in the figure below) to avoid a short-circuit. The set off has been highlighted in green in the figure below. As I explained above, this set off is created because Kim uses photosensitive mask pattern M to precisely control the location of the PAD_Ps. By providing the green offset, Kim's process already increases the minimum distance between the

pad and adjacent conductive layers to prevent a short-circuit. Kim's process further deals with this by ensuring that pad unit's of adjacent conductive layers do not overlap. *Id.* 7:63-67.

FIG. 5



126. A POSITA would know that this offset could be precisely controlled for these types of devices. Kim itself makes this clear by describing that the PAD_Ps could be made narrower, showing the accuracy of the mask. Kim 11:57-12:11, Fig. 9. I note that Dr. Lee points to this same disclosure as an explanation for why a POSITA would want to round the sides of the PAD_P. Ex. 1003 ¶246. But Kim merely says that differing widths may be used. Kim never suggests that a width so large as to erase the green offset such that short-circuits

are again a problem should be used and a POSITA would not read Kim in such a way.

127. Dr. Lee confirmed that Kim avoids short circuits using offsetting during his '666 patent deposition.

Q. Okay. **So Kim teaches that offsetting the adjacent conducting layer in the step direction helps to avoid a short circuit;** is that fair?

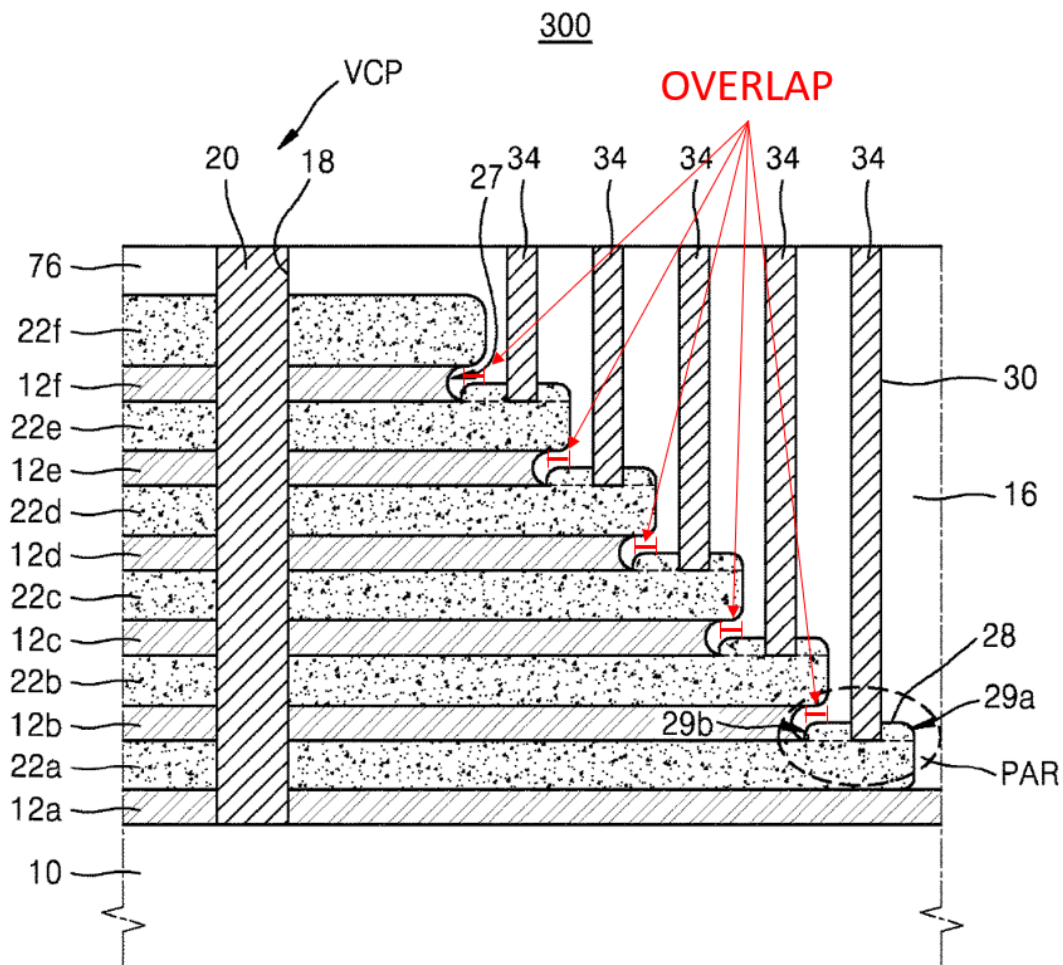
A. **Yeah.** You have to offset it. Otherwise if you don't offset it, you will have short circuit. So, **yes, Kim does provide a technique -- one technique to prevent shorting?** Ex. 2031 183:22-184:8.

128. Dr. Lee only points to Park as teaching that rounded pad side surfaces help prevent short-circuits. Ex. 1003 ¶246. But Park and Kim are fundamentally different in this regard such that a POSITA would not look at Park as teaching something useful in Kim's process.

129. With respect to Park, Dr. Lee mixes his discussion and explanation of the reference. Park describes an embodiment in connection with Park Figure 5, and a different embodiment in connection with Park Figure 7. In describing Park, Dr. Lee includes discussion regarding both embodiments. *See* Ex. 1003 ¶¶227-230, 243, 246, 250-251, 258, 260. Dr. Lee never includes Park Figure 5 despite citing discussion about it. He instead applies that discussion to Park Figure 7 without explanation. This matters because, according to Park, the

Figure 7 embodiment “do[es] not have a stepped form.” Park (Ex. 1009) 9:50-59. Kim, on the other hand, does have a stepped form. Dr. Lee provides no explanation for why a POSITA would look to a reference without a stepped form and be motivated to apply it to Kim, which does have a stepped form. Below is Park’s Figure 5 embodiment, which has a stepped form, which I have annotated to note the overlap between Park’s pad regions (PAR). This overlap creates a higher risk of short-circuit in Park’s pad regions and is part of the reason why Park uses a process with rounded pad regions. *See, e.g.*, Park 7:17-22.

FIG. 5



130. As explained above, Kim does not have this overlap because it uses the photosensitive resin pattern M to precisely control the location of its PAD_P to avoid overlap and to avoid this short-circuit problem. *See, e.g.*, Kim 7:63-67 (“The pad unit PAD and the adjacent pad unit PAD may not overlap with each other.”). Park, by contrast, does not use a mask pattern to control the location of its pad regions.

131. As noted above, Park itself explains that the Figure 7 embodiment is similar to the Figure 5 embodiment with the exception that the stacked layers “do not have a stepped form but are inclined.” Park 9:53-58. As shown in Figure 7, the lack of steps means a lack of pad regions for connection of individual word lines. In other words, in Figure 7, aside from the single contact 84 shown, the other conductive layers 72c-72f are not used as word lines. A POSITA would not find Park’s Figure 7 embodiment suitable for 3D memories like those in Kim or the ’838 patent. For example, as the ’838 patent explains, “[a]s the demand for higher storage capacity continues to increase, the number of vertical levels of the staircase structures also increases.” ’838 patent 5:36-39. In other words, to increase the density of 3D memories, more stairs are desirable. Park’s Figure 7 embodiment does not have this feature. Furthermore, like Park’s Figure 5 embodiment, Park’s Figure 7 embodiment also does not use a mask pattern to control the location of its one pad region. Because Kim’s process forms its PAD regions in a completely different way, a POSITA would understand that (a) Kim does not need rounded sides for the reasons Park explains and (b) Park’s pad regions could not be swapped into Kim’s structure without completely changing Kim’s process, which would eliminate numerous stated benefits in Kim,

including this short-circuit problem that Kim solves through its process. Dr. Lee did not provide any reason or motivation for a POSITA to do so.³

132. Another way that Kim addresses short-circuits is that Kim retains “auxiliary insulating layer 122 positioned between the adjacent protrusion pads PAD_P positioned at different rows.” Kim 9:50-55, Fig. 4B. As Kim explains, because of this, “the short-circuit between the pad units PAD may be effectively prevented.” *Id.* 9:50-55, Fig. 4B. As I explained above, this is a result of Kim’s process using photosensitive resin pattern M with the green offset I depicted above. Because only the specific regions 122_I in Kim are subjected to the ion injection process, the other portions that remained covered by the solid (pink) part of the photosensitive resin pattern M are unaffected and remain in place and provide insulation between the PADs in Kim.

133. Should short-circuits between PAD regions still be a concern to a POSITA, Kim provides a third way to prevent short-circuits. As Kim explains, if due to the PAD_P a minimum distance rule would be violated, the “z-direction

³ The same is true of Park’s Figure 8 embodiment, which Dr. Lee and the Petition occasionally cite as well. Like Park Figure 7, Park Figure 8 also does not have a stepped structure and has only a single contact to a single pad. Park at 11:6-13, Fig. 8.

thickness of the insulating layer 110 may be larger than the minimum distance in the z-direction between two adjacent pad units PAD to effectively prevent a short-circuit between the two adjacent pad units PAD.” Kim 8:66-9:11. What this means is, if a POSITA is making Kim’s device and has a short-circuit problem, Kim instructs the POSITA to slightly thicken the insulating layers as a further measure to avoid short-circuits.

134. In my opinion, because Kim already provides its process three different ways to avoid short-circuits between adjacent PAD regions, a POSITA would not be motivated to change Kim in order to solve a problem Kim had already solved. A POSITA especially would not do so based on Park, which is the only reference Dr. Lee cites for his opinion, because Park’s structures (Figure 5 and Figure 7) are formed by a different process that has a more problematic structure for short-circuits and does not provide ways to avoid the short-circuit like Kim already does.

b. A POSITA Would Not Have Modified Kim In View Of Park, Yun, Or Nam

135. As explained in the previous section, a POSITA would not be motivated to modify Kim to avoid short-circuits. Dr. Lee’s only other explanation is that “this type of pad was also well known in the art as shown, not only by Kim, but also by Park, Yun, and Nam.” Ex. 1003 ¶243; *see also id.*

¶226. But this is wrong too. First, as I explain further below, Yun does not teach

a pad region with curved side surface in contact with the first material layer, as required by claim 13. Thus, a POSITA modifying Kim according to Yun's teaching would not arrive at the claimed structure. Second, given that Dr. Lee and the Petition put forward only two references that purportedly show a curved pad region in the correct location, this does not prove that such structures were well known to a POSITA. For example, neither Dr. Lee nor the Petition point to textbooks showing such a structure that may suggest that a POSITA would have been well aware of such structures. Third, semiconductor processes are not so simple that a POSITA simply sees a particularly shaped structure and substitutes it into a structure made by a different process. The pad regions of each of Park, Yun, and Nam are formed through processes significantly different from Kim's. I address these differences below for each reference.

136. As to all three references, Dr. Lee only says that “[a] POSITA would have recognized that this process could be readily adapted to form a curved opening that surrounds a curved contact pad.” Ex. 1003 ¶256. His explanation is that “the ion implantation step shown in Figure 12 of Kim would simply be tailored to form a ‘doped region 122_I’ with curved rather than straight sides. The rest of the process would proceed in the same way, resulting on contact pads located within an opening 122_O in insulation layer 122 with curved sides.” *Id.* Notably, Dr. Lee never explains how the ion implantation step could be tailored

in this way. Indeed, it could not for the reasons I explained in connection with describing Kim's process. Specifically, Kim creates openings in the photosensitive resin pattern M so that the entire region 122_I is doped and subsequently removed. Rounded corners cannot be formed in this process. And because the pad regions of each of Park, Yun, and Nam are formed through processes significantly different from Kim's, a POSITA would not modify Kim's process absent very compelling reason, which Dr. Lee and the Petition fail to give.

Park (Ex. 1009)

137. Part of the reason why a POSITA would not be motivated to modify Kim to improve short-circuits in the way suggested by Park is because the processes in Kim and Park are very different. Dr. Lee does not address this.

138. Dr. Lee notes that Park also uses ion implantation, Ex. 1003 ¶¶257-258, but the ion implantation in Park is not what creates the rounded sides. And so Park does not teach a POSITA a way to tailor the implantation step of Kim as Dr. Lee states. *Id.* ¶256.

139. Instead, as Dr. Lee admits, Park uses oxidation and ion implantation to arrive at rounded sides. The rounded shape is a result of the oxidation and not the ion implantation. As Park explains, “[a]s shown in FIG. 6C, an additional insulating layer 40 is formed by oxidizing surfaces and side surfaces of the

stepped sacrificial layer patterns 14a through 14f that are externally exposed.

The additional insulating layer 40 may be formed by thermally oxidizing the surfaces and the side surfaces of the sacrificial layer patterns 14a through 14f. ...

One end of the additional insulating layer 40 may be rounded by an oxidation process.” Park 8:28-38, Fig. 6C. As can be seen in Park Figure 6C the rounded shape already appears before any ion injection occurs, which happens in a subsequent step. *Id.* 8:43-51, Fig. 6D.

140. Dr. Lee does not explain how a POSITA would add this oxidation step to Kim’s process to create rounded sides, let alone why a POSITA would do so. In my opinion, a POSITA would not be able to substitute Park’s additional insulating layer 40, formed through thermal oxidation, into Kim’s process and would not be motivated to do so. In Park, the additional insulating layer 40 is grown through thermal oxidation on sacrificial layer 14a-14f. Because of the intervening insulating layers 12b-12f, the additional insulating layer 40 is discontinuous, grown only on the tops and sides of the sacrificial layers. Park 8:28-38; Fig. 6A-6C. The discontinuity is necessary in Park because the entirety of the additional insulating layer 40 becomes conductive after subsequent processing steps. Park 8:43-9:21, Fig. 6F. By contrast, Kim forms a continuous auxiliary insulating layer 122 over its entire stepped structure. Kim 12:58-60, Fig. 11. This continuous structure is one of the key features in Kim. As Kim

explains, “the short-circuit between the pad units PAD may be effectively prevented through the auxiliary insulating layer 122 positioned between the adjacent protrusion pads PAD_P positioned at different rows. The semiconductor memory device according to same [sic] embodiments of the inventive concepts may have enhanced reliability.” *Id.* 9:50-55. To achieve a rounded side as Dr. Lee suggests, a POSITA would have to change Kim’s process at least by not forming the auxiliary insulating layer 122 and not using the photosensitive resin pattern M to precisely locate its PAD_P, two key features of Kim’s process. Indeed, the portions of Kim’s auxiliary layer that Dr. Lee and the Petitioner suggest rounding are not exposed, and oxidizing them would not create rounding. Moreover, this would eliminate Kim’s stated enhanced reliability and other advantages described above. Removing those steps would effectively abandon Kim’s process, as they are key parts of the process, and use Park’s process from the start. There is no reason for a POSITA to modify Kim in this way, and Dr. Lee does not provide any explanation.

Yun (Ex. 1021)

141. Dr. Lee provides no explanation at all for why a POSITA would look to Yun to modify Kim. While Dr. Lee states “numerous prior art references similarly employ ion implantation to form contact pads with rounded or curved sides,” he does not cite Yun as one of them. Ex. 1003 ¶¶257-60. Yun does not

mention ion implantation. Dr. Lee's only purported basis is that that curved structures were well known, Ex. 1003 ¶¶226, 243-244, but as noted above Yun does not even disclose a curved surface that would lead to claim 13's structure, and Dr. Lee has not demonstrated that such structures were so well known that a POSITA would be able to simply modify Kim's process to use them. In my opinion, a POSITA would not have been motivated to modify Kim's process to try and use pad structures from Yun.

142. Furthermore, in every embodiment of Yun, the side of pads 120 that are closest to the interlayer insulating layers 102 are not rounded or curved. As Yun explains, the "inner side surface of the protrusion part 65 may have a flat surface," while only the "outer side surface," away from the interlayer insulating layers 102 "may be rounded." Yun (Ex. 1021) 8:31-40, Fig. 3, Figs. 5A-5F. Furthermore, in every embodiment of Yun, the inner side surface of the pads 120 does not contact the interlayer insulating layer 102. A POSITA would therefore understand that the portion of Yun's pads that Dr. Lee says Kim could simply be tailored to use would not have a "first side surface comprising a curved side surface" that is "in contact with the first material layer" as recited in claim 13.

143. While Dr. Lee has pointed to no motivation to do so, a POSITA looking to use Yun's pad structures in Kim's process would recognize the differences in those processes and that significant changes would be needed to

Kim. Yun's pad structures are formed thicker on the stepped area to provide "a process margin for forming contact plugs 150 having different vertical heights." Yun 7:27-33. Kim already includes PAD_P for this very reason. Kim 11:48-50. Thus, a POSITA would have no reason to use Yun's pad structures in place of Kim's. Furthermore, Yun does not use a mask pattern to create its pad structures, and therefore cannot precisely control their location and provide margin against short-circuits in the same way that Kim already does. In my opinion, a POSITA would not be motivated to make such changes to Kim, which would negate some of Kim's advantages, as I have discussed above, without any benefit.

Nam (Ex. 1022)

144. Dr. Lee provides no explanation at all for why a POSITA would look to Nam to modify Kim. While Dr. Lee notes that Nam also uses ion implantation, Ex. 1003 ¶259, the ion implantation in Nam is very different from that in Kim, as is the rest of Nam's pad formation. And so Nam does not teach a POSITA a way to tailor the implantation step of Kim as Dr. Lee states. Ex. 1003 ¶256.

145. Nam purports to form a convex, or bull nose shaped, pad regions by injecting impurities into a sacrificial layer to create a damaged region, and then enlarging the damaged regions through heat. Nam (Ex. 1022) [0099]-[0100], Fig. 32, Fig. 33, Fig. 34, Fig. 36. Thus, in Nam, ion injection is performed such

that impurities are implanted toward the center of the sacrificial layer in the area where the pads are formed. *Id.* [0099], Fig. 33. The curvature in Nam supposedly results from the application of heat when forming another layer causing diffusion of the impurities and an increase in the volume of the damaged regions. Nam does this because it wants to increase the size of the pad regions to avoid the problem of the contact punching through the pad causing a short-circuit between gate electrode layers. *Id.* [0044]-[0045], [0065], [0107]-[0108], Fig. 7, Figs. 8A-8B, Fig. 37, Fig. 39. But as can be seen by comparing Nam's Figures 34, 36, and 37, the increase in the pad size has the effect of pushing the pads closer together. Decreasing that distance could lead to a short-circuit defect between gate electrode layers. I further note that Nam does not provide any description or way to mitigate a potential short-circuit defect between gate electrode layers.

146. Nam's process described in the last paragraph is different from Kim's process. Rather than performing ion injection on the sacrificial region in hopes of enlarging it, Kim performs ion injection through the photosensitive resin pattern M into the auxiliary insulating layer 122 that was formed on top of the sacrificial layer. As I explained above, this precisely controls the location of Kim's PAD_P. A POSITA would see Kim's existing process as more controllable and less likely to lead to defect than a process like Nam's which

even the Petition explains can result in a range of structures if followed.

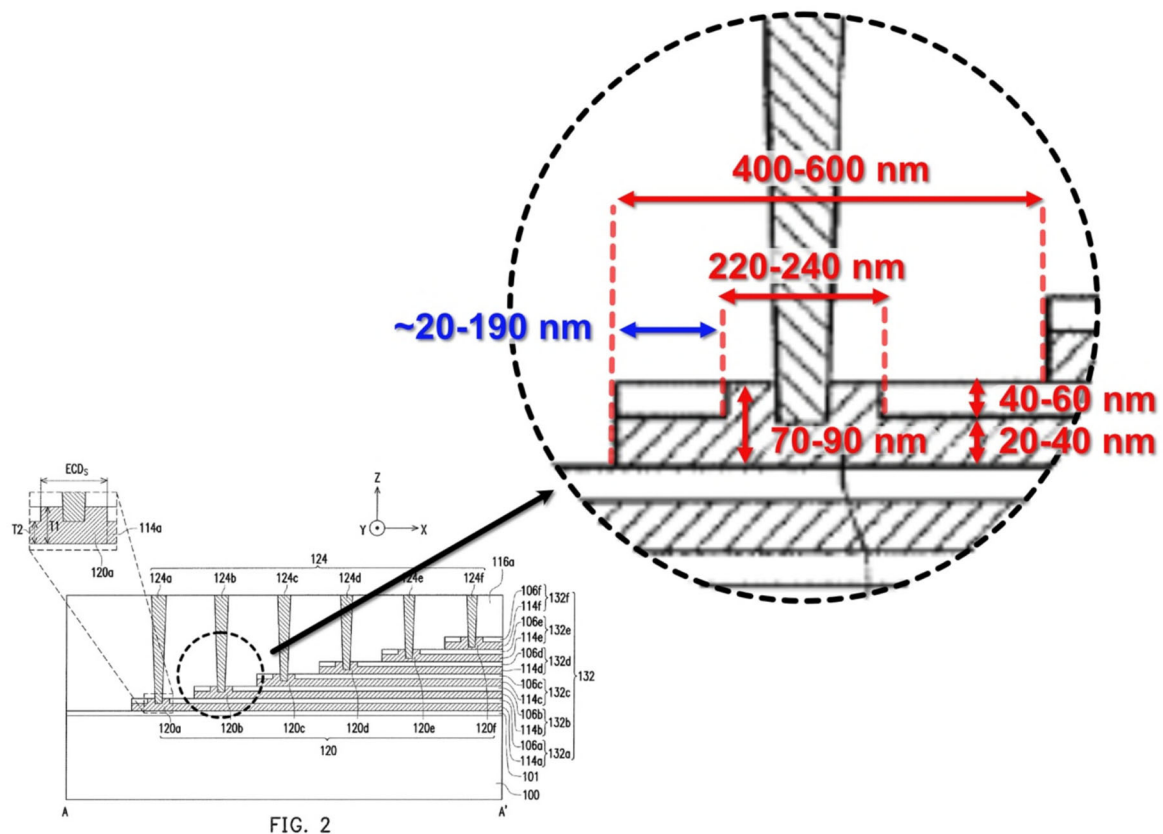
Moreover, as I already explained, Kim's PAD_P already solves the very problem of punch through in forming contacts that Nam tries to solve with its enlarged pad regions. Kim 7:58-8:28, 11:48-56. In my opinion, a POSITA would not be motivated to make such changes to Kim, which would negate some of Kim's advantages, as I have discussed above, without any benefit.

147. Thus, in my opinion, a POSITA would not modify Kim for any of the reasons suggested in the Petition and by Dr. Lee. As Kim does not show the claimed "curved side surface" on its own, nor render it obvious, a POSITA would not have found claim 13 obvious with respect to Ground 1.

IX. Ground 2: Claims 3 and 18 Are Not Obvious In View of Kim and Yang (Ex. 1007)

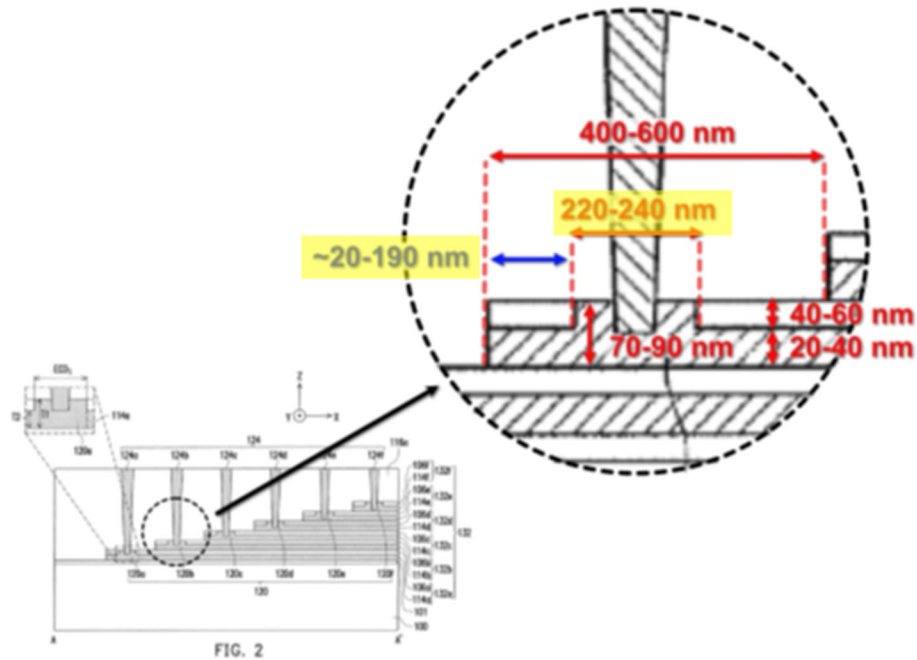
148. The Petition and Dr. Lee assert that a POSITA would combine Kim and Yang to arrive at claims 3 and 18. I note that the Petition recognizes that "Kim does not provide a numerical example quantifying the distance between the side of its landing pad and the side of the conductive layer below it." Pet. 54. However, the Petitioner claims that "a POSITA would have considered it obvious to employ a value falling within the range required by these claims: "10 nm and 300 nm." *Id.* I disagree.

149. Yang is the only reference the Petition and Dr. Lee cite to support their argument. Pet. 54-59. They claim that Yang discloses the dimensions annotated below.



Pet. 57 (numbers added by Petitioner).

150. But Yang does not disclose each of these dimensions as Petitioner claims. I have highlighted the dimensions Yang does not disclose in yellow.



Pet. 57 (yellow highlighting added).

151. First, Yang does not disclose the contact pad width. Dr. Lee himself admitted that Yang does not explicitly disclose creating contact openings that are 193 nm.

Q. But Yang does not disclose using the 193 nanometer ArF excimer laser stepper to create contact openings that are 193 nanometers.

A. Not explicitly. Ex. 2030 (Lee '838 Dep.) 77:1-5 (objections omitted).

152. Instead, Dr. Lee states regarding the contact pad width:

Yang also explains that its contact pads have a “width ECDs” that “is greater than the sum of the width ECDc of the contact openings 122” connecting to the pads and “two specification values S (i.e., $ECDs > ECDc + 2S$).” Yang, 10:7-21. Yang provides an example

where the contact opening is formed using a “193 nm- ArF excimer laser stepper” with a “specification value S ... in a range of 10 nm to 20 nm, for instance.” *Id.*, 10:17-21. In other words, in this example, ECDc would be 193 nm (or ~200 nm), and S would be in the range of 10-20 nm. This in turn means that ECDs (the size of the contact pad) is greater than either 200 nm + 20 nm or 200 + 40 nm, or a value in the range of ~220-240 nm. Ex. 1003 ¶311.

153. In short, Dr. Lee calculates the contact pad width by assuming that the width of the contact openings 122 (discussed in Yang as the “width ECDc”) is ~193 nm only because the contact opening is “formed using a 193 nm-ArF excimer laser stepper.” Ex. 1003 ¶311. A POSITA would not make such an assumption as there is no reason for it. Dr. Lee himself recognized that the size was not dictated by the laser wavelength alone. Ex. 2030 75:13-21. Thus, the contact openings in Yang are not the same width as the wavelength of the laser used to form them because the laser wavelength alone does not set feature size.

154. A POSITA would have understood and known in 2017 that a ArF excimer laser can print features both far larger and smaller than their wavelength using standard techniques. For example, as discussed in one 2014 article, a chip had features “sized ten times smaller than the wavelength of laser used in lithography.” Ex. 2025.

155. Yang states that the “when the exposure machine applied to perform the manufacturing process of the contact openings is a 193 nm-ArF excimer laser

stepper (manufactured by ASML, model 1450H), the specification value S may be in a range of 10 nm to 20 nm, for instance.” Yang 10:16-21. ASML is a known manufacturer of lithography lasers and its model 1450 laser was known to form features both larger and smaller than the wavelength of the laser. For example, in a 2006 press release, ASML stated that its 193-nm excimer laser XT:1450 could form a features having a size of 57 nm. Ex. 2026. ASML’s own website recognizes that its 193 nm Ar-F laser “enabled features sizes of 38 nm to be printed.” Ex. 2027. Thus a POSITA would not have understood that the contact openings would match the laser wavelength, as there is a range of feature sizes the 193 nm laser could form, both larger and smaller than the ~193 nm that Dr. Lee assumes is used in Yang. Dr. Lee himself admitted that a POSITA could use the laser described in Yang to make contact openings larger and smaller than 193 nm.

Q. So you could use the excimer laser described in Yang **to make contact openings larger than 193 and smaller than 193 nanometers**. Correct?

A. **You could**, but once again, the prior art reference number similar to Kim, such as Yang, in this case, simply provide a – an example and relevant dimensions for someone who would like to implement Kim's structure. Ex. # (Lee Dep.) 75:13-21.

156. Second, Yang does not provide dimensions of purported lateral displacement of the side of the landing pad and the side of the second material layer beneath it. Instead, Dr. Lee purports to calculate it, based on measurements provided in Yang as well as three unfounded assumptions: (1) contact pad width (which I discussed above), (2) the pads being in the approximate middle of the stair, and (3) that Yang's pads would be set back by at least 20 nm. I have bolded those unfounded assumptions from Dr. Lee's declaration below.

Given these dimensions, a POSITA would have recognized that **if the pads are located approximately in the middle of each staircase step**, Yang's pad will be set back from the edge of the underlying conductive layer 114 by ~80-190 nm. This range can be determined as follows: the staircase step has a length of 400-600 nm. **The contact pad has a width of 220-240 nm.** The maximum amount of uncovered step space would be 600 nm – 220 nm, or 380 nm. When the contact pad **is located in the middle of the step**, there will be 190 nm of space between the pad and the step edges. The minimum amount of uncovered step space would be 400 nm – 240 nm, or 160 nm. When the contact pad **is located in the middle of the step**, there will be 80 nm of space between the pad and the step edges. Ex. 1003 ¶312.

But, as shown in Figure 2, when doing so **the space between the pad edge and the end of underlying conductive layer still**

correspond to at least the minimum thickness of the conductive and insulating layers. *See id.* ¶314; Yang Fig. 2.

Thus, a POSITA would have understood that Yang's pads would **be set back by at least 20nm (the minimum layer thickness contemplated by Yang).** Ex. 1003 ¶315.

157. As I discussed above, Yang does not teach the contact pad width.

158. Dr. Lee's next assumption, that the pad is located in the middle of the stair, is also not taught by Yang. Indeed, Dr. Lee admitted that he did not "think explicitly they—Yang disclose that relevant -- relative position" of the pads "situated approximately in the middle of each step." Ex. 2030 79:2-80:14. Instead, Dr. Lee resorted to stating that it was a "common practice" and shown in Yang "Figure 2."

Q. Other than Figure 2, do you rely on any other disclosures in Yang for your opinion that Yang's pads are situated approximately in the middle of each step?

A. **I don't think explicitly they – Yang disclose that relevant -- relative position**, but a person of ordinary skill in the art would understand that not only Figure 2 illustrate the pad is situated approximately in each -- in the middle of each step of the staircase, but in practice, you also want the pad to be in the middle -- approximately in the middle of each step because if you get too close to one side, to the right or one -- on the -- too close to the -- to the left, any slight misalignment will give you a nonfunctional chip. So,

therefore, by usual practice and ensure good tolerance of the -- the process and such that you create, which we saw in the highest yield of the manufacturing fabrication process, that it is a standard process, standard practice to put the pads to be located approximately in the middle of each step of the staircase structure. So Yang does not have to explicitly mention that or disclose that in these specifications. It is well understood and it is well common practice. Ex. 2030 79:2-80:8.

159. But neither Dr. Lee's declaration nor the Petition mention why a POSITA would assume the pad is in the center of each step. Indeed, the '838 patent itself places the pad at the end, and not the center, of the step. '838 patent Fig. 8. In addition, many prior art references identified by Dr. Lee, including Lee, Yun, and Park, show the pad placement at or near the end of the step. Lee Fig. 7B; Yun Fig. 5A; Park Fig. 7. And while I am not a lawyer, my understanding from counsel is that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue. Since Yang's specification says nothing about the location of the pad on the step, Figure 2 cannot evidence the sizes of the pad and the dimensions between the pad edge and the edge of the stair.

160. Dr. Lee then assumes "the space between the pad edge and the end of underlying conductive layer still correspond to at least the minimum thickness of the conductive and insulating layers." Ex. 1003 ¶314. Such an assumption is

non-sensical to a POSITA. There is no basis to assume that the thickness of the conductive and insulating layers in Yang (which are vertical dimensions) would correspond to the space between the pad edge and end of underlying conductive layer (which is a horizontal dimension). A POSITA would have understood those are completely different dimensions and thus would not have equated them to each other. Indeed, there is no correlation between thickness (a vertical dimension) and offset (a horizontal dimension). And even if Fig. 2 in Yang shows the size of the thickness of the conductive and insulating layers being nearly the same as the offset of pad edge and underlying conductive layer (and even that is a stretch), my understanding from Counsel is that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue. Here, Yang's specification is silent on the amount of offset and thus Yang Figure 2 cannot be used to show the dimensions of the offset.

161. Even if Yang taught the dimensions Dr. Lee purports it teaches (and it does not), a POSITA would not be able to import Yang's dimensions into Kim because the two references rely on fundamentally different processes in creating the staircase structure. Instead, a POSITA would have understood that incorporating Yang's dimensions into Kim (as Dr. Lee and the Petition suggest) would require a wholesale redesign of Kim.

162. As I describe above, and as Dr. Lee admits in his declaration, Kim's structure is formed by first creating a "step-shaped 'stacking structure SS'" by forming "a 'plurality' of alternating 'insulating layers 110 and ... gate electrodes 300' located over a 'substrate 100.'" Ex. 1003 ¶99; Kim 5:53-55, Fig. 4B. After these steps are created, auxiliary insulating layer 122 is deposited on the steps. Kim 12:34-37, 12:57-60. Only **after** auxiliary layer 122 is deposited on the stairs does Kim create openings to form PAD_P structures using the ion implementation process I describe above. *Id.* 12:61-67. Most of the deposited dielectric layer 122 remains as part of Kim's structure. *Id.* Fig. 4B.

163. Meanwhile, Yang uses a completely different process with more steps and there is no reason to use it with Kim. Unlike in Kim, Yang forms openings in both the insulating and sacrificial layers through an etch that occurs alongside step formation "until the stair step structure is formed." Yang 3:11-29. Subsequently, Yang fills the openings with another material compatible with the original sacrificial layer, which will be removed in its entirety later. *Id.* 8:4-17. In one embodiment, the filling material is a nitride while the original sacrificial layer can be polysilicon or nitride. *Id.* 8:14-15, 8:65-66, 6:19-21. After depositing the interlayer dielectric, "a tungsten replacement process is performed to replace the first layers 104a-104f and third layers 112a-112f with tungsten (W)." *Id.* 8:39-41.

164. A POSITA would not be motivated to implement Yang's dimensions into Kim because doing so would require a wholesale redesign of Kim. Indeed, the processes used to form Kim's dimensions and Yang's are distinct and incompatible with each other.

X. Ground 3: Claims 1, 4-7, 12, 16-17, and 19-20 Are Not Obvious In View of Lee

A. Overview of Lee (Ex. 1006)

165. Lee describes 3D semiconductor memory devices with “a plurality of stacked structures is patterned stepwise” in the contact region. Lee (Ex. 1006) [0005]-[0006], [0009]-[0010]. The conductive parts of the stepwise structure are described as having “a pad structure,” and where the conductive parts are not covered by the layer above, the “pad portions have a greater thickness than unexposed portions of the plurality of first conductive layers.” *Id.* [0009]. The pad portions are where “contact plugs” make electrical connections to conductive word lines. *Id.* [0006], [0042], Figs. 7A-7B.

166. A set of alternating layers of “first material layers 21” and “second material layers 22” are formed. *Id.* [0029], Figs. 2A-2B. The “first material layers 21” may be a sacrificial layer to start. *Id.* [0030]-[0031]. The “second material layers 22” are insulating layers. *Id.* [0030]. I note that “first” and “second” layers in Lee are reversed in name compared to those in claims 1 and

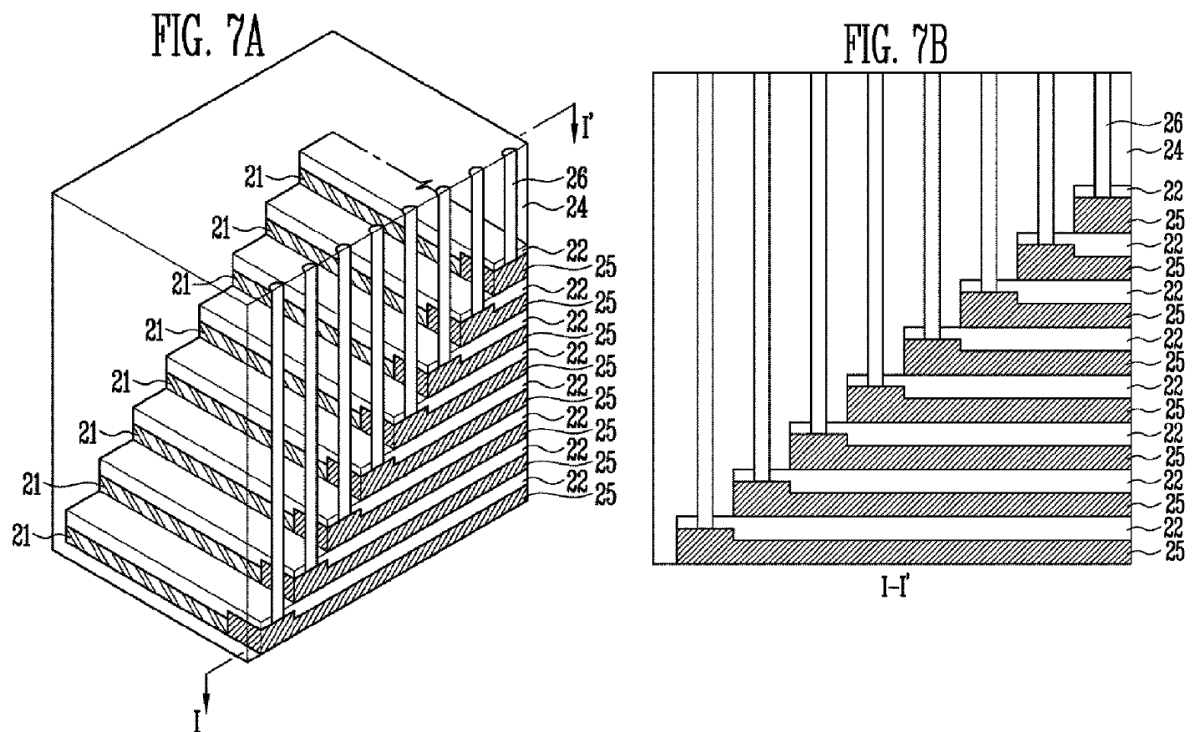
12 as described in the '838 patent. These are then “patterned stepwise.” *Id.*

[0032], Figs. 2A-2B.

167. Impurities are then implanted into the exposed portions of second material layers 22 of the stacked structure. Lee [0034]-[0035], Figs. 3A-3B. Then, recessed regions are formed by removing part of the first material layers 21 by first forming an interlayer insulating layer 24 over the structure, and then introducing an etchant through a slit formed in the stacked structures. *Id.* [0036], Figs. 4A-4B. “As illustrated in FIGS. 5A and 5B, the thickness of ends of the recessed regions RC may be increased. For example, the second material layers 22 exposed by the recessed regions RC may be etched to a predetermined thickness by using a wet etch process. Since an etch rate of the impurity region 23 is higher than that of a region implanted with no impurities, an etch amount of the impurity region 23 may be greater than that of a non-implanted region. Therefore, the ends of the recessed regions RC may be extended.” Lee [0038], Figs. 5A-5B.

168. Subsequently, conductive layers 25 are formed in the recessed regions. *Id.* [0040], Figs. 6A-6B. “As a result, the conductive layers 25 may be formed in which the pad portions PAD exposed at the end of the stacked structure ST may have a greater thickness than unexposed portions of the conductive layers 25.” *Id.* [0041]. Then, contact holes can be formed through the interlayer

insulating layer 24 to expose the pad portions PAD, which holes then can be filled with a conductive material to become contact plugs 26 to the pad portions PAD. Lee [0042], Figs. 7A-7B. Lee Figures 7A and 7B are reproduced below. As can be seen, in Lee's structure, the insulating "second material layers 22" extend over the entirety of the conductive layers 25 below on each step. The contact plugs 26 are formed through the insulating "second material layers 22" to reach the pad portions PAD of the conductive layers 25 beneath.



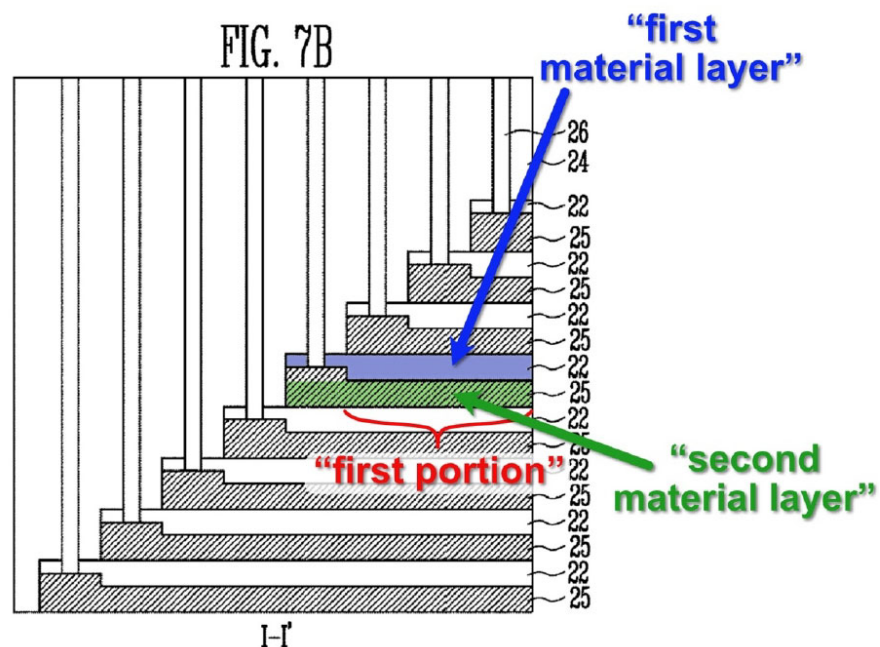
169. Other embodiments are also described, including some relied on by Petitioner's expert. But they are not germane to the discussion below, so I have omitted those details here.

B. Petitioner's Expert Does Not Show Obviousness of Claims 1 and 12 in View of Lee

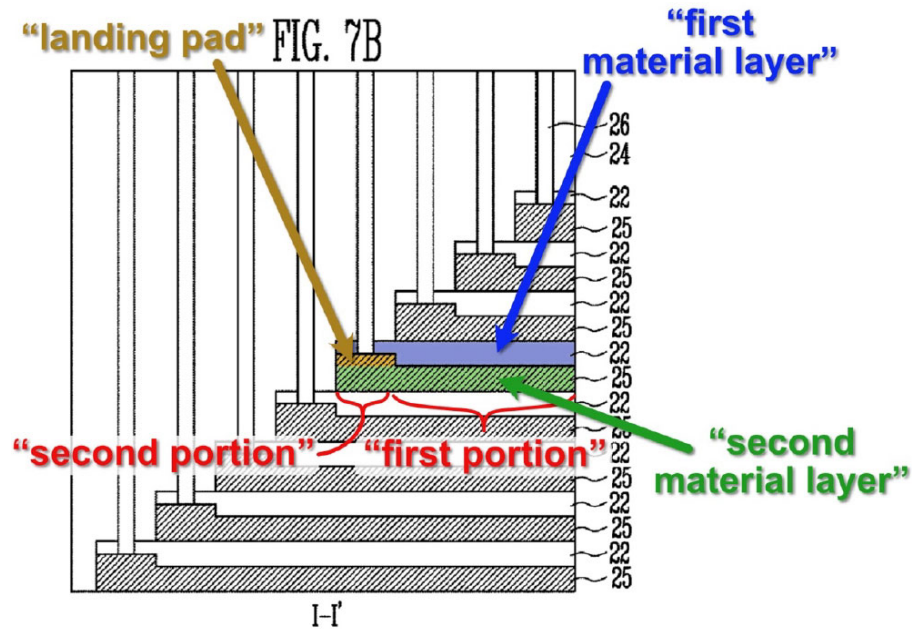
170. I have reviewed Petitioner's expert's mapping of Lee to the limitations of claims 1 and 12 of the '838 patent, and specifically the mapping to the claimed "first material layer," "landing pad," "second material layer," and the "first portion" and "second portion" of the "second material layer." *See* Ex. 1003 ¶¶348-393. As explained in Sections VI and VII above, claims 1 and 12 of the '838 patent describe a specific arrangement and relationship between the "first material layer," the "landing pad," and first and second portions of the "second material layer."

171. Petitioner's expert starts with Lee Figure 7B as annotated below. *See* Ex. 1003 ¶¶351-354. Notably, Petitioner's expert annotates that the "first material layer" extends over the entirety of the "second material layer." Yet, he arbitrarily designates a "first portion" of the second material layer without explaining why. In my opinion, this arbitrary and unexplained selection is due to a hindsight reconstruction of the challenged claims. As Petitioner's expert acknowledges, Lee's layer 22, which Petitioner's expert maps to the "first material layer" of the claims, extends over the entirety of the identified "second material layer." Thus, there is no identifiable "portion" at all that layer 22 is "disposed over" because it is over the entirety of it. This fails to show the structure of claims 1 and 12 of the '838 patent, which describe a correspondence

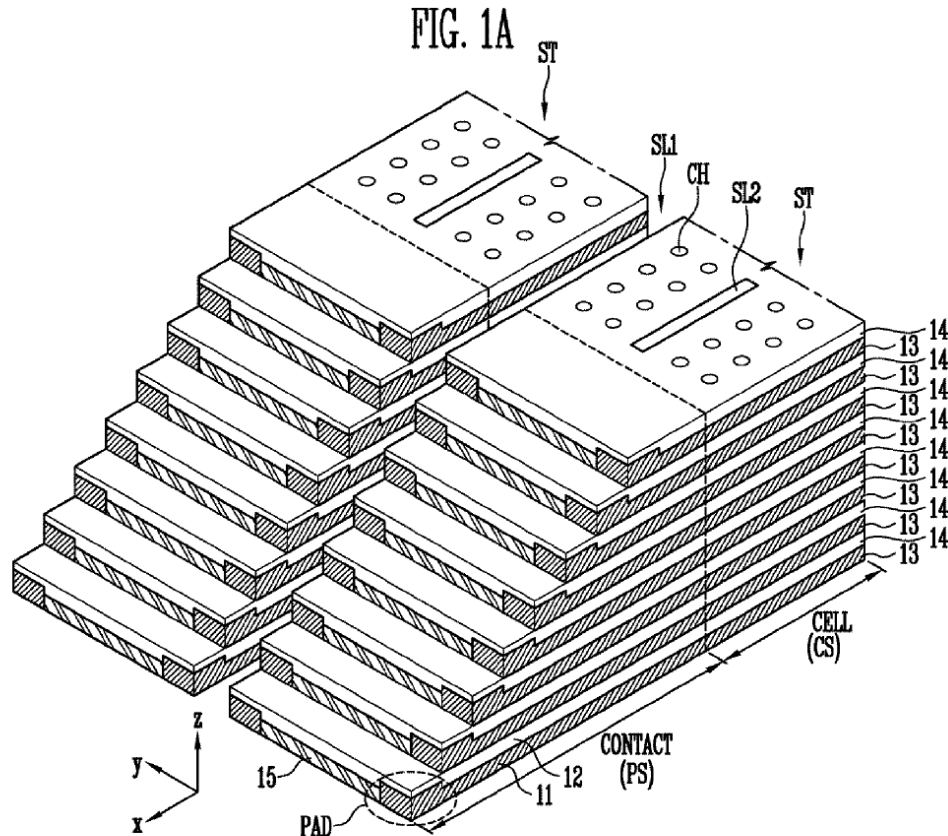
between the “first material layer” and the “first portion of the second material layer.”



172. Despite the lack of explanation for the arbitrary “first portion” label, Petitioner’s expert identifies part of conductive layer 25 as the “landing pad,” annotated in orange below. *See* Ex. 1003 ¶¶356-360. This is also is unexplained.



173. In his analysis, Petitioner's expert states that "the pad portion PAD on the end of each of Lee's conductive layer (annotated orange / brown) is the claimed "landing pad." Ex. 1003 ¶360 (emphasis removed). However, what Petitioner's expert annotates in orange above is not what Lee refers to as "the pad portion PAD" as he states. Instead, Lee explains, referring to Lee Figure 1A, that "[p]ortions of the first conductive layers 11 that are exposed along the stepped end of the pad structure PS may be defined as pad portions PAD." Lee [0023], Fig. 1A. A POSITA would understand that the pad portions PAD are all of the conductive material that is not covered by a step above. Lee indicates this in Figure 1A by circling all of the end of the conductive material 11 and labeling it "PAD."



174. After two arbitrary labels inconsistent with the teachings of Lee itself, Petitioner's expert then labels a "second portion." In my opinion, this series of arbitrary labels that are not associated with the structures described in Lee evidences the hindsight reconstruction of Petitioner's expert's mapping of Lee to the requirements of claims 1 and 12. As claims 1 and 12 require, there is a correspondence between the "first material layer" and the "first portion of the second material layer." Likewise, there is a correspondence between the "landing pad" and the "second portion of the second material layer." Like with Ground 1, Petitioner's expert simply ignores the claimed relationships. But for

the reasons I have given, these relationships describe the claimed structure, identifying the relationships between the claimed features in the claimed structures. To ignore those relationships is to omit them from the claims. Again, one can see this if one considers the claims with “a first portion of” and “a second portion of” (and “the second portion of”) removed. Then there is no defined relationship and no distinct and separate portions claimed. The “landing pad” and the “first material layer” just need to be over the “second material layer.” That is essentially all that Petitioner’s expert shows with Lee. That would also be inconsistent with the discussion above in Sections VI and VII regarding the specification and how the “first portion” and “second portion” are described as separate and distinct as extents in the x-direction.

175. The Petition states that “[t]he claims require only that an insulating layer be ‘disposed over a first portion’ of an underlying conductive layer. They do not prohibit the insulating layer from also covering other portions of the same conductive layer.” Pet. 62. For the reasons explained above, I disagree with this interpretation. In my opinion, it ignores the claimed relationships of the features, renders “first portion” and “second portion” meaningless, and is contrary to the plain language of the claims.

176. Thus, in my opinion, claims 1 and 12 are not obvious in view of Lee as argued by Petitioner's expert. As the remainder of Ground 3 discusses dependent claims, obviousness of those claims also has not been shown.

XI. Ground 4: Claims 3 and 18 Are Not Obvious In View of Lee and Haller

177. The Petition and Dr. Lee assert that a POSITA would combine Lee and Haller to arrive at claims 3 and 18. In particular, they argue that a POSITA would have “understood Lee, when considered in view of the example dimensions of Haller, to render” these claims obvious. Pet. 77. The Petition admits that “Lee does not provide an example of layer 28's thickness.” Instead, the Petition combines Lee with Haller by taking a modified version of Lee Fig. 7B that includes a barrier layer 28 (which I take issue with as discussed above regarding Ground 3) and “apply[] Haller's example spacer and etch stop dimension—30 nm—to Lee” and its barrier layer 28. Pet. 78-79. A POSITA would not be motivated to do that.

178. First, the processes for forming Lee's barrier layer 28 and Haller's spacer and etch stop are very different and incompatible.

179. The process used to form Haller's spacer and etch stop provides near complete control of the dimensions. Haller teaches a wordline comprising “a semiconductor layer 214” and “a passivation layer 216 (e.g., oxide) to separate the wordline from an adjacent wordline.” Haller (Ex. 1008) 4:29-32, Fig. 2. A

recess 302 is then formed into semiconductor layer 214 of the wordlines “by wet etching the semiconductor material comprising the layers 214.” *Id.* 4:37-43, Fig.

3. That recess 302 is then filled by conformally depositing an insulative dielectric material, such as a nitride, to fill the etched recess. *Id.* 4:44-49, Fig. 4. Such a process provides complete control of the size of the spacer, since the dimensions are controlled directly by the amount of etch.

180. Dr. Lee confirmed this process is used by Haller and that it is a “well-controlled process.”

Q. The spacer 502 in Haller is formed by depositing insulative dielectric material into a recess that is 30 nanometers in length. Correct?

A. Right.

Q. So spacer 502 is formed by depositing dielectric material into the recess.

A. That's right. Ex. 2030 116:14-21.

Q. So to form the recess for the spacer, Haller etches under the oxide.

A. Under 216, yes, the passivation limit of the oxide.

Q. So in Haller, the size of the recess is based on the amount of the etch. Correct?

A. That's right.

Q. So the bigger the etch is, the bigger the spacer is.

A. Bigger the recess.

Q. All right. The bigger the etch is, the bigger the recess is. Right?

A. Right. The spacer is not formed yet.

Q. Okay. So in Haller, the size of the recess depends on how big you etch. Correct?

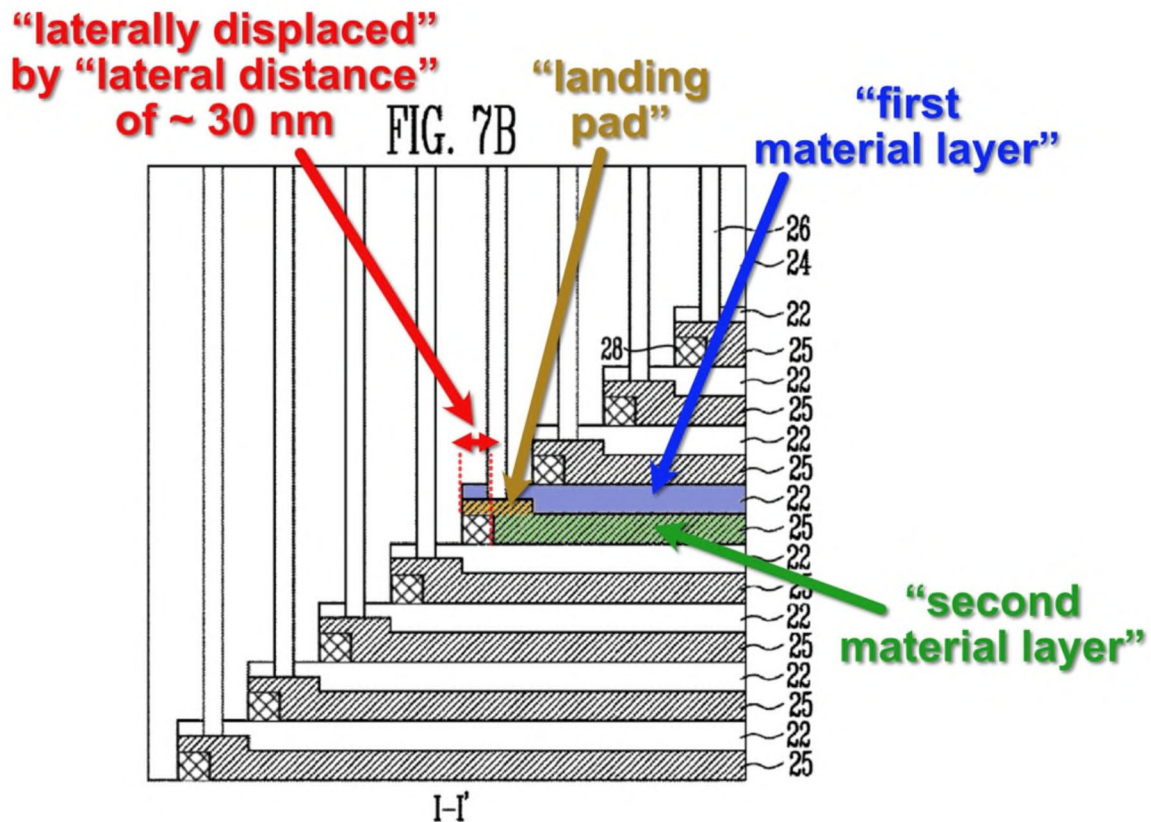
A. The etch back process is a very well-controlled process. *Id.* 116:14-21.

181. Lee's process in forming barrier layer 28 is not so well controlled. Lee's barrier layer 28 is formed by oxidizing sacrificial layer 21. Lee [0048]-[0050]. Lee teaches "a sacrificial layer such as a nitride layer," referring to silicon nitride material typically used in 3D NAND. Lee [0030]. Upon thermal oxidation of nitride with oxygen at temperatures compatible with 3D NAND memory processing (<800-900°C), hardly any oxidation occurs. Kuiper 758-763. Typically, a thin layer of SiO₂ forms on the nitride surface rapidly, which becomes a barrier to further oxygen diffusion. The oxygen can no longer reach the underlying silicon nitride, thereby slowing the oxidation reaction after 1-2 nanometers of surface oxide. Lin G87-G89. Dr. Lee suggests that Haller's 30 nm of spacer may be applied to Lee's barrier layer. But only the first few

nanometers of the silicon nitride may oxidize; that is, the barrier cannot be made as thick as claimed. Kuiper 758-763; Lin G87-G89. Thus, Dr. Lee's arbitrary transfer of spacer dimensions from Haller to Lee fails because Lee's barrier layer cannot be made by Lee's process in the size purportedly taught by Haller.

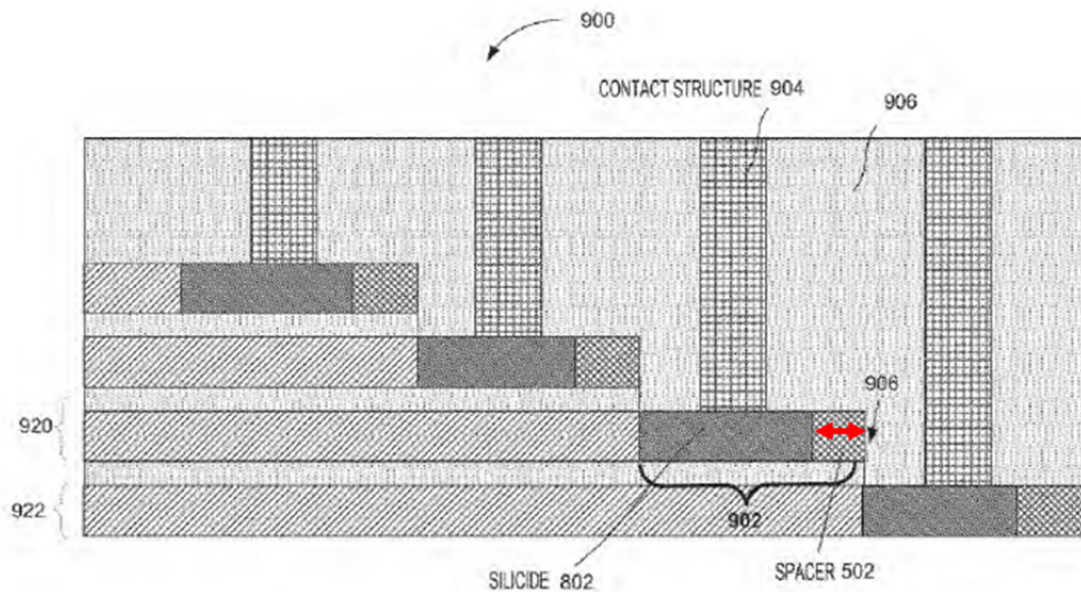
Achieving the dimensions of Haller's spacer in Lee would require redesigning the process in Lee, as the two processes are incompatible. I note neither Dr. Lee nor the Petition identify the degree of control provided by Lee's process.

182. Further, the dimensions of Lee's barrier layer are not analogous to those of Haller's spacer. What Petitioner and Dr. Lee identify as the dimensions of the Lee barrier layer (the red "layer displacement" arrow) is beneath the purported landing pad.



Ex. 1003 ¶447; Lee [0048]-[0050].

183. Meanwhile, as shown in the annotated Fig. 9 from Haller, the spacer dimensions Dr. Lee seeks to import into Lee are not beneath the landing pad but rather next to it. Haller 6:30-42, 6:53-63, Fig. 9.



184. Thus, a POSITA would not consider using dimensions of the Haller spacer for Lee's barrier layer because they are not analogous: they occupy distinct positions relative to the landing pad.

185. Further, a POSITA would not use Haller's spacer dimensions for Lee's barrier layer 28 because they have different purposes. Lee teaches that the purpose of barrier layer 28 is "to ensure an etch margin when the ends of the recessed regions RC are extended" and to ensure "a sufficient distance... between the stacked conductive layers to prevent any deterioration." Lee [0049]. Haller's spacer, however, is not dimensioned based on ensuring etch margins or adding distance between stacked layers. Instead, Haller's spacer is dimensioned to "prevent the wordline contact structure 902 from leaking over the end 906 of the wordline 920, formed by the spacer 502, to the adjacent wordline 922."

Haller 6:59-63. Those are different purposes. Thus a POSITA would not have any motivation to use dimensions needed to prevent misalignment of the wordline contact structure (like those of Haller's spacer) with Lee's barrier layer 28 which is dimensioned for a different reason: so that "since an etch margin is ensured by the barrier layers 27 and 28, a sufficient distance may be ensured between the stacked conductive layers (pad portions) to prevent deterioration." Lee [0049].

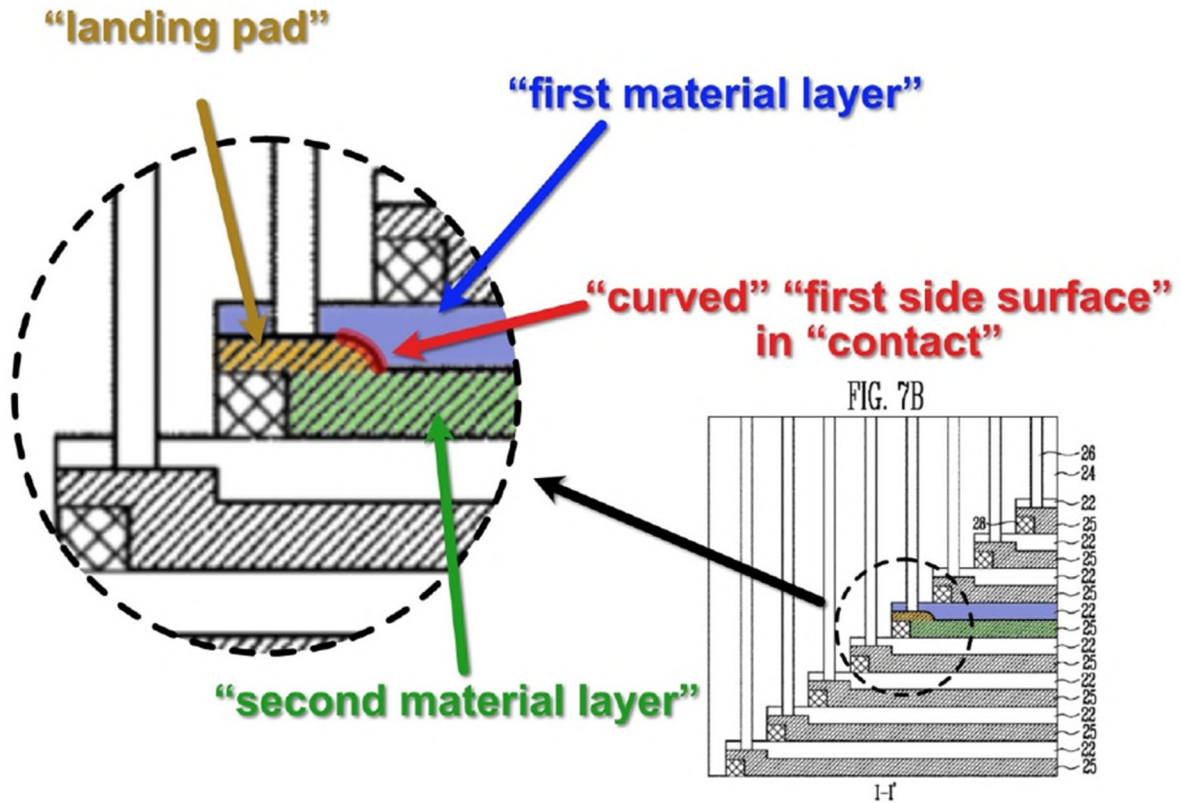
186. Dr. Lee opines that "a POSITA would have recognized that layers in three-dimensional memory devices routinely had thicknesses in the range of approximately 20-90 nm." Ex. 1003 ¶453. Yet he only can provide a single instance which he even purports to include that thickness—Yang. But as I stated above, Yang does not disclose thickness or amount of lateral displacement required by claims 3 and 18 of the '838 patent. Thus, Dr. Lee does not cite any reference with that thickness.

XII. Ground 5: Claim 13-15 Are Not Obvious In View of Lee and Park

187. The Petition and Dr. Lee assert that a POSITA would combine Lee with Park to arrive at claim 13 and also the claims depending on claim 13, namely claims 14-15. Since claims 13-15 depend on claim 12, it is my opinion that a POSITA would not find these claims obvious for the same reasons that I discuss regarding Ground 3.

188. I note that the Petition simply provides the purported result of this combination on Page 83, but does not describe how a POSITA would combine Lee with Park to get there. The Petition cites to Dr. Lee's declaration to provide the missing details. In my opinion, Dr. Lee has made two critical errors in his analysis, which show that combining Lee with Park as the Petition proposes would not lead a POSITA to claim 13's structure, and in fact, would be impossible as proposed.

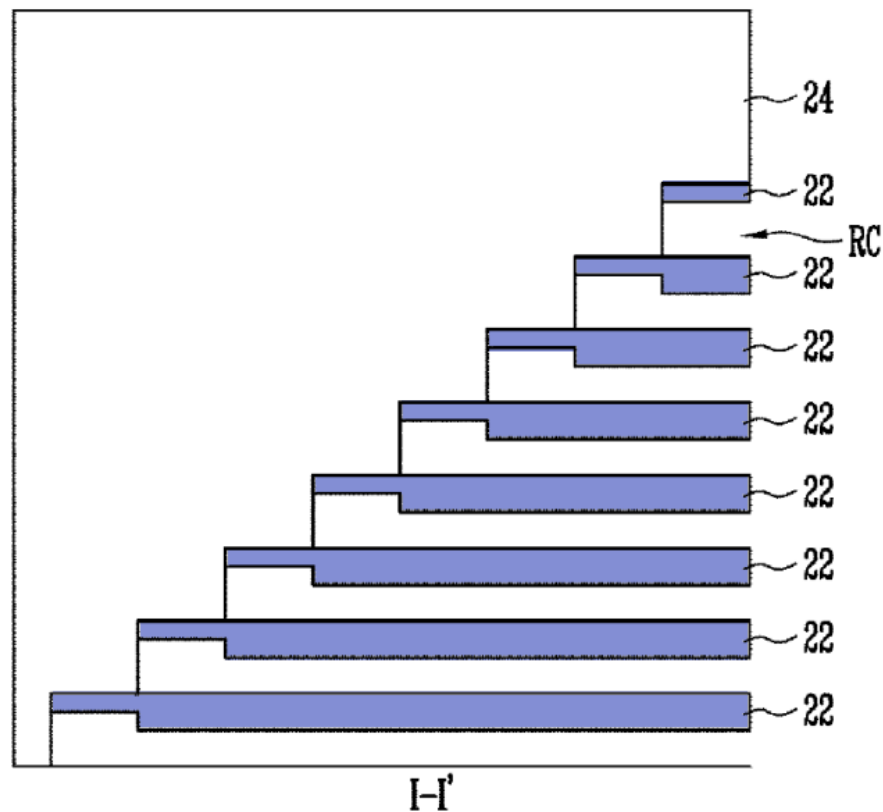
189. The Petition uses the below figure to identify structures in Lee. As the Petition recognizes, where Lee's pad portions PAD contact insulating layer 22, there are "straight sides." Pet. 80. The Petition and Dr. Lee rely on Park's process to get to a purported curved side surface.



Lee Fig. 7B (annotated; modified; concentrated) (cited on Pet. 83).

190. Dr. Lee explains that insulating layer 22 is an “oxide layer.” Ex. 1003 ¶370 (quoting Lee [0030]). Dr. Lee then states that, in the combination, “the process shown in Figures 3B, 4B, and 5B of Lee could still be followed,” resulting “in the same-shaped openings shown in Figure 5B of Lee.” Ex. 1003 ¶472. Below I have reproduced Figure 5B of Lee, with the insulating layers 22 filled in with blue. Thus, according to Dr. Lee, the blue below is solid oxide after following the process in Lee through Figure 5B.

FIG. 5B



191. To get to curved sides, supposedly following Park's teachings, Dr. Lee says, "to achieve a rounded rather than straight sided contact pad, oxidant would be introduced into the openings." Ex. 1003 ¶472. In the above figure, the white portions are the "openings" and the blue portions are oxide insulating layers. By contrast, the oxidation in Park is performed on the "sacrificial layer patterns." Park 12:6-23. In Park, the sacrificial layers are not made of silicon dioxide, instead they are made of "silicon nitride" or "polysilicon," i.e., materials

that can be oxidized. *Id.* 11:67-12:2. In Park's process then, an oxygen gas would be introduced to oxidize the silicon nitride or polysilicon.

192. Dr. Lee confirmed during his deposition regarding the '666 patent that Park's process involved thermally oxidizing silicon nitride or polysilicon using oxygen gas.

Q. The sacrificial layers that are thermally oxidized are made of silicon nitride or polysilicon, correct?

A. The sacrificial layer 62A through 62F or maybe even higher are made of material that can selectively etch relative to silicon dioxide, I think such as silicon nitride or polysilicon. So you're right that the interlayer insulating layer pattern 52A through 52F are made of silicon dioxide whereas the sacrificial layer 62A to 62F are made of either silicon nitride or polysilicon.

Q. In Park, the sacrificial layers are oxidized by applying an oxygen gas to the sacrificial layers?

A. One can do that, yes.

Q. And by applying the oxygen gas to the silicon nitrate in Park, that layer is then oxidized to form silicon dioxide, correct?

A. Yes.

Ex. 2031 248:18-249:17, 250:22-251:8.

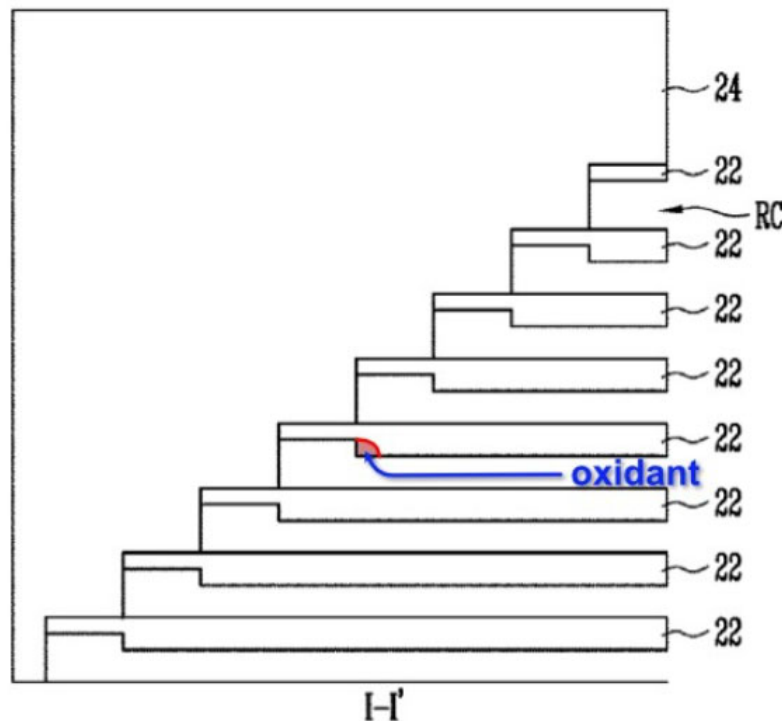
193. In contrast to Park, introducing such an oxidant into the openings of Lee's structure above will not promote further oxidation to the existing oxide layers 22. Any sacrificial layer 21 has already been removed in the relevant region that Dr. Lee annotates in Lee Figure 5B, so nothing remains to be oxidized. *See* Lee [0036]. Nor would introducing an oxidant change the shape of the existing oxide layers 22. It is not possible to further oxidize a stable solid oxide material with oxygen gas as in Park. That is why Park's thermal oxidation process is performed on silicon nitride or polysilicon, which are not oxides to begin with but they can readily be oxidized to form silicon dioxide. *See, e.g.,* Plummer 345-350. A POSITA would understand this and not expect the combination of Lee and Park to achieve any change in shape or any rounding in Lee's Figure 5B. Thus, in my opinion, a POSITA would not have an expectation of success following the Petition and Dr. Lee's proposed combination.

194. Dr. Lee's deposition testimony regarding his testimony on the '666 patent confirms that his opinion is faulty. Dr. Lee's opinion is premised on the idea that there is a "thin oxide" layer that is on top of a pure silicon layer, as then the oxygen gas can diffuse through the oxide layer to form additional silicon oxide with the pure silicon layer. *See* Ex. 2031 267:1-6 ("You react a silicon with oxygen to form SiO₂. And that silicon exist in silicon dioxide and also exist **in the underlying substrate.**"), 261:20-262:3 (Q. "So it's your testimony that

you can oxidize a solid oxide using oxygen gas? A. I do that all the time in my lab. You have a **thin oxide**, you want to grow more, so you expose it to oxygen. And that it will grow oxide. Simple as that.”), 260:11-261:4 (“when you have a thin oxide, let’s say, on top of a silicon substrate, if you want to add more oxide, one way to do that is by exposing it to oxygen so that oxygen will diffuse through the thin oxide and react with silicon underneath the thin oxide and form additional SiO₂”). But as just explained above, no such extra silicon is available in Lee. In Lee Figure 5B, layer 22 is silicon dioxide and there is no adjacent silicon for the oxidant to reach and further oxidize. As Dr. Lee admitted in his deposition regarding the ’838 patent, “Lee doesn’t describe there being any pure silicon in layer 22.” Ex. 2030 125:13-15. As such, the oxygen will find no silicon to oxidize and form the “curved corner” discussed by Dr. Lee in Exhibit 1003 ¶¶471-476.

195. There are further problems with Dr. Lee’s combination. Using the figure below, Dr. Lee says “[t]he exterior corner (red below) would be rounded via oxidation first and most aggressively.” Ex. 1003 ¶473. But where Dr. Lee has drawn this supposed “exterior corner” is inside the solid insulating layer 22.

FIG. 5B



196. To go from the above figure to Dr. Lee's figure under paragraph 477 of his declaration suggests that he is somehow removing part of insulating layer 22, but Dr. Lee never mentions any removal. By contrast, the oxidation process in Park that he is combining with Lee is a growing of an oxide layer. This can be seen in comparing Park's Figure 9A with Park's Figure 9B, the latter of which depicts "additional insulating layer 66 [] formed by oxidizing surfaces and side surfaces of the sacrificial layer patterns 62b through 62f that are externally exposed." Park 12:6-9. As can be seen, layer 66 has been formed on top of the exposed surfaces, it did not eat into and remove any of the sacrificial layers as Dr. Lee appears to be suggesting, though never even explains. In my opinion, a

POSITA would not expect success in trying to form rounding inside a solid oxide structure by introducing an oxidant. While the oxidant may diffuse through the oxide, it cannot react further with a fully formed oxide. *See, e.g.*, Plummer 312-321.

197. Silicon dioxide (SiO_2) is the most stable oxide of silicon and cannot be further oxidized under ordinary chemical conditions. This stability can be rationalized in terms of electronic structure, the octet rule, and thermodynamics.

198. At the atomic level, silicon in SiO_2 adopts a formal oxidation state of +4. Each silicon atom is tetrahedrally coordinated by four oxygen atoms, with each Si–O bond representing a polar covalent interaction. This bonding arrangement satisfies the **octet rule**: silicon contributes its four valence electrons ($3s^2 3p^2$), which are shared with oxygen atoms, while each oxygen atom (which requires two additional electrons to complete its octet) achieves a stable electronic configuration by forming two Si–O bonds. Zumdahl (Ex. 2029) 98-139 (discussion on octet rule). The extended three-dimensional network of SiO_4 tetrahedra in quartz or amorphous SiO_2 ensures that every atom in the lattice is electronically saturated. Plummer 290-296.

199. Because the octet rule is satisfied for both silicon (+4, $1s^2 2s^2 2p^6 3s^2 3p^6$ noble-gas configuration) and oxygen (–2, with a filled valence shell), there are no low-energy pathways for additional oxidation. Attempting to

“oxidize” further would require pushing silicon beyond the +4 oxidation state, which is chemically inaccessible: silicon lacks available low-lying orbitals to form stable bonds in a higher oxidation state. Silicon cannot exceed +4 because the energetics of removing additional electrons from the filled neon-like core are prohibitive. Zumdahl 99-139 (discussion on octet rule).

200. Thermodynamically, SiO_2 represents the global minimum in Gibbs free energy for silicon–oxygen compounds at standard conditions. Intermediate oxides such as SiO or suboxides (Si_2O_3 , SiO_x with $0 < x < 2$) are metastable and readily disproportionate or oxidize to SiO_2 . Chen 1-10. However, there is no higher oxide “ SiO_3 ” or “ SiO_4 ” that is stable under ambient conditions, because these would require silicon in formal oxidation states of +6 or +8, which are not accessible for main group elements in the third period without invoking hypervalent bonding schemes that are neither observed experimentally nor supported by quantum chemical calculations.

201. Thus, once silicon is fully oxidized to SiO_2 , the octet rule and fundamental energetic considerations forbid any further oxidation. In fact, SiO_2 is often used as a chemically inert passivation layer in microelectronics precisely because of this stability. Plummer 287-290.

202. In his deposition regarding the '838 patent, Dr. Lee argued that layer 22 in Lee Figure 5, is a “non-stoichiometric silicon oxide layer.” Ex. 2030

129:6-10. But I see no basis for this statement. While a “[s]ilicon dioxide film deposited using LPCVD or APCVD at low temperatures ... can be nonstoichiometric and ... often porous” (Plummer 564), such a film would never be used as a critical insulating layer in a 3D NAND device like Lee due to its inferior insulating properties and stability. Notably, Lee never suggests or mentions such an approach. In other words, a POSITA would understand Lee does not include nonstoichiometric silicon oxide as the critical insulator layer between word lines (layer 22) because of (1) the inferior dielectric properties of nonstoichiometric oxide (2) the unstable nature and higher reactivity of nonstoichiometric silicon oxide and (3) the lack of any suggestion of using such a unusual approach. Such use of non-stoichiometric oxide would render 3D NAND structures non-operational.

203. Stoichiometric silicon dioxide (SiO_2) is used in CMOS based devices primarily because of its density, purity, thermal stability, chemical inertness, and superior dielectric properties. Plummer 563. While non-stoichiometric silicon oxide, also known as silicon sub-oxide (SiO_x where $x < 2$), is used in some niche roles (e.g., sacrificial oxides, for stress engineering, in memristor, etc.), it is generally undesirable as a dielectric for a functional device or structural film in CMOS, because its properties are significantly inferior—and often unpredictable—relative to stoichiometric SiO_2 .

204. Non-stoichiometric SiO_x ($x < 2$) contains a high density of defects and traps, such as oxygen vacancies, sub-oxide species (Si^+ , Si^{2+} , Si^{3+}) and weak Si-O networks. Chen 1-10; Barranco 1-8. These defects can allow for charge trapping and/or electron hopping that affects the layer's insulating properties. Silicon oxide has a bandgap that can drop from ~ 9 eV for the stoichiometric SiO_2 to 4 eV for the non-stoichiometric $\text{SiO}_{1.3}$, and to even lower value for extremely oxygen deficient oxide ($x < 1$). Barranco 5-9. Such a reduction in bandgap can lead to orders-of-magnitude higher tunneling current leakage for the same oxide thickness. Further, the presence of Si-Si bonds and oxygen vacancies can affect dielectric strength and breakdown characteristics. These deficiencies render non-stoichiometric oxide unsuitable for structural dielectric use in NAND memories.

205. Non-stoichiometric SiO_x is chemically and structurally unstable. It can readily absorb oxygen from ambient or oxidize at elevated temperature during subsequent processing, which changes its thickness, refractive index, density, stress, and other properties. Chen 1-10. When deposited, sub-oxide can form at variable composition spatially with inconsistent physical and chemical properties, unacceptable for high-volume manufacturing (where variability of $< 1\%$ is required). *Id.*

206. There are additional problems in using non-stoichiometric SiO_x layers in conventional CMOS relating to their lower density, that allows rapid

moisture diffusion, and poor thermal stability during thermal annealing. Chen 1-

10. In addition, non-stoichiometric SiO_x exhibits very different etch rates and unpredictable etch selectivity vs. Si, SiN, SiO_2 , which pose integration issues (patterning, spacer formation, isolation).

207. In summary, good and stable electrical isolation between word lines in 3D NAND is critical, and cannot be met by the inferior insulating and structural properties of silicon sub-oxide. A POSITA would avoid using non-stoichiometric silicon oxide layers between word lines.

208. Thus, in my opinion, a POSITA would not combine Lee with Park in the manner proposed by the Petition and Dr. Lee, as a POSITA would have no expectation of success in arriving at a curved side surface.

XIII. Conclusion

All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true. Further, I am aware that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001. I declare under penalty of perjury that the foregoing is true and correct.

Executed on November 25, 2025, in Pasadena, CA.

A handwritten signature in blue ink, appearing to read 'Konstantinos P. Giapis', written over a horizontal line.

Konstantinos Giapis