

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

Case No. PGR2025-00021
U.S. Patent No. 12,010,838

REPLY DECLARATION OF DR. JACK C. LEE

I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron” or “Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to reply to certain of the positions set forth in Patent Owner’s Response (Paper 28) and opinions in a November 26, 2025 declaration of Konstantinos Giapis (Ex. 2019) submitted by Patent Owner in an *inter partes* review proceeding relating to U.S. Patent No. 12,010,838, which I refer to herein as the ’838 patent.

3. I am being compensated at my current standard consulting rate, plus reimbursement for any reasonable expenses. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

4. The prior declaration I submitted in connection with this proceeding, which I understand has been designated as Ex. 1003, sets forth among other topics my educational background and professional experience (Ex. 1003, ¶¶ 5-13 and

associated Exhibit 1004), my understanding of the law (*id.*, ¶¶ 18-33), an overview of pertinent technical background (*id.*, ¶¶ 39-61), an overview of the '838 patent and its prosecution history (*id.*, ¶¶ 62-86), the knowledge and characteristics of a person having ordinary skill in the art (*id.*, ¶¶ 34-38), and my opinion that the '838 patent's claim terms are already readily understandable and can be afforded their plain and ordinary meaning (*id.*, ¶¶ 87-90).

5. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, my work with those of ordinary skill at the time of the alleged invention, and my general experience in the field of art.

6. I have also reviewed and considered the materials listed in my prior declaration (*id.*, ¶ 17), the Board's Institution Decision (Paper 19), Patent Owner's Response (Paper 22), the transcript of my deposition in this proceeding (Ex. 2030) and IPR2025-00189 (Ex. 2031), the Giapis Declaration (Ex. 2019), and the following materials to the extent relevant to my opinions:

Exhibit	Description
1076	Transcript of the February 11, 2026 Deposition of Konstantinos Giapis in PGR2025-00021
1077	Excerpt from <u>Merriam-Webster Dictionary</u> (1998)
1079	Transcript of the November 12, 2025 Deposition of Konstantinos Giapis in IPR2025-00189

1080	Falcony, <u>Characterization of Excess Si in Nonstoichiometric SiO₂ Films by Optical and Surface Analysis Techniques</u> , J. Electrochem. So., Vol 144, No. 1, 379-383 (Jan 1997)
1081	Bedjaoui et al., <u>Si nanocrystal-containing SiO_x (x<2) produced by thermal annealing of PECVD realized thin films</u> , Materials Science and Engineering B 124-125, 508-512 (2005)
1082	U.S. Patent No. 9,728,547 to Ohsaki et al.
2020	U.S. Patent No. 9,005,884 B2 (“884 Patent”)
2021	U.S. Patent No. 11,145,666 B2 (“666 Patent”)
2022	Excerpt of File History of U.S. Patent Application No. 16/126,956
2023	Counterpoint Tech. Mkt. Rsch., Scaling to 1,000-Layer 3D NAND in the AI Era (July 2024) (“Counterpoint”)
2024	3D FLASH MEMORIES (Roni Micheloni ed. 2016) (“Micheloni”) (excerpt)
2025	EFY Bureau, <u>At 20nm, Chips Have Features Sized Ten Times Smaller Than the Wavelength of Laser Used in Lithography</u> , electronicsforu.com (Dec. 4, 2014)
2026	Press Release, ASML, <u>ASML Extends ArF Leadership</u> (Dec. 6, 2006)
2027	ASML, <u>Light and Lasers</u> (Nov. 17, 2025)
2028	James D. Plummer et al., SILICON VLSI TECHNOLOGY: FUNDAMENTALS, PRACTICE AND MODELING (Prentice Hall Elecs. & VLSI Series) (Charles Sodini ed. 2000) (excerpts)
2029	Steven S. Zumdahl et al., CHEMISTRY: AN ATOMS FIRST APPROACH (3d ed. 2021) (excerpt)
2032-2040	Exhibits 1-9 from my IPR2025-00189 deposition
2041	U.S. Patent Application Publication No. 2018/0301460 A1 (“Yoo”)
2042	A.E.T. Kuiper et al., <u>Oxidation Behaviour of LPCVD Silicon Oxynitride Films</u> , 33/34 Applied Surface Sci. 757 (1988) (“Kuiper”)
2043	Yen-Po Lin & Jenn-Gwo Hwu, <u>Quality Improvement in LPCVD Silicon Nitrides by Anodic and Rapid Thermal Oxidations</u> , 7 Electrochemical Solid-State Letters G87 (2004) (“Lin”)

2044	X.Y. Chen et al., <u>Annealing and Oxidation of Silicon Oxide Films Prepared by Plasma-Enhanced Chemical Vapor Deposition</u> , 97 J. Applied Physics 014913 (2005) (“Chen”)
2045	A. Barranco et al., <u>Electronic State Characterization of SiO_x Thin Films Prepared by Evaporation</u> , 97 J. Applied Physics 113714 (2005) (“Barranco”)

7. The paragraphs below respond to certain of the arguments and assertions made by Patent Owner and Dr. Giapis in this proceeding. In these paragraphs, I address only a fraction of the opinions and assertions Dr. Giapis set forth in his declaration. The fact that I do not respond to any particular opinion expressed by Dr. Giapis should not be considered should not be interpreted as agreement, acceptance, or concession of any kind.

II. KIM GROUNDS

A. Kim Teaches the Claimed “Portion[s]”

8. According to Dr. Giapis, Kim purportedly lacks the claimed “second portion” and “first portion” of a “second material layer.” *See, e.g.*, Ex. 2019, ¶¶ 98-109.

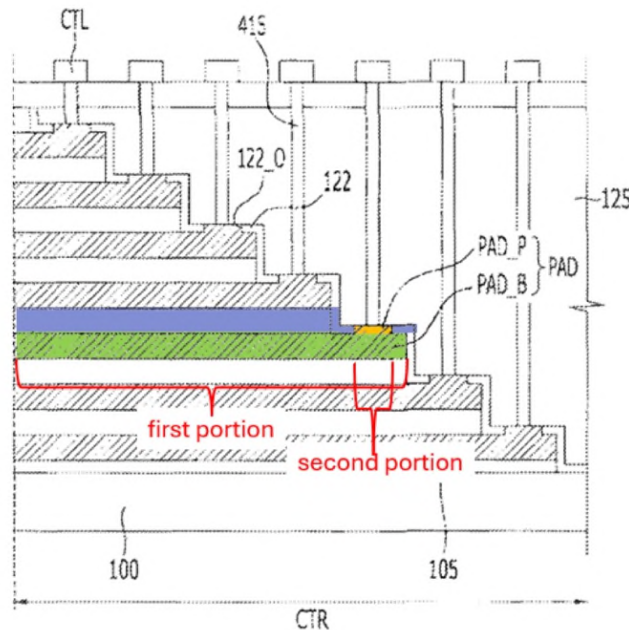
9. In support of this, Dr. Giapis proposes—and then relies on—a narrow construction of these claim terms. In particular, Dr. Giapis proposes the following constructions:

Claim Term	Dr. Giapis Construction
“wherein the first material layer is disposed over a first portion of the second material layer”	“wherein the first material layer is disposed over a first portion of the second material layer but not a second portion of the second material layer ”
“a landing pad disposed over the second portion of the second material layer”	“a landing pad disposed over the second portion of the second material but not the first portion of the second material layer ”

Id., ¶ 48 (with red annotations added).

10. As shown by the red annotations (which I added), Dr. Giapis essentially just repeats the claim language, but then grafts on an additional negative limitation. These negative limitations prohibit any “first material layer” from being over the “second portion” of the “second material layer,” or any “landing pad” from being over the “first portion” of the “second material layer.”

11. According to Dr. Giapis, both the Petition and my original declaration somehow “arbitrarily” labeled Kim’s “first portion” and “second portion.” *Id.*, ¶¶ 107-108. Dr. Giapis then goes on to apply his specific, narrow construction of the claim term and identify what he believes the “first portion” and “second portion” of Kim’s conductive layers to be. This is shown below:



Id., ¶ 107. Dr. Giapis then concludes that this cannot satisfy the claims, because “Kim’s ‘first portion’ and the ‘second portion’ of the second material layer overlap.” *Id.* Indeed, Dr. Giapis goes so far to argue that the ’838 patent’s claims somehow exclude all “island shaped” landing pads. *Id.*, ¶ 108.

12. I disagree with Dr. Giapis’s opinion for multiple reasons. First, Dr. Giapis relies on an erroneous claim construction. A POSITA would not understand the claims to be limited in the manner he proposes. Second, Dr. Giapis contradicts and ignores Kim’s own identification and labeling of the different parts of its conductive layers (these Kim identified parts are the “portions” I identified in my original declaration). Third, Dr. Giapis also ignores that Kim’s landing pad is also implemented as a “step.” Such a pad satisfies even his narrow interpretation of the claims. I will address each of these opinions below.

1. Dr. Giapis Misconstrues the Claims

13. As I explained in my opening declaration, the '838 patent's claim terms do not require further construction and can instead be afforded their plain and ordinary meaning. *See* Ex. 1003, ¶ 90. This includes the claim terms including the phrases “first portion” and “second portion.” These terms are readily understandable and do not require additional construction. The claims would most certainly not be understood to mean what Dr. Giapis says they mean.

14. Beginning with the claim language, claim 1 (and similar claim 12) merely refer to a “second material layer” (a conductive layer) that ***has*** “a first portion” and “a second portion.” *See* '838 patent, claims 1, 12.

15. The term “portion” has a straightforward plain and ordinary meaning to a POSITA: it refers to a “part” of a larger whole. *E.g.*, Ex. 1077, 406 (defining “portion” as “a part of a whole”). So, the claim here simply requires a “second material layer” that has a “first” part and a “second” part. Nothing about the claims requires these parts to have any specific structure or dimension, other than that they are distinguishable parts of the same conductive layer as understood by a POSITA.

16. Consistent with this well-understood plain and ordinary meaning of the word “portion,” the '838 patent itself repeatedly uses the term “portion” to refer to a part of a larger whole. *E.g.*, '838 patent, 5:40-43 (discussing both “an upper portion” and “lower portion” of a “staircase”), 5:66-6:1 (referencing “a portion of a

top surface of a layer”); *see also* 4:39-40, 7:15-17, 8:20-33, 8:34-65, 11:60-64, 12:38-59.

17. The patent never uses “portion” to require specific, definite dimensions or layout. It does not define the terms “first portion” and “second portion” in the narrow, specific way Dr. Giapis proposes.

18. Next, there is no other claim language that would require the narrowing limitations Dr. Giapis seeks to impose.

19. Claim 1 (and claim 12) do state that the “landing pad” is “disposed over” the “second portion” and the “first material layer” is “disposed over” the “second portion.” ’838 patent, claims 1, 12.

20. A POSITA would not, however, consider this language to be a re-definition of the term “portion.” Instead, it functions to specify where the “landing pad” and “first material layer” are: they are over “portions” of the same “second material layer.”

21. Next, Dr. Giapis’s construction effectively grafts the word “only” onto the claims. Claims 1 and 12 do not use this word in connection with the “first portion” and “second portion.” Instead, claims 1 and 12 provide that (1) the “first material layer” be “disposed over” the “first portion” and (2) the “landing pad” be “disposed over” the “second portion.” Dr. Giapis’s construction improperly imports

a negative limitation (“only”) that appears nowhere in the claim language and is inconsistent with the open-ended nature of the claims.

22. The claims do not say that the “first material layer” is “only” over the “first portion” and nowhere else, or that the “first material layer” is the “only” structure over the “first portion.” Likewise, the claims do not say that the “landing pad” is “only” over the “second portion” and nowhere else, or that the “landing pad” is the “only” structure over the “second portion.”

23. Instead, the claim is open to other structure besides the “first material layer” being over the “first portion.” It is also open to other structure besides the “landing pad” being over the “second portion.” And the claim allows the “first material layer” and “landing pad” to be present in locations other than the “first portion” and “second portion,” so long as they are at least “disposed over” the “first portion” and “second portion” as the claims require. Dr. Giapis does not recognize this, leading him to impose limitations on the claims without justification or support in the claim language itself.

24. The specification also does not require a narrow construction. Dr. Giapis walks through several the ’838 patent’s figures in an effort to argue that the claims must be interpreted narrowly. Ex. 2019, ¶¶ 50, 55 (discussing Fig. 8), 53 (discussing Fig. 5), 54 (discussing Fig. 7).

25. The specification explicitly notes, however, that these figures are not meant to be limiting. For instance, according to the patent, “specific configurations and arrangements are discussed ... for illustrative purposes only.” ’838 patent, 3:36-37. Further, the patent states that it is meant to embrace not only what is shown in the figures, but also “adaptations and modifications” of depicted embodiments, confirming that the figures do not limit claim scope. *Id.*, 13:14-22.

26. Dr. Giapis also opines that the claims must be limited because “the manufacturing process described in the ’838 patent can only result in ‘a first portion of a second material layer’ that is separate and distinct from the ‘second portion.’” Ex. 2019, ¶ 55.

27. As an initial matter, this statement is incorrect as a matter of claim logic. Because the “first portion” and “second portion” of the “second material layer” are different parts of a larger whole, they are always “separate and distinct.” As I explain below, Kim does in fact include “separate and distinct” portions: the PAD_B and the rest of its gate electrode 300. It is only Dr. Giapis’s odd and arbitrary labeling of Kim’s figures that creates an overlap.

28. Next, the fact that the ’838 patent discusses an example manufacturing method would not be understood by a POSITA to limit the claims. The patent itself says this, explaining that “any suitable deposition methods” may be used to form the various layers making up its memory. ’838 patent, 6:53-65.

29. Dr. Giapis also discusses the '838 patent's prosecution history. Ex. 2019, ¶¶ 60-61. Here he includes a number of annotated figures from prior art where he purports to identify a “first portion” and “second portion” of a “second material layer.”

30. I have also reviewed the '838 patent prosecution history. Neither the Examiner nor the applicant discussed the meaning of either “first portion” or “second portion.” *See generally* Ex. 1002.

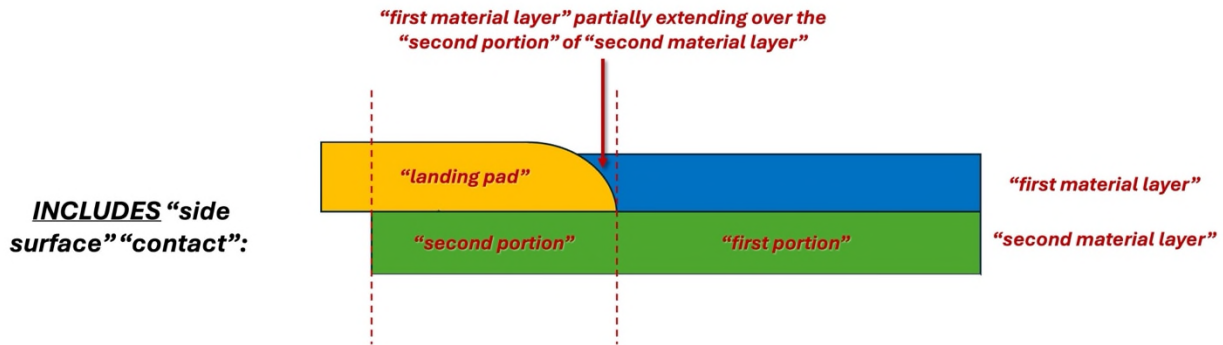
31. Further, none of the labeled, annotated figures Dr. Giapis includes in his declaration appear in the prosecution history. Those simply reflect his opinion now. They are not the applicant's (or the Examiner's) views of the prior art or claims while the '838 patent was pending. This makes the figures—and everything Dr. Giapis now says about them—entirely irrelevant to the meaning of “first portion” and “second portion.”

32. While Dr. Giapis does not state this in his declaration, Patent Owner concedes in its response that the prosecution history “suggests neither an expansion nor disavowal of claim scope....” Response, 9. I agree that there is nothing in the prosecution history that would lead a POSITA to conclude that the claims have anything other than their plain and ordinary meaning.

33. Not only does it lack support in the intrinsic record, but Dr. Giapis’s construction—if adopted—would read out the ’838 patent’s only embodiment. I understand that a claim construction that has this effect is rarely correct.

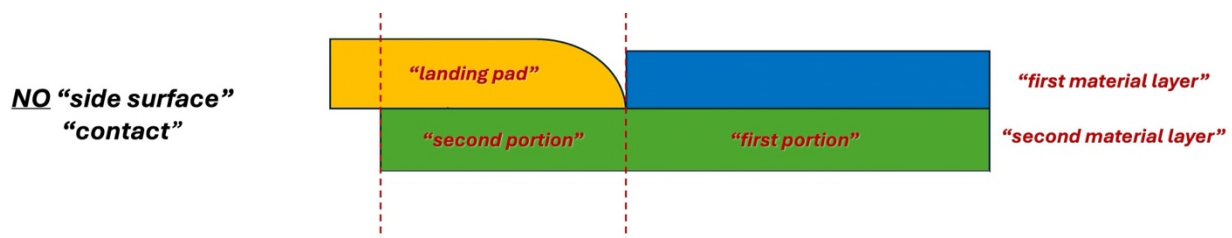
34. Dr. Giapis explains that Figure 8—this is the only figure in the ’838 patent that depicts only figure showing a complete staircase structure—depicts “landing pads” with a “curved side surface” that is “in contact” with an adjacent “first material layer.” Ex. 2019, ¶ 32.

35. In order for there to be contact with this type of curved “side surface,” the “first material layer” must necessarily extend at least partially over the “second portion” of the “second material layer.” Otherwise, the claimed contact cannot occur. This is shown below, with the portion of the “first material layer” extending over the “second portion” to contact that “landing pad[’s]” curved side surface indicated. The below figure is based on what appears to be shown in Figure 8 of the ’838 patent (although the figure’s resolution is too poor to determine definitively what is shown). The blue “first material layer” includes both insulating layer 502 and whatever other insulation exists between the end of layer 502 and the landing pad 820 (such as dielectric layer 825).



36. Identification of the “first material layer” in the manner depicted above is, in my opinion, not only necessary to satisfy the claims, but it is consistent with patent’s definition of “layer.” According to the ’838 patent, a “layer” includes the material between “any set of horizontal planes.” ’838 patent, 4:38-51. Here this is all the insulation above the plane formed by the top of a one “second material layer” and below the plane formed by the bottom of another, higher located “second material layer.”

37. If the “first material layer” did not extend over the “second portion” and includes only the material as shown in the figure below (i.e., just insulating layer 502 in Figure 8 and not all the material between the planes formed by adjacent “second material” or conductive layers), there would be no contact between the first material layer and the “curved side surface” of the landing pad:



38. Because Dr. Giapis’s definition prohibits any of the “first material layer” from being present over the “second portion,” Patent Owner effectively reads Figure 8 out of the claims. Either there is no “contact” between the “first material layer” and the curved surface of the “landing pad,” or there is “contact” but the “first material layer” extends over the “second portion.” There is, however, no embodiment in the ’838 patent where (1) there is “contact” between the curved surface of a “landing pad” and the “first material layer” and, at the same time, (2) the “first material layer” does not extend over the “second portion.”

2. Kim Teaches What the Claims Require When Properly Construed

39. When claims 1 and 12 are properly interpreted in accordance with the plain and ordinary meanings of their terms, the claims require only that the “first portion” and “second portion” be parts of a larger conductive layer.

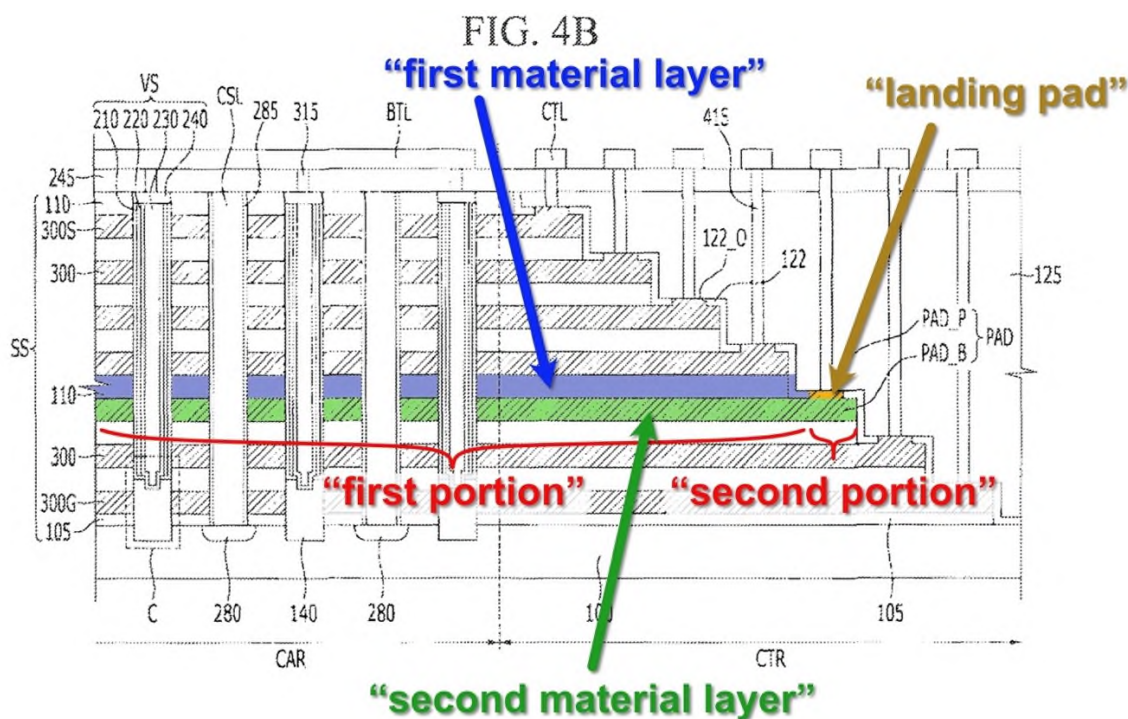
40. Kim includes such a structure: each of its “gate electrode[s] 300” includes a “PAD_B” at its “end.” Kim, 7:58-67.

41. In fact, Kim explicitly characterizes this “PAD_B” as a “part of the gate electrode” that is “exposed” for form a step and extends “into the contact region CTR.” *Id.* (emphasis added).

42. So, consistent with Kim itself, I identified what Kim characterizes as a “part” of its conductive layer—the “PAD_B”—as the claimed “second portion.” *See*

Ex. 1003, ¶¶ 168-175. Dr. Giapis did not do so. Instead, he completely ignores Kim's teaching that its PAD_B is "part" of a larger conductive layer.

43. Moreover, Kim's "PAD_P" (its "landing pad") is over the "PAD_B," while its dielectric layers 110 and 122 (its "first material layer") are over the rest of the gate electrode 300 of which the "PAD_B" is part. Because of this, just as the claims require, Kim teaches a memory with a "second material layer" (gate electrode 300). A "landing pad" (PAD_P) is over a "second portion" (PAD_B) of this layer, and a "first material layer" (dielectric layers 110 and 122) is over a "first portion" (the rest of gate electrode 300 minus the PAD_B) of the same layer. This is shown in the annotated figure below:



Kim, Fig. 4B (annotated).

44. Next, I disagree with Dr. Giapis that my application of the plain and ordinary meaning of the terms “first portion” and “second portion” somehow renders the terms “meaningless.” Ex. 2019, ¶ 52.

45. Again, Kim’s “first portion” and “second portion” are separate and distinct: PAD_B is the end part of gate electrode 300 that is exposed to form a step. See Petition, 27-31. It is only Dr. Giapis’s interpretation—which ignores Kim’s teaching that each conductive layer includes a PAD_B at its end and reads limits into the claims—that produces this result.

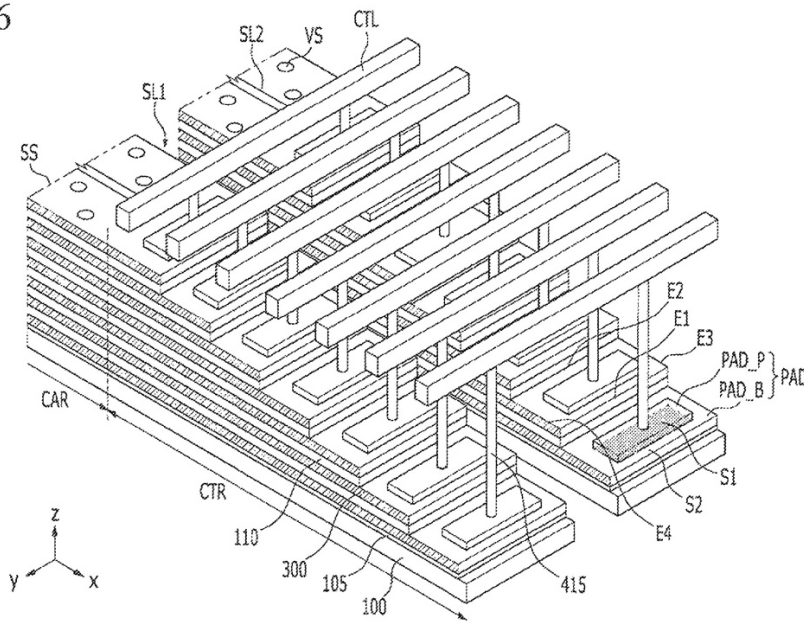
3. Kim Satisfies the Claims Even When Patent Owner’s Narrow Understanding of the Claims Is Applied

46. Finally, even assuming that Dr. Giapis’s narrow interpretation is correct, and the claims are determined to exclude memories with “island” landing pads where the “first material layer” extends over and around the landing pad, Kim would still render the claims obvious.

47. As I explained in my opening declaration (Ex. 1003, ¶ 180), Kim teaches that its landing pads can have an “island shape” or be a “step with respect to the surface of the base pad.” Kim, 8:23-28.

48. When the landing pad is formed as a step, the “first material layer” will not extend around the pad. Instead, it will end and be interrupted by the step as shown in blue below:

FIG. 6



Id., Figs. 5, 6. *see also* Fig. 5. In Figure 5, the landing pad is “inside from the edges E1 and E2” but “coplanar” or “aligned” “with the edges E3 and E4” of the staircase structure. *Id.*, 8:35-65. This results in a discontinuity in the insulating layer: it stops at the pad. In Figure 6, however, Kim’s landing pad is “inside and spaced apart from the four edges E1, E2, E3, and E4” of the staircase structure. *See* Kim, 10:19-29 Because the stepped landing pad structure shown in Figure 5 (and referenced as one of Kim’s pad designs in my opening declaration) includes an insulating layer that stops at the pad, the “first material layer” is in fact only over the “first portion” of the “second material layer.” It is not also over the “second portion.”

B. Kim Teaches a Landing Pad With a “Curved Side Surface”

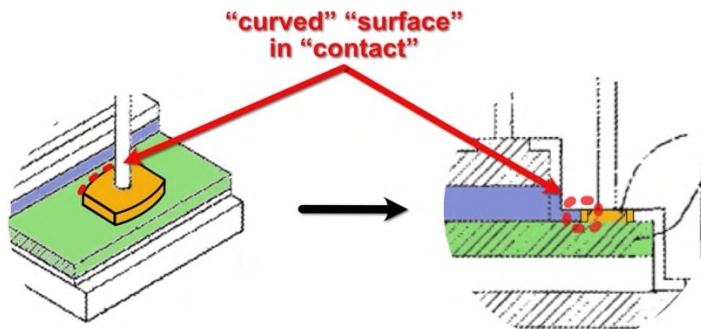
50. Dr. Giapis next argues that Kim lacks “curved side surface” required by claim 13-15 of the ’838 patent. *See* Ex. 2023, ¶¶ 40-61.

51. In my prior declaration, I explained that Kim teaches at least two different types of landing pads with the claimed type of “curved side surface.” See Ex. 1003, ¶¶ 223-266.

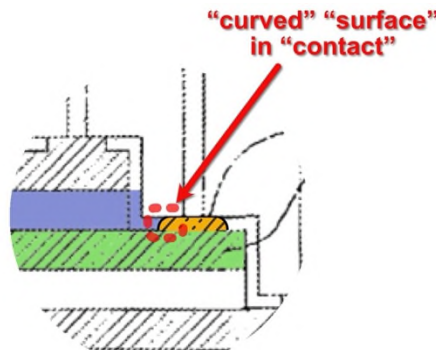
52. In particular, while not explicitly shown in any figure, Kim explains that its “protrusion pad PAD_P is not limited thereto and ... may have a shape including a curved surface based on a virtual rectangular parallel[] shape, a cylindrical shape, or any shape.” Kim, 8:29-34.

53. I also explained that a POSITA would have understood this to be referring to pads that are, among other things, (1) generally cylindrical and curved when viewed from above and (2) curved when viewed in cross section as shown below:

**Generally cylindrical
pad:**



**Pad curved in cross
section:**

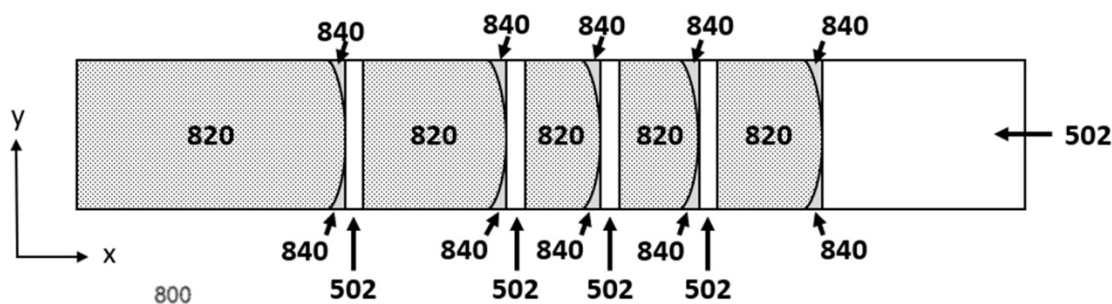


See Ex. 1003, ¶¶ 223-266.

54. I then concluded that even though “curved” pads are not shown in Kim’s figures, a POSITA would nonetheless have considered use of such a pad with Kim to be obvious (both because such pad designs are known and have well known benefits, and because Kim itself contemplates their use with its memory).

55. Dr. Giapis disputes Kim’s teachings (and my opinions) in this regard. He argues (1) that generally cylindrical pads are not covered by the claims (*e.g.*, Ex. 2019, ¶ 97), (2) that pads curved in cross section are not achievable in Kim (*e.g.*, *id.*, ¶ 114), and (3) that a POSITA would not have been motivated to employ a “curved” pad (*e.g.*, *id.*, ¶¶ 123-147).

56. Before addressing these points, I note that Kim’s “curved” pads are formable as either an “island” or a “step” as Kim itself discloses. See Kim, 8:23-28. A pad curved in cross-section would simply extend to the edges E3 and E4 of the staircase structure, thus forming a step. A generally cylindrical pad would be formed in the manner shown in Dr. Giapis’s declaration at paragraph 83:



Ex. 2019, ¶ 83 (top view of pads with a generally cylindrical “curved side surface”).

1. Dr. Giapis Misconstrues the “Curved Side Surface”

57. Dr. Giapis’s opinions regarding Kim’s generally cylindrical landing pads are premised on an erroneous claim construction. Dr. Giapis does not apply the plain and ordinary meaning of “curved side surface” in his declaration. Instead, he reads narrowing limitations into the term that depart significantly from that plain and ordinary meaning.

58. Again, it is my opinion that none of the ’838 patent’s claim terms require construction: they are all readily understandable. This includes the term “curved side surface.” The term “curved side surface” would be understood to simply refer to a surface that is curved, i.e., deviating from a planar surface, without limitation to a particular axis or orientation, i.e., there is no requirement that the curve be in the vertical z-axis direction, perpendicular to a substrate surface, or the like. Any curved surface qualifies.

59. According to Dr. Giapis, the claimed “curved side surface” must be “a vertical surface curved along a direction (e.g., the z-axis) perpendicular to the top surface of the structure.” Ex. 2019, ¶ 63.

60. This understanding of “curved side surface” departs from the plain and ordinary meaning of the term and finds no support in claims, specification, or prosecution history.

61. In particular, claim 13 requires only a landing pad with “a curved side surface.” The claim does not use the words “vertical,” “z-axis,” or “perpendicular.” Those limitations are read into the claim by Dr. Giapis. He points to nothing in the claims that requires this specific (and not some other) type of “curved” surface.

62. The specification of the ’838 patent also does not require the narrowing limitations Dr. Giapis seeks to impose.

63. The ’838 patent defines the term “horizontal” (“nominally parallel to a lateral surface of a substrate”) and “vertical” (“nominally perpendicular to the lateral surface of a substrate”). ’838 patent, 5:6-16. It also uses terms such as “perpendicular” and “z-axis.” *Id.*, 5:59-61. Terms like these plainly could have been included in claim 13 to further characterize and limit the “curved side surface.” The fact that this type of language is missing—despite the fact that the applicant went to the trouble to include it in the specification—would strongly indicate to a POSITA that the claims are not limited in the way Dr. Giapis argues.

64. Dr. Giapis also states that “Figure 8 is the only embodiment of the claimed ‘curved side surface’” in the ’838 patent. Ex. 2019, ¶ 76. Thus, he argues that the claims must be limited to the type of curved surface purportedly shown in this figure.

65. Similarly, Dr. Giapis also takes the position that “[t]he methods of manufacturing taught by the ’838 patent form a curved side surface that is a ‘vertical

surface curved along a direction (e.g., the z-axis) perpendicular to the top surface of the structure.” *Id.*, ¶ 79. Per Dr. Giapis, “there is no process described in the ’838 patent for curving the surfaces of the landing pads in connection with the insulating layers in the x-y plane.” *Id.*, ¶ 80

66. In my opinion, there are numerous problems with these opinions.

67. First, the ’838 patent includes no views of its memory device in the x-y plane. Thus, it is not possible to state—as Dr. Giapis does—that the patent lacks a “curved side surface” in this plane. The patent does not say one way or the other.

68. Moreover, as I have already noted, the patent repeatedly explains that it is not to be limited to the specific structure shown in its figures. ’838 patent, 2:66-3:4 (figures are just meant to “illustrate”); 3:35-43 (“other configurations and arrangements” contemplated, patent “can also be employed in a variety of other applications”); 13:14-28 (embodiments meant to “modif[ied] and/or adapt[ed]”).

69. Second, it is not true that the “methods of manufacturing” set forth in the ’838 patent produce only a surface that is curved along the z-axis.

70. Dr. Giapis references the ’838 patent’s figures (which he believes show a “curved side surface”) and the specification’s discussion of “poor step coverage” to conclude that a POSITA would have “select[ed] and optimize[d] specific gas-phase deposition techniques capable of supplying both directional and isotropic fluxes of depositing molecules to the staircase structure, such as plasma-enhanced

CVD and directional sputter deposition (PVD) among others.” Ex. 2019, ¶ 36. By “carefully balanc[ing]” these “two flux components,” a “surface curvature in the vertical direction” is supposedly produced. *Id.*

71. As an initial matter, claim 13 is directed to the resulting apparatus, not to any particular manufacturing recipe, and a POSITA would understand that the claimed “curved side surface” limitation describes the structure of the conductive layer, not a specific way of depositing or etching films to achieve that structure.

72. Next, the ’838 patent also says nothing even like what Dr. Giapis says it does. It does not use the word “curved.” It does not discuss “flux components.” It does not mention “directional” or “isotropic fluxes.”

73. Further, the patent does not even limit itself to techniques “such as plasma-enhanced CVD and directional sputter deposition (PVD).” Instead, it states that its layers can be formed using other techniques, such as “low pressure CVD (LPCVD)” and “atomic layer deposition (ALD)” along with “any suitable deposition techniques or combinations thereof.” ’838 patent, 9:7-12; *see also id.*, 2:41-47.

74. Deposition techniques like LPCVD and ALD—by themselves—typically will not produce a vertically curved landing pad side surface like that shown in the ’838 patent’s figures. These techniques can, however, produce landing pads that are curved in the x-y plane (using an appropriate shaped mask during deposition). Moreover, “poor step coverage” is a descriptive term for non-conformal

thickness distribution and does not impose any particular direction of curvature. A POSITA would understand that non-conformal deposition can produce curvature in different directions depending on feature geometry, shadowing, and mask shape, rather than only in the z-direction.

75. This is reflected in Plummer textbook (Ex. 2008) that Dr. Giapis cites. In particular, Plummer explains that “CVD has historically been used in the integrated circuit industry mainly for silicon and dielectric deposition, primarily due to its good quality films and good step coverage[.]” Ex. 2028, 511. And LPCVD deposition processes in particular are designed such that “equal fluxes of reactant gases ... reach every location in order to achieve uniform depositions.” *Id.*, 525. Thus, use of a LPCVD process will produce good step coverage (and no curve in the z-axis direction), not poor step coverage. ALD similarly produces conformal step coverage and also will not produce a curve in the z-axis direction. Both methods, however, can produce a curve in the y-axis direction. This, in my view, further confirms that the claims cannot be properly limited to just “curved side surfaces” that curve in the z-axis direction. Instead, the claims also embrace surfaces that curve in other directions, including the y-axis direction.

76. Because the claims embrace “curved side surfaces” that are curved in the y-axis direction, Kim’s generally cylindrical contact pads do in fact satisfy the claims.

2. Pads Curved When Viewed from the Side Can be Employed with Kim

77. According to Dr. Giapis, the second type of pad I mentioned in my declaration—one curved when viewed from the side—“cannot be formed” using the manufacturing process that Kim expressly discloses. *E.g.*, Ex. 2019, ¶ 136. Dr. Giapis does not dispute that this type of pad includes a “curved side surface” as claimed.

78. As I noted in my original declaration, pads that are curved when viewed from the side are disclosed in numerous prior art references, including Park (Ex. 1009), Nam (Ex. 1022), and Yun (Ex. 1021). For example, Park teaches rounding through an additional oxidation step, Nam teaches rounding through post-implantation heat-induced spreading, and Yun teaches similar curved pad geometries. *See* Ex. 1003, ¶¶ 226-240.

79. Not only do these references provide examples of memories that employ landing pads with curved side surfaces when viewed in cross-section, but they explain how such a pad can be manufactured. Each of these references teaches a practical, well-established technique for producing rounded or curved pads.

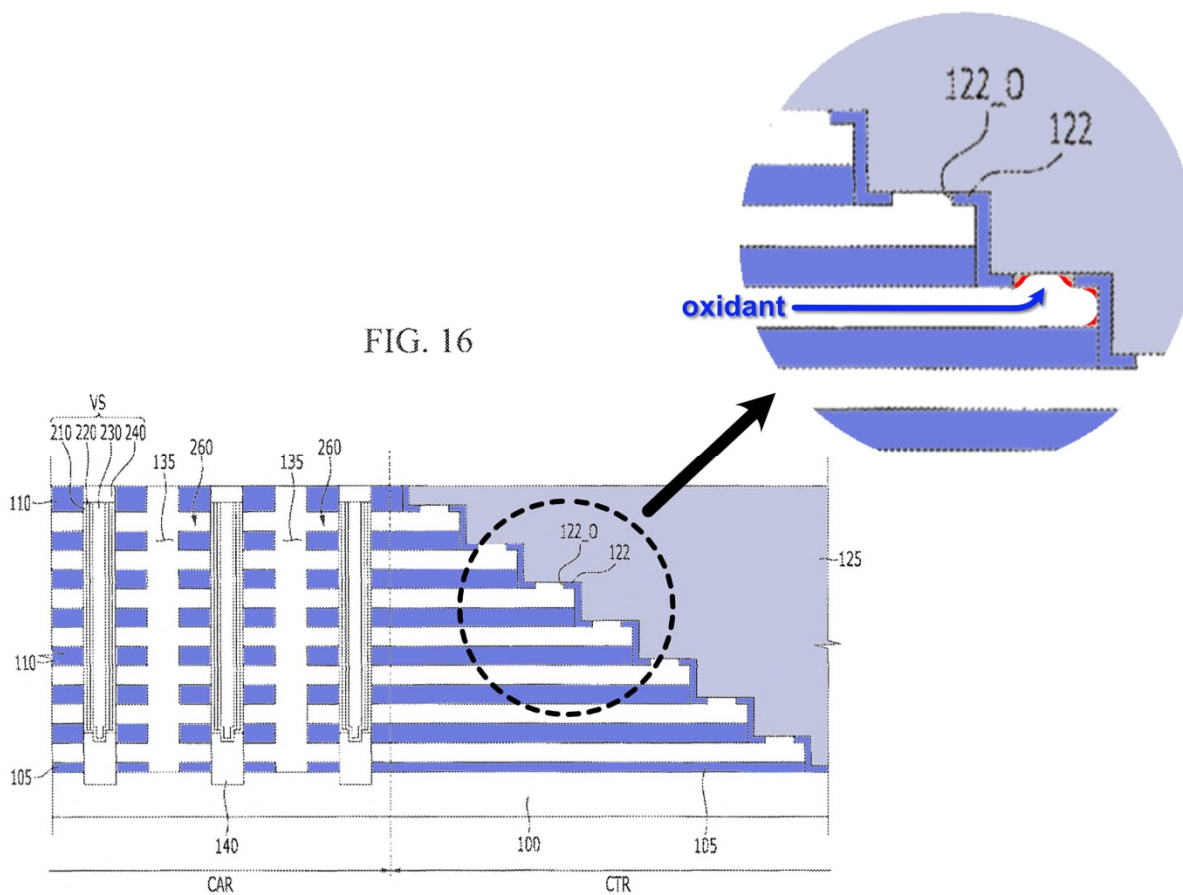
80. As I previously noted, a POSITA would have recognized that these pad manufacturing methods are readily applicable to Kim. *See id.*, ¶¶ 251-260.

81. For example, Park teaches that a rounded pad can be achieved by performing an additional “oxidation” step during the pad formation process. See Park, 7:17-29, 8:33-49.

82. A POSITA would have understood that Kim is readily modifiable to produce rounded landing pads (with curved side surfaces) following this same approach, because Park’s oxidation-induced rounding process is additive, occurs preferentially at exposed corners, and can be incorporated into Kim’s sequence without altering Kim’s overall architecture or fabrication objectives.

83. In particular, after Kim’s sacrificial layers are removed (along with the area 122_I where ion implantation occurred), an oxidant would be introduced into the space between the remaining oxide layers (shown in blue below). This oxidant would further oxidize excess silicon present in the oxide layer resulting in the formation of additional silicon oxide (shown in red below).

84. Further oxidation would occur and silicon oxide would form preferentially in the corners and exposed edges of the oxide layers:



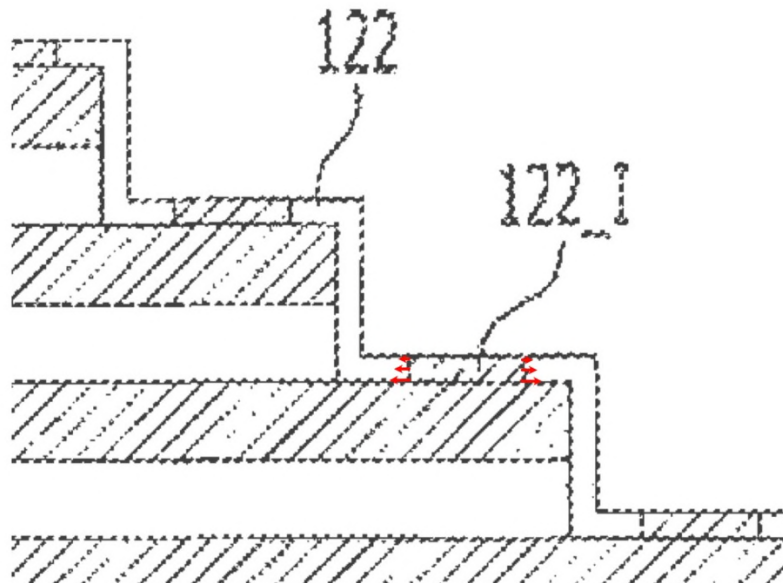
85. As I discuss below in connection with the Lee reference, a POSITA would have recognized (and considered it obvious) to achieve rounding by further oxidizing an existing oxide layer like that taught by Kim. Dr. Giapis's opinion to the contrary is incorrect and unsupported.

86. Alternatively, a POSITA would have considered it obvious to employ Nam's process to obtain landing pads with curved side surfaces in Kim.

87. As I explained in my opening declaration, Kim already shapes its contact pad by performing ion implantation on the areas 122_I of its insulating layer 122. See Ex. 1003, ¶¶ 252-256. To achieve a rounded contact pad, all that is required

is a minor adaptation or tailoring of this ion implantation step via an additional heating step. As Nam explains, application of heat after ion implantation causes the damaged region to spread, resulting in curved contact pad. See Nam, ¶ [0060] (after ion implantation, “[t]he impurity doped” in the target areas, including the “interlayer insulating layers[,]” “may be spread due to heat applied thereto in a subsequent process”).

88. An example of this is shown below. Application of heat will cause the impurities implanted in Kim’s insulating layer 122 in area 122_I to spread, resulting in a damaged region with a rounded shape (and curved side surfaces). The spread is indicated with small red arrows. This in turn will produce a rounded landing pad like that depicted in Nam:



Kim, Fig. 13 (excerpted and annotated).

89. Dr. Giapis argues that the processes used by references like Park and Nam are “fundamentally different” from that in Kim. *E.g.*, Ex. 2019, ¶ 128. This is not the case.

90. Kim, Park, and Nam all teach 3D memory structures. *See* Kim, Fig. 3, 1:28-30; Park, Fig. 1, 1:12-22; Nam, Fig. 2, ¶ [0003]. They all also reference various types of curved landing pads. Kim, 8:29-34; Park, 8:37-42; Nam, ¶¶ [0066], [0077]. And they all employ ion implantation during the formation of these pads. *See* Kim, 13:1-11; Park, 7:17-29; Nam, ¶¶ [0066], [0098]-[0107].

91. Park and Nam are thus not “fundamentally different” from Kim. Instead, all that is required to generate a rounded landing pad using Kim’s existing process is (1) an extra oxidation step (when Park’s rounding approach is employed) or (2) an extra heating step (when Nam’s rounding approach is employed). This is simple, straightforward design work that is well within the capabilities of a POSITA. A POSITA also would have fully expected either approach to succeed when applied to Kim (as both approaches were demonstrated to successfully produce rounded landing pads in both Park and Nam). In practice, semiconductor engineers routinely adapt individual process steps—such as oxidation steps that promote rounding, or post-implant anneals that promote diffusion—from one flow to another, and a POSITA would not view differences in overall device layout as a reason to ignore well-understood rounding techniques taught in Park and Nam.

92. In sum, Dr. Giapis’s opinion appears to require the bodily grafting of Park and Nam into Kim, as opposed to the straightforward and obvious adaptation of Kim that a POSITA would have performed following the teachings of the prior art.

93. Dr. Giapis also takes the position that use of Nam’s pad rounding method “would negate some of Kim’s advantages.” Ex. 2019, ¶ 146. According to Dr. Giapis, increasing the pad size via a heating step would bring them closer to adjoining conductive structure and be contrary to Kim’s purported instruction to “precisely control[] the location” of its landing pads. *Id.* I disagree with both points.

94. Kim explains both that its pads can have different widths (Kim, 11:57-12:7) and different shapes (*id.*, 8:29-34). A POSITA would have understood that a rounded contact pad that is slightly wider than a square or rectangular pad is one of the shapes Kim contemplates for use. Moreover, a rounded pad would have provided two clear benefits: (1) the bottom of the pad would be wider, thus producing a more extensive thicker area for purposes of preventing contact punch-through during manufacture while (2) the top of the pad would be narrower, which would increase the distance between the pads and adjacent conductive structures.

95. Next, Kim does not use the word “precise,” or state anywhere that its pad formation process is intended to produce “precisely” shaped pads. Again, as I

note immediately above, Kim is open to various different pad shapes and sizes (including pad shapes that vary from step-to-step).

3. A POSITA Would Have Been Motivated to Use “Curved” Landing Pads with Kim

96. Dr. Giapis also takes the position that a POSITA would not have been motivated to employ a rounded pad with Kim because “Kim already has numerous features that address and solve” the “short-circuit problem.” Ex. 2019, ¶ 124. This is also wrong.

97. To address the potential short circuit problem between conductive structures in its memory, Kim adjusts the size, shape, and positioning of its pads. *See* Kim, 9:46-49 (noting that Kim’s pad can be sized and located “inside from the edge surface” of the base pad “to prevent ... short-circuit”). It also adds thickened layers of insulation around the pad. *See id.*, 9:50-55 (“auxiliary insulating layer 122” is “positioned between ... adjacent protrusion pads”), 9:7-11 (insulation “thickness” is increased to “prevent[] ... short circuit”).

98. A POSITA would have recognized that rounded landing pad (with curved side surfaces) operates to increase the distance between the landing pad and adjacent conductive structure.

99. A rounded landing also—because it is further away—increases the thickness of insulation surrounding the landing pad.

100. In other words, a POSITA would have recognized that a rounded landing pad not only furthers Kim's goal to avoid short circuits, but does so in a way that is both consistent with Kim and amounts to nothing more than an extension of the short-circuit preventing approaches Kim already employs. This is why a POSITA would have been motivated to employ a rounded pad with Kim: it assists in solving a problem Kim identifies (potential short circuits) and does so in a way Kim itself identifies as a potential solution (increasing distance and insulation between conductive structures). Even if Dr. Giapis's narrow view were adopted and the "curved side surface" had to be curved only in the z-direction (which I do not agree with), claim 13 would still be obvious. Park's oxidation and Nam's annealing both create vertical curvature at exposed corners, and a POSITA would expect the same result when applied to Kim's pads. Thus, even under Patent Owner's construction, the prior art still yields a pad with a curved side surface in contact with the insulating layer, as claim 13 requires.

C. Kim and Yang Render Claims 3 and 8 Obvious

101. Claims 3 and 8 require that the claimed "landing pad" be offset from the side of the underlying "second material layer" by 10-300 nm. '838 patent, claims 3, 8.

102. As I explained in my prior declaration (Ex. 1003, ¶¶ 298-335), Yang (Ex. 1007) provides an example of typical, routinely used 3D memory staircase dimensions.

103. As I noted (*id.*, ¶ 333), when the '838 patent was filed, 3D memory staircases typically had steps that were a few hundred nanometers long. This is exactly what Yang teaches: its steps are from 400-600nm. *See, e.g.*, Yang, 7:23-28. Typical landing pads were in the range of about 200nm. Given these typical landing pad and step sizes, the claimed range here embraces almost all possible landing pad positionings on typical 3D memory steps. In fact, the only way to fall outside the claimed range would be to form the landing pad unusually small (as a percentage of the step size) and locate it as far as possible from the step edge, or form it very large (again as a percentage of the step size) and locate it right up against the step edge. Neither of these types of pads are taught by either Kim or Yang. Instead, both references teach typically sized pads that are approximately centered on the memory's steps. *See, e.g.*, Kim, Fig. 4B; Yang, Fig. 2.

104. Dr. Giapis does not appear to dispute these opinions. Instead, he appears to limit himself to Yang.

105. Here, he argues that Yang purportedly “does not disclose the contact pad width.” Ex. 2019, ¶ 151.

106. In arriving at this conclusion, Dr. Giapis both appears to misread Yang and misunderstand my opinion.

107. First, Dr. Giapis improperly focuses on what is shown in Yang's figures. I did not rely exclusively on Yang's figures alone in my declaration. Instead, I relied on the figures along with Yang's textual description of the dimensions it employs in its specification. As I described in my original declaration, Yang provides numerous dimensions, including: (1) the overall dimension of each depicted staircase step (400-600nm), (2) the thickness of each layer (~50nm), (3) the thickness of its pads (~80nm), (4) the type and specification of the laser employed to form its landing pads, and (5) how much larger its pads are than the associated contact openings (20-40nm). *See* Ex. 1003, ¶¶ 308-317. It is this description in Yang and Yang's figures together that would have led a POSITA to conclude that the prior art teaches landing pad offsets falling within the claimed range.

108. Second, Dr. Giapis wrongly argues that in the prior art, "the pad" is not obviously "located in the middle of the stair." Ex. 2019, ¶ 158. I did not simply "assum[e]" without support that this is how the memories of the prior art would be formed. I did not have to make this assumption because the art plainly teaches memories with landing pads that are approximately centered. Both Kim and Yang unambiguously depict pads located approximately in the center of each step. *See*,

e.g., Kim, Fig. 4B; Yang, Fig. 2. In fact, Kim itself states that its landing pad is intended to be situated in the “center” of the underlying PAD_B. Kim, 10:40-48.

109. Third, Dr. Giapis takes issue with my opinion that a POSITA would have considered it obvious to form a landing pad that is approximately 200 nm wide because Yang teaches use of a 193 nm-ArF excimer laser. Ex. 2019, ¶¶ 153-155. Here, Dr. Giapis explains that this type of laser can “print features both far larger and smaller than” its “wavelength.” *Id.*, ¶ 154. This is inconsistent with Yang, misses the point, and misunderstands my opinion.

110. Yang does not teach landing pads that are “far larger and smaller” than 200nm. In Yang, the landing pads have a “width ECDs.” Yang, 8:7-10; Fig. 2. Yang explains that this “width ECDs” is double the “thickness T3” of insulation layer 112 that is deposited during manufacture. *Id.* Yang also explains that “thickness T3” “must be greater than the thickness of the” pairs of conductive and insulating layers. *Id.*, 8:12-13. Since these layers can be up to 100nm thick (*id.*, 6:24-28), Yang’s landing pad will be on the order of 200nm wide.

111. This also makes practical sense. Yang explains that its landing pads are 20-40nm larger than its contact openings. If the landing pads were only 20nm wide (the purported minimum size identified by Dr. Giapis), then the contact openings would be non-existent. Yang, of course, teaches contact openings with actual dimension. *See, e.g.*, Yang, Fig. 2. Further, if the landing pads were multiple times

larger than 200nm (as Dr. Giapis also appears to argue), they would occupy the entirety of Yang's step. This is also not what Yang teaches: its pads are smaller than its steps. *Id.* This—coupled with the dimensions Yang provides—leads to the conclusion that Yang employs an approximately 200nm pad that is offset from the edge of the underlying conductive layer by the amount described in my original declaration.

112. I also note that Dr. Giapis does not dispute that Yang's laser would be able to form a pad that is approximately 200 nm wide. So, not only is this the size landing pad a POSITA would consider Yang to teach, but it is readily achievable using the tools that Yang discloses.

113. Finally, in my opinion Dr. Giapis's contention that Kim's and Yang's "processes are incompatible" (Ex. 2019, ¶ 164) misses the point.

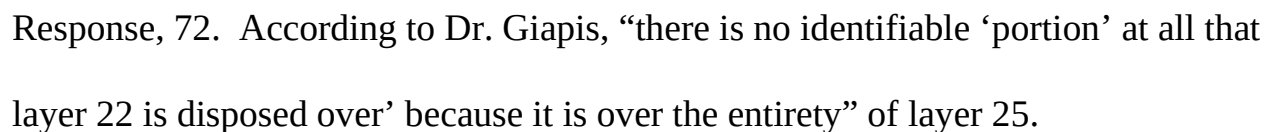
114. I did not propose that Kim be modified to employ Yang's manufacturing process. I cited Yang simply because its staircase is shaped similarly to Kim's and because it provides an example of typical memory staircase dimensions.

III. LEE GROUNDS

A. Lee Teaches the Claimed "Portions"

115. My original declaration explained in detail why Lee renders the '838 patent's claims obvious. *See* Ex. 1003, ¶¶ 386-429.

117. Patent Owner characterizes Lee as follows:



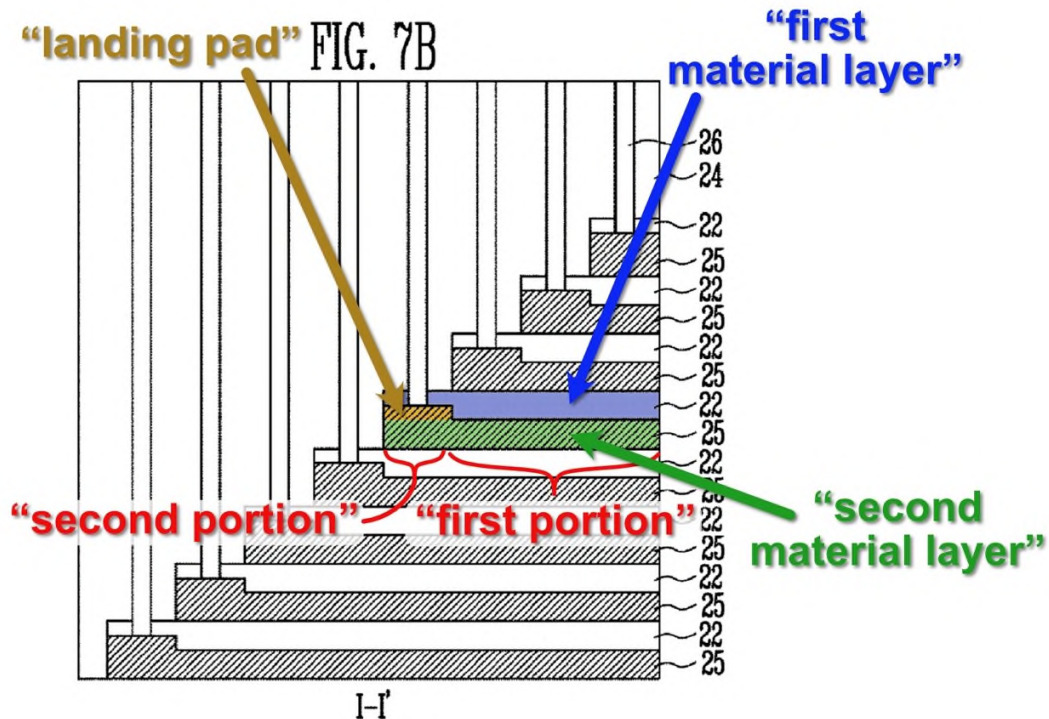
119. First, the '838 patent does not define the terms “first portion” and “second portion” in the same, narrow way Patent Owner and Dr. Giapis do. See *supra* Section II.A.1. The claims also do not exclude structure where the “first

material layer” extends over the “second portion.” Moreover, if the claims were interpreted this way, they would improperly exclude the ’838 patent’s only embodiment.

120. Second, both Patent Owner and Dr. Giapis ignore Lee’s disclosure. They also ignore that the “portions” of Lee’s “second material layer” identified in my prior declaration are the same as those in the ’838 patent.

121. According to Lee, each of its “conductive layers 11” includes a “pad portion[] PAD” at its “end.” Lee, [0023]. This is what I identified as the “second portion” in Lee: the very same structure that Lee itself characterizes as a “portion.” The rest of the conductive layer excluding this “end” “portion” is the “first portion” of the “second material layer. Rather than following Lee, Patent Owner and Dr. Giapis ignore Lee and come up with their own, completely different “first portion” and “second portion.”

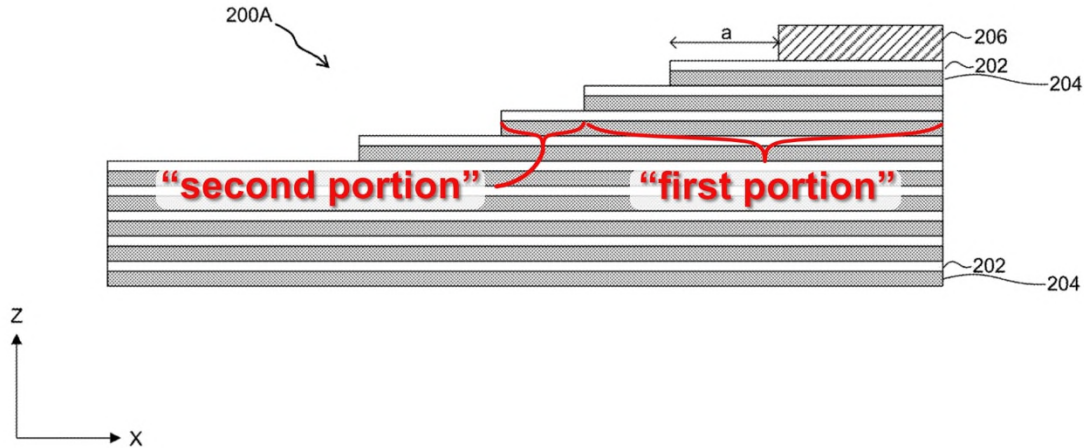
122. Next, Lee’s “second portion” corresponds to the part of a conductive layer forming a staircase step. This is shown below:



Lee, Fig. 7A (annotated).

123. The '838 patent uses the term "portion" to refer to the very same structure. In the '838 patent, each "step" in a memory's staircase structure "exposes a portion of a top of a surface of an SC layer." '838 patent, 7:10-12 (emphasis added); *see also id.*, 5:66-6:1 ("[a] step of the staircase structure exposes a portion of a top surface of a layer stack..."). The "SC layer" is later replaced with conductive material to become the "second material layer." *Id.*, 10:19-24.

124. In other words, in the '838 patent, the "second portion" is simply the part of the "second material layer" corresponding to a step. The "first portion" is the other part of the "second material" that does not correspond to a step:



Id., Fig. 2A (annotated). I identified the same type of “first portion” and “second portion”: the “second portion” is the part of Lee’s conductive layers corresponding to a step, while the “first portion” is the rest of the conductive layer that is not a step. In contrast, Dr. Giapis manufactured his own characterization of Lee that diverges not only from Lee, but also how the ’838 patent itself uses the term “portion.”

B. Lee and Park Render “Curved” Landing Pads Obvious

125. My original declaration also explained why the claims 13-15 would have been obvious over the combination of Lee and Park. *See* Ex. 1003, ¶¶ 457-499.

126. Here, Dr. Giapis argues that a POSITA would have been unable “to achieve any change in shape or any rounding in Lee’s” landing pads because “[i]t is not possible to further oxidize a stable solid oxide material with oxygen gas as in Park.” Ex. 2019, ¶ 193. Dr. Giapis goes on to assert that Lee’s “silicon dioxide” layer includes “no ... extra silicon” that can be oxidized. *Id.*, ¶ 194.

127. To begin, Lee explains that its insulation layers are formed from “oxide” (see Lee, ¶ [0030]), not “stable solid oxide material” like “silicon dioxide” as Dr. Giapis appears to assume.

128. As a technical matter, the assertion that formation of a silicon oxide layer prevents further oxidation is incorrect. Oxidation of silicon-containing materials is governed by well-established diffusion-controlled kinetics, in which oxidant species diffuse through an already-formed SiO₂ layer and react at the underlying silicon or silicon-containing interface, such that oxide thickness continues to increase as diffusion and reaction proceed, rather than terminating once an oxide layer forms.

129. As explained in standard semiconductor processing texts, including Plummer et al., thermal oxidation proceeds by transport of oxidizing species through the existing oxide, with reaction occurring at the silicon or silicon-containing interface, not by direct exposure of bare silicon to oxygen. See Plummer (Ex. 2028) at pp. 329–359, explaining that oxide growth continues as oxygen diffuses through previously formed oxide and reacts at the interface.

130. Accordingly, the presence of an oxide layer does not act as a barrier that halts further oxidation, but rather forms the medium through which continued oxidation occurs, with oxide thickness increasing as diffusion and reaction proceed.

131. Next, a silicon oxide layer can (and often does) include extra silicon such that it is able to be further oxidized when exposed to an oxidant.

132. For example, when the '838 patent was filed, silicon oxide films with non-stoichiometric amounts of oxygen (*i.e.*, SiO_x , where $0 < x < 2$) were both known and in routine use.

133. This is discussed in numerous references. For example, the Plummer text cited by Dr. Giapis explains that CVD “deposited films of silicon dioxide” used in “microelectronic structures” as “dielectric layers to electrically separate conductive regions” “can be nonstoichiometric.” Ex. 2028, 563-64.

134. Another article notes that CVD—a deposition method routinely used when forming insulating layers in memory devices—can be employed to form “stoichiometric SiO_2 to an oxide with about 14 a/o of Si in excess” *See, e.g.*, Ex. 1080, 379.

135. Yet another reference explains that “substoichiometric SiO_x ($0 < x < 2$) thin films” can also be formed using other methods, such as PECVD. Ex. 1081, 508.

136. Indeed, the prior art even specifically discloses the use of non-stoichiometric silicon oxides as insulating layers in 3D memory. U.S. Patent No. 9,728,547 to Osaki et al. (Ex. 1082) provides an example. Osaki explains that it “relates generally to the field of three-dimensional memory devices.” *Id.*, 1:9-10. Like all such devices, Osaki’s memory includes alternating “insulating layers 32”

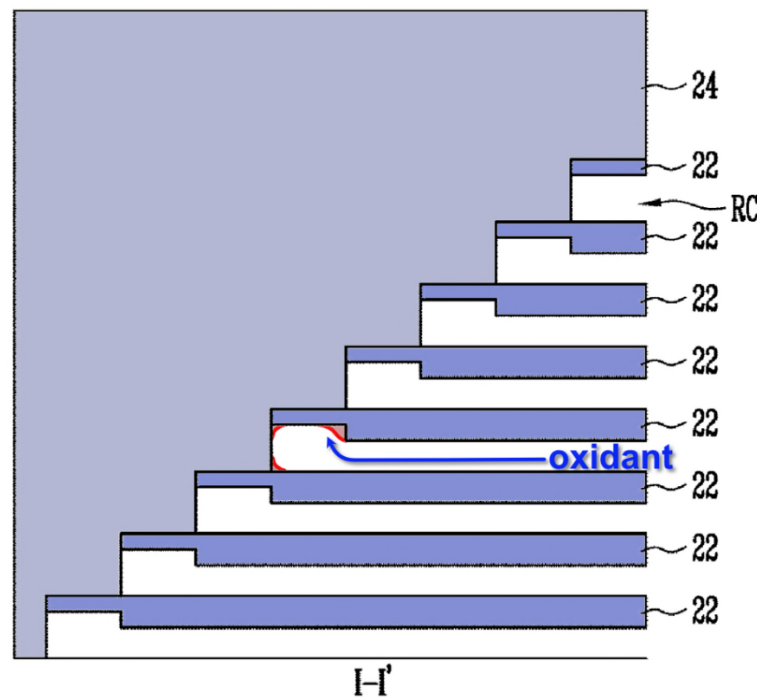
and “gate dielectric layer[s] 12” arranged in a stack on a substrate. *Id.*, 7:25-29. Osaki explains that “each insulating layer 32 can be an insulating material layer” formed from, for instance, “silicon oxide...” *Id.*, 8:4-16. Per Osaki, the term “silicon oxide” includes “silicon dioxide as well as non-stoichiometric silicon oxides having more or less than two oxygen atoms for each silicon atom[.]” *Id.*, 6:45-51.

137. This type of nonstoichiometric silicon oxide film will include more than one atom of silicon for every two atoms of oxygen. Because of this, the film includes excess silicon and will be further oxidized when it is exposed to an oxidant. I explained how this type of further oxidation occurs during one of my prior depositions. Ex. 2031, 261:20-266:1. In such a film, the excess silicon atoms act as readily available reaction sites, so when oxygen is introduced, these silicon atoms can oxidize to form additional Si–O bonds, leading to further oxide growth.

138. As I noted in my original declaration—and during deposition—when a silicon oxide layer is further oxidized, additional silicon oxide forms preferentially in the areas of exposed, exterior corners. *See* Ex. 1003, ¶¶ 473-474; Ex. 2031, 267:7-268:22. This includes the corners within the spaces between Lee’s existing oxide layers 22 as illustrated in Fig. 5B below (with the original corners indicated in blue). By “exterior corner,” I did not mean above Lee’s staircase structure. This was a reference to corners that are exposed within the spaces previously occupied by Lee’s sacrificial layers. Further oxide growth—and rounding—will occur in the regions

shown in red in Fig. 5B, with the largest amount of oxidation occurring in the rightmost area (as there are two adjacent corners there). This is an additive process. Additional silicon oxide will form on top of the original silicon oxide. The process will continue either until all excess silicon is consumed, or the oxidant is removed. Because the nonstoichiometric film contains silicon atoms that are not fully bonded to oxygen, these under-coordinated silicon atoms preferentially react first, with oxide growth initiating and accelerating at the exposed corner sites.

FIG. 5B



139. Dr. Giapis's testimony regarding "nonstoichiometric" silicon oxides is inaccurate, technically unsupported, and is contradicted by the very textbook on

which he relies in an effort to show how a POSITA would have understood the '666 patent (along with other published articles that make the same point).

140. According to Dr. Giapis, nonstoichiometric silicon oxide is “structurally unstable” and “contains a high density of defects.” Ex. 2019, ¶ 204-205. He also states that the material “allows rapid moisture diffusion, and pore thermal stability during thermal annealing.” *Id.*, ¶ 206. He next notes that “non-stoichiometric SiO_x exhibits very different etch rates and unpredictable etch selectivity...” *Id.*

141. None of the references he cites, however, say anything remotely like this. His opinions are baseless, and unsupported.

142. Nonstoichiometric silicon oxide is repeatedly referenced in the prior art as a material that is routinely generated using standard procedures, and is usable as memory dielectric layers. *See, e.g.*, Ex. 2028, 563-64. The material will only be “structurally unstable” and have the purported “defects” and other issues Dr. Giapis references if it exhibits an extreme oxygen deficiency (*i.e.*, SiO_x, where x is closer to 0 than 2).

143. Nonstoichiometric silicon oxide, as that term is used in the semiconductor processing literature, refers to an oxide network in which there is excess silicon (oxygen deficiency) relative to the ideal SiO₂ ratio, resulting in silicon–silicon bonds and oxygen vacancies within the silicon–oxygen lattice, not

substitution of oxygen with another element. As Plummer explains, oxidant species can diffuse through SiO_2 at elevated temperatures and oxidation proceeds preferentially at corners and stress-concentrated regions (Ex. 2028, 329-359), so a POSITA would understand that oxygen can continue to react in oxygen-deficient regions or at exposed geometric discontinuities in a nonstoichiometric oxide film, resulting in additional oxide growth and local rounding even when an SiO_2 film is already present.

144. It results from the presence of extra silicon atoms (creating oxygen vacancies) within the silicon-oxygen crystalline lattice.

145. An example of this is shown in the Plummer text below. Note the extra silicon atom that is not surrounded by oxygen atoms. A nonstoichiometric silicon oxide will have many instances of such silicon atoms within its crystalline lattice (some present via silicon-silicon bonds, and some present via a silicon-oxygen bond but missing a second such bond to oxygen):

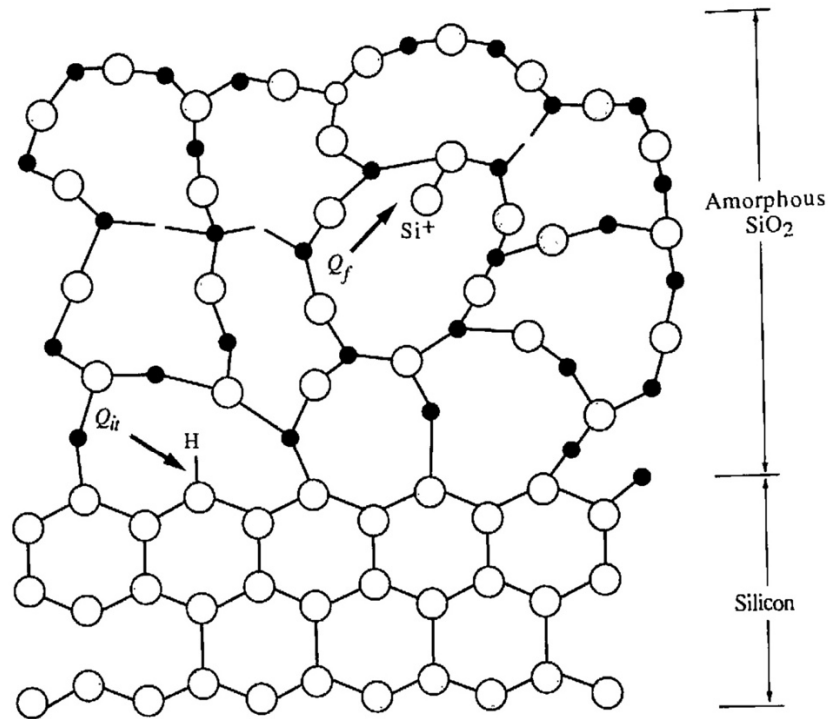


Figure 6-39 Conceptual atomic level picture of the Si/SiO₂ interface showing possible structural origins of Q_f and Q_{it} . Q_f corresponds to the excess Si⁺ atom; Q_{it} is shown as an incompletely bonded Si atom near the interface, passivated in this example with an H bond. The larger circles correspond to Si atoms; the smaller circles to O atoms.

Ex. 2028, 354.

146. A non-stoichiometric silicon oxide film (particularly one where x in SiO _{x} is closer to 1 than 2) will include many such extra silicon atoms. Again, such a material is not inherently “defective.” Indeed, it would be highly unusual for a perfectly stoichiometric silicon oxide to be produced using standard, known manufacturing techniques.

147. Not only is such a material known and readily achievable, but a POSITA would have immediately recognized that it would have been desirable to further oxidize the non-stoichiometric film to reduce the amount of extra silicon.

This would not only produce a rounded landing pad but would allow the material's uniformity to improve.

C. Lee and Haller Render Claims 3 and 8 Obvious

148. Ground 4 explained why Lee and Haller render claims 3 and 8 obvious. *See* Ex. 1003, ¶¶ 430-456.

149. Here, Dr. Giapis argues that Haller is inapplicable because “Lee’s barrier layer” purportedly cannot be formed “as thick as” Haller’s spacer. Ex. 2019, ¶ 181.

150. According to Dr. Giapis, “only the first few nanometers of the silicon nitride” barrier layer Lee employs “may oxidize” supposedly preventing formation of a thick barrier layer. *Id.* Here, Dr. Giapis posits that once a “thin layer of SiO₂ forms on the nitride surface,” it will act as “a barrier to further oxygen diffusion” preventing further oxide formation. *Id.*

151. No such thing occurs. Silicon oxide does not operate as a “barrier to further oxygen diffusion.” If it did, it would be impossible to grow an oxide of any material thickness on the surface of a silicon substrate. But it is well known in the art that very thick oxide layers can be grown on not only silicon, but also silicon nitride. This is because oxygen will diffuse through a silicon oxide layer, reach the source of silicon below (such as the silicon substrate, or silicon in silicon nitride), and produce additional silicon oxide.

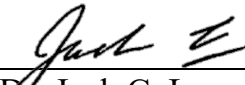
152. It also bears noting that neither of the two exhibits Dr. Giapis cites (Ex. 2042 and 2043) say anything at all about the thickness of a silicon oxide layer that develops when silicon nitride is oxidized. Dr. Giapis's opinion here is not only technologically wrong but lacks record support.

153. Second, any difference between Lee's and Haller's processes is irrelevant. I did not propose that Lee be modified to follow Haller's manufacturing process. Instead, I only pointed to Haller as an example of an acceptable prior art landing pad offsets. *See* Ex. 1003, ¶¶ 437-446.

154. Dr. Giapis is also wrong that Lee's and Haller's respective offsets serve different purposes. Instead, a POSITA would recognize that they serve the very same purpose: ensuring adequate spacing between adjacent conductive structure. Lee, [0049] (offset avoids contact between "stacked conductive layers"); Haller, 6:59-63 (offset "prevent[s]" contact with "adjacent wordline").

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: February 14, 2026

Signature: 
Dr. Jack C. Lee