A Built-In-Test Circuit for Functional Verification & PVT Variations Monitoring of CMOS RF Circuits

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Abstract: Built-In-Test (BIT) for Radio Frequency (RF) integrated circuits can reduce the testing cost, especially with the increase of integration level and operating frequency. A fully integrated CMOS BIT detection circuit is presented in this work. This BIT detection circuit is rectifier-based and low threshold voltage diode-connected MOS transistor with substrate positively-biased is used to improve the detecting sensitivity. As an example, a 2.4GHz LNA is used, the high frequency small signal gain is extracted and the gain fluctuation due to Process, supply Voltage and Temperature (PVT) variations is also investigated. The simulation results show that this BIT detection circuit can realize on-chip functional verification of RF circuits and also monitor the influence of PVT variations on the performance of the circuit without affecting the high frequency performance of the measured RF circuits.

I INTRODUCTION

With the scaling down of CMOS process technology, bulk silicon CMOS process technology has been increasingly used for Radio Frequency (RF) integrated circuits in recent years. The main benefits from the scaling down of CMOS devices are the increase in transit frequency (f_t) and greater integration, which make RF integrated circuits feasible based on bulk silicon CMOS process. However, the continual scaling down of feature size causes increased difficulty in testing RF circuits with high operating frequencies. There are two main problems for the testing of RF circuits; relaying the multi-gigahertz RF signal to the external tester without affecting the performance of RF circuit under test; and prohibitively expensive RF production testers. Reliable high frequency testing has become a significant restrictive and influential factor for the time-to-market of novel wireless products [1-3]. Therefore, in order to reduce the time and cost, it is important to find an easier way to do the functional verification of RF circuits.

Built-in-Test (BIT) detection circuits provide a flexible way to test the output signal of RF IC by including circuits on-chip that allow the high frequency output signal to be tested by a lower frequency or DC external tester [4-7]. BIT circuits can transform the RF output signal into DC signal, and this approach has been used for functional verification and production real-time monitoring. So, testing of RF integrated circuits with DC or low frequency testing equipments becomes easy and the testing cost is reduced to a large extent, especially with the increase of integration level and operating frequency. Since the last two decades BIT or BIST (Built-In-Self-Test) strategies have been a common practice for the testing of digital and mixed-signal systems [8-10]. However, when considering RF circuits, there are some problems related to RF BIST testing, the need for powerful ADC and DACs, cost in additional chip area, power, etc. In order to reduce the high frequency testing cost and monitoring the performance of the designed RF circuits during product evaluation, some works have been done to develop efficient BIT testing techniques for the RF circuits [11-17]. Recent efforts for RF circuit testing have focused on the design of on-chip embedded detectors, or sensors, where the output signals can be tested easily [13, 16-17], and on the methodologies and algorithms for automated test design [15, 16]. However, it is not an

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easy task to design an integrated BIT detection circuit. Generally, the BIT detection circuit should not influence the performance of the tested RF circuit, should not consume too much chip area or power. At the same time, the BIT detection circuit should have high sensitivity and can detect weak RF signals. Most importantly, the output results of the BIT detection circuit should reflect necessary information such as the gain of the tested RF circuits. In addition, BIT circuit should be robust to process, supply voltage and temperature (PVT) variations which affect the performance of RF IC to a large extent.

Integrated circuit (IC) manufacturing variations can be placed in two categories: random variations; and systematic variations. Random variations are inherent fluctuations in process parameters, such as those due to random dopant fluctuations from die-to-die, wafer-to-wafer and lot-to-lot. On the other hand, systematic variations depend on the layout pattern and are therefore predictable [18-19]. Process variation can greatly influence the performance of an integrated circuit. In addition, the fluctuation of supply voltage and temperature also influence the performance of the circuit. Thus, performance fluctuation due to PVT variation must be evaluated easily from the output of BIT detection circuit.

As the BIT circuit is optimized for the circuit under test (CUT), and as the set-up and performance requirements for the external tester are drastically reduced, the testing time can also decrease. Figure 1 shows the test circuit schematic with on-chip BIT detection circuit. There are several points in RF circuits and systems can be accessed to evaluate the high frequency performance. In the analyses, the stimulus is provided by external signal source, but the response of different circuits can be found through the BIT detection circuit.

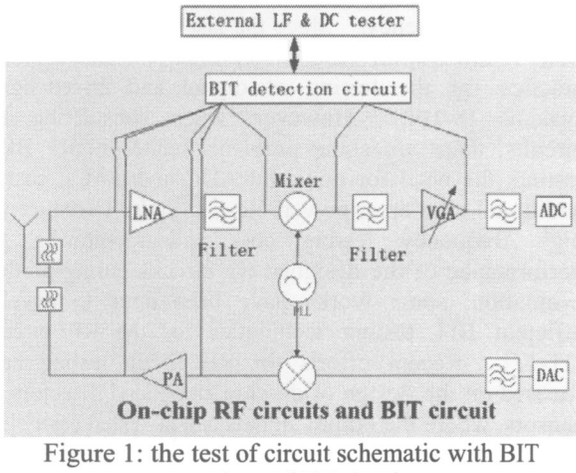

Figure 1: the test of circuit schematic with BIT and tested RF circuits

In this paper, a BIT detection circuit for the testing of RF integrated circuits is proposed. As an example, a 2.4 GHz LNA is designed and its high frequency small signal gain has been extracted and verified by using a novel BIT detection circuit. At the same time, process, supply voltage and temperature variations are considered during the analysis, and the gain difference of the LNA circuit due to PVT variations is investigated by using the results extracted from the output of BIT circuit. The BIT detection circuit used is rectifier-based, utilizing substrate positively biased low threshold voltage MOS transistors to act as rectifying diodes. The high frequency small signal gain of the LNA circuit can be obtained without influencing the performance of the tested RF circuit. Due to the adoption of substrate-positively-biased scheme, this BIT detection circuit has higher sensitivity to detect weaker input RF signal. In section II, the BIT detection circuit is presented and the performance of the transformation from RF signal to DC signal is verified. The 2.4 GHz LNA circuit is given in section III with details of its high frequency small signal performance provided. Section IV includes the functional verification and the analyses of the monitoring of PVT variations by using the result from BIT detection circuit. The paper concludes with some results and conclusions about the validity of using this novel BIT circuit for high frequency circuit testing..

II PROPOSED BIT CIRCUIT

Figure 2 illustrates the BIT detection circuit, which is a charge pump rectifier configuration proposed for high voltage generation [20]. By using the diode-connected MOS transistors and capacitors, this circuit can

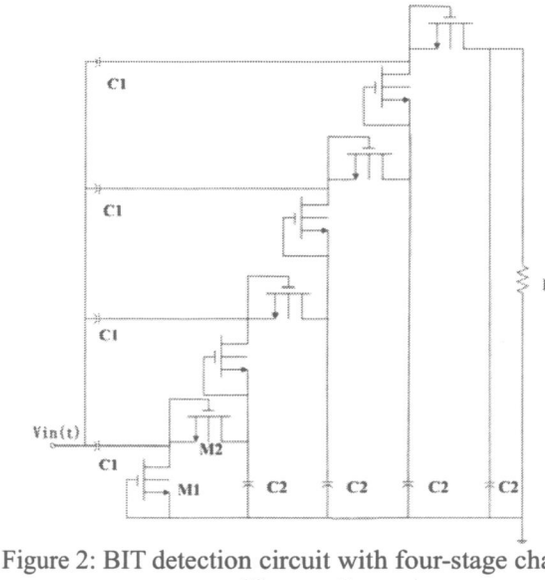

Figure 2: BIT detection circuit with four-stage charge pump rectifier configuration

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transform the input high frequency signal to a corresponding DC signal. For one stage operation, C_1 and M_1 will shift the input voltage up at point A and C_2 and M_2 will rectify the voltage at A. By using this method, the rectifier delivers a constant output current and a constant output voltage. Figure 3 is a graph showing the relationship of rectifier output voltage to the RF input signal power (p1). The input power sweeps from -40dBm to 20dBm in 0.1V steps, and the operating frequency is 2.4GHz. From the result it can be seen that the input high frequency signal can be transformed into DC value and the output voltage varies with the input signal power. As there is no biasing voltage needed, this BIT circuit is a passive one, and a separate supply pad during fabrication for the separate control of this detection circuit is not needed. The parameters of the components in the circuits shown in Figure 2 are C_1=100fF, C_2=700fF, and the channel length and width are 0.3um and 0.35um respectively. The capacitance of C_2 is a little larger, but it can be used as on-chip decoupling capacitor to filter the noise coming from the supply. The circuit parameters can be optimized to give the most optimal performance according to the requirement of the circuit specifications.

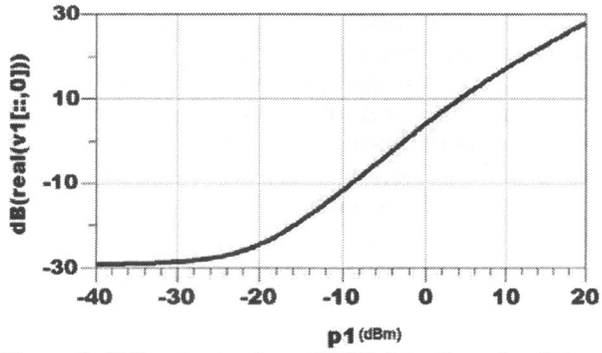

Figure 3: DC output value of BIT detection circuit in figure 2 at different input signal power

In order to detect the weak RF input signal, a lower turn-on-voltage diode is required. To achieve this, the threshold voltage of diode-connected MOS transistor should be low. For our example, a UMC 0.18um low-threshold-voltage MOS transistor was selected for use in the rectifier circuit. By using this low threshold voltage MOS transistor the ability of this circuit to detect weak input signal can be improved. At the same time, a substrate-positively-biased scheme with 0.6V is also adopted to further reduce the turn-on voltage of diode-connected MOS transistor and to improve the detecting sensitivity. The validity of using positively-biased substrate for the improvement of detecting sensitivity can be seen in Figure 6.

III LNA CIRCUIT EXAMPLES

A 2.4GHz low noise amplifier (LNA) (in Figure 4) has been designed and was used to investigate the validity of this BIT detection circuit for the RF circuit testing, and for the examination of the influence of PVT variations on performance. This LNA includes two stages with a fully on-chip input matching network. The UMC 0.18um mixed signal design kits was used, and the high frequency small signal performance of the LNA is summarized in table I.

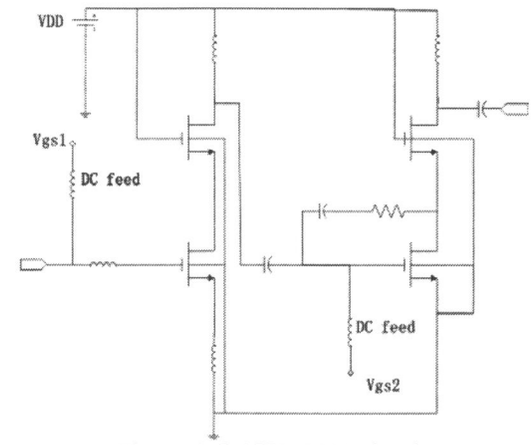

Figure 4: 2.4GHz LNA circuit

Table I the HF performance of 2.4GHz stand-alone low noise amplifier

Frequency (GHz)	Gain (dB)	NF (dB)	S11 (dB)	IP1dB (dBm)
2.4	18.64	2.16	-9	-10

IV RESULTS

For the results in this section, the Agilent ADS simulator was used for the simulations, and to verify the validity of the transformation from RF signal to DC signal.

a) Functional Verification

In this section, this BIT detection circuit for RF testing and for the monitoring of PVT variations of CMOS RF IC is verified by attaching the BIT detection circuit to the tested LNA circuit. This is called combined circuit in the following analyses. This combined circuit includes the LNA circuit in figure 4 and BIT detection circuit in figure 2 which connect these two circuits in the way shown in figure 1. The high frequency small signal gain of LNA circuit can be obtained by extracting from the DC output signal of BIT detection circuit without using a high frequency external tester.

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During the analysis, the input signal amplitude sweeps from -40dBm to 0dBm in steps of 1dB. Figure 5 shows the output time domain signal of the combined circuit. It can be seen that this circuit can realize the transformation from RF output signal to DC signal with different input RF signal amplitude of low noise amplifier.

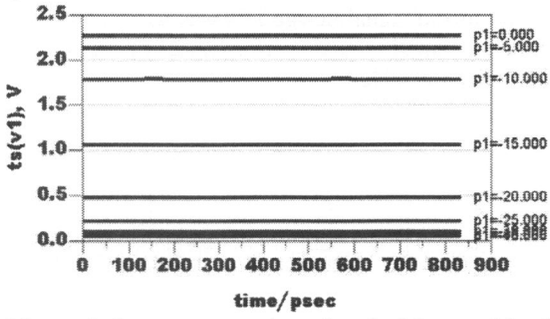

Figure 5: the output transient signal of the combined circuit

Figure 6 evaluates the effectiveness of the positive substrate bias (PSB) of MOS transistors used in BIT detection circuit. With substrate-positively-biased diode-connected MOS transistors in the BIT detection circuit, increased sensitivity can be obtained, for example, for -40dBm input power, the output voltage of the combined circuit is 42mV (marker m1). The output is 6mV (marker m2) when the substrate-positively-biased scheme is not used. This indicates the significant improvement in sensitivity that can be achieved by adopting substrate positively biased scheme.

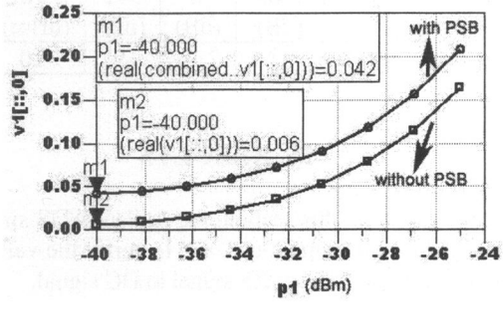

Figure 6: the sensitivity comparison with and without substrate-positively-biased MOS transistors

The high frequency small signal gain of LNA is extracted by using BIT detection circuit. Figure 7 gives the extracted high frequency small signal gain of the LNA, where the BIT detection circuit is attached to the input and output of tested LNA circuit respectively. The curve with marker m2 is the output of BIT detection circuit when attached to the input of LNA and the curve with marker m1 is the output of the BIT detection circuit when attached to the output of LNA. The input amplitude p1 is swept from -40dBm to 0dBm in steps of 0.1dBm. The gain of LNA can be measured as the horizontal distance in dB between marker m1 and m2 when two curves enter into linear region. It can be found that the gain is 18.4dB, and the extracted gain has no much difference with the high frequency gain of stand-alone LNA. From this figure, it can be concluded that this BIT circuit can do functional verification for the CMOS RF circuits.

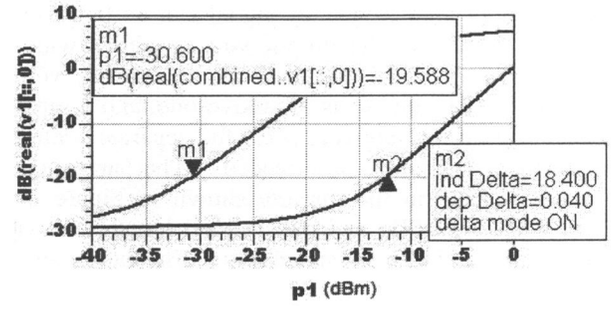

Figure 7: the high frequency small signal gain extracted from the output of BIT circuit attached both at the input and output of LNA

Table II summarizes this 2.4GHz LNA output high frequency performance with and without BIT circuit attached. It can be seen by comparison of the data shown in table I that there is little influence of the high frequency performance of the LNA circuit due to the attached BIT detection circuit. This is critical for any BIT circuit for RF systems.

Table II the performance of 2.4GHz low noise amplifier with and without the BIT detection circuit attached

Circuit	Gain (dB)	NF (dB)	S11 (dB)	IP1 (dBm)
with BIT	18.62	2.16	-9	-10
without	18.64	2.16	-9	-10

b) PVT Variations Monitoring

With this BIT circuit the high frequency small signal gain of LNA can be obtained without using high frequency tester. However, the influence of process, supply voltage and temperature variations on the performance of CMOS RF circuits needs to be fully evaluated. Because this BIT detection circuit is rectifier based, most of circuit components work at a lower frequency than the input signal frequency, except for the first transistor and capacitor. So, the performance of this BIT detection circuit is not going to be influenced so severely as the RF circuit by process or voltage variations which impact on device speed. This BIT detection circuit can be used to evaluate the influence of PVT variations on the performance of RF circuit.

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During the analysis, ±20% and ±10% percentage variations are used for all the parameters in the combined circuit, the supply voltage changes from 1.6V to 2.0V and operating temperature varies from -35° to +80°. The difference in small signal gain of the stand-alone LNA and that extracted from the output of the combined circuit was compared under different PVT variations. For process variation, two extreme process variations are included, namely all parameters in the combined circuit vary from unchanged to the plus or minus maximum percentage variation.

Figure 8 shows the gain difference due to the process, supply voltage and temperature variations. Shown in the figure are the gain differences extracted from the output of BIT circuit, and that obtained from the stand alone LNA. From the results obtained, and those shown in Figure 8, this BIT scheme is able to accurately measure the gain variations, to within 0.5 dB of the LNA for significant variations in process and voltage. For significant temperature variations, the BIT circuit is not as accurate as each transistor in the BIT circuit will experience small variations in threshold voltage due to temperature changes. However even for over a 50° variation, the error is only 1.5 dB. Thus it can be said that PVT variations can be detected and monitored through this on-chip BIT detection circuit.

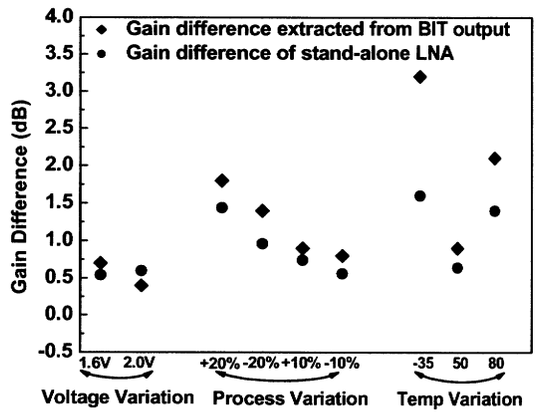

Figure 8: the comparison of gain difference due to PVT variations

V CONCLUSIONS

In this work, a CMOS BIT circuit is presented for RF IC testing. This on-chip circuit can measure the power of high frequency signals allowing accurate gain measurements to be made. The validity of this BIT detection circuit for the functional verification of RF circuits and the evaluation of the influence of the PVT variations on the performance of RF circuits have been tested by using 2.4GHz LNA circuit. This BIT detection circuit is rectifier-based and utilizes low threshold voltage MOS transistors with -positively-biased substrates to act as diodes to enhance sensitivity. For functional verification high frequency small signal gain can be extracted from the DC output value of this BIT detection circuit without influencing the high frequency performance of the circuit under test. By using this methodology the gain fluctuation of LNA due to PVT variations is also investigated. The achieved results show that this BIT detection circuit can be used to test RF circuits, do functional verification and monitor the performance fluctuation due to the PVT variations without affecting the HF performance of tested RF integrated circuits.

VI ACKNOWLEDGEMENTS

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