A Phase Noise Minimization of CMOS VCOs over Wide Tuning Range and Large PVT Variations

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***Abstract*-An automatic amplitude control circuit to minimize the phase noise of a LC-VCO is proposed and implemented by a 0.18-µm CMOS process. The phase noise lower than -90dBc/Hz at 100kHz offset is achieved over a wide tuning range (from 2.2GHz to 2.8GHz) under large process (ΔV_{th} = ±100mV), temperature (from −35°C to 85°C), and power supply (from 1.8V to 3V) variations.**

I. Introduction

A rapid performance improvement of a recent CMOS device enlarges its application area in the integrated RF transceiver [1-3]. However, circuit designers are facing a difficult trade-off between the performance and the yield because the process variation becomes large as the device is scaled. For a yield improvement and a cost reduction, a robust circuit design that has a calibration or tracking mechanism becomes more and more important.

In an RF transceiver, a phase noise of the local oscillator is a critical parameter and determines the system performance. In general, increasing the oscillation amplitude reduces the phase noise of a LC-VCO [4,5]. However, too large amplitude makes the transistors generating a negative-gm operate in the triode region and de-Q the LC-tank, which results in a degraded phase noise [6]. Compared with bipolar transistors, the device parameters of MOSFETs widely change according to process, supply voltage, and temperature (PVT) variations. Furthermore, the Q of the LC-tank theoretically depends on the oscillation frequency. Therefore, it is very difficult to maintain the optimum oscillation amplitude without a feedback control. Although several papers [7,8] reported automatic amplitude control (AAC) circuits for the CMOS LC-VCOs, they have not discussed the optimum amplitude and the influence of the PVT variations.

This paper presents a novel circuit that automatically controls the oscillation amplitude of CMOS VCOs to the optimal level for the phase noise reduction. The proposed technique uses a V_{th} of the MOSFET as a reference level and has an ability to compensate the PVT variations. The low phase noise operation over a wide frequency range under the large PVT variations is demonstrated.

II. AAC Circuit for Minimum Phase Noise

The schematic of the VCO and the proposed AAC circuit are shown in Fig. 1. As shown in Fig. 2, the peak-to-peak oscillation amplitude is equal to $V_{GS} - V_{DS}$ of M1 and M2. As the bias current is increased, the oscillation amplitude becomes large and the phase noise decreases. However, once the oscillation amplitude becomes larger than the threshold voltage (V_{th}) of M1 and M2, each transistor enters the triode region and the equivalent parallel resistance of the LC-tank decreases. This reduces the Q of the tank and drastically degrades the phase noise of the VCO. Especially in CMOS LC-VCOs, degradation of the tank Q generates higher order harmonics in the oscillation waveform and up-converts the flicker noise of the current source M10[4,6]. The above discussion indicates that the optimal value of the peak-to-peak amplitude, which is its maximal possible value, is V_{th}.

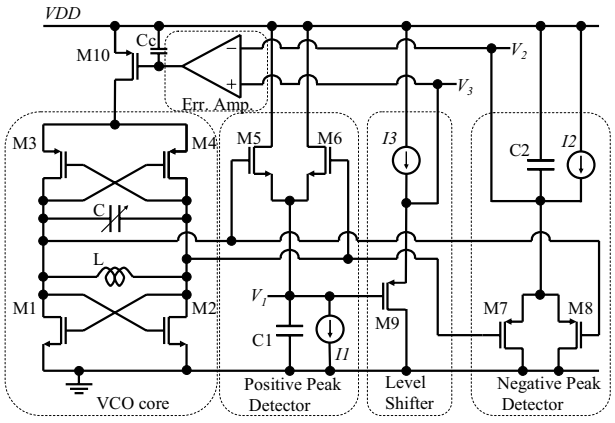
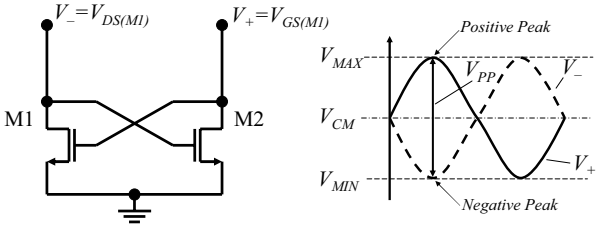


Fig. 1. Proposed VCO automatic amplitude control circuit.



Condition for saturation : $V_{GS(M1)} - V_{DS(M1)} \leqq V_{th}$

$\therefore V_+ - V_- = V_{PP} \leqq V_{th}$

Fig. 2. VCO swing of cross-coupled NMOS

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Since the oscillation amplitude strongly depends on the circuit parameters such as a Q of the tank and transconductance of the MOSFETs, it is almost impossible to keep the amplitude at optimum level without feedback control. Even when oscillation amplitude is controlled in a feedback loop [7,8], a fixed reference level does not track the PVT variations since the V_{th} depends on the process and temperature. Although LC-tank circuit can be used to keep high impedance even when the MOSFETs are in triode region [6], it is not suitable for wide tuning range VCO because its impedance decreases at off resonance. Furthermore, it increases a chip size and a die cost.

To control the peak-to-peak amplitude, our AAC circuit uses the threshold voltage itself as the reference level in a feedback loop. Since the reference level tracks the PVT variations, the oscillation amplitude is always kept at the optimal level. Therefore, a low phase noise can be achieved over wide tuning range under large PVT variations.

The AAC circuit consists of two peak detectors, a source follower for level shift, and an error amplifier as shown in Fig. 1. The rectifier consisting of M5, M6, C1 and current source *I1* detects the positive peak of the oscillation signal of the VCO. The output voltage (V_1) of the positive peak detector is described as

$$V_1 \approx V_{MAX} - V_{GSN}. \quad (1)$$

V_{GSN} is the gate to source voltage of M5 and M6. Since they are biased by a small current (5uA), the V_{GSN} is approximately equal to the threshold voltage (V_{thN}) of M5 and M6. Therefore (1) can be rewritten as

$$V_1 \approx V_{MAX} - V_{thN}. \quad (2)$$

On the other hand, the rectifier consisting of M7, M8, C2 and current source *I2* detects the negative peak of VCO signal. The output level (V_2) of the negative peak detector is described as

$$V_2 \approx V_{MIN} + |V_{thP}|. \quad (3)$$

V_{thP} is the threshold voltage of M7 and M8. The output level of the positive peak detector (V_1) is shifted by $|V_{thP}|$ through a source follower circuit consisting of M9 and *I3*. The output (V_3) of the source follower is described as,

$$V_3 \approx V_1 + |V_{thP}| = V_{MAX} - V_{thN} + |V_{thP}|. \quad (4)$$

Finally, the V_3 and V_2 are connected to the positive and negative input pins of the error amplifier, respectively. The output of the error amplifier is fed back to the current source (M10) of the VCO core. If V_3 is larger than V_2, the error amplifier reduces the bias current of the VCO and the oscillation amplitude decreases until V_3 becomes equal to V_2. On the other hand, when the V_3 becomes smaller than V_2, the error amplifier increases the bias current and oscillation amplitude of the VCO until the V_3 becomes equal to V_2. As a result, the VCO is biased so that the equation $V_3=V_2$ is satisfied. From equations (3) and (4), $V_3=V_2$ leads

$$V_{MAX} - V_{MIN} = V_{thN}. \quad (5)$$

Equation (5) means that the peak-to-peak amplitude of the VCO is equal to the threshold voltage of NMOSs, which is the optimal condition for the phase noise minimization.

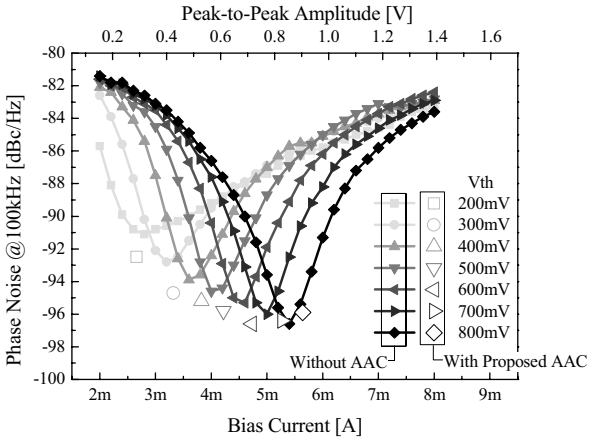

Fig. 3. Simulated phase noise at 100kHz-offset vs. bias current for different values of threshold voltage of NMOS FETs.

The closed-loop stability was verified by harmonic balance simulation in a commercial simulator. Even when the PMOS M3 and M4 operate at a triode region, the existence of current source M10 keeps the impedance of the tank high. Though the amplitude of the VCO varies with V_{th} in this scheme, it does not become a problem since the gain of frequency mixers can be flattened when the VCO signal is amplified by using a buffer.

Fig. 3 shows the simulated phase noise at 100 kHz-offset of the VCO with or without the proposed AAC for different values of V_{th}. The lower horizontal axis shows the bias current and the upper horizontal axis shows the corresponding peak-to-peak amplitude voltage of the VCO. Solid lines with closed symbols correspond to the case without proposed AAC. Each curve exhibits *V-shaped* characteristics: The phase noise decreases with the increase of the bias current at first. However, once the bias current exceeds the optimal current, the phase noise increases with the bias current. Note that each peak-to-peak amplitude (upper horizontal axis in Fig. 3) at the optimal current is approximately equal to the V_{th}. Therefore, the simulated phase noise for VCO with the proposed AAC (open symbols in Fig. 3), which uses V_{th} as reference level, successfully tracks the point of the optimal bias current and the minimal phase noise.

III. Implementation and Experimental Results

The VCO with the proposed AAC circuit is implemented in a 5-layer metal (Al) 0.18-μm standard digital CMOS process with MIM capacitors. The oscillation frequency can be tuned from 2.2GHz to 2.8GHz which covers 2.4GHz ISM band. The on-chip differential spiral inductor is 144μm on a side and has three turns. Measured inductance is 1.5nH and Q ranges from 3.5 to 4.5 over the oscillation frequency range. The tank capacitor consists of switchable MIM capacitors for a coarse-tuning and a p-n junction varactor for a fine-tuning. A digital tuning circuit selects an optimal setting of the

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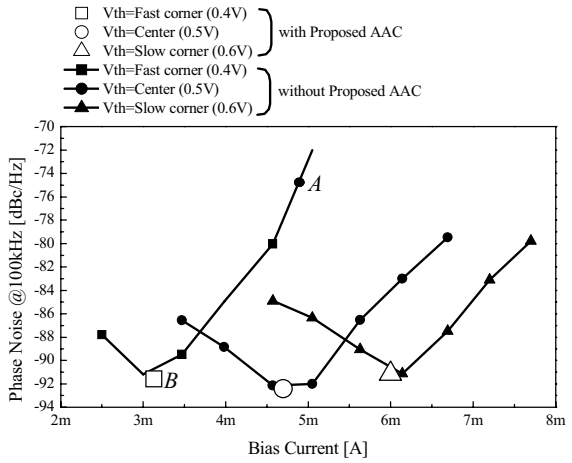

Fig. 4. Measured phase noise vs. bias current for different V_{th}s.

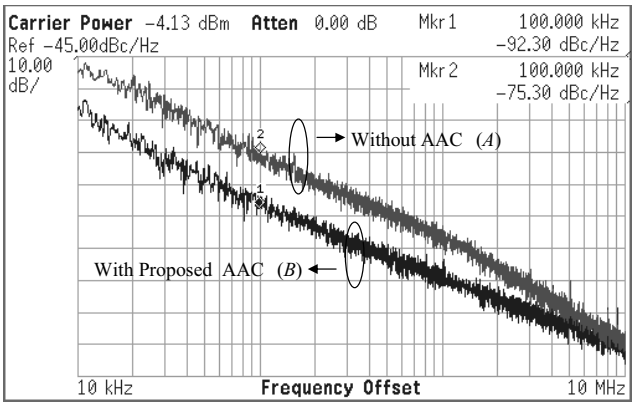

Fig. 5. Phase noise spectra at *A* and *B* in Fig. 4.

switchable capacitors according to the required oscillation frequency. The VCO tuning sensitivity (*Kv*) by the pn-junction varactor is kept less than 50 MHz/V to prevent the phase noise degradation.

Fig. 4 shows the measured phase noise at 100 kHz-offset as a function of the bias current. The oscillation frequency is set at 2440 MHz. To investigate the influence of the process variation, corner samples with threshold voltage varied by ±0.1V are fabricated as well as the center sample (V_{th} = 0.5V). As can be seen, the characteristics are very similar to the simulation results shown in Fig. 3. In the case without AAC, each curve shows *V-shaped*, and a higher V_{th} sample requires larger bias current to minimize the phase noise. By proposed AAC, the VCO is successfully set to its optimal bias current and phase noise lower than -92dBc/Hz is achieved despite the V_{th} variation. The phase noise spectra of fast corner sample at the point *A* and the point *B* are shown in Fig. 5. If the bias current is fixed to 4.7mA, which is the optimal value for the center V_{th} sample but not optimal for the fast corner sample, the phase noise degrades to -75dBc/Hz (*A*). However, the proposed AAC circuit controls the bias current to the optimal value for the fast corner sample (3.1mA),

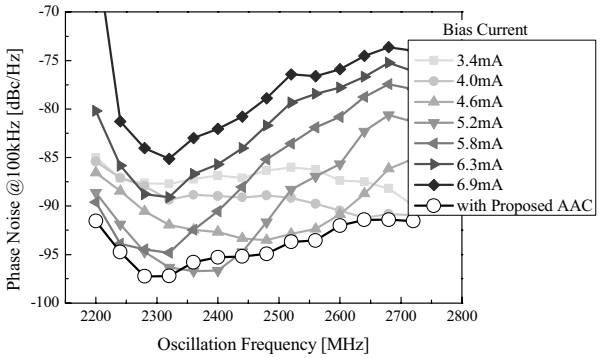

Fig. 6. Measured phase noise vs. oscillation frequency.

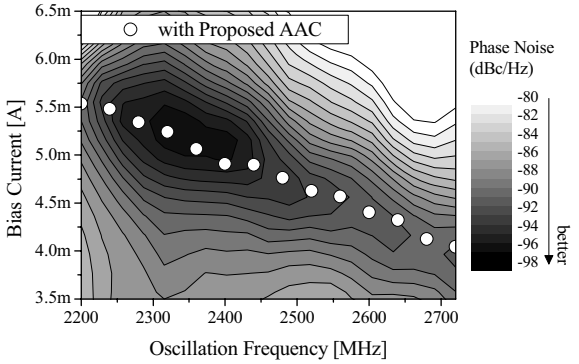

Fig. 7. Measured phase noise vs. bias current and oscillation frequency.

and suppresses the phase noise to -92dBc/Hz (*B*) at 100kHz-offset.

The phase noise dependences on the oscillation frequency, temperature, and power supply voltage are shown in Fig. 6 through Fig. 9, respectively. Fig. 6 shows the values of the phase noise as a function of the oscillation frequency with or without proposed AAC. Without AAC (closed symbols), since the Q of the tank varies with the oscillation frequency, the optimal bias current varies as well. Therefore, the phase noise strongly depends on the oscillation frequency when the bias current is fixed. However, in the case with AAC (open circles), the bias current is set to the optimal value at each frequency, and phase noise is kept lower than -92dBc/Hz from 2.2GHz to 2.8GHz. Fig. 7 shows a contour plot of the phase noise when the frequency (X-axis) and the bias current (Y-axis) are swept. The open circles in the graph show the bias current controlled by the AAC circuit. As the oscillation frequency lowers, the equivalent parallel resistance decreases because of the degradation of Q of the inductor. On the other hand, the optimal amplitude keeps constant since the value of V_{th} does not change. Therefore, at a lower frequency, more current is required to keep the optimal amplitude. The open circles trace the minimal point of the phase noise at each frequency, which indicates that the VCO is optimally biased by the AAC.

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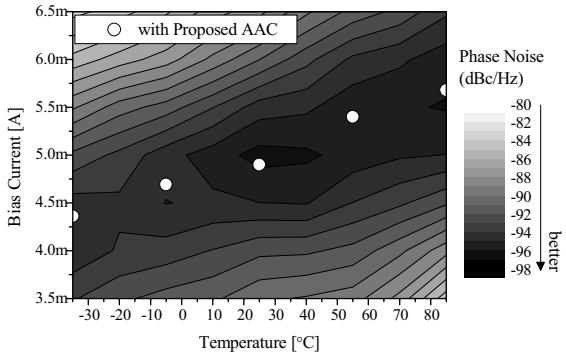

Fig. 8. Measured phase noise vs. bias current and temperature.

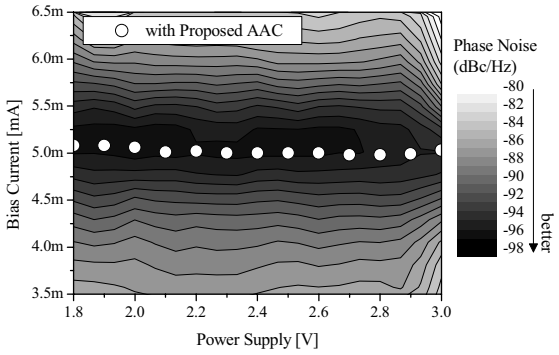

Fig. 9. Measured phase noise vs. bias current and power supply voltage.

The dependence on temperature is shown in Fig. 8. A larger current is required as the temperature increases because the *gm* of the MOSFETs decreases. On the other hand, the optimal amplitude decreases because the V_{th} decreases as the temperature increases. Therefore, maintaining the optimal amplitude is very difficult when the temperature varies. From -35°C to 85°C, the proposed AAC circuit (open circles) tracks the optimal bias current, and phase noise is kept lower than -94dBc/Hz.

The dependence on the supply voltage is shown in Fig. 9. The optimal bias current for minimal phase noise does not depend on the supply voltage ranging from 1.8V to 3.0V. Therefore, a complicated supply-independent biasing circuit is required when the AAC circuit is not used. On the other hand, the proposed AAC circuit controls the bias current automatically at optimal bias current.

Measured performance of the implemented VCO with the proposed AAC is summarized in Table I. The photograph of the fabricated VCO with the proposed AAC circuit is shown in Fig. 10. The circuit area is 0.3mm^2 and current consumption at the nominal condition is 5mA.

TABLE I
MEASURED PERFORMANCE OF THE VCO WITH PROPOSED AAC

Parameter	Range
Threshold Voltage (V_{th})	0.5V ± 100mV
Temperature	-35°C ~ 85°C
Power Supply Voltage	1.8V ~ 3.0V
Oscillation Frequency	2.2GHz ~ 2.8GHz
Current	2.2mA ~ 7.0mA (5mA@center cond.)
Phase Noise	< -90dBc/Hz @100kHz-offset

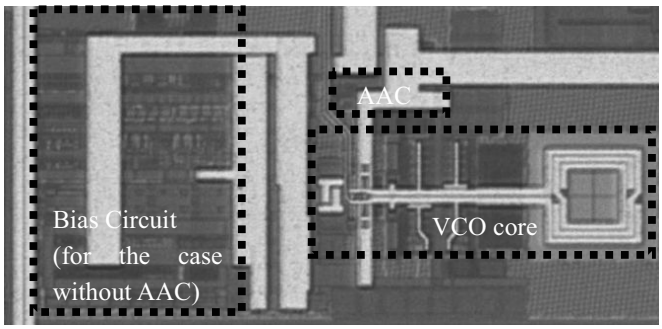

Fig. 10. Photograph of the VCO with proposed AAC.

IV. CONCLUSION

We proposed a novel scheme to minimize the phase noise of a wide tuning range CMOS LC-VCO. Experimental results showed that the proposed AAC circuit successfully controlled the oscillation amplitude at the optimal level using the threshold voltage of NMOS as a reference. The tracking ability of the proposed AAC circuit was verified under large process, temperature, and supply voltage variations. Our scheme can be used to improve the chip yield.

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