

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, DC**

**Before The Honorable MaryJoan McNamara
Administrative Law Judge**

In the Matter of

**CERTAIN DYNAMIC RANDOM ACCESS
MEMORY (DRAM) DEVICES,
PRODUCTS CONTAINING THE SAME,
AND COMPONENTS THEREOF**

Investigation No. 337-TA-1472

**SAMSUNG RESPONDENTS' SECOND SUPPLEMENTAL
OBJECTIONS AND RESPONSES TO COMPLAINANT
NETLIST INC.'S FIRST SET OF INTERROGATORIES (NOS. 1-38)**

Pursuant to the United States International Trade Commission's Rules of Practice and Procedure, 19 C.F.R. §§ 210.27 and 210.29, and the ALJ's Ground Rules (Order No. 2), Respondents Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. (collectively, "Samsung" or "Respondents"), by counsel, hereby submit their second supplemental responses and objections to Complainant Netlist, Inc.'s ("Netlist's" or "Complainant's") First Set of Interrogatories (Nos. 1-38) to Samsung. As Samsung's investigation in this matter is continuing, Samsung reserves the right to amend and/or supplement these responses in accordance with the Commission's Rules, the Ground Rules, and the Procedural Schedule.

GENERAL STATEMENT AND OBJECTIONS

The Responses and Objections provided here are submitted on behalf of Samsung and reflect Samsung's continuing investigation of facts and discovery of information and documents relating to the claims and defenses at issue in this Investigation. Accordingly, Samsung's responses to these Interrogatories are based only upon Samsung's current knowledge and reasonable belief.

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RESPONSE TO INTERROGATORY NO. 32 (JANUARY 22, 2026):

In addition to and without limiting the foregoing General Objections, which are incorporated by reference as though fully set forth herein, Samsung objects to this Interrogatory to the extent it seeks information protected from discovery by the attorney-client privilege, attorney work product doctrine, or any other applicable privilege or immunity. Samsung objects to this Interrogatory to the extent it requires legal conclusions and/or expert analysis regarding interpretation of claim terms and characterization of the accused products, features, and/or functionalities. Samsung objects to this Interrogatory to the extent it seeks premature disclosure of expert opinions or contentions, in advance of the date when such disclosure is required by any Procedural Schedule entered in this Investigation. Samsung further objects to this Interrogatory to the extent it seeks Samsung's contentions in a specific format.

Subject to and without waiving any general or specific objections, Samsung responds as follows: Samsung will provide its contentions responsive to this Interrogatory on a date to be agreed between the parties for exchange of contentions.

Samsung states that it is continuing to investigate the subject matter of this Interrogatory and reserves the right to supplement its response to the extent it locates any non-privileged, relevant documents or information responsive to this Interrogatory in accordance with the procedures and timetables established by the Commission's Rules of Practice and Procedure, the Ground Rules, and the Procedural Schedule entered in this Investigation, and after Samsung has been afforded an adequate opportunity to investigate Complainant's allegations through discovery in this Investigation.

[REDACTED]

FIRST SUPPLEMENTAL RESPONSE TO INTERROGATORY NO. 32 (MARCH 25, 2026):

Subject to and without waiving the specific objections and general objections, Samsung responds as follows:

Netlist has accused hundreds of Samsung products of infringement. *See* Samsung's Resp. to Interrogs. Nos. 1, 12 (Mar. 25, 2026). To the extent Netlist arguably presents evidence specific to one Samsung product, its deficient contentions fail to show that the allegations and cited evidence are applicable to any other Accused Product(s) or that any one product is representative of any other Accused Product(s).

Samsung's investigation is ongoing, and Samsung reserves the right to further supplement its response to this Interrogatory as discovery progresses.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

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[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

4. '087 Patent

The Accused Products do not infringe the asserted claims of the '087 Patent (claims 1, 2, 5, 7, 8, 13, 17, 18, 20, 22, 23) for at least the reasons explained below. Netlist's contentions are deficient, and Netlist has not demonstrated that any Accused Products practice the asserted claims of the '087 Patent. Nor has Netlist shown that any asserted claim is infringed under the doctrine of equivalents. Netlist's contentions regarding infringement under the doctrine of equivalents consist of a mere reference to "the doctrine of equivalents" and provide no analysis. *See, e.g.*, '087 Chart at 1. Nor has Netlist shown that Samsung has indirectly infringed any asserted claim of the '087 Patent, either contributorily or through inducement. Netlist's contentions regarding indirect infringement consist of a bare recitation of the legal test for contributory infringement and

[REDACTED]

inducement. *See* '087 Chart at 1. Samsung also notes that Netlist improperly relies on prior proceedings involving different patents, different claims, and different claim terms. Samsung reserves all rights to respond to any updates by Netlist that purport to identify hardware that allegedly implements one or more limitations of the asserted claims of the '087 Patent or otherwise purport to change or clarify any of Netlist's infringement contentions.

(a) Claim 1

The Accused Products do not infringe claim 1 of the '087 Patent, for multiple reasons. For example and without limitation, Netlist does not identify with any specificity the accused “first set of C/A signals associated with a memory read operation and ... second set of C/A signals associated with a memory write operation.” Netlist merely identifies tables of C/A and control signals without explaining how such signals purportedly meet the limitations of claim 1. For example, Netlist identifies Read and Write commands, but does not explain how these C/A signals allegedly meet other limitations of claim 1, and mixes and matches C/A signals to meet various limitations. As one example, Netlist identifies the Read Command (RD, RDA) and Write Command (WR, WRA) for limitation 1[c], *see* '087 Chart at 68, 70, then identifies control signals such as SelectWIR, CaptureWR, and ShiftWR for limitation 1[i]. *See id.* at 163. Netlist also has not shown evidence or explained how the state of conduits changing in response to different operating modes of a purported control circuit controlled by control signals is a change in response to C/A signals, as required by claim 1.

Further for example, the Accused Products do not include “first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies” or “second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured to

[REDACTED]

conduct any signal from any of the stacked DRAM dies to the control die.” Netlist has not shown that the interconnects it identifies as the first or second unidirectional interconnects are unidirectional as required by claim 1. Netlist identifies “interconnects for read strobes or read clock signals such as [REDACTED]” as the first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies. *See* ’087 Chart at 194. Netlist identifies “interconnects for write strobes or write clock signals such as WCKs” as the second unidirectional interconnects configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured to conduct any signal from any of the stacked DRAM dies to the control die. *See id.* [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED]

[REDACTED]

[REDACTED] The “evidence” that Netlist cites in its claim chart merely refers to signals that are unidirectional, [REDACTED]

[REDACTED] *See, e.g.,* ’087 Chart at 194-211. The JEDEC standard does not describe or require unidirectional interconnects. *See id.* at 195.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

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[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED]

[REDACTED]

Further for example, the Accused Products do not include a “control die [that] further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal.” This limitation requires that the C/A signals (not including a chip select signal) select between the first and second conduit. This control of these data conduits is done for memory read and write operations, as the preceding limitation identifies them as “the first conduit of the first data conduits” and “a second conduit of the second data conduits.” Controlling the conduits allows the data conduits to be in a state where data can be written to or read from memory. [REDACTED]

[REDACTED]

[REDACTED] Chip select signals enable or select array dies for data transfer. *See* '087 Patent at 16:5-12. In the context of HBM, SID signals are chip select signals, because they enable TSV drivers to drive data to particular, selected DRAM dies. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED]

[REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED]

[REDACTED]

In its infringement contentions, Netlist points to states of conduits being controlled by “different operating modes” or “in response to lane repair control signals” or “read, write, and other commands for memory operations” as allegedly meeting this claim limitation. *See* '087 Chart at 189. Netlist states that “the various commands do not include chip select signals, and commands entered through both the PHY region and D/A region would not include chip select signals. Nor does the IEEE 1500 test protocol include chip select signals.” *See* '087 Chart at 187. As support for this, Netlist cites the JESD238A Table 6.3.1 Command Truth Table and states that “[a]s seen in the truth table above, commands do not include chip select signals.” *Id.* at 188. However, the truth table shows stack ID (SID) signals, which are signals used to select dies for reading and writing. [REDACTED]

[REDACTED] Netlist’s expert witness Dr. Brogioli successfully argued in C.A. No. 21-cv-463 (E.D.Tex.) that for the related '060 Patent, SID signals are chip select signals. He argued that for a given SID signal or combination of SID0/SID1 signals received at a given channel, only one DRAM die will be selected. Because each channel is associated with only one of the four dies

[REDACTED]

in a stack, the value of SID received at a given channel uniquely identifies a DRAM die. In fact, Dr. Brogioli specifically argued that [REDACTED]

[REDACTED]

[REDACTED]. These SID signals are required to control the respective state of the first and second data conduits in order to select which data conduits should drive or receive data.

Additionally, the functionality that Netlist identifies does not control the states of the conduits as required by this limitation, nor does Netlist attempt to explain how it allegedly does so. First, Netlist does not explain how different operating modes are a C/A signal where the “control logic [is] configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals.” Operating modes are not C/A signals, and the explicit claim language requires that the conduit states are controlled in response to C/A signals. Second, the “lane repair control signals” that Netlist identifies are signals that control use of spare lanes when a faulty lane is identified, not command/address signals as claimed. Finally, Netlist identifying “read, write and other commands for memory operations” is without bounds, and Netlist does not explain what C/A signals it alleges control the states of the conduits. Rather, SID signals, as discussed above, are among the “commands for memory operations” used to control the respective state of the conduits.

Further for example, the Accused Products do not include “a first data terminal” where “a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal.” [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] Netlist points to the WSI terminal as allegedly meeting this claim requirement. But claim 1 requires that “the DRAM package is configured to receive C/A signals via the C/A terminals and is further *configured to receive or output data signals via the data terminals in response to the (C/A) signals.*” (emphasis added). The same limitation further states that “the DRAM package is configured to output first data signals in response to a first set of C/A signals *associated with a memory read operation* and to receive second data signals in response to a second set of C/A signals *associated with a memory write operation.*” Therefore, the data terminals, including “a first data terminal,” must receive or output data signals in response to C/A signals that are associated with a memory read or memory write operation. In its claim chart, Netlist identifies alleged data conduits in the D/A testing region that purportedly share the same terminal. Specifically, Netlist identifies the test signal input WSI in the IEEE 1500 Port as the purported first data terminal shared by the conduits. *See* ’087 Chart at 159. Netlist then identifies control signals such as SelectWIR, CaptureWR, ShiftWR, and UpdateWR as purported “command signals.” *See* ’087 Chart at 163. But these signals are not C/A signals as required by the express claim language; they are control signals that merely control the state of the WIR buffer. Tellingly, Netlist later alleges that “the state of the data conduits may be controlled in response to lane repair control signals.” *See* ’087 Chart at 189. As explained above, these are not command/address signals as claimed. Additionally, the identified signals are not associated with data signals as required by the express claim language because, as Netlist admits, the IEEE 1500 Port only relates to *test* signals. *Id.* at 164. Nor are the identified control signals associated with read and write operations as required by claim 1; [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

See, e.g., Samsung_1472_00531859 at -532062.

(b) Claim 2

The Accused Products do not infringe claim 2 of the '087 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 2 depends from claim 1 and the Accused Products do not infringe claim 2 at least for the same reasons that they do not infringe claim 1.

Further for example, Netlist has not shown that all of the Accused Products include “stacked DRAM dies [that] include at least 8 stacked DRAM dies.” Netlist only accuses “some configurations” of having at least 8 stacked DRAM dies, but does not differentiate between those configurations it accuses of having 8 or more stacked DRAM dies and those that do not. Netlist’s infringement contentions do not identify which Accused Products have 8 or more stacked DRAM dies or differentiate between different models of HBM generations. For example, at least the Accused Flashbolt, Flarebolt, and Aquabolt Products have a 4 stacked DRAM die configuration. *See Samsung_1472_00592964 at -592971; Samsung_1472_00598038 at -598043; Samsung_1472_00597740 at -597744.*

(c) Claim 5

The Accused Products do not infringe claim 5 of the '087 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 5 depends from claim 1 and the Accused Products do not infringe claim 5 at least for the same reasons that they do not infringe claim 1.

Further, Netlist only accuses “some configurations” of meeting the limitation “the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and

subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently conducted via the first data interconnects in parallel.” Netlist’s infringement contentions do not identify which Accused Products allegedly have this configuration or differentiate between different models of HBM generations. Further, for example, Netlist’s infringement contentions do not show that the first or second data signals are conducted or received in parallel. Netlist does not provide argument or evidence as to how “in at least some configurations” the Accused Products meet this limitation.

(d) Claim 7

The Accused Products do not infringe claim 7 of the ’087 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 7 depends from claim 1 and the Accused Products do not infringe claim 7 at least for the same reasons that they do not infringe claim 1.

(e) Claim 8

The Accused Products do not infringe claim 8 of the ’087 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 8 depends from claim 1 and the Accused Products do not infringe claim 8 at least for the same reasons that they do not infringe claim 1.

Further, Netlist only accuses “some configurations” of meeting the limitation “the at least one DRAM die of the second plurality of DRAM dies has at least one electrical connection leading from the at least one TSV, the at least one electrical connection is not electrically connected to any data port on the at least one DRAM die.” Netlist’s infringement contentions do not identify which Accused Products allegedly have this configuration or differentiate between different models of HBM generations.

(f) Claim 13

[REDACTED]

The Accused Products do not infringe claim 13 of the '087 Patent. For example, as discussed for claim 1, Netlist's infringement contentions do not identify the accused C/A signals that purportedly meet the different limitations of the claim. Further, Netlist does not explain what the claimed "interface" is via which the DRAM package receives command/address (C/A) signals, and via which the DRAM package receives or outputs data signals, the interface including terminals, the terminals including C/A terminals and data terminals.

Further, the Accused Products do not meet the "unidirectional" limitations of claim 13 for the same reasons discussed above with regard to claim 1.

(g) Claim 17

The Accused Products do not infringe claim 17 of the '087 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 17 depends from claim 13 and the Accused Products do not infringe claim 17 at least for the same reasons that they do not infringe claim 13.

Additionally, Netlist only accuses "some configurations" of meeting the additional limitation of claim 17, which claims "the signal conduits in the control die include first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby: the first data conduits are enabled to receive and drive the first data signals in response to the first set of C/A signals; the second conduits are enabled to receive and drive the second data signals in response to the second set of C/A signals; each of the first data conduits are placed in a non-driving state after driving the first data signals; each of the second data conduits are placed in a non-driving state after driving the second data signals; and data

[REDACTED]

conduit in the first and second data conduits in a non-driving state are not configured to receive or drive any signals.” Netlist’s infringement contentions do not identify which Accused Products allegedly have this configuration or differentiate between different models of HBM generations. Further for example, Netlist’s infringement contentions do not identify how the Accused Products’ alleged C/A signals are consecutive sets of C/A signals. Further for example, Netlist’s infringement contentions do not show how the first conduits are allegedly placed in a non-driving state after driving the first data signals or how the second data conduits are placed in a non-driving state after driving the second data signals.

(h) Claim 18

The Accused Products do not infringe claim 18 of the ’087 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 18 depends from claim 13 and the Accused Products do not infringe claim 18 at least for the same reasons that they do not infringe claim 13.

Further, Netlist does not cite to a single document in its infringement contentions for this claim. Netlist’s infringement contentions merely cite back to discussions and evidence for different claim limitations without explanation of how they relate to this claim or purport to show infringement of this claim by the Accused Products.

Further for example, the Accused Products do not include a “control die [that] includes logic configurable to control respective states of the first conduit and the second conduit in response to one or more C/A signals received via one or more second terminals of the terminals, wherein the one or more C/A signals do not include any chip select signal.” The Accused Products do not meet this limitation for the same reasons discussed with respect to the limitation of claim 1 that “the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the

[REDACTED]

C/A terminals, wherein the one or more C/A signals do not include any chip select signal.” In claim 18, the “one or more second terminals of the terminals” refers to a C/A terminal as it receives C/A signals. *See* ’087 Patent, cl 18.

(i) Claim 20

The Accused Products do not infringe claim 20 of the ’087 Patent. Netlist does not cite to a single document in its infringement contentions for this claim. Netlist’s infringement contentions merely cite back to discussions and evidence for different claim limitations without explanation of how they relate to this claim or purport to show infringement of this claim by the Accused Products.

Further for example, the Accused Products do not include “first unidirectional interconnects ... wherein the control die is configured to receive signals from the first unidirectional interconnects ... wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects” or “second unidirectional interconnects ... wherein the control die is configured ... to drive signals to the second unidirectional interconnects ... wherein the control is not configured ... to receive any signals from any of the second unidirectional interconnects” for the same reason the accused HBM products do not meet the “unidirectional” limitations of claim 1.

Further for example, the Accused Products do not include a “control die [that] further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal.” The Accused Products do not meet this limitation for the same reasons discussed with respect to the limitation of claim 1 that a “control die [that] further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or

[REDACTED]

more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal.”

Further for example, the Accused Products do not include “a first data terminal” where “the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal.” The Accused Products do not meet this limitation for the same reasons discussed with respect to the limitation of claim 1 that requires “a first data terminal” where “a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal.” Further, claim 20 requires that “the DRAM package is configured to receive C/A signals via the C/A terminals and *receives or outputs data signals via the data terminals in response to the (C/A) signals*, wherein the DRAM package is configured to *output a first n-bit-wide data signal via the data terminals in response to a set of C/A signals associated with a memory read operation* and to *receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation*, n being 32 or 64.” This is substantially similar to claim 1’s limitations that “the DRAM package is configured to receive C/A signals via the C/A terminals and is further *configured to receive or output data signals via the data terminals in response to the (C/A) signals*” and “the DRAM package is configured to output first data signals in response to a first set of C/A signals *associated with a memory read operation* and to receive second data signals in response to a second set of C/A signals *associated with a memory write operation*.” Therefore, the Accused products do not meet this limitation for the same reasons discussed for claim 1.

[REDACTED]

(j) Claim 22

The Accused Products do not infringe claim 22 of the '087 Patent because they do not meet each and every limitation of that claim, either literally or under the doctrine of equivalents. Claim 22 depends from claim 20 and the Accused Products do not infringe claim 22 at least for the same reasons that they do not infringe claim 20.

(k) Claim 23

The Accused Products do not infringe claim 23 of the '087 Patent.

For example, the Accused Products do not include “the power supply interconnects [that] include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies.” [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] Netlist cites documents that purport to show that the Accused Products have [REDACTED], but does explain how the cited documents show the Accused Products allegedly meet this limitation.

Further for example, the Accused Products do not include “first unidirectional interconnects ... wherein the control die is configured to receive signals from the first unidirectional interconnects ... wherein the control die is not configured to drive any signal to any

[REDACTED]

of the first unidirectional interconnects” or “second unidirectional interconnects ... wherein the control die is configured ... to drive signals to the second unidirectional interconnects ... wherein the control is not configured ... to receive any signals from any of the second unidirectional interconnects.” The Accused Products do not meet this limitation for the same reasons discussed with respect to the “unidirectional” limitations of claim 1.

Further for example, the Accused Products do not include a “control die [that] further includes control logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal.” The Accused Products do not meet this limitation for the same reasons discussed with respect to the limitation of claim 1 that a “control die [that] further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, wherein the one or more C/A signals do not include any chip select signal.”

Further for example, the Accused Products do not include “a first data terminal” where “the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal.” The Accused Products do not meet this limitation for the same reasons discussed with respect to the “a first data terminal” limitation of claim 20.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

Dated: March 25, 2026

Respectfully Submitted,

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