1 UNITED STATES PATENT AND TRADEMARK OFFICE

2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3 - - - - - - - - - - - - - - x

4 SAMSUNG ELECTRONICS CO., :

5 LTD., :

6 Petitioner, : Case IPR2025-01431

7 v. : U.S. Patent No.

8 NETLIST, INC., : 10,025,731

9 Patent Owner. :

10 - - - - - - - - - - - - - - X

11

12 Deposition of ANDREW WOLFE, Ph.D.

13 Conducted Virtually

14 Friday, May 15, 2026

15 11:57 a.m. EDT

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19

20 Job No.: 633281

21 Pages 1 - 113

22 Reported by: Debra A. Whitehead

1 Deposition of ANDREW WOLFE, Ph.D., conducted
2 virtually.
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5 Pursuant to notice, before Debra Ann Whitehead,
6 E-Notary Public in and for the Commonwealth of
7 Virginia.
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21 Agent, Baker Botts
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1 C O N T E N T S

2 EXAMINATION OF ANDREW WOLFE, Ph.D. PAGE
3 By Mr. Bemben 5
4 By Mr. Chandler 91
5 By Mr. Bemben 102
6
7 EXHIBITS MARKED IN TODAY'S SESSION
8 (None marked)
9
10 EXHIBITS MARKED IN PRIOR SESSIONS
11 (Not Attached)

12 DEPOSITION EXHIBIT PAGE
13 Exhibit 1001 25
14 Exhibit 1003 14
15 Exhibit 1005 34
16 Exhibit 1010 27
17 Exhibit 1039 24
18 Exhibit 1042 99
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22

1 P R O C E E D I N G S
2 ANDREW WOLFE, Ph.D.,
3 having been duly sworn, testified as follows: 11:57:42
4 EXAMINATION BY COUNSEL FOR PATENT OWNER 11:57:42
5 BY MR. BEMBEN: 11:57:42
6 Q Dr. Wolfe, please state your full name, 11:57:44
7 for the record. 11:57:46
8 A Andrew Wolfe. 11:57:47
9 Q You understand that you are under oath? 11:57:48
10 A I do. 11:57:52
11 Q Are you on any medication that would 11:57:52
12 impair your ability to give truthful testimony 11:57:57
13 today? 11:57:59
14 A No. 11:57:59
15 Q Is there any reason that you cannot give 11:57:59
16 truthful testimony today? 11:58:02
17 A No. 11:58:04
18 Q You've been deposed before. Correct? 11:58:04
19 A Yes. 11:58:07
20 Q Let's go over the ground rules. So I ask 11:58:08
21 that you provide verbal answers so that the 11:58:10
22 reporter can transcribe our conversation. Okay? 11:58:12

1 A Okay. 11:58:15
2 Q Let's try not to speak over each other, 11:58:16
3 and that's hard to do sometimes remotely. You 11:58:19
4 understand that I am here today to ask the 11:58:22
5 questions, and you are here to answer them. 11:58:24
6 Correct? 11:58:25
7 A Yes. 11:58:26
8 Q If you don't understand a question that I 11:58:26
9 ask please let me know, and I'll try to clarify 11:58:29
10 the question. Okay? 11:58:32
11 A Okay. 11:58:34
12 Q If you answer, I'm going to assume that 11:58:35
13 you understood my question. Is that fair? 11:58:37
14 A Okay. 11:58:39
15 Q We can take breaks about every hour. But 11:58:39
16 if you need a break just let me know, and I'll try 11:58:45
17 to finish up the line of questioning that I'm on 11:58:49
18 and we can take a break. Okay? 11:58:50
19 A Okay. 11:58:53
20 Q Also, I'm not here to play games with 11:58:54
21 you. This is not a memory contest for you. If 11:58:55
22 there is a document that you know of or that 11:58:58

1 you've reviewed that I haven't introduced yet and 11:59:00
2 you need it to access it please let me know, and 11:59:03
3 I'll introduce it so you can look at it. Okay? 11:59:05
4 A Okay. 11:59:08
5 Q This is a remote deposition. Correct? 11:59:08
6 A Yes. 11:59:12
7 Q Where are you? 11:59:12
8 A In my office in Santa Clara. 11:59:16
9 Q Is anyone with you? 11:59:18
10 A No. 11:59:20
11 Q What materials do you have with you, if 11:59:20
12 any? 11:59:25
13 A Well, I have my computer. I have all 11:59:26
14 kinds of materials, including all of the -- the 11:59:29
15 entire case file from the PTAB. I also have 11:59:34
16 printed copies of U.S. Patent 10,025,731, I have 11:59:41
17 Exhibit 1003, my declaration. I have the Abadeer 11:59:52
18 patent application, 2008/0218290. The Dour 12:00:00
19 patent, 7,020,818, and the Ellsberry application, 12:00:13
20 2006/0277355. 12:00:21
21 Q Any other materials printed that you have 12:00:29
22 with you? 12:00:32

1 A Those are all the printed materials. 12:00:33
2 Q And so the -- you mentioned a U.S. Patent 12:00:36
3 Number 10,025,731. And that's Exhibit -- that's 12:00:38
4 previously marked as Exhibit 1001 in this 12:00:43
5 proceeding. Correct? 12:00:46
6 A Yes. 12:00:47
7 Q And that's the '731 patent that we're 12:00:47
8 here to discuss today. Correct? 12:00:49
9 A Right. 12:00:51
10 Q And the -- you mentioned Abadeer patent 12:00:51
11 application. I believe that has been previously 12:00:57
12 marked as Exhibit 1039. 12:00:59
13 Is that right? 12:01:02
14 A Let me check. Those exhibit numbers get 12:01:07
15 cut off when I print them on eight and a half by 12:01:09
16 11. 12:01:13
17 Yes, that's Exhibit 1039. 12:01:14
18 Q And the Dour patent, that's Exhibit 1018. 12:01:15
19 Correct? 12:01:17
20 A Yes. 12:01:17
21 Q And Ellsberry is Exhibit 1005? 12:01:23
22 A Yes. 12:01:27

1 Q Now, the copies of all of those 12:01:27
2 references that you just mentioned that you have, 12:01:30
3 those are clean copies that you printed. Correct? 12:01:33
4 A As I said, they are exactly what I 12:01:38
5 downloaded off the PTAB site. 12:01:41
6 Q Okay. 12:01:44
7 A I have not noticed any markings on them. 12:01:45
8 Q You haven't added any markings on them? 12:01:47
9 A I have not added any markings, no. 12:01:49
10 Q Do you have any notes with you? 12:01:50
11 A No. No. I have -- there's one place 12:01:52
12 where I noticed a typo in the -- in Exhibit 1003, 12:01:57
13 so I just have a flag on it so that I can remember 12:02:03
14 to tell you about it. 12:02:06
15 Q So that's your declaration. Do you want 12:02:08
16 to, since you brought it up, do you want to just 12:02:09
17 tell me now? 12:02:13
18 A Sure. Page 82, Paragraph 125. By the 12:02:14
19 second sentence it should say, "I have compared 12:02:28
20 each and every limitation in Claims 1 through 18 12:02:31
21 to Grounds 1 and 2, and I have prepared a claim 12:02:34
22 chart showing why each and every limitation is 12:02:38

1 obvious in light of Grounds 1 and 2. See Exhibit 12:02:40
2 1093." 12:02:45
3 Q Got it. Okay. So Grounds 3 and 4 should 12:02:48
4 be Grounds 1 and 2, and the Exhibit 1095 should be 12:02:51
5 1093. Correct? 12:02:55
6 A Yes. 12:02:57
7 Q Got it. 12:02:57
8 A Yes. 12:02:58
9 Q Okay. Since we're doing this now, was 12:02:58
10 there anything else that you noticed that you 12:03:00
11 wanted to correct in your declaration? 12:03:02
12 A Not that I'm aware of. 12:03:05
13 Q So you understand that you're here to be 12:03:07
14 deposed in an IPR proceeding. Correct? 12:03:14
15 A Yes. 12:03:17
16 Q Are you aware that Netlist and Samsung 12:03:17
17 are involved in district court litigation 12:03:21
18 involving the '731 patent? 12:03:23
19 A I was not. 12:03:26
20 Q So you're not involved in that 12:03:26
21 litigation? 12:03:30
22 A Not as far as I know. 12:03:32

1 Q Are you aware that Netlist and Samsung 12:03:33
2 are involved in litigation at the International 12:03:35
3 Trade Commission involving the '731 patent? 12:03:38
4 A I am aware of that. 12:03:41
5 Q Are you involved in that ITC litigation? 12:03:42
6 A Not directly. Again, I don't know if 12:03:46
7 they've used any opinions in this IPR, but I have 12:03:50
8 not spoken to anybody with regard to that 12:03:53
9 litigation. 12:03:56
10 Q How did you come to be involved in this 12:03:57
11 IPR proceeding? 12:04:03
12 A My understanding is that there have been 12:04:05
13 a large number of ongoing disputes between Netlist 12:04:08
14 and Samsung. I was contacted about 12:04:11
15 four-and-a-half years ago to provide opinions on 12:04:13
16 some of them. And I've provided opinions on -- 12:04:15
17 with respect to a number of IPRs and I think some 12:04:19
18 reexams related to these. And, actually, a post 12:04:25
19 grant review as well, related to this portfolio 12:04:29
20 over the last four-and-a-half years. 12:04:31
21 Q How many IPRs and PGRs have you served as 12:04:33
22 an expert in, do you know roughly? 12:04:39

1 A Somebody had mentioned a number around 12:04:43
2 130 to me. 12:04:45
3 Q And that's -- is that -- strike that. 12:04:48
4 When did you start serving as an expert 12:04:52
5 in IPRs and PGRs? 12:04:54
6 A Probably within weeks after the IPR 12:04:58
7 process started. 12:05:00
8 Q I'm sorry, let me rephrase the question. 12:05:01
9 So when was the first time that you were an 12:05:02
10 expert, you served as an expert in an IPR 12:05:05
11 proceeding? 12:05:07
12 How long have you been doing this, 12:05:08
13 essentially? 12:05:09
14 A Again, I don't remember. But as soon 12:05:10
15 as -- I mean, I had been an expert in litigation 12:05:12
16 and ITC work. And as soon as IPRs started to -- 12:05:17
17 were approved under statute, I started to work on 12:05:23
18 those, too. 12:05:26
19 Q I see. 12:05:27
20 A I don't remember when that was. 12:05:27
21 Q So soon after the IPR proceedings became 12:05:28
22 available at the PTAB? 12:05:33

1 A Yes. 12:05:35
2 Q Did you prepare for this deposition? 12:05:35
3 A Yes. 12:05:43
4 Q What did you do? 12:05:43
5 A Well, specifically for this deposition I 12:05:47
6 reviewed the materials and then I met with counsel 12:05:50
7 twice. 12:05:52
8 Q Did you meet with -- when you say 12:05:55
9 "counsel," who are you referring to? 12:05:56
10 A Mr. Chandler and Mr. Pazmandi. 12:06:01
11 Q Did you meet with anyone other than Mr. 12:06:03
12 Chandler and Mr. Pazmandi? 12:06:06
13 MR. CHANDLER: And it's Dr. Pazmandi. 12:06:10
14 A Not to prepare for this deposition, no. 12:06:13
15 Q Did you meet with anyone other than 12:06:14
16 Mr. Chandler and Dr. Pazmandi in relation to this 12:06:21
17 IPR proceeding? 12:06:26
18 A No. 12:06:26
19 Q How long did you prepare for this 12:06:27
20 deposition? 12:06:31
21 A Well, again, there was a lot of 12:06:37
22 preparation that was not specifically for this 12:06:39

1 deposition; it was preparation in writing the 12:06:40
2 declaration. Some of these references I've been 12:06:45
3 working with for years. So specifically for this 12:06:48
4 deposition? I'm, you know -- after all the papers 12:06:55
5 have been filed, I'm not sure; but probably 12:07:03
6 somewhere around a dozen hours. 12:07:07
7 Q You have a copy of your declaration, but 12:07:10
8 let me officially entered it into the record. 12:07:16
9 MR. BEMBEN: So I'd like to provide a 12:07:19
10 copy of Exhibit 1003. This is the declaration of 12:07:20
11 Dr. Andrew Wolfe regarding U.S. Patent Number 12:07:25
12 10,025,731. This is previously marked. 12:07:30
13 (Exhibit 1003, previously marked, not 12:07:30
14 attached.) 12:07:32
15 Q Dr. Wolfe, you mentioned you have a copy. 12:07:32
16 Correct? 12:07:34
17 A I do. 12:07:35
18 Q And you obviously are familiar with this 12:07:35
19 document. This is your declaration. Correct? 12:07:38
20 A Yes. 12:07:41
21 Q So you mentioned that you spent time 12:07:41
22 preparing for the deposition, but also in 12:07:46

1 preparing the declaration? 12:07:50
2 A Yes. 12:07:50
3 Q With respect to preparing the 12:07:50
4 declaration, how much time did you spend? 12:07:52
5 A I don't know. And again, it's hard to 12:07:55
6 segregate it because some of these references I've 12:07:58
7 been working with for years and I've charted them 12:08:04
8 many times against many different kinds of things. 12:08:08
9 Q Can you ballpark it? 12:08:11
10 A Not really. Again, it's been spread over 12:08:13
11 a lot of time. There have been multiple patents 12:08:15
12 in the portfolio that I've been working on. So 12:08:18
13 just from memory, I can't sort it all out. 12:08:21
14 Q Did you write your declaration? 12:08:23
15 A I didn't write every word. I prepared 12:08:27
16 the declaration. I worked with counsel, and we 12:08:28
17 re-used some things that I prepared previously. 12:08:35
18 There were some cases where I described my 12:08:37
19 opinions to counsel and they did drafts, and then 12:08:39
20 I reviewed them and made sure they reflected what 12:08:44
21 I had told them. There were other cases where I 12:08:47
22 wrote text. 12:08:49

1 Q You mentioned Paragraph 125 already of 12:08:50
2 your declaration. 12:08:55
3 Can you turn to that, please. 12:08:56
4 A Sure. 12:08:58
5 Okay. 12:09:07
6 Q So in this paragraph you mention that you 12:09:07
7 prepared a claim chart. Correct? 12:09:23
8 A Yes. 12:09:28
9 Q And I noticed that following Paragraph 12:09:28
10 125 you address certain elements of Claim 1. 12:09:30
11 Is that correct? 12:09:35
12 A Yes. 12:09:35
13 Q And I noticed that you did not address 12:09:36
14 all of the elements of Claim 1. 12:09:39
15 Is that correct? 12:09:42
16 MR. CHANDLER: Objection. Form. 12:09:43
17 A Not in the declaration; I do in the claim 12:09:44
18 chart. 12:09:49
19 Q Okay. What is the relationship between 12:09:49
20 the declaration and the claim chart? 12:09:51
21 A One of the opinions and one of the 12:09:53
22 statements that I make in the declaration is that 12:09:57

1 I did do a complete analysis of the claim and 12:09:58
2 found it to be obvious. But it didn't seem 12:10:00
3 necessary for purposes of this proceeding for me 12:10:04
4 to opine on each and every element. But I did 12:10:07
5 want to provide the context and the evidence that 12:10:12
6 I had reviewed the entirety of the claim. So 12:10:15
7 that's the point of Exhibit 1093. 12:10:17
8 Q Is it your typical practice not to opine 12:10:21
9 on every element of a claim that you're 12:10:24
10 addressing? 12:10:26
11 MR. CHANDLER: Objection. Form. 12:10:26
12 A It depends on the venue and -- and the 12:10:28
13 situation. Some cases there just may be no need 12:10:33
14 for expert opinion on an element. 12:10:47
15 Q Is that the situation here? 12:10:48
16 A If I did opine on an element in the 12:10:49
17 declaration specifically, I didn't think there was 12:10:51
18 a need for expert opinion. But it doesn't mean 12:10:53
19 that I didn't find the element to be there. And 12:10:56
20 that's why I attached 1093. 12:10:59
21 Q Did you prepare Exhibit 1093? 12:11:00
22 (Exhibit 1093, previously marked, not 12:11:00

1 attached.) 12:11:00
2 A Yes; in a similar manner as the 12:11:05
3 declaration. 12:11:08
4 Q Did you choose which elements you would 12:11:08
5 address in the declaration? 12:11:14
6 A I consulted with counsel and went from -- 12:11:26
7 used counsel's guidance as to which ones they 12:11:29
8 thought needed expert testimony. 12:11:32
9 Q Did you agree that the elements that you 12:11:38
10 addressed in your declaration were the only ones 12:12:04
11 that required expert testimony? 12:12:06
12 A I didn't really have an opinion one way 12:12:10
13 or the other. They were writing the petition. 12:12:12
14 They were making the decision as to when they were 12:12:14
15 going to rely on an expert. And where they wanted 12:12:16
16 to rely on an expert, I provided my opinions. 12:12:20
17 Q And you said you have done this before, 12:12:23
18 is that correct, where you have only addressed 12:12:29
19 certain claim elements in a declaration? 12:12:31
20 A I can't remember a specific case, but I 12:12:36
21 think I have. I think in some cases I've written 12:12:38
22 a declaration that only addresses a single claim 12:12:40

1 element. 12:12:44
2 Q When you're functioning on the petitioner 12:12:44
3 side? 12:12:47
4 A I don't recall. 12:12:48
5 Q Let's go back to Paragraph 125. 12:12:48
6 A Okay. 12:12:57
7 Q So you have presented two grounds in this 12:12:57
8 declaration. 12:13:00
9 Is that correct? 12:13:00
10 A Yes. 12:13:01
11 Q Ground 1 is the combination of Ellsberry 12:13:01
12 and Dour. Correct? 12:13:08
13 A Correct. 12:13:09
14 Q And Ground 2 is the combination of 12:13:09
15 Ellsberry, Dour, and Abadeer? 12:13:14
16 A Correct. 12:13:16
17 Q I'm trying to understand the difference 12:13:17
18 between Grounds 1 and 2 with respect to Abadeer. 12:13:22
19 So what -- in your opinion, what does 12:13:24
20 Abadeer add to Ground 2 that Dour does not teach? 12:13:26
21 A So I believe Dour teaches embodiment -- 12:13:32
22 so I believe the Ellsberry-Dour combination 12:13:36

1 teaches embodiments that were within the scope of 12:13:40
2 all the claims. Dour teaches an adaptive 12:13:43
3 impedance matching circuit that adapts to a 12:13:49
4 certain set of things; like temperature or voltage 12:13:54
5 changes. 12:13:59
6 Abadeer teaches a more sophisticated one 12:14:01
7 that also adapts to changes in signal frequency. 12:14:04
8 So it is a more sophisticated solution. I think 12:14:09
9 they're both within the scope of the claims. 12:14:12
10 Q Let's walk through, can you take a look 12:14:14
11 at Paragraph -- starting in Paragraph 126. This 12:14:22
12 is where you address the preamble of Claim 1. 12:14:27
13 A Okay. 12:14:30
14 Q And for the preamble of Claim 1, Element 12:14:32
15 1.A, it appears that you're only relying on 12:14:36
16 Ellsberry. 12:14:38
17 Is that correct? 12:14:39
18 MR. CHANDLER: Objection. Form. 12:14:39
19 A Well, I'm always relying on these 12:14:41
20 combinations. But Ellsberry provides the teaching 12:14:43
21 of a memory module, or at least sufficient 12:14:48
22 teaching that we don't need to also look to the 12:14:53

1 secondary reference. 12:14:57
2 Q Just so that I'm clear, to address the 12:14:57
3 preamble, you're relying on Ellsberry. Correct? 12:14:59
4 A Well, as I said, I'm always relying on 12:15:05
5 the combination for the claim elements. But the 12:15:08
6 evidence that I cite is from Ellsberry for the 12:15:09
7 preamble. 12:15:14
8 Q I guess I don't understand what you mean 12:15:14
9 by that. You're always relying on the combination 12:15:16
10 for the claim elements. 12:15:18
11 What do you mean by that? 12:15:19
12 A So when I'm mapping the grounds, I am 12:15:22
13 mapping the combination of Ellsberry and Dour in 12:15:25
14 Claim 1, and the combination of three references 12:15:28
15 in Ground 2. There aren't -- there's not an 12:15:32
16 Ellsberry-only ground. But for an individual 12:15:36
17 element, I don't necessarily need to look to both 12:15:42
18 references to find sufficient evidence of the 12:15:44
19 teachings. 12:15:49
20 Q And for this element, Element 1.A, the 12:15:49
21 preamble, my question just is you're relying on 12:15:52
22 Ellsberry for this specific element. Correct? 12:15:56

1 MR. CHANDLER: Objection. Form. 12:15:58
2 A To illustrate the teachings of the 12:15:59
3 preamble, I have cited to Ellsberry. 12:16:03
4 Q Okay. And then moving on to Paragraph 12:16:06
5 128 of your declaration, Element 1.C, correct me 12:16:11
6 if I am wrong, but it also appears that you're 12:16:15
7 relying on Ellsberry to address this specific 12:16:16
8 limitation as well? 12:16:19
9 A For 1.C I have also cited to the evidence 12:16:21
10 in Ellsberry. 12:16:24
11 Q And then the next limitation you address 12:16:26
12 is 1.E.1. And this is starting in Paragraph 131 12:16:28
13 of your declaration. 12:16:32
14 Do you see that? 12:16:33
15 A I do. 12:16:34
16 Q And again, for Element 1.E.1 it appears 12:16:34
17 that you're relying on Ellsberry to teach the 12:16:40
18 specific limitation. 12:16:44
19 Is that correct? 12:16:45
20 A Yes, on 1.E.1 I cite to evidence in 12:16:49
21 Ellsberry for the teachings. 12:16:53
22 Q And then turning to Element 1.E.2, your 12:16:54

1 Paragraph 134, starting at 134. It appears that 12:17:01
2 for this element you're relying on all three 12:17:04
3 references, Ellsberry, Dour, and Abadeer. 12:17:08
4 Is that correct? 12:17:11
5 A Yes, just two of the references with 12:17:14
6 respect to the first ground, and all three 12:17:16
7 references with respect to the second ground. 12:17:17
8 Q Understood. And then for the next 12:17:21
9 limitation that you address, Element 1.F.2, 12:17:23
10 starting on Paragraph 137, do you see that? 12:17:27
11 A I do. 12:17:33
12 Q So to address Element 1.F.2, it appears 12:17:34
13 that you're relying on the combination of 12:17:37
14 Ellsberry and Dour. 12:17:38
15 Is that correct? 12:17:39
16 A I cite to Ellsberry and Dour for that 12:17:42
17 claim element. 12:17:45
18 Q And so for -- strike that. 12:17:45
19 Can you turn to Abadeer. 12:18:08
20 MR. BEMBEN: I'd like to introduce 12:18:10
21 Abadeer. This has been previously marked as 12:18:12
22 Exhibit 1039. 12:18:14

1 (Exhibit 1039, previously marked, not 12:18:17
2 attached.) 12:18:19
3 MR. BEMBEN: It is U.S. Patent 12:18:19
4 Application Publication 2008/0218290. We've been 12:18:22
5 referring to this as Abadeer. 12:18:30
6 Q Do you have that in front of you? 12:18:32
7 A I do. 12:18:33
8 Q And are you familiar with Abadeer? 12:18:33
9 A Yes. 12:18:37
10 Q You've read Abadeer and you understand 12:18:37
11 it? 12:18:42
12 A Yes. 12:18:42
13 Q Does Abadeer discuss ranks? 12:18:42
14 A I don't recall a discussion of rank in 12:19:11
15 Abadeer. That teaching comes from Ellsberry. 12:19:13
16 Q Abadeer does not discuss DRAM chips that 12:19:16
17 are arranged in ranks. Correct? 12:19:29
18 A Not that I recall. 12:19:40
19 Q So Abadeer does not discuss dynamically 12:19:42
20 controlling a programmable impedance-matching 12:19:44
21 circuit based on which rank is selected. Correct? 12:19:47
22 A Not in isolation, no. But in combination 12:19:53

1 with Ellsberry it does. 12:19:56
2 Q Let's turn to the '731 patent. 12:19:57
3 A Okay. 12:20:20
4 MR. BEMBEN: So I'd like to introduce 12:20:22
5 what has been previously marked as Exhibit 1001. 12:20:24
6 (Exhibit 1001, previously marked, not 12:20:28
7 attached.) 12:20:28
8 MR. BEMBEN: This is U.S. Patent 12:20:28
9 10,025,731. 12:20:31
10 Q Dr. Wolfe, have you seen this before? 12:20:33
11 A I have. 12:20:35
12 Q Are you familiar with the '731 patent? 12:20:35
13 A Yes. 12:20:39
14 Q You have read it and understand it? 12:20:39
15 A Yes. 12:20:43
16 Q Have you read all of the claims? 12:20:43
17 A Yes. 12:20:47
18 Q You understand the claims? 12:20:47
19 A I believe so, yes. 12:20:53
20 Q Let's start on the second page of the 12:20:54
21 patent. This is Page 2, Item 60. 12:21:09
22 Do you see where it talks about 12:21:14

1 provisional applications? 12:21:16
2 A Yes. 12:21:20
3 Q Do you agree that the '731 patent claims 12:21:21
4 priority to provisional applications that were 12:21:24
5 filed on April 14, 2008? 12:21:25
6 A It appears to make that claim. 12:21:31
7 Q Are you disputing that the '731 patent is 12:21:33
8 entitled to this 2008 priority date? 12:21:36
9 A Let me just take a quick look at my 12:21:41
10 declaration again. 12:21:45
11 I don't think I provided an opinion on 12:22:15
12 that. 12:22:20
13 Q When you formed your opinions regarding 12:22:21
14 obviousness, you understand that you must consider 12:22:23
15 the prior art from the perspective of a person of 12:22:25
16 skill in the art at the time of invention. Right? 12:22:27
17 A Yes. 12:22:29
18 Q Now, what did you use as the time of the 12:22:29
19 invention when you analyzed the '731 patent? 12:22:34
20 A I did use the April 2008 date, but it 12:22:38
21 would not have been any different if I had used a 12:22:42
22 2009 date. 12:22:45

1 Q You said you had electronic copies of 12:22:46
2 other exhibits in the record. Correct, Dr. Wolfe? 12:23:14
3 A Yes. I don't know if I have them all, 12:23:17
4 because there are a lot. But I have a lot. 12:23:19
5 Q Do you have access to an electronic copy 12:23:22
6 of Exhibit 1010? 12:23:25
7 A Yes. 12:23:30
8 MR. BEMBEN: So I'd like to introduce 12:23:31
9 what has been previously marked as Exhibit 1010. 12:23:34
10 (Exhibit 1010, previously marked, not 12:23:42
11 attached.) 12:23:43
12 Q It's JEDEC Standard No. 21-C DDR SDRAM 12:23:43
13 Registered DIMM Design Specification, that's on 12:23:43
14 the front page. 12:23:43
15 Do you see that, Dr. Wolfe? 12:23:54
16 A I do. 12:23:54
17 Q Are you familiar with this document? 12:23:54
18 A Yes; but there are many documents like 12:23:56
19 this, so I need to look at them very, very 12:23:58
20 carefully to make sure that I'm remembering the 12:24:01
21 right one. 12:24:05
22 Q This is one that was provided with your 12:24:06

1 declaration. And I believe that you mentioned it 12:24:08
2 in your exhibit list at the end of your 12:24:11
3 declaration. Correct? 12:24:13
4 A Correct. 12:24:15
5 Q So you've reviewed this document? 12:24:15
6 A I have. 12:24:20
7 Q At a high level, what does this document 12:24:20
8 describe, or what is this document? 12:24:24
9 A It describes both physical and electrical 12:24:29
10 standards for building a registered dual inline 12:24:35
11 memory module using certain DDR technologies. 12:24:42
12 Q Is it fair to say that this is a 12:24:51
13 specification for a memory module as opposed to 12:24:54
14 some of the other specifications in the record 12:24:59
15 that are for the DRAM chips themselves? 12:25:01
16 A That is generally the case, yes. 12:25:04
17 Q Can you go to Page 6 of Exhibit 1010? 12:25:06
18 A Okay. 12:25:13
19 Q And I'm look at Architecture Pin 12:25:14
20 Description. 12:25:23
21 Do you see that? 12:25:24
22 A Yes. 12:25:25

1 Q The pin description is the pins of the 12:25:25
2 DIMM itself. Correct? 12:25:34
3 A Yes. I mean, pin means something 12:25:36
4 specific in this context, but yes. 12:25:39
5 Q What does it mean in this context? 12:25:41
6 A It means a connection terminal, and in 12:25:50
7 the case of these products it is a copper or gold 12:25:53
8 strip on one side of the circuit board that 12:25:58
9 represents a connection. 12:26:03
10 Q And these are connections for the memory 12:26:04
11 module itself. Correct? 12:26:06
12 A Well, they're connections on the memory 12:26:10
13 module. If you connect it to something, then it's 12:26:13
14 a connection to the memory module. 12:26:15
15 Q And what do you connect the DIMM to? 12:26:17
16 A Usually to a DIMM socket, which would be 12:26:20
17 part of a host computer. 12:26:23
18 Q And in the host computer, how is the 12:26:25
19 memory accessed in the DIMM? 12:26:30
20 MR. CHANDLER: Objection. Form. 12:26:35
21 A That's a very broad question. 12:26:36
22 Q Is there typically a memory controller 12:26:37

1 that accesses the memory module? 12:26:40
2 A There would typically be one or more 12:26:44
3 memory controllers, yes. 12:26:46
4 Q And the memory controller sends commands 12:26:47
5 as well as other information using these pins. 12:26:51
6 Is that correct? 12:26:54
7 A Sends a variety of signals, and we would 12:26:56
8 typically classify some of those as commands. 12:26:58
9 Q Do you see the pin description Pin Name 12:27:00
10 S0 through S3? It's kind of in the middle of the 12:27:07
11 page? 12:27:13
12 A Yes, those are chip select lines. 12:27:14
13 Q What do you mean by "chip select lines"? 12:27:20
14 A You know, there's a detailed explanation 12:27:26
15 of their functionality throughout this document in 12:27:28
16 combination with the component documents. But at 12:27:32
17 a very high level, a chip select is sent as part 12:27:36
18 of the command to determine in this case which 12:27:39
19 bank of chips should receive and respond to the 12:27:49
20 command. 12:27:53
21 Q I see. And is it your opinion that -- 12:27:53
22 strike that. 12:27:57

1 And so in this, these S0 through S3, they 12:27:57
2 are used to select the physical banks 0, 1, 2, and 12:28:04
3 3? Am I reading that correct? 12:28:08
4 A Yes. If that many banks exist. 12:28:10
5 Q If that many banks exist. So, for 12:28:13
6 example, S0 would be used to select Bank 0. 12:28:16
7 Is that correct? 12:28:22
8 A That's probably arbitrary. But yeah, I 12:28:28
9 guess yeah, that's right, we'd probably just -- 12:28:30
10 various documents can say various things. But it 12:28:31
11 would be fair to just call whatever is selected by 12:28:34
12 S0 Bank 0 in operation. 12:28:37
13 Q Can you explain how the signals -- I'm 12:28:40
14 sorry, how the pins S0 through S3 are used to 12:28:44
15 select a bank? 12:28:48
16 MR. CHANDLER: Objection. Form. 12:28:51
17 A Not -- it's not in this document. It's 12:28:55
18 in other documents. But there are timing diagrams 12:28:58
19 that describe how those signals should be sent and 12:29:01
20 when they should be sent in order to select a 12:29:05
21 bank. And it -- you know, there are many 12:29:07
22 different bank configurations supported under this 12:29:09

1 standard. So there can be small differences. 12:29:12
2 Q And the system memory controller sends 12:29:20
3 signals to S0 through S3 to select a bank. 12:29:23
4 Correct? 12:29:26
5 MR. CHANDLER: Objection. Form. 12:29:28
6 A In a general sense. Now, in these 12:29:30
7 particular registered DIMMs they are sent to the 12:29:32
8 register. The register then generates another set 12:29:35
9 of signals, which are actually used to physically 12:29:37
10 select the bank. 12:29:40
11 Q I see. But they're sent from the memory 12:29:41
12 controller. Correct? 12:29:44
13 MR. CHANDLER: Objection. Form. 12:29:45
14 A They're sent to the DIMM. Ordinarily 12:29:47
15 they're sent from the memory controller, but there 12:29:51
16 could be other ways to do it. 12:29:55
17 Q How does the memory controller know how 12:29:57
18 many banks are on a memory module? 12:29:59
19 A I believe it gets that information by 12:30:09
20 reading a configuration from the serial PD. It 12:30:13
21 doesn't -- it doesn't literally know how many 12:30:20
22 banks there are, right, because of the possibility 12:30:22

1 of rank multiplication, but it knows how many 12:30:25
2 banks it thinks there are. 12:30:29
3 Q Okay. And can you explain what the 12:30:31
4 serial PD is that you just mentioned? 12:30:36
5 A It's a small read-only memory that's 12:30:38
6 provided on this particular family of DIMMs that 12:30:40
7 contains configuration information. 12:30:43
8 Q And that configuration information would 12:30:47
9 include how many banks are available? 12:30:49
10 A I think so. Again, I don't have that 12:30:52
11 spec in front of me. 12:30:54
12 Q So but the memory -- the memory 12:30:55
13 controller would use the signals -- strike that. 12:31:00
14 The memory controller would send signals 12:31:04
15 to the pins S0 to S3 to access a specific bank. 12:31:07
16 Is that right? 12:31:12
17 MR. CHANDLER: Objection. Form. 12:31:13
18 A Again, it's what it thinks is a specific 12:31:14
19 bank. The DIMM itself through the register can 12:31:16
20 have a different number of physical banks than -- 12:31:22
21 than it's representing to the memory controller. 12:31:26
22 Q Can you pull out the Ellsberry reference. 12:31:34

1 A Sure. 12:32:13
2 MR. BEMBEN: And so I'd like to introduce 12:32:14
3 what has been previously marked as Exhibit 1005. 12:32:16
4 This is U.S. Patent Application Publication 12:32:20
5 2006/0277355. 12:32:24
6 (Exhibit 1005, previously marked, not 12:32:27
7 attached.) 12:32:27
8 Q Dr. Wolfe, are you familiar with 12:32:27
9 Ellsberry? 12:32:31
10 A Yes. 12:32:34
11 Q You read Ellsberry and you understand it? 12:32:35
12 A Yes. 12:32:38
13 Q Can you turn to Paragraph 23 of 12:32:38
14 Ellsberry? 12:32:47
15 A Okay. 12:33:03
16 Q Do you see where it says in Paragraph 23, 12:33:04
17 "The term 'memory device' refers to any device 12:33:08
18 capable of storing information, including DRAM"? 12:33:10
19 A Yes, that is the way that it is used in 12:33:15
20 Ellsberry. 12:33:18
21 Q Does that definition of memory device 12:33:18
22 align with your understanding of memory device in 12:33:22

1 this case? 12:33:26
2 MR. CHANDLER: Objection. Form. 12:33:26
3 A No. I think -- I think the '731 patent 12:33:29
4 describes it in a narrower sense. 12:33:36
5 Q How so? 12:33:38
6 A Let me pull it up. 12:33:40
7 I don't recall any descriptions beyond 12:34:19
8 DRAM in the '731. And also, in context in the 12:34:23
9 '731, I think specification describes memory 12:34:33
10 device as being a chip. And that's reinforced in 12:34:36
11 Column 5, Lines 20 and 21, where it says that the 12:34:41
12 memory module includes a plurality of memory 12:34:46
13 devices on the printed circuit board. 12:34:48
14 So the memory device is, at least in the 12:34:52
15 only embodiment that I see described, are things 12:34:56
16 that can be placed on the printed circuit board. 12:34:59
17 Q Claim 1 of the '731 patent recites the 12:35:04
18 term "memory device." Correct? 12:35:18
19 A Yes. And again, in one case, if we look 12:35:23
20 at the Column 17, Line 1, again it's a plurality 12:35:27
21 of memory devices on the printed circuit board. 12:35:32
22 Q And so just to make sure I'm 12:35:34

1 understanding, your understanding of memory device 12:35:36
2 as it's recited in Claim 1 is that it has to be a 12:35:37
3 chip. 12:35:41
4 Is that right? 12:35:41
5 MR. CHANDLER: Objection to form. 12:35:42
6 A No. I think it has to be a device that 12:35:45
7 can be mounted on a printed circuit board. At 12:35:49
8 least the most natural reading of both 12:35:52
9 specification and the claims is that it refers to 12:35:56
10 the entirety of the device that would be mounted 12:35:58
11 on the printed circuit board. 12:36:00
12 Q And the basis for that opinion is you 12:36:01
13 said Column 17, Line 1? 12:36:13
14 Is that right? 12:36:15
15 A No. Again, I think that's my -- I think 12:36:17
16 that's the most reasonable understanding of what's 12:36:23
17 being described in the specification as a whole. 12:36:25
18 But it's also consistent with Column 5, Lines 20 12:36:27
19 and 21 and Column 17, Line 1. 12:36:30
20 So for purposes of my opinions, it's 12:36:36
21 sufficient to determine that that's within the 12:36:39
22 scope of the claim, because that's what was in the 12:36:43

1 prior art. 12:36:47
2 Q When I asked you if your understanding of 12:36:51
3 a memory device as it's recited in Claim 1 is that 12:37:26
4 it has to be a chip, you responded, No; I think it 12:37:30
5 has to be a device that can be mounted on a 12:37:34
6 printed circuit board. 12:37:36
7 Do you recall that answer? 12:37:37
8 A Yes. 12:37:38
9 Q When you -- when you said "on a printed 12:37:38
10 circuit board," are you interpreting "on" to be 12:37:43
11 mounted directly on? 12:37:49
12 A Certainly that's what was in the prior 12:37:59
13 art. I hadn't really considered any other 12:38:03
14 alternatives. 12:38:13
15 I mean, generally the plain meaning of 12:38:21
16 mounting something on a printed circuit board is 12:38:25
17 to solder it to the printed circuit board. And I 12:38:28
18 didn't see a description of anything else in the 12:38:31
19 '731 patent. 12:38:33
20 Q Can you go to your declaration, turn to 12:38:48
21 your declaration. Let's take a look at Paragraph 12:39:11
22 88. 12:39:30

1 A Okay. 12:39:44
2 Q Do you see where you refer to something 12:39:44
3 called DFE? 12:39:54
4 A Yes. 12:39:56
5 Q What is DFE? 12:39:56
6 A I don't remember exactly what it stands 12:40:00
7 for. It's an equalizer that's used in certain 12:40:02
8 modern DRAM configurations. 12:40:05
9 Q Do you see where you say, ODT? 12:40:10
10 A Yes. 12:40:12
11 Q What is ODT? 12:40:12
12 A On die termination. 12:40:16
13 Q And so is it your understanding that in 12:40:17
14 DDR5 DRAM chips include both DFE and ODT 12:40:22
15 circuitry? 12:40:27
16 MR. CHANDLER: Objection. Outside the 12:40:27
17 scope of the direct testimony. 12:40:28
18 A I'd have to look back at the 12:40:41
19 specification. 12:40:42
20 Q The specification of what? 12:40:42
21 A The DDR5. 12:40:45
22 I suspect that it does, but I don't 12:40:56

1 recall for certain. 12:40:59
2 Q So DFE, I believe it's decision feedback 12:41:00
3 equalizer. 12:41:04
4 Does that sound right to you? 12:41:05
5 A Something like that. 12:41:06
6 Q Do you know whether -- strike that. 12:41:07
7 Are you aware that DFE circuitry in DRAM 12:41:17
8 chips was introduced in DDR5? 12:41:20
9 A That's the first place I'm aware of 12:41:27
10 seeing the term, but I don't know if it appeared 12:41:30
11 in any place earlier. 12:41:32
12 Q So as far as you understand, before DDR5, 12:41:33
13 DRAM chips did not include DFE. 12:41:36
14 Is that right? 12:41:39
15 A I'm not aware of that specific term being 12:41:40
16 used before DDR5. 12:41:45
17 Q Okay. Can you turn to Paragraph 89 of 12:41:46
18 your declaration. 12:41:56
19 A Yes. 12:41:56
20 Q Do you see where you say "Netlist's 12:41:56
21 apparently broad construction"? 12:42:05
22 A Yes. 12:42:08

1 Q What did you mean by that? 12:42:08
2 A Again, it's just my understanding that in 12:42:11
3 the ITC Netlist has suggested that -- that the 12:42:15
4 memory device does not need to be a chip or module 12:42:24
5 on the printed circuit board. But that would be a 12:42:30
6 broadening of the claim. I don't think anybody 12:42:34
7 has suggested that the memory device cannot be a 12:42:35
8 chip on the printed circuit board. 12:42:39
9 So given that, my obviousness opinions 12:42:42
10 apply under either construction. 12:42:45
11 Q When you said your understanding is that 12:42:47
12 in the ITC Netlist suggested that construction, 12:42:59
13 did you mean the district court case? 12:43:05
14 A I may have misunderstood, but I thought 12:43:07
15 that what I was told was that these came from the 12:43:09
16 ITC. But I may have misunderstood. 12:43:12
17 Q I think in Paragraph 88 of your 12:43:17
18 specification -- sorry. In Paragraph 88 of your 12:43:19
19 declaration you cite to Exhibit 1044 and 1045. It 12:43:21
20 is district court -- 12:43:28
21 A Yeah. 12:43:30
22 Q Before I thought that you mentioned you 12:43:30

1 hadn't spoken to anyone about the ITC proceeding. 12:43:36
2 Is that right? 12:43:38
3 A I have not. I have not. Yeah. All I -- 12:43:39
4 all that was communicated to me is what's in 12:43:44
5 Paragraph 88. 12:43:45
6 Q Gotcha. Okay. 12:43:46
7 And so do you understand that Netlist's 12:43:49
8 position in the district court case is that the 12:43:51
9 memory cores in the DDR5 DRAM chip are a memory 12:43:54
10 device, as that claim is used in Claim 1 of the 12:43:59
11 '731 patent? 12:44:04
12 A That's what I was told. 12:44:04
13 Q And do you agree with that position? 12:44:05
14 A As I said, I don't think that's the 12:44:09
15 ordinary meaning that I see in the '731 patent. 12:44:11
16 But it doesn't impact my opinions in this 12:44:14
17 declaration one way or the other. 12:44:19
18 Q To you what is the plain and ordinary 12:44:21
19 meaning of "memory device" as that term is used in 12:44:22
20 Claim 1 of the '731 patent? 12:44:25
21 A Well, I said it's a complete device that 12:44:27
22 can be mounted on the printed circuit board, that 12:44:30

1 is mounted on the printed circuit board. 12:44:34
2 Q Did you provide that construction 12:44:36
3 anywhere in your declaration? 12:44:58
4 A No; because as I said, under any 12:45:01
5 reasonable construction, I think that the prior 12:45:04
6 art that I've cited renders the claims obvious. 12:45:07
7 Q Let's go back to Ellsberry. And can you 12:45:12
8 turn to Paragraph 27 of Ellsberry? 12:46:01
9 A Sure. Give me a minute. 12:46:03
10 Okay. 12:46:28
11 Q Do you see about two-thirds of the way 12:46:28
12 down there's a sentence, "Thus, the 12:46:36
13 capacity-expanding memory device 108 is compatible 12:46:39
14 with existing system architectures and transparent 12:46:42
15 to the rest of the system (e.g., microprocessor, 12:46:45
16 operating system, et cetera.)"? 12:46:51
17 A Yes. 12:46:53
18 Q What does Ellsberry mean that the 12:46:54
19 capacity-expanding memory device is transparent to 12:46:57
20 the rest of the system? 12:47:00
21 A It means that the system cannot tell 12:47:04
22 logically or electrically that there is ranked 12:47:11

1 multiplication going on, because there's an 12:47:17
2 intermediate circuit that isolates the multiple 12:47:21
3 memory banks from the memory controller and 12:47:24
4 performs all of the translations that -- that take 12:47:25
5 place. 12:47:27
6 Now, when you take that in the entirety 12:47:28
7 of the context of Ellsberry, what you understand 12:47:32
8 is it's a little bit more sophisticated than that. 12:47:36
9 That the memory-expanding module -- or the 12:47:47
10 memory-expanding device, capacity-expanding memory 12:47:51
11 device, will have an additional cycle of latency. 12:47:55
12 But that's within the standards. 12:48:06
13 So it's perfectly fine to just represent 12:48:10
14 to the memory controller that you're a DIMM with a 12:48:15
15 different latency than the memory chips that are 12:48:19
16 actually on the DIMM. That there's rank 12:48:22
17 multiplication going on. 12:48:25
18 Q Does that theory that you just mentioned 12:48:25
19 have anything to do with the transparent -- the 12:48:41
20 transparency that's described in Paragraph 27? 12:48:43
21 A In some sense. The memory DIMM will say 12:48:46
22 that it has a certain latency. Let's say 12:48:54

1 hypothetically five. And the host memory 12:48:57
2 controller doesn't need to be concerned as to 12:49:03
3 whether or not it's a rank multiplied memory with 12:49:05
4 a latency of five built around chips with a 12:49:09
5 latency of four, or it's a nonranked multiplied 12:49:13
6 memory with a latency of five built around chips 12:49:17
7 that have a latency of five, or within the spec 12:49:21
8 you could actually have a nonrank multiplied 12:49:24
9 memory module with a latency of five that has 12:49:28
10 chips with a latency of four. You don't have to 12:49:35
11 represent the fastest possible speed of your chips 12:49:37
12 to the host memory controller, just what you 12:49:43
13 expect the operating latency to be. 12:49:47
14 Q I see. And you believe that hiding the 12:49:54
15 latency is part of the transparency that's 12:49:56
16 described in Paragraph 27? 12:49:59
17 Is that right? 12:50:00
18 A It's one of the factors that allows for 12:50:04
19 transparency. 12:50:07
20 Q You also mentioned in your answer, one of 12:50:08
21 your previous answers about translations, 12:50:13
22 performing translations. 12:50:15

1 Do you recall that? 12:50:17
2 A Sure. 12:50:19
3 Q You said that there's an intermediate 12:50:20
4 circuit that performs all the translations. 12:50:23
5 What did you mean by that? 12:50:28
6 A Takes the addresses and chip select 12:50:33
7 signals coming into the DIMM, and it produces a 12:50:36
8 new set of address and chip select signals for the 12:50:40
9 individual ranks. 12:50:46
10 Q So you're talking about memory 12:50:48
11 translations. 12:50:50
12 Is that right? 12:50:51
13 A Signal translations of address and 12:50:55
14 control signals. 12:50:56
15 Q Okay. Is that described somewhere in 12:50:58
16 Ellsberry? 12:51:02
17 A I don't know if it just is in one place, 12:51:03
18 but it's kind of the whole -- it's the entirety of 12:51:05
19 the -- of the teachings. But I will tell you one 12:51:08
20 place where that is particularly illustrative -- 12:51:12
21 and again, there are multiple modes. But -- but 12:51:21
22 Figure 8 in its various parts shows some of that 12:51:34

1 operation. 12:51:39
2 Q Figure 8 shows what operation? 12:52:10
3 A Columns A, B, and C show what the memory 12:52:13
4 controller sends. And Column -- Column D is also 12:52:24
5 from the memory controller. Column E and F is 12:52:33
6 what the switch chip sends to one of the ranks, 12:52:40
7 and Columns G and H are what the memory switch 12:52:46
8 will send to the other rank in this particular 12:52:54
9 embodiment. 12:52:58
10 Q The answer that you just gave when you 12:52:59
11 mentioned "memory switch," are you referring to 12:53:12
12 the switch ASICs that are in Figure 2 of 12:53:15
13 Ellsberry? 12:53:18
14 MR. CHANDLER: Objection. Form. 12:53:19
15 A Yes. And also the circuit that's shown 12:53:37
16 in Figure 3. 12:53:40
17 Some of it's done by the control ASIC as 12:53:46
18 well, 204. 12:53:49
19 Q And just for the record, when we say 12:53:50
20 ASIC, yeah, A-S-I-C. ASIC stands for 12:53:54
21 application-specific integrated circuit. 12:54:01
22 Right, Dr. Wolfe? 12:54:04

1 A Traditionally, yes. 12:54:06
2 Q Is that how it's being used here in 12:54:06
3 Ellsberry? 12:54:09
4 A I think so. 12:54:09
5 Q And so just getting back to Figure 8, you 12:54:10
6 said that the information in Columns A, B, and -- 12:54:13
7 A, B, C and D are coming from the memory 12:54:18
8 controller? 12:54:21
9 Is that right? 12:54:21
10 A Yeah. I'm not sure about -- the column 12:54:22
11 numbering is a little weird here, so I'm just 12:54:26
12 calling the first one A. 12:54:29
13 Q So the first four columns? 12:54:29
14 A I'm sorry, I missed that. 12:54:34
15 Q The first four columns. 12:54:36
16 A Yeah, I believe those are coming from the 12:54:39
17 memory controller. 12:54:41
18 Q And then the next two columns would be 12:54:42
19 coming from the switch ASIC? 12:54:46
20 A I think in particular these -- those -- 12:54:50
21 let me look. Those are going to come from the 12:54:55
22 control ASIC. 12:55:02

1 Q So the first four columns in Figure 8 are 12:55:03
2 coming from the memory controller. Right? 12:55:17
3 MR. CHANDLER: Objection. Form. 12:55:21
4 Q And the next four columns -- I'm sorry. 12:55:23
5 Dr. Wolfe, did you answer that question? Let me 12:55:27
6 repeat the question. 12:55:30
7 The first four columns in Figure 8 are 12:55:31
8 coming from the memory controller. Correct? 12:55:33
9 MR. CHANDLER: Objection. Form. 12:55:35
10 A Or whatever's connected to the DIMM 12:55:36
11 interface. 12:55:38
12 Q I think you used memory controller. Is 12:55:39
13 there something else that would be connected to 12:55:44
14 the DIMM interface? 12:55:46
15 A It would typically be a memory 12:55:47
16 controller. But again, you can use all kinds of 12:55:50
17 things to connect to a memory. 12:55:52
18 Q But it's coming from something external 12:55:55
19 to the DIMM interface? 12:55:57
20 MR. CHANDLER: Objection. Form. 12:55:59
21 A Yeah. Yes. 12:56:00
22 Q And then the next four columns in Figure 12:56:01

1 8 are coming from the control ASIC on the memory 12:56:06
2 module. 12:56:10
3 Is that correct? 12:56:11
4 A One or more control ASICs. They are 12:56:12
5 illustrated as two in Figure 2. 12:56:16
6 Q So that's Figure 8 of Ellsberry. Can you 12:56:25
7 go to Paragraph 37 of Ellsberry? 12:56:29
8 A Okay. 12:56:31
9 Q Paragraph 37 Ellsberry discusses Figures 12:56:54
10 7A through F. Right? 12:57:01
11 A Yes. 12:57:04
12 Q And I believe earlier you talked about 12:57:04
13 address translation. 12:57:07
14 Do you recall that? 12:57:09
15 A Yes. 12:57:13
16 Q Is Paragraph 38 of Ellsberry describing 12:57:13
17 that address translation that you were talking 12:57:16
18 about? 12:57:20
19 A Paragraph 37? 12:57:21
20 Q Yes. 12:57:22
21 A For a variety of different embodiments it 12:57:24
22 does. 12:57:26

1 Q Can you explain to me how Ellsberry's 12:57:26
2 address mapping table works in Figure 7? 12:57:31
3 A It's different for each embodiment. 12:57:35
4 Pretty much every row represents a different 12:57:38
5 embodiment. 12:57:41
6 Q Can you just -- maybe the first row in 12:57:41
7 Figure 7A. 12:57:44
8 A So that's not one that I'm relying on 12:57:45
9 because that's based on a column mode, and I've 12:57:48
10 relied on the row mode for the row and bank mode. 12:57:54
11 Q Okay. Can you select one that you have 12:57:59
12 relied on and let me know which one? 12:58:01
13 A I think the last one on 7A is 12:58:18
14 representative. 12:58:20
15 Q Okay. Can you explain to me how -- what 12:58:22
16 that row is showing? 12:58:26
17 A Sure. Bank address comes in. On this 12:58:28
18 particular embodiment the bank address can 12:58:39
19 actually be sent to each of the ranks. And again, 12:58:41
20 only the address translation is here. There are 12:58:46
21 some chip select signal generations and command 12:58:48
22 generations that have to happen concurrently. 12:58:52

1 The column address is also sent along. 12:58:57
2 But it's the row address that's used for rank 12:59:02
3 multiplication here. And the bit, I believe 13, 12:59:05
4 yeah, Bit 13 of the row address is used to select 12:59:18
5 between the two ranks. So if Bit 13 is a zero, 12:59:22
6 one of the ranks is selected. And if Bit 13 is a 12:59:30
7 one, the other rank is selected. 12:59:33
8 Q So we're talking about the third row in 12:59:35
9 Figure 7A. Correct? 12:59:42
10 A Yes. 12:59:44
11 Q And in the column Primary Address Space 12:59:44
12 for the third row, what does primary address space 12:59:49
13 mean? 12:59:54
14 A It refers to the way that addresses are 12:59:55
15 going to be provided to the DIMM. 12:59:58
16 Q And what are those addresses being 13:00:04
17 provided by? 13:00:08
18 A Again, commonly a memory controller. 13:00:09
19 Q And in the last column of Figure 7A it 13:00:12
20 says, "secondary address space." 13:00:15
21 Do you see that? 13:00:17
22 A Yes. 13:00:18

1 Q What does that mean? 13:00:18
2 A That describes the two different ranks 13:00:19
3 that are going to be provided with remapped 13:00:21
4 addresses. Again, specifically for this 13:00:26
5 embodiment. 13:00:39
6 MR. BEMBEN: Dr. Wolfe, we've been going 13:00:55
7 for about an hour. Would you like to take a break 13:00:58
8 or would you like to keep going? 13:01:00
9 THE WITNESS: Why don't we take a break. 13:01:02
10 MR. BEMBEN: How long would you like? 13:01:03
11 THE WITNESS: Five minutes is fine. 13:01:06
12 MR. BEMBEN: Okay. Let's go off the 13:01:07
13 record and be back at five after. 13:01:09
14 (A recess was taken.) 13:01:14
15 BY MR. BEMBEN: 13:08:20
16 Q Dr. Wolfe, can you turn to Figure 2 of 13:08:22
17 Ellsberry. 13:08:25
18 A Okay. 13:08:31
19 Q We already talked a little bit about that 13:08:31
20 control ASIC 204. I want to understand a little 13:08:34
21 more about it. 13:08:38
22 So that control ASIC 204 receives address 13:08:39

1 and commands signals via the DIMM interface 202. 13:08:42
2 Is that right? 13:08:50
3 A It does. 13:08:50
4 Q And those address and command signals are 13:08:51
5 sent by a host that's external to the DIMM. 13:08:56
6 Is that correct? 13:08:59
7 A That would be common. 13:09:01
8 Q And that could be a memory controller? 13:09:03
9 A It could be. 13:09:06
10 Q After the control ASIC receives the 13:09:06
11 memory and it -- strike that. 13:09:12
12 After the control ASIC receives the 13:09:13
13 memory addresses and commands from the host 13:09:15
14 controller, it buffers the memory addresses and 13:09:18
15 commands in a register. 13:09:20
16 Is that right? 13:09:21
17 MR. CHANDLER: Objection. Form. 13:09:23
18 A That's one of the things that it does. 13:09:34
19 Q If we turn to Paragraph 108 of your 13:09:36
20 declaration. 13:09:41
21 A Okay. 13:10:04
22 Q I believe you refer to the control ASIC 13:10:04

1 as a register. 13:10:08
2 Is that correct? 13:10:09
3 MR. CHANDLER: Objection. Form. 13:10:11
4 A I think I'm referring to the traditional 13:10:41
5 RDIMM as the register. Ellsberry has the control 13:10:44
6 ASIC and a corresponding position. 13:10:47
7 Q You say, As well as additional 13:10:53
8 functionality in the register, open paren, gray, 13:11:11
9 which Ellsberry calls the control ASIC. 13:11:14
10 Do you see that? 13:11:15
11 A Right. So in other words, where the 13:11:20
12 RDIMM had a register, Ellsberry replaces that with 13:11:24
13 a register plus additional functionality. 13:11:29
14 Q Can you turn back to Ellsberry Figure 5. 13:11:51
15 A Okay. 13:12:38
16 Q So Figure 5 of Ellsberry shows a DIMM. 13:12:38
17 Is that right? 13:12:44
18 A I'm sorry, I missed a word there. 13:12:46
19 Q Figure 5 of Ellsberry shows a DIMM? 13:12:47
20 A Yes. Not a standard DIMM, but an 13:12:53
21 Ellsberry DIMM. 13:12:56
22 Q The DIMM includes two rows of DDR2 DRAM 13:12:57

1 chips. Right? 13:13:04
2 A Physically it does, yes. Well, on the 13:13:05
3 front side. There's probably two more on the back 13:13:08
4 side. I don't remember. 13:13:15
5 Q All right. But two rows are shown on the 13:13:17
6 side that we see in Figure 5. Correct? 13:13:20
7 A Yes. 13:13:22
8 Q What dimensions of the DIMM in Figure 13:13:22
9 5 -- what are the dimensions of the DIMM shown in 13:13:30
10 Figure 5? 13:13:32
11 A Like length, width, and depth? 13:13:40
12 Q Yes. 13:13:42
13 A Let me look. I don't remember. It 13:13:43
14 really was not critical to my opinion. 13:13:49
15 I'm not seeing that disclosed at the 13:14:11
16 moment. 13:14:13
17 Q What would you expect the dimensions of a 13:14:16
18 DIMM that has DDR2 chips on it to be? 13:14:18
19 A Well, again, I don't know that it 13:14:28
20 matters. Again, there's nothing that limits 13:14:30
21 Ellsberry to being in a standard form factor. But 13:14:37
22 if it were, I would expect the width to correspond 13:14:42

1 to the DDR2 DIMM standard and the thickness to 13:14:54
2 correspond to the DDR2 DIMM standard. But the 13:15:04
3 height might or might not; it might be taller. 13:15:09
4 Q What would the height of a DIMM in the 13:15:18
5 DDR2 standard be? 13:15:22
6 A I don't have the DDR2 standard in front 13:15:27
7 of me. 13:15:30
8 Q Do you have a ballpark? 13:15:30
9 A My recollection, somewhere in the 13:15:39
10 ballpark of 35 millimeters, but I don't remember 13:15:42
11 if that's a typical or a restriction. 13:15:46
12 Q And Figure 5 of Ellsberry shows memory 13:15:49
13 bank switches 508. Correct? The D? 13:16:01
14 A Yes. 13:16:37
15 Q Is it your understanding that the memory 13:16:38
16 bank switches are connected to the DRAM chips in 13:16:43
17 Figure 5? 13:16:49
18 A Yeah, certain connections would be 13:16:56
19 connected to the DRAM chips, yes. 13:16:57
20 Q Which connections? 13:16:59
21 A It would be similar to what's illustrated 13:17:02
22 in Figure 2. It would be data, pins, some 13:17:04

1 strobes, and in the DM pins, which I think are 13:17:14
2 masks. 13:17:29
3 Q Is it your understanding that in Figure 5 13:17:29
4 of Ellsberry the bank switch 508 is connected to 13:17:33
5 both DRAM Chip 512 and DRAM Chip 504? 13:17:36
6 A I don't see 504. Oh. Oh. Oh. Oh, no, 13:17:45
7 I see it. Right. Sorry. There are a bunch of 13:17:52
8 512s all over the place. 13:17:56
9 Yes; not using the same wires. But yes. 13:18:02
10 Q And so those, as mentioned, DRAM Chip 504 13:18:04
11 and DRAM Chip 512 connected to Bank Switch 508, 13:18:22
12 there's other DRAM chips in other bank switches on 13:18:28
13 the memory module Figure 5 that are not labeled. 13:18:32
14 Correct? 13:18:35
15 A They're not labeled with drawing numbers, 13:18:37
16 correct. 13:18:40
17 Q Right, with drawing numbers. 13:18:41
18 Is it your understanding that the other 13:18:43
19 DRAM chips that are above the memory bank switch 13:18:46
20 would be connected to the memory bank switch? 13:18:50
21 MR. CHANDLER: Objection. Form. 13:18:57
22 A It operates as a rank. It always works 13:19:01

1 at the full width of the DIMM, so -- 13:19:03
2 Q I guess -- 13:19:07
3 A -- in this case that would be nine chips 13:19:09
4 wide. 13:19:11
5 So the nine top chips are connected to 13:19:12
6 the nine switch chips, and the nine middle chips 13:19:14
7 are connected to the nine switch chips through 13:19:18
8 separate ports. 13:19:21
9 Q I guess I'm just trying to understand 13:19:21
10 which of the DRAM chips are connected to which of 13:19:28
11 the bank switches 508, or how you understand that? 13:19:31
12 A Again, I don't think it's restrictive; 13:19:37
13 it's only meant to be illustrative. But I think 13:19:39
14 the first D would connect to the two chips on the 13:19:42
15 left, and the next D would connect to the next two 13:19:48
16 chips, and the next D would connect to the next 13:19:50
17 two chips. But they all operate in lockstep. 13:19:54
18 Q And the wire length of the wire that 13:20:02
19 connects from the bank switch 508 to 512, how long 13:20:09
20 would that be? 13:20:13
21 A Oh, I don't know exactly. Somewhere in 13:20:17
22 the neighborhood of 15 millimeters. Again, I 13:20:20

1 mean, it's got to be routed, so it's nontrivial, 13:20:25
2 but somewhere in that ballpark. 13:20:31
3 Q What is the ballpark of the length of the 13:20:33
4 wire that connects 508 to 504? 13:20:36
5 A Ballpark, twice that. 13:20:39
6 Q So 30 millimeters? 13:20:42
7 A Somewhere in that range. Again, there's 13:20:44
8 going to be some variation. 13:20:50
9 Q All right. Can we go to Paragraph 128 of 13:20:58
10 your declaration. 13:21:09
11 A Sure. 13:21:33
12 Q Do you see the bracketed section that 13:21:33
13 spans Pages 85 through 86 of your declaration? 13:21:36
14 A That starts, "e.g."? 13:21:43
15 Q Yeah. "E.g., memory devices 1310"? 13:21:44
16 A Yes. 13:21:48
17 Q Okay. Here you say that the memory 13:21:48
18 devices in Figure 13 of Ellsberry correspond to 13:21:55
19 four ranks. 13:21:58
20 Do you see that? 13:22:17
21 A I see that. 13:22:38
22 Q Can you explain to me why you believe 13:22:40

1 that Figure 13 of Ellsberry shows four ranks? 13:22:41
2 MR. CHANDLER: Objection. Form. 13:22:52
3 A In Figure 13, which is not the one that I 13:22:57
4 relied on, I don't think, for -- well, this is 13:22:59
5 Figure 13. 13:23:11
6 Figure 13 shows an embodiment where each 13:23:13
7 rank is eight bits wide. 13:23:16
8 Q Did you finish? 13:23:43
9 A And each of those ranks has an 13:23:49
10 independent select signal coming out of the 13:23:54
11 control unit ASIC. That's it. 13:23:58
12 Q So isn't the fact that there's an 13:24:09
13 independent select signal coming out of control 13:24:18
14 ASIC that dictates that there are four ranks? 13:24:22
15 A That's one factor. But the other factor 13:24:27
16 is that each rank is defined by the fact that it 13:24:29
17 can independently provide the full width of the 13:24:33
18 DIMM, which in this case is eight bits. 13:24:36
19 Q Is it your opinion that in Ellsberry a 13:24:38
20 bank is the same as the claimed rank? 13:25:26
21 A By claimed rank you mean the rank claimed 13:25:36
22 in '731? 13:25:39

1 Q Yes. 13:25:40
2 A Yes, Ellsberry essentially explains 13:25:41
3 that -- that there -- it was written at a time 13:25:46
4 where those terms were often used interchangeably, 13:25:52
5 and that he's not distinguishing between a rank 13:25:58
6 and a bank in his teachings. 13:26:01
7 Q Where does Ellsberry explain that? 13:26:02
8 A I don't recall. Let me see. So I guess 13:26:17
9 he doesn't come out and say it in so many words. 13:26:37
10 But what he refers to as a bank, he then cites to 13:26:40
11 the JEDEC standards, and the JEDEC standards 13:26:43
12 sometimes use the term "rank" for the same thing. 13:26:47
13 And I believe I cited to some third-party 13:26:50
14 contemporaneous teachings, as well as my own 13:26:52
15 knowledge from the time in my declaration, that 13:26:59
16 explain why that is. 13:27:01
17 But essentially this was all during a 13:27:02
18 transition period in which those two terms were 13:27:07
19 often used interchangeably. And even within the 13:27:12
20 JEDEC standards they would replace the phrase 13:27:15
21 "bank" with "rank" from one standard to the next 13:27:19
22 without any change in meaning. 13:27:23

1 Q During the transition period that you 13:27:27
2 just mentioned, were the terms "bank" and "rank" 13:27:29
3 always used interchangeably? 13:27:31
4 A No. You had to look at context. But -- 13:27:34
5 but most commonly they were. 13:27:36
6 Rank was used to describe what had 13:27:40
7 previously been called a bank. 13:27:42
8 Q Okay. Could we go to Page 87 of your 13:27:45
9 declaration. 13:28:00
10 A Sure. 13:28:00
11 Q Do you see the annotated versions of 13:28:11
12 Figures 2 and 5 of Ellsberry? 13:28:14
13 A Yes. 13:28:17
14 Q There's a red box around a portion of 13:28:17
15 Figure 5 of Ellsberry. 13:28:23
16 Do you see that? 13:28:25
17 A Yes. 13:28:27
18 Q And there's a red box around Figure 2 of 13:28:27
19 Ellsberry. 13:28:31
20 Do you see that? 13:28:31
21 A Yes. 13:28:33
22 Q And then there's an arrow from the red 13:28:33

box around Figure 5 to the red box around Figure 2? 13:28:38 13:28:41

A Yes. 13:28:41

Q So what are you trying to show there? 13:28:42

A Figure 2 is illustrative of a -- of a -- of an implementation of Ellsberry's invention that corresponds to a narrower bit width and could be described, could be shown as a subset of Figure 5. While Figure 5 describes a full 72-bit-wide embodiment. 13:28:47 13:29:09 13:29:14 13:29:18 13:29:23 13:29:28

Q Is it your opinion that what is shown in the box around Figure 5 is equivalent to what is shown in the box around Figure 2 of Ellsberry? 13:29:29 13:29:31 13:29:36

MR. CHANDLER: Objection. Form. 13:29:38

Q Let me rephrase that. 13:29:42

Is it your opinion that what is shown in the red box around Figure 5 is equivalent to what is shown in the red box around Figure 2? 13:29:43 13:29:46 13:29:49

MR. CHANDLER: Objection. Form. 13:29:51

A The teachings are to be understood together. Right? So Figure 5 is an embodiment where each -- the chips is eight bits wide, and 13:29:55 13:29:57 13:30:08

1 its operation can be understood in more detail by 13:30:15
2 referring to Figure 2. 13:30:18
3 Figure 2 only shows one byte per port. 13:30:29
4 But the way it's described in Ellsberry, it's 13:30:38
5 illustrative of the concepts; it's not limited to 13:30:41
6 one byte per port. And Figure 5 shows that you 13:30:45
7 can have a wider rank. 13:30:47
8 And I think yet -- again, Figure 2 only 13:30:58
9 illustrates one byte per port. But if you look at 13:31:02
10 it really carefully they're numbered zero and N, 13:31:06
11 and there's a little squiggle up at the top that I 13:31:09
12 think is intended to inform the reader that this 13:31:12
13 part -- portion of the circuit can be replicated 13:31:16
14 many times to have a wider rank. 13:31:18
15 Q How many ranks are shown in Figure 5? 13:31:26
16 Or -- yes, I'm sorry, how many ranks are shown in 13:31:30
17 Figure 5? 13:31:33
18 A Let me go back and look at Ellsberry. 13:31:42
19 Two. It's -- says in one implementation 13:32:29
20 illustrated in Figure 5, but the illustration is 13:32:35
21 of two. 13:32:38
22 Q Can you turn to Paragraph 131 of your 13:32:39

1 declaration. 13:33:15
2 A Okay. 13:33:30
3 Q And this is where you begin -- strike 13:33:30
4 that. 13:33:35
5 This is where you address Element 1.E.1 13:33:35
6 related to the correction circuits. 13:33:38
7 Is that correct? 13:33:42
8 A Yes. 13:33:43
9 Q What is your understanding of the plain 13:33:43
10 and ordinary meaning of correction circuits? 13:33:44
11 A I think it would be a circuit that could 13:34:20
12 make a correction in the signal it's receiving. 13:34:21
13 Q That's how a person of ordinary skill in 13:34:24
14 the art would have understood this term in the 13:34:40
15 '731 patent? 13:34:41
16 MR. CHANDLER: Objection. 13:34:42
17 A The only actual circuit that's described 13:34:55
18 in the '731 patent is -- is an active termination 13:34:57
19 circuit. And that's what I found in the prior 13:35:02
20 art. So I really didn't have to go any further 13:35:04
21 than that. 13:35:08
22 Q What is the active termination circuit 13:35:09

1 that you're referring to in the '731 patent? 13:35:17
2 A For example, impedance matching circuit 13:35:24
3 152. Maybe more broadly it's 150. Correction 13:35:28
4 Circuit 150, which includes both the course and 13:35:50
5 the fine correction circuit. 13:35:58
6 Q So is it your understanding that the 13:35:59
7 correction circuit 150 of the '731 patent only 13:36:15
8 performs active termination? 13:36:20
9 A It adjusts for impedance mismatches, and 13:36:25
10 that's what I found in the prior art. 13:36:29
11 Q Does the patent describe that the 13:36:31
12 correction circuit 150 performs anything other 13:36:35
13 than impedance mismatches? 13:36:37
14 A I don't recall. But it certainly didn't 13:36:42
15 require any more than that. 13:36:43
16 Q Can you turn to Claim 1 of the '731 13:37:46
17 patent. 13:37:49
18 A Okay. 13:37:57
19 Q And starting on Line 12 of Column 17, it 13:37:57
20 says, "Each circuit of the at least one circuit 13:37:59
21 further comprising a set of correction circuits." 13:38:03
22 Do you see that? 13:38:06

1 A Yes. 13:38:07
2 Q And then if we go down to Line 19 it 13:38:07
3 says, "Each correction circuit of the set of 13:38:11
4 correction circuits including at least one 13:38:12
5 programmable impedance mismatching circuit"? 13:38:17
6 A Yes. 13:38:20
7 Q So are you interpreting the impedance 13:38:20
8 matching circuit to be the same as the correction 13:38:23
9 circuit in Claim 1? 13:38:28
10 A No. But it's sufficient to satisfy the 13:38:29
11 limitation, and that's all I had to find in the 13:38:34
12 prior art. 13:38:37
13 Q And what is the basis for that opinion? 13:38:37
14 MR. CHANDLER: Objection. Form. 13:38:58
15 A That it's all that the limitation says 13:39:00
16 it's necessary to include. It doesn't -- doesn't 13:39:03
17 say that it's necessary to include anything else 13:39:06
18 in the correction circuit, other than at least one 13:39:08
19 programmable impedance matching circuit. 13:39:14
20 Q And then in Claim 6, starting down at 13:39:17
21 Column 17 Line 55, it says, "Wherein the each 13:39:32
22 correction circuit of the set of correction 13:39:35

1 circuits in the each circuit of the at least one 13:39:35
2 circuit further includes a delay circuit." 13:39:39
3 Do you see that? 13:39:41
4 A Yes. For Claim 6 I also found the delay 13:39:43
5 circuit. 13:39:48
6 Q And is it your opinion that the delay 13:39:48
7 circuit, Figure 6, is the same as the impedance 13:39:50
8 matching circuit in Claim 1? 13:39:57
9 MR. CHANDLER: Objection. Form. 13:39:59
10 A No; I identified a different circuit, 13:40:18
11 delay circuit. 13:40:21
12 Q What circuit did you identify for Claim 13:40:31
13 6? 13:40:33
14 A I identified the latency extension 13:40:51
15 circuitry that's described in Ellsberry. 13:40:53
16 Q Where is the latency extension circuitry 13:41:12
17 of Ellsberry? 13:41:43
18 MR. CHANDLER: Objection. Form. 13:41:44
19 A It was mostly described functionally, but 13:41:47
20 I believe it's in the switch ASIC. 13:41:49
21 Q Where in the switch ASIC would it be? 13:41:51
22 A Oh, I don't know. As I said, it's 13:41:56

1 described -- it's described functionally as being 13:41:59
2 part of the switch ASIC. I don't think it's -- it 13:42:02
3 would -- it would be in -- let's see if we can 13:42:06
4 tell. I think it's in Elements 402 and 404 and 13:42:12
5 controlled by the control block in Figure 4. 13:42:41
6 Q 402 of Ellsberry is a signal driver. 13:43:05
7 Correct? 13:43:10
8 A It's also got a register in there. 13:43:12
9 Q Ellsberry -- I believe Ellsberry refers 13:43:14
10 to 402 as a bidirectional signal driver. 13:43:19
11 Is that correct? 13:43:22
12 A It does. But it also illustrates it as 13:43:27
13 having a register. 13:43:29
14 Q Okay. And it's your opinion that the 13:43:30
15 bidirectional signal drivers 402 and 404 are the 13:43:33
16 claimed correction circuits. 13:43:39
17 Is that right? 13:43:40
18 A They're a portion of it, along with 13:43:41
19 the -- the adaptive terminators in the 13:43:44
20 combination. 13:43:47
21 Q Can we go to Paragraph 131 of your 13:43:48
22 declaration? 13:44:04

1 A Okay. 13:44:04
2 Q So in 131 you -- in Paragraphs 131 13:44:13
3 through 133 you address Element 1.E.1. 13:44:18
4 Is that correct? 13:44:23
5 A Yes. 13:44:31
6 Q And you are relying on Ellsberry. 13:44:31
7 Is that correct? 13:44:36
8 MR. CHANDLER: Objection. Form. 13:44:38
9 A Again, in the -- the grounds as Ellsberry 13:44:49
10 is modified by the other references. But the -- I 13:44:54
11 point to evidence in Ellsberry to show where the 13:45:01
12 correction circuits be. Then later when we talk 13:45:05
13 about the programmable impedance matching circuit, 13:45:08
14 I described the modifications. 13:45:11
15 Q But it's your position that the 13:45:12
16 bidirectional signal drivers are correction 13:45:14
17 circuits. 13:45:16
18 Is that correct? 13:45:16
19 MR. CHANDLER: Objection. Form. 13:45:18
20 A As modified by Dour or Dour and Abadeer. 13:45:19
21 Q Where in your declaration do you explain 13:45:30
22 that the bidirectional signal drivers as modified 13:45:31

1 by Dour are the -- are the claimed correction 13:45:37
2 circuits of Element 1.E.1? 13:45:40
3 A Starting in Paragraph 134, where I talk 13:45:44
4 about the language that describes the 13:45:48
5 characteristics of the correction circuits. 13:45:50
6 Q But is it your opinion that the read 13:46:15
7 driver of 402 in Ellsberry itself is a correction 13:46:20
8 circuit? 13:46:25
9 A No. The entirety of 402 and 404 as 13:46:27
10 modified by Dour or Dour and Abadeer would be the 13:46:31
11 claimed correction circuit. 13:46:36
12 Q In Paragraph 133 -- and this is on Page 13:46:38
13 92 of your declaration -- the first full sentence, 13:47:51
14 you say, "For example, during read operations, 13:47:56
15 read drivers (triangles with READ in Figure 4 13:48:00
16 above) in the 'bidirectional signal drivers 402 13:48:05
17 and 404' end quote, correct DQ read data signals 13:48:10
18 by amplifying and reshaping the signals, so that 13:48:15
19 the system controller receives the correct read 13:48:18
20 information via port at 230 and 'DIMM interface 13:48:20
21 202.'" 13:48:25
22 Do you see that? 13:48:26

1 A Yes. 13:48:27
2 Q Does Ellsberry state that the 13:48:28
3 bidirectional signal drivers amplify and reshape 13:48:32
4 signals? 13:48:35
5 A I don't recall if that's the exact 13:48:46
6 language, but that was my understanding of the 13:48:47
7 teachings. 13:48:48
8 Q So Ellsberry does not state that? 13:48:48
9 MR. CHANDLER: Objection. Form. 13:48:56
10 A I don't recall the exact language. 13:48:57
11 Q Let's go to Ellsberry. Paragraph 45. 13:48:59
12 A Uh-huh. 13:49:20
13 Q It says in the second sentence of 13:49:20
14 Paragraph 45, "Data is transmitted from DIMM 13:49:31
15 interface 202 via the data bus 230 to 13:49:33
16 bidirectional signal drivers 402 and 404 that 13:49:37
17 transmit and receive data over separate buses 234 13:49:41
18 and 236 to the different sets of memory banks." 13:49:46
19 Do you see that? 13:49:49
20 A Yes. 13:49:50
21 Q I don't believe that the bidirectional 13:49:50
22 signal drivers 402 and 404 are described anywhere 13:49:54

1 else in Ellsberry. 13:49:57
2 Are you aware of that? 13:50:00
3 A They're illustrated. I don't think 13:50:04
4 they're discussed anywhere else. 13:50:06
5 Q So let me ask my question again, then. 13:50:08
6 Does Ellsberry state that the bidirectional signal 13:50:10
7 drivers amplify and reshape signals? 13:50:12
8 MR. CHANDLER: Objection. Form. 13:50:15
9 A I don't think he uses those words, but 13:50:16
10 that's what it teaches. That's what a person of 13:50:18
11 ordinary skill would understand from the shape, 13:50:20
12 the triangle shape, and the placement as shown in 13:50:24
13 Figure 4. It also talks about the fact that it 13:50:29
14 uses a tuning mechanism to adjust buffer drive 13:50:35
15 strength, that teaches it to me. And it talks 13:50:39
16 about using it for impedance calibration. So that 13:50:42
17 also talks -- to me describes reshaping signals. 13:50:48
18 Q What do you mean by "reshaping signals"? 13:50:57
19 A In this particular case it means reducing 13:51:02
20 reflections. Also because of the amplification of 13:51:11
21 the buffering driver, it can sharpen edges. 13:51:16
22 Q The signal drivers 402 and 404 also have 13:51:32

1 DQ write latches. 13:51:36
2 Is that right? 13:51:41
3 A They do. 13:51:42
4 Q What do those DQ write latches do? 13:51:42
5 A Those add a delay in write operations. 13:51:46
6 Q Where does Ellsberry explain that they 13:51:48
7 add a delay? 13:51:51
8 A That's what latches do. 13:51:51
9 Q Okay. So that's just a natural function 13:51:54
10 of the latch. 13:51:57
11 Is that right? 13:51:57
12 A Let me look at the language. There may 13:51:58
13 have been a reference to it as well. 13:52:01
14 The way the latch is used in that 13:52:36
15 circuit, that would be its natural function. Plus 13:52:37
16 a person of ordinary skill would understand this 13:52:40
17 in the context of the -- of the DDR technology 13:52:42
18 that Ellsberry references. And those DDR 13:52:47
19 technologies -- they may even show it -- has a 13:52:52
20 single posted CAS value. So whenever you make a 13:52:58
21 change for DDR to the read latency which is 13:53:13
22 described in Ellsberry, you have to have a 13:53:17

1 corresponding write latency adjustment as well. 13:53:20
2 Q And it's your opinion that the 13:53:27
3 functionality that you just described is performed 13:53:33
4 by the DQ latch in Ellsberry? 13:53:36
5 A The latch in 402 and 404, yes. That's -- 13:53:41
6 that's what's being communicated to the reader. 13:53:45
7 Q How is that being communicated to the 13:53:47
8 reader? What in Ellsberry teaches that? 13:53:51
9 A Well, ordinarily when you put a latch in 13:53:56
10 the middle of a -- of a communication path, that 13:53:59
11 would represent a delay. In this particular case, 13:54:03
12 when read in conjunction with the DDR 13:54:11
13 specification, a person of ordinary skill in the 13:54:14
14 art would understand that that delay is -- is 13:54:16
15 matching the one-cycle latency adjustment that's 13:54:20
16 described in Ellsberry. 13:54:25
17 Q So it has to be read in conjunction with 13:54:26
18 the DDR specification in order to get to that? 13:54:30
19 A With some knowledge of the DDR 13:54:34
20 specification, that would help, yes. But again, a 13:54:35
21 portion of that specification is quoted in Figure 13:54:40
22 9. It's referenced throughout Ellsberry. It's 13:54:42

1 not -- not like a person would have to go find it 13:54:46
2 on their own. They -- it's just the context of 13:54:48
3 the description in Ellsberry. 13:54:51
4 Q Let's go to Paragraph 137 of your 13:54:52
5 declaration. 13:55:36
6 This is where you start addressing 13:55:50
7 Element 1.F.2. 13:55:52
8 Is that right? 13:55:53
9 A Yes. 13:55:54
10 Q And for Element 1.F.2 you are relying on 13:55:54
11 the combination of Ellsberry and Dour. 13:55:57
12 Is that correct? 13:55:59
13 MR. CHANDLER: Objection. Form. 13:56:02
14 A That's the evidence that I cite, yes, for 13:56:11
15 the two different grounds. 13:56:13
16 Q Does Ellsberry alone disclose dynamically 13:56:15
17 controlling a programmable impedance-matching 13:56:23
18 circuit based on which rank is selected? 13:56:25
19 A Ellsberry discloses -- let me see if I 13:56:33
20 can get the language right here. 13:56:38
21 Ellsberry discloses programmable 13:57:16
22 impedance calibration and suggests that the reason 13:57:19

1 that it's needed is because of the variation in 13:57:22
2 wiring characteristics in the DIMM, which would 13:57:27
3 correspond to the bank selection. 13:57:31
4 But in my opinions I haven't relied on 13:57:34
5 that alone. I have augmented it by the teachings 13:57:37
6 of Dour. 13:57:40
7 Q Does Dour discuss ranks? 13:57:42
8 A No; but it discusses wire lengths, which, 13:57:45
9 as we talked about before, is a natural 13:57:59
10 consequence of ranks. 13:58:04
11 Q Let's go to Dour. Can you show me where 13:58:06
12 Dour talks about wire lengths? 13:58:12
13 A I don't think it uses the phrase "wire 13:59:55
14 lengths," but it does teach, even in the abstract, 13:59:57
15 that it's compensating for the physical 14:00:03
16 characteristics of the device. And then talks 14:00:05
17 about, even in the background section, that these 14:00:12
18 devices are connected over wired buses. And 14:00:18
19 that's part of the physical characteristics that's 14:00:23
20 being compensated for. 14:00:25
21 Q Where do you see physical 14:00:31
22 characteristics? 14:00:34

1 A Fourth line of the abstract. It may 14:00:38
2 appear elsewhere as well. 14:00:43
3 Q So in the abstract second sentence it 14:00:55
4 says, "The on die termination circuit may be 14:00:58
5 programmed to compensate for environmental 14:01:03
6 conditions and the physical characteristics of the 14:01:04
7 device." 14:01:06
8 Correct? 14:01:08
9 A Yes. And then that's described in more 14:01:09
10 detail in Column 4. 14:01:11
11 Q What do you understand "the device" to be 14:01:15
12 in that sentence of the abstract? 14:01:19
13 A Well, I guess the physical 14:01:34
14 characteristics of the device would be the actual 14:01:35
15 memory chip. But the environmental conditions 14:01:43
16 would include the things that it's connected to. 14:01:46
17 MR. BEMBEN: We've been going for about 14:02:10
18 another hour. Do you want to take a quick break? 14:02:13
19 THE WITNESS: Sure. 14:02:15
20 MR. BEMBEN: Do you want to do ten 14:02:16
21 minutes this time? 14:02:17
22 THE WITNESS: Sure. 14:02:19

1 MR. BEMBEN: Off the record. 14:02:20
2 (A recess was taken.) 14:02:21
3 BY MR. BEMBEN: 14:12:50
4 Q Dr. Wolfe, can you go back to Dour and go 14:12:51
5 to Column 4, please? 14:12:53
6 A Yes. 14:12:54
7 Q And can you review Lines 4 through 20 of 14:13:03
8 Column 4 of Dour? 14:13:07
9 A Okay. 14:13:08
10 Q Do you see in Line 15 where Dour refers 14:13:15
11 to PVT? 14:13:17
12 A Yes. 14:13:21
13 Q In this art that stands for process, 14:13:21
14 voltage, and temperature. 14:13:25
15 Is that right? 14:13:26
16 A No, not here. Let me look. 14:13:28
17 Here it's physical characteristics, 14:13:34
18 voltage, and temperature. 14:13:36
19 Q Okay. What do you understand "physical 14:13:37
20 characteristics" to mean? 14:13:42
21 A I think it's pretty broad in this 14:13:51
22 description. It includes, you know, if you look 14:13:53

1 at the whole context, including kind of what's 14:13:55
2 described in Column 3, I think it includes the 14:13:59
3 characteristics of communication line 205. 14:14:04
4 Q But in Column 4 when Dour says physical 14:14:09
5 characteristics, voltage levels, and temperature 14:14:13
6 of Block 403, do you see that? 14:14:15
7 A Yes. 14:14:18
8 Q So he's referring to Block 403, which is 14:14:18
9 in Figure 4. Correct? 14:14:20
10 A Yes. This is all about one embodiment. 14:14:25
11 Yes. 14:14:27
12 Q When he refers to voltage levels, he's 14:14:27
13 referring to the supply voltage. 14:14:31
14 Is that correct? 14:14:33
15 MR. CHANDLER: Objection. Form. 14:14:36
16 A No. I think it's signal voltage. 14:14:41
17 Q And why do you believe it's signal 14:14:42
18 voltage of Block 43? 14:14:49
19 A Because it talks about voltage levels. 14:14:51
20 Q Supply voltage don't have voltage levels? 14:14:56
21 A Could be. But he doesn't say supply 14:14:59
22 voltage; what he says is broader. 14:15:01

1 Q But it would be voltage levels of Block 14:15:04
2 403. 14:15:12
3 Is that correct? 14:15:12
4 A In this embodiment, yes. 14:15:13
5 Q Are you familiar with PVT outside of the 14:15:16
6 Dour reference? 14:15:50
7 A In various contexts, yes. 14:15:55
8 Q In the context of circuits? 14:15:57
9 A Huh? 14:16:00
10 Q In the context of circuits? 14:16:01
11 A Then again, it depends what the -- I 14:16:05
12 mean, in certain documents it's used to mean 14:16:07
13 certain things. 14:16:09
14 Q Have you heard it stand for process, 14:16:10
15 voltage, and temperature? 14:16:14
16 A In some contexts it does. Again, there's 14:16:16
17 a definition here, so I wouldn't -- wouldn't try 14:16:19
18 to read that into Dour. 14:16:21
19 Q But what contexts have you heard PVT 14:16:23
20 stand for process, voltage, and temperature? 14:16:28
21 A When I worked in integrated circuit 14:16:30
22 manufacturing. 14:16:32

1 Q So for integrated circuits? 14:16:33
2 A Well, more specifically when I worked 14:16:37
3 with fabs, you know. 14:16:39
4 Q Fabrication. Okay. And in the V in PVT 14:16:41
5 when you worked in integrated circuit fabrication, 14:16:46
6 did that stand for the supply voltage? 14:16:48
7 A Depended on the context. 14:16:52
8 Q In what context did the V in PVT stand 14:16:53
9 for supply voltage? 14:17:02
10 A Situation-specific. Other situations it 14:17:04
11 refers to threshold voltages. 14:17:07
12 Q Can you not identify any specifics? 14:17:12
13 A No. I mean, it's been 20-plus years 14:17:17
14 since I worked in that field. 14:17:21
15 And again, it's not ambiguous what it 14:17:29
16 means in the paragraph we just read. 14:17:32
17 Q What do you mean by that? 14:17:37
18 A I mean it literally says, gives us three 14:17:39
19 phrases that start with P, V, and T and then puts 14:17:43
20 PVT in parentheses. I don't think it's at all 14:17:49
21 ambiguous that it refers to those three things on 14:17:51
22 Line 15 of Column 4. 14:17:55

1 Q And voltage levels refers to voltage 14:17:56
2 levels of Block 403. Correct? 14:17:59
3 MR. CHANDLER: Objection. 14:18:00
4 Q In Line 15? 14:18:01
5 MR. CHANDLER: Objection. 14:18:02
6 A Well, it actually says signals in Block 14:18:03
7 403. 14:18:05
8 Q No. It says -- let's just read that 14:18:09
9 sentence then. "In one embodiment, finite state 14:18:11
10 machine may encode the impedance of signals in 14:18:14
11 Block 403 based on physical characteristics, 14:18:17
12 voltage levels and temperatures (PVT) of Block 14:18:21
13 403." 14:18:24
14 So are you reading "voltage levels" as 14:18:25
15 modifying "signals" in that sentence? 14:18:27
16 A No. I just think that it -- there's no 14:18:30
17 reason to assume that it excludes any voltage 14:18:33
18 levels in Block 403. 14:18:36
19 Q Are you familiar with the concept of 14:18:37
20 objective factors of nonobviousness? 14:18:53
21 A I think so. I mean, usually I hear them 14:18:57
22 referred to as objective indicia of 14:19:01

1 nonobviousness. 14:19:02
2 Q Okay. Go to Paragraph 36 of your 14:19:03
3 declaration. 14:19:07
4 So you referred to them as "objective 14:19:17
5 factors." That's why I used that terminology. 14:19:19
6 Do you see that? 14:19:21
7 A Yeah. I think those mean the same thing. 14:19:21
8 Q Are you aware that taking of licenses by 14:19:23
9 others is one of those objective indicia? 14:19:25
10 A It can be if there's a nexus to the 14:19:28
11 claims at issue. 14:19:30
12 Q So your understanding of the licensing 14:19:34
13 secondary consideration, that that is only valid 14:19:56
14 if there's a nexus to the claims at issue. 14:19:57
15 Is that right? 14:19:59
16 A It's only irrelevant. It only has 14:20:03
17 nontrivial weight if there's a nexus to the claims 14:20:06
18 at issue. 14:20:10
19 Q Are you aware that Samsung previously 14:20:11
20 licensed the '731 patent? 14:20:15
21 MR. CHANDLER: Objection. Form. 14:20:20
22 A I don't know. I know there was a license 14:20:21

1 with -- with Netlist, but I don't know the scope 14:20:23
2 of that license. 14:20:27
3 Q So you are not aware that Samsung had 14:20:29
4 previously licensed the '731 patent? 14:20:30
5 MR. CHANDLER: Objection. Form. 14:20:33
6 A I'm not aware of whether or not it was in 14:20:34
7 the portfolio at that time or not. But I have not 14:20:36
8 seen any evidence that -- that Samsung considered 14:20:42
9 the '731 to be an important part of that license. 14:20:46
10 Q And why would that be relevant, that 14:20:50
11 Samsung considered it to be an important part of 14:20:52
12 the license? 14:20:56
13 A Because that would be a factor I would 14:20:56
14 consider to determine whether or not there was any 14:20:58
15 significant impact on obviousness. Just the fact 14:21:01
16 that if a company takes a license to a thousand 14:21:06
17 patents because they're concerned about potential 14:21:11
18 infringement of Patent A, that's not very 14:21:16
19 informative about Patent B that might be in that 14:21:19
20 same portfolio. 14:21:23
21 Q And that's your understanding of 14:21:28
22 licensing as a secondary consideration of 14:21:31

1 nonobviousness? 14:21:35
2 A My understanding is that for it to have 14:21:36
3 any significant impact there has to be a nexus to 14:21:38
4 the asserted claims. 14:21:41
5 Q And the licensee has to think that it was 14:21:42
6 important. 14:21:44
7 Is that right? 14:21:44
8 MR. CHANDLER: Objection. 14:21:46
9 A There can be various way to show a nexus, 14:21:47
10 but I'm not aware of any in this case. 14:21:49
11 Q But you mentioned also whether the 14:21:51
12 patent -- strike that. 14:21:57
13 You also mentioned whether the licensee 14:21:57
14 felt that the patent was important in your 14:21:59
15 testimony. 14:22:03
16 A That could be one way to show a nexus. 14:22:04
17 Q That could be one way to show a nexus. I 14:22:06
18 see. Okay. 14:22:10
19 So if I were to tell you that there was 14:22:17
20 no requirement for licensing to show a nexus for 14:22:18
21 it to have weight in an obviousness consideration, 14:22:22
22 would that change your opinion? 14:22:27

1 A I would need to understand more, because 14:22:30
2 that's not the way I've been instructed in the 14:22:32
3 past. 14:22:34
4 Q Okay. 14:22:34
5 A I mean, it can have weight, just not 14:22:37
6 substantial weight. 14:22:39
7 Q But just to confirm, you were -- when you 14:22:40
8 prepared your declaration in this matter, you were 14:22:49
9 not aware that Samsung had previously licensed the 14:22:52
10 '731 patent. 14:22:56
11 Is that correct? 14:22:56
12 MR. CHANDLER: Objection. Form. 14:22:57
13 A I was aware that it had licensed a large 14:22:59
14 portfolio, but I was not aware of the individual 14:23:02
15 patents in the portfolio. 14:23:04
16 Q So you did not know that Samsung had 14:23:09
17 licensed the '731 patent. 14:23:11
18 Is that correct? 14:23:13
19 A I didn't know one way or another if it 14:23:15
20 was within the portfolio. But I was not aware of 14:23:18
21 any evidence that -- that there was a nexus 14:23:21
22 between that license and the '731 patent. 14:23:25

1 Q And you believe that the law requires a 14:23:30
2 nexus for licensing? 14:23:33
3 A For it to have a substantial impact on 14:23:36
4 the question of obviousness. 14:23:38
5 Q Understood. 14:23:41
6 MR. BEMBEN: Okay. Can we take a 14:23:45
7 five-minute break. I think we might be wrapping 14:23:46
8 up. 14:23:48
9 (A recess was taken.) 14:23:50
10 BY MR. BEMBEN: 14:30:40
11 Q A few more questions for you, Dr. Wolfe. 14:30:40
12 Can you go to Claim 1 again in the '731 patent. 14:30:43
13 A Sure. 14:30:46
14 Okay. 14:30:52
15 Q And then if you take a look at Line -- 14:30:53
16 Column 17, I believe it's Line 16. It refers to 14:30:57
17 signals. 14:31:01
18 A Yes. 14:31:06
19 Q I'll read that clause. It says, "Each 14:31:07
20 correction circuit of the set of correction 14:31:09
21 circuits being configured to make corrections in 14:31:12
22 one or more signals transmitted between a 14:31:14

1 respective port connection of the first set of 14:31:18
2 port connections and a corresponding port 14:31:20
3 connection in the second set of port connections." 14:31:22
4 A Yes. 14:31:24
5 Q It is a bit of a mouthful but it says, 14:31:24
6 "signals" in there. 14:31:27
7 What is your understanding of the term 14:31:28
8 "signals"? 14:31:29
9 A I think it's just referring to the fact 14:31:32
10 that there are going to be multiple wires between 14:31:34
11 those two ports. 14:31:41
12 Q That's not limited to any specific type 14:31:45
13 of signal. 14:31:47
14 Is that correct? 14:31:48
15 MR. CHANDLER: Objection. Form. 14:31:49
16 A I think in context it's talking about the 14:31:51
17 data signals. 14:31:53
18 Q Can you go to Column 15 of the '731 14:31:57
19 patent. 14:32:01
20 A Okay. 14:32:03
21 Q Line 12. Starting on Line 12. You see 14:32:03
22 it says, "Each of the second set of ports 126 and 14:32:11

1 corresponding interfaces of the second set of 14:32:14
2 interfaces 340 corresponds to a memory signal 14:32:17
3 (e.g., a data, address, and/or control signal) of 14:32:21
4 at least one memory bus between the host system 14:32:27
5 and the memory module." 14:32:30
6 Do you see that? 14:32:31
7 A I see that. 14:32:32
8 Q And so the '731 uses the term -- used the 14:32:33
9 term "signal" and provides examples of data, 14:32:37
10 address, and/or control. 14:32:40
11 Do you see that? 14:32:41
12 MR. CHANDLER: Objection. 14:32:42
13 A In Column 15, yes. 14:32:43
14 Q And it's your opinion that when that term 14:32:44
15 "signal" is used in Claim 1, that it's not 14:32:51
16 referring to different types of signals that are 14:32:56
17 mentioned in Column 15? 14:33:00
18 A Well, I read it as being the data 14:33:05
19 signals, because those are the ones that are 14:33:07
20 taught as being adjusted in response to address 14:33:08
21 and control signals. 14:33:13
22 I didn't see any place where the spec 14:33:15

1 teaches adjusted address and control signals in 14:33:17
2 response to address and control signals. But all 14:33:22
3 I really needed for my opinion was to know that it 14:33:24
4 included -- was that data signals were sufficient 14:33:28
5 to meet that claim element, and that's what I 14:33:31
6 found in the prior art. 14:33:33
7 Q In your declaration did you provide any 14:33:35
8 opinion that the term signal -- "signals" in Claim 14:33:52
9 1 is limited to data signals? 14:33:56
10 A No. No. I simply identified data 14:34:04
11 signals as being sufficient to meet the 14:34:08
12 limitation. 14:34:10
13 MR. BEMBEN: Okay. No further questions 14:34:15
14 at this time. I pass the witness. 14:34:20
15 MR. CHANDLER: I am going to go off the 14:34:21
16 record for ten minutes. Let me go through my 14:34:23
17 notes. 14:34:25
18 (A recess was taken.) 14:34:26
19 EXAMINATION BY COUNSEL FOR PETITIONER 14:44:28
20 BY MR. CHANDLER: 14:44:28
21 Q Dr. Wolfe, I have some followup questions 14:44:29
22 to clarify some of the questions and answers from 14:44:32

1 counsel for Netlist. 14:44:35
2 Could you start by pulling up the 14:44:38
3 Ellsberry reference marked as Exhibit 1005 and 14:44:41
4 then also pull up your expert declaration marked 14:44:45
5 as Exhibit 1003 and let me know when you have both 14:44:49
6 of those in front of you, and then I'll direct you 14:44:52
7 to -- 14:44:55
8 A I do. 14:44:57
9 Q All right. So if you could put in front 14:44:57
10 of you Figure 8 of the Ellsberry reference marked 14:45:01
11 as Exhibit 1005 and then Page 101 of your expert 14:45:05
12 declaration marked as Exhibit 1003, and let me 14:45:11
13 know when you have those in front of you. 14:45:15
14 A Okay. 8A? Is that okay? 14:45:18
15 Q Correct. 14:45:20
16 A And where in the declaration? 14:45:24
17 Q Page 101. 14:45:25
18 A Okay. 14:45:32
19 Q There were questions and answers about 14:45:32
20 Figure 8 of Ellsberry where I objected to the form 14:45:35
21 because I found the questions and answers 14:45:39
22 confusing. So I'd like to follow up on that 14:45:42

1 discussion and get some clarification from you. 14:45:47
2 Understood? 14:45:51
3 A Okay. 14:45:52
4 Q So in Figure 8A of Ellsberry marked as 14:45:52
5 Exhibit 1005, there are some letters at the 14:45:57
6 bottom, A, B, C, D, E, F, G, H, I, and there are 14:46:01
7 also some labels at the top of each column. 14:46:06
8 Do you see that? 14:46:09
9 A I do. 14:46:11
10 Q And rather than use those letters at the 14:46:11
11 bottom, which is a little vague and confusing, I'm 14:46:15
12 going to refer to the labels at the top of Figure 14:46:19
13 8 of Ellsberry, marked as Exhibit 1005. 14:46:23
14 Understood? 14:46:28
15 A Okay. 14:46:29
16 Q And what was confusing to me about the 14:46:29
17 questions and answers is that there was this 14:46:31
18 concept of where do signals come from, something 14:46:35
19 along those lines, which I found a little 14:46:39
20 confusing because it was vague as to whether that 14:46:43
21 referred to the very first origin of a signal that 14:46:51
22 may have been transformed along the way or if 14:46:55

1 it -- or what. 14:46:59
2 So what I want to do is go through each 14:47:02
3 of these column labels and have you explain what 14:47:07
4 Ellsberry's teaching and use Page 101 of your 14:47:10
5 declaration marked as Exhibit 1003 to help your 14:47:14
6 explanation of what is being taught by Figure 8 of 14:47:18
7 Ellsberry. Understood? 14:47:22
8 A Sure. Yeah. Not every column is a 14:47:24
9 signal in Figure 8. 14:47:26
10 MR. BEMBEN: And let me just object to 14:47:28
11 that. You're testifying on the record here, and 14:47:29
12 you're coaching the witness. 14:47:32
13 Q So when you were asked about the first 14:47:37
14 column of Figure 1 that's labeled Command, what is 14:47:38
15 that referring to, and how does it correspond to 14:47:44
16 what's shown on Page 101 of your expert 14:47:47
17 declaration? 14:47:53
18 A "Command" is a portion of what's 14:47:54
19 highlighted in orange. It comes from the DIMM 14:47:58
20 interface to the control ASIC on Page 101. 14:48:00
21 Q And then the second column in Figure 8A 14:48:03
22 of Ellsberry is labeled Mode. 14:48:08

1 Do you see that? 14:48:12
2 A Yes. 14:48:12
3 Q And then in that column labeled Mode of 14:48:13
4 Figure 8A of Ellsberry do you see there's Xs, or 14:48:17
5 it says "col," which I assume is column, and then 14:48:22
6 another entry is "row/bank"? 14:48:27
7 A Yes. 14:48:35
8 Q So what is the Mode column in Figure 8A 14:48:35
9 of Ellsberry marked as Exhibit 1005 referring to? 14:48:40
10 A Ellsberry describes different 14:48:47
11 embodiments. One is operating on using portions 14:48:50
12 of the column address for bank selection. The 14:48:55
13 other one uses portions of the row or bank address 14:48:59
14 for column selection. Those can either be hard 14:49:03
15 wired into the embodiment or they can be 14:49:08
16 programmed into the control ASIC. And where 14:49:10
17 there's an X, I think it means either mode. 14:49:13
18 Q And is there a figure that -- of 14:49:17
19 Ellsberry that provides more description on column 14:49:22
20 versus row/bank? 14:49:26
21 A Yeah. We looked at that in Figure 7 14:49:31
22 before. 14:49:33

1 Q And can you explain that a little bit 14:49:33
2 more? 14:49:38
3 A Yeah. We went through the examples in 14:49:39
4 7A. And the actual selection of a bank and the 14:49:41
5 signal that's used to select the bank, signal or 14:49:47
6 signals, depends on the mode. 14:49:51
7 Q So in Figure 7A there is a column label 14:49:53
8 that says Mode, and there's a column label that 14:50:03
9 says Physical Bank Select. What is the 14:50:06
10 relationship between those two columns in Figure 14:50:10
11 7A and the column in Figure 8A that has the column 14:50:14
12 labeled Mode? 14:50:18
13 A The Mode column in 7A corresponds to the 14:50:21
14 Mode column in 8A. Although the operation for the 14:50:25
15 row mode and the bank address mode are the same, 14:50:29
16 those are concatenated. 14:50:33
17 The physical bank select is just a 14:50:37
18 variation of each mode. It doesn't really reflect 14:50:39
19 it in 8A. 14:50:41
20 Q All right. Going back to Figure 8A, the 14:50:43
21 third column has the label ADDR, which I assume 14:50:48
22 refers to address. Could you explain what that 14:50:57

1 column in Figure 8A is referring to with reference 14:51:00
2 to Page 101 of your expert declaration marked as 14:51:03
3 Exhibit 1003? 14:51:06
4 MR. BEMBEN: Objection. Form. 14:51:08
5 A Sure. That reflects the address received 14:51:13
6 by the control ASIC. But in particular in Figure 14:51:24
7 8A it's just not relevant to any of the decisions 14:51:31
8 that are being illustrated here. 14:51:36
9 Q All right. And then the next column in 14:51:38
10 Figure 8A of Ellsberry is labeled P Bank, and 14:51:41
11 under that there's an X in some rows, there's an A 14:51:47
12 in some rows, and there's a B in some rows. 14:51:52
13 Do you see that? 14:51:55
14 A Yes. 14:51:56
15 Q And what does the Column P Bank in Figure 14:51:56
16 8A in Ellsberry refer to? And can you explain it 14:52:00
17 with reference to your annotation on Page 101 of 14:52:04
18 your expert declaration marked as Exhibit 1003? 14:52:06
19 A Yes. So there's a slight difference here 14:52:11
20 in that the illustration on 101 is a four-bank 14:52:13
21 system, where 8A is a two-bank system. But that 14:52:17
22 describes the bank to be selected. And for the 14:52:19

1 various configurations, Figure 7 shows you the 14:52:23
2 criteria for selection under PFY Bank Select. So 14:52:27
3 it shows you the result of that selection. And 14:52:34
4 that selection would be reflected in the chip 14:52:36
5 selects that come out in blue from the control 14:52:41
6 ASIC up to the various memory chips. 14:52:46
7 Q All right. And then using, for example, 14:52:50
8 in Figure 8A there's an entry in the table for the 14:52:54
9 write commands in the far left column. 14:53:02
10 Do you see that entry in Figure 8A of 14:53:04
11 Ellsberry? 14:53:08
12 A Yes. 14:53:09
13 Q So for example, when the write command in 14:53:09
14 the far left column of Figure 8A of Ellsberry is 14:53:17
15 received, can you explain, using the annotation on 14:53:24
16 Page 101 of your declaration marked as Exhibit 14:53:29
17 1003, what Ellsberry is teaching in Figure 8A? 14:53:33
18 A Sure. So again, you only have to look at 14:53:40
19 a subset of the banks here. But it means that one 14:53:45
20 of the banks -- so the command that comes into the 14:53:48
21 control ASIC is not necessarily the command that 14:53:52
22 gets sent out. It generates new commands. And 14:53:54

1 what it will do is, instead of sending a write 14:53:57
2 command to both banks, it will choose to send a 14:54:00
3 write command to one bank based on the P bank 14:54:02
4 field, and a no op command to the other bank. And 14:54:06
5 those will be sent again up through that wide blue 14:54:12
6 area marked 200. And then one will be sent down 14:54:16
7 through the narrow arrow that goes down to Bank 2, 14:54:19
8 for example. The other one to Bank 3. 14:54:27
9 Q All right. Could you please pull up 14:54:31
10 Exhibit 1042 and let me know when you have it. 14:54:42
11 (Exhibit 1042, previously marked, not 14:54:42
12 attached.) 14:54:42
13 A Okay. 14:54:58
14 MR. BEMBEN: Let me just object to scope. 14:54:58
15 This did not come up in the cross-examination. 14:55:00
16 Q Please read to yourself Paragraphs 41 to 14:55:04
17 44 and 48 of Exhibit 1042, and let me know when 14:55:09
18 you've completed reviewing those paragraphs. 14:55:14
19 MR. BEMBEN: Objection to scope. 14:55:18
20 A Okay. 14:55:41
21 Q Do you recall counsel from Netlist asking 14:55:41
22 you questions about objective evidence of 14:55:47

1 nonobviousness, sometimes referred to as objective 14:55:52
2 indicia of nonobviousness, also sometimes referred 14:55:56
3 to as secondary considerations of nonobviousness? 14:55:59
4 A I do. 14:56:02
5 Q And do you recall counsel from Netlist 14:56:02
6 asking you questions about whether Samsung had 14:56:06
7 taken a license to the '731 patent at issue in 14:56:09
8 this proceeding? 14:56:13
9 A '731 patent? 14:56:16
10 Q Yeah. 14:56:18
11 A Yes. 14:56:19
12 Q Now, I want you to assume that the facts 14:56:22
13 as laid out in Paragraphs 41 to 44 and 48 of 14:56:28
14 Exhibit 1042 are true. And based on that 14:56:34
15 assumption, what impact would that have on your 14:56:42
16 opinion about whether there are secondary 14:56:52
17 considerations of nonobviousness with respect 14:56:56
18 to -- with respect to the '731 patent? 14:57:01
19 A So I recognize that this is a secondary 14:57:05
20 consideration of nonobviousness, but I would find 14:57:07
21 it to be insubstantial because, one, the license 14:57:10
22 is quite small for a company the size of Samsung; 14:57:17

1 and, two, there's simply no evidence at this point 14:57:20
2 that the existence of the '731 patent had any 14:57:24
3 meaningful impact on the decision to take this 14:57:28
4 license or the amount paid. 14:57:33
5 Q And to be clear, I want you to assume 14:57:35
6 that there is a nexus between the license and the 14:57:37
7 '731 patent. And with that assumption, what 14:57:44
8 impact does the weight of the secondary 14:57:50
9 consideration of licensing of the '731 patent have 14:57:54
10 on your opinions with respect to the obviousness 14:57:58
11 of the claims of the '731 patent in light of the 14:58:01
12 prior art? 14:58:03
13 A Again, it has to be taken into 14:58:05
14 consideration. But based on the evidence so far, 14:58:07
15 it has an insubstantial impact on my opinion. 14:58:10
16 Q And does it change your ultimate opinion 14:58:14
17 about the obviousness of the claims of the '731 14:58:16
18 patent? 14:58:19
19 A No. 14:58:20
20 MR. CHANDLER: All right. No further 14:58:27
21 questions. 14:58:29
22 MR. BEMBEN: Let's take a break to -- so 14:58:30

1 that we can discuss. 14:58:34
2 Do you want to take a lunch break, 14:58:36
3 Dr. Wolfe? I know it's about noon there. 14:58:38
4 THE WITNESS: I can't imagine you have 14:58:41
5 enough questions on recross that it's worth taking 14:58:42
6 a lunch break. 14:58:47
7 MR. BEMBEN: Oh, you don't know me. It's 14:58:48
8 up to you. We can -- 14:58:52
9 THE WITNESS: I assume we're not going to 14:58:54
10 go more than another hour. 14:58:56
11 MR. BEMBEN: That's a safe assumption. 14:58:58
12 THE WITNESS: Then I don't need a lunch 14:58:59
13 break. 14:59:01
14 MR. BEMBEN: Let's take 15. Okay? 14:59:01
15 THE WITNESS: Okay. 14:59:03
16 (A recess was taken.) 14:59:05
17 EXAMINATION BY COUNSEL FOR PATENT OWNER 15:20:43
18 BY MR. BEMBEN: 15:20:43
19 Q Dr. Wolfe, can you go back to Exhibit 15:20:44
20 1042 which Mr. Chandler introduced into the record 15:20:47
21 during redirect? 15:20:53
22 A Sure. 15:20:54

1 Q What is Exhibit 1042? 15:20:54
2 A I believe it's a district court 15:20:57
3 Complaint. 15:21:02
4 Q And who are the plaintiffs in this 15:21:02
5 district court Complaint? 15:21:04
6 A Samsung. Samsung entities. I don't 15:21:09
7 really understand the corporate structure of 15:21:12
8 Samsung. Plus Avnet, who I believe is a 15:21:13
9 distributor. 15:21:17
10 Q So there's three Samsung entities that 15:21:19
11 are plaintiffs. Correct? 15:21:22
12 MR. CHANDLER: Objection. Outside the 15:21:23
13 scope of cross. 15:21:25
14 A Again, I don't know the corporate 15:21:26
15 structure, but it appears that way. 15:21:29
16 Q Okay. 15:21:32
17 MR. CHANDLER: Outside the scope of 15:21:33
18 redirect. 15:21:34
19 MR. BEMBEN: You introduced this exhibit, 15:21:37
20 so ... 15:21:39
21 Q It says that there are three plaintiffs, 15:21:39
22 Plaintiffs Samsung Electronics Co. Limited, which 15:21:42

1 they abbreviate SEC. 15:21:44
2 Do you see that? 15:21:46
3 MR. CHANDLER: Objection. Outside the 15:21:49
4 scope of redirect. 15:21:50
5 A I see that. 15:21:51
6 Q And there's another plaintiff, Samsung 15:21:52
7 Semiconductor, Incorporated, which they abbreviate 15:21:55
8 SSI. 15:21:56
9 Do you see that? 15:21:57
10 MR. CHANDLER: Same objection. 15:21:58
11 A I see that. 15:21:59
12 Q And there is a third Samsung entity, 15:22:00
13 Samsung Electronics America, Inc., which they 15:22:06
14 abbreviate SEA. 15:22:11
15 Do you see that? 15:22:11
16 A Yes. 15:22:12
17 MR. CHANDLER: Same objection. 15:22:15
18 Q Dr. Wolfe, can you answer? 15:22:16
19 A I do. 15:22:17
20 Q And there is another plaintiff, Avnet, 15:22:17
21 Incorporated. 15:22:20
22 Do you see that? 15:22:21

1 MR. CHANDLER: Same objection. 15:22:22
2 A I do. 15:22:23
3 Q And what is your understanding of a 15:22:23
4 declaratory judgment action for noninfringement? 15:22:25
5 MR. CHANDLER: Objection. Outside the 15:22:28
6 scope of redirect. 15:22:29
7 A Again, I'm not an attorney, but I believe 15:22:32
8 that if one can demonstrate that there's a 15:22:37
9 substantial threat of being accused of 15:22:42
10 infringement, one can ask a court to rule that 15:22:44
11 there is no infringement. 15:22:48
12 Q And you said that you're not familiar 15:22:52
13 with Samsung's corporate structure. But are you 15:22:54
14 familiar with Samsung Electronics America, SEA? 15:22:56
15 MR. CHANDLER: Objection. Outside the 15:23:00
16 scope of redirect. 15:23:01
17 A Again, I'm -- I understand that that 15:23:03
18 entity exists, but I don't understand what their 15:23:05
19 role is in the scope of Samsung's businesses. 15:23:10
20 Q How are you familiar with SEA? 15:23:12
21 MR. CHANDLER: Outside the scope of 15:23:22
22 redirect. I object. 15:23:23

1 A They have come up as an entity in 15:23:25
2 previous cases. 15:23:27
3 Q Previous cases that you've worked on? 15:23:28
4 A Yes. Yeah, on both sides; both for them 15:23:31
5 and against them. 15:23:34
6 Q Did you meet with counsel for SEA in this 15:23:35
7 IPR? 15:23:40
8 MR. CHANDLER: Objection. Outside the 15:23:40
9 scope of redirect. 15:23:41
10 A I met with counsel from Baker Botts. I 15:23:45
11 don't -- I'd have to go look and see exactly which 15:23:48
12 entity they represent. 15:23:53
13 Q Did you meet with counsel for Avnet in 15:23:54
14 this IPR? 15:23:58
15 A That's never come up. Again, I don't 15:24:03
16 know whether or not Baker Botts represents Avnet, 15:24:05
17 but that name has never come up in my work. 15:24:08
18 Q Okay. Can you go to Paragraph 146 of 15:24:12
19 Exhibit 1042. 15:24:15
20 A Yes. 15:24:20
21 MR. CHANDLER: I'm sorry, what was the 15:24:27
22 paragraph number? 15:24:28

1 MR. BEMBEN: Paragraph 146. 15:24:29
2 MR. CHANDLER: Objection. Outside the 15:24:31
3 scope of redirect. 15:24:32
4 Q Can you see in Paragraph 146, Dr. Wolfe, 15:24:34
5 that it states, "A substantial, immediate, and 15:24:37
6 real controversy exists between plaintiffs and 15:24:40
7 Netlist regarding whether plaintiffs or their 15:24:43
8 customers or end users infringe the '731 patent by 15:24:45
9 making, using, selling, and/or offering for sale 15:24:49
10 the Samsung DDR4 and DDR5 products in the United 15:24:52
11 States, or by importing the Samsung DDR4 and DDR5 15:24:56
12 products into the United States. A judicial 15:25:00
13 declaration is necessary to determine the parties' 15:25:03
14 respective rights regarding the '731 patent." 15:25:05
15 Do you see that? 15:25:08
16 A I do see that. 15:25:08
17 Q In that paragraph who do you understand 15:25:10
18 the plaintiffs to be? 15:25:13
19 MR. CHANDLER: Objection. Outside the 15:25:16
20 scope of redirect, and also outside the scope of 15:25:17
21 direct. 15:25:23
22 A So I'm just looking for context to make 15:25:26

1 sure it's part of the same Complaint, and not an 15:25:28
2 included document. 15:25:31
3 Again, I'm not an attorney, but my 15:25:33
4 understanding is that the four parties that we 15:25:35
5 discussed previously are the plaintiffs. 15:25:37
6 Q If Samsung invalidated the '731 patent in 15:25:38
7 this IPR, would the plaintiffs avoid potential 15:25:45
8 infringement liability? 15:25:48
9 MR. CHANDLER: Objection. Outside the 15:25:49
10 scope of both direct and redirect. 15:25:51
11 A Again, I'm not an attorney; but my 15:25:55
12 understanding is that they would. 15:25:58
13 Q If Samsung invalidated the '731 patent in 15:25:59
14 this IPR, would the controversy with respect to 15:26:02
15 the '731 patent between Samsung and Netlist be 15:26:04
16 resolved? 15:26:07
17 MR. CHANDLER: Objection. Outside the 15:26:08
18 scope of direct, redirect. Calls for a legal 15:26:09
19 conclusion. 15:26:12
20 A Yeah, now you're really getting beyond my 15:26:12
21 knowledge. 15:26:15
22 Q Well, if the patent is invalidated, can 15:26:15

1 you assert an invalid patent? 15:26:19
2 MR. CHANDLER: Same objection. 15:26:23
3 A My understanding is an invalid patent 15:26:23
4 cannot be infringed, but again, I'm not an 15:26:26
5 attorney. 15:26:29
6 Q In your opinion, would the plaintiffs 15:26:29
7 benefit if Samsung successfully invalidated the 15:26:36
8 '731 patent in this IPR? 15:26:40
9 MR. CHANDLER: Objection. Outside the 15:26:41
10 scope of direct and redirect. 15:26:42
11 A So I don't even actually know whether or 15:26:48
12 not this case is still pending. So, I mean, 15:26:53
13 hypothetically they would, but I don't have enough 15:26:56
14 of a factual basis to know one way or the other. 15:26:58
15 Q And if this case was pending, would that 15:27:00
16 change your answer? 15:27:02
17 MR. CHANDLER: Same objection. 15:27:04
18 A It would still be somewhat speculative, 15:27:08
19 because, again, I don't know whether or not -- I 15:27:10
20 know that they've asserted that they are at risk, 15:27:12
21 but I haven't seen the facts underlying it. 15:27:13
22 MR. BEMBEN: I have no further questions, 15:27:18

1 Dr. Wolfe. Thank you. 15:27:19
2 MR. CHANDLER: And I would just, for the 15:27:22
3 record, we would request from our side the 15:27:23
4 transcript within one week. We'd like the 15:27:28
5 opportunity to review and make corrections. 15:27:29
6 And I understood from the beginning that 15:27:32
7 there would be I guess a copy of this Zoom 15:27:34
8 recording. So that would be useful as well, in 15:27:39
9 the event that we need to make a correction to 15:27:41
10 something. 15:27:44
11 (Off the record at 3:28 p.m. EDT.)
12
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1 ACKNOWLEDGMENT OF DEPONENT
2 I, ANDREW WOLFE, Ph.D., do hereby
3 acknowledge that I have read and examined the
4 foregoing testimony, and the same is a true,
5 correct and complete transcription of the
6 testimony given by me, and any corrections appear
7 on the attached Errata sheet signed by me.
8
9 _____ _____
10 (DATE) (SIGNATURE)
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1 C E R T I F I C A T E
2 I, Debra Ann Whitehead, E-Notary Public in and for
3 the Commonwealth of Virginia, do hereby certify:
4
5 That ANDREW WOLFE, Ph.D., the witness
6 whose deposition is hereinbefore set forth, was duly
7 sworn by me before the commencement of such
8 deposition and that such deposition was taken
9 virtually and is a true record of the testimony
10 given by such witness.
11
12 I further certify that the adverse party,
13 SAMSUNG ELECTRONICS CO., LTD., was represented by
14 counsel at the deposition.
15
16 I further certify that the deposition of
17 ANDREW WOLFE, Ph.D., occurred virtually, on Friday,
18 May 15, 2026, from 11:57 a.m. to 3:28 p.m. EDT.
19
20
21
22

1 I further certify that I am not related to
2 any of the parties to this action by blood or
3 marriage, I am not employed by or an attorney to any
4 of the parties to this action, and that I am in no
5 way interested, financially or otherwise, in the
6 outcome of this matter.
7
8 IN WITNESS WHEREOF, I have hereunto set my
9 hand this 19th day of May, 2026.
10
11 My commission expires:
12 October 31, 2027
13
14
15 ----------
16 E-NOTARY PUBLIC IN AND FOR THE
17 COMMONWEALTH OF VIRGINIA
18
19
20
21
22

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