

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner

v.

NETLIST, INC.,
Patent Owner

Case PGR2025-00071
U.S. Patent No. 12,308,087

**DECLARATION OF MICHAEL C. BROGIOLI IN SUPPORT OF
PATENT OWNER'S RESPONSE**

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Netlist EX2058
Samsung v. Netlist
PGR2025-00071

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I, Michael C. Brogioli, hereby declare as follows.

I. INTRODUCTION

1. I have been retained as an expert witness on behalf of Patent Owner Netlist, Inc. (“Patent Owner”) for the above-captioned post-grant review (PGR). I am being compensated for my time in connection with this PGR at my standard consulting rate.

2. I understand that this Declaration accompanies the Patent Owner’s Response filed in this PGR involving U.S. Patent No. 12,308,087 (“the ’087 patent”) (EX1001), which resulted from U.S. Patent Application No. 17/694,649 (“the ’649 application”), filed on March 14, 2022. I understand that the ’087 patent claims a priority date of at least November 3, 2011. I refer to this date throughout this declaration.

3. In preparing this Declaration, I have reviewed the ’087 patent and each of the documents cited herein, in light of general knowledge in the art before November 3, 2011. In formulating my opinions, I have relied upon my experience, education, and knowledge in the relevant art. In formulating my opinions, I have also considered the viewpoint of a person of ordinary skill in the art (“POSA”) in the November 2011 time frame.

II. MY BACKGROUND AND QUALIFICATIONS

4. Below is a summary of my education and experience. My *curriculum*

*vita*e, included as Exhibit 2059 hereto, records my education, experience, and publications in greater detail.

5. I am currently an Adjunct Professor of Electrical and Computer engineering at Rice University in Houston, Texas, and Managing Director of Polymathic Consulting in Austin, Texas. I received my Bachelor of Electrical Engineering from Rensselaer Polytechnic Institute in 1999, my Master of Science in Electrical and Computer Engineering from Rice University in 2003, and my Doctorate of Electrical and Computer Engineering from Rice University in 2007.

6. While at Rice University, I developed various computer architecture designs for embedded and high-performance systems, including memory systems. For example, from 1999 to 2003, I worked in the area of low-power computing, specifically focusing on dynamic power management and performance of configurable memory systems, including SRAM based caches. From 2002 to 2004, I developed Spinach, a computer architecture design and modeling toolset, which models system components common to all programmable computing environments, including memory systems, microprocessors, interconnects, etc. From 2004 to 2009, I developed Spinach DSP-FPGA, a modular and composable simulator design infrastructure for programmable and reconfigurable embedded SOC architectures specifically targeting mobile, low-power, and embedded and portable computing devices. From 2005 to 2009, I developed and published a

retargetable compiler infrastructure and hardware design exploration toolkit for systems related to embedded computing technologies, which is also used in the design space exploration of memory systems and related technologies. Many of these tools have been used at United States universities in the area of electrical and computer engineering research.

7. In the late 1990s, I was a hardware and software developer at Vicarious Visions in New York, developing third-party titles for Nintendo's handheld consoles, in addition to various hardware interfaces and software optimizations related to the limited memory I/O and size. During my career, I have served as Chief Technology Officer, advisory board, and board of directors member, often in co-founding roles.

8. From June 2006 to August 2007, I worked as the Technical Co-Founder of Method Seven LLC in Boston, MA, working with high-performance software and hardware systems architecture. I am currently a co-founder, co-inventor, and Chief Technology Officer of Network Native, an Internet of Things technology company as well as others that are detailed on my CV (Exhibit 2059).

9. I have held the position of Adjunct Professor at Rice University since 2009 and the position of Managing Director at Polymathic Consulting since 2011. At Rice University, I instruct graduate-level curriculum in the areas of computer architecture, hardware and software systems. I also advise on university research

and various design initiatives. At Polymathic Consulting, I work with a range of technologists from early-stage start-ups to Fortune 500 companies on similar technologies.

10. From 2008 to 2009, I was Senior Engineer working in high-performance compiler designs and next-generation microprocessors and architectures at Freescale Semiconductor in Austin, TX. From November 2009 to October 2011, I was Chief Architect, Senior Member Technical Staff, at Freescale Semiconductor in Austin, TX (formerly Motorola), responsible for management of technology, engineering roadmaps, design lead on software infrastructure, and next-generation microprocessor architectures for embedded computing. During my tenure at Freescale Semiconductor, I was in charge of system developer tools for processor design, both in the hardware and software spaces. These included tools used for the programming of processors, simulation and design of processors, and related technologies.

11. I have previously worked for Texas Instruments' Advanced Architecture and Chip Technology division in Houston, Texas, in the areas of high-performance mobile and embedded systems design at the hardware and systems software level, specifically around heterogeneous computing, high-speed bus, and interconnect technologies. I also have worked at Intel Corporation's Microprocessor Research Labs in the areas of computer architecture and compiler

technologies.

12. I am recognized as an expert in the field of computer architecture, computer hardware and computer software systems as they relate to the subject matter at hand. I am a member of the Institute of Electrical and Electronics Engineers (IEEE) and have been a Program Committee member for the IEEE and ACM Design Automation Conference since 2011, and have held the role of Program Chair of Design Automation Conference in the area of Embedded Computing.

13. Over the past 20 plus years, I have authored numerous peer-reviewed publications, as well as engineering books in the area of computer hardware and software design. Many of these incorporate technologies specific to the subject matter at hand, including memory system design, optimization for memory systems, and interconnect technology. These publications are disclosed in my *curriculum vitae*, attached as Exhibit 2059. I have previously served as an engineering consultant and testifying witness on matters related to, and including, microprocessors, chip technology, memory systems, memory modules and related aspects of JEDEC standards, as well as various memory and interconnect technologies. My curriculum vitae contains more information on my background and experience, as well as the cases in which I have served as an expert witness over at least the past four years.

14. I am also a named inventor on the following United States patents and patent applications: U.S. Pat. Nos. 11,526,180; 11,354,757; 11,340,877; U.S. Pat. Appl. No. 17/060,025 (U.S. Publication No. 2021/0099522); and U.S. Pat. Appl. No. 15/110,643 (U.S. Publication No. 2016/0328993). More information regarding the patent applications for which I am a named inventor can be found in my *curriculum vitae*, attached as Exhibit 2059.

15. I have extensive firsthand experience with the technology underlying the '087 patent. I have worked with various SRAM and DRAM technologies, including software and systems optimization related to size and performance of such memories, since the late 1990s. My development of various embedded systems work in the late 1990s include SRAM technologies and high speed access of said systems. Further work in the late 1990s included optimization of memory intensive applications for efficient high performance usage of SRAM and DRAM memory systems, and optimizations for memory system I/O. My work in the early 2000s was around the use of configurable memory systems and caches comprised of SRAM technologies, and the optimization of memory accesses to maximize CPU compute throughput. I have designed memory system architectures, and system simulation and design technologies both in my doctoral research and publications, as well as within my various roles in industry going back to the early and mid-2000s. I am also familiar with non-volatile memory systems, such as

those based on NAND or NOR.

III. SUMMARY OF OPINIONS

16. It is my opinion that there is sufficient written description support for claims 1-28 of the '087 patent, both in the specification as filed and through the priority chain back to the earliest non-provisional application 13/288,850 filed on November 3, 2011.

17. It is my opinion that independent claim 24 contains a clear typographical error, and as properly understood by a POSA, claims 24-28 are not indefinite.

18. It is my opinion that claims 1-28 of the '087 patent would not have been obvious over the combinations that Samsung and Dr. Wolfe propose in Grounds 3 and 4.

IV. LIST OF DOCUMENTS CONSIDERED

Exhibit/Paper No.	Description
1	Petition for Post-Grant Review of U.S. Patent No. 12,308,087
1001	U.S. Patent No. 12,308,087
1002	File History of U.S. Patent No. 12,308,087 (Application No. 17/694,649), <i>available at</i> ">https://patentcenter.uspto.gov/applications/17694649/ifw/docs?application=>
1003	Declaration of Dr. Andrew Wolfe

Exhibit/Paper No.	Description
1006	File History of U.S. Patent Application No. 14/337,168 (filed July 21, 2014)
1007	File History of U.S. Patent Application No. 15/095,288 (filed Apr. 11, 2016)
1008	File History of U.S. Patent Application No. 15/602,099 (filed May 22, 2017)
1009	File History of U.S. Patent Application No. 16/412,308 (filed May 14, 2019)
1010	File History of U.S. Patent Application No. 17/157,903 (filed Jan. 25, 2021)
1018	U.S. Patent Application Publication No. 2010/0195364 to Riho (published Aug. 5, 2010) (“Riho2”)
1047	U.S. Patent No. 9,123,552 to Keeth <i>et al.</i> (filed Mar. 30, 2010, issued Sept. 1, 2015)
1048	U.S. Patent No. 9,665,507 to Shaeffer <i>et al.</i> (provisional filed July 22, 2010, nonprovisional filed May 11, 2011, issued May 30, 2017)
1070	File History of U.S. Patent No. 8,787,060 (Application No. 13/288,850 filed Nov. 3, 2011)
1089	Netlist’s infringement contentions against Samsung in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:25-cv-00557 (E.D. Tex. July 16, 2025) (U.S. Patent No. 12,308,087)
1091	Declaration of Dr. Andrew Wolfe in IPR2022-01427 (EX1003 in IPR2022-01427)
2060	Transcript of the Deposition of Andrew Wolfe, Ph.D., May 22, 2026

Exhibit/Paper No.	Description
2132	Redacted Version of Samsung Respondents' Second Supplemental Objections and Responses to Complainant Netlist's First Set of Interrogatories (Nos. 1-38), Certain Dynamic Random Access Memory (DRAM) Devices, Products Containing the Same, and Components Thereof, Inv. No. 337-TA-1472 (ITC), March 25, 2026
2146	Redline Comparison of U.S. Patent Application No. 13/288,850 to U.S. Patent Application No. 14/337,168
2147	Redline Comparison of U.S. Patent Application No. 13/288,850 to U.S. Patent Application No. 15/095,288
2148	Redline Comparison of U.S. Patent Application No. 13/288,850 to U.S. Patent Application No. 15/602,099
2149	Redline Comparison of U.S. Patent Application No. 13/288,850 to U.S. Patent Application No. 16/412,308
2150	Redline Comparison of U.S. Patent Application No. 13/288,850 to U.S. Patent Application No. 17/157,903
2151	Redline Comparison of U.S. Patent Application No. 13/288,850 to U.S. Patent Application No. 17/694,649

V. LEGAL UNDERSTANDING

A. My Understanding of Priority Law and the Written Description Requirement

19. I understand each claim must be analyzed to determine its effective priority date by comparing each of its elements to the application it is in and/or any priority applications.

20. I understand that in order for a claim to claim priority to a previously

filed application, the claim must have written description support in that priority document and the written description needs to have been carried over into the application the claim appears in.

21. I understand that the written description provided by a patent specification must convey clearly to a POSA that the applicant was in possession of the claimed invention as of the patent's filing date or as of the filing date of a related earlier-filed application if the patent owner would like to receive the benefit of that earlier date (here, I have been asked to assess the '087 patent's written description as of the filing date of the earlier '850 related application: November 3, 2011). And I understand that this involves an objective inquiry into the disclosure provided in the specification from the perspective of a POSA as of November 3, 2011.

22. I understand "possession" of the claimed invention does not mean physical possession and does not require making or testing the invention. Possession of the claimed invention is shown by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. I also understand that written description support must be explicit, expressed, or inherent in the priority document. The support cannot merely obviously flow from the priority document.

23. I further understand that this written description requirement must be assessed in view of the state of the knowledge of a POSA in the art. In addition, I understand that a patent specification is written for a POSA and that such a hypothetical person presumably has all of the knowledge of the state of the art as of the patent's filing date, in addition to the knowledge provided by the patent specification itself.

24. I understand that there is sufficient (i.e., adequate) written description support when a POSA can visualize or recognize the full scope of the claimed subject matter and that the claimed subject matter need not be provided verbatim in a specification. I also understand that a skilled artisan comes to the patent with knowledge in the art, therefore, it is unnecessary to spell out every detail of the invention in the specification for a skilled artisan to conclude that there is written description support.

B. My Understanding of Claim Construction

25. I understand that during an *inter partes* review proceeding, claims are to be construed in light of the specification as would be read by a person of ordinary skill in the relevant art at the time the application was filed. I understand that claim terms are given their ordinary and customary meaning as would be understood by a person of ordinary skill in the relevant art in the context of the entire disclosure. A claim term, however, will not receive its ordinary meaning if

the patentee acted as his own lexicographer and clearly set forth a definition of the claim term in the specification. In this case, the claim term will receive the definition set forth in the patent.

C. My Understanding of Obviousness

26. I understand that a patent claim is invalid if the claimed invention would have been obvious to a POSA at the time the application was filed. This means that even if all of the requirements of the claim cannot be found in a single prior art reference that would anticipate the claim, the claim can still be invalid.

27. To obtain a patent, a claimed invention must have, as of the priority date, been nonobvious in view of the prior art in the field. I understand that an invention is obvious when the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a POSA at the time the invention was made.

28. I understand that to prove that prior art or a combination of prior art renders a patent obvious, it is necessary to:

(1) identify the particular references that, singly or in combination, render the patent obvious;

(2) specifically identify which elements of the patent claim appear in each of the asserted references; and

(3) explain how the prior art references would have been combined or

modified in order to create the inventions claimed in the asserted claim.

29. I also understand that prior art references can be combined under several different circumstances. For example, it is my understanding that one such circumstance is when a proposed combination of prior art references results in a system that represents a predictable variation, which is achieved using prior art elements according to their established functions.

30. I also understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight when considering the prior art. I understand this test should not be rigidly applied, but that the test can be important to avoid such hindsight. I also understand that, when combining references, characterizing the references as “primary” and “secondary” is merely a matter of presentation with no legal significance. For instance, whether a combination is presented as reference A in view of reference B or reference B in view of reference A does not affect the underlying obviousness considerations for a patent claim.

31. I understand that certain objective indicia can be important evidence as to whether a patent is obvious or nonobvious. Such indicia include:

(1) commercial success of products covered by the patent claims; (2) a long-felt need for the invention; (3) failed attempts by others to make the invention;

(4) copying of the invention by others in the field; (5) unexpected results achieved by the invention as compared to the closest prior art; (6) praise of the invention by the infringer or others in the field; (7) the taking of licenses under the patent by others; (8) expressions of surprise by experts and those skilled in the art at the making of the invention; and (9) the patentee proceeded contrary to the accepted wisdom of the prior art.

32. I also understand that “obviousness” is a legal conclusion based on the underlying factual issues of the scope and content of the prior art, the differences between the claimed invention and the prior art, the level of ordinary skill in the prior art, and any objective indicia of non-obviousness.

33. For that reason, I am not rendering a legal opinion on the ultimate legal question of obviousness. Rather, my testimony addresses the underlying facts and factual analysis that would support a legal conclusion of obviousness or non-obviousness, and when I use the term obvious, I am referring to the perspective of one of ordinary skill in the art at the time of invention.

D. A Person of Ordinary Skill in the Art

34. I understand that a person of ordinary skill in the relevant art (“POSA”) is presumed to be aware of all pertinent art, thinks along conventional wisdom in the art, and is a person of ordinary creativity—not an automaton.

35. I have been asked to consider the level of ordinary skill in the field

that someone would have had at the time the claimed invention was made. In deciding the level of ordinary skill, I considered the following:

- the levels of education and experience of persons working in the field;
- the types of problems encountered in the field; and
- the sophistication of the technology.

36. My opinion below explains how a POSA would have understood the technology described in the references I have identified herein around the April 14, 2008 timeframe, which I have been advised is the earliest possible effective filing date for the '731 patent.

37. Regardless of whether I use “I” or a “POSA” during my technical analysis below, all of my statements and opinions are to be understood to be based on how a POSA would have understood or read a document at the time of the alleged invention.

VI. THE '087 PATENT

A. Overview

38. The '087 patent discloses and claims an innovative arrangement of stacked dies and interconnects used in Netlist's high-bandwidth memory (“HBM”) technology. *See* EX1001, 1:32-35, 2:36-60. Conventional dynamic random access memory (“DRAM”) packages often consist of a single silicon chip (or “die”)

housed in a plastic or ceramic package. To increase the capacity of individual memory devices, memory makers began “stacking” multiple dies in a single DRAM package where each DRAM interfaces with an external device (such as a host) through external connections such as long, dangling wires along the peripheral of the DRAM circuit. *See* EX1001, 1:46-2:24. But the high electrical load resulting from such external connections negatively affected performance. EX1001, 2:25-32.

39. For example, the '087 patent's background section describes an existing memory package of Figure 1A, which shows memory package 100 with control die 130 and three array dies 110. EX1001, 1:46-60. Control die 130 has driver 134, which drives data signals from control die 130 to each array die via interconnect 142, and driver 140, which drives command and address signals to each array die. EX1001, 1:51-58.

40. The '087 patent explains that “a load exists on each of the drivers 134, 140 ... by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies.” EX1001, 2:25-28. It further explains that “to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver” and that “a larger driver not only consumes more space on the control die, but also consumes more power.” EX1001, 2:28-32.

41. The '087 patent discloses reducing driver size and power consumption “by increasing the number of die interconnects and reducing the number of array dies that are in electrical communication with each die interconnect.” EX1001, 4:3-7. The '087 patent illustrates an exemplary configuration in Figure 2, reproduced below, which shows memory package 200 with control die 230 and four array dies 210a–210d. EX1001, 4:62-63. Control die 230 is connected to array dies 210a and 210b by die interconnect 220a, as shown by the darkened circles. EX1001, 5:7-53. Die interconnect 220b connects control die 230 to array dies 210c and 210d, as shown by the darkened circles, but die interconnect 220b is not electrically connected to array dies 210a and 210b, as shown by the unfilled circles. EX1001, 5:61-6:8. The '087 patent explains, “[e]xamples of die interconnects include, but are not limited to, through-silicon vias (TSV), conducting rods, wire bonds, and pins.” EX1001, 5:35-37.

VII. THE ASSERTED REFERENCES

A. Keeth

43. Keeth describes a stack of memory dice connected to an interface die. Keeth's system enables "concurrent communication between [the] interface die and a plurality of die stacks" using "interleaved conductive paths in stacked devices," such that "a vault control circuit may concurrently communicate with (e.g., access and send data to) multiple partitions in the vault and thereby improve bandwidth." EX1047, Title, 4:12-15.

44. Keeth describes in Figure 1 (below, annotated) that the control circuit 130 is part of the interface die 110 and the control circuit 130 assigns and retains ID information. EX1047, 3:20-28. Keeth states that "[t]he conductive paths 106 may communicate (e.g., transfer) information such as data, address, control, ID information, among other information." EX1047, 3:5-8. Keeth explains that "control circuit 130 of interface die 110" may "be configured to assign ID information during initialization of the stack 102" and "operate to retain the assigned ID information after the initialization of the stack 102, such as in order for control circuit 130 to reference each die 120 through 123 by the ID information." EX1047, 3:26-33.

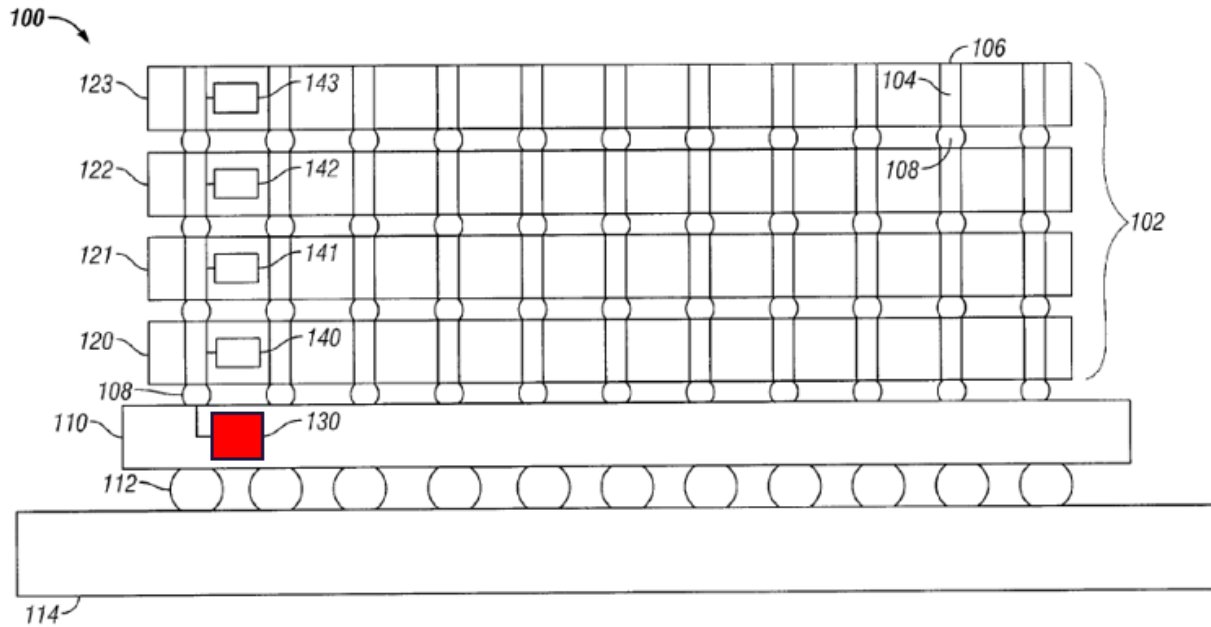


FIG. 1

EX1047, FIG. 1 (annotated).

45. Keeth describes that “each memory die in a dice stack may be divided into a plurality of partitions” that are “vertically aligned across multiple dice in the stack” to form a “vault.” EX1047, 1:65-2:6. Keeth explains, “[t]he partitions of a vault may share address and command control connections (e.g., TSVs) and input/output data pins among other connections, and each partition may have a different chip select line to prevent data contention.” EX1047, 2:6-10.

46. Keeth depicts this configuration in Figure 2, which shows four dice (220-223) each having four memory partitions (e.g., 204). EX1047, 3:44-54. Figure 2 also shows four vaults (e.g., 206), each having four memory partitions (one from each dice) and a vault control circuit 212 that are vertically stacked. EX1047, 3:44-54. The memory partitions in a vault share vertical communicative

paths 208 that couple each memory partition of the vault to the vault control circuit. EX1047, 3:44-54. In Figure 2 of Keeth, any data terminal used to exchange data with an external device (e.g., memory controller) would be located at the bottom of interface die 210. See EX1047, FIG. 3 (showing interface die 310 and bumps 312).

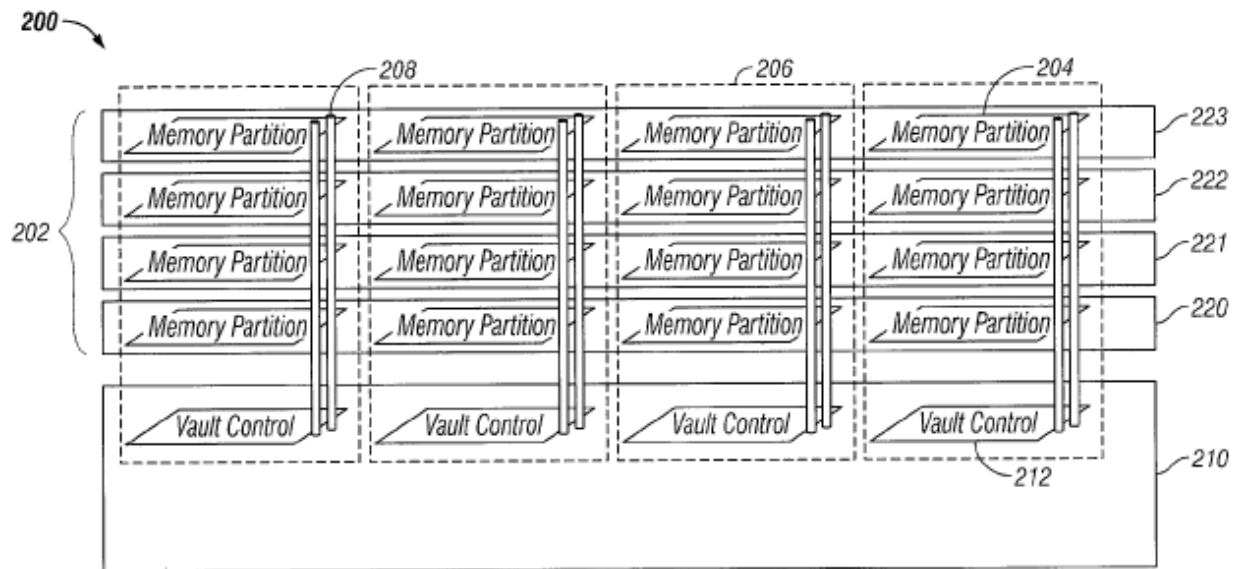


FIG. 2
EX1047, FIG. 2

47. In Figure 5, Keeth discloses a memory package that incorporates “partition interleaving.” EX1047, 5:24-26; *see also* EX1047, 6:53-57 (Figure 7). Keeth teaches that “[a]lternating dice in the stack 502 may be part of separate vaults. For example, the first and third dice 520 and 522 along with respective I/O circuits and the conductive path 505 and 507 may be a part of a first vault while second and fourth dice 521 and 523 along with respective I/O circuits and

conductive paths 506 and 508 may be part of a second vault.” EX1047, 6:11-16.

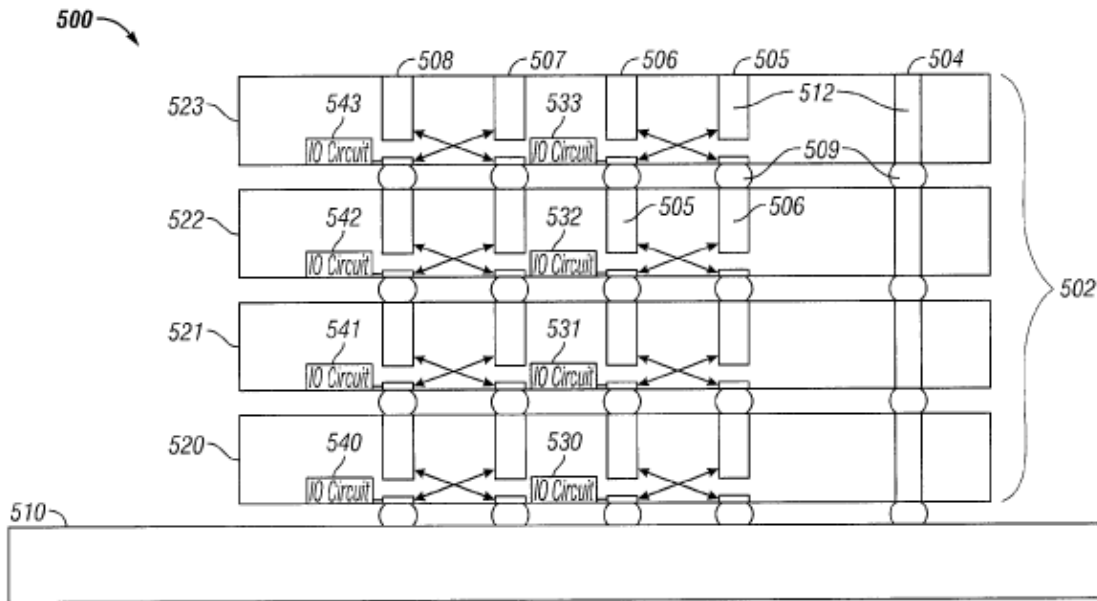


FIG. 5

EX1047, FIG. 5

48. Additionally, Keeth’s interleaving conductive paths are expressly depicted as bi-directional with double-headed arrows in Figure 5. EX1047, FIG. 5. Keeth states that “the command circuits and/or address circuits of each dice 520 through 523 may be connected to and utilize the interleaving conductive paths 505 through 508 in order to communicate command and/or address signals.” EX1047, 6:4-10; *see also* EX1047, 3:5-9 (stating that the conductive paths “may communicate (e.g., transfer) information such as data, address, control, ID information, among other information.”). In other words, Keeth teaches transmitting unidirectional signals, such as command and address signals that are transmitted from the interface die to one or more of the dice, using bidirectional

interconnects. Keeth also states that the interleaving conductive paths 505 through 508 “allow[] the interface die 510 to concurrently access the first and second vaults and concurrently drive data to partitions within the vaults.” EX1047, 6:17-19.

B. Shaeffer

49. Shaeffer focuses on a “protocol including a command-specified timing reference signal” that provides timing information “to the memory controller from individual ranks to make timing updates to compensate for the noise and drift of the rank” “after the rank has been idle for a time period.” EX1048, Title, 1:67-2:3, 2:29-34.

50. Schaeffer describes that “[a]t any given time at most one rank is actively accessed, while all other ranks are idle but still consuming idle power” and “power can be saved by moving timing control components ... from the ranks to the memory controller.” EX1048, 1:59-67. Shaeffer’s timing reference signal is “a calibration preamble” “for a rank which is being accessed for the first time after an idle period” “to compensate for low-frequency timing drifts and timing jitter” EX1048, 2:50-59, 4:21-23. Shaeffer defines that “‘ranks’ are used to refer to 1 or more memory devices which are accessed and ... transfers data for a given data access operation.” EX1048, 3:11-14. Shaeffer also explicitly states that “the calibration preamble is only requested when the first transaction to a newly accessed rank is a read access.” EX1048, 3:5-7.

51. Shaeffer uses “the terms ‘timing reference signal (TRS)’, ‘calibration preamble’ and ‘preamble’ ... interchangeably.” EX1048, 3:9-11. Shaeffer teaches that the preamble (or TRS) is transmitted from the memory ranks to the memory controller. *See, e.g.*, EX1048, 2:64-3:1 (the “TRS ... is conveyed from the memory device, to the memory controller” via the same “signaling resource” as the EDC), 4:23-26 (“transmitting a timing reference signal (TRS) from the rank to the memory controller”), 5:60-67, FIG. 1A (below, showing EDC signal transmitted from memory ranks to memory controller), FIG. 3 (showing preamble sent from memory rank to memory controller ahead of read data).

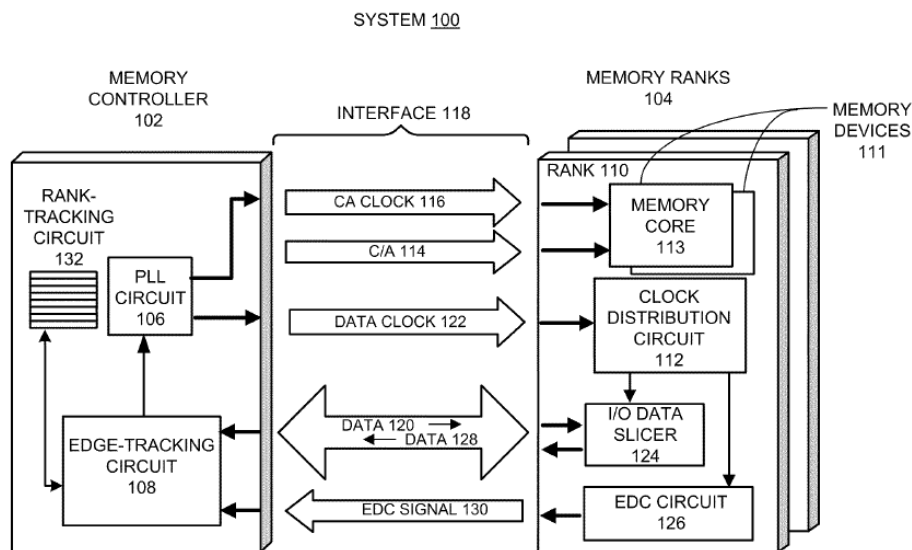


FIG. 1A

EX1048, FIG. 1A

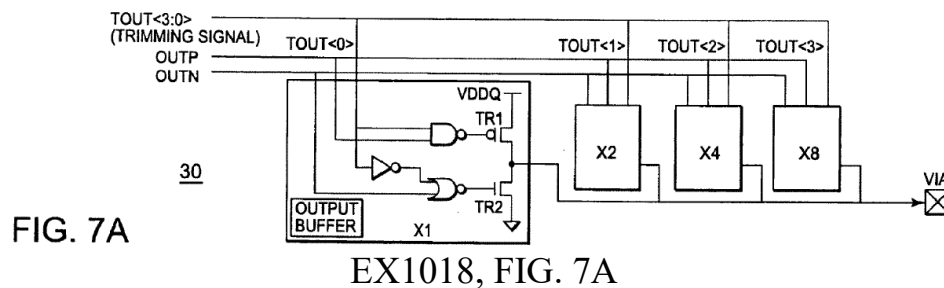
C. Riho2

52. Riho2 describes a DRAM “formed by stacking a plurality of chip dies,” in which each chip die includes “TSVs (Through-Silicon Vias)” and

“mutually connected by a technique using bumps or ... the TSV technique.”

EX1018, [0003], [0037]. Riho2’s FIG. 7A (below) shows “a circuit configuration for optimizing the output drive capacity of output buffers” “according to a change in the time constant caused by parasitic capacitance and parasitic resistance.”

EX1018, [0097]. Riho2 states that “there are provided four output buffers X1, X2, X4, and X8 having mutually different drive capacities.” EX1018, [0097].



VIII. THERE IS WRITTEN DESCRIPTION SUPPORT FOR THE '087 PATENT CLAIMS IN THE PRIORITY APPLICATION AND THROUGH THE PRIORITY CHAIN

A. The '087 application priority chain

53. The '087 patent was filed March 14, 2022, as application No. 17/697,649. EX1001, (22); *see* EX1002, 11-44 (as-filed '649 specification).
54. The earliest non-provisional application in the '087 patent’s priority chain is application No. 13/288,850, filed on November 3, 2011. *See* EX1070, 4-42 (as-filed '850 application).
55. Application No. 14/377,168 was filed as a continuation of the '850 application on July 21, 2014. *See* EX1006, 5-41 (as-filed '168 application).

56. Application No. 15/095,288 was filed as a continuation of the '168 application on April 11, 2016. *See* EX1007, 8-44 (as-filed '288 application).

57. Application No. 15/602,099 was filed as a continuation of the '288 application on May 22, 2017. *See* EX1008, 8-43 (as-filed '099 application).

58. Application No. 16/412,308 was filed as a continuation of the '099 application on May 14, 2019. *See* EX1009, 15-49 (as-filed '308 application).

59. Application No. 17/157,903 was filed as a continuation of the '308 application on January 25, 2021. *See* EX1010, 22-56 (as-filed '903 specification).

60. The '649 application, from which the '087 patent issued is a continuation of the '903 application. EX1001, (63).

B. There is written description support for the '087 patent claims.

61. In my opinion, the '087 specification provides sufficient description to reasonably convey to a POSA that the inventors were in possession of the inventions recited in claims 1-28 of the '087 patent.

62. In the chart attached as **Appendix A**, which I incorporate by reference fully herein, I provide citations to portions of the '087 patent specification that support each of claims 1-28 of the '087 patent. The chart also includes parallel citations to the corresponding portions of the earliest non-provisional application, the '850 application, which issued as U.S. Patent No. 8,787,090 ("the '060 patent").

63. Each of the intervening priority applications also contains support for claims 1-28 of the '087 patent. As seen in Exhibits 2146 - 2151, the specification of each application in the priority chain is substantially the same as the as-filed '850 specification.

C. Dr. Wolfe's general contentions regarding the lack of disclosure of the specifically claimed embodiments are factually flawed.

1. The '087 patent describes alternative features and explicitly links the disclosed embodiments.

64. I understand that Samsung argues “[a] patent owner cannot show written description support by picking and choosing claim elements from different embodiments that are never linked together in the specification.” Pet., 13.

65. In my opinion, the support for the '087 claims does not come from disparate unlinked embodiments. Instead, the specification describes alternative features that may (or may not) be included in the disclosed memory packages and explicitly links the disclosed embodiments.

66. As shown in the chart in **Appendix A**, the support for the claims is provided in the discussion of Figures 2-4 and 8. Figures 2 and 3 each illustrate an exemplary memory package. EX1001,¹ 3:31-37. Figure 4 illustrates an exemplary

¹ For convenience, citations in the written description discussion are to the as-published '087 patent specification, which was not amended during prosecution, *see*

driver structure. EX1001, 3:37-39. Figure 8 illustrates an exemplary memory module. EX1001, 3:49-51.

67. The Specification explicitly connects Figures 2 and 3, noting that “some or all of the embodiments described above with respect to the memory package 200 [of Figure 2, below] may be applicable to the memory package 300 [of Figure 3, below]. However, for ease of illustration and to simplify discussion, certain elements are omitted in FIG. 3 Nevertheless, it should be understood that the memory package 300 can include the same or similar elements as described above with respect to the memory package 200.” EX1001, 9:65-10:9.

EX1002. As I note above, Exhibits 2146-2151 demonstrate that each of the as-filed specifications throughout the priority chain include substantially the same disclosure.

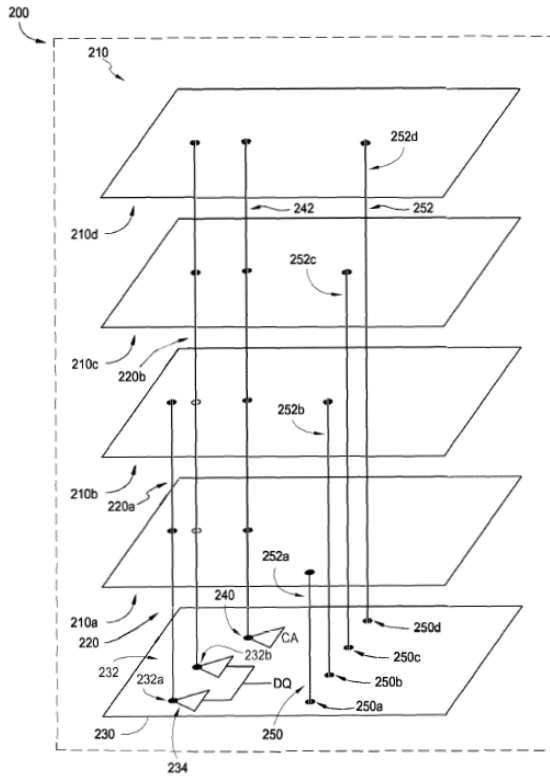


FIG. 2

EX1001, FIG. 2

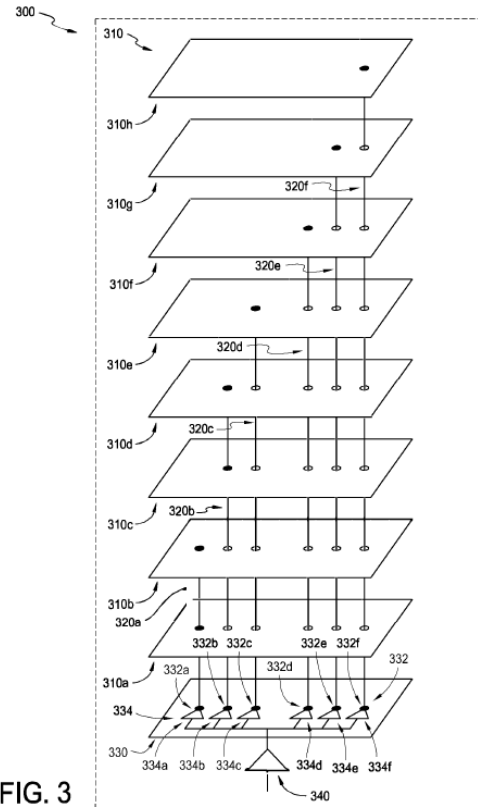


FIG. 3

EX1001, FIG. 3

68. The Specification also explicitly connects the exemplary driver structure 400 of Figure 4, below, to the control die 230, 330 of Figures 2 and 3, respectively. *See* EX1001, 15:7-20. In particular, the Specification describes that “the control die 230 [of Figure 2] may include the driver structure 400 in place of the combination of drivers 232a and 232b. Similarly, ... the control die 330 [of Figure 3] may include a structure similar to the driver structure 400 in place of the drivers 334.” EX1001, 15:13-18.

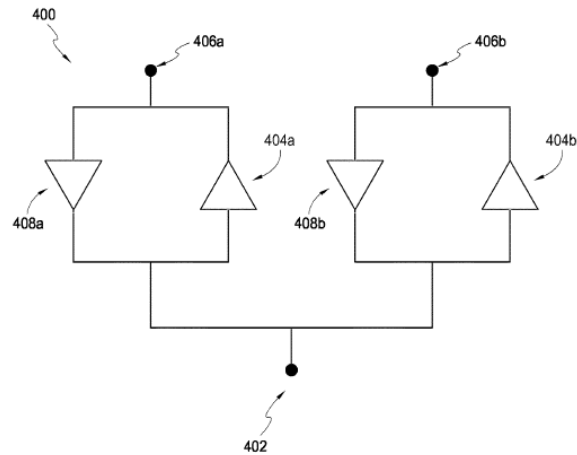


FIG. 4

EX1001, FIG. 4

69. The Specification also explicitly connects the embodiment of Figure 8, below, to those of Figures 2 and 3. In discussing Figure 8, the Specification describes that “[i]n certain embodiments, the control dies 822 can include some or all of the embodiments described above with respect to the control dies 230 and 330 [of Figures 2 and 3, respectively]. Moreover, in certain embodiments, the memory packages 820 can include some or all of the embodiments described above with respect to the memory package 200 and 300,” thus explicitly connecting the disclosure of Figure 8 to that of Figures 2 and 3. EX1001, 21:7-13.

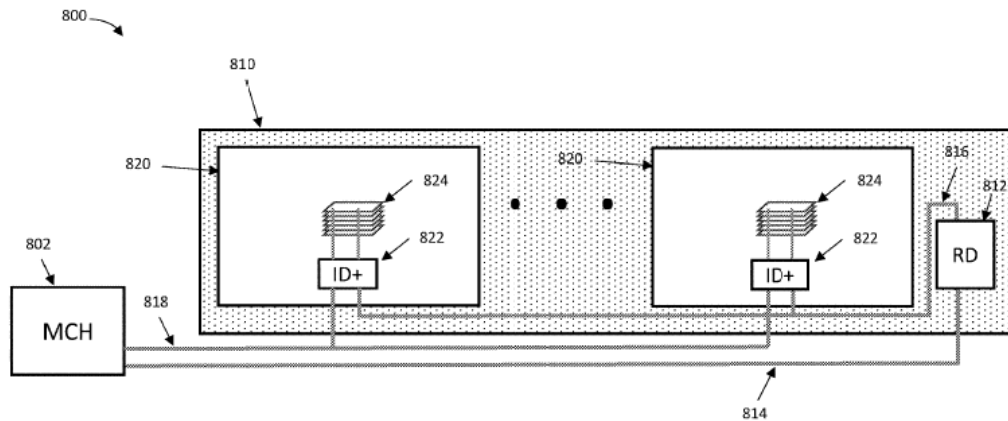


FIG. 8

EX1001, FIG. 8

70. Based at least on these disclosures in the specification, a POSA would have understood that the embodiments described in Figures 2-4 and 8 are not disparate, unlinked embodiments. Instead, the different figures illustrate alternatives, and in my opinion a POSA would also have readily recognized how to select amongst these various disclosed alternatives to achieve the desired product. For example, a POSA would have understood that in the case of needing to transfer data/address/command signal(s) to and from an array die one may use drivers in both directions. Conversely, if a signal need only be communicated to an array die, or from an array die to a control die, drivers would only be necessary in the single direction of desired signal path. Another example is the use of memory cell technology, whereby a POSA would have understood and appreciated certain design choices that may result in the use of SRAM technology, while others may result in the use of DRAM technology for a given implementation.

71. Each of the '087 claims simply recite specific combinations of these disclosed alternative features. In my opinion, the '087 specification discloses a list of options, and claims a particular narrowed embodiment selected therefrom.

72. And the '087 patent explicitly teaches that various combinations of the disclosed features may be implemented by a POSA. For example, in addition to the specific linking disclosure identified above, the specification further recognizes that “*various equivalent modifications [of the specific disclosed embodiment] are possible within the scope of the invention, as those skilled in the relevant art will recognize,*” that “[t]he elements and acts of the various embodiments described above can be combined to provide further embodiments,” and that the described “embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms.” EX1001, 22:63-23:2 (emphasis added), 23:13-17, 23:31-36.

2. A POSA would not consider there to be over 100 million possible combinations of features, as Dr. Wolfe contends.

73. Dr. Wolfe contends that “the '087 Patent refers to various possibilities that could be combined in over 100 million different ways.” EX1003, ¶103. In my opinion, this contention ignores the reality of how a POSA would consider the disclosure of the '087 patent.

74. For example, Rows A and B of Dr. Wolfe's chart (EX1003, ¶103) merely identify known examples of memory dies and interconnects.. Based on these examples, a POSA would have recognized that certain aspects of the disclosed invention (e.g., die stacking and die interconnect configuration) were applicable to any of these types of memory and could use known interconnects.

75. Further, the signals identified in Row D of Dr. Wolfe's chart (EX1003, ¶103) are not alternatives but rather typical signals that may be used in memory such DRAM. For example, data, address, and command signals are not alternative implementations; they are known signals that are transmitted in a DRAM device. And row E of Dr. Wolfe's chart (EX1003, ¶103) merely lists interconnects that can carry those signals.

76. In my opinion, many of Dr. Wolfe's so-called "possibilities" are basic design choices and implementation options. Indeed, Dr. Wolfe acknowledged that selecting appropriate features for a desired application "depend[s] on the details of the situation" and "on what the problem is and what the analysis is and what the objectives are." EX2060, 36:5-19. In response to the question: "And would a person of ordinary skill in the art [have] been able to analyze the problem in order to achieve the objective?", he further acknowledged, "For some problems, yes." EX2060, 36:20-37:1.

77. In my opinion, it would have been well within the skill of a POSA to select appropriate combinations, including those recited in the '087 claims, *based on the options disclosed in the specification* and the desired results.

78. For example, Dr. Wolfe's Row A discusses various types of array dies, namely (1) DDR DRAM, (2) SDRAM, (3) flash, (4) SRAM, (5) GDDR SDRAM or (6) other graphics memory. EX1003, ¶103. A POSA would have realized that a memory device can be, and often is, comprised of a single type of memory technology such as DDR DRAM, or perhaps SRAM. In designing a DDR DRAM device, such as those used in high performance computing applications, a POSA would have recognized that 5 of the 6 alternatives listed in Dr. Wolfe's Row A would not be used in conjunction with DDR SDRAM. In a similar style, Dr. Wolfe's Row E contemplates bidirectional/unidirectional interconnects and conduits. A POSA again would have appreciated that there are specific signals within a memory system that may require bidirectionality, while others may only require unidirectionality. A command to a memory device, such as a read or write command, may only require the "unidirectional going up (e.g., from the control die up to the array die(s))" as the patent specification states. EX1003, ¶103. A POSA would not need to exhaustively assess each and every one of the alternative signal directionalities discussed throughout the '087 specification to appreciate the characteristics of a write command within the context of the patent.

D. Dr. Wolfe’s contentions regarding specific limitations also fail.

79. Dr. Wolfe also contends there is no written description support for specific limitations of the ’087 patent claims. EX1003, ¶¶46-148. I disagree for the reasons discussed below. In general, Dr. Wolfe’s contentions take an impermissibly narrow view of the disclosure that is divorced from how a skilled artisan would have understood the ’087 patent’s teachings.

80. As I explain below, there is sufficient written description support for each of the following limitations. My discussion focuses on claim 1, but a similar analysis would apply to the other identified claims. Indeed, Dr. Wolfe addresses the claims together as well and does not identify any differences between the various claims that would affect the analysis.

1. The disclosure supports “unidirectional interconnects/conduits for conducting signals down the stack.”²

81. Claim element [1.1] recites:

wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured

² The quoted text in the headings in subsections VIII.D.1-5 are Dr. Wolfe’s characterizations of the claim elements, not the actual claim language. I use the same terminology for convenience.

to conduct any signal from the control die to any of the stacked
DRAM dies;

EX1001, 24:62-67; *see also* claim elements [9.d.2], [9.j.1], [13.o], [20.j], [20.k],
[23.j], [23.k], [24.j].

82. I disagree with Dr. Wolfe’s opinion that the “claimed unidirectional interconnect/conduit for conducting signals only **down** the stack is not disclosed in the specification.” EX1003, ¶106; *also* EX1003, ¶¶109-114. I note that Dr. Wolfe recognizes that the specification supports unidirectional interconnects that transmit signals “up” the stack, which is correct. EX1003, ¶109; EX1001, 9:9-36, 14:40-51.

83. The specification’s disclosure regarding at least Figures 2 and 3, which are expressly linked, supports the claimed unidirectional interconnects. *See* EX1001, 9:65-10:9 (linking Figures 2 and 3. The specification expressly discloses a unidirectional interconnect for conducting signals “down the stack”:

Alternatively, the memory package 300 comprises one or more die interconnects 320 that are configured to **enable a signal to be driven to the array dies 310 without enabling a signal to be received from the array dies 310** (e.g., the die interconnects 320 may **not be bi-directional**). *In certain embodiments where one or more of the die interconnects 320 are not bi-directional, the memory package 300 may include additional die interconnects (not shown) that are in electrical communication with the one or more additional conduits or drivers and*

that are configured to enable a signal from the array dies 310 to be transmitted to the one or more additional conduits or drivers.

EX1001, 14:40-51 (emphasis added).

84. The first half of this quoted language describes claim element [1.m], i.e., unidirectional interconnects for conducting signals to the DRAM dies (“up the stack”). Here, the disclosure characterizes interconnects that are “not [] bi-directional” as (1) “enabl[ing] a signal to be driven to the array dies 310” (i.e., configured to conduct signals in one direction), (2) “without enabling a signal to be received from the array dies 310” (i.e., not configured to conduct any signal in the other direction). The second half of the quoted language (in italics) describes complementary claim element [1.l], at issue here, and uses parallel language to describe that these element [1.l] interconnects, likewise, “are not bi-directional.” This language, thus, teaches that these element [1.l] interconnects (1) enable signals to be transmitted from the DRAM dies downwards toward the additional conduits or drivers in the bottom logic die (“down the stack”) but (2) do not enable signals to be transmitted to the DRAM dies.

85. According to Dr. Wolfe, the disclosure quoted above is insufficient because it does not support additional bidirectional data interconnects. EX1003, ¶112.

86. But the specification expressly discloses that bidirectional data interconnects may also be included in the memory package. To start, the specification discloses that “*one or more* of the die interconnects 320 are configured to be bi-directional, thereby enabling a signal to be driven to the array dies 310 via the die interconnect 320, and to enable a signal received from the array dies 310 along the same die interconnect 320 to be transmitted to a corresponding conduit 332 of the control die 330.” EX1001, 14:33-40 (emphasis added). It further discloses that the signal can be (but is not limited) to a “data signal.” EX1001, 10:48-54. In my opinion, these disclosures provide support for element [1.1]’s requirement that “the die interconnects *further* include unidirectional interconnects.”

87. The specification also discloses: (1) with respect to Figure 2, data interconnects that may be “bi-directional,” EX1001, 9:6-10; *see* Pet., 25; and (2) that the memory package 300 of Figure 3 may include elements of the memory package 200 of Figure 2, EX1001, 9:65-10:9. A POSA would have understood that bidirectional data interconnects (of package 200) is one such element that could be included in package 300. In my opinion, the specification thus supports a DRAM package having one or more bidirectional data interconnects *and* one or more unidirectional (non-data) interconnects.

88. Accordingly, in my opinion there is written description support for claim elements [1.l], [9.d.2], [9.j.1], [13.o], [20.j], [20.k], [23.j], [23.k], and [24.j].

2. The disclosure supports “unidirectional first/second/fourth/sixth/eighth etc. signals.”

89. Claim elements [1.p.1] recites:

wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first unidirectional interconnects,

EX1001, 25:20-24. And claim element [1.p.2] recites:

in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.

EX1001, 25:24-28; *see also* claim elements [9.d.2], [9.e.2], [13.n], [20.l.1], [20.l.2], [23.l.1], [23.l.2], [24.m.2], [24.o.2], [24.n.2], [24.p.2].

90. I disagree with Dr. Wolfe’s opinion that there is no disclosure of the claimed “[first]/[second] signals,” in Claims 1, 13, 20, and 23, “one or more signals” in Claim 9, and “[second]/[sixth] signals” and “[fourth]/[eighth] signals” in Claim 24 (collectively the ‘Unidirectional Signals’) which are “conducted via unidirectional interconnects or driven by unidirectional conduits.” EX1003, ¶¶115-117, 120-121.

91. In [1.p.1] and [1.p.2], the “first signals” are “receive[d] ... via the first unidirectional interconnects” of claim element [1.l] and the “second signals” are “drive[n] ... via the second unidirectional interconnects” of claim element [1.m]. As I discussed above, the specification discloses the first unidirectional interconnects of element [1.l], *see* Section VIII.D.1, and Dr. Wolfe acknowledges that the specification discloses the second unidirectional interconnects, *see* EX1003, ¶109.

92. Further, the specification explicitly describes different types of signals, including “a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal.” *See* EX1001, 10:48-54. Dr. Wolfe contends that the claimed “first” and “second” signals are additional types of signal not explicitly disclosed. EX1003, ¶120. But a POSA would have understood that the claim language is simply distinguishing elements of the claim and not reciting an additional undisclosed signal type.

93. Accordingly, in my opinion there is written description support for claim elements [1.p.1], [1.p.2], [9.d.2], [9.e.2], [13.n], [20.1.1], [20.1.2], [23.1.1], [23.1.2], [24.m.2], [24.o.2], [24.n.2], and [24.p.2].

3. The disclosure supports “multiple types of interconnects with selective electrical communication.”

94. Claim element [1.f] recites:

wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;

EX1001, 24:20-24. And claim element [1.h.1] recites:

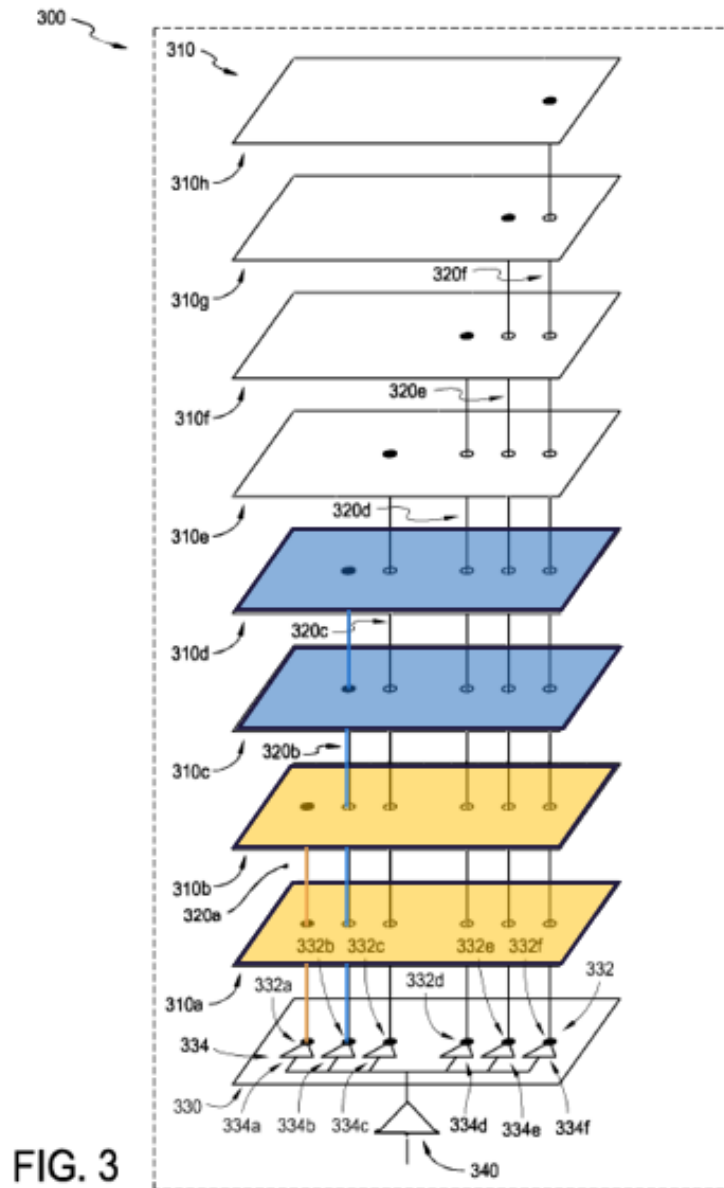
wherein a first data interconnect of the first data interconnects is in electrical communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies,

EX1001, 24:30-34. Claim elements [1.g] and [1.i] respectively recite similar limitations but for “a second C/A interconnect” and “a second data interconnect” in electrical communication with “the second plurality of DRAM dies” and not with “the first plurality of DRAM dies.” EX1001, 24:25-29, 24:46-50. *See also* claim elements [9.f.1], [9.g], [9.h], [9.i], [13.g], [13.h.1], [13.j], [13.k], [23.f.1], [23.f.2], [23.m.1], [23.m.2].

95. I disagree with Dr. Wolfe’s opinion that the ’087 specification does not provide support for these claim elements. *See* EX1003, ¶¶126, 129-132.

96. In the embodiment of Figure 3 (annotated below), the claimed “first plurality of DRAM dies” correspond to dies 310a/b (shown in blue) and the

claimed “second plurality of DRAM dies” correspond to dies 310c/d (shown in orange). As seen, die interconnect 320a (blue) is in electrical communication with only dies 310a/b; die interconnect 320b (orange) is in electrical communication with only dies 310c/d. EX1001, 10:10-47.



EX1001, FIG. 3 (annotated)

97. Dr. Wolfe contends the specification “does not disclose the combination of at least two different types of interconnects ... where each type of interconnect is in selective electrical communication with DRAM dies (or ports on those dies).” EX1003, ¶129. Pointing to Figure 3, Dr. Wolfe notes that “Figure 3 of the patent only shows selective electrical communication for *one* type of interconnect (i.e., for the signal supplied by the buffer 340).” EX1003, ¶129. Dr. Wolfe’s opinion takes an impermissibly narrow view of the disclosure.

98. Figure 3 is “for ease of illustration and to simplify discussion,” and the specification states that “certain elements are omitted in FIG. 3.” EX1001, 10:3-5. A POSA would have understood that this figure illustrates generally how interconnects (for accessing a single port per DRAM die) are connected to the stacked dies. A POSA would have further understood that Figure 3 is not intended to illustrate how many different types of interconnects are included in the memory package.

99. Indeed, the specification makes it clear that the signal (conducted by the die interconnects shown in Figure 3) “can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few.” EX1001, 10:48-50. Because more than one type of these signals are used to operate the DRAM dies, the specification makes clear that different types of die interconnects are included in the memory package and that

each type of die interconnects can be configured as shown in Figure 3. From this disclosure, a POSA would have immediately recognized that Figure 3 illustrates a single port and interconnect per DRAM die only for simplicity. *See* EX1001, 10:3-5.

100. Further, the disclosure specifically recognizes “[e]ach of the array dies 310 may *include one or more ports* (not shown) that enable electrical communication between the circuitry of the array dies 310 and *one or more die interconnects* 320.” EX1001, 10:14-17 (emphasis added). And, as discussed above, the signal can be any number of signal types, including “*a data signal*” or “*a command or address signal*” as relevant here. EX1001, 10:48-50 (emphasis added).

101. Dr. Wolfe further contends:

there is no disclosure of the unusual requirement in claims 1 and 9 that there are “first” and “second” “C/A interconnects” in selective electrical communication with ports of the DRAM dies, but ***both*** the “first set of C/A signals” ***and*** the “second set of C/A signals” are conducted on the “***first*** C/A interconnects” (while other signals may be on the “***second*** C/A interconnects”).

EX1003, ¶131.

102. The relevant claim language at claim element [1.d] recites:

die interconnects including C/A interconnects and data interconnects,
the C/A interconnects including at least first C/A interconnects and

second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals, EX1001, 23:62-67. Dr. Wolfe contends this is an “unusual requirement,” but completely ignores how memory typically operates. *See, e.g., also* EX1001, 2:3-6 (describing typical read/write operations). For example, a POSA would have readily been aware of JEDEC standards for DRAM memory devices that expressly disclose various types of read and write operations to memory. In the case of DRAM type devices, the JEDEC standards disclose the various signaling formats within the RAS, CAS, CS and WE signals that encode various of the read and write commands supported by a given DRAM technology.

103. In my opinion, a POSA would have understood from the clear language of the claim that the “first” and “second” C/A signals are both conducted on the “first C/A interconnects,” and are respectively associated with read and write operations (see element [1.c.2]) for the first plurality of DRAM dies (see element [1.f]). This is consistent with typical memory operation, in which read and write operations occur at different times, and a DRAM die would receive C/A signals associated with read *and* write operations (albeit at different times) in order to function as intended. And, as Dr. Wolfe correctly notes “other signals may be on the ‘second C/A interconnect,’” EX1003, ¶131—these other signals (e.g., C/A signals associated with read and write operations for the second plurality of

DRAM dies (see element [1.g])) are simply not recited in the open-ended claim 1.

104. Accordingly, in my opinion there is written description support for claim elements [1.f], [1.g], [1.h.1], [1.i], [9.f.1], [9.g], [9.h], [9.i], [13.g], [13.h.1], [13.j], [13.k], [23.f.1], [23.f.2], [23.m.1], and [23.m.2].

4. The disclosure supports “‘C/A signals’ that ‘do not include any chip select signal.’”

105. Claim element [1.k.2] recites “wherein the one or more C/A signals do not include any chip select signal.” EX1001, 24:59-61; *see also* claim elements [1.j]-[1.k.1], [18.a.1]-[18.a.2], [20.g]-[20.h.2], [23.g]-[23.h.2].

106. Dr. Wolfe contends the specification does not disclose this claim element. *See* EX1003, ¶¶133, 136-139. I disagree. In particular, Dr. Wolfe notes, “[t]he ’087 Patent provides affirmative examples of using the chip select signals, not prohibitions against including any chip select signal.” EX1003, ¶137 (citing EX1001, 15:31-40, 16:5-12).

107. As recited in claim element [1.k.1], which provides context for element [1.k.2], the “one or more C/A signals” are “received via one or more of the C/A terminals.” EX1001, 24:58-59. Dr. Wolfe’s opinion does not acknowledge this requirement. Instead, he contends that because the ’087 patent provides examples of using chip select signals, it cannot teach that the “one or more C/A signals do not include any chip select signal.” EX1003, ¶¶136-139.

108. The claim recites that the “one or more C/A signals” *that are* “received via one or more of the C/A terminals” “do not include any chip select signal.” Thus, the claim excludes chip select signals from being included in the received C/A signals. The Specification describes embodiments where chip select signals are *generated by* the control die (as opposed to being *received by* the memory package at the C/A terminals). See EX1001, 9:61-64 (“In some embodiments, the control die 230 may determine the array die 210 to select based on, for example, an address signal. In such embodiments, *the control die may generate the chip select signals.*” (emphasis added)). In this embodiment, the C/A signals received via the C/A terminals (which transmit signals to the memory package) do not include any chip select signal, as required by claim 1. Instead, the C/A signals received via the C/A terminals are an address signal. EX1001, 9:61-63. The chip select signal is then generated by the control die. EX1001, 9:63-64. This chip select signal is generated internal to the memory package and thus is not included in the C/A signal “received via one or more of the C/A terminals.”

109. Additionally, the '087 claims are directed to a “DRAM package,” such as the memory package 820 on memory module 810 in Figure 8. EX1001, 21:13-14. The specification also teaches embodiments that use “data path control signals,” which are not chip-select signals. EX1001, 21:4-7. The data path control signals are generated by the register device and may be received by the DRAM

package via dedicated signal lines instead of other C/A signals (which may include the chip select signals). EX1001, 21:41-47, 21:63-22:5, 22:12-17. These alternative embodiments also support the claimed feature.

110. Accordingly, in my opinion there is written description support for claim elements [1.j]-[1.k.2], [18.a.1]-[18.a.2], [20.g]-[20.h.2], and [23.g]-[23.h.2].

5. The disclosure supports that “the control die does not include emulation logic” in dependent claim 6.

111. Claim element [6.c] recites:

wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies

EX1001, 25:53-57; *see also* claim elements [20.m], [23.n]. Dr. Wolfe contends “[t]he specification of the ’087 Patent also does not provide written description for the negative limitation that ‘the control die does not include emulation logic.’”

EX1003, ¶143; *see also* EX1003, ¶¶140, 143-148. I disagree.

112. The specification explains that rank multiplication may be performed by the register device 812, which is outside of the DRAM package. EX1001, 22:18-21, FIG. 8. The specification also describes embodiments in which “the memory module 810 does not perform rank multiplication.” EX1001, 22:39-42.

113. A POSA would have known that “rank multiplication” is a type of “emulation logic.” Dr. Wolfe agrees. *See, e.g.*, EX1091, ¶161 (Dr. Wolfe testifying that rank multiplication is an emulation technique); EX2060, 70:22-72:2 (Dr. Wolfe confirming that the ’087 specification describes “rank multiplication” and that a POSA would have understood this to be a way to implement “emulation logic”).

114. Accordingly, in my opinion there is written description support for claim elements [6.c], [20.m], and [23.n].

E. Disclaimed claim 24 contains a clear drafting error.

115. In my opinion, disclaimed claim 24 contains a clear drafting error, as discussed below.

116. According to Samsung, the claimed “fifth” and “sixth,” signals are “self-conflicting,” and the “eighth” signals are “associated with two different operations.” Pet., 28-31. For example, Samsung argues:

The specification does not disclose any self-conflicting signals, like the “fifth signals,” that are associated with a *write* operation (i.e., going *up*), but sent *down* from the array die to the control die, and that contradiction also renders the claims indefinite.

Pet., 28.

117. Looking at the parallelism of claim elements 24.m to 24.p (see chart below), it is apparent the issues identified by Samsung are the result of a clear

drafting error. A POSA would have understood the claim should properly read as shown by the edits highlighted in yellow below:

24.m.1	in response to the first set of C/A signals , a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first die interconnects, a first subset of the second conduits is configured to receive first signals <i>associated with the first set of C/A signals</i> via a first subset of the second die interconnects and to drive the first signals to the interface; and
24.m.2	a first subset of the third conduits is configured to receive one or more second signals <i>associated with the first set of C/A signals</i> from a first subset of the third die interconnect and drive the one or more second signals to the interface;
24.n.1	in response to the second set of C/A signals , the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first die interconnects, the first subset of the second conduits is configured to receive third signals <i>associated with the second set of C/A signals</i> from the interface and to drive the third signals to the first subset of the second die interconnects; and
24.n.2	a first subset of the fourth conduits is configured to receive one or more fourth signals <i>associated with the second set of C/A signals</i> from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect;

24.o.1	in response to the third set of C/A signals , a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the <u>second third</u> set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface; and
24.o.2	a second subset of the third conduits is configured to receive one or more sixth signals associated with the <u>second third</u> set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface;
24.p.1	in response to the fourth set of C/A signals , the second subset of the first conduits is configured to drive the fourth set of C/A signals to the second subset of the first die interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the interface and to drive the seventh signals to the second subset of the second die interconnects; and
24.p.2	a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the <u>second fourth</u> set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth die interconnect;

118. A POSA would have immediately recognized the drafting error present in claim 24, as identified and corrected above. Indeed, Dr. Wolfe recognizes the clear error, asserting that claim 24 has “contradictory and nonsensical requirements.” EX1003, ¶¶122-125; *see also* EX2060, 55:5-17 (Dr.

Wolfe acknowledging that a POSA would have understood the claim as written “doesn’t make any sense”), 114:11-14 (Dr. Wolfe acknowledging that “even if [the claims] lack written description we can still understand the claims”).

119. Further, it is clear that the claim was intended to have been drafted with the parallel structure, as identified and shown in corrected form above. This makes the specific correction required clear to a POSA. This is confirmed by the prosecution history. Issued claim 24 was added as application claim 25 on December 11, 2024. EX1002, 764-766. Application claim 27, which depends from application claim 25 and was added at the same time, confirms that the claimed “fifth signals” and “sixth signals” are associated with the “*third* set of C/A signals” and that the claimed “seventh signals” and “eighth signals” are associated with the “*fourth* set of C/A signals.” EX1002, 767.

120. Accordingly, in my opinion, claim 24 contains a clear drafting error, which would have been clearly evident to a POSA, and the correction of which would have been apparent from the claim itself as confirmed by the prosecution history.

IX. THE CLAIMS WOULD NOT HAVE BEEN OBVIOUS

A. Keeth does not disclose or render obvious element 1.j.

121. Keeth does not disclose or render obvious element 1.j, which recites: “wherein a first conduit of the first data conduits is coupled between the first data

interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal.”

122. Dependent claim 18 and independent claims 20 and 23 recite the same element. Accordingly, Samsung’s failure to prove this element is taught demonstrates that claims 1-8, 18, and 20-23 are non-obvious.

123. Figure 4 of the ’087 patent, annotated and reproduced below, provides support for element 1.j. EX1003, ¶¶133, 137 (discussing Figure 4 and describing element 1.j as “a fork-in-the-road configuration”); *see* Pet., 93-94 (same). I note that element 1.j does not require drivers 404a-b and 408a-b of Figure 4.

124. As shown in the annotated figure below, the “first data terminal” (red) exchanges data signals with an external device, such as a memory controller. EX1001, 23:52-55 (“the DRAM package ... is further configured to receive or output data signals via the data terminals”). A control die (light blue) is “coupled between the terminals and the stacked DRAM dies,” which would be above the control die in the annotated figure. EX1001, 24:9-10. The control die includes the “first data conduit” (green) and the “second data conduit” (dark blue). EX1001, 24:10-11 (“the control die including conduits, the conduits including ... data conduits”). The “first data conduit” (green) is coupled between the “first data interconnect” (also green) and the “first data terminal” (red). Similarly, the “second

data conduit” (dark blue) is coupled between the “second data interconnect” (also dark blue) and the “first data terminal” (red).

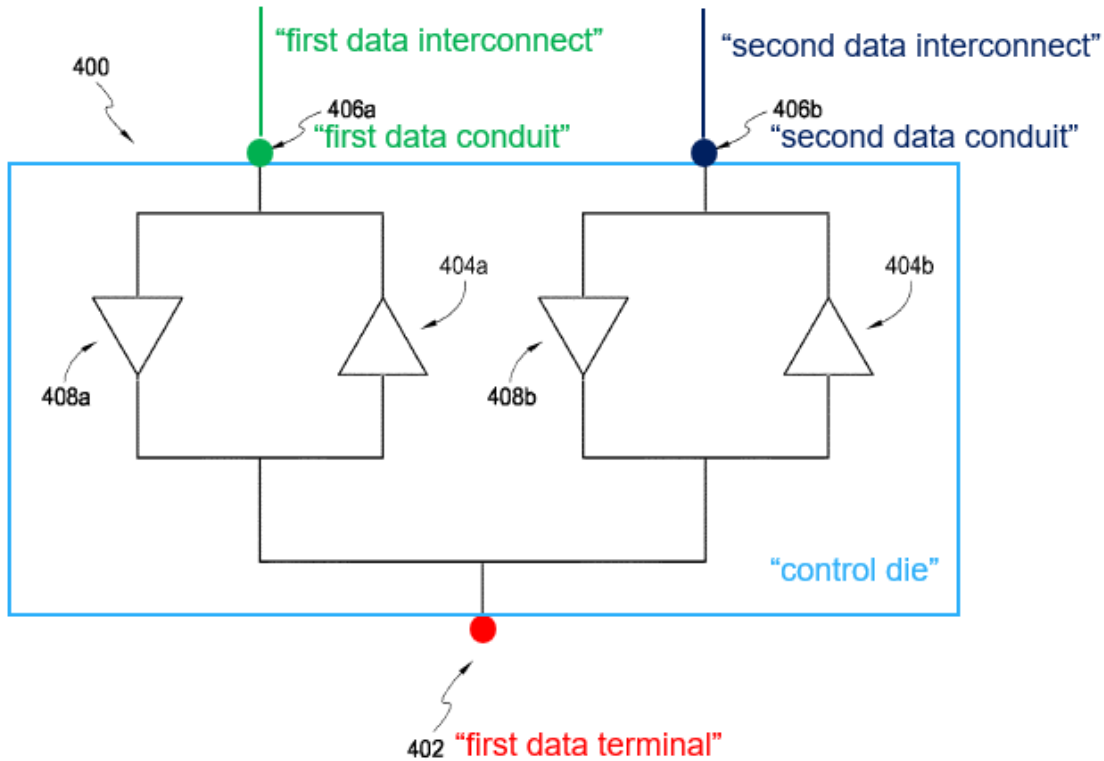


FIG. 4

EX1001, FIG. 4 (annotated).

125. Samsung relies on Keeth to address element 1.j. Pet., 90-92. Samsung maps Keeth’s interface die (e.g., 110 of Figure 1; 510 of Figure 5) to the claimed “control die.” Pet., 75. And Samsung argues Keeth’s vault control circuit on the interface die (e.g., 212 of Figure 2) includes the claimed “data conduits.” Pet., 77; *see also* Pet., 80. I note that Keeth does not actually describe or show data conduits.

126. For element 1.j, Samsung proposes modifying Keeth to couple first and second data conduits to the same input/output data terminal. Pet., 91. According to Samsung, the result would be that Keeth’s “even and odd dies share I/O data pins to improve bandwidth.” *Id.* Samsung alleges that Keeth’s teachings in column 1 of sharing “input/output data pins” and in columns 4 and 5 of concurrently accessing multiple dice would have motivated a POSA to make the modification. *Id.*

127. I disagree for several reasons. First, Samsung’s attempt to link Keeth’s teachings in column 1 with those in columns 4-5 mischaracterizes Keeth. Keeth teaches that (1) the “memory partitions” of the same “vault” may share the vertical conductive paths that connect to the interface die and (2) the odd and even dice are in different vaults. Keeth does not suggest, and a POSA would not have understood, that different vaults share one of the I/O pins that the interface die uses to exchange data with an external device. Second, a POSA would not have made the proposed modification because it would reduce—not improve—the bandwidth of Keeth’s memory package, which is contrary to Keeth’s express teachings.

128. I do not agree with Samsung’s and Dr. Wolfe’s characterization of Keeth’s teachings. Keeth does not suggest that any of the conductive paths that carry data between the dice stack and the interface die are coupled to the same data terminal (or I/O pin) of the interface die that is used to exchange data with an

external device (e.g., memory controller). Samsung's statement that Keeth at 1:65-2:10 teaches "the stacked DRAM dies 'may share ... input/output data pins' on the interface die to improve bandwidth" is incomplete and inaccurate.

129. Keeth teaches that "each memory die in a dice stack may be divided into a plurality of partitions" that are "vertically aligned across multiple dice in the stack" to form a "vault." EX1047, 1:65-2:6. Keeth explains, "The *partitions of a vault may share* address and command control connections (e.g., TSVs) and *input/output data pins* among other connections, and each partition may have a different chip select line to prevent data contention." EX1047, 2:6-10.

130. Keeth depicts this configuration in Figure 2, which shows four dice (220-223) each having four memory partitions (e.g., 204). EX1047, 3:44-54. Figure 2 also shows four vaults (e.g., 206), each having four memory partitions (one from each dice) and a vault control circuit 212 that are vertically stacked. *Id.* The memory partitions in a vault share vertical communicative paths 208 that couple each memory partition of the vault to the vault control circuit (e.g., 212). *Id.* In Figure 2 of Keeth, a POSA would have understood that any data terminal used to exchange data with an external device (e.g., memory controller) would be located at the bottom of interface die 210. *See* EX1047, FIG. 3 (showing interface die 310 and bumps 312). Keeth does not teach or suggest that two of the communicative paths 208 (in the same vault or in other vaults) are coupled to a

share an I/O pin that the interface die 210 uses to exchange data with an external device.

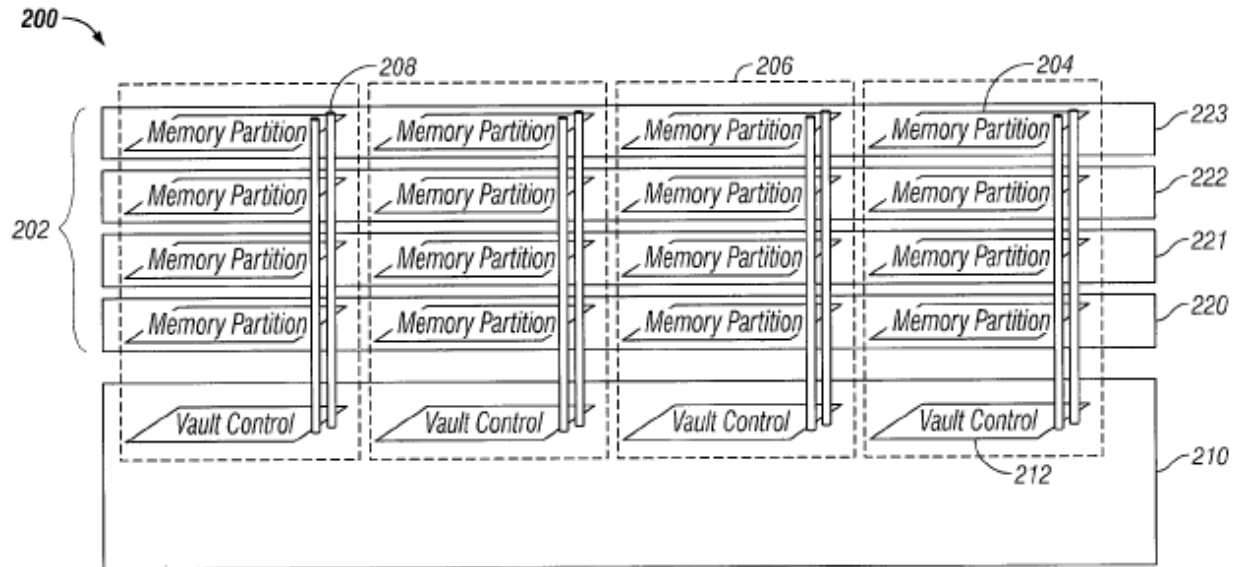


FIG. 2

EX1047, FIG. 2.

131. Samsung’s suggestion that Keeth’s odd and even dice would share I/O pins further mischaracterizes Keeth’s teachings. In Figure 5, Keeth discloses a memory package that incorporates “partition interleaving” of a “dice stack 502 [that] includes four dice 520, 521, 522, and 523.” EX1047, 5:24-30. Keeth explains that the “[a]lternating dice in the stack 502 may be part of *separate* vaults,” for example, the first and third dice are part of a first vault; the second and fourth dice are part of a second vault. EX1047, 6:11-16 (emphasis added).

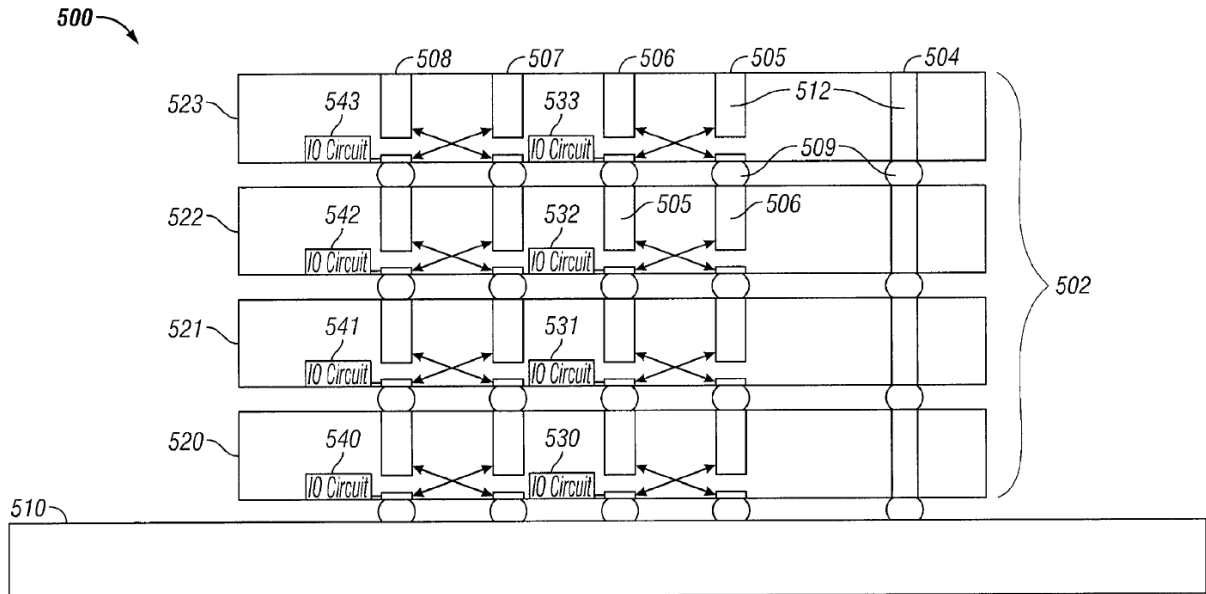


FIG. 5

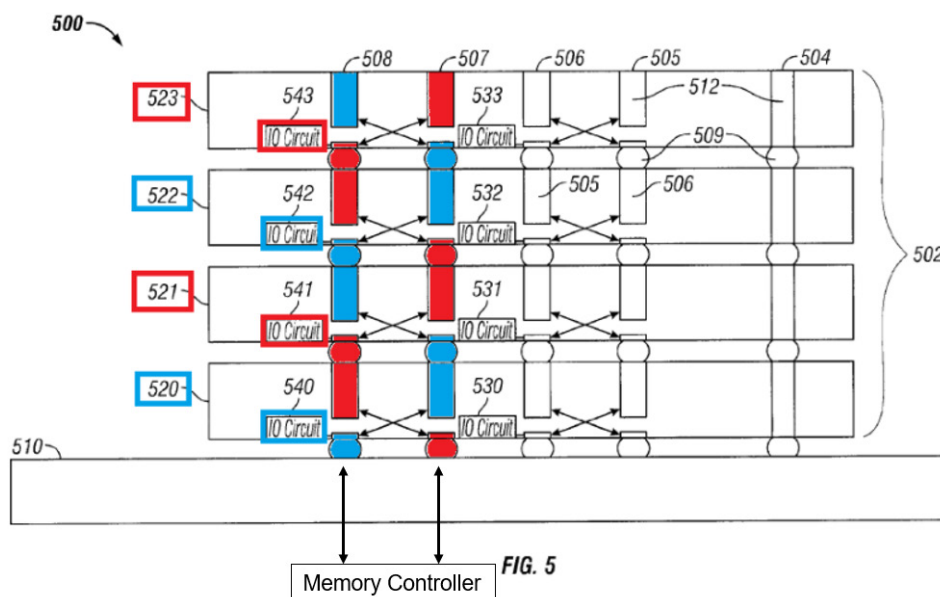
EX1047, FIG. 5.

132. So Keeth's teaching (in column 1) about the memory partitions within the *same vault* sharing communicative paths would not have suggested to a POSA that the even and odd dice in *different vaults* would share one of the I/O pins that the interface die uses to exchange data with an external device. This mischaracterization of Keeth forms the basis of Samsung's and Dr. Wolfe's proposed modification, which is the first reason that this modification fails and a POSA would not have been motivated to make it.

133. Samsung's and Dr. Wolfe's proposed modification also fails because it would reduce—not improve—the bandwidth of Keeth's memory package. Such a reduction in bandwidth is contrary to Keeth's express teachings directed to improving bandwidth, which would have led a POSA away from the proposed

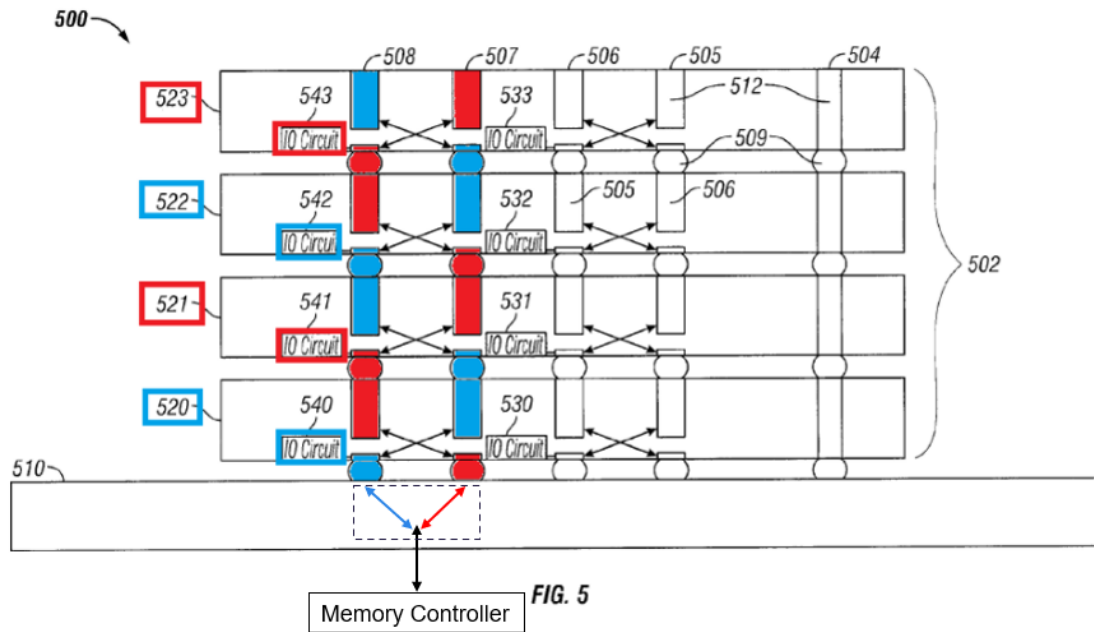
modification.

134. The annotated version of Figure 5 below depicts Keeth's disclosed operation. EX1047, 6:11-29. Keeth's first and third dice 520 and 522 (odd dice, first vault) along with their respective I/O circuits 540 and 542 are shown in blue. Keeth's second and fourth dice 521 and 523 (even dice, second vault) along with their respective I/O circuits 541 and 543 are shown in red. Keeth explains that "this construction allows the interface die 520 to concurrently access the first and second vaults." EX1047, 6:16-19; *see also* EX1047, 5:63-67 ("increasing bandwidth"). For example, interface die 510 can access dice 520 in the first vault and dice 521 in the second vault concurrently, when allows interface die 520 to concurrently provide data from both vaults to an external memory controller via separate I/O pins, increasing the memory package's bandwidth.



EX1047, FIG. 5 (annotated to show Keeth's operation).

135. The second annotated version of Figure 5 of Keeth below shows Samsung's and Dr. Wolfe's proposed modification. As shown in the dotted black box, Samsung proposes coupling conduits of the odd and even dies (e.g., 520 and 521) to the same I/O data pin, which Samsung alleges would "improve bandwidth." Pet., 91. I disagree. The proposed arrangement permits only one of the vaults (odd or even) to use the I/O pin to exchange data with the memory controller, which would create a bottleneck at the I/O pin. I note that Dr. Wolfe opined that the "fork-in-the-road configuration" means "only one read driver and one corresponding chip can be selected to drive read data at a time to the output terminal." EX1003, ¶137; *see also* Pet., 94 (arguing the "'conduits' need to be selectively controlled to prevent data collisions through the '*first data terminal*'"). His opinion supports my position. By coupling the two conduits of odd and even dies to a singular I/O data pin, the resultant bandwidth of the conduits and dies they are connected to would be cut in half. Each pathway of conduit A and conduit B, for example, must now be transmitted over the single I/O pin via this fork-in-the-road configuration. Using such a configuration, coupled with the need to prevent data collisions on the data terminal, would result in significantly reducing by half, if not more, the I/O bandwidth of the memory device as a whole.



EX1047, FIG. 5 (annotated to show Samsung's proposed modification).

136. Samsung's and Dr. Wolfe's proposed modification reduces the bandwidth of Keeth's memory package. Because this result is contrary to Keeth's express teachings, a POSA would not have pursued this modification.

137. Samsung suggests another modification to Keeth: adding "parallel-to-serial and serial-to-parallel converters" to implement "down rate-conversion." Pet., 92. But Samsung provides no explanation how this additional modification would have been implemented in Keeth. And regardless, the proposed modification cuts directly against the spirit of Keeth's invention of high bandwidth concurrent communication. This is because the additional proposed modification would result in the same reduction in bandwidth that is contrary to Keeth's goals, and POSA would not have made this additional modification.

B. The Keeth-Shaeffer combination does not disclose or render obvious elements 1.k.1 and 1.k.2.

138. The combination of Keeth and Shaeffer does not disclose or render obvious elements 1.k.1 and 1.k.2, which recite:

[1.k.1] wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals, [1.k.2] wherein the one or more C/A signals do not include any chip select signal.

139. I note that “the first and second conduits” of element 1.k.1 are the conduits that the patent introduced in element 1.j above. The “one or more C/A signals received via one or more of the C/A terminals” are received from a device that is external to the DRAM package, such as a memory controller. EX1001, 23:52-55 (“the DRAM package is configured to receive C/A signals via the C/A terminals”); EX2060, 60:7-61:15.

140. Dependent claim 18 and independent claims 20 and 23 recite the same element. Accordingly, Samsung’s failure to prove this element is taught demonstrates that claims 1-8, 18, and 20-23 are non-obvious.

141. The combination of Keeth and Shaeffer fails to disclose or renders obvious “one or more C/A signals” that “do not include any chip select signal.” Samsung first argues (i) that Netlist contends that a stack identification (SID) signal is not a “chip select signal” and (ii) because Keeth’s ID information is

allegedly an SID, Keeth's ID information satisfies element 1.k.2. Pet., 94 ("Netlist contends limitation [1.k.2] is satisfied by stack ID (SID) information, EX1089, 70-71, which Keeth also teaches, EX1047, 3:5-8, 3:21-38 ("ID information ... for control circuit ... to reference each die").").

142. I understand that Samsung asserted in the co-pending ITC investigation that "[i]n the context of HBM, SID signals are chip select signals, because they enable TSV drivers to drive data to particular, selected DRAM dies." EX2132, 110 But even if Keeth's ID information is an SID, Keeth does not teach that the ID information is received in "one or more" of the claimed "C/A signals" that are received from a device that is external to the memory package. Keeth's only discussion of the ID information is in 3:5-8 and 3:21-38. *See* Pet., 94 (citing same). In 3:5-8, Keeth merely discloses that the conductive paths of the dice stack may communicate the ID information: "The conductive paths 106 may communicate (e.g., transfer) information Such as data, address, control, ID information, among other information." EX1047, 3:5-8. And in 3:21-38, Keeth explains that "control circuit 130 of interface die 110" may (i) "be configured to assign ID information during initialization of the stack 102" and (ii) "operate to retain the assigned ID information after the initialization of the stack 102, such as in order for control circuit 130 to reference each die 120 through 123 by the ID information" EX1047, 3:26-33. But Keeth does not teach or suggest that the ID

information is received via one more C/A terminals and used to control respective states of first and second data conduits.

143. Keeth discloses that the control circuit 130 that assigns and retains the ID information is part of the interface die 110, as shown in annotated Figure 1 below. EX1047, 3:27. Keeth does not suggest that a C/A terminal on the interface die 110 receives the ID information.

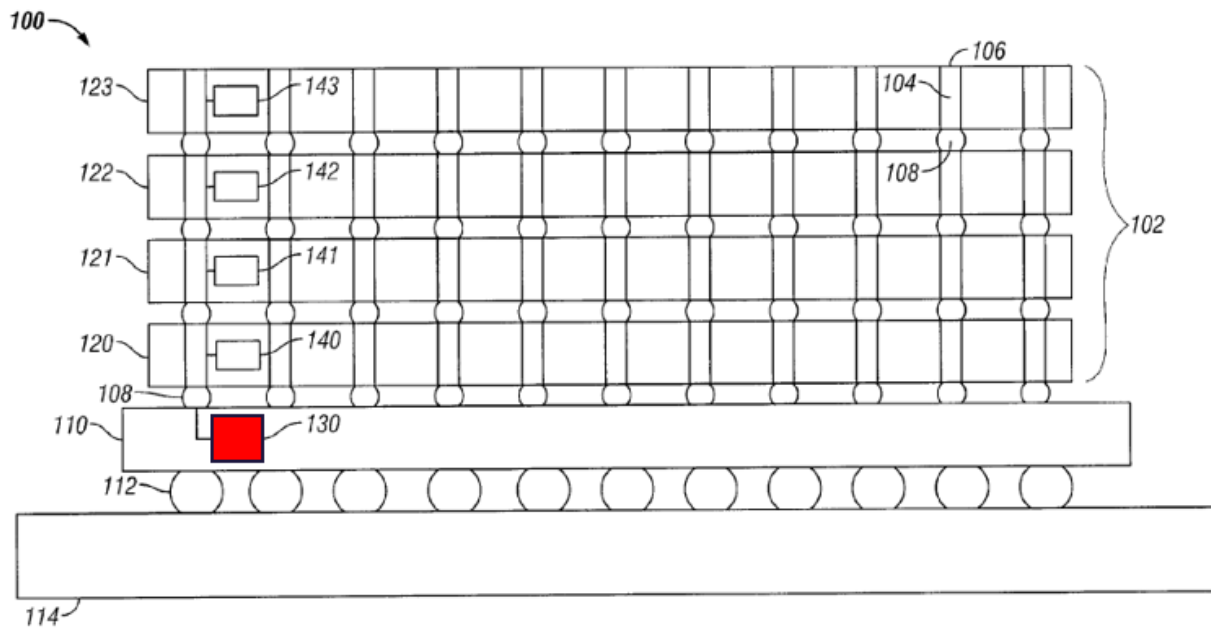


FIG. 1

EX1047, FIG. 1 (annotated).

144. Samsung next argues that implementing Shaeffer’s “timing preamble” or “TRS signal burst” in Keeth’s memory package satisfies element 1.k.2. Pet., 94. But neither the timing preamble or the TRS signal burst describes a C/A signal that DRAM package receives via a C/A terminal from an external device. See EX2060, 60:7-61:15 (testifying that the C/A signal comes from “[s]omething outside of the

claim structure” like a “processor” or “memory controller”).

145. Shaeffer discloses that it uses “the terms ‘timing reference signal (TRS)’, ‘calibration preamble’ and ‘preamble’ ... interchangeably.” EX1048, 3:9-11. And Shaeffer mentions “TRS signal burst” only once to refer to a TRS signal having a certain burst length. EX1048, 10:7-12. Shaeffer teaches that the preamble (or TRS) is transmitted from the memory ranks to the memory controller. *See, e.g.*, EX1048, 2:64-3:1 (the “TRS ... is conveyed from the memory device, to the memory controller” via the same “signaling resource” as the EDC), 4:23-26 (“transmitting a timing reference signal (TRS) from the rank to the memory controller”), 5:60-67, FIG. 1A (showing EDC signal transmitted from memory ranks to memory controller), FIG. 3 (showing preamble sent from memory rank to memory controller ahead of read data).

146. Samsung’s position is that one of Shaeffer’s memory ranks is akin to one of Keeth’s dice, which is not technically accurate. *See Pet.*, 69. But, in any event, applying Samsung’s theory, Shaeffer’s preamble (or TRS) would be transmitted from one of Keeth’s dice to the interface die and then to an external device (e.g., memory controller). Indeed, that is exactly what Samsung proposes to address the claimed “first unidirectional interconnects.” *Pet.*, 95-98 (alleging a POSA would implement Shaeffer’s TRS in Keeth’s interleaved interconnects to send the TRS from the DRAM dies to the control die). This does not satisfy claim

elements 1.k.1 and 1.k.2, which require the C/A signal to be received by the DRAM package from an external device like a memory controller or, as Dr. Wolfe said, “[s]omething outside of the claim structure.” EX2060, 60:7-61:15.

147. Samsung and Dr. Wolfe suggest that Keeth at 2:6-10 suggests C/A signals for write operations that do not include any chip select signal. Their theory is not developed and is not supported by Keeth. Here, Keeth teaches only that “each partition [of a vault] may have a different chip select *line* to prevent data contention.” EX1047, 2:6-10. This teaching does not even mention C/A signals, let alone a C/A signal that does not include a chip select signal, and thus Samsung’s argument fails.

148. I note that the ’087 patent teaches that the control die may determine which DRAM die to select based on an address signal, and then the control die may generate chip select signals. EX1001, 9:61-64. It appears that Samsung’s undeveloped theory is based on the patent’s teachings, which I understand is considered hindsight analysis that is not permitted in evaluating obviousness.

149. Finally, element 1.k.1 requires that the “control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals” Samsung has not shown that any of the signals that they rely on (e.g., Keeth’s ID information, Shaeffer’s preamble) are used by Keeth’s vault control circuit to control the state

of two data conduits (which again Keeth does not show) that are coupled to a data terminal.

C. The Keeth-Shaeffer combination does not disclose or render obvious unidirectional interconnects (elements 1.*l* and 1.*m*).

150. It is my opinion that the Keeth-Shaeffer combination fails to disclose or render obvious the “unidirectional interconnects.” Because all the independent claims recite unidirectional interconnects, Samsung’s failure to prove this element demonstrates that claims 1-23 are non-obvious.

151. Element 1.d.1 introduces “die interconnects” and element 1.d.3 requires that “each of *the* die interconnects includ[es] one or more through silicon vias (TSVs).” EX1001, 23:62-63; 24:3-8; *see* Pet., xvi (claim listing). Elements 1.*l* and 1.*m* further require that “*the* die interconnects” of elements 1.d.1 and 1.d.3 include first and second “unidirectional interconnects,” respectively:

[1.*l*] “wherein *the* die interconnects further include *first unidirectional interconnects* configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies.”

[1.*m*] “wherein *the* die interconnects further include *second unidirectional interconnects* configured to conduct signals from the control die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die.”

152. Samsung and Dr. Wolfe propose modifying Keeth’s “interleaving interconnects” to be unidirectional. Pet., 43, 53, 95-100; EX1003, ¶¶176, 194, 248. Specifically, they argue that “a POSITA would have been motivated to look for advantageous signaling protocols—such as those in Shaeffer—that can be used in Keeth’s memory vaults and *interleaving* connections.” Pet., 43; EX1003, ¶176. They then propose that implementing specific allegedly unidirectional signals or protocols disclosed by Shaeffer in Keeth’s interleaving interconnects satisfies the “unidirectional interconnects” elements. Pet., 97 (referring to analysis at “pp.38-52”), 99 (same). And in suggesting a further modification, they explain that the “conductive paths in the stack of the Keeth-Shaeffer combination” are the “*interleaving* conductive paths.” Pet., 53; EX1003, ¶194.

153. Dr. Wolfe confirmed that Samsung’s theory for the “unidirectional interconnects” requires modifying Keeth’s interleaving interconnects. Addressing the claimed “first unidirectional interconnects,” he opined: “As discussed above, it would have been obvious to a Skilled Artisan *to implement Shaeffer’s signaling protocol*, including its TRS/EDC signaling, *in Keeth’s memory stack using its interleaving die connections* between the interface die and the memory dice, e.g., in order to achieve independent control and increase bandwidth.” EX1003, ¶258.

154. Samsung’s arguments regarding element 1.d.3 further demonstrate that its obviousness theory relies on modifying Keeth’s interleaving interconnects.

Pet., 73-74. Element 1.d.3 requires that “each of the die interconnects” includes one or more TSVs. EX1001, 24:3-8. Samsung alleges that the interleaving interconnects shown in Figures 5-7 of Keeth include the required TSVs. Pet., 73-74. Dr. Wolfe did not address element 1.d.3. *See* EX2060, 27:3-9.

155. In sum, Samsung’s and Dr. Wolfe’s arguments that the Keeth-Shaeffer combination teaches the “unidirectional interconnects” elements relies on modifying Keeth’s interleaving interconnects. But they overlooked that Keeth expressly discloses that its interleaving interconnects are *bidirectional*.

156. Keeth’s interleaving interconnects are bidirectional. Keeth discloses interleaving interconnects in the embodiments shown in Figures 5 and 7. EX1047, 5:24-38, 6:63-7:36, FIGS. 5 (505-508), 7 (705-708). Figure 5 and 7 use double-headed arrows to show that the interleaving interconnects are bidirectional. *Id.* Keeth explains, “The arrows illustrate communicative paths crossing over at each die 520 through 523 that may be implemented using conventional metal and via layers available within the DRAM.” EX1047, 5:54-57. Keeth also discloses that the interleaving interconnects are connected to input/output (I/O) circuits (e.g., 540-543 of Figure 5) for *bidirectional communication*. EX1047, 5:39-62, 7:4-20; *see also* EX1047, 3:21-26 (teaching that non-interleaving interconnects shown in Figure 1 are used to communicate “to and from” dice 120-123, and thus are bidirectional). Keeth also discloses transmitting unidirectional signals using these

bidirectional interconnects. For example, Keeth teaches that the command circuits and/or address circuits of each dice 520 through 523 may be connected to and utilize the interleaving conductive paths 505 through 508 in order to communicate command and/or address signals.” EX1047, 6:4-10. A POSA would have understood that command and address signals Keeth is describing would be sent from the interface die to one or more dice in the stack (not from the dice in the stack to the interface die).

157. I have been advised and understand that patent drawings can be relied on for what they clearly show. Figures 5 and 7 of Keeth clearly show the interleaving interconnects are bidirectional, which Keeth’s textual description (e.g., discussing the I/O circuitry connected to the interconnects) supports and confirms.

158. I note that Samsung and Dr. Wolfe appear to agree. They annotated Figure 5 of Keeth, reproduced below, to show a first conductive path 507 in red and a second conductive path 508 in blue. Pet., 67. As shown by the double-headed arrows in Figure 5 of Keeth and confirmed by Samsung’s own annotations in red and blue, Keeth’s interleaving conductive paths are expressly depicted as bidirectional. EX1047, FIG. 5; Pet., 67.

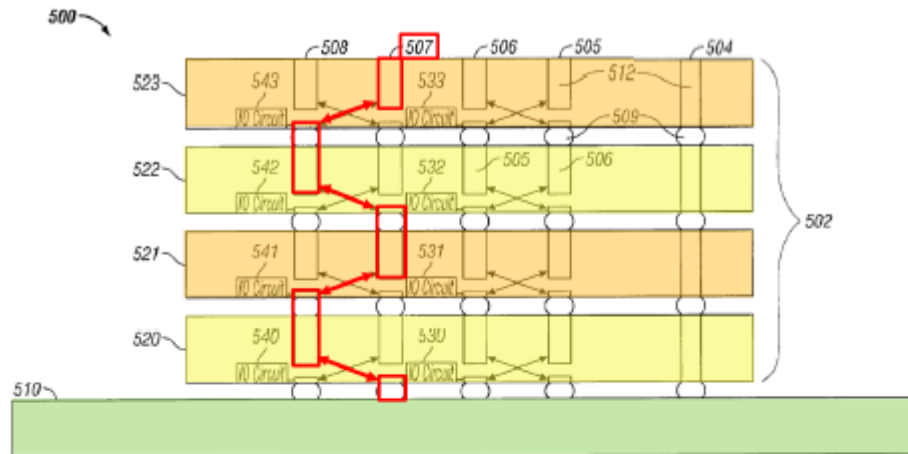


FIG. 5

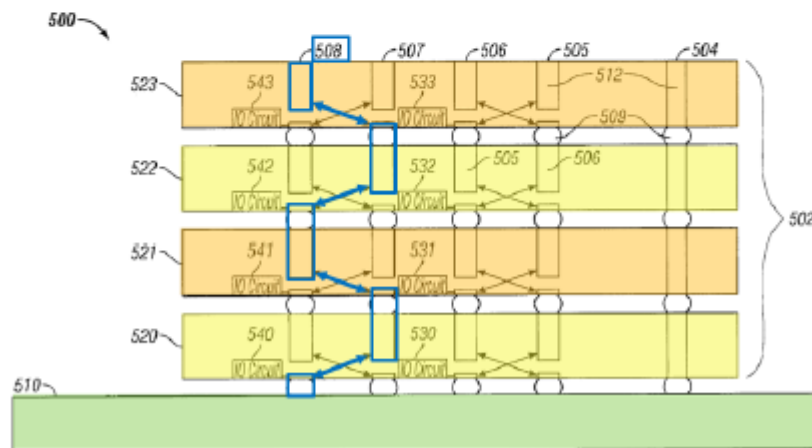


FIG. 5

Pet., 67 (annotating Figure 5 of Keeth, EX1047).

159. Samsung even confirmed in its pre-institution briefing that patent drawings often convey and should be relied on for teaching “simple concept[s].” Paper 11, 14. There, it argued the Office erred during examination by failing to consider Shaeffer because “a unidirectional interconnect is another example of a simple concept easier to find in a figure (e.g., an arrow pointing in one direction) than with keywords.” *Id.* The same is plainly true of Keeth’s arrows pointing in

two directions.

160. Turning to Samsung's and Dr. Wolfe's specific allegations for the "unidirectional interconnects" recited in elements 1.*l* and 1.*m*, they argue that it would have been obvious to implement Shaeffer's interface for transmitting certain signals in Keeth's die interconnects. Pet., 95-100. For element 1.*l*, Samsung alleges that "a POSITA would have implemented Shaeffer's TRS/EDC signaling in Keeth's die interconnects." Pet., 97. And for element 1.*m*, Samsung alleges that a POSITA would have implemented Shaeffer's Data Clock 122 signaling in Keeth's die interconnects. Pet., 99-100.

161. Samsung's arguments thus fail because they fail to account for the fact that Keeth's interleaving interconnects are bidirectional. Additionally, a POSA would not have made Samsung's modification because it is contrary to Keeth's express disclosure. Finally, a POSA would not reasonably expect success in making the modification.

162. Keeth's express disclosures, including that the interleaving interconnects are bidirectional, teach away or at least would have discouraged a POSA from Samsung's proposed modification. Keeth expresses a desire to reduce die size while maintaining or improving bandwidth. EX1047, 2:11-33. Keeth explains that concurrent communication with multiple partitions "requires a greater number of connections and dedicated circuitry at each die and at corresponding

control circuits of the interface die.” EX1047, 2:20-23. Keeth’s solution of bidirectional, interleaving interconnects enables the desired concurrent communication while limiting the number of interconnects and corresponding circuitry, thus reducing die size. EX1047, 2:42-46 (“In many embodiments, interleaving connections (e.g., TSVs) permits a reduction in die size. Alternating connecting conductive paths to I/O logic circuitry along partitions of a vault can reduce dedicated circuitry and die space required for additional circuitry on the die.”), 4:12-16 (“By interleaving the connections, a vault control circuit may concurrently communicate with (e.g., access and send data to) multiple partitions in the vault and thereby improve bandwidth.”).

163. A POSA would have understood that replacing one of Keeth’s bidirectional interconnects would require two unidirectional interconnects (one for each direction) in order to maintain bidirectional communication. This would increase the number of required interconnects and accompanying control circuitry and thus increase die size. Keeth’s teachings of using bidirectional interconnects and reducing die size is contrary to and would have led a POSA away from Samsung’s proposal to modify Keeth’s bidirectional interleaving interconnects into unidirectional interconnects. Notably, neither Samsung nor Dr. Wolfe provides any explanation why a POSA would have modified Keeth’s bi-directional die interconnects to be unidirectional. *See* Pet., 95-100; EX1003, ¶¶245-254.

164. And, as I mentioned, Keeth also discloses transmitting unidirectional signals using these bidirectional interconnects. So even if a POSA modified Keeth to implement Shaeffer's unidirectional signals (e.g., the preamble or a strobe), there is no evidence that a POSA would have sent those signals on unidirectional interconnects. Rather, a POSA would have understood they would be sent on Keeth's bidirectional interconnects.

165. Samsung fails to prove the requisite reasonable expectation of success to modify Keeth's bidirectional interconnects. It provides only a single, cursory sentence to address this requirement: "Lastly, as evidenced by these prior art references, including industry standards, implementing Shaeffer's signaling protocols in the memory stack of Keeth was well within the level of skill at the time and a POSITA would have a reasonable expectation of success in making the combination." Pet., 51-52.

166. Samsung's cursory allegation is insufficient to satisfy its burden, particularly considering Keeth's express teachings about reducing die size while maintaining or improving bandwidth. EX1047, 2:11-33.

X. CONCLUSION

In signing this declaration, I recognize that the declaration will be filed as evidence in a post-grant review before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required, I will appear for cross-examination within the United States during the time allotted.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on this 8th day of June 2026, in Austin, Texas.

A handwritten signature in dark ink, appearing to read "Michael C. Brogioli", is written over a horizontal line.

Michael C. Brogioli, Ph.D.

Declaration of Michael C. Brogioli in Support of Patent Owner's Response – Appendix A

U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
1.a	A dynamic random access memory (DRAM) package, comprising:	2:36-44¹ (“In certain embodiments, an apparatus is provided that comprises a DRAM package operable to communicate with a system memory controller via a command/address bus and a data bus. The DRAM package comprises stacked array 40 dies including at least a first array die and a second array die stacked over at least the first array die, and terminals including control terminals, via which the DRAM package receives command/address signals, and data terminals, via which the DRAM package receives or outputs data signals.”); 4:39-41 (“One example of a memory package that includes array dies and a control die is the Hybrid Memory Cube (HMC).”); 4:50-54 (“The memory package 200 can include any type of memory package. For example, the memory package 200 may be a DRAM package, a SDRAM package, a flash memory package, or a DDR SDRAM package (e.g., DDR3, DDR4), to name a few.”); <i>Also</i>, 3:46-48, 17:65-18:12, 18:20-57, 19:4-21 (3DS DIMM).	3:17-21² 3:28-31³ 4:57-59 5:1-5 3:65-67, 18:15-30, 18:38-19:7, 19:21-41.

¹ For convenience, citations are to the as-published '087 patent specification. The same disclosure is included in the as-filed application.

² Similar disclosure: (“In certain embodiments, an apparatus is provided that comprises a register device configured to receive command/address signals from a memory control hub and to generate data path control signals. The apparatus further comprises a plurality of DRAM packages.”)

³ Similar disclosure: (“Further, each of the DRAM packages comprises a plurality of DDR DRAM dies operatively coupled to the control die to receive the data signals from the control die.”)

Declaration of Michael C. Brogioli in Support of Patent Owner's Response – Appendix A

U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
1.b.1	stacked DRAM dies including at least a first plurality of DRAM dies and a second plurality of DRAM dies,	Fig. 2 (DRAM dies 210a-b and DRAM dies 210c-d); Fig. 3 (DRAM dies 310a-b and DRAM dies 310c-d); 4:50-54 (“The memory package 200 can include any type of memory package. For example, the memory package 200 may be a DRAM package, a SDRAM package, a flash memory package, or a DDR SDRAM package (e.g., DDR3, DDR4), to name a few.”); 4:62-63 (“The memory package 200 may include a plurality of array dies 210 (e.g., array dies 210a-210d).”); 5:7-9 (“As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (3DS).”); 5:41-47 (“In certain embodiments, at least one of the die interconnects 220 is in electrical communication with at least one data port from each of at least two array dies 210 without being in electrical communication with a data port from at least one array die 210, which may be in electrical communication with a different die interconnect 220.”); 5:48-60 (“For example, die interconnect 220a may be in electrical communication with a data port from array die 210a and a data port from array die 210b (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c or any data ports from array die 210d. The data ports of array dies 210a and 210b in electrical communication with the die interconnect 220a can be corresponding to the same data bit (e.g., D0). Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, . . .) of array dies 210a and 210b. These other die interconnects	Fig. 2; Fig. 3; 5:1-5; 5:12-13 5:23-26 5:57-62 5:64-6:8

Declaration of Michael C. Brogioli in Support of Patent Owner's Response – Appendix A

U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		can be electrically isolated from the corresponding data ports of array dies 210c and 210d.”); 5:61-6:21 (“However, continuing this example, the die interconnect 220b may be in electrical communication with a data port from array die 210c and a data port from array die 210d (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., D0) without being in electrical communication with any data ports from array die 210a and array die 210b. Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, . . .) of array dies 210c and 210d. Despite not being in electrical communication with any data ports from array die 210a and 210b, in some implementations, the die interconnect 220b may pass through the array dies 210a and 210b (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b. For some implementations, each of the array dies 210 may be in electrical communication with corresponding die interconnects 220, without any of the die interconnects 220 being in electrical communication with all of the array dies 210. Where existing systems may utilize a single die interconnect to be in electrical communication with the corresponding data ports of each array die (e.g., the data ports corresponding to the same bit), certain embodiments described herein utilize multiple die interconnects to provide electrical communication to the corresponding data ports of the array dies (e.g., the data ports corresponding to the same data bit) with none of the multiple die interconnects in electrical communication with data ports of all the array dies.”);	6:9-35

Declaration of Michael C. Brogioli in Support of Patent Owner's Response – Appendix A

U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		9:65-10:3 (“FIG. 3 schematically illustrates another example embodiment of a memory package 300 in accordance with the present disclosure. In certain embodiments, some or all of the embodiments described above with respect to the memory package 200 may be applicable to the memory package 300.”); 10:10-26 (“The memory package 300 may include a plurality of array dies 310 (e.g., array dies 310a-310h). In the implementation illustrated in FIG.3, the memory package includes eight array dies. However, as stated earlier, the memory package 300 may include more or fewer array dies. Each of the array dies 310 may include one or more ports (not shown) that enable electrical communication between the circuitry of the array dies 310 and one or more die interconnects 320. Each of these die interconnects 320 may be coupled to, or in electrical communication with at least one port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical communication with a port from at least one array die 310, which may be in electrical communication with a different die interconnect 320.”); <i>see also e.g., 2:36-3:20, 15:40-41, 15:52-61, 16:13-25.</i>	10:7-11 10:18-34 2:19-3:40, 15:57-67, 16:1-10, 16:29-41
1.b.2	each DRAM die of the stacked DRAM dies including C/A ports, data ports and DRAM memory cells, wherein	Figs. 2-3; 5:2-7 (“Each of the array dies 210a-210d may include circuitry (e.g., memory cells) (not shown) for storing data. Examples of array dies compatible with	Figs. 2-3 5:19-23

Declaration of Michael C. Brogioli in Support of Patent Owner's Response – Appendix A

U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;	certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above).”); 5:25-29 (“Each of the array dies 210 may include one or more data ports (not shown). The data ports enable electrical communication and data transfer between the corresponding memory circuitry of the array dies 210 and a communication pathway (e.g., a die interconnect).”); 5:32-35 (“For example, certain versions of HMC have been reported to have 512 data ports per die, with the corresponding bits of each die all connected to a single die interconnect (e.g., TSV).”); 9:18-21 (“In some embodiments, the control die 230 may include additional command/address conduits 240 and die interconnects 242, which may be in electrical communication with at least one port of each of the array dies 210.”); 9:25-36 (“These signals may be command signals, address signals, or may serve as both command and address signals (e.g., may include a memory cell address and a write command or a read command) either simultaneously or based on a determining criterion, such as the edge of a clock signal. The command die 230 may include a command/address conduit 240 and corresponding die interconnect 242 for each bit of the command/address signals that the memory package 200 is configured to support. The number of bits of the command/address signals may be the same or may be different from the number of data bits of the memory package 200.”); 10:14-17 (“Each of the array dies 310 may include one or more ports (not shown) that enable electrical communication between the circuitry of the array dies 310 and one or more die interconnects 320.”);	5:41-45 5:48-51 9:28-31 9:33-45 10:22-25

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		10:48-59 (“In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground Voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits configured to provide a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal to one or more die interconnects. Consequently, in some embodiments, the drivers 334 may be configured to drive signals other than data signals.”); <i>see also e.g.</i>, 2:3-6 (“The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects.”); 4:50-54 (“The memory package 200 can include any type of memory package. For example, the memory package 200 may be a DRAM package, a SDRAM package, a flash memory package, or a DDR SDRAM package (e.g., DDR3, DDR4), to name a few.”).	10:56-67 1:53-56 5:1-5
1.c.1	terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals	Figs. 2-3 4:56-61 (“Further, the memory package 200 may include input/output terminals (not shown) that are configured to be placed in electrical communication with circuitry of the memory module to transmit signals between the memory package 200 and a Memory Control Hub (MCH) (not shown).”);	Figs. 2-3 5:7-10

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals,	4:65-67 (“Further, circuitry of the array dies 210 may be in electrical communication with the input/output terminals of the memory package 200.”); 6:22-47 (“In addition to the plurality of array dies 210, the memory package 200 includes a control die 230, . . . The control die 230 may include a number of data conduits 232, which includes data conduits 232a and 232b. Each of these data conduits 232 may be configured to transmit a data signal to a single die interconnect 220. For example, the data conduit 232a may be configured to transmit a data signal to the die interconnect 220a without transmitting the data signal to the die interconnect 220b. Conversely, the data conduit 232b may be configured to transmit the data signal to the die interconnect 220b without transmitting the data signal to the die interconnect 220a (e.g., data conduit 232b is electrically isolated from die interconnect 220a and data conduit 232a is electrically isolated from die interconnect 220b).”); 6:35-47 (“The control die 230 may include a number of data conduits 232, which includes data conduits 232a and 232b. Each of these data conduits 232 may be configured to transmit a data signal to a single die interconnect 220. For example, the data conduit 232a may be configured to transmit a data signal to the die interconnect 220a without transmitting the data signal to the die interconnect 220b. Conversely, the data conduit 232b may be configured to transmit the data signal to the die interconnect 220b without transmitting the data signal to the die interconnect 220a (e.g., data conduit 232b is electrically isolated from die interconnect 220a and data conduit 232a is electrically isolated from die interconnect 220b).”); 6:56-63 (“Each of the data conduits 232 may be configured to receive the data signal from a common source. For instance, the data conduit 232a and the data	5:15-17 6:36-59 6:48-59 7:1-8

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		conduit 232b may each receive a substantially similar, if not identical, data signal from the same signal source (e.g. the data signal corresponding to the same data bit). The source of the data signal may include a data path, a driver, a latch, a pin, or any other construct that may provide a data signal to a data conduit.”); 9:18-21 (“In some embodiments, the control die 230 may include additional command/address conduits 240 and die interconnects 242, which may be in electrical communication with at least one port of each of the array dies 210.”); 9:56-59 (“For example, a register (not shown) that is part of a memory module that includes the memory package 200 may determine the chip select signals and drive the chip select signals to the array dies 210.”); 9:61-64 (“In some embodiments, the control die 230 may determine the array die 210 to select based on, for example, an address signal. In such embodiments, the control die may generate the chip select signals.”); 10:27-32 (“In addition to the plurality of array dies 310, the memory package 300 includes a control die 330. In some embodiments, the control die 330 may include a number of conduits 332 (e.g., conduits 332a-332f). Each of these conduits 332 may be configured to transmit a signal to a single die interconnect 320.”); 10:48-50 (“In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few.”);	9:28-31 9:64-10:1 10:2-6 10:35-40 10:56-58

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		15:8-10 (“FIG. 4 illustrates an example embodiment of a driver structure 400 of a control die (e.g. control die 230) in accordance with the present disclosure.”); 15:67-16:4 (“The drivers 408a and 408b can each be configured to drive a signal received from a respective data conduit 406a and 406b to the input/output port 402 and to another component that may be in electrical communication with the input/output port 402, such as a MCH.”); 21:4-7 (“Further, the register device 812 may generate data path control signals, which can be provided to a control die 822, or isolation device, of a memory package 820 via one or more data path control lines 816.”); 21:63-22:5 (“In some embodiments, the memory module 810 is selectively configurable into two operational modes. In the first operational mode, the register device 812 generates data path control signals provided to the control dies 822 via the data path control lines 816. The control dies 822 may decode command/address signals included with the data path control signals generated by the register device 812. In some implementations, the control dies 822 use the data path control signals to operate the data path control circuits of the control dies 822.”).	15:26-27 16:16-20 21:21-24 22:12-21
1.c.2	wherein the DRAM package is configured to output first data signals in response to a first set of C/A signals associated with a	Figs. 2-3; 2:3-5 (“The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects.”);	Figs. 2-3 1:53-56

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	memory read operation and to receive second data signals in response to a second set of C/A signals associated with a memory write operation;	8:54-9:3 (“The memory package 200 may generally include as many additional data conduits and corresponding die interconnects as the number of bits the memory package 200 is designed or configured to support per memory address. Thus, if for example, the memory package 200 is configured to be a 16-bit memory, the memory package 200 may include 16 pairs of data conduits 232 and 16 pairs of corresponding die interconnects 220. Similarly, if the memory package 200 is configured as a 32- or 64-bit memory, the memory package 200 may include 32 or 64 pairs of data conduits 232 and 32 or 64 pairs of corresponding die interconnects 220. Generally, the data conduits and die interconnects for each bit are configured identically. Thus, for the memory package 200, each data conduit is configured to be in electrical communication with a die interconnect that is configured to be in electrical communication with a pair of the array dies 210.”); 9:6-14 (“In certain embodiments, the same die interconnects and the same corresponding data conduits may be used to transfer data both to and from the array dies 210. In such embodiments, the die interconnects may be bi-directional. In alternative embodiments, separate die interconnects and corresponding data conduits may be used to transfer data to the array dies 210 and data from the array dies 210 to the control die 230.”); 9:25-30 (“These signals may be command signals, address signals, or may serve as both command and address signals (e.g., may include a memory cell address and a write command or a read command) either simultaneously or based on a determining criterion, such as the edge of a clock signal.”); 15:35-37 (“This control signal, in some cases, may correspond to one or more of a command/address signal (e.g., read/write) and a chip select signal.”);	8:65-9:14 9:17-24 9:35-39 15:51-54

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		15:62-16:4 (“Similar to the input/output port 402, the conduits 406a and 406b can be configured to receive a signal from the die interconnects that are in electrical communication with the conduits 406a and 406b. In turn, the signal received at one of the conduits 406a and 406b can be provided to drivers 408a and 408b respectively. The drivers 408a and 408b can each be configured to drive a signal received from a respective data conduit 406a and 406b to the input/output port 402 and to another component that may be in electrical communication with the input/output port 402, such as a MCH.”); 19:4-21 (“In contrast to the JEDEC DDR3 RDIMM standard, the 3DS-DIMM proposal requires the DRAM package 720 to include the controller die 722 that controls all data paths timing and operations. This arrangement of the DRAM package reduces the load on the data bus, however, it presents three significant shortcomings: 1) The command/address buffer in the 3DS DRAM package introduces clock cycle latency since it needs to provide clock synchronous operation to the DRAM dies in the package; 2) The data path control circuit (e.g., ODT, read/write data direction) in the control die becomes very complicated to support semi-synchronous (fly-by) data path control among all 3DS DRAM packages that are on a DIMM; and 3) The variations in the DRAM die timing characteristics within each 3DS DRAM package would be likely to require resynchronization of the data signals during the read/write operations, which increases the read/write latency and the read-to-write and write-to-read turn around time.”)	16:11-20 19:21-40

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
1.d.1	die interconnects including C/A interconnects and data interconnects, the C/A interconnects including at least first C/A interconnects and second C/A interconnects, the first C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,	Figs. 2-3; 5:30-6:21 (“In the example schematically illustrated in FIG. 2, the memory package 200 includes a plurality of die interconnects 220 (e.g., die interconnects 220a, 220b). For example, certain versions of HMC have been reported to have 512 data ports per die, with the corresponding bits of each die all connected to a single die interconnect (e.g., TSV). . . . Each of these die interconnects 220 may be coupled to, or in electrical communication with at least one data port of at least one of the array dies 210. In certain embodiments, at least one of the die interconnects 220 is in electrical communication with at least one data port from each of at least two array dies 210 without being in electrical communication with a data port from at least one array die 210, which may be in electrical communication with a different die interconnect 220. [¶] For example, die interconnect 220a may be in electrical communication with a data port from array die 210a and a data port from array die 210b (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c or any data ports from array die 210d. The data ports of array dies 210a and 210b in electrical communication with the die interconnect 220a can be corresponding to the same data bit (e.g., D0). Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, . . .) of array dies 210a and 210b. These other die interconnects can be electrically isolated from the corresponding data ports of array dies 210c and 210d. However, continuing this example, the die interconnect 220b may be in electrical communication with a data port from array die 210c and a data port from array die 210d (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., D0) without being in electrical communication with any data ports from array die 210a and	Figs. 2-3 5:46-6:35

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		array die 210b. Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, . . .) of array dies 210c and 210d. Despite not being in electrical communication with any data ports from array die 210a and 210b, in some implementations, the die interconnect 220b may pass through the array dies 210a and 210b (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b. For some implementations, each of the array dies 210 may be in electrical communication with corresponding die interconnects 220, without any of the die interconnects 220 being in electrical communication with all of the array dies 210. Where existing systems may utilize a single die interconnect to be in electrical communication with the corresponding data ports of each array die (e.g., the data ports corresponding to the same bit), certain embodiments described herein utilize multiple die interconnects to provide electrical communication to the corresponding data ports of the array dies (e.g., the data ports corresponding to the same data bit) with none of the multiple die interconnects in electrical communication with data ports of all the array dies.”); 6:35-47 (“The control die 230 may include a number of data conduits 232, which includes data conduits 232a and 232b. Each of these data conduits 232 may be configured to transmit a data signal to a single die interconnect 220. For example, the data conduit 232a may be configured to transmit a data signal to the die interconnect 220a without transmitting the data signal to the die interconnect 220b. Conversely, the data conduit 232b may be configured to transmit the data signal to the die interconnect 220b without transmitting the data signal to the die interconnect 220a (e.g., data conduit 232b is electrically	6:48-59

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		isolated from die interconnect 220a and data conduit 232a is electrically isolated from die interconnect 220b).”); 8:23-51 (“In addition, the die interconnects 220 may use via holes to pass through an array die that is not configured to be in electrical communication with the die interconnect. For instance, die interconnect 220b may pass through array dies 210a and 210b using TSVs that do not enable electrical communication between the die interconnect 220b and data ports of the array dies 210a and 210b (illustrated by the unfilled circles). In this way, the array dies 210a, 210b are not responsive to the data signal beings transmitted by the die interconnect 220b. However, the die interconnect 220b may be connected with at least one data port of each of the array dies 210c and 210d using a via (illustrated by the filled or darkened circles). In cases where the die interconnect passes through an array die that is not configured to be in electrical communication with the die interconnect, the TSV may include an insulator or an air gap between the die interconnect and the array die circuitry that is large enough to prevent electrical communication between the die interconnect and the array die circuitry. In certain embodiments, the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same. However, in such cases, electrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be stubs. These stubs are not configured to provide electrical communication with the memory cells of the array die.”);	8:35-62

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		9:18-36 (“In some embodiments, the control die 230 may include additional command/address conduits 240 and die interconnects 242, which may be in electrical communication with at least one port of each of the array dies 210. For simplicity, FIG. 2 shows only a single such conduit 240 and die interconnect 242. The command/address conduits 240 are configured to provide corresponding signals to the die interconnects 242. These signals may be command signals, address signals, or may serve as both command and address signals (e.g., may include a memory cell address and a write command or a read command) either simultaneously or based on a determining criterion, such as the edge of a clock signal. The command die 230 may include a command/address conduit 240 and corresponding die interconnect 242 for each bit of the command/ address signals that the memory package 200 is configured to support. The number of bits of the command/address signals may be the same or may be different from the number of data bits of the memory package 200.”); 10:10-26 (“The memory package 300 may include a plurality of array dies 310 (e.g., array dies 310a-310h). In the implementation illustrated in FIG.3, the memory package includes eight array dies. However, as stated earlier, the memory package 300 may include more or fewer array dies. Each of the array dies 310 may include one or more ports (not shown) that enable electrical communication between the circuitry of the array dies 310 and one or more die interconnects 320. Each of these die interconnects 320 may be coupled to, or in electrical communication with at least one port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical	9:28-45 10:18-34

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		communication with a port from at least one array die 310, which may be in electrical communication with a different die interconnect 320.”); 10:27-32 (“In addition to the plurality of array dies 310, the memory package 300 includes a control die 330. In some embodiments, the control die 330 may include a number of conduits 332 (e.g., conduits 332a-332f). Each of these conduits 332 may be configured to transmit a signal to a single die interconnect 320.”); 10:48-59 (“In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits configured to provide a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal to one or more die interconnects. Consequently, in some embodiments, the drivers 334 may be configured to drive signals other than data signals.”); See also citations for elements 1.b.1.-1.b.2.	10:35-40 10:56-67
1.d.2	the data interconnects including at least first data interconnects and second data interconnects, the first data interconnects	See citations for 1.d.1	

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	configured to conduct the first data signals and the second data signals,		
1.d.3	each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies and configured to conduct signals to and/or from the one or more DRAM dies in the stacked DRAM dies through the one or more TSVs;	Figs. 2-3; 5:32-38 (“For example, certain versions of HMC have been reported to have 512 data ports per die, with the corresponding bits of each die all connected to a single die interconnect (e.g., TSV). Examples of die interconnects include, but are not limited to, through-silicon vias (TSV), conducting rods, wire bonds, and pins. (See e.g., U.S. Pat. Nos. 7,633,165 and 7,683,459.)”); 8:15-22 (“Moreover, the die interconnects 220 may use vias, or through-silicon vias (TSVs) to couple with or to electrically communicate with an array die. For instance, die interconnect 220a may be connected with data ports of the array dies 210a and 210b using vias (illustrated by the filled or darkened circles). Examples of TSVs which may be used with the present disclosure are described further in U.S. Pat. Nos. 7,633,165 and 7,683,459.”); 8:25-51 (“For instance, die interconnect 220b may pass through array dies 210a and 210b using TSVs that do not enable electrical communication between the die interconnect 220b and data ports of the array dies 210a and 210b (illustrated by the unfilled circles). In this way, the array dies 210a, 210b are not responsive to the data signal beings transmitted by the die interconnect 220b. However, the die interconnect 220b may be connected with at least one data port of each of the array dies 210c and 210d using a via (illustrated by the filled or darkened circles). In cases where the die interconnect passes through an array die that is not configured to be in electrical communication with the die interconnect, the	Figs. 2-3 5:48-54 8:27-34 8:37-62

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		TSV may include an insulator or an air gap between the die interconnect and the array die circuitry that is large enough to prevent electrical communication between the die interconnect and the array die circuitry. In certain embodiments, the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same. However, in such cases, electrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be stubs. These stubs are not configured to provide electrical communication with the memory cells of the array die.”); 9:67-10:3 (“In certain embodiments, some or all of the embodiments described above with respect to the memory package 200 may be applicable to the memory package 300.”).	10:9-11

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1.e.1	a control die coupled between the terminals and the stacked DRAM dies,	Figs. 2-3; 6:22-47 (“In addition to the plurality of array dies 210, the memory package 200 includes a control die 230, . . . The control die 230 may include a number of data conduits 232, which includes data conduits 232a and 232b. Each of these data conduits 232 may be configured to transmit a data signal to a single die interconnect 220. For example, the data conduit 232a may be configured to transmit a data signal to the die interconnect 220a without transmitting the data signal to the die interconnect 220b. Conversely, the data conduit 232b may be configured to transmit the data signal to the die interconnect 220b without transmitting the data signal to the die interconnect 220a (e.g., data conduit 232b is electrically isolated from die interconnect 220a and data conduit 232a is electrically isolated from die interconnect 220b).”); 6:56-63 (“The control die 230 may include a number of data conduits 232, which includes data conduits 232a and 232b. Each of these data conduits 232 may be configured to transmit a data signal to a single die interconnect 220. For example, the data conduit 232a may be configured to transmit a data signal to the die interconnect 220a without transmitting the data signal to the die interconnect 220b. Conversely, the data conduit 232b may be configured to transmit the data signal to the die interconnect 220b without transmitting the data signal to the die interconnect 220a (e.g., data conduit 232b is electrically isolated from die interconnect 220a and data conduit 232a is electrically isolated from die interconnect 220b); 9:18-21 (“In some embodiments, the control die 230 may include additional command/address conduits 240 and die interconnects 242, which may be in electrical communication with at least one port of each of the array dies 210.”);	Figs. 2-3 6:36-59 7:1-8 9:28-31
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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		9:56-59 (“For example, a register (not shown) that is part of a memory module that includes the memory package 200 may determine the chip select signals and drive the chip select signals to the array dies 210.”); 9:61-63 (“In some embodiments, the control die 230 may determine the array die 210 to select based on, for example, an address signal.”); 10:27-32 (“In addition to the plurality of array dies 310, the memory package 300 includes a control die 330. In some embodiments, the control die 330 may include a number of conduits 332 (e.g., conduits 332a-332f). Each of these conduits 332 may be configured to transmit a signal to a single die inter connect 320.”); 10:48-50 (“In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few.”); 15:8-10 (“FIG. 4 illustrates an example embodiment of a driver structure 400 of a control die (e.g. control die 230) in accordance with the present disclosure.”); 15:67-16:4 (“The drivers 408a and 408b can each be configured to drive a signal received from a respective data conduit 406a and 406b to the input/output port 402 and to another component that may be in electrical communication with the input/output port 402, such as a MCH.”); See also citations for element 1.c.1.	9:65-10:1 10:2-4 10:35-40 10:56-58 15:26-27 16:16-20

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1.e.2	the control die including conduits, the conduits including C/A conduits and data conduits,	Figs. 2-3; 5:30-6:21 (“In the example schematically illustrated in FIG. 2, the memory package 200 includes a plurality of die interconnects 220 (e.g., die interconnects 220a, 220b). For example, certain versions of HMC have been reported to have 512 data ports per die, with the corresponding bits of each die all connected to a single die interconnect (e.g., TSV). . . . Each of these die interconnects 220 may be coupled to, or in electrical communication with at least one data port of at least one of the array dies 210. In certain embodiments, at least one of the die interconnects 220 is in electrical communication with at least one data port from each of at least two array dies 210 without being in electrical communication with a data port from at least one array die 210, which may be in electrical communication with a different die interconnect 220. For example, die interconnect 220a may be in electrical communication with a data port from array die 210a and a data port from array die 210b (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c or any data ports from array die 210d. The data ports of array dies 210a and 210b in electrical communication with the die interconnect 220a can be corresponding to the same data bit (e.g., D0). Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, . . .) of array dies 210a and 210b. These other die interconnects can be electrically isolated from the corresponding data ports of array dies 210c and 210d. [¶] However, continuing this example, the die interconnect 220b may be in electrical communication with a data port from array die 210c and a data port from array die 210d (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., D0) without being in electrical communication with any data ports from array die 210a and array die 210b. Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1,	Figs. 2-3 5:46-6:35
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	D2, . . .) of array dies 210c and 210d. Despite not being in electrical communication with any data ports from array die 210a and 210b, in some implementations, the die interconnect 220b may pass through the array dies 210a and 210b (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b. For some implementations, each of the array dies 210 may be in electrical communication with corresponding die interconnects 220, without any of the die interconnects 220 being in electrical communication with all of the array dies 210. Where existing systems may utilize a single die interconnect to be in electrical communication with the corresponding data ports of each array die (e.g., the data ports corresponding to the same bit), certain embodiments described herein utilize multiple die interconnects to provide electrical communication to the corresponding data ports of the array dies (e.g., the data ports corresponding to the same data bit) with none of the multiple die interconnects in electrical communication with data ports of all the array dies.”); 6:35-47 (“The control die 230 may include a number of data conduits 232, which includes data conduits 232a and 232b. Each of these data conduits 232 may be configured to transmit a data signal to a single die interconnect 220. For example, the data conduit 232a may be configured to transmit a data signal to the die interconnect 220a without transmitting the data signal to the die interconnect 220b. Conversely, the data conduit 232b may be configured to transmit the data signal to the die interconnect 220b without transmitting the data signal to the die interconnect 220a (e.g., data conduit 232b is electrically isolated from die interconnect 220a and data conduit 232a is electrically isolated from die interconnect 220b).”); 8:54-9:6 (“The memory package 200 may generally include as many additional data conduits and corresponding die interconnects as the number of bits the	6:48-59 8:65-9:16
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	memory package 200 is designed or configured to support per memory address. Thus, if for example, the memory package 200 is configured to be a 16-bit memory, the memory package 200 may include 16 pairs of data conduits 232 and 16 pairs of corresponding die interconnects 220. Similarly, if the memory package 200 is configured as a 32- or 64-bit memory, the memory package 200 may include 32 or 64 pairs of data conduits 232 and 32 or 64 pairs of corresponding die interconnects 220. Generally, the data conduits and die interconnects for each bit are configured identically. Thus, for the memory package 200, each data conduit is configured to be in electrical communication with a die interconnect that is configured to be in electrical communication with a pair of the array dies 210. However, it is possible that, in some embodiments, the data conduits and die interconnects of different bits may be configured differently.”); 9:18-36 (“In some embodiments, the control die 230 may include additional command/address conduits 240 and die interconnects 242, which may be in electrical communication with at least one port of each of the array dies 210. For simplicity, FIG. 2 shows only a single such conduit 240 and die interconnect 242. The command/address conduits 240 are configured to provide corresponding signals to the die interconnects 242. These signals may be command signals, address signals, or may serve as both command and address signals (e.g., may include a memory cell address and a write command or a read command) either simultaneously or based on a determining criterion, such as the edge of a clock signal. The command die 230 may include a command/address conduit 240 and corresponding die interconnect 242 for each bit of the command/ address signals that the memory package 200 is configured to support. The number of bits of the command/address signals may be the same or may be different from the number of data bits of the memory package 200.”);	9:28-45
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	10:28-32 (“In addition to the plurality of array dies 310, the memory package 300 includes a control die 330. In some embodiments, the control die 330 may include a number of conduits 332 (e.g., conduits 332a-332f). Each of these conduits 332 may be configured to transmit a signal to a single die interconnect 320.”); 10:33-47 (“Further, implementations of the conduits 332 may include one or more drivers 334 (e.g., drivers 334a-334f). Each of the drivers 334 may be configured to drive a signal along a corresponding die interconnect 320. For instance, the driver 334a of the conduit 332a may be configured to drive a signal along the die interconnect 320a to one or more of the array dies 310a and 310b. As a second example, the driver 334b of the conduit 332b may be configured to drive a signal along the die interconnect 320b to one or more of the array dies 310c and 310d. Although the die interconnect 320b may pass through the array dies 310a and 310b, because the die inter connect 320b, in the example illustrated in FIG. 3, is not configured to be in electrical communication with the array dies 310a and 310b, the driver 334b does not drive the signal to the array dies 310a and 310b.”); 10:48-59 “In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits configured to provide a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal to one or more die interconnects. Consequently, in some embodiments, the drivers 334 may be configured to drive signals other than data signals”; See also citations for elements 1.c.1., 1.d.1-1.d.3.	10:35-40 10:41-55 10:56-67
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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
1.e.3	the C/A conduits including at least first C/A conduits coupled to respective ones of the first C/A interconnects and second C/A conduits coupled to respective ones of the second C/A interconnects,	See citations for element 1.e.2.	
1.e.4	the data conduits including at least first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects;	See citations for element 1.e.2.	
1.f	wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A	Figs. 2-3; 5:30-6:21 (“In the example schematically illustrated in FIG. 2, the memory package 200 includes a plurality of die interconnects 220 (e.g., die interconnects 220a, 220b). For example, certain versions of HMC have been reported to have 512 data ports per die, with the corresponding bits of each die all connected to a single die interconnect (e.g., TSV). . . . Each of these die interconnects 220	Figs. 2-3 5:46-6:35

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;	may be coupled to, or in electrical communication with at least one data port of at least one of the array dies 210. In certain embodiments, at least one of the die interconnects 220 is in electrical communication with at least one data port from each of at least two array dies 210 without being in electrical communication with a data port from at least one array die 210, which may be in electrical communication with a different die interconnect 220. [¶] For example, die interconnect 220a may be in electrical communication with a data port from array die 210a and a data port from array die 210b (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c or any data ports from array die 210d. The data ports of array dies 210a and 210b in electrical communication with the die interconnect 220a can be corresponding to the same data bit (e.g., D0). Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, . . .) of array dies 210a and 210b. These other die interconnects can be electrically isolated from the corresponding data ports of array dies 210c and 210d. However, continuing this example, the die interconnect 220b may be in electrical communication with a data port from array die 210c and a data port from array die 210d (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., D0) without being in electrical communication with any data ports from array die 210a and array die 210b. Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, . . .) of array dies 210c and 210d. Despite not being in electrical communication with any data ports from array die 210a and 210b, in some implementations, the die interconnect 220b may pass through the array dies 210a and 210b (as illustrated by the unfilled circles) e.g., through through-holes	

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		or vias of array dies 210a and 210b. For some implementations, each of the array dies 210 may be in electrical communication with corresponding die interconnects 220, without any of the die interconnects 220 being in electrical communication with all of the array dies 210. Where existing systems may utilize a single die interconnect to be in electrical communication with the corresponding data ports of each array die (e.g., the data ports corresponding to the same bit), certain embodiments described herein utilize multiple die interconnects to provide electrical communication to the corresponding data ports of the array dies (e.g., the data ports corresponding to the same data bit) with none of the multiple die interconnects in electrical communication with data ports of all the array dies.”); 6:35-47 (“The control die 230 may include a number of data conduits 232, which includes data conduits 232a and 232b. Each of these data conduits 232 may be configured to transmit a data signal to a single die interconnect 220. For example, the data conduit 232a may be configured to transmit a data signal to the die interconnect 220a without transmitting the data signal to the die interconnect 220b. Conversely, the data conduit 232b may be configured to transmit the data signal to the die interconnect 220b without transmitting the data signal to the die interconnect 220a (e.g., data conduit 232b is electrically isolated from die interconnect 220a and data conduit 232a is electrically isolated from die interconnect 220b).”); 8:23-51 (“In addition, the die interconnects 220 may use via holes to pass through an array die that is not configured to be in electrical communication with the die interconnect. For instance, die interconnect 220b may pass through array dies 210a and 210b using TSVs that do not enable electrical	6:48-59 8:35-62

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		communication between the die interconnect 220b and data ports of the array dies 210a and 210b (illustrated by the unfilled circles). In this way, the array dies 210a, 210b are not responsive to the data signal beings transmitted by the die interconnect 220b. However, the die interconnect 220b may be connected with at least one data port of each of the array dies 210c and 210d using a via (illustrated by the filled or darkened circles). In cases where the die interconnect passes through an array die that is not configured to be in electrical communication with the die interconnect, the TSV may include an insulator or an air gap between the die interconnect and the array die circuitry that is large enough to prevent electrical communication between the die interconnect and the array die circuitry. In certain embodiments, the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same. However, in such cases, electrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be stubs. These stubs are not configured to provide electrical communication with the memory cells of the array die.”); 9:18-36 (“In some embodiments, the control die 230 may include additional command/address conduits 240 and die interconnects 242, which may be in electrical communication with at least one port of each of the array dies 210. For simplicity, FIG. 2 shows only a single such conduit 240 and die interconnect 242. The command/address conduits 240 are configured to provide corresponding signals to the die interconnects 242. These signals may be command signals, address signals, or may serve as both command and address signals (e.g., may include a memory cell address and a write command or a read	9:28-45

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		command) either simultaneously or based on a determining criterion, such as the edge of a clock signal. The command die 230 may include a command/address conduit 240 and corresponding die interconnect 242 for each bit of the command/ address signals that the memory package 200 is configured to support. The number of bits of the command/address signals may be the same or may be different from the number of data bits of the memory package 200.”); 10:3-4 (“However, for ease of illustration and to simplify discussion, certain elements are omitted in FIG. 3.”); 10:10-26 (“The memory package 300 may include a plurality of array dies 310 (e.g., array dies 310a-310h). In the implementation illustrated in FIG.3, the memory package includes eight array dies. However, as stated earlier, the memory package 300 may include more or fewer array dies. Each of the array dies 310 may include one or more ports (not shown) that enable electrical communication between the circuitry of the array dies 310 and one or more die interconnects 320. Each of these die interconnects 320 may be coupled to, or in electrical communication with at least one port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical communication with a port from at least one array die 310, which may be in electrical communication with a different die interconnect 320.”); 10:27-32 (“In addition to the plurality of array dies 310, the memory package 300 includes a control die 330. In some embodiments, the control die 330 may include a number of conduits 332 (e.g., conduits 332a-332f). Each of these	10:12-13 10:18-34 10:35-40

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		conduits 332 may be configured to transmit a signal to a single die interconnect 320.”); 10:48-59 “In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits configured to provide a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal to one or more die interconnects. Consequently, in some embodiments, the drivers 334 may be configured to drive signals other than data signals.”; See also citations for elements 1.c.1., 1.d.1-1.d.3.	10:56-67
1.g	wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with	See citations for element 1.f.	

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	any C/A port on any of the first plurality of DRAM dies;		
1.h.1	wherein a first data interconnect of the first data interconnects is in electrically communication with corresponding data ports on the first plurality of DRAM dies and not in electrical communication with any data port on any of the second plurality of DRAM dies,	See citations for element 1.f.	
1.h.2	each of the first data interconnects including a first respective set of TSVs, the first respective set of TSVs including a TSV in each DRAM die of the	8:15-22 (“Moreover, the die interconnects 220 may use vias, or through-silicon vias (TSVs) to couple with or to electrically communicate with an array die. For instance, die interconnect 220a may be connected with data ports of the array dies 210a and 210b using vias (illustrated by the filled or darkened circles). Examples of TSVs which may be used with the present disclosure are described further in U.S. Pat. Nos. 7,633,165 and 7,683,459.”));	8:27-34

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	first plurality of DRAM dies and at least one TSV in at least one DRAM die of the second plurality of DRAM dies,	8:25-35 (“For instance, die interconnect 220b may pass through array dies 210a and 210b using TSVs that do not enable electrical communication between the die interconnect 220b and data ports of the array dies 210a and 210b (illustrated by the unfilled circles). . . However, the die interconnect 220b may be connected with at least one data port of each of the array dies 210c and 210d using a via (illustrated by the filled or darkened circles).”); 10:33-47 (“Further, implementations of the conduits 332 may include one or more drivers 334 (e.g., drivers 334a-334f). Each of the drivers 334 may be configured to drive a signal along a corresponding die interconnect 320. For instance, the driver 334a of the conduit 332a may be configured to drive a signal along the die interconnect 320a to one or more of the array dies 310a and 310b. As a second example, the driver 334b of the conduit 332b may be configured to drive a signal along the die interconnect 320b to one or more of the array dies 310c and 310d. Although the die interconnect 320b may pass through the array dies 310a and 310b, because the die interconnect 320b, in the example illustrated in FIG. 3, is not configured to be in electrical communication with the array dies 310a and 310b, the driver 334b does not drive the signal to the array dies 310a and 310b.”); See also citations for elements 1.c.1, 1.d.1-1.d.3.	8:37-47 10:41-55
1.h.3	wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical	See citations for element 1.h.2	

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	communication with a corresponding data port on the each DRAM die, and wherein the at least one TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;		
1.i	wherein a second data interconnect of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of	See citations for element 1.h.2	

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	the first plurality of DRAM dies;		
1.j	wherein a first conduit of the first data conduits is coupled between the first data interconnect and a first data terminal of the data terminals, and a second conduit of the second data conduits is coupled between the second data interconnect and the first data terminal;	Figs. 2-4; 6:56-63 (“Each of the data conduits 232 may be configured to receive the data signal from a common source. For instance, the data conduit 232a and the data conduit 232b may each receive a substantially similar, if not identical, data signal from the same signal source (e.g. the data signal corresponding to the same data bit). The source of the data signal may include a data path, a driver, a latch, a pin, or any other construct that may provide a data signal to a data conduit.”); 10:60-64 (“Generally, the signal that each of the drivers 334 drive to the corresponding die interconnects 320 is from a common source. Thus, each of the drivers 334, in certain embodiments, is driving the same signal to each corresponding die interconnect 320.”); 14:52-57 (“In addition to the drivers 334 of the control die 330, the memory package 300 may include one or more pre-drivers 340. A pre-driver 340, shown schematically in FIG. 3, may be large enough to drive a signal (e.g., a data signal) to any of the drivers 332 and subsequently, to any of the array dies 310.”); 14:66-15:7 (“Just as the memory package 300 may include a pre-driver 340 for providing a signal to the conduits 332, the memory package 300 may include a post-driver (not shown) for driving an output signal from the control die 330. This post-driver may drive the output signal to additional latches and/or drivers. In some embodiments, the post-driver may drive the signal from the memory	Figs. 2-4 7:1-8 11:1-5 15:4-8 15:17-25

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		package 300 to a bus or other electrical path that is in electrical communication with the memory package 300.”);	
1.k.1	wherein the control die further includes control logic configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more of the C/A terminals,	Figs. 2-4; 6:32-34 (“Further, in some embodiments, the control die 230 may comprise a logic layer (e.g., the logic layer of an HMC).”); 9:61-64 (“In some embodiments, the control die 230 may determine the array die 210 to select based on, for example, an address signal. In such embodiments, the control die may generate the chip select signals.”); 15:8-20 (“FIG. 4 illustrates an example embodiment of a driver structure 400 of a control die (e.g. control die 230) in accordance with the present disclosure. The driver structure 400 is configured for a single data bit. Thus, a control die for a 32-bit memory package will generally include at least 32 instances of the driver structure 400, one per bit. In some embodiments, the control die 230 may include the driver structure 400 in place of the combination of drivers 232a and 232b. Similarly, in certain embodiments, the control die 330 may include a structure similar to the driver structure 400 in place of the drivers 334. In such embodiments, the driver structure 400 would be modified to enable a signal (e.g., data signal) to be driven to the six conduits 332.”); 15:31-37 (“In some embodiments, the driver structure 400 is bi-directional. In such embodiments, operation of the drivers 404a and 404b, and 408a and 408b may be controlled or enabled by a control signal (e.g., a directional control signal). This control signal, in some cases, may correspond to one or more of a command/address signal (e.g., read/write) and a chip select signal. In some implementations, the drivers 404a and 404b may drive a signal to the array die	Figs. 2-4 6:46-47 10:2-6 15:26-38 15:48-57

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		corresponding to the chip select signal, and not to array dies that do not correspond to a chip select signal.”); 20:1-17 (“For example, assuming that the memory package 300 implements selective isolation, if a chip select signal is received that corresponds to a selection of array die 310b, then the driver 334a will drive a signal along the die interconnect320a to the array die 310b, and the remaining drivers (e.g., drivers 334b 334f) will maintain their state (e.g., not drive the signal). Address pass-through is described in further detail below. [¶] The data path control circuit of certain embodiments may have at least two operational modes: mode-C (HCDIMM/ RDIMM Compatible mode) and mode-3DS (3DS DIMM compatible mode). In mode-C, the array dies 824 (e.g. a DDSP) receive the data path control signals from the register device 812, which can be configured to control a command/ address time slot and a data bus time slot. In mode-3DS, the control die 822 internally generates the data path control signals to ensure the proper operation of the data path.”); 21:4-14 (“Further, the register device 812 may generate data path control signals, which can be provided to a control die 822, or isolation device, of a memory package 820 via one or more data path control lines 816. In certain embodiments, the control dies 822 can include some or all of the embodiments described above with respect to the control dies 230 and 330. Moreover, in certain embodiments, the memory packages 820 can include some or all of the embodiments described above with respect to the memory package 200 and 300. In general, the memory module 812 may include one or more memory packages 820.”);	20:19-34 21:21-31

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		21:63-22:5 (“In some embodiments, the memory module 810 is selectively configurable into two operational modes. In the first operational mode, the register device 812 generates data path control signals provided to the control dies 822 via the data path control lines 816. The control dies 822 may decode command/address signals included with the data path control signals generated by the register device 812. In some implementations, the control dies 822 use the data path control signals to operate the data path control circuits of the control dies 822.”); 19:4-7 (“In contrast to the JEDEC DDR3 RDIMM standard, the 3DS-DIMM proposal requires the DRAM package 720 to include the controller die 722 that controls all data paths timing and operations.”).	22:12-21 19:21-24
1.k.2	wherein the one or more C/A signals do not include any chip select signal;	9:25-30 (“These signals may be command signals, address signals, or may serve as both command and address signals (e.g., may include a memory cell address and a write command or a read command) either simultaneously or based on a determining criterion, such as the edge of a clock signal.”); 9:56-59 (“For example, a register (not shown) that is part of a memory module that includes the memory package 200 may determine the chip select signals and drive the chip select signals to the array dies 210.”); 9:61-64 (“In some embodiments, the control die 230 may determine the array die 210 to select based on, for example, an address signal. In such embodiments, the control die may generate the chip select signals”); 21:4-14 (“Further, the register device 812 may generate data path control signals, which can be provided to a control die 822, or isolation device, of a	9:35-39 9:64-10:1 10:2-6 21:21-31

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		memory package 820 via one or more data path control lines 816. In certain embodiments, the control dies 822 can include some or all of the embodiments described above with respect to the control dies 230 and 330. Moreover, in certain embodiments, the memory packages 820 can include some or all of the embodiments described above with respect to the memory package 200 and 300. In general, the memory module 812 may include one or more memory packages 820.”); 21:41-47 (“Each of the control dies 822 may be configured to receive data signals from the memory control hub 802 via the data bus 818. Further, the control dies 822 may provide data signals to the memory control hub 802 via the data bus 818. The control dies 822 may also receive data path control signals and/or command/address signals from the register device 812 via the data path control lines 816.”); 21:63-22:5 (“In some embodiments, the memory module 810 is selectively configurable into two operational modes. In the first operational mode, the register device 812 generates data path control signals provided to the control dies 822 via the data path control lines 816. The control dies 822 may decode command/address signals included with the data path control signals generated by the register device 813. In some implementations, the control dies 822 use the data path control signals to operate the data path control circuits of the control dies 822.”); 22:12-17 (“Other operational modes may also be possible. In some embodiments, the data path control signals generated by the register device 812 may include decoded command/address signals that are decoded from	21:57-63 22:12-21 22:28-33

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		command/address signals received from the memory control hub 802 via the command/address bus 814.”).	
1.1	wherein the die interconnects further include first unidirectional interconnects configured to conduct signals from one or more DRAM dies of the stacked DRAM dies to the control die and not configured to conduct any signal from the control die to any of the stacked DRAM dies;	9:6-17 (“In certain embodiments, the same die interconnects and the same corresponding data conduits may be used to transfer data both to and from the array dies 210. In such embodiments, the die interconnects may be bidirectional. In alternative embodiments, separate die interconnects and corresponding data conduits may be used to transfer data to the array dies 210 and data from the array dies 210 to the control die 230. Thus, such embodiments may include double the number of die interconnects and data conduits as embodiments that use the same die interconnect to transfer data to and from an array die.”); 14:33-51 (“In some implementations, one or more of the die interconnects 320 are configured to be bi-directional, thereby enabling a signal to be driven to the array dies 310 via the die interconnect 320, and to enable a signal received from the array dies 310 along the same die interconnect 320 to be transmitted to a corresponding conduit 332 of the control die 330. Alternatively, the memory package 300 comprises one or more die interconnects 320 that are configured to enable a signal to be driven to the array dies 310 without enabling a signal to be received from the array dies 310 (e.g., the die interconnects 320 may not be bi-directional). In certain embodiments where one or more of the die interconnects 320 are not bi-directional, the memory package 300 may include additional die interconnects (not shown) that are in electrical communication with the one or more additional conduits or drivers and that are configured to enable a signal from the array dies 310 to be transmitted to the one or more additional conduits or drivers.”);	9:17-26 14:53-15:3

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		16:15-25 (“For example, instead of the drivers 404a and 408a being in electrical communication with the same conduit 406a, each of the drivers 404a and 408a can be in electrical communication with a separate conduit and consequently a separate die interconnect. In such an example, the drivers 404a and 408a may still be in electrical communication with the same input/output port 402, or each driver may be in electrical communication with a separate port, the driver 404a in electrical communication with an input port, and the driver 408a in communication with an output port.”); <i>See also, e.g.,</i> 10:10-26 (“The memory package 300 may include a plurality of array dies 310 (e.g., array dies 310a-310h). In the implementation illustrated in FIG.3, the memory package includes eight array dies. However, as stated earlier, the memory package 300 may include more or fewer array dies. Each of the array dies 310 may include one or more ports (not shown) that enable electrical communication between the circuitry of the array dies 310 and one or more die interconnects 320. Each of these die interconnects 320 may be coupled to, or in electrical communication with at least one port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical communication with a port from at least one array die 310, which may be in electrical communication with a different die interconnect 320.”); 10:27-32 (“In addition to the plurality of array dies 310, the memory package 300 includes a control die 330. In some embodiments, the control die 330 may include a number of conduits 332 (e.g., conduits 332a-332f). Each of these	16:31-41 10:18-34 10:35-40

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
		conduits 332 may be configured to transmit a signal to a single die interconnect 320.”); 10:48-54 (“In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320.”); 3:56-60 (“In addition to the below, the following U.S. patents are incorporated in their entirety by reference herein: U.S. Patent Nos. 7,289,386, 7,286,436, 7,442,050, 7,375,970, 7,254,036, 7,532,537, 7,636,274, 7,630,202, 7,619,893, 7,619,912, 7,811,097. Further, the following U.S. patent applications are incorporated in their entirety by reference herein: U.S. patent application Ser. Nos. 12/422,912, 12/422,853, 12/577,682, 12/629,827, 12/606,136, 12/874,900, 12/422,925, 12/504,131, 12/761,179, and 12/815,339.”); <i>See also, e.g.,</i> US 7,619,912, 23:60-25:5 (DQS signal collision in back-to-back read operations).	10:56-62 4:8-16
1.m	wherein the die interconnects further include second unidirectional interconnects configured to conduct signals from the control	See citations for element 1.l	

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	die to one or more DRAM dies of the stacked DRAM dies and not configured conduct any signal from any of the stacked DRAM dies to the control die;		
1.n	wherein the control die is configured to receive signals from one or more DRAM dies of the stacked DRAM dies via the first unidirectional interconnects and is not configured to drive any signal to any of the stacked DRAM dies via any of the first unidirectional interconnects;	See citations for element 1.l	

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
1.o	wherein the control die is configured to drive signals to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects and is not configured to receive any signal from any of the stacked DRAM dies via any of the second unidirectional interconnects; and	See citations for element 1.1	
1.p.1	wherein the control die is configured to, in response to the first set of C/A signals, receive first signals associated with the memory read operation from a DRAM die of the stacked DRAM dies via the first	See citations for element 1.1.	

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	Claim 1	Support in '087 Specification (EX1001)	8,787,060 (EX1069)
	unidirectional interconnects, and		
1.p.2	in response to the second set of C/A signals, drive second signals associated with the memory write operation to one or more DRAM dies of the stacked DRAM dies via the second unidirectional interconnects.	See citations for element 1.1.	

Claim 2	Support in '087 Written Description	'060 patent
2. The DRAM package of claim 1, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.	Fig. 3; 5:20-24 (“For example, as illustrated in FIG. 3, the memory package 200 may include eight array dies. As further examples, the memory package 200 may include three or sixteen array dies.”).	Fig. 3 5:37-40

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Claim 3	Support in '087 Written Description	'060 patent
3. The DRAM package of claim 2, wherein the stacked DRAM dies include 16 stacked DRAM dies.	See citations for claim 2.	

Claim 4	Support in '087 Written Description	'060 patent
4. The DRAM package of claim 1, wherein: the first conduit includes a first driver configured to have a first driver size and the second conduit includes a second driver configured to have a second driver size; and the second driver size is different from the first driver size.	10:65–11:2 (“The size of the drivers 334 is generally related to the load on the driver 334. In certain embodiments, the load on each driver 334 corresponds to the load of the respective conduit 332. Although not limited as such, the load may be measured as a capacitive load, such as a parasitic capacitance.”); 13:49-14:19 (“In some cases, the load on each conduit 332 and/or driver 334 may be evenly balanced. In other words, the load on each conduit 332 and/or driver 334 may be substantially the same. To achieve a balanced load, each of the conduits 332 may be in electrical communication with a combination of array dies 310 and die interconnect 320 segments that results in a load that is substantially equivalent to the loads of the other conduits 332. In certain embodiments, the load of the conduits 332 is balanced despite each conduit 332 being in electrical communication with a different subset of the array dies 310. However, in alternative embodiments, the load of each conduit 332 and/or driver 334 may differ. This difference in the load of the conduits 332 and/or drivers 334 may be a design decision (e.g. to maintain a specific number of drivers). Alternatively, or in addition, the load difference between conduits 332 and/or drivers 334 may occur because the loads of the array dies 310 and the die interconnect segments 320 do not allow for perfect or substantially even load balancing. [¶] As previously stated, in some	11:6-10 14:4-39

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Claim 4	Support in '087 Written Description	'060 patent
	embodiments the loads of the conduits 332 and/or drivers 334 may be balanced to minimize the difference between any pair of conduits 332 and/or drivers 334. For example, as illustrated in FIG. 3, a driver in electrical communication with a longer die interconnect, which may consequently include more die interconnect segments, is likely to obtain a larger load contribution from the die interconnect than a driver in electrical communication with a shorter die interconnect (e.g., compare driver 334f to 334a). Thus, the driver in electrical communication with the longer die interconnect may be in electrical communication with fewer array dies than the driver in electrical communication with the shorter die interconnect (e.g. compare driver 334f to 334a). The selection of die interconnect length and the selection of array dies to place in electrical communication with the die interconnects may therefore be dependent on the load of each segment of the die interconnects 320 and the loads of the array dies 310.”)	

Claim 5	Support in '087 Written Description	'060 patent
5. The DRAM package of claim 1, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package in parallel and subsequently	8:54-9:3 (“The memory package 200 may generally include as many additional data conduits and corresponding die interconnects as the number of bits the memory package 200 is designed or configured to support per memory address. Thus, if, for example, the memory package 200 is configured to be a 16-bit memory, the memory package 200 may include 16 pairs of data conduits 232 and 16 pairs of corresponding die interconnects 220. Similarly, if the memory package 200 is configured as a 32-or 64-bit memory, the memory package 200 may include 32 or 64 pairs of data conduits 232 and 32 or 64 pairs of corresponding die interconnects 220. Generally, the data conduits and die interconnects for each bit are configured identically. Thus, for the memory package 200, each data conduit is configured to be in	8:65-9:14

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Claim 5	Support in '087 Written Description	'060 patent
conducted via the first data interconnects in parallel.	electrical communication with a die interconnect that is configured to be in electrical communication with a pair of the array dies 210.”)	

Claim 6	Support in '087 Written Description	'060 patent
6.a The DRAM package of claim 1, wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals; and	9:18-21 “The command die 230 may include a command/address conduit 240 and corresponding die interconnect 242 for each bit of the command/address signals that the memory package 200 is configured to support.” 9:37-64 “In addition, in certain embodiments, the control die 230 may include a plurality of chip select conduits 250 (e.g., chip select conduits 250a-250d as shown in FIG. 2). Further, the control die 230 may include corresponding die interconnects 252 (e.g., die interconnects 252a-252d) with one die interconnect 252 in electrical communication with one chip select conduit 250 and one array die 210. Each of the die interconnects 252 may be in electrical communication with a different array die 210. For example, the die interconnect 252a may be in electrical communication with the array die 210a and the die interconnect 252b may be in electrical communication with the array die 210b. Each of the chip select conduits 250 may be configured to provide a chip select signal to a corresponding array die 210 via a corresponding die interconnect 252. [¶] In some embodiments, the control die 230 may include additional drivers that are configured to drive the chip select signals along the die interconnects 252. Alternatively, the chip select signals may be driven by drivers that are external to the control die 230. For example, a register (not shown) that is part of a memory module that includes the memory package 200 may determine the chip select signals and drive the chip select signals to the array dies 210. As a second example, the chip select	9:39-42 9:46-10:6

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Claim 6	Support in '087 Written Description	'060 patent
	signals may be provided by an MCH. In some embodiments, the control die 230 may determine the array die 210 to select based on, for example, an address signal. In such embodiments, the control die may generate the chip select signals.”); 15:35-37 (“This control signal, in some cases, may correspond to one or more of a command/address signal (e.g., read/write) and a chip select signal.”); 21:4-14 (“Further, the register device 812 may generate data path control signals, which can be provided to a control die 822, or isolation device, of a memory package 820 via one or more data path control lines 816. In certain embodiments, the control dies 822 can include some or all of the embodiments described above with respect to the control dies 230 and 330. Moreover, in certain embodiments, the memory packages 820 can include some or all of the embodiments described above with respect to the memory package 200 and 300. In general, the memory module 812 may include one or more memory packages 820.”); 21:41-47 (“Each of the control dies 822 may be configured to receive data signals from the memory control hub 802 via the data bus 818. Further, the control dies 822 may provide data signals to the memory control hub 802 via the data bus 818. The control dies 822 may also receive data path control signals and/or command/address signals from the register device 812 via the data path control lines 816.”); 21:63-22:5 (“In some embodiments, the memory module 810 is selectively configurable into two operational modes. In the first operational mode, the register device 812 generates data path control signals provided to the control dies 822 via the data path control lines 816. The control dies 822 may decode command/address signals included with the data path control signals	15:51-54 21:21-31 21:57-63 22:12-21

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Claim 6	Support in '087 Written Description	'060 patent
	generated by the register device 812. In some implementations, the control dies 822 use the data path control signals to operate the data path control circuits of the control dies 822.”); 22:12-17 (“Other operational modes may also be possible. In some embodiments, the data path control signals generated by the register device 812 may include decoded command/address signals that are decoded from command/address signals received from the memory control hub 802 via the command/ address bus 814.”).	22:28-33
6b. the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second data signals;	See citations for element 6.a.	
6c. wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.	22:18-42 (“In some embodiments, the register device 812 may be configured to perform rank multiplication. In addition, or alternatively, the control dies 822 may be configured to perform rank multiplication . . . In certain embodiments, when the memory module 810 is operating in the second operation module as described above, the memory module 810 does not perform rank multiplication.”).	22:34-57

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Claim 7	Support in '087 Written Description	'060 patent
7. The DRAM package of claim 1, wherein the control die is further configured to control timing of command/address signals driven to the stacked DRAM dies and/or timing of data signals communicated between the stacked DRAM dies and the data terminals to prevent signal collisions.	18:49-53 (“The controller die 722 may include data buffers, a data path timing controller, a secondary command/address buffer, a programmable secondary 1-to-2 rank decoder, and a data path signal (e.g., ODT, ODT, RTT) controller.”);	18:65-19:2
	19:4-7 (“In contrast to the JEDEC DDR3 RDIMM standard, the 3DS-DIMM proposal requires the DRAM package 720 to include the controller die 722 that controls all data paths timing and operations.”);	19:21-24
	20:9-17 (“The data path control circuit of certain embodiments may have at least two operational modes: mode-C (HCDIMM/ RDIMM Compatible mode) and mode-3DS (3DS DIMM compatible mode). In mode-C, the array dies 824 (e.g. a DDSP) receive the data path control signals from the register device 812, which can be configured to control a command/ address time slot and a data bus time slot. In mode-3DS, the control die 822 internally generates the data path control signals to ensure the proper operation of the data path.”);	20:26-34
	20:20-24 (“the memory module 800 may comprise a set of optional control input pins (in addition to the package pins that are included in 3DS-DRAM packages) which in mode-C receive the data path control signals from the register device 812.”);	20:37-41
	21:7-13 (“In certain embodiments, the control dies 822 can include some or all of the embodiments described above with respect to the control dies 230 and 330. Moreover, in certain embodiments, the memory packages 820 can include some or all of the embodiments described above with respect to the memory package 200 and 300.”);	21:24-29

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Claim 7	Support in '087 Written Description	'060 patent
	21:22-40 (“Some implementations of the control dies 822 include a plurality of command/address buffers (not shown). These buffers may comprise latches. In certain embodiments, the buffers are configured to hold command/address signals to control the timing of command/address signals to control the timing of command/address signals. In some cases, controlling the timing of the command/address signals may reduce or slow signal degradation. In some implementations, the control dies 822 include a plurality of data buffers, which may control the timing of data signals to reduce or slow signal degradation. Further, the control dies 822 may include a data path control circuit (not shown) that is configured to control command/address time slots and data bus time slots. Controlling the command/address time slots and the data bus time slots enables the control dies 822 to reduce or prevent signal collisions caused by multiple memory packages 820 sharing the data path control lines 816 and the data bus 818. In some implementations, the data path control circuit may be separate from the control die 822.”).	21:39-56

Claim 8	Support in '087 Written Description	'060 patent
8. The DRAM package of claim 1, wherein the at least one DRAM die of the second plurality of DRAM dies has at least one electrical connection leading from the at least one TSV, the at least one electrical connection is not electrically	8:41-51 (“In certain embodiments, the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same. However, in such cases, electrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be stubs. These stubs are not configured to provide electrical communication with the memory cells of the array die.”).	8:53-62

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Claim 8	Support in '087 Written Description	'060 patent
connected to any data port on the at least one DRAM die.		

	Claim 9	Support in '087 Written Description
9.a	A method, comprising:	Throughout the specification
9.b.1	at a dynamic random access memory (DRAM) package including stacked DRAM dies, the stacked DRAM dies including a first plurality of DRAM dies and a second plurality of DRAM dies, each DRAM die of the stacked DRAM dies including command and/or address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received at the C/A ports,	See citations for elements 1.a, 1.b.1, and 1.b.2.
9.b.2	the DRAM package further including an interface, via which the DRAM package receives C/A signals, and via which the DRAM package receives or outputs data signals in response to C/A signals received via the interface, the interface including terminals,	See citations for element 1.c.1.
9.b.3	the DRAM package further including die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the stacked DRAM dies,	See citations for elements 1.d.1-1.d.3.
9.b.4	the die interconnects including C/A interconnects, data interconnects, first unidirectional interconnects and second unidirectional interconnects, the C/A interconnects	See citations for elements 1.d.1, 1.d.2, and 1.l.

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	Claim 9	Support in '087 Written Description
	including first C/A interconnects and second C/A interconnects, the data interconnects including first data interconnects and second data interconnects,	
9.c	receiving via the interface a first set of C/A signals for a memory read operation and a second set of C/A signals for a memory write operation, the first set of C/A signals including one or more first signals to select a first DRAM die in the first plurality of DRAM dies to respond to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the first plurality of stacked DRAM dies to respond to the second set of C/A signals;	See citations for element 1.c.1 and claim 6.
9.d.1	in response to the first set of C/A signals, driving the first set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving from the first DRAM die first data signals associated with the first set of C/A signals via the first data interconnects, driving the first data signals to the interface, and	See citations for elements 1.e.1 to 1.e.3.
9.d.2	receiving from the first DRAM die one or more signals associated with the first set of C/A signals via one or more of the first unidirectional interconnects;	See citations for element 1.l.
9.e.1	in response to the second set of C/A signals, driving the second set of C/A signals to C/A ports of the first plurality of DRAM dies via the first C/A interconnects, receiving second signals associated with the second set of C/A signals from the interface, driving the second data signals to the first plurality of DRAM dies via the first data	See citations for element 1.c.1 and claim 6.

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	Claim 9	Support in '087 Written Description
	interconnects and not to any of the second plurality of DRAM dies via any of the data interconnects, and	
9.e.2	driving one or more signals associated with the second set of C/A signals to the first plurality of DRAM dies via one or more of the second unidirectional interconnects;	See citations for element 1.l.
9.f.1	wherein each of the first data interconnects is in electrical communication with corresponding data ports on a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port on any other DRAM die of the stacked DRAM dies,	See citations for element 1.f.
9.f.2	each of the first data interconnects including a respective set of TSVs, the respective set of TSVs including a TSV in each DRAM die of the first plurality of DRAM dies and at least one additional TSV in at least one DRAM die of the second plurality of DRAM dies,	See citations for element 1.h.2.
9.f.3	wherein the TSV in the each DRAM die of the first plurality of DRAM dies is in electrical communication with a corresponding data port on the each DRAM die, and wherein the at least one additional TSV in the at least one DRAM die of the second plurality of DRAM dies is not in electrical communication with any data port on the at least one DRAM die;	See citations for element 1.h.2
9.g	wherein each of the second data interconnects is in electrical communication with corresponding data ports on the second plurality of DRAM dies and not in electrical communication with any data port on any of the first plurality of DRAM dies;	See citations for elements 1.f and 1.h.2

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 9	Support in '087 Written Description
9.h	wherein a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first plurality of DRAM dies and not in electrical communication with any C/A port on any of the second plurality of DRAM dies;	See citations for element 1.f.
9.i	wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second plurality of DRAM dies and not in electrical communication with any C/A port on any of the first plurality of DRAM dies;	See citations for element 1.f.
9.j.1	wherein the first unidirectional interconnects are not configured to conduct any signals to any of the stacked DRAM dies and	See citations for element 1.l.
9.j.2	the second unidirectional interconnects are not configured to conduct any signals from any of the stacked DRAM dies;	See citations for element 1.l.
9.k	wherein the first data signals include at least 32 signals that are received via the first data interconnects in parallel and subsequently driven to the interface in parallel; and	See citations for claim 5.
9.l	wherein the second data signals include at least 32 signals that are received from the interface in parallel and subsequently driven to the first plurality of DRAM dies in parallel.	See citations for claim 5.

Claim 10	Support in '087 Written Description
10. The method of claim 9, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.	See citations for claim 2

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U.S. Patent No. 12,308,087 – Written Description Support

Claim 11	Support in '087 Written Description
11. The method of claim 9, wherein the first data signals include 32 or 64 signals conducted via the first data interconnects in parallel and subsequently output by the DRAM package via the interface in parallel, and wherein the second data signals include 32 or 64 signals received by the DRAM package via the interface in parallel and subsequently conducted via the first data interconnects in parallel.	See citations for claim 5

Claim 12	Support in '087 Written Description
12.a The method of claim 9, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, the method further comprising:	See citations for element 17.a.2
12.b enabling first drivers to receive and drive the first data signals in response to the first set of C/A signals;	See citations for element 17.b.
12.c enabling second drivers to receive and drive the second data signals in response to the second set of C/A signals; and	See citations for element 17.b.
12.d maintaining each of the first drivers and the second drivers in a non-driving state after driving of the first data signals by the first drivers and before receiving of the second data signals by the second drivers;	See citations for element 17.b.
12.e wherein any driver of the first and second drivers in a non-driving state is not configured to receive or drive any signal.	See citations for element 17.b.

	Claim 13	Support in '087 Written Description	'060 patent
13.a	A dynamic random access memory	See citations for element 1.a	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
	(DRAM) package, comprising:		
13.b	a plurality of stacked DRAM dies, each DRAM die of the plurality of stacked DRAM dies including command/address (C/A) ports, data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells in response to C/A signals received via the C/A ports, each of the data ports being a bi-directional data port;	See citations for elements 1.b.1 and 1.b.2	
13.c	an interface, via which the DRAM package receives command/address (C/A) signals, and via which the DRAM	See citations for element 1.c.1	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
	package receives or outputs data signals, the interface including terminals, the terminals including C/A terminals and data terminals;		
13.d	die interconnects, each of the die interconnects including one or more through silicon vias (TSVs) in one or more DRAM dies in the plurality of stacked DRAM dies; and	See citations for elements 1.d.1-1.d.3, 1.h.1-1.h.3, 1.i.	
13.e	a control die coupled between the interface and the plurality of stacked DRAM dies, the control die including signal conduits coupled, respectively, to the die interconnects;	See citations for elements 1.e.1 to 1.e.4.	
13.f	wherein: the die interconnects include a first set of	See citations for elements 1.d.1-1.d.2, 1f-1i, 1l-1p.2	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
	C/A interconnects, a second set of C/A interconnects, first data interconnects, second data interconnects, first unidirectional interconnects, and second unidirectional interconnects;		
13.g	each of the first data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port on each of a first subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port on any of a second subset of the plurality of stacked DRAM dies;	See citations for elements 1.d.1-1.d.2, 1f-1i. <i>See also, e.g.,</i> Figs. 2-3 and associated description; 9:7-10 (“In certain embodiments, the same die interconnects and the same corresponding data conduits may be used to transfer data both to and from the array dies 210. In such embodiments, the die interconnects may be bi-directional.”); 14:33-40 (“In some implementations, one or more of the die interconnects 320 are configured to be bidirectional, thereby enabling a signal to be driven to the array dies 310 via the die interconnect 320, and to enable a signal received from the array dies 310 along the same die interconnect 320 to be transmitted to a corresponding conduit 332 of the control die 330.”).	Figs. 2-3 9:17-20 14:53-59

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	Claim 13	Support in '087 Written Description	'060 patent
13.h.1	each of the second data interconnects is a bi-directional interconnect configured to be in electrical communication with a corresponding data port of each of the second subset of the plurality of stacked DRAM dies and is not configured to be in electrical communication with any data port of the first subset of the plurality of stacked DRAM dies,	See citations for element 13.g.	
13.h.2	each subset of the first subset and the second subset of the plurality of stacked DRAM dies including two or more DRAM dies;	See citations for element 1.b.1; <i>see also e.g.</i> , Figs. 2-3 and associated description.	Figs. 2-3
13.i	the control die is configurable to drive a first set of C/A signals received by the DRAM package via the	See citations for elements 1.c.2, 1.e.1-1.e.4.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
	interface to the first subset of the plurality of stacked DRAM dies via the first C/A interconnects, and is further configurable to drive a second set of C/A signals received by the DRAM package via the interface to the second subset of the plurality of stacked DRAM dies via the second C/A interconnects;		
13.j	a first C/A interconnect of the first C/A interconnects is in electrical communication with corresponding C/A ports on the first subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of	See citations for elements 1.b.1, 1.d.1, 1f, 1g.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
	the second subset of the plurality of stacked DRAM dies;		
13.k	wherein a second C/A interconnect of the second C/A interconnects is in electrical communication with corresponding C/A ports on the second subset of the plurality of stacked DRAM dies and not in electrical communication with any C/A port on any of the first subset of the plurality of stacked DRAM dies;	See citations for elements 1.b.1, 1.d.1, 1f, 1g.	
13.l	the first set of C/A signals include one or more first signals to select a first DRAM die in the first subset of the plurality of stacked DRAM dies to respond	See citations for elements 1.b.1, 1.d.1, 1f, 1g, 1.k.1-1.k.2. Figs. 2-3; 9:18-21 (“The command die 230 may include a command/address conduit 240 and corresponding die interconnect 242 for each bit of the command/address signals that the memory package 200 is configured to support.”);	Figs. 2-3 9:39-43

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
	to the first set of C/A signals, and the second set of C/A signals include one or more second signals to select a second DRAM die in the second subset of the plurality of stacked DRAM dies to respond to the second set of C/A signals;	9:37-51 (“In addition, in certain embodiments, the control die 230 may include a plurality of chip select conduits 250 (e.g., chip select conduits 250a-250d as shown in FIG. 2). . . Each of the chip select conduits 250 may be configured to provide a chip select signal to a corresponding array die 210 via a corresponding die interconnect 252.”); 15:35-37 (“This control signal, in some cases, may correspond to one or more of a command/address signal (e.g., read/write) and a chip select signal.”); See also 9:30-36, 9:37-10:9, 15:31-51, 16:5-12, 20:1-17, 21:63-22:17, 22:18-42	9:46-60 15:51-54 9:39-45, 9:46-10:17, 15:48-67, 16:21-28, 20:19-34, 22:12-27, 22:34-57
13.m	the control die is further configurable to drive first data signals associated with the first set of C/A signals between the first data interconnects and the interface and to drive second data signals associated with the second set of C/A signals between the second data	See citations for element 1.k.1; <i>See also</i> 15:8-16:4 (“FIG. 4 illustrates an example embodiment of a driver structure 400 of a control die (e.g. control die 230) in accordance with the present disclosure. . . The driver structure 400 can include an input/output port 402 configured to receive or send a signal, such as a data signal. Signals received at the input/output port 402 can be provided to the drivers 404a and 404b. In turn, these drivers 404a and 404b can drive the signal to conduits 406a and 406b respectively, which are in electrical communication with corresponding die interconnects. Each of the die interconnects may be in electrical communication	15:26-48

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
	interconnects and the interface;	with different array dies in accordance with certain embodiments described herein. . . In some embodiments, the driver structure 400 is bi-directional. . .”).	
13.n	the control die is further configurable to, in response to the first set of C/A signals being for a memory read operation, receive one or more first signals associated with the memory read operation from one or more of the first unidirectional interconnects, and in response to the second set of C/A signals being for a memory write operation, drive one or more second signals associated with the memory write operation to one or more of the second unidirectional interconnects;	See citations for elements 1.1-1.p.2.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
13.o	the one or more of the first unidirectional interconnects are configured to conduct the one or more first signals from the first DRAM die to the control die and not configured to conduct any signal from the control die to any of the plurality of stacked DRAM dies;	See citations for elements 1.1-1.p.2.	
13.p	the one or more of the second unidirectional interconnects are configured to conduct the one or more second signals from the control die to the second DRAM die and not configured to conduct any signal from any of the plurality of stacked DRAM dies to the control die;	See citations for elements 1.1-1.p.2.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
13.q	the control die is configurable to receive the one or more first signals from the first DRAM die via the one or more of the first unidirectional interconnects and is not configurable to drive any signal to any of the plurality of stacked DRAM dies via any of the first unidirectional interconnects;	See citations for elements 1.1-1.p.2.	
13.r	the control die is configurable to drive the one or more second signals to the second DRAM die via the one or more of the second unidirectional interconnects and is not configurable to receive any signal from any of the plurality of stacked DRAM dies via any of	See citations for elements 1.1-1.p.2.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
	the second unidirectional interconnects;		
13.s	each respective data interconnect of the first data interconnects includes a respective set of through silicon vias (TSVs), the respective set of TSVs including a first subset of TSVs in respective DRAM dies in the first subset of DRAM dies and at least one second TSV in at least one second DRAM die of the second subset of plurality of stacked DRAM dies;	See citations for elements 1b.1, 1.d.3, 1.h.1-1.h.3, 1i.	
13.t	a respective TSV of the first subset of TSVs in a respective DRAM die of the first subset of DRAM dies is in electrical	See citations for elements 1b.1, 1.d.3, 1.h.1-1.h.3, 1i.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 13	Support in '087 Written Description	'060 patent
	communication with a corresponding data port on the respective DRAM die in the first subset of DRAM dies; and		
13.u	each of the at least one second TSV in a corresponding DRAM die of the at least one second DRAM die is not in electrical communication with and is not connected to any data port on the corresponding DRAM die.	See citations for elements 1b.1, 1.d.3, 1.h.1-1.h.3, 1i.	

Claim 14	Support in '087 Written Description
14. The DRAM package of claim 13, wherein the plurality of stacked DRAM dies include at least 8 stacked DRAM dies.	See citations for claim 2

Claim 15	Support in '087 Written Description
15. The DRAM package of claim 14, wherein the plurality of stacked DRAM dies include 16 stacked DRAM dies.	See citations for claim 3.

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U.S. Patent No. 12,308,087 – Written Description Support

Claim 16	Support in '087 Written Description
16. The DRAM package of claim 13, wherein the each of the at least one second TSV in the corresponding DRAM die of the at least one second DRAM die is connected to one or more electrical connections leading from the each of the at least one second TSV, the one or more electrical connections are not configured to provide any electrical communication with memory cells on the corresponding DRAM die.	See citations for claim 8.

Claim 17	Support in '087 Written Description	'060 patent
17.a.1 The DRAM package of claim 13, wherein the signal conduits in the control die include first data conduits coupled to respective ones of the first data interconnects and second data conduits coupled to respective ones of the second data interconnects,	See citations for elements 1.e.2-1.e.4.	
17.a.2 wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals, wherein the control die further includes logic configured to control states of the data conduits in response to	<i>See</i> citations for elements 1.k.1-1.k.2; <i>see also</i>: 19:16-21 (“the read-to-write and write-to-read turn around time”); 21:28-38 (“In some implementations, the control dies 822 include a plurality of data buffers, which may control the timing of data signals to reduce or slow signal degradation. Further, the control dies 822 may include a data path control circuit (not shown) that is configured to control command/address	19:35-40 21:45-54

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U.S. Patent No. 12,308,087 – Written Description Support

Claim 17	Support in '087 Written Description	'060 patent
C/A signals received via the interface, whereby:	time slots and data bus time slots. Controlling the command/address time slots and the data bus time slots enables the control dies 822 to reduce or prevent signal collisions caused by multiple memory packages 820 sharing the data path control lines 816 and the data bus 818”); 19:63-20:7 (“Selective isolation refers generally to a driver corresponding to an array die driving a signal to the array die in response to a corresponding chip select signal while additional drivers corresponding to additional array dies maintain a previous state (e.g. do not drive the signal). For example, assuming that the memory package 300 implements selective isolation, if a chip select signal is received that corresponds to a selection of array die 310b, then the driver 334a will drive a signal along the die interconnect 320a to the array die 310b, and the remaining drivers (e.g., drivers 334b 334f) will maintain their state (e.g., not drive the signal).”).	20:14-24
17.b the first data conduits are enabled to receive and drive the first data signals in response to the first set of C/A signals;	See citations for elements 1.e.2-1.e.4, 17.a.2; <i>see also, e.g.,</i> 19:57-20:8 (“Certain embodiments of the architecture described herein differs from the 3DS-DIMM architecture in that instead of the controller die of the 3DS-DIMM (which provides a secondary address buffer, and a second rank multiplication decoder), certain embodiments described herein use an "ID+" die as a control die 822, which can provide both selective isolation and address pass-through. Selective isolation refers generally to a driver corresponding to an array die driving a signal to the array die in response to a corresponding chip select signal while additional drivers corresponding to additional array dies maintain a previous state (e.g. do not drive the signal).	20:8-24

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Claim 17	Support in '087 Written Description	'060 patent
	For example, assuming that the memory package 300 implements selective isolation, if a chip select signal is received that corresponds to a selection of array die 310b, then the driver 334a will drive a signal along the die interconnect 320a to the array die 310b, and the remaining drivers (e.g., drivers 334b-334f) will maintain their state (e.g., not drive the signal).”); 3:56-62 (“In addition to the below, the following U.S. patents are incorporated in their entirety by reference herein: U.S. Pat. Nos. 7,289,386, 7,286,436, 7,442,050, 7,375,970, 7,254,036, 7,532,537, 7,636,274, 7,630,202, 7,619,893, 7,619,912, 7,811,097. Further, the following U.S. patent applications are incorporated in their entirety by reference herein: U.S. patent application Ser. Nos. 12/422,912, 12/422,853, 12/577,682, 12/629,827, 12/606,136, 12/874,900, 12/422,925, 12/504,131, 12/761,179, and 1; 2/815,339.”); See also, e.g., U.S Pat. App. No. 12/761,179, FIG. 6 and related description.	4:8-16
17.c the second conduits are enabled to receive and drive the second data signals in response to the second set of C/A signals;	See citations for element 17.b.	
17.d each of the first data conduits are placed in a non-driving state after driving the first data signals;	See citations for element 17.b.	
17.e each of the second data conduits are placed in a non-driving state after driving the second data signals; and	See citations for element 17.b.	

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Claim 17	Support in '087 Written Description	'060 patent
17.f data conduit in the first and second data conduits in a non-driving state are not configured to receive or drive any signals.	See citations for element 17.b.	

Claim 18	Support in '087 Written Description
18.a.1 The DRAM package of claim 13, wherein the terminals include a first terminal coupled to a first die interconnect of the first data interconnects via a first conduit of the signal conduits and to a second die interconnect of the second data interconnects via a second conduit of the signal conduits,	See citations for element 1.j
18.a.2 wherein the control die includes logic configurable to control respective states of the first conduit and the second conduit in response to one or more C/A signals received via one or more second terminals of the terminals, wherein the one or more C/A signals do not include any chip select signal.	See citations for elements 1.k.1 and 1.k.2.

Claim 19	Support in '087 Written Description
19. The DRAM package of claim 13, wherein the first data signals include 32 or 64 signals received or output by the DRAM package in parallel and conducted via the first data interconnects in parallel, and wherein the second data signals include 32 or 64 signals received or output by the DRAM package in parallel and subsequently conducted via the second data interconnects in parallel.	See citations for claim 5.

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 20	Support in '087 Written Description	'060 patent
20.a	A dynamic random access memory (DRAM) package, comprising:	See citations for element 1.a.	
20.b.	stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;	See citations for elements 1.b.1 and 1.b.2.	
20.c.1	terminals including command and/or address (C/A) terminals and data terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and receives or outputs data signals via the data terminals in response to the (C/A) signals,	See citations for elements 1.c.1 and 1.c.2.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 20	Support in '087 Written Description	'060 patent
20.c.2	wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in response to a set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;	See citations for elements 1.c.2 and claim 5.	
20.d.1	die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A	See citations for element 1.d.1.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 20	Support in '087 Written Description	'060 patent
	signals and the second set of C/A signals,		
20.d.2	the data interconnects including a first set of data interconnects configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal,	See citations for element 1.d.1.	
20.d.3	wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and	See citations for element 1.d.3.	
20.e.1	a control die coupled between the terminals and the stacked DRAM dies,	See citations for element 1.e.1.	
20.e.2	the control die including conduits	See citations for elements 1.e.2-1.e.4.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 20	Support in '087 Written Description	'060 patent
	coupled to respective ones of the die interconnects;		
20.f.1	wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies,	See citations for elements 1.d.1-1.d.2, 1f-1i.	
20.f.2	the second data interconnect configured to be in electrical	See citations for element 1.f	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 20	Support in '087 Written Description	'060 patent
	communication with a corresponding data port of each of a second plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;		
20.g	wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;	See citations for elements 1.e.2, 1.e.4, 1.j.	
20.h.1	wherein the control die further includes control	See citations for element 1.k.1	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 20	Support in '087 Written Description	'060 patent
	logic configurable to control respective states of the first data conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals,		
20.h.2	wherein the one or more C/A signals do not include any chip select signal;	See citations for element 1.k.2	
20.i	wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;	See citations for elements 1.l-1.p.2.	
20.j	wherein the control die is configured to receive signals from the first unidirectional interconnects and to	See citations for elements 1.l-1.p.2.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 20	Support in '087 Written Description	'060 patent
	drive signals to the second unidirectional interconnects;		
20.k	wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects; and	See citations for elements 1.1-1.p.2.	
20.1.1	wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and	See citations for elements 1.1-1.p.2.	

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	Claim 20	Support in '087 Written Description	'060 patent
20.1.2	wherein, in response to the second set of C/A signals, the control die is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects;	See citations for elements 1.1-1.p.2.	
20.m	wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.	See citations for element 6.c.	

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U.S. Patent No. 12,308,087 – Written Description Support

Claim 21	Support in '087 Written Description
21. The DRAM package of claim 20, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.	See citations for claim 2

Claim 22	Support in '087 Written Description	'060 patent
22.a The DRAM package of claim 20, wherein: the first set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to output the first data signals; and	See citations for elements 1.k.2 and 6.a. See also e.g., Figs. 2-3, 9:30-36, 9:37-10:9, 15:31-51, 16:5-12, 20:1-17, 21:63-22:17, 22:18-42.	Figs. 2-3, 9:39-45, 9:46-10:17, 15:48-67, 16:21-28, 20:19-34, 22:12-33, 22:34-57.
22b. the second set of C/A signals include one or more signals to select one DRAM die among the first plurality of DRAM dies to receive the second data signals.	See citations for elements 6.a and 22.a.	

	Claim 23	Support in '087 Written Description	'060 patent
23.a	A dynamic random access memory (DRAM) package, comprising:	See citations for element 1.a.	
23.b	stacked DRAM dies, each DRAM die of the stacked DRAM dies including data ports and DRAM memory	See citations for elements 1.b.1 and 1.b.2.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 23	Support in '087 Written Description	'060 patent
	cells, wherein the each DRAM die is configurable to transfer data between the data ports and the DRAM memory cells;		
23.c.1	terminals including command and/or address (C/A) terminals, data terminals, and power supply terminals, wherein the DRAM package is configured to receive C/A signals via the C/A terminals and is further configured to receive or output data signals via the data terminals in response to the (C/A) signals,	See citations for elements 1.c.1 and 1.c.2. See also 10:48-59 (“In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits configured to provide a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal to one or more die interconnects. Consequently, in some embodiments, the drivers 334 may be configured to drive signals other than data signals.”).	10:56-67
23.c.2	wherein the DRAM package is configured to output a first n-bit-wide data signal via the data terminals in	See citations for elements 1.c.2, 20.c.2, and claim 5.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 23	Support in '087 Written Description	'060 patent
	response to a first set of C/A signals associated with a memory read operation and to receive a second n-bit-wide data signal via the data terminals in response to a second set of C/A signals associated with a memory write operation, n being 32 or 64;		
23.d.1	die interconnects including C/A interconnects and data interconnects, the C/A interconnects including a first set of C/A interconnects configured to conduct the first set of C/A signals and the second set of C/A signals,	See citations for element 1.d.1.	
23.d.2	the data interconnects including a first set of data interconnects	See citations for element 1.d.2.	

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	Claim 23	Support in '087 Written Description	'060 patent
	configured to conduct the first n-bit-wide data signal and the second n-bit-wide data signal,		
23.d.3	wherein each die interconnect of the die interconnects includes one or more TSVs in one or more DRAM dies in the stacked DRAM dies and is configured to conduct signals to and/or from the one or more DRAM dies through the one or more TSVs; and	See citations for element 1.d.3.	
23.e.1	a control die coupled between the terminals and the stacked DRAM dies,	See citations for element 1.e.1.	
23.e.2	the control die including conduits coupled to respective ones of the die interconnects;	See citations for elements 1.e.2-1.e.4.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 23	Support in '087 Written Description	'060 patent
23.f.1	wherein the data interconnects include at least a first data interconnect and a second data interconnect, the first data interconnect configured to be in electrical communication with a corresponding data port of each of a first plurality of DRAM dies of the stacked DRAM dies and not in electrical communication with any data port of any of a second plurality of DRAM dies of the stacked DRAM dies,	See citations for elements 1.d.1-1.d.2, 1.f.-1.i..	
23.f.2	the second data interconnect configured to be in electrical communication with a corresponding data port of each of a second	See citations for elements 1.d.1-1.d.2, 1.f.-1.i..	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 23	Support in '087 Written Description	'060 patent
	plurality of DRAM dies and not in electrical communication with any data port of any of the first plurality of DRAM dies;		
23.g	wherein the conduits include at least a first data conduit and a second data conduit, the first data conduits being coupled between the first data interconnect and a first data terminal of the data terminals, and the second data conduit being coupled between the second data interconnect and the first data terminal;	See citations for elements 1.e.2, 1.e.4, 1.j.	
23.h.1	wherein the control die further includes control logic configurable to control respective states of the first data	See citations for element 1.k.1	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 23	Support in '087 Written Description	'060 patent
	conduit and the second data conduit in response to one or more C/A signals received via one or more of the C/A terminals,		
23.h.2	wherein the one or more C/A signals do not include any chip select signal;	See citations for element 1.k.2	
23.i	wherein the die interconnects further include first unidirectional interconnects and second unidirectional interconnects;	See citations for elements 1.l-1.p.2.	
23.j	wherein the control die is configured to receive signals from the first unidirectional interconnects and to drive signals to the second unidirectional interconnects;	See citations for elements 1.l-1.p.2.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 23	Support in '087 Written Description	'060 patent
23.k	wherein the control die is not configured to drive any signal to any of the first unidirectional interconnects or to receive any signal from any of the second unidirectional interconnects; and	See citations for elements 1.1-1.p.2.	
23.1.1	wherein, in response to the first set of C/A signals, the control die is configured to receive one or more first signals associated with the memory read operation from one of the one or more DRAM dies via one or more of the first unidirectional interconnects, and	See citations for elements 1.1-1.p.2.	
23.1.2	wherein, in response to the second set of C/A signals, the control die	See citations for elements 1.1-1.p.2.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 23	Support in '087 Written Description	'060 patent
	is configured to drive one or more second signals associated with the memory write operation to the one or more DRAM dies via one or more of the second unidirectional interconnects;		
23.m.1	wherein the power supply interconnects include a first supply voltage interconnect and a second supply voltage interconnect, wherein the first supply voltage interconnect is configured to conduct a supply voltage received at a power supply terminal to each of the first plurality of DRAM dies and not to any of the second plurality of DRAM dies, and	Figs. 2-3 and associated text, 10:10-26 (“The memory package 300 may include a plurality of array dies 310 (e.g., array dies 310a-310h). In the implementation illustrated in FIG.3, the memory package includes eight array dies. However, as stated earlier, the memory package 300 may include more or fewer array dies. Each of the array dies 310 may include one or more ports (not shown) that enable electrical communication between the circuitry of the array dies 310 and one or more die interconnects 320. Each of these die interconnects 320 may be coupled to, or in electrical communication with at least one port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical communication with a port from at least one array die 310, which may be in electrical communication with a different die interconnect 320.”); 10:48-59 (“In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data	Figs. 203 10:18-34 10:56-67

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	Claim 23	Support in '087 Written Description	'060 patent
		signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits configured to provide a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal to one or more die interconnects. Consequently, in some embodiments, the drivers 334 may be configured to drive signals other than data signals.”).	
23.m.2	wherein the second supply voltage interconnect is configured to conduct the supply voltage received at the power supply terminal to each of the second plurality of DRAM dies and not to any of the first plurality of DRAM dies; and	See citations for element 23.m.1.	
23.n	wherein the control die does not include emulation logic that performs emulation causing two or more DRAM dies of the	See citations for element 20.m.1.	

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 23	Support in '087 Written Description	'060 patent
	stacked DRAM dies to emulate a single DRAM die having a larger capacity than each of the two or more DRAM dies.		

	Claim 24	Support in '087 Written Description
24.a	A dynamic random access memory (DRAM) package, comprising:	See citations for element 1.a.
24.b	stacked DRAM dies, wherein each DRAM die of the stacked DRAM dies includes signal ports and DRAM memory cells, and is configurable to receive C/A signals via a first portion of the signal ports and to transfer data between the DRAM memory cells and a second portion of the signal ports;	See citations for elements 1.b.1 and 1.b.2.
24.c	an interface via which the DRAM package receives C/A signals and receives or outputs data signals;	See citations for element 23.c.1
24.d.1	a control die coupled between the interface and the stacked DRAM dies,	See citations for elements 1.e.1 to 1.e.4.
24.d.2	the control die including signal conduits and logic configured to control at least some of the signal conduits; and	See citations for elements 1.e.1 to 1.e.4 and 1.k.1.
24.e	die interconnects, each die interconnect of the die interconnects coupled between at least one corresponding conduit in the control die and one corresponding signal port in each of a subset of the stacked DRAM dies, the	See citations for elements 1.d.1, 13.g, and 1.h.2.

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 24	Support in '087 Written Description
	each die interconnect including through silicon vias (TSVs) in at least some of the stacked DRAM dies;	
24.f	wherein: the signal conduits include first conduits, second conduits, third conduits and fourth conduits;	See citations for elements 1.e.3 and 1.l.
24.g	the die interconnects include first die interconnects coupled to respective ones of the first conduits, second die interconnects coupled to respective ones of the second conduits, third die interconnects coupled to respective ones of the third conduits, and fourth die interconnects coupled to respective ones of the fourth conduits;	See citations for elements 1.e.3 and 1.l.
24.h	each of the first conduits being a unidirectional conduit configurable to drive a signal to a corresponding first die interconnect and not configurable to receive any signal from the corresponding first die interconnect;	See citations for elements 1.e.3. See also, e.g., 9:18-30
24.i	each of the second conduits being a bidirectional conduit configurable to drive a signal to a corresponding one of the second die interconnects or to receive a signal from the corresponding second die interconnect;	See citations for elements 1.e.3, 13.g and 1.l.
24.j	each of the third conduits being a unidirectional conduit configurable to drive a signal received from a corresponding third die interconnect to the interface and not configurable to drive any signal to the corresponding third die interconnect;	See citations for elements 1.e.3 and 1.l.
24.k	each of the fourth conduits being a unidirectional conduit configurable to drive a signal received from the interface to a corresponding fourth die interconnect and not	See citations for element 1.l.

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U.S. Patent No. 12,308,087 – Written Description Support

	Claim 24	Support in '087 Written Description
	configurable to receive any signal from the corresponding fourth die interconnect;	
24.1	the DRAM package is configurable to receive via the interface a first set of C/A signals for a memory read operation, a second set of C/A signals for a memory write operation, a third set of C/A signals for a memory read operation and a fourth set of C/A signals for a memory write operation;	See citations for element 1.c.2
24.m.1	in response to the first set of C/A signals, a first subset of the first conduits is configured to drive the first set of C/A signals to a first subset of the first die interconnects, a first subset of the second conduits is configured to receive first signals associated with the first set of C/A signals via a first subset of the second die interconnects and to drive the first signals to the interface; and	See citations for elements 1.e.2, 1.e.3 and 1.l.
24.m.2	a first subset of the third conduits is configured to receive one or more second signals associated with the first set of C/A signals from a first subset of the third die interconnect and drive the one or more second signals to the interface;	See citations for elements 1.e.2, 1.e.3 and 1.l.
24.n.1	in response to the second set of C/A signals, the first subset of the first conduits is configured to drive the second set of C/A signals to the first subset of the first die interconnects, the first subset of the second conduits is configured to receive third signals associated with the second set of C/A signals from the interface and to drive the third signals to the first subset of the second die interconnects; and	See citations for elements 1.e.2, 1.e.3 and 1.l.

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	Claim 24	Support in '087 Written Description
24.n.2	a first subset of the fourth conduits is configured to receive one or more fourth signals associated with the second set of C/A signals from the interface and to drive the one or more fourth signals to a first subset of the fourth die interconnect;	See citations for elements 1.e.2, 1.e.3 and 1.l.
24.o.1	in response to the third set of C/A signals, a second subset of the first conduits is configured to drive the third set of C/A signals to a second subset of the first die interconnects, a second subset of the second conduits is configured to receive fifth signals associated with the ~~second~~ <u>third</u> ⁴ set of C/A signals via a second subset of the second die interconnects and to drive the fifth signals to the interface; and	See citations for elements 1.e.2, 1.e.3 and 1.l.
24.o.2	a second subset of the third conduits is configured to receive one or more sixth signals associated with the ~~second~~ <u>third</u> set of C/A signals from a second subset of the third die interconnect and drive the one or more sixth signals to the interface;	See citations for elements 1.e.2, 1.e.3 and 1.l.
24.p.1	in response to the fourth set of C/A signals, the second subset of the first conduits is configured to drive the fourth set of C/A signals to the second subset of the first die interconnects, the second subset of the second conduits is configured to receive seventh signals associated with the fourth set of C/A signals from the	See citations for elements 1.e.2, 1.e.3 and 1.l.

⁴ As I explain in my declaration, claim 24 contains a clear drafting error, which would have been clearly evident to a POSITA, and the correction of which would have been apparent from the claim itself as confirmed by the prosecution history.

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	Claim 24	Support in '087 Written Description
	interface and to drive the seventh signals to the second subset of the second die interconnects; and	
24.p.2	a second subset of the fourth conduits is configured to receive one or more eighth signals associated with the ~~second~~ fourth set of C/A signals from the interface and to drive the one or more eight signals to a second subset of the fourth die interconnect;	See citations for elements 1.e.2, 1.e.3 and 1.l.
24.q	each conduit in the first subset of the first, second, third or fourth conduits is distinct from any conduit in the second subset of the first, second, third or fourth conduits;	See citations for elements 1.h.1, 1.h.2, 1.e.2, 1.e.3 and 1.l.
24.r	each die interconnect in the first subset of the first, second, third or fourth die interconnects is distinct from any die interconnect in the second subset of the first, second, third or fourth die interconnects;	See citations for elements 1.h.1 and 1.h.2
24.s.1	the first signals driven by the first subset of the second conduits in response to first set of C/A signals include at least 32 signals driven in parallel;	See citations for claim 5.
24.s.2	the third signals driven by the first subset of the second conduits in response to second set of C/A signals include at least 32 signals driven in parallel;	See citations for claim 5.
24.s.3	the fifth signals driven by the second subset of the second conduits in response to third set of C/A signals include at least 32 signals driven in parallel; and	See citations for claim 5.
24.s.4	the sixth signals driven by the second subset of the second conduits in response to fourth set of C/A signals include at least 32 signals driven in parallel.	See citations for claim 5.

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Claim 25	Support in '087 Written Description
25.a.1 The DRAM package of claim 24, wherein the stacked DRAM dies include a first subset of DRAM dies and a second subset of DRAM dies, wherein each of the first subset of the second die interconnects is configured to be in electrical communication with a corresponding signal port of each of a first subset of DRAM dies and not in electrical communication with any signal port of any of the second subset of DRAM dies,	See citations for elements 1.b.1, 1.b.2, 1.d.2, 1.f
25.a.2 wherein each of the second subset of the second die interconnects is configured to be in electrical communication with a corresponding signal port of each of the second subset of DRAM dies and not in electrical communication with any signal port of any of the first subset of DRAM dies, and wherein:	See citations for element 25.a.1, 6.a
25.b the first set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to output the first signals and the one or more second signals;	See citations for element 6.a.
25.c the second set of C/A signals include one or more signals selecting a DRAM die in the first subset of DRAM dies to receive the third signals and the one or more fourth signals;	See citations for element 6.a.
25.d the third set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to output the fifth signals and the one or more sixth signals;	See citations for element 6.a.
25.e the fourth set of C/A signals include one or more signals selecting a DRAM die in the second subset of DRAM dies to receive the seventh signals and the one or more eighth signals;	See citations for element 6.a.
25.f the interface includes terminals via which the DRAM package receives and/or outputs signals, the terminals including a first terminal coupled to a first die interconnect of the first subset	See citations for elements 1.f and 1.j.

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Claim 25	Support in '087 Written Description
of the second die interconnects via a first conduit of the signal conduits and to a second die interconnect of the second subset of the second die interconnects via a second conduit of the signal conduits; and	
25.g the logic is configurable to control respective states of the first and second conduits in response to one or more C/A signals received via one or more second terminals in the interface, wherein the one or more C/A signals do not include any chip select signal.	See citations for elements 1.k.1 and 1.k.2.

Claim 26	Support in '087 Written Description
26.a.1 The DRAM package of claim 25, wherein the first set of C/A signals and the second set of C/A signals are consecutive sets of C/A signals,	See citations for element 17.a.2.
26.a.2 wherein the control die further includes logic configured to control states of the data conduits in response to C/A signals received via the interface, whereby:	See citations for element 17.a.2.
26.b the first subset of the second conduits is enabled to receive and drive the first signals in response to the first set of C/A signals;	See citations for element 17.b.
26.c the first subset of the second conduits is enabled to receive and drive the third signals in response to the second set of C/A signals; and	See citations for element 17.b.
26.d the first subset of the second conduits is maintained at a non-driving state after driving the first signals and before receiving the third signals;	See citations for element 17.b.

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Claim 26	Support in '087 Written Description
26.e a conduit in the first subset of the second conduits or the second subset of the second conduits in a non-driving state is not configured to receive or drive any signal.	See citations for element 17.b.
Claim 27	Support
27. The DRAM package of claim 24, wherein the stacked DRAM dies include at least 8 stacked DRAM dies.	See citations for claim 2.
Claim 28	Support
28. The DRAM package of claim 27, wherein the stacked DRAM dies include 16 stacked DRAM dies.	See citations for claim 2.