

ARTIFACT SHEET

Enter artifact number below. Artifact number is application number + artifact type code (see list below) + sequential letter (A, B, C ...). the first artifact folder for an artifact type receives the letter A, the second B, etc.. Examples: 59123456PA, 59123456PB, 59123456ZA, 59123456ZB

18822880ZA

Indicate quantity of a single type of artifact received but not scanned. Create individual artifact folder/box and artifact number for each Artifact Type.

☐

CD(s)/DVD(s) containing:
Computer Program Listing
Doc Code: Computer

Number Of Disc(s)

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Artifact Type Code: P

Sequence listing
Doc Code Artifact

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Artifact Type Code: S

Unspecified content
Doc Code: Artifact

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Table
Doc Code: Artifact

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Artifact Type Code: T

☐

Set(s) Color Documents or B/W Photographs
Doc Code: Artifact Artifact Type Code: C

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Confidential Information Disclosure Statement or Other Documents marked Proprietary, Trade Secrets, Subject to Protective Order, Material Submitted under MPEP 724.02, etc.
Doc Code: Artifact Artifact Type Code: X

☐

1

Other documents, including Microfilm(s), Video Tape(s), Model(s), Bound Document(s), Color NPL, Returned Patent Grants, etc.
Description:
Doc Code: Artifact Artifact Type Code: Z

May 12, 2022



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818
139982	7590	03/04/2025	EXAMINER	
Wissing Miller LLP			RODELA, EDUARDO A	
Industrious at Hudson Yards			ART UNIT	
31 Hudson Yards, 11th Floor			PAPER NUMBER	
New York, NY 10001			2893	
			NOTIFICATION DATE	
			DELIVERY MODE	
			03/04/2025	
			ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

APPLICATION NO.	ISSUE DATE	PATENT NO.
18/822,880	04-Mar-2025	12243948

Wissing Miller LLP
Industrious at Hudson Yards
New York, NY 10001

EGRANT NOTIFICATION

Your electronic patent grant (eGrant) is now available, which can be accessed via Patent Center at <https://patentcenter.uspto.gov>

The electronic patent grant is the official patent grant under 35 U.S.C. 153. For more information, please visit <https://www.uspto.gov/electronicgrants>



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	03/04/2025	12243948	309-0015USCIPDIV	5818

139982 7590 02/12/2025
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at <https://patentcenter.uspto.gov/>. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at <https://certifiedcopycenter.uspto.gov/index.html>. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (<https://patentcenter.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PATENT CENTER site <https://patentcenter.uspto.gov> for additional inventors):

Shih-Yuan WANG, Palo Alto, CA;

Shih-Ping WANG, Los Altos, CA;

APPLICANT(s) (Please see PATENT CENTER site <https://patentcenter.uspto.gov> for additional applicants):

W&W Sens Devices, Inc., Los Altos, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

139982 7590 01/15/2025
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

Mary Ellen Finnegan	(Typed or printed name)
/Mary Ellen Finnegan/	(Signature)
January 16, 2025	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818
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TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional	SMALL	\$480	\$0.00	\$0.00	\$480	04/15/2025
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EXAMINER	ART UNIT	CLASS-SUBCLASS
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RODELA, EDUARDO A	2893	136-256000
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1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Wissing Miller LLP

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

W&W Sens Devices, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Los Altos, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 600125

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Ivan S. Kavrukov/

Date January 16, 2025

Typed or printed name Ivan S. Kavrukov

Registration No. 25,161



UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
18/822,880

RECEIPT DATE / TIME
01/16/2025 12:41:33 PM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68771694	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_IssueFeeTransmittal-Final.pdf	1	Issue Fee Payment (PTO-85B)	408 KB
309-0015USCIPDIV_IssueFeeLtr WithStatementOfAllowance-Final.pdf	2	Miscellaneous Incoming Letter	496 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV_IssueFeeTrans	8AAB7CE76E8992CA2444B68989549F47FEFB096D4FBD2333A 75565428216E8025E3A58501335123ED5E3D408C9F2D262375

mittal-Final.pdf

EC51F5F566C2269F8FE01A1E0EE47

309-

0015USCIPDIV_IssueFeeLtrWit
hStatementOfAllowance-
Final.pdf89F60478599B652FEF7112DBFF86AB2A985D4F3CF5F8759AD
1C8FB1899FEEF6E3320B687DCC29A6BE1E5A9222821A71715
D2307997AD2F43811C4EF66566A2EE

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Shih-Yuan WANG et al.
Serial No.: 18/822,880
Examiner: EDUARDO A RODELA
Group Art Unit 2893
Filing Date: 09/03/2024
For: MICROSTRUCTURE ENHANCED ABSORPTION
PHOTOSENSITIVE DEVICES
Conf. No. 5818

31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: January 16, 2025

I hereby certify that this correspondence is being transmitted via
Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan

(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/

(Signature of person signing transmittal)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER ACCOMPANYING ISSUE FEE PAYMENT

Submitted herewith for filing in the U.S. Patent and Trademark Office are the following:

- ☒ Part B – Issue Fee Transmittal;
- ☒ Payment by credit card and Authorization to charge Deposit Account 600125 in payment of any fee deficiencies;

Applicant Comments to Examiner's Statement of Reasons for Allowance

The applicant recognizes that in accordance with M.P.E.P. § 1302.14, the Examiner's reasons for allowance need not set forth all the details as to why the claims are allowed. In the above identified

application, the applicant does not concede that the examiner's stated reasons for allowance are the only reasons for which the claims are allowable. In particular, the applicant does not concede that all the recited limitations are necessary to distinguish the prior art of record or to satisfy the requirements of 35 U.S.C. § 112. In addition, the dependent claims are allowable on their own merits and are allowable based on a sub-combination of the recited features of the dependent claims and their respective base claims. Applicant confirms that the claim amendments were made to expedite the grant of a patent with the allowed claims without prejudice to pursue the subject matter of the original claims in one or more continuing applications.

If there are any questions regarding this submission, the Examiner is encouraged to contact the undersigned via telephone at (917) 945-0121. I hereby authorize the USPTO to communicate any subject matter of this application by electronic mail at [wmdocket@wissingmiller.com]. I understand that a copy of these communications will be made of record in the application file.

By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel. (917) 945-0121

Date: January 16, 2025
Address: (associated with Customer Number: 139982)
31 Hudson Yards, 11th Floor
New York, New York 10001
Attorney's Telephone No.: (917) 945-0121



UNITED STATES
PATENT AND TRADEMARK OFFICE

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #
18/822,880

RECEIPT DATE / TIME
01/16/2025 12:41:33 PM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68771694	AUTHORIZED BY	Ivan Kavrukov
CUSTOMER #	139982	FILING DATE	09/03/2024
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Shih-Yuan WANG

Payment Information

PAYMENT METHOD CARD / 2892	PAYMENT TRANSACTION ID E20251FC42506969	PAYMENT AUTHORIZED BY Mary Ellen Finnegan
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PRE-AUTHORIZED ACCOUNT 600125	PRE-AUTHORIZED CATEGORY 37 CFR 1.21 (Miscellaneous fees and charges)
---	--

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
2501	UTILITY ISSUE FEE	480.00	1	480.00
TOTAL AMOUNT:				\$480.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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New International Application Filed with the USPTO as a Receiving Office

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

139982 7590 01/15/2025
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER

RODELA, EDUARDO A

ART UNIT PAPER NUMBER

2893

DATE MAILED: 01/15/2025

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0.00	\$0.00	\$480	04/15/2025

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

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Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
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Certificate of Mailing or Transmission

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(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

18/822,880 09/03/2024 Shih-Yuan WANG 309-0015USCIPDIV 5818

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional SMALL \$480 \$0.00 \$0.00 \$480 04/15/2025

EXAMINER	ART UNIT	CLASS-SUBCLASS
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RODELA, EDUARDO A 2893 136-256000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818
139982	7590	01/15/2025	EXAMINER	
Wissing Miller LLP Industrious at Hudson Yards 31 Hudson Yards, 11th Floor New York, NY 10001			RODELA, EDUARDO A	
			ART UNIT	PAPER NUMBER
			2893	
DATE MAILED: 01/15/2025				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).

<https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf>

Routine uses of the information in this record may include disclosure to:

- 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
- 2) a federal, state, local, or international agency, in response to its request;
- 3) a contractor of the USPTO having need for the information in order to perform a contract;
- 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
- 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
- 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
- 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
- 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
- 9) the Office of Personnel Management (OPM) for personnel research purposes; and
- 10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Notice of Allowability	Application No. 18/822,880	Applicant(s) WANG et al.	
	Examiner Eduardo A Rodela	Art Unit 2893	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 11/22/2024.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-2 and 4-17. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. ☐ Other _____.
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date. _____.	

	/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893
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DETAILED ACTION

This correspondence is in response to the communications received October 31, 2024. Claims 1, 2 and 4-17 are pending. This office action is being examined under an expedited “special” status due to Applicant’s Age, see “Petition Decision” document dated October 28, 2024 in the file wrapper.

Response to Arguments

Support for the newly amended claim 1 limitation of, “wherein at least some of the holes are elongated along the respective light receiving surfaces”, can be found in ¶ 0249, lines 30-31, “The pillars, holes, **hole(s) in pillar** and pillar(s) in holes **can have any shape, for example a rectangular pillar within a round hole**, can have any mixture thereof to optimize enhancement...” and in Fig. 46 and the associated description in the specification.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority

The first instance of pillars having recesses formed therein can be found in provisional application 61/834,873 (dated June 13, 2013), on pg. 39. Therefore, the instant application’s effective date is **June 13, 2013**.

Applicant's Claim to Figure Comparison

It is noted that this comparison is merely for the benefit of reviewers of this office action during prosecution, to allow for an understanding of the examiner's interpretation of the Applicant's independent claims as compared to disclosed embodiments in Applicant's Figures. No response or comments are necessary from Applicant.

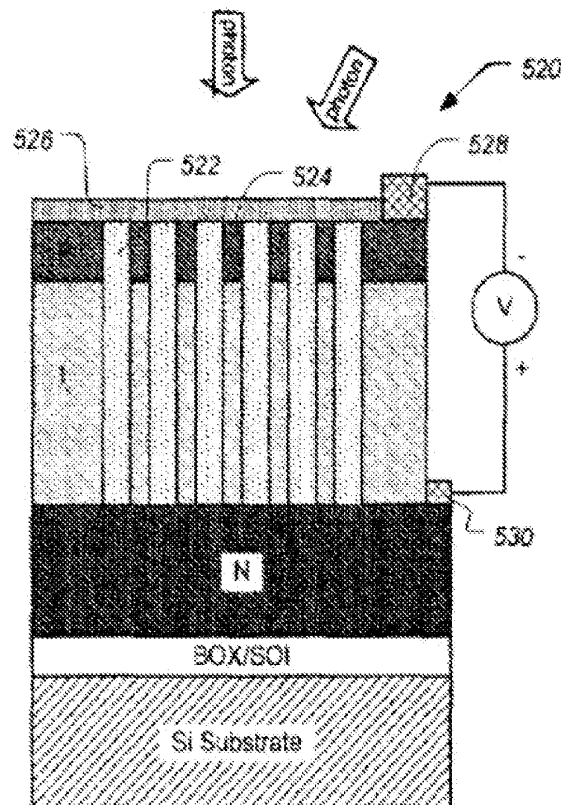


FIG. 5B

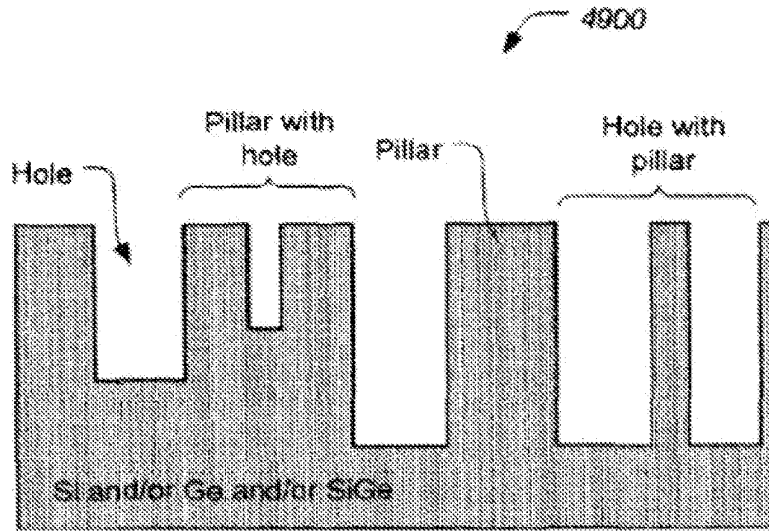


FIG. 49

Regarding claim 1, the Applicant discloses in Figs. 5B and 49, an integrated structure comprising:

an array of pillars ("pillars 524", ¶ 0132) comprising Si, Ge, and/or SiGe alloy semiconductor material, wherein at least some of the pillars are configured to include **photodetectors** and have respective light-receiving surfaces and respective sides ("The PD (and APO) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area)", ¶ 0132);

wherein at least some of the pillars comprise P-doped and N- doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers ("The PD (and APO) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area)", ¶ 0132);

one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other shapes at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;

wherein at least some of the holes are elongated along the respective light receiving surfaces (see Figs. 46 and 49, ¶ 0249)

side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;

a solid dielectric material forming a base dielectric region for the array;

electrical contacts configured to provide electrical pathways coupled electrically to at least some of the **photodetectors**, including for selected reverse-biasing thereof;

wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the **photodetectors** relative to like **photodetectors** lacking said holes.

REASONS FOR ALLOWANCE

Claims 1, 2 and 4-17 are allowed.

The following is an Examiner's statement of reasons for allowance: The pillar shaped photodetector device as recited in the claims of the instant invention fail to be taught by the prior art cited of interest.

Regarding claim 1, the prior art of Yu et al. (US 2011/0309331) discloses in Fig. 5 and Lunev et al. (US 2014/0016660) discloses in Fig. 4B, pillar shaped photodetector devices, but fails to disclose the specific characteristic recited in the claims of the instant invention e.g. the combination of claimed features of an array of pillars with particular material composition and NP junction sensitive to visible and infrared wavelengths, one or more holes that are fabricated as recesses at or under the light receiving surface of at least some of the pillars, wherein at least some of the holes are elongated along the respective light receiving surfaces, side isolation, solid dielectric forming base dielectric, electrical contacts and the presence of the holes increase absorption by a specific amount.

Regarding claim 14, the prior art of Yu et al. (US 2011/0309331) discloses in Figs. 4 and 5, a integrated photoconversion array, but fails to disclose the specific characteristic recited in the claims of the instant invention e.g. the combination of claimed features of an array of pillars comprising Si, Ge, and/or alloyed SiGe semiconductor material, the pillars comprise p-type and n-type doped regions for generating charge carriers, holes in the light receiving surface of at least some of the pillars, the holes are filled with solid dielectric material, side isolation, solid dielectric material forming a base dielectric region for the array, electrical contacts, the presence of holes increases absorption of light by factor of 1.1, and the array is monolithically

integrated with electronic devices for signal processing and transmission, in conjunction with the feature of,

“each of the holes has an elongated shape extending in length over less than the width of the light receiving surface in which the hole is fabricated”.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A Rodela whose telephone number is (571)272-8797. The examiner can normally be reached M-F, 8:30-5:00pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yara B Green can be reached on (571) 270-3035. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC)

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Page 8

at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDUARDO A RODELA/
Primary Examiner, Art Unit 2893

<i>Examiner-Initiated Interview Summary</i>	Application No. 18/822,880	Applicant(s) WANG et al.		
	Examiner Eduardo A Rodela	Art Unit 2893	AIA (First Inventor to File) Status Yes	Page 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	Title	Type
Eduardo A Rodela	Primary Examiner	Telephonic
Ivan Kavrukov	Attorney of Record	

Date of Interview: 19 December 2024

Issues Discussed:

Other

Examiner sought aid in determining support for amendment to claim 1. Support was supplied and the location noted in the current office action.

	/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893
<p>Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04</p> <p>Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing</p>	

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Search Notes 	Application/Control No. 18/822,880	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

CPC - Searched*		
Symbol	Date	Examiner
H01L31/02019; H01L31/022408; H01L31/02327; H01L31/02363; H01L31/028; H01L31/035281; H01L31/105; H01L31/107; H01L31/0236,02363,0352	12/19/2024	EAR

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E search - see history for complete details	12/19/2024	EAR
Applicant & Inventor search	12/19/2024	EAR

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
noted CPC search area	in conjunction with a text limited search	12/19/2024	EAR

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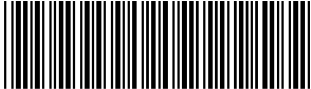
Issue Classification 	Application/Control No. 18/822,880	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

CPC						
Symbol					Type	Version
H01L	/	31	/	035272	F	2013-01-01
G02B	/	6	/	136	I	2013-01-01
H01L	/	23	/	66	I	2013-01-01
H01L	/	31	/	02005	I	2013-01-01
H01L	/	31	/	02016	I	2013-01-01
H01L	/	31	/	02019	I	2013-01-01
H01L	/	31	/	022408	I	2013-01-01
H01L	/	31	/	022475	I	2013-01-01
H01L	/	31	/	02327	I	2013-01-01
H01L	/	31	/	02363	I	2013-01-01
H01L	/	31	/	024	I	2013-01-01
H01L	/	31	/	028	I	2013-01-01
H01L	/	31	/	0284	I	2013-01-01
H01L	/	31	/	0304	I	2013-01-01
H01L	/	31	/	03046	I	2013-01-01
H01L	/	31	/	0312	I	2013-01-01
H01L	/	31	/	035209	I	2013-01-01
H01L	/	31	/	035227	I	2013-01-01
H01L	/	31	/	035281	I	2013-01-01
H01L	/	31	/	036	I	2013-01-01
H01L	/	31	/	054	I	2014-12-01
H01L	/	31	/	0745	I	2013-01-01
H01L	/	31	/	075	I	2013-01-01
H01L	/	31	/	077	I	2013-01-01
H01L	/	31	/	105	I	2013-01-01
H01L	/	31	/	1055	I	2013-01-01
H01L	/	31	/	107	I	2013-01-01
H01L	/	31	/	1075	I	2013-01-01
H01L	/	31	/	1804	I	2013-01-01
H01L	/	31	/	1808	I	2013-01-01
H01L	/	31	/	1812	I	2013-01-01

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	16	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	19 December 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	46, 49

U.S. Patent and Trademark Office

Part of Paper No.: 20241219

Issue Classification 	Application/Control No. 18/822,880	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

CPC						
Symbol					Type	Version
H01L	/	31	/	184	I	2013-01-01
H01L	/	31	/	1844	I	2013-01-01
G02B	/	6	/	122	I	2013-01-01
Y02E	/	10	/	548	A	2013-01-01
G02B	/	2006	/	12097	A	2013-01-01
G02B	/	2006	/	12176	A	2013-01-01
H01L	/	2223	/	6627	A	2013-01-01
Y02E	/	10	/	52	A	2013-01-01

CPC Combination Sets					
Symbol	Type	Set	Ranking	Version	
/		/			

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	16	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	19 December 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	46, 49

U.S. Patent and Trademark Office

Part of Paper No.: 20241219

Issue Classification 	Application/Control No. 18/822,880	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L	/	31	/ 0232
H01L	/	31	/ 0352
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	16	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	19 December 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	46, 49

U.S. Patent and Trademark Office

Part of Paper No.: 20241219

Issue Classification 	Application/Control No. 18/822,880	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	9	10												
2	2	10	11												
	3	11	12												
3	4	12	13												
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5	6	14	15												
6	7	15	16												
7	8	16	17												
8	9														

NONE	Total Claims Allowed:	
(Assistant Examiner)	(Date)	16
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	19 December 2024	O.G. Print Claim(s)
(Primary Examiner)	(Date)	1
		O.G. Print Figure
		46, 49

Bibliographic Data

Application No: 18/822,880

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☐ No ☐ Met After Allowance

Verified and Acknowledged: /EDUARDO A RODELA/

Examiner's Signature

Initials

Title:

MICROSTRUCTURE ENHANCED ABSORPTION
PHOTOSENSITIVE DEVICES

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/03/2024	136	2893	309-0015USCIPDIV
RULE			

APPLICANTS

W&W Sens Devices, Inc., Los Altos, CA, UNITED STATES

INVENTORS

Shih-Yuan WANG, Palo Alto, CA, UNITED STATES

Shih-Ping WANG,

CONTINUING DATA

This application is a DIV of 18385213 10/30/2023 PAT 12087871

18385213 is a CIP of 18113474 02/23/2023

18385213 is a CIP of 17974325 10/26/2022 PAT 11830954

18113474 is a DIV of 17707429 03/29/2022 PAT 11621360

17707429 is a DIV of 17532831 11/22/2021 PAT 11309444

17707429 is a CIP of 17182954 02/23/2021 PAT 11791432

17532831 is a CIP of 17182954 02/23/2021 PAT 11791432

17182954 is a DIV of 16528958 08/01/2019 PAT 11121271

16528958 has PRO of 62874418 07/15/2019

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16528958 has PRO of 62870533 07/03/2019

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16528958 has PRO of 62863852 06/19/2019

16528958 has PRO of 62863231 06/18/2019

16528958 has PRO of 62860115 06/11/2019

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16528958 has PRO of 62846554 05/10/2019
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16528958 has PRO of 62841798 05/01/2019
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16528958 has PRO of 62819604 03/17/2019
16528958 has PRO of 62819669 03/17/2019
16528958 is a CIP of 16296985 03/08/2019 PAT 10468543
16528958 has PRO of 62808949 02/22/2019
16528958 has PRO of 62805850 02/14/2019
16528958 has PRO of 62802718 02/08/2019
16528958 has PRO of 62802171 02/06/2019
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16528958 has PRO of 62797263 01/26/2019
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16528958 has PRO of 62716310 08/08/2018
16528958 has PRO of 62713455 08/01/2018
16528958 is a CIP of PCT/US2018/043289 07/23/2018
16528958 is a CIP of 16042535 07/23/2018 PAT 10700225
16042535 has PRO of 62682909 06/09/2018
16042535 has PRO of 62677609 05/29/2018
16042535 has PRO of 62675130 05/22/2018
16528958 is a CIP of 15979821 05/15/2018 PAT 10624300
16042535 has PRO of 62669194 05/09/2018
16042535 has PRO of 62666005 05/02/2018

16042535 has PRO of 62662217 04/24/2018
16042535 has PRO of 62659072 04/17/2018
16042535 has PRO of 62659067 04/17/2018
16042535 has PRO of 62652830 04/04/2018
16042535 has PRO of 62651087 03/31/2018
16042535 has PRO of 62651053 03/30/2018
16042535 has PRO of 62646871 03/22/2018
16042535 has PRO of 62645810 03/21/2018
16042535 has PRO of 62643010 03/14/2018
16042535 has PRO of 62640522 03/08/2018
16042535 has PRO of 62639920 03/07/2018
16042535 has PRO of 62639472 03/06/2018
16042535 has PRO of 62639356 03/06/2018
16042535 has PRO of 62637945 03/02/2018
16042535 has PRO of 62634692 02/23/2018
16042535 has PRO of 62633514 02/21/2018
16042535 has PRO of 62631630 02/17/2018
16042535 has PRO of 62628764 02/09/2018
16042535 has PRO of 62623971 01/30/2018
16042535 has PRO of 62615314 01/09/2018
16042535 has PRO of 62607860 12/19/2017
16042535 has PRO of 62599246 12/15/2017
16042535 has PRO of 62591072 11/27/2017
16042535 is a CIP of 15797821 10/30/2017 PAT 10446700
16528958 is a CON of 15797821 10/30/2017 PAT 10446700
15979821 has PRO of 62561869 09/22/2017
16042535 has PRO of 62561869 09/22/2017
16042535 has PRO of 62556426 09/10/2017
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15979821 has PRO of 62553844 09/02/2017
16042535 has PRO of 62553844 09/02/2017
15979821 has PRO of 62547728 08/18/2017
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16042535 has PRO of 62542243 08/07/2017
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15979821 has PRO of 62488998 04/24/2017
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15979821 is a CIP of 14947718 11/20/2015 PAT 10622498
16528958 is a CIP of 14947718 11/20/2015 PAT 10622498
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15309922 is a CON of 14943898 11/17/2015 PAT 9530905
15309922 is a 371 of PCT/US2015/061120 11/17/2015
14943898 has PRO of 62232716 09/25/2015
14945003 has PRO of 62232716 09/25/2015
14943898 has PRO of 62213556 09/02/2015
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14943898 has PRO of 62209311 08/24/2015
14945003 has PRO of 62209311 08/24/2015
14943898 has PRO of 62205717 08/15/2015
14945003 has PRO of 62205717 08/15/2015
14943898 has PRO of 62199607 07/31/2015
14945003 has PRO of 62199607 07/31/2015
14945003 has PRO of 62197120 07/27/2015
14943898 has PRO of 62197120 07/27/2015
14945003 has PRO of 62188876 07/06/2015

14943898 has PRO of 62188876 07/06/2015
14943898 has PRO of 62182602 06/21/2015
14945003 has PRO of 62182602 06/21/2015
14943898 has PRO of 62175855 06/15/2015
14945003 has PRO of 62175855 06/15/2015
14945003 has PRO of 62174498 06/11/2015
14943898 has PRO of 62174498 06/11/2015
14943898 has PRO of 62171915 06/05/2015
14945003 has PRO of 62171915 06/05/2015
14943898 has PRO of 62157876 05/06/2015
14945003 has PRO of 62157876 05/06/2015
14943898 has PRO of 62154675 04/29/2015
14945003 has PRO of 62154675 04/29/2015
14945003 has PRO of 62153443 04/27/2015
14943898 has PRO of 62153443 04/27/2015
14943898 has PRO of 62139511 03/27/2015
14945003 has PRO of 62139511 03/27/2015
14945003 has PRO of 62111582 02/03/2015
14943898 has PRO of 62111582 02/03/2015
14945003 has PRO of 62100025 01/05/2015
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PCT/US2018/043289 has PRO of 61905109 11/15/2013
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Doc code: IDS

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Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		18822880	
	Filing Date		2024-09-03	
	First Named Inventor	Shih-Yuan WANG		
	Art Unit	2893		
	Examiner Name	EDUARDO A RODELA		
	Attorney Docket Number	309-0015USCIPDIV		

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
	1	5315147		1994-05-24	Solomon			
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	1	20190001989		2019-01-17	Wang			
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	1	8905043	WO		1989-06-01	Santa Barbara Research Center		☐
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		18822880	
	Filing Date		2024-09-03	
	First Named Inventor	Shih-Yuan WANG		
	Art Unit	2893		
	Examiner Name	EDUARDO A RODELA		
	Attorney Docket Number	309-0015USCIPDIV		

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Examiner Signature	/EDUARDO A RODELA/	Date Considered	12/19/2024
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-12-05
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L40	36	((US-11282970-B1 OR US-9515218-B2 OR US-8384007-B2 OR US-9793439-B2 OR US-9312448-B2 OR US-9196763-B2 OR US-8835905-B2 OR US-8970751-B2 OR US-9362459-B2 OR US-7833425-B2 OR US-8592949-B2 OR US-5759292-A OR US-7276749-B2).did. AND USPT.dbnm.) OR ((US-20130125965-A1 OR US-20130112256-A1 OR US-20120313078-A1 OR US-20120298843-A1 OR US-20120196401-A1 OR US-20120153124-A1 OR US-20110315988-A1 OR US-20110309331-A1 OR US-20110297214-A1 OR US-20110272014-A1 OR US-20110253982-A1 OR US-20110226937-A1 OR US-20110180894-A1 OR US-20110133160-A1 OR US-20110057286-A1 OR US-20140016660-A1 OR US-20130026519-A1 OR US-20140070245-A1 OR US-20140174521-A1 OR US-20130330871-A1 OR US-20110281078-A1 OR US-20100116332-A1 OR US-20140125851-A1).did. AND PGPB.dbnm.)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/17 11:12 AM
L41	36	((US-11282970-B1 OR US-9515218-B2 OR US-8384007-B2 OR US-9793439-B2 OR US-9312448-B2 OR US-9196763-B2 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	OR	ON	ON	2024/12/19 02:38 PM

		US-8835905-B2 OR US-8970751-B2 OR US-9362459-B2 OR US-7833425-B2 OR US-8592949-B2 OR US-5759292-A OR US- 7276749-B2).did. AND USPT.dbnm.) OR ((US- 20130125965-A1 OR US-20130112256-A1 OR US-20120313078- A1 OR US- 20120298843-A1 OR US-20120196401-A1 OR US-20120153124- A1 OR US- 20110315988-A1 OR US-20110309331-A1 OR US-20110297214- A1 OR US- 20110272014-A1 OR US-20110253982-A1 OR US-20110226937- A1 OR US- 20110180894-A1 OR US-20110133160-A1 OR US-20110057286- A1 OR US- 20140016660-A1 OR US-20130026519-A1 OR US-20140070245- A1 OR US- 20140174521-A1 OR US-20130330871-A1 OR US-20110281078- A1 OR US- 20100116332-A1 OR US-20140125851- A1).did. AND PGPB.dbnm.)	HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L42	17	("3620829" "4078945" "4227942" "4640001" "4675466").pn. OR ("5759292").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:17 PM
L43	3	((("W&W") near3 ("SENS") near3 ("DEVICES") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT)	OR	ON	ON	2024/12/19 03:20 PM
L44	863	((("WANG") near3 ("Shih-Yuan")) OR (("WANG") near3 ("Shih-Ping"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2024/12/19 03:20 PM
L45	84115	(H01L31/02019 OR H01L31/022408 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2024/12/19 03:20 PM

		H01L31/02327 OR H01L31/02363 OR H01L31/028 OR H01L31/035281 OR H01L31/105 OR H01L31/107).cpc.	AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L46	2293797	(light OR infrared OR "IR") WITH (pillar OR column\$2 OR cylinder)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L47	30927299	(aperture\$1 OR gaps OR void OR divot)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L48	191	("20050092925" "20050 184354" "20070092192 " "20070190434" "2008 0047604" "2008021874 0" "20080248608" "200 80265449" "200810125 82" "20090188557" "20 090267049" "20100029 067" "20100126548" "2 0100193768" "2010019 7068" "20100221866" "	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2024/12/19 03:20 PM

		20100313941 "20120193676 "20120292676 "20130207222 "20140001528 "20150041965 "20160225631 "4571559 "4637129 "4716449 "5451767 "5457327A "5625636 "5757057 "5886374 "6027956 "6177289 "6667528 "7115971 "7397101 "7495306 "7601597 "7674563 "7772615 "7795064 "7893348 "7898052 "7972934 "8114695 "8129710 "8436370 "8357960 "20050092925 "20050184354 "20060218740 "20070092192 "20080265449 "20090188557 "20100126548 "20100193766 "20100197068 "4637129 "5457327 "7115971 "7397101 "7501597 "7674563 "7795064 "7893346 "8129710").PN.	RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L49	101	("20070190434 "20080047604 "20080248608 "20081012582 "20090267049 "20100029067 "20100221866 "20100313941 "20120193676 "20120292676 "20130207222 "20140001528 "20150041965 "20160225631 "4571559 "4716449 "5451767 "5625636 "5757057 "5886374 "6027956 "6177289 "6667528 "7495306 "7772615 "7898052 "7972934 "8114695 "8357960 "8436370").PN.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L50	1	"20070007621"	(US-PGPUB)	OR	ON	ON	2024/12/19 03:20 PM
L51	31537	H01L31/0236,02363,0352.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO,	OR	ON	ON	2024/12/19 03:20 PM

L52	95452	L5 OR L14	MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L53	1111	(@rtpd<="20131115" OR @rtad<="20131115" OR @pd<="20131115" OR @ad<="20131115") AND L15 AND L7 AND L6	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L54	391	(@rtpd<="20131115" OR @rtad<="20131115" OR @pd<="20131115" OR @ad<="20131115") AND L15 AND L7 AND L6	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L55	508	("1918848" "3903427" "4017332" "4292512" "4316048" "4357415" "4387265" "4394571" "4400221" "4443890" "4513168" "4531055" "4620237" "4678772" "4827335" "4846556" "4857973" "4876586" "4880613" "4896941"	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM

		"4950625" "4971928"				
		"4972244" "4990988"				
		"5071490" "5081049"				
		"5096520" "5124543"				
		"5217911" "5247349"				
		"5272518" "5311047"				
		"5347147" "5362972"				
		"5374841" "5391896"				
		"5401968" "5449626"				
		"5468652" "5602661"				
		"5612780" "5671914"				
		"5696863" "5723945"				
		"5747796" "5767507"				
		"5798535" "5844290"				
		"5853446" "5857053"				
		"5877492" "5880495"				
		"5885881" "5900623"				
		"5943463" "5968528"				
		"6013871" "6033582"				
		"6037243" "6046466"				
		"6074892" "6100551"				
		"6270548" "6301420"				
		"6326649" "6388243"				
		"6388648" "6407439"				
		"6459034" "6463204"				
		"6542231" "6563995"				
		"6566723" "6680216"				
		"6709929" "6720594"				
		"6771314" "6805139"				
		"6812473" "6904187"				
		"6927145" "6960526"				
		"6967120" "6969899"				
		"6987258" "6996147"				
		"7052927" "7064372"				
		"7105428" "7106938"				
		"7109517" "7153720"				
		"7163659" "7192533"				
		"7208783" "7230286"				
		"7235475" "7241434"				
		"7253017" "7254151"				
		"7262400" "7265328"				
		"7272287" "7285812"				
		"7306963" "7307327"				
		"7311889" "7326915"				
		"7330404" "7335962"				
		"7336860" "7339110"				
		"7358583" "7381966"				
		"7388147" "7416911"				
		"7446025" "7462774"				
		"7471428" "7491269"				
		"7507293" "7521322"				
		"7524694" "7582587"				
		"7582857" "7598482"				
		"7622367" "7626685"				
		"7646138" "7646943"				
		"7647695" "7649665"				
		"7655860" "7663202"				
		"7692860" "7704806"				

		"7713779" "7719678" "7719688" "7732769" "7732839" "7736954" "7740824" "7790495" "7872324" "7888155" "7902540" "7948555" "8030729" "8035184" "8049203" "8063450" "8067299" "8067736" "8084728" "8093675" "8118170" "8143658" "8154127" "8193524" "8208776" "8212136" "8212138" "8222705" "8242353" "8269985" "8274039" "8299472" "8330090" "8384007" "8455857" "8471190" "8514411" "8546742" "8748799" "8766272" "8791470" "8810808" "8835831" "8866065" "9000353" "20020003201" "20020020846" "20020021879" "20020071468" "20020104821" "20020109082" "20020117675" "20020130311" "20020172820" "20030003300" "20030006363" "20030077907" "20030089899" "20030103744" "20030132480" "20030160176" "20030189202" "20030227090" "20040011975" "20040021062" "20040026684" "20040058058" "20040065362" "20040075464" "20040095658" "20040109666" "20040114847" "20040118337" "20040118377" "20040122328" "20040124366" "20040155247" "20040156610" "20040160522" "20040180461"				
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		"20040213307"					
		"20040217086"					
		"20040223681"					
		"20040241965"					
		"20040252957"					
		"20040261840"					
		"20050009224"					
		"20050035381"					
		"20050082676"					
		"20050087601"					
		"20050095699"					
		"20050109388"					
		"20050116271"					
		"20050133476"					
		"20050161662"					
		"20050164514"					
		"20050190453"					
		"20050201704"					
		"20050218468"					
		"20050224707"					
		"20050242409"					
		"20050284517"					
		"20060011362"					
		"20060027071"					
		"20060038990"					
		"20060113622"					
		"20060115230"					
		"20060121371"					
		"20060146323"					
		"20060162766"					
		"20060180197"					
		"20060208320"					
		"20060257071"					
		"20060260674"					
		"20060273262"					
		"20060273389"					
		"20060284118"					
		"20070012980"					
		"20070012985"					
		"20070023799"					
		"20070025504"					
		"20070029545"					
		"20070052050"					
		"20070076481"					
		"20070082255"					
		"20070099292"					
		"20070104441"					
		"20070107773"					
		"20070108371"					
		"20070114622"					
		"20070120254"					
		"20070126037"					
		"20070137697"					
		"20070138376"					
		"20070138380"					
		"20070138459"					
		"20070139740"					
		"20070140638"					

		"20070145512"					
		"20070148599"					
		"20070152248"					
		"20070155025"					
		"20070164270"					
		"20070170418"					
		"20070172623"					
		"20070172970"					
		"20070187787"					
		"20070196239"					
		"20070200054"					
		"20070205483"					
		"20070217754"					
		"20070228421"					
		"20070238265"					
		"20070238285"					
		"20070241260"					
		"20070246689"					
		"20070248958"					
		"20070272828"					
		"20070278500"					
		"20070285378"					
		"20070290193"					
		"20070290265"					
		"20080001498"					
		"20080006319"					
		"20080006891"					
		"20080029701"					
		"20080036038"					
		"20080044984"					
		"20080047601"					
		"20080047604"					
		"20080055451"					
		"20080065451"					
		"20080073742"					
		"20080079022"					
		"20080079076"					
		"20080083963"					
		"20080088014"					
		"20080090401"					
		"20080092938"					
		"20080096308"					
		"20080108170"					
		"20080116537"					
		"20080128760"					
		"20080137188"					
		"20080143906"					
		"20080145965"					
		"20080149914"					
		"20080149944"					
		"20080157253"					
		"20080166883"					
		"20080169017"					
		"20080169019"					
		"20080173615"					
		"20080178924"					
		"20080188029"					
		"20080191278"					

		"20080191298"					
		"20080211945"					
		"20080218740"					
		"20080224115"					
		"20080225140"					
		"20080233280"					
		"20080237568"					
		"20080246020"					
		"20080246123"					
		"20080248304"					
		"20080251780"					
		"20080258747"					
		"20080260225"					
		"20080264478"					
		"20080266556"					
		"20080266572"					
		"20080271783"					
		"20080277646"					
		"20080283728"					
		"20080283883"					
		"20080297281"					
		"20080311693"					
		"20080311712"					
		"20090001498"					
		"20090020150"					
		"20090020687"					
		"20090032687"					
		"20090046362"					
		"20090046749"					
		"20090050204"					
		"20090052029"					
		"20090057650"					
		"20090072145"					
		"20090104160"					
		"20090120498"					
		"20090121136"					
		"20090127442"					
		"20090146198"					
		"20090151782"					
		"20090152664"					
		"20090153961"					
		"20090165844"					
		"20090173976"					
		"20090179225"					
		"20090179289"					
		"20090188552"					
		"20090189144"					
		"20090189145"					
		"20090194160"					
		"20090199597"					
		"20090201400"					
		"20090206405"					
		"20090211622"					
		"20090223558"					
		"20090224245"					
		"20090224349"					
		"20090230039"					
		"20090233445"					

		"20090242018"					
		"20090243016"					
		"20090244514"					
		"20090260687"					
		"20090261438"					
		"20090266418"					
		"20090266974"					
		"20090272423"					
		"20090278998"					
		"20090289320"					
		"20090305454"					
		"20100006817"					
		"20100019252"					
		"20100019296"					
		"20100019355"					
		"20100025710"					
		"20100078055"					
		"20100078056"					
		"20100090341"					
		"20100101633"					
		"20100104494"					
		"20100110433"					
		"20100116976"					
		"20100126573"					
		"20100127153"					
		"20100132779"					
		"20100133986"					
		"20100136721"					
		"20100148221"					
		"20100163714"					
		"20100163941"					
		"20100178018"					
		"20100186809"					
		"20100187404"					
		"20100200065"					
		"20100207103"					
		"20100218816"					
		"20100229939"					
		"20100230653"					
		"20100237454"					
		"20100240104"					
		"20100244108"					
		"20100244169"					
		"20100249877"					
		"20100258184"					
		"20100276572"					
		"20100277607"					
		"20100282314"					
		"20100295019"					
		"20100302440"					
		"20100304061"					
		"20100308214"					
		"20100313952"					
		"20100319763"					
		"20100320444"					
		"20110018424"					
		"20110036396"					
		"20110037133"					

		"20110049572"					
		"20110050042"					
		"20110057231"					
		"20110057234"					
		"20110057286"					
		"20110080508"					
		"20110084212"					
		"20110127490"					
		"20110133060"					
		"20110133160"					
		"20110135814"					
		"20110139176"					
		"20110146771"					
		"20110147870"					
		"20110180894"					
		"20110195577"					
		"20110220191"					
		"20110226937"					
		"20110248315"					
		"20110249219"					
		"20110249322"					
		"20110253982"					
		"20110272014"					
		"20110297214"					
		"20110309237"					
		"20110309240"					
		"20110309331"					
		"20110315988"					
		"20110316106"					
		"20120006390"					
		"20120009714"					
		"20120014837"					
		"20120029328"					
		"20120031454"					
		"20120060905"					
		"20120075513"					
		"20120153124"					
		"20120192939"					
		"20120196383"					
		"20120196401"					
		"20120240999"					
		"20120258563"					
		"20120280345"					
		"20120298843"					
		"20120313078"					
		"20120318336"					
		"20120322164"					
		"20130000704"					
		"20130020620"					
		"20130037100"					
		"20130112256"					
		"20130125965"					
		"20130174904"					
		"20130220406"					
		"20130341749"					
		"20140045209"					
		"20140096816"					
		"20140117401"					

L56	1	"20150171272").pn. AND (PGPB USPT USOC).dbnm. "9312448".pn.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L57	386	(@r pd<="20130613" OR @r ad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L15 AND L7 AND L6	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L58	38	("6946682" "7601993" "7923753" "8525227" "8604511" "8735941" "8941146" "8969198" "9660043" "20020142548" "20070187677" "20080173898" "20080217625" "20080258150" "20090035884" "20090127575" "20090212276" "20100059781" "20110018024" "20110143507" "20110198641" "20110233520" "20110233596" "20120049152" "20120119189" "20120235204" "20120248500" "20130026519" "20130320352" "20140016660" "20140264454").pn. OR ("9793439").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L59	36	(@r pd<="20130613" OR @r ad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L21	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L60	1	"20110309331"	(US-PGPUB)	OR	ON	ON	2024/12/19 03:20 PM
L61	1	"20140016660"	(US-PGPUB)	OR	ON	ON	2024/12/19 03:20 PM
L62	214	(texture OR recesses OR divots OR holes) WITH surface WITH	(US-PGPUB)	OR	ON	ON	2024/12/19 03:20 PM

L63	277	(diode) WITH (absorb\$3 OR absorption OR efficiency) WITH light (@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L25	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L64	1996	(textur\$3 OR texturized) WITH ("1" OR "10" OR "20" OR "30 OR "40 OR "50") NEAR (nanometer\$1 OR "nm"))	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L65	245	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L27 AND L14	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L66	76	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L27 AND L14	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L67	594	(textur\$3 OR texturized) WITH surface WITH (increas\$3 NEAR (efficiency OR absorb\$3 OR absorption))	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L68	78	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND L14	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L69	36	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND L14 AND (percent\$3 OR	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM

L70	0	("%) (@rtpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND (L14 SAME (percent\$3 OR "%"))	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L71	0	((@rtpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND (L14 SAME (percent\$3 OR "%"))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L72	7638562	(signal NEAR process\$3) AND (output OR transmission)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L73	244	((@rtpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L14 AND L35	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L74	4526	((@rtpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND (cmos NEAR imager) AND L35	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L75	747	((@rtpd<="20130613" OR	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM

L76	0	@rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND (cmos NEAR imager) AND ((signal NEAR process\$3) AND (output OR transmission)) AND monolithic\$4 (L2 OR L3 OR L15) AND ((integrated NEAR structure)(array)(pillars) (holes)(p-doped)(n- doped)(light NEAR receiving NEAR surfaces)(visible)(infrare d)(wavelengths)(photos ensitive NEAR area)(charge NEAR carriers)(holes)(recesse s)(side NEAR isolation)(base NEAR dielectric)(electrical NEAR contacts)(factor)(increa se)(abosorption)("1.1")). clm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2024/12/19 03:20 PM
L77	36	((US-11282970-B1 OR US-9515218-B2 OR US-8384007-B2 OR US-9793439-B2 OR US-9312448-B2 OR US-9196763-B2 OR US-8835905-B2 OR US-8970751-B2 OR US-9362459-B2 OR US-7833425-B2 OR US-8592949-B2 OR US-5759292-A OR US- 7276749-B2).did. AND USPT.dbnm.) OR ((US- 20130125965-A1 OR US-20130112256-A1 OR US-20120313078- A1 OR US- 20120298843-A1 OR US-20120196401-A1 OR US-20120153124- A1 OR US- 20110315988-A1 OR US-20110309331-A1 OR US-20110297214- A1 OR US- 20110272014-A1 OR US-20110253982-A1 OR US-20110226937- A1 OR US-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM

L78	36	20110180894-A1 OR US-20110133160-A1 OR US-20110057286-A1 OR US- 20140016660-A1 OR US-20130026519-A1 OR US-20140070245-A1 OR US- 20140174521-A1 OR US-20130330871-A1 OR US-20110281078-A1 OR US- 20100116332-A1 OR US-20140125851-A1).did. AND PGPB.dbnm.) ((US-11282970-B1 OR US-9515218-B2 OR US-8384007-B2 OR US-9793439-B2 OR US-9312448-B2 OR US-9196763-B2 OR US-8835905-B2 OR US-8970751-B2 OR US-9362459-B2 OR US-7833425-B2 OR US-8592949-B2 OR US-5759292-A OR US- 7276749-B2).did. AND USPT.dbnm.) OR ((US- 20130125965-A1 OR US-20130112256-A1 OR US-20120313078-A1 OR US- 20120298843-A1 OR US-20120196401-A1 OR US-20120153124-A1 OR US- 20110315988-A1 OR US-20110309331-A1 OR US-20110297214-A1 OR US- 20110272014-A1 OR US-20110253982-A1 OR US-20110226937-A1 OR US- 20110180894-A1 OR US-20110133160-A1 OR US-20110057286-A1 OR US- 20140016660-A1 OR US-20130026519-A1 OR US-20140070245-A1 OR US- 20140174521-A1 OR US-20130330871-A1 OR US-20110281078-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
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L79	17	A1 OR US-20100116332-A1 OR US-20140125851-A1).did. AND PGPB.dbnm.) ("3620829" "4078945" "4227942" "4640001" "4675466").pn. OR ("5759292").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
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PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	0	(L43 OR L44 OR L52) AND ((array)(pillars)(semiconductor)(photodetectors)(light-receiving NEAR surfaces)(P-doped)(N-doped)(regions)(visible)(infrared)(wavelengths)(electrical NEAR charge NEAR carriers)(holes)(recesses)(elongated)(depth)(isolation)(solid NEAR dielectric NEAR material)(absorption)(factor)).clm.	(US-PGPUB; USPAT)	AND	ON	ON	2024/12/19 05:03 PM

Doc code: IDS

PTO/SB/08a (02-18)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 11/30/2020. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

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	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	18822880
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	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-11-18
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV

CONFIRMATION NO. 5818

PUBLICATION NOTICE



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Date Mailed: 12/26/2024

Title:MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Publication No.US-2024-0429332-A1

Publication Date:12/26/2024

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Microstructure-enhanced absorption photosensitive device

Abstract

translated from Japanese

A technique for improving photon absorption in a semiconductor using a microstructure is described. The microstructure is, for example, a hole and effectively increases the absorption of photons. Using a microstructure to improve absorption for silicon photodiodes and silicon avalanche photodiodes can result in a bandwidth exceeding 10 GHz/s for photons having a wavelength of 850 nm with a quantum efficiency of about 90% or more. In short, their thickness dimensions allow them to be conveniently integrated on the same Si chip as CMOS, BiCMOS and other electronics, resulting in packaging advantages, reduced capacitance. Therefore, the speed is further increased. [Solution] [Selection] Figure 1

Classifications

● G02S6/4204 Packages, e.g. shape, construction, internal or external details the coupling comprising intermediate optical elements, e.g. lenses, holograms.

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JP2018508970A

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File History

Series

Other languages: Japanese

Inventor: 三星電子株式会社, 三星電子株式会社, 三星電子株式会社, 三星電子株式会社, 三星電子株式会社

Current Assignee: Samsung Devices Inc

Worldwide applications

2015 US CN US WO JP EP US

Application JP2017526132A events

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Status Active

2035-11-17 Anticipated expiration

Info: Parent citations (70), Cited by (80), Legal events, Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Claims (80)

Hide Dependent
translated from Japanese

in an integrated detector / processor circuit for data communication having both a photodetector with microstructure enhanced light absorption formed in a single semiconductor chip and an electronic processor.

Light sensing having a photon absorption region formed on a semiconductor substrate and configured to absorb photons from an optical source signal modulated for data communication and to provide a corresponding output electrical signal & vessel is provided.

The photon absorption region has a plurality of holes therein, the holes extend toward the substrate, and are configured to simultaneously receive the same source signal in the plurality of holes. And

An electronic processor is also formed on the semiconductor substrate and is operatively associated with the photon absorption region to receive the output electrical signal therefrom and process it into a processed output, thereby receiving the optical source signal and the Forms a single semiconductor chip that outputs processed output.

The photon absorption region and the electronic processor have respective thicknesses that are about the same thickness, and a cathode region and an anode region are operatively associated with the photon absorption region and the reverse bias circuit. The reverse bias circuit is configured to apply a voltage between the cathode region and the anode region such that the cathode region is driven to a more positive voltage than the anode region.

Integrated detector / processor circuit. The integrated detector / processor circuit of claim 1, wherein the photon absorption region has a thickness in the range of 0.5 to 5 micrometers. The electronic processor comprises an application specific integrated circuit (ASIC) having at least one of a complementary metal oxide semiconductor (CMOS) device, a bipolar (BI) device, and a BiCMOS device. The integrated detector / processor circuit of claim 1. 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 40% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 50% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 60% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 40% of the incident source signal at a wavelength between 1400 nm and 1700 nm and provide a corresponding output electrical signal. 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 50% of the incident source signal at a wavelength between 1400 nm and 1700 nm and provide a corresponding output electrical signal. 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 60% of the incident source signal at a wavelength between 1400 nm and 1700 nm and provide a corresponding output electrical signal. The photon absorption region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over a selected wavelength span of at least 20 nm of a source signal wavelength from 800 nm to 900 nm. Integrated detector / processor circuit. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over a wavelength span of at least 20 nm of a source signal wavelength between 1400 nm and 1700 nm. Detector / processor circuit. Each hole has a cross section parallel to the surface of the substrate and the maximum dimension of the cross section is between 400 nm and 2800 nm, and each hole is from the center of the nearest adjacent hole of the plurality of holes. 2. The integrated detector / processor circuit of claim 1 having centers separated by less than 3500 nm. The photodetector further comprises a P layer and an N layer that are highly doped at or above $10^{19} / \text{cm}^3$ and located on the sides of the photon absorption region, and The integrated detector / processor circuit of claim 1

wherein the photon absorption region is lightly doped or intrinsically undoped and at most $10^{16} / \text{cm}^3$. The integrated detector / processor circuit of claim 1, wherein the photodetector comprises an avalanche photodetector. The integrated detector / processor circuit of claim 1 wherein the photon absorption region comprises Si. The integrated detector / processor circuit of claim 1 wherein the photon absorption region comprises Ge. The photodetector has a tapered or stepped hole configured to receive an optical fiber carrying the source signal and maintain one end of the fiber at a selected distance from the photon absorption region. The integrated detector / processor circuit of claim 1. The integrated detector / processor circuit of claim 17 further comprising a lens between the end of the fiber and the photon absorption region. The integration of claim 1, wherein the photodetector has a reflective structure configured to generate multiple reflections of the source signal such that the source signal traverses the photon absorption region multiple times. Detector / processor circuit. The integrated detector / processor circuit of claim 1, wherein the photodetector is configured to receive the source signal from two opposing sides of the photon absorption region. 2. The integrated detector / processor circuit of claim 1, wherein the holes are configured to generate a coupled resonance in the conversion of optical signals to electrical signals in the plurality of groups of holes to improve source signal absorption. In addition, one or more additional photodetectors are formed on the semiconductor substrate and receive respective additional source signals and provide respective output electrical signals corresponding thereto. An absorption region, and one or more additional electronic processors are also formed on the semiconductor substrate and are operatively associated with the respective photon absorption regions of the additional photodetector. The integrated detector / processor circuit of claim 1, wherein said integrated detector / processor circuit is configured to receive and process said respective output electrical signals therefrom. 2. The integrated detector / processor circuit according to claim 1, wherein the plurality of holes improve absorption of photons in a wavelength range including the wavelength of the source signal as compared to the other photodetectors that do not have holes. The integrated detector / processor circuit of claim 1, wherein the electronic processor includes one or more types selected from the group, consisting of a transimpedance amplifier, signal processing electronics, and routing electronics. The integration of claim 1 wherein the capacitance associated with the photodetector is reduced compared to the same photodetector except that its anode and cathode regions are operatively connected to a conventional bond pad. Detector / processor circuit. The photodetector further has a multiplication region and has a gain greater than 2 and detects the source signal in a data bandwidth greater than 10 GHz at a source signal wavelength of 800 to 900 nm. 2. The integrated detector / processor circuit of claim 1, wherein said integrated detector / processor circuit is an avalanche photodiode, in optical / electronic systems.

The photodetector and the active electronic circuit are constructed on the same semiconductor substrate and are operatively associated with each other to form a single integrated circuit chip.

A laser generates an optical source signal that is modulated at a data rate of Gb/s and carries information at the Gb/s rate.

An optical fiber is associated with the laser and receives the optical source signal at its input and carries it to its output.

The photodetector is associated with the output end of the optical fiber and is configured to receive the optical source signal and convert it to an electrical output signal; and the active electronic circuit comprises the photodetector and is configured to receive the output electrical signal and process the electrical output signal to output the processed electrical signal.

system. 28. The system of claim 27, wherein each of the source signal and the electrical output signal is modulated at a rate of at least 5 Gb/s . 28. The system of claim 27, wherein the photodetector and the active electronic circuit have a thickness that is approximately the same size. The photodetector has a photon absorption region including a plurality of holes extending toward the semiconductor substrate, and the plurality of holes are configured to simultaneously receive the same source signal. 28. The system of claim 27. Highly doped P and N layers are located on the sides of the photon absorption region, and the photon absorption region has a thickness in the range of 0.5-5.0 micrometers; and 28. The system of claim 27, wherein the system is intentionally undoped or lightly doped compared to the P and N regions. 28. The system of claim 27, wherein the photodetector is biased to sweep at least one of electrons or holes in a direction along a direction in which the source signal is received by the light detector. 25. The system of claim 27, wherein each of the photodetector and the active electronic circuit is silicon based. 26. The system of claim 27, wherein the light detector is an avalanche light detector in a photodetector having optical absorption with improved microstructure.

A photon absorption region having a thickness between 0.5 and 5 micrometers and configured to absorb photons from a source signal modulated for data communication and provide a corresponding output electrical signal. Provided.

The photon absorption region has a plurality of holes, the plurality of holes extending through at least a portion of the thickness of the photon absorption region and the same source signal in the plurality of holes. And the photon absorption region receives and corresponds to more than 40% of the incident source signal at a wavelength in at least one of the range of 800 nm to 900 nm and 1400 nm to 1700 nm. And an output electric signal to be supplied.

Photodetector. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 40% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 50% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 60% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 40% of the incident source signal at a wavelength between 1400 nm and 1700 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 50% of the incident source signal at a wavelength between 1400 nm and 1700 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 60% of the incident source signal at a wavelength of 1400 nm to 1700 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over a wavelength span of at least 20 nm of a source signal wavelength from 800 nm to 900 nm. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over a wavelength span of at least 20 nm of a source signal wavelength between 1400 nm and 1700 nm. Each hole has a cross section parallel to the top surface of the substrate and has a maximum dimension between 400 nm and 2500 nm, and each hole is adjacent to the nearest of the plurality of holes. 36. The photodetector of claim 35, having a center spaced from the center of the hole by less than 3500 nm. The photodetector further comprises a P layer and an N layer that are highly doped at or beyond $10^{19} / \text{cm}^3$ and located on the sides of the photon absorption region; and photodetector of claim 35, wherein said photon absorbing region in the or intrinsically being lightly doped is at most $10^{16} / \text{cm}^3$ being undoped. 36. The photodetector of claim 35, wherein the photodetector comprises an avalanche photodetector. 36. The photodetector of claim 35, wherein the photon absorption region comprises Si. 36. The photodetector of claim 35, wherein the photon absorption region comprises Ge. The photodetector has a tapered or stepped hole configured to receive an optical fiber carrying the source signal and maintain one end of the fiber at a selected distance from the photon absorption region. 36. The photodetector of claim 35. 50. The photodetector of claim 49, further comprising a lens between the end of the fiber and the photon absorption region. 36. The photodetector of claim 35, wherein the photodetector has a reflective structure configured to generate a plurality of reflections of the source signal such that the source signal traverses the photon absorption region a plurality of times. 36. The light detector of claim 35, wherein the light detector is configured to receive the source signal from two corresponding sides of the photon absorption region, in a photodetector having a microstructure-enhanced light absorption.

Cathode region.

Anode region.

A reverse bias circuit configured to apply a voltage between the cathode region and the anode region such that the cathode region is driven to a more positive voltage than the anode region.

A substrate material having an upper surface, and a photon absorption region that is operatively associated with the cathode region and the anode region and configured to absorb photons from a source signal and is composed of silicon. A plurality of holes, each parallel to the upper substrate surface and having a maximum dimension between 400 nm and 2500 nm, each hole being less than 3500 nm from the center of the adjacent hole closest to the plurality of holes. The photon absorption region having the plurality of holes having centers separated by a distance.

Having a light detector. 54. The photodetector of claim 53, wherein the source signal has a wavelength greater than 800 nm and less than 1000 nm. 54. The photodetector of claim 53, wherein the plurality of holes are arranged in an array that is periodically spaced. 56. The photodetector of claim 55, wherein the periodically spaced array has a hexagonal or square grid pattern. 84. The photodetector of claim 83, wherein the plurality of holes improve photon absorption in a wavelength range that includes the wavelength

of the source signal compared to a photodetector that has no holes but is otherwise identical. 54. The photodetector of claim 53, wherein each of the holes has a predominantly circular cross section that is parallel to the upper substrate surface. 54. The photodetector of claim 53, wherein the cathode region and the anode region are operatively connected to integrated circuit electronics, and the photodetector and integrated circuit electronics are integrated on a single silicon chip. 60. The photodetector of claim 53, wherein the integrated circuit electronics includes one or more types selected from the group consisting of mutual impedance amplifiers, signal processing electronics, and routing electronics. 80. The capacity associated with the photodetector is reduced compared to an otherwise identical photodetector that operatively connects its anode and cathode regions to a conventional bond pad. Light detector. Furthermore, it has a multiplication region formed from silicon, and the photodetector is configured to detect the source signal with a data bandwidth greater than 5 Gb / s at a source signal wavelength of 850 nm. 54. The photodetector of claim 53, wherein the photodetector is an avalanche photodiode having a gain greater than two. 54. The light detection of claim 53, wherein the light detector is configured to detect the source signal with a data bandwidth greater than 2.5 Gb / s at a source signal wavelength of 850 nm with a quantum efficiency of at least 30%. vessel. 54. The light detection of claim 53, wherein the light detector is configured to detect the source signal with a data bandwidth greater than 2.5 Gb / s at a source signal wavelength of 850 nm with a quantum efficiency of at least 50%. vessel. 54. The photodetector of claim 53, wherein the photodetector is configured to detect the source signal with a data bandwidth of 5 Gb / s or greater at a source signal wavelength of 850 nm with a quantum efficiency of at least 30%. 54. The photodetector of claim 53, wherein the photodetector is configured to detect the source signal with a data bandwidth of 5 Gb / s or more at a source signal wavelength of 850 nm with a quantum efficiency of at least 50%. 54. The photodetector of claim 53, wherein the plurality of holes are formed by etching away a portion of silicon.

The light detector is configured such that a portion of the source signal passes through the photon absorption region for the first time, reflects off a surface, and then passes through the light absorption region for the second time. 54. The photodetector of claim 53. And further comprising a substrate, and wherein the cathode region, the absorption region, and the anode region are formed above the substrate and the photodetector is opposite the substrate. 54. The photodetector of claim 53, wherein the photodetector is configured to receive the source signal from a direction facing the surface. In a photodetector having a microstructure-enhanced light absorption,

Cathode region,

Anode region,

A reverse bias circuit configured to apply a voltage between the cathode region and the anode region such that the cathode region is driven to a more positive voltage than the anode region;

A substrate material having an upper surface, and a photon comprising a germanium-based material that is operatively associated with the cathode region and the anode region and configured to absorb photons from a source signal. An absorption region, the germanium-based absorption region including a plurality of holes each having a cross-section parallel to the upper substrate surface and having a maximum dimension between 780 nm and 3000 nm. And each hole has a center having a center that is separated by less than 5000 nm from the center of the nearest neighboring hole of the plurality of holes.

Having a light detector. 71. The germanium-based photon absorption layer is formed above one or more layers of silicon material by at least one of an epitaxial growth and an epitaxial lateral overgrowth process. Photo detector. 72. The photodetector of claim 71, further comprising a Ge buffer layer configured to initiate Ge crystal growth on the top silicon layer. The photodetector of claim 70, wherein the anode region comprises a P-doped germanium layer formed by at least one of an epitaxial growth and an epitaxial lateral overgrowth process. 71. The photodetector of claim 70, wherein the photodetector is an avalanche photodiode and further has a multiplication region made of silicon. 71. The photodetector of claim 70, wherein the source signal has a wavelength greater than 1200 nm and less than 1900 nm. 76. The photodetector of claim 75, wherein the source signal has a wavelength greater than 1400 nm. 72. The light detection of claim 70, wherein the light detector is configured to detect the source signal at a data bandwidth greater than 2 Gb / s at a source signal wavelength of 1550 nm with a quantum efficiency of at least 30%. vessel. 72. The light detection of claim 70, wherein the light detector is configured to detect the source signal in a data bandwidth greater than 2 Gb / s at a source signal wavelength of 1550 nm with a quantum efficiency of at least 50%. vessel. 71. The light detection of claim 70, wherein the light detector is configured to detect the source signal at a data signal bandwidth greater than 5 Gb / s at a source signal wavelength of 1550 nm with a quantum efficiency of at least 30%. vessel. 71. The light detection of claim 70, wherein the light detector is configured to detect the source signal at a data signal bandwidth greater than 5 Gb / s at a source signal wavelength of 1550 nm with a quantum efficiency of at least 50%. vessel.

Description

translated from Japanese

This patent application claims the priority of each of the following provisional applications and is incorporated herein by reference:

US Provisional Application No. 62 / 081,538, filed November 18, 2014 US Provisional Application No. 62 / 081,879, filed December 11, 2014 US Provisional Application No. 62 / 100,025, 2015 Filed on May 5 US provisional application number 62 / 111,582, filed February 3, 2015 US provisional application number 62 / 139,511, filed March 27, 2015 US provisional application number 62 / 153,443, filed April 23, 2015 United States provisional application number 62 / 154,675, filed April 29, 2015 United States provisional application number 62 / 157,876, filed May 6, 2015 United States provisional application number 62 / U.S. Provisional Application No. 62 / 174,498, filed Jun. 11, 2015 U.S. Provisional Application No. 62 / 175,953, 2015 US Provisional Application No. 62 / 182,602, filed June 15, 2015 U.S. Provisional Application No. 62 / 188,076, filed June 23, 2015 U.S. Provisional Application No. 62 / 197, filed July 6, 2015, 120, filed July 27, 2015 US provisional application number 62 / 199,807, filed July 31, 2015 US provisional application number 62 / 205,717, filed August 15, 2015 United States provisional application No. 62 / 209,311, filed August 24, 2015 US provisional application number 62 / 218,556, filed September 2, 2015 US provisional application number 62 / 232,716, September 28, 2015 Applications This patent application is related to the following provisional and non-provisional applications, each of which is incorporated herein by reference.

International Patent Application No. PCT / US14 / 39268, filed May 22, 2014 United States provisional application number 61 / 826,448, filed May 22, 2013 United States provisional application number 61 / 834,873, June 2013 US Provisional Application No. 61 / 843,057, filed July 4, 2013 US Provisional Application No. 61 / 905,109, filed November 15, 2013 US Provisional Application No. 62 / 012,915, Application, June 27, 2014 All provisional and non-provisional patent applications cited above are collectively referred to herein as "commonly assigned and incorporated applications."

This patent specification generally presents an invention primarily related to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure-enhanced absorption characteristics.

Optical fiber communications are widely used in applications such as remote communications and communications within large data centers. Because of the attenuation loss associated with using shorter optical wavelengths, most optical fiber communications use optical wavelengths above 800 nm. A commonly used communication window exists between 800 nm and 1675 nm. The main part of an optical receiver used in an optical fiber communication system is a photodetector, which is usually in the form of a photodiode (PD) or an avalanche photodiode (APD).

A high quality, low noise APD can be composed of silicon. However, although silicon absorbs light in the visible and near infrared ranges, it becomes more transparent at longer optical wavelengths. Silicon PD and APD can be made for optical wavelengths above 800 nm by increasing the thickness of the absorption "I" region of the device. However, in order to obtain adequate quantum efficiency, the thickness of the silicon "I" region is too low for the current and future telecommunications and data center applications where the maximum bandwidth of the device is large. It becomes very big.

Other materials are used to avoid the inherent problems that silicon PD and APD have for longer wavelengths and higher bandwidths. Germanium (Ge) detects infrared up to a wavelength of 1700 nm, but has a relatively high multiplication noise. InGaAs can detect even longer than 1600 nm and has less multiplication noise than Ge, but has much higher multiplication noise than silicon. It is known that InGaAs is most typically used as an absorption region for heterostructure diodes involving InP as a substrate and as a multiplication layer. This material system is compatible with an absorption window of approximately 900-1700 nm. However, both InGaAs devices are relatively expensive and have relatively high multiplication noise when compared to silicon, and are difficult to integrate with Si electronics as a single chip.

information published by major companies in the photodetector business (http://files.zinnovid.com/downloads/FF43A/559d3823777b29943ea-fb06-4179-ac71-64627908460d/Finisar_Investor_Presentation.pdf) shows, on page 18 that the current market for optical communications equipment is 7 billion US it is above the dollar and the compound annual growth rate is 12%. The photodiode (PD) used for the 850 nm wavelength uses a GaAs material, and for the 1550 nm wavelength, the photodiode is based on an InP material, which is expensive and Si-based electronics. It is difficult to integrate with. Thus, there is a long market and there is a long-standing need for the development of better equipment. To date, neither a photodiode based on a Si material for 850 nm nor an avalanche photodiode (APD) exists, and the data rate is 5 Gb / s or more in the top or bottom irradiation type. As is known, there are no commercially available photodiodes or avalanche photodiodes based on Ge on Si (Ge on Si) materials for 1550 nm. However, the effort to develop better devices for such a large market was not lacking. For example, a proposal has been made for a resonant photodiode manufactured in Si material (Resonant Cavity Enhanced High-Speed Si Photodiodes Shown by Epitaxial Lateral Overgrowth) Schaub et al., IEEE Photonics Technology Letters, Vol. 11, No. 12, December 1999, but it has not become recognized in the market. Other types of high speed photodiodes in waveguide form have been proposed, for example, a reference 40 GHz Si / Ge uni-travelling carrier waveguide photodiode (Ref. 40 GHz Si / Ge uni-travelling carrier waveguide photodiode), Piel et al., DOI 10.1109 / JLT. 2014.2310780, Journal of Lightwave Technology Monolithic Ge / Si Avalanche Photodiodes, Kang et al., 978-1-4244-4403-6 / 09 / \$ 25.00 Copyright 2009 IEEE High-speed Ge monolithically integrated with large cross-section silicon-on-insulator waveguide, Feng et al. Applied Physics Letters 95, 261105 (2009), doi: 10.1063 / 1.3279129; in which case light is coupled into the optical waveguide from the edge and the absorption length is Ge at 1550 nm, 100um or more to compensate for weak absorption coefficient It is possible to in these previously proposed waveguide photodiode structures, light propagates along the length of the waveguide and the PIN waveguide is such that the direction of light propagation and the direction of the electric field are predominantly perpendicular. An electric field is applied across Since light travels about 1000 times faster than the electron / hole saturation rate in Si, the waveguide PD should be, for example, 200 microns long and the "I" in the PIN should be, for example, 2 microns. And a bandwidth exceeding 10 Gb / s can be achieved. Such end coupling of light is costly in packaging compared to surface illumination as described in this patent specification, where the waveguide cross-sectional dimensions are typically a few microns. In contrast to the case of a known surface-illuminated photodiode or avalanche photodiode, it is several tens of microns. Known waveguide PD / APDs are often only single-mode optics, whereas surface-illuminated PD / APDs described in this patent are both single-mode and multimode optics. It is possible to use. In addition, known waveguide photodiodes are difficult to test at the wafer level, whereas the surface-illuminated photodiodes described in this patent specification can be easily tested at the wafer level. Known waveguide / avalanche photodiodes are mostly used in special photonic circuits and are not widely available on the market. Top / bottom-illuminated Si and Ge-on-Si PD / APD that can be integrated with Si are commercially available with data rates of 5 Gb / s or higher at wavelengths of 850 nm and 1550 nm. That is ignorant. In contrast, photodiodes on Si-based materials as described in this patent specification can be monolithically integrated with integrated electronics on a single Si chip, in which case significantly reducing the cost of packaging. Furthermore, the microstructured PD / APD described in this patent specification at a nominal wavelength of 850 nm can be predominantly for short distances, for example less than 1 meter, and in some cases Optical data transmission distances can be less than 10 meters, and in some cases less than 100 meters, and in some cases less than 1000 meters. The electric field in the microstructured PD / APD direction of the incident optical beam and in the "I" region of the PIN or NIP structure is predominantly collinear and / or approximately collinear. This patent specification is expected to make such devices possible and convert the current data center between blades and / or almost all to optical data transmission within a blade, and that significantly increases data transmission bandwidth capability and significantly reduces power consumption.

The spirit and scope of the claims are not limited to embodiments that solve any particular disadvantages or that operate only in environments such as those described above. Rather, this background is provided to illustrate one exemplary technology area in which some embodiments described herein may be implemented.

Resonant Cavity Enhanced High-Speed Si Photodiodes Shown by Epitaxial Lateral Overgrowth, Schaub et al., IEEE Photonics Technology Letters, Vol. 12, December 1999 Reference 40 GHz Si / Ge single traveling carrier waveguide photodiode (Ref. 40 GHz Si / Ge uni-travelling carrier waveguide photodiode), Piel et al., DOI 10.1109 / JLT. 2014.2310780, Journal of Lightwave Technology Monolithic Ge / Si Avalanche Photodiodes, Kang et al., 978-1-4244-4403-6 / 09 / \$ 25.00 Copyright 2009 IEEE High-speed Ge photolithographic monolithically integrated with large cross-section silicon-on-insulator waveguide, Feng et al. Applied Physics Letters 95, 261105 (2009) doi: 10.1063 / 1.3279129

According to some embodiments, an integrated detector / processor circuit for data communication includes a photodetector with microstructure enhanced optical absorption, and an electronic processor formed on a single semiconductor chip. Here:

The single chip includes a photon absorption region configured to absorb photons from an optical source signal modulated for data communication and to provide a corresponding output electrical signal. The photon absorption region is a plurality of holes extending therethrough toward the substrate, wherein the same source signal is transmitted through the plurality of holes. The plurality of holes configured to receive simultaneously, and an electronic processor is also formed on the semiconductor substrate and is operatively associated with the photon absorption region to receive the output electrical signal. Forming a single semiconductor chip that receives the optical source signal and outputs the processed output, thereby processing the photon absorption region and the electron The processors have respective thicknesses of the same magnitude, and a cathode region and an anode region are operatively associated with the photon absorption region and a reverse bias circuit, the reverse bias circuit being in the cathode region is configured to apply a voltage between the cathode region and the anode region so as to be driven to a more positive voltage than the anode region.

The thickness of the photon absorption region is preferably in the range of 0.5 to 5 μm. The electronic processor can be an application specific integrated circuit (ASIC) having at least one of complementary metal oxide semiconductor (CMOS) devices, bipolar (B) devices, and BiCMOS devices. In turn, The photon absorption region is configured to absorb more than 40%, 50%, or 60% of the incident source signal at a wavelength of 800 nm to 900 nm, or 1400 nm to 1700 nm, and provide a corresponding output electrical signal. It is possible. The photon absorption region may be configured to provide the incident source signal at an absorption percentage that varies by less than 20% over a selected wavelength range of at least 20 nm of a source signal wavelength of 800 nm to 900 nm, or 1400 nm to 1700 nm. Is possible.

Each hole has a maximum dimension between 400 nm and 3500 nm and can have a cross section parallel to the surface of the substrate, and each hole is the closest of the plurality of holes. It is possible to have a center that is separated from the center of the adjacent hole by less than 3500 nm. The photodetector preferably further comprises a P layer and an N layer that are highly doped at or beyond $10^{18} / \text{cm}^3$ and located on the sides of the photon absorption region. And the photon absorption region is preferably lightly doped or intentionally undoped and at most $10^{16} / \text{cm}^3$. The photodetector can include an avalanche photodetector and the photon absorption region can include at least one of Si and Ge. The photodetector may have a tapered or stepped hole configured to receive an optical fiber carrying the source signal and to maintain an end of the fiber at a selected distance from the photon absorption region. Is possible. A lens can be included between the end of the fiber and the photon absorption region. The photodetector may further include a reflective structure configured to generate multiple reflections of the source signal, thereby causing the source signal to traverse the photon absorption region multiple times. The light detector can be configured to receive the source signal from two opposite sides of the photon absorption region, and the holes are adapted to convert light into electrical signals in groups of the holes. It is possible to generate a coupled resonance, thereby improving the source signal absorption.

One or more additional photodetectors can be formed on the semiconductor substrate, each receiving a respective additional source signal and providing a corresponding respective output electrical signal. A photon absorption region, and one or more additional electronic processors are formed on the semiconductor substrate and the additional output electrical signals are received and processed therefrom. It can also be operatively associated with each photon absorption region of the photodetector. The plurality of holes have no holes in a plurality of wavelength ranges including the wavelength of the source signal, but the others can be configured to improve photon absorption as compared with the same photodetector. The electronic processor may include one or more types selected from the group consisting of mutual impedance amplifiers, signal processing electronics, and routing electronics. The capacitance associated with the photodetector is reduced compared to the

same photodetector, except that the anode and cathode regions are operatively connected to a conventional bond pad. The photodetector can further have a multiplication region, which is an avalanche photodiode that detects the source signal with a data bandwidth greater than 10 gigabits / s at a source signal wavelength of 800-900 nm. And has a gain greater than 2.

In some embodiments, in an optical / electronic system, a photodetector and active electronic circuitry are provided that are built on the same semiconductor substrate and are operatively associated with each other. A laser is provided that forms a single integrated circuit chip and is modulated at the Gb / s rate of data to generate the optical source signal carrying information at the Gb / s rate; and An optical fiber is provided in association with the laser to receive the optical source signal at its input and send it to its output, in which case the photodetector detects the optical source signal. Associated with the output end of the optical fiber for receiving and configured to convert it to an electrical output signal, and the active electronic circuit comprises: There is a light detector to process an electrical output signal being associated with and configured to output an electrical signal of the processed to receive the output electrical signal. Each of the source signal and the electrical output signal can be modulated at a rate of at least 5 Gb / s. The photodetector and the active electronic circuit can have a similar thickness. The photodetector can have a photon absorption region that includes a plurality of holes extending toward the semiconductor substrate, in which case the plurality of holes receive the same source signal. It is supposed to be received at the same time. Highly doped P and N layers can be located on the sides of the photon absorption region, and the photon absorption region can have a thickness in the range of 0.1 to 5.0 μm . Yes, and preferably not intentionally doped or lightly doped compared to the P and N regions. The photodetector can be biased to sweep electrons or holes in a direction along the direction in which the source signal is received by the photodetector. Each of the photodetector and the active electronic circuit may be silicon based. The photodetector can be an avalanche photodetector.

In some embodiments, the photodetector with microstructure enhanced light absorption preferably has a thickness between 0.5 μm and 5 μm and is modulated for data communications. A photon absorption region configured to absorb a photon from a source signal and supply an output electrical signal corresponding to the photon absorption region, wherein the photon absorption region passes through at least part of the thickness of the photon absorption region. A plurality of extending holes, wherein the plurality of holes are configured to simultaneously receive the same source signal in the plurality of holes; and the photon absorption region is 800 nm to Absorbs more than 40% of the incident source signal at a wavelength in 980 nm and at least one of the ranges 1400 nm to 1700 nm and provides a corresponding output electrical signal. It is supposed to be a form to pay. The photon absorption region can be configured to absorb incident source signals at an absorption percentage that varies by less than 20% over a wavelength range of at least 20 nm of a source signal wavelength of 800 nm to 900 nm or 1400 nm to 1700 nm.

Each hole preferably has a cross section parallel to the top surface of the substrate having a maximum dimension between 400 nm and 2500 nm, and each hole is preferably within the plurality of holes. Has a center that is separated by less than 3500 nm from the center of the adjacent hole. The photodetector further comprises a P layer and an N layer, which are preferably highly doped at or above $10^{19} / \text{cm}^3$ and in the photon absorption region. Located on the side and the photon absorption region is preferably intentionally doped or lightly doped at most $10^{18} / \text{cm}^3$. The photodetector can comprise an avalanche photodetector. The photon absorption region can comprise Si or Ge. The photodetector has a tapered or stepped hole configured to receive an optical fiber carrying the source signal and to maintain an end of the fiber at a selected distance from the photon absorption region. A lens can be included between the end of the fiber and the photon absorption region. The light detector may have a reflective structure configured to generate multiple reflections of the source signal, thereby traversing the photon absorption region multiple times with the source signal. The light detector may be configured to receive the source signal from two opposite sides of the photon absorption region.

In some embodiments, a photodetector with microstructure enhanced light absorption includes a cathode region, an anode region, and the cathode region such that the cathode region is driven to a more positive voltage than the anode region. A reverse bias circuit configured to apply a voltage between the anode region, a substrate material having an upper surface, and a photon from a source signal that is operatively associated with the cathode region and the anode region. A photon absorption region composed of silicon, the silicon absorption region being parallel to the upper substrate surface, each having a maximum dimension between 400 nm and 2500 nm. A plurality of holes having a uniform cross section, and each hole is located 35 from the center of the nearest adjacent hole of the plurality of holes. By less than 60m are spaced apart. The source signal can have a wavelength greater than 800 nm and less than 1000 nm. The plurality of holes can be arranged in a periodically spaced array that can have a hexagonal or square grid pattern. The plurality of holes improve photon absorption compared to those without holes, but the others are the same photodetectors in the wavelength range including the wavelength of the source signal. Each of the holes may have a predominantly circular cross section parallel to the upper substrate surface. The cathode region and anode region can be operatively connected to integrated circuit electronics, and the photodetector and integrated circuit electronics can be integrated on a single silicon chip, in which case the The integrated circuit electronics can include one or more types selected from the group consisting of mutual impedance amplifiers, signal processing electronics, and routing electronics. The capacitance associated with the photodetector can be reduced compared to the same photodetector, except that its anode and cathode regions are operatively connected to a conventional bond pad. The photodetector may further have a multiplication region formed from silicon, in which case the photodetector has a gain greater than 2 at a source signal wavelength of 850 nm. An avalanche photodiode configured to detect the source signal in a data bandwidth greater than 5 Gb / s. The photodetector may be configured to detect the source signal at a data bandwidth of 2.5 Gb / s or higher at a source signal wavelength of 850 nm with a quantum efficiency of at least 30% or 50%, or 5 Gb / s or higher. Is possible. The plurality of holes can be formed by etching away a part of silicon. The photodetector can be configured such that a portion of the source signal first passes through the photon absorption region, reflects off the surface, and then passes again through the photon absorption region. The photodetector can further include a substrate, in which case the cathode and anode regions are formed above the substrate and the photodetector is on the opposite side of the substrate. The source signal is received from the direction facing the side of the photodetector.

In some embodiments, a photodetector with microstructure enhanced light absorption includes a cathode region, an anode region, and the cathode region such that the cathode region is driven to a more positive voltage than the anode region. A reverse bias circuit configured to apply a voltage between the cathode region and the anode region, a substrate material having an upper surface, and photons from the source signal that are operatively associated with the cathode region and the anode region. And a photon absorption region composed of a germanium-based material, each of the germanium-based absorption regions having a maximum dimension between 750 nm and 3000 nm. A plurality of holes having a cross-section parallel to the surface of the upper substrate and each hole being a plurality of holes. Nearest neighbor of the inner has a center which is spaced from the center of the hole by less than 5000 nm. The germanium-based photon absorption layer may be formed on one or more layers of silicon material by at least one of an epitaxial growth and an epitaxial lateral overgrowth process. Is possible. The photodetector may further include a Ge buffer layer configured to initiate Ge crystal growth on the top silicon layer. The anode region of the photodetector can have a P-doped germanium layer formed by at least one of an epitaxial growth and an epitaxial lateral overgrowth process. The photodetector can be an avalanche photodiode and can further have a multiplication region formed from silicon. The source signal can have a wavelength greater than 1200 nm and less than 1900 nm, or greater than 1400 nm. The photodetector can be configured to detect the source signal in a data bandwidth greater than 2 Gb / s or 5 Gb / s at a source signal wavelength of 1550 nm with a quantum efficiency of at least 30% or 50%. Is there.

As used in this document, grammatical conjunctions such as "and", "or", and "and / or" are all examples of their conjunction, it is intended to represent that one or more of the objects, subjects may occur or exist. Thus, as used in this document, the term "or" in all passages means "inclusive or" rather than "exclusive or". Represents.

As used herein, the term "single hole" or "multiple holes" refers to an opening into or through a substrate or substances. Likewise, in general, the openings can have any shape and cross section including circular, elliptical, polygonal, and random shapes.

To further clarify the above and other advantages and features of the subject matter of this patent specification, specific examples of embodiments thereof are illustrated in the accompanying drawings. It should be understood that these drawings are merely illustrative of the embodiments and are not to be considered as limiting.

This is understood from the relationship of $A = A_0 e^{-\alpha L}$, where A is the attenuation amplitude of the incident photon flux A_0 , α is an absorption coefficient, and L is a path length in which absorption is performed. Therefore, instead of making L 100 times longer, it is possible to define the effective α so that the effective α is 100 times larger than an unimproved absorption coefficient such as a bulk absorption coefficient. For example, the resonance / coupled resonance / scattering / near field effect of the microstructure provides 100 times longer path length uniformity, in which case the resonance / scattering / near field microstructure is only 1 micron long. Assent. A simpler description of this is that the photons in the resonant / coupled resonant structure make 50 reciprocations before reaching the value of $1/e$ of its original amplitude, and therefore its uniform linear length is 100 times the length of. For convenience of explanation, resonance / coupled resonance / linear and nonlinear field enhancement / scattering / near-field effects will be collectively referred to herein as "resonant", which means resonance, coupled resonance, slow wave, etc. can include scattering, near field, plasmon, nonlinear and linear optical field effects.

As used herein, the terms "microstructure" and "microstructure type" refer to dimensions and / or dimensions in which at least one dimension is a micron scale, a submicron scale, and / or a subwavelength scale and / or a wavelength scale. It means various shapes of pillars, voids, holes and mesas.

According to some embodiments, the present technique for improving effective absorption is based on any combination of III-V materials, such as silicon, germanium, InP, GaAs, GaN, GaN, InGaAs, and III-V materials. It is possible to apply to various substances including As used herein, the term "substance group" of III-V materials is lattice matched or nearly lattice matched (within a few percent) to GaAs, InP, GaN, InSb semiconductors. Defined as any substance. For example, the InP material group can include InGaAs, InGaAsP, InAlAs, and InAs. According to some embodiments, in the case of microstructures, there is a thin buffer layer of selective area growth (SAG), epitaxial lateral overgrowth (ELO), Ge or InGaAs or other III-V material in silicon microstructures. Re-growth, such as with or without epitaxial growth (EG), can be performed without the deleterious effects of lattice mismatch. This is because the size of the lattice mismatch material footprint on silicon is small (approximately a few microns to a submicron). This allows Ge and other III-V materials to be integrated with silicon without using conventional buffer layers (such as amorphous Si in the case of Ge-on-Si growth). The heterogeneous integration of multiple materials is a combination of homo- or heterostructures, crystalline and microcrystalline and amorphous semiconductors, conductors such as carbon, graphene, insulators, dielectrics, solids, gases, liquids such as glass, or it can be a polymer that can be semiconducting. Ge and III-V materials can also be grown on Si with or without buffer layers using SOG, ELO, EG methods that can cover areas that cover the wafer scale from areas larger than a micron scale to it.

According to some embodiments, buried oxide (BOX), silicon-on-insulator (SOI), silicon-on-sapphire (SOS), amorphous semiconductor, etc. are used to reduce the effective refractive index. Low index materials such as low density semiconductors, nanowire semiconductors, voids and holes are used. Refractive index is an intrinsic property of a substance. However, according to some embodiments, structures such as voids, voids, and / or holes (which can be filled or partially filled with a low refractive index material) have dimensions on the order of optical wavelengths. In some cases, the optical electromagnetic field will see an average refractive index consisting of the material refractive index and the structure (which can be filled or partially filled with a low refractive index material). This average is referred to herein as the effective refractive index. According to some embodiments, it is not necessary to use a low index or low effective index material in the microstructures.

According to some embodiments, techniques for improving effective absorption can be applied to various materials, including silicon, germanium, III-V materials, such as InP, GaAs, GaN, InGaAs, and any combination of III-V materials. It is possible to apply.

Due to the microstructure, capacitance can also be expressed in terms of effective capacitance: (1) the dielectric constant of one semiconductor and (2) the semiconductor, dielectric, gas, vacuum, partial vacuum, glass or a parallel capacitance with the dielectric constant of another substance that can be a liquid, such as a polymer (polyimide, mylar, or other organic compound). The effective capacity of the device is a combination of the capacities of parallel capacitors, which can be two or more. According to some embodiments, the advantage of using a microstructure is that its effective capacity can be significantly reduced from that of a uniform material such as a semiconductor. The RC time (resistive capacity) is one of basic times for determining the bandwidth of the photodiode and the avalanche photodiode. The lower capacity allows the device to have a larger area while maintaining a reasonably high data rate bandwidth and / or the fundamental time to determine the bandwidth of the PD / APD. It is possible to increase the data rate bandwidth by reducing the thickness of the device in order to reduce the transit time of holes and / or.

According to some embodiments, the photosensor may be a photodiode (PD), avalanche photodiode (APD), photovoltaic cell (PV) or solar cell, or any optoelectronic device that converts photons to electrons. In possible. According to some embodiments, emitters or emitters that convert electrons / holes into photons, such as lasers and light emitting diodes, can also be realized using microstructures.

According to some embodiments, the improved absorption results in APD / PD, (1) weak bulk absorption coefficient, eg, QE (quantum efficiency) is greater than 30% or greater than 50% and data bandwidth Expands the sensitivity of APD / PD to photons with energy (or wavelength) close to the material bandgap when A is greater than 3 Gb / s and about 1000 1 / cm or less, and (2) shorter absorption Operate with higher data rate bandwidth (eg, greater than 10 Gb / s) due to longer and shorter transit times, (3) increase quantum efficiency with improved absorption, and (4) for avalanche photodiodes it can be made of silicon with low excess noise and good multiplication characteristics, and (5) compatible with Si photonics and CMOS processes. That, According to some embodiments, the PD / APD induces signal processing, signal amplification, memory, CPU, electrical transmitter, optical waveguide, integrated optics, and other ICs for specific applications, etc. It is possible to integrate with an ASIC (Application Specific Integrated Circuit). This is beneficial for mass production using CMOS foundries, in addition, surface (or bottom) illuminated PD / APD integrated with or without electronics can be tested with wafer level probing and can handle both single mode and multimode. It is. A single optical and electrical chip bypasses the need for a ceramic multichip carrier and significantly reduces assembly and packaging costs. Silicon benches can also be used in connection with optical alignment to optical components such as lenses, fibers, etc. as needed.

According to some embodiments, silicon is used for avalanche gain. Silicon has much lower noise than avalanche photodiodes. By integrating Ge with silicon, absorption occurs in the Ge material and electronic gain occurs in the silicon. Depending on the optical wavelength, eg, below 1100 nm, silicon can be used for both absorption and electronic gain, as well as the use of microstructures.

According to some embodiments, the absorption of photons in the semiconductor is improved using a microstructure. The microstructure provides greater absorption of photons for resonance, coupled resonance, field enhancement, near field and subwavelength effects, scattering, plasmons, linear and nonlinear optical fields, photonic crystals, and given physical length Absorption modes in high contrast gratings in the near-field region that can both effectively increase the effective absorption length and / or improve the absorption coefficient to the effective coefficient, both linear and non-linear effects. Alternatively, it is possible to have an effect such as a loss mode.

According to some embodiments, the microstructure used for absorption enhancement for silicon photodiodes and / or avalanche photodiodes has a quantum efficiency of approximately due to increased length and / or modulus. > 50%, in some cases (QE> 70%, wavelength around 850 nm (which is the preferred wavelength for current data communications) and bandwidth 10 Gb / s (or equivalently, digital coding Depending on the format, there may be silicon PDs and APDs that exceed approximately 6.75 GHz).

Silicon optical detectors are very robust due to the maturity of materials and processing techniques, and their surfaces are free of dangling bonds that can generate surface states and carrier recombination centers. It can be easily passivated, and for APD applications, the ionization ratio between holes and electrons (k coefficient). Silicon has a lower k coefficient than any III-V material) And low noise, and such detectors are CMOS compatible for integration with signal processing electronics and Si photonics.

According to some embodiments, the light generated carrier is P for high modulation bandwidth (over 10 Gb / s bandwidth) and high quantum efficiency and for APD for high current gain with gain greater than 1 dB. -Sweep out with an external reverse bias in the absorption "Y" (sometimes referred to as "Y") region of an I-N diode (PD) or P-I-P-N diode (APD).

Microstructure photodiodes and avalanche photodiodes with bandwidths greater than 1 Gb / s are used in communications. Optical signal use techniques such as binary (intensity), phase / frequency shift (subcarrier, heterodyne communication), polarization (polarization) coding, multi-wavelength such as wavelength division multiplexing, and polarization multiplexing. And has information stamped on the light. The optical signal travels in the air and / or through a fiber and hits a microstructure photodiode and / or avalanche photodiode, where information imprinted on the optical signal can be extracted as an electrical signal it is. In some cases, it may be necessary to mix one or more other optical sources, such as in heterodyne or homodyne.

FIG. 1 is a schematic diagram illustrating an optical data transmission system capable of using the present microstructured photodiode / avalanche photodiode, according to some embodiments. The optical data transmission system 100 includes an optical source 110, a transmission medium 120 such as air and / or optical fiber, and a microstructure type photodiode / avalanche photodiode MS-PD / APD. According to some embodiments, the optical source 110 can be a laser. Electrical data 112 is imprinted on the optical signal with a power supply 114 that forward biases the laser 110 for direct modulation. The output of the laser 110 can be coupled to the optical fiber 120 via a coupler 122 such as a ball lens. The optical signal propagates through fiber 120 (or air) and can be coupled from fiber 120 to high speed microstructure photodiode / avalanche photodiode 130, for example, via lens 124, where the optical signal is the converted data 132 and the resulting data 132 (consistent with data 112) is recovered. The microstructure photodiode / avalanche photodiode is reverse biased using a power supply 134.

According to some embodiments, a wavelength selective element can be integrated with the microstructured photodiode and the microstructured avalanche photodiode. In particular, an array of microstructured photodiodes / avalanche photodiodes is fabricated on a single chip that can contain application specific integrated circuits comprising, for example, CMOS, bi-CMOS, bipolar devices and circuits. It is possible. Wavelength selection elements such as bandpass filters can be used for coarse wavelength division multiplexing (CWDM), in which case each carries, for example, 10-40 Gb / s modulation data. Wavelengths of 810, 820, 830, 840, 850, 860, 870, and 880 nm can have an overall data rate of 80-320 Gb / s within a single transmission medium.

Examples of wavelength selective elements include high contrast subwavelength gratings, arrays of subwavelength holes in metal or dielectric films, and dielectric layers having alternating refractive indices, such as in Bragg reflectors. Fig. The high wavelength selective element may be a bandpass filter that includes a number of high contrast gratings to form a cavity resonator. The element can also be a combination of grating and other wavelength selective elements such as subwavelength hole arrays and / or Bragg mirrors on metal or semi-metal films.

Furthermore, the photodiode / avalanche photodiode microstructure itself can form reflectors such as high contrast gratings so that it can be both wavelength selective and absorption length enhanced. In particular, the photon absorption region of the photodiode / avalanche photodiode can be improved. According to some embodiments, additional high contrast gratings can be fabricated on top of microstructured / avalanche photodiodes to form a resonant optical cavity for wavelength selectivity. In this case, if one of the high contrast gratings can be electrically biased to generate a voltage between the two wavelength selection elements, the selected wavelength, such as a tunable optical filter, is used. It is possible to synchronize.

FIG. 2 is a schematic diagram illustrating wavelength selection elements included with a microstructured photodiode (MS-PD) and a microstructured avalanche photodiode (MS-APD), according to some embodiments. In this case, using the wavelength selection element 220, only wavelengths within the selected wavelength range are incident on the MS-PD / APD 130. According to some embodiments, the window can be 120 nm in width (eg, a central wavelength of 820 nm $\pm$ 5 nm, in which case the bandpass is 10 nm centered at 820 nm). In the case shown in FIG. 2, the high contrast grating 220 is made of silicon that can be integrated with the silicon MS-PD / APD 130. According to some embodiments, the microstructure feature 210 of the microstructured photodiode / avalanche photodiode 130 is itself wavelength selective in addition to the ability to improve the absorption characteristics of the photodiode / avalanche photodiode. It is also possible to operate as a container. If the microstructure 210 of the MS-PD / APD 130 is configured as a wavelength selector, the addition of a high contrast grating 220 forms a resonant cavity that can function as a bandpass filter.

FIG. 3 is a schematic diagram illustrating an MS-PD / APD having a plurality of wavelength selection elements according to some embodiments. In this case, a plurality of wavelength selection elements 320 and 322 are manufactured and integrated within the MS-PD / APD 130. Wavelength selection elements 320 and 322 are dual high contrast gratings that function as bandpass filters. According to some embodiments, it is possible to produce a tunable bandpass filter when a voltage is applied to one wavelength selection element relative to the other.

FIGS. 4A to 4D are graphs showing various bandpass filter characteristics based on some embodiments. In the plots in FIGS. 4A, 4B, 4C, and 4D, the center wavelengths are 820, 830, 840, and 850 nm, respectively, and "R" is the reflectance. For example, at the center wavelength for a bandwidth of 10 nm, the reflectivity is practically zero and most of the light is transmitted, while outside the bandwidth, the reflectivity is almost 100% and the transmission is actually close to zero.

FIG. 5 is a schematic diagram illustrating a coarse wavelength division multiplexing (CWDM) configuration according to some embodiments. In this case, four wavelengths propagate through a transmission medium in which the center wavelengths are 820, 830, 840, and 850 nm and each has a modulation data rate of 25 Gb / s with respect to a total data rate of 100 Gb / s. The optical bands are separated by the band pass filters on the MS-PD / APDs 530, 532, 534, and 546 by being reflected by each wavelength selection MS-PD / APD. After each reflection, the light is reflected through reflector 550 to the next wavelength selective MS-PD / APD and so on until all optical bands are absorbed by the designated MS-PD / APD. Is called. Each central wavelength carries one data channel, for example, 820 nm carrier channel 1 at a data rate of 25 Gb / s, and an MS-PD 530 with a bandpass filter at 820 nm converts the 820 nm signal into an optical signal. The recovered data channel 1 is generated for further signal processing by a CMOS ASIC (not shown) that is separated from the rest of the chip and integrated.

According to some embodiments, the MS-PD / APD epitaxial layer thickness is compatible with the epitaxial layer thickness and the structure of the CMOS (complementary metal oxide semiconductor) process, and therefore can be integrated with a CMOS ASIC. is possible. In contrast, a conventional silicon photodiode at 850 nm with a data rate of 1.25 Gb / s has an epitaxial layer greater than 10 μ m thickness and 5% quantum efficiency. Thus, the relatively thick layers of conventional silicon photodiodes are not easily compatible with CMOS processes.

According to some embodiments, the light absorbing layer can be non-crystalline. In particular, it can be hydrogenated amorphous Si (a-Si:H) deposited by, for example, plasma enhanced chemical vapor deposition (PECVD) and / or hot wire chemical vapor deposition (HWCVD). The layer is typically on the order of 0.2-3 μ m thick. High efficiency and high bandwidth for high speed data communication applications by sweeping light generated carriers by applying a reverse bias voltage across the light absorption region (ie, the i region of the pin photodiode structure) make it possible. The layer on the non-crystalline layer can be a transparent or translucent conductive metal or a conductive oxide such as indium tin oxide. The top layer can be a thin layer of amorphous material doped to form a pin structure.

6A and 6B are schematic diagrams illustrating some basic components of a microstructured photodiode, according to some embodiments. FIG. 6 (A) shows the material structure 600 before etching the microstructure, and FIG. 6 (B) shows the MS-PD 640 after etching. It should be noted that, according to some embodiments, the microstructure is a hole 622, and in some other embodiments, the microstructure is a pillar. In some other embodiments, the microstructure is a combination of holes and pillars. The "a" layer 608 can be non-crystalline (eg, hydrogenated amorphous Si (a-Si:H)) grown on a crystalline or non-crystalline N layer. The P layer 610 can also be amorphous and highly doped P or a conductive oxide or metal. N layer 606 can also be a metal or a conductive oxide. Ohmic contacts 628 and 630 are used to apply a bias between the P and N layers to form a high electric field in the i layer 608 that sweeps away hydrogenated carriers. The substrate 602 can be, for example, a non-crystalline and / or dielectric such as quartz, a conductor such as glass, ceramic, and / or metal, silicide, or conductive polymer. According to some embodiments, "a", also known as "i" layer 608, can have a thickness range of 0.2 to 3 μ m.

FIGS. 7A and 7B are schematic diagrams showing some basic components of a bottom-illuminated photodiode according to some embodiments. FIG. 7A shows the material structure 700 before etching the microstructure, and FIG. 7B shows the bottom-illuminated MS-PD 760 after etching the microstructure (holes 722, etc.). In the case of bottom-illuminated PD / APD, the "a" or "i" region 708 can be non-crystalline such as a-Si, H, and the "N" layer 710 can also be non-crystalline. Meanwhile, the "P" layer 706 can be crystalline or non-crystalline on the BOX / SOI 704 and can be a crystalline or non-crystalline substrate 702. However, it is desirable that the substrate 702 and the P layer 706 be crystalline in order to minimize optical loss. This is because it is less absorptive than amorphous silicon at wavelengths in the range of 800-1100 nm. For a "double or multi-bounce" PD / APD, the absorption region "a" layer 708 can have a thickness range of 0.2 to 2 μ m. This is because the optical signal

reflects off the N-metal contact 726 and returns to the "is" absorbing layer 708. The thickness of the "is" layer 708 can be reduced, thus reducing transit time and increasing the photodiode or avalanche photodiode bandwidth.

FIGS. 8A and 8B are schematic diagrams illustrating some basic parts of an MS-APD structure, according to some embodiments. FIG. 8A shows the material structure 800 before etching the microstructure, and FIG. 8B shows the MS-APD 800 after etching. The "is" region 808 for light absorption can be crystalline or non-crystalline such as a-Si:H. Crystalline avalanche gain regions of PIN silicon (823, 818, and 825) are grown on a silicon substrate or BOX / SOI (buried oxide / silicon-on-insulator) substrate 802. The P_u upper layer 810 can be crystalline or non-crystalline. A transparent metal oxide layer 826 can be provided to form ohmic contacts with the P_u layer 810 and / or to reduce sheet resistance. It should be noted that the optical signal may come straight (vertical) to the top surface, or it may come at an angle as indicated by the photon arrow. The microstructure 822 can be a hole, a pillar, or a combination thereof. Although shown in FIG. 8B is a top-illuminated APD 800, according to some embodiments, BOX / SOI can be used to remove the bulk of the substrate, and the APD can be irradiated from the bottom in the wavelength range of 800-1100 nm. A reverse bias is applied between the P ohmic and bond metal 828 through the P layer 810 and the N ohmic and bond metal 830 through the N substrate 802. The reverse bias sweeps away hydrogenated carriers and provides electronic gain. A typical bias voltage for PD is 1 to 10 volts reverse bias, and in the case of APD, the range is approximately 5 to 50 volts reverse bias. As in all PIN and PIPIN devices described herein, P and N are interchangeable, for example, for photodiodes and avalanche photodiodes, PIN can be NIP and PIPIN is NIMP, is possible. The anode or P layer is negatively biased with respect to the cathode N-layer.

FIGS. 9A and 9B are schematic diagrams illustrating certain aspects of a selective area growth (SAG) APD structure before and after SAG of III-V or Ge material, according to some embodiments. FIG. 9A shows a SiAPD structure with etched holes 922 (or areas around the pillars). It is possible to perform selective area growth (SAG) epitaxial growth of III-V material or Ge, in which case the P_u layer 910 and is layer 908 are a-Si:H can be non-crystalline, such as H, or it can be crystalline silicon. In particular, the microstructure I region 904 can be InGaAs or Ge, and the P region 902 can be InGaAs. According to some embodiments, it is possible to manufacture a SAG PD comprising InGaAs or Ge, starting with a PD structure with the avalanche gain layer (P layer 920 and I layer 918) removed. Other materials such as GaN, ZnSe, InP, and GaAs can also be used in SAG. According to some embodiments, other amorphous semiconductors such as amorphous Ge can be used. According to some embodiments, it is possible to use amorphous silicon due to a higher absorption coefficient than photon crystalline silicon, which has energy above indirect transitions.

FIG. 10 is a schematic diagram illustrating a simplified microstructured silicon photodiode with a PIN epitaxial layer according to some embodiments. Holes 1022 are etched into a buried oxide layer (BOX) 1004 that can be 0.2 to 10 μm thick. This structure 1000 provides high contrast in the refractive index between silicon and silicon dioxide, which can improve absorption. The I layer 1008 can have a thickness in the range of 0.5 to 5 μm , and the P layer 1010 and the N layer 1006 can have a thickness in the range of 0.1 to 5 μm . The absorption enhancement can be over 50% in the wavelength range of 800 to 900 nm or more. Its improved absorption is due to a certain wavelength of the optical signal generated by directly modulating a laser, such as a vertical cavity surface emitting laser, or by indirect modulation in which an optical modulator modulates the laser light. It is possible to optimize for the range. The modulated laser light at 60 / s is the optical signal. The optical signal is incident on the microstructured photodiode 1000 either at normal incidence or at an angle to normal incidence. A reverse bias is applied between the anode 1020 of P-ohmic contact and the cathode 1030 of N-ohmic contact for high-speed operation of the microstructure photodiode 1000. What is not shown is a 10 to 100 nm thick passivation layer on the silicon surface, for example, Si₃N₄ (vapor) or dry oxidation to reduce dangling bonds that occur during surface recombination, grown by atomic layer deposition, vapor deposition of silicon dioxide.

FIG. 11 is a schematic diagram illustrating a simplified microstructured silicon photodiode having a PIN epitaxial layer according to some embodiments. MS-PD 1100 is identical to MS-PD 1000, except that the microstructured hole 1122 is not completely etched through the BOX layer 1004. According to some embodiments, an N layer 1006 of 0.01 to 2 μm can be left.

12 (A) (C) illustrate a simulation situation using the Finite Difference Time Domain (FDTD) of the Maxwell Propagation Equation Method for a specific microstructured hole pattern, based on some examples. FIG. 12A shows a hexagonal hole pattern in which the distance between the centers of the holes is 495 nm in the x direction and 860 nm in the y direction. As shown in FIG. 12B, the hole has been etched completely through to a depth of 2 μm , the hole diameter being 385 nm at the top and 430 nm at the bottom. FIG. 12C is a plot showing the results of a simulation using a finite difference time domain technique. Curves 1210, 1212 and 1214 indicate the absorptance, reflectance, and transmittance, respectively. In this particular example, it is understood that for a 2 μm thick silicon, it is possible to absorb more than 60% of light in the wavelength range of 805 to 830 nm. By varying the hole diameter, spacing, and etch depth, it is possible to optimize the absorption for a specific wavelength of the optical signal. According to some embodiments, the hole diameter can be varied from 200 to 1600 nm, the spacing can be varied from 200 to 3500 nm, and the depth can be varied from 0.1 to 2 μm . It is possible.

FIG. 13 is a schematic diagram illustrating an epitaxial layer structure for a high-contrast microstructured photodiode (PD) with P-I-N doping according to some embodiments. Starting with a BOX (buried oxide) 1304 in Si 1302, the thickness of the oxide layer is still in the range of 0.1 to 10 microns or more, and a thin Ge buffer layer 1370 is grown on the NSI 1302. It is possible. With or without the Ge buffer layer 1370, the subsequent N, I, P layers 1306, 1308, 1310 can be made of Ge and / or III-V such as InGaAs, InP, InGaAsP, GaAs, AlGaAs, GaN, InGaN, AlGaIn, etc. it can be a substance group. When the N, I, P layers 1306, 1308, and 1310 are Si, the Ge buffer layer 1370 can be omitted. For high speed operation of the PD, the N layer 1306 can range from 0.1 to 5 microns and the I layer 1308 can range from 0.2 to 3 microns thick. And the P layer 1310 can range from 0.1 to 2 microns. The last layer, in this example the P layer 1310, can be a combination of multiple layers, such as an InP and P layer with a thin InGaAs capping.

FIG. 14 is a schematic diagram illustrating an epitaxial layer structure for a high contrast microstructured photodiode (PD) with P-I-N doping according to some embodiments. The PIN heterostructure can be such that the Ge buffer layer 1470 is at or near the interface between the I layer 1408 and the N layer 1406, in which case the I layer 1408 and the P layer 1410 are Ge and / or Si it is the same as that of FIG. 13 except that it can be made into a III-V substance group. The advantage of this example structure is that for photon energies below the Ge bandgap, a smaller number of electron-hole pairs are generated in the N layer 1406, where photogenerated carriers are generated by the high electric field in the I layer 1408. It is possible to diffuse into the region, resulting in a slow component in the fast response of the PD. The Ge buffer layer may not be necessary for heterogrowth.

FIG. 15 is a schematic diagram illustrating an epitaxial layer structure for a high contrast microstructured photodiode (PD) with P-I-N doping, according to some embodiments. The PIN heterostructure is similar to that of FIGS. 13 and 14 except that only the I region 1508 is Ge and / or lower bandgap materials such as III-V materials such as InGaAs, InP, InGaAsP and InAs. It is the same. Both P layer 1510 and N layer 1506 are composed of a higher band gap material. According to some embodiments, the P layer 1510 and the N layer 1506 have a higher band gap energy than the photon energy, and the I layer 1508 has a band-gap energy equal to or lower than the photon energy. Have. For example, the N layer 1506 can be Si, the I layer 1508 can be InGaAs and / or Ge, and the P layer 1510 can be Si and / or InP. The Ge buffer layer may or may not be necessary for heterogrowth. The advantage of having higher band gap materials in the P and N regions is to minimize the photocarriers generated in these regions. The optical carriers generated in the P and N regions can diffuse into the high electric field region, resulting in a relatively slow component in the photodiode response to short optical pulses. Thus, reducing the optical carriers generated in the P and N regions is a "tail effect". In an optical mod pulse or a set of pulses as in a bitstream for optically transmitting data. In response to this, the fall time of the electrical pulse output of the PD is decreased. High doping of the P and N regions also reduces the minority carrier lifetime so that photocarriers generated in these regions can recombine before diffusing into the high electric field "I" region.

FIG. 16 is a schematic diagram illustrating some aspects of the fabrication of a high contrast microstructured photodiode (PD) based on some embodiments. The exemplary structure illustrated in FIG. 13 is shown with holes 1622 etched through the PIN layers 1510, 1508, 1506 all the way to the oxide layer 1304 embedded in the

silicon layer 1302. Dry and / or wet etches can be used and a passivation layer can be added to the exposed surface by atomic layer deposition. In this example, a Ge buffer layer 1370 is provided at the interface between the N layer 1306 and the Si layer 1302. According to some embodiments, similar manufacturing methods are used for the structures shown in FIGS.

FIGS. 17A-D are schematic diagrams illustrating examples of hole placement, spacing, dimensions, and passivation layers based on some embodiments. FIG. 17A shows a hexagonal layout with a passivation layer thickness of 50 nm with an interval of 200 nm. FIG. 17B shows a square layout. FIGS. 17C and 17D show tapered and vertical hole shapes, respectively. Although these illustrated examples are for silicon, the technique can also be applied to Ge and III-V material groups with minor modifications to the dimensions. The holes can have a circular cross section, or, according to some embodiments, can be other shapes, such as an ellipse, a rectangle, and the like.

FIG. 18 is a schematic diagram illustrating further aspects of the fabrication of a high contrast microstructured photodiode (PD) based on some embodiments. The exemplary structure illustrated in FIGS. 13 and 16 is shown after etching the microstructured hole 1622 and depositing and annealing a P ohmic contact layer 1828.

FIG. 19 is a schematic diagram illustrating some additional aspects of the fabrication of a high contrast microstructured photodiode (PD) based on some embodiments. Illustrative structures illustrated in FIGS. 13, 16, and 18 are shown. After the P ohmic contact 1828 is deposited and annealed, the mesa can be etched to remove the material 1972 to define the PD capacitance. The mesa diameter can range from 5 microns to over 100 microns, depending on the RC time desired for the PD. Passivation of exposed P and N regions is performed to minimize leakage current due to, for example, dangling bonds. According to some embodiments, using ion implantation, such as proton bombardment instead of mesa etching to define the capacity of the PIN structure by generating electrically semi-insulating or insulating regions, is also possible.

FIG. 20 is a schematic diagram illustrating some additional aspects of the fabrication of a high contrast microstructured photodiode (PD) based on some embodiments. Illustrative structures illustrated in FIGS. 13, 16, 18, and 19 are shown. After the mesa etching, a ring or partial ring-shaped N ohmic contact 2030 is formed on the N layer 1306. An insulating layer is formed from a material such as polyimide so that a bridging path is formed to connect the metallization from the P ohmic contact 1828 to a bond pad (not shown) to apply an electrical bias to the P region 1310. Additional processing steps for completing the PD are not shown. For simplification, the metal for connection between the N ohmic contact 2030 and the N bond pad is not shown. A reverse electrical bias is applied to the P and N ohmic contacts 1828 and 2030 to form a high electric field in the I layer 1308. According to some embodiments, a negative 1 to negative 10 volt voltage can be applied.

FIG. 21 is a schematic diagram illustrating several aspects of a lossy high contrast microstructured photodiode (PD) based on some embodiments. FIG. 21 shows a microstructure type PPD in which light travels twice in the absorption layer 1308. This is accomplished by removing a portion 2174 of the Si substrate 1302 down to the oxide layer 1304 and coating the oxide with a metal reflector 2176 such as Au, Ag, Al or Cu. According to some embodiments, it can be in the form of a Bragg reflector for either broadband or wavelength selectivity. According to some embodiments, a Bragg layer may also be included on the top surface of the P layer 1310 to provide additional wavelength selectivity, particularly for use in coarse wavelength division multiplexing, or wavelength division multiplexing, is possible.

FIGS. 22A and 22B show a simulation situation using the FDTD method for a particular microstructure PD based on some embodiments. FIG. 22B is a plot showing simulation results of photon absorption with respect to photon wavelength for the double bounce structure as shown in FIG. Exemplary thicknesses used in the simulation are as follows: oxide 1304 is 2 microns, P silicon 1310 is 300 nm, Si 1308 is 2 microns, and N silicon 1302 is 300 nm, and reflector 2176 is 100 nm thick Au. As shown in FIG. 22A, a hexagonal microstructure hole is adopted. As shown in FIG. 22A, the hole has a center-to-center hexagonal period of 600 nm, a hole diameter of 480 nm, and a SiO₂ passivation of 90 nm. These dimensions are just one example for a microstructured hole with a corresponding simulation of absorption characteristics versus wavelength. As can be understood from the curves 2210 (absorption) and 2212 (reflection) in FIG. 22B, the absorption was found to be significantly higher than in the case of Si without a microstructured hole. For example, in the vicinity of the 850 nm wavelength, the absorption is better than 70%.

FIG. 23 is a schematic diagram illustrating certain aspects of a high-contrast microstructure PD according to some embodiments. Substructure is similar to the structure of FIG. 20, i.e., Si substrate 2302, SiO₂ layer 2304, and a SiN layer 2306. It is also possible to provide a lower Si layer 2308. In this case, Ge is used as the upper I layer 2309 and the P layer 2310. The P layer 2310 can also be composed of InP that can be grown on the Ge layer 2309. The advantage of InPP layer 2310 is that it is less absorptive at wavelengths of 0.9-2 μ m. P layer 2310 can also be composed of GaAs grown on Ge layer 2309. Further, a microstructure hole 2322, a P ohmic contact 2328, and an N ohmic contact 2330 are also shown. It should be noted that light can be incident on the top surface of P layer 2310 and / or on Si substrate surface 2302.

FIG. 24 is a schematic diagram illustrating the situation of a heteroepitaxial microstructure PD based on some embodiments. In this case, the I region can be a composite of Si (lower layer 2408) and InGaAs (upper I layer 2409) separated by a Ge layer 2470. The P region 2410 is InP. According to some embodiments, the I region can be InGaAs grown entirely on a thin layer of buffered Ge layer 2470. In addition, Si substrate 2402, oxide layer 2404, N layer 2406, microstructure hole 2422, P ohmic contact 2428, and N ohmic contact 2430 are also shown. This is an example of a high contrast microstructure PD structure. It can further incorporate a metal reflector as in FIG. 21, in which case Si is removed by etching into the oxide layer underneath the PD and Au, Ag, Al or Cu metal. It is possible to deposit a layer and reflect the light towards the absorbing layer. It is also possible to use a Bragg reflector as described above. In this example, light comes from the P layer side. The light can also come from the Si substrate side, in which case a reflector is placed on the P layer to run the I layer twice. The advantages of such a configuration include that the absorption is significantly improved by running the absorption region twice or more while keeping the I layer unchanged from that of the single run. Yes: By reducing the absorption area thickness to, for example, half that of a single running PD, the speed of the PD is increased. This is because the travel time for a light-generated carrier need only travel half the distance of a single travel PD. The high contrast microstructure means that the refractive index difference between the bulk semiconductor material in the space or air and SiO₂ and / or another surface interface in the microstructure and a surface interface. Light interacts with the microstructure in a complex manner of coupled eigenmodes or resonator cells, where each hexagonal or square cell in the grating is a linear and nonlinear optical that may be generated. In addition to field enhancement, it can be thought of as an individual resonator coupled with its adjacent cell or resonator. If there is little or no optical loss, the coupled resonator structure can have a high Q (resonator quality factor), i.e. before the light disappears, for example, it is possible to bounce repeatedly within the microstructure over 10^4 to 10^6 times. However, if there is some optical loss, such as due to weak absorption, Q may be low and light may bounce repeatedly within the microstructure less than 100 times, or less than 20-30 times. The microstructure in PD / APD is a low-Q high-contrast structure or a lossy high-contrast structure, and the Q of each cell is coupled to an adjacent cell.

FIG. 25 shows a high contrast structure for an optical emitter, such as a light emitting diode (LED) or vertical surface emitting laser (VCSEL), according to some embodiments. The optical light emitter 2500 has a heteroepitaxial layer structure. A Si layer 2506 is formed on the Si substrate 2502 and the SiO₂ layer 2504. A buffer Ge layer 2570 can be formed on the Si layer 2506, followed by a layer 2510, which can be InAs quantum dots 2572 and can be coated with GaAs and AlGaAs. It is. Further, the "n" layer can be as thin as about 1000 nm or less and a simple SiPIN microstructure that is forward biased can be a photon emitter.

FIG. 26 shows a basic structure for a high contrast 1.3 micron wavelength photomixer (PE), for example, according to some embodiments. The active layer for the 1.3 micron wavelength emitter is the InAs quantum dot layer 2679 (shown in FIG. 26) or 2679 in FIG. 26, sandwiched between the GaAsP layer 2604 and the N layer 2608, and these are AlGaAsP layer 2606 and N layer. And a PGaAs capping layer 2670 as a final layer. Typical thicknesses can be found in the literature. For example, see Quantum Dot Lasers for Silicon Photonics such as Ay Lu, S. Srinivasan, J. Norman, AC Clossard, JE Bowers, Photonics Research 3 (5), 81-89 (2015). This document is incorporated herein by reference. Furthermore, there may be multiple layers of quantum dots and / or coating layers. The microstructure can be configured such that standing wave

peaks are located in one or more of the DB layers to optimize gain and optical field overlap. In the case of MS-PE / APD, the length of the microstructure is such that an integer number of wavelengths reciprocate at a particular wavelength, for example, to optimize the absorption enhancement at that particular wavelength. It is possible. Furthermore, a single microstructure, eg, a single hole, has improved absorption or emissions for either PE or MS-PD / APD compared to a similar structure without a microstructure. It is possible.

FIG. 27 is a schematic diagram illustrating some basic features of a high contrast microstructured photoemitter (PE) structure with etched holes, according to some embodiments. Its material structure is the same as that of PE 2500 shown in FIG. Microstructure hole 2722 is etched into active layer 2510. P and N ohmic contacts 2728 and 2730 are used to forward bias the device 2700, ie, to make P positive with respect to N to generate photons from the active layer 2510, which is the present example. Heterostructure quantum dots 2572 at a wavelength of 1.3 microns. Other active layers and coating layers can be used to generate light at other wavelengths from visible to infrared light. Depending on the wavelength of light, light can be emitted from the top surface and / or from the bottom surface via the oxide layer 2504. An advantage of a microstructured high contrast photon emitter is that photons interact longer with the gain layer in the case of the active layer and / or laser. Because, the high contrast structure can have a very high Q, the Q spans 10^5 to more than one million range, because the structure is almost having an optical loss. This is because the quantum dots provide optical gain. The high contrast, low loss microstructured photoemitter can operate as an LED, as a VCSEL, and / or as a laser and / or a high power LED. The PE is forward biased and the P-ohmic or P layer is at a positive voltage relative to the N-ohmic or N-layer cathode 2730.

FIG. 28 is a schematic diagram illustrating several aspects of a PE based on some embodiments. PE 2800 is similar to PE 2700 shown in FIG. 27 except that a portion 2874 of substrate 2502 has been removed in oxide layer 2504 below the light exit region. A Bragg reflector, such as a metal and / or distributed Bragg reflector (DBR) 2504, is formed on the oxide layer to reflect the light generated in the active layer back to the surface of the P layer 2510. According to some embodiments, device 2800 operates in LED mode and / or laser mode.

FIG. 29 is a schematic diagram illustrating several aspects of a PE based on some embodiments. PE 2900 is similar to PE 2800 of FIG. 28 except that it includes a reflector 2928 that can be metal and optionally can also operate as a P-ohmic contact. According to some embodiments, a separate P-ohmic can be provided. The reflector 2928 may be a distributed Bragg reflector and / or partly metal and partly DBR. Light is emitted from the lower surface of the oxide layer 2504 and through the substrate 2502 from which a portion 2874 has been removed. The photoemitter or light emitter 2900 can operate in a laser mode, such as an LED and / or VCSEL mode. According to some embodiments, the photoemitter 2900 can operate in edge mode, in which case light is emitted in plane rather than perpendicular to the plane of the active layer, along the emission edge. There may or may not be a mirror such as DBR or meta.

FIG. 30 is a schematic diagram illustrating several aspects of a PE based on some embodiments. The PE 3000 is similar to the PE 2800 of FIG. 28, but is configured as a VDSSEL (Vertical cavity surface emitting laser). PE3000 has a high contrast microstructured hole (or column) and is heteroepitaxially grown on Si. It should be noted that only very basic parts are shown for the sake of brevity. The high contrast structure can be sandwiched by reflectors 2928 and 3076. The P layer 2510 can be a DBR grown by semiconductor epitaxy, followed by a P-ohmic metallization layer 2928. According to some embodiments, the DBR can be formed from a conductive oxide or a non-conductive oxide, with a P metal on the DBR and / or on its side as in FIG. It is possible to provide. The mirror 3076 on the bottom side of the oxide layer 2504 can be a metal and / or DBR of a dielectric layer of different refractive index. The light output as shown is from the bottom, but can also be from the top.

FIG. 31 is a schematic diagram illustrating some aspects of a simple PIN photodiode structure, according to some embodiments. The "I" layer 3108, P and N layers 3110 and 3106 are highly doped and / or degenerately doped to minimize the diffusion current due to the photocarriers generated in the region outside the high electric field region. Reduce the life of minority carriers. N and P doping can be in the range of $1 \times 10^{18} \text{ to } 5 \times 10^{21} / \text{cm}^3$ or more. The I layer 3108 is not intentionally doped and can be less than $5 \times 10^{16} / \text{cm}^3$. Further, an oxide layer 3104 and a Si substrate 3102 are shown. As in the previous example, Ge and / or III-V materials can be grown with and without the addition of a Ge buffer layer and the P and N layers are also highly doped and / or degenerately doped is also possible. The doping need not be uniform and can have a gradient, for example, an "I" layer interface to minimize dopant diffusion into the "I" layer during epitaxial growth. Reduce doping in nearby P or N layers.

By reducing the lifetime of minority carriers in the P and N layers, the photogenerated carriers in these layers can diffuse and / or recombine before moving into the high electric field "I". In the high electric field "I", electrons and / or holes may contribute to the photocurrent resulting in deterioration of the photodiode modulation type frequency response. Therefore, it is desirable to minimize the contribution of photocurrent due to carriers generated outside the high electric field region.

Other methods of reducing minority carrier lifetime include introducing defects such as partial and / or complete via ion implantation in the P and / or N regions. The ions introduced can be inert ions and / or active ions, with or without partial or complete thermal annealing. Furthermore, the microstructured holes (and / or pillars) may or may not be partially passivated, so the low field regions of the N and P layers act as carrier sinks. While in the high field region of the "I" layer, the carriers are quickly swept away. Passivation can be noticeably selective on the "I" layer.

FIG. 32 is a schematic diagram illustrating some aspects of MS-PD manufacturing according to some embodiments. The starting material structure can be as illustrated in structure 3100 of FIG. A simple NIP (N and P are interchangeable for PIN) microstructured photodiode is shown, with holes 3222 etched into the top of the P layer 3106. Its purpose is to passivate the walls of the N and "I" layers and not passivate the walls of the P layer, thereby reducing the lifetime of minority carriers in the P layer generated by light having a wavelength of, for example, 780 to 980 nm. Decrease. The surface state on the non-passivated P wall can act as a potential sink for minority carriers, where the carriers are recombined.

FIG. 33 is a schematic diagram illustrating certain aspects of MS-PD manufacturing according to some embodiments. The passivation of the sidewalls of the N and "I" layer holes 3222 is shown, resulting in the formation of a passivation layer 3324. The passivation may be carried out using thermal oxidation and / or SiO_2 atomic layer deposition. A 5-50 nm thick thermal oxide 3324 can be grown on the sidewall, for example. Other thicknesses can be grown. After thermal oxidation, the hole can be continuously etched, for example, through the P layer 3106 and etched into the SiO_2 layer 3104. Not all process steps are shown, for example, it is possible to protect the I layer with a thermal oxide (not shown) during the duration of the hole etching.

FIG. 34 is a schematic diagram showing aspects of MS-PD manufacturing based on some embodiments. After passivation, hole 3222 is further etched as indicated by area 3422. It should be noted that the N and P layers can be interchanged, and thus a PIN structure can be used instead of the NIP structure as shown in this example. The holes 3222 can be etched into the SiO_2 layer 3104 and / or they can only be partially etched through the P layer 3106 so that a thin P layer remains. The side of the hole 3222 in the P layer 3106 is not passivated in this example, and its surface state will draw any minority carriers generated by light into the potential sink and recombine. It is possible. According to some embodiments, the P layer 3106 can also be passivated and / or partially passivated. Since layer 3106 can also be highly doped, the minority carrier lifetime can be tens of picoseconds or less.

FIG. 35 is a schematic diagram illustrating certain aspects of an MS-PD according to some embodiments. Microstructured NIP photodiode 3560 has N and "I" layer passivated sidewalls, but the P layer sidewalls have unpassivated microstructure holes 3222. Ohmic contacts 3528 and 3530 to the N and P layers, respectively, are added to provide a reverse bias for high speed operation of the photodiode 3560. The light incident on the N side of the photodiode is either perpendicular and / or deviated from perpendicular to the N layer surface.

FIG. 36 is a schematic diagram illustrating certain aspects of MS-PD, according to some embodiments. The microstructured hole photodiode 3660 has a SiNIP layer, in which case the passivation is partial on the sidewall, similar to the PD 3660 shown in FIG. However, in the case of PD 3660, light comes from the Si substrate side.

through the optical fiber 3650 where the via 3672 is etched to allow a self-aligned process, in which case the fiber 3650 has a lens 3660 or without 3662, guided through via 3672 to the correct position for optical coupling into microstructures photodiode 3650. A dielectric layer 3676 approximately 0.1-10 μm thick can be positioned on the N layer 3110 above the hole 3222. On the dielectric layer 3676 towards a metal reflector 3678 such as Ag or Au (or any other suitable metal or alloy, eg. Al, Ni, Cr, etc.) and / or an absorbing "I" layer 3108 in order to reflect the light, a dielectric laminate such as a Bragg reflector (BR) can be provided. It is also possible to provide an anti-reflective coating 3673. It is also possible to grow Ge and / or III-V material with or without the addition of a Ge buffer layer, as in the previous example.

FIG. 37 is a schematic diagram illustrating a technique for reducing minority carrier lifetime according to some embodiments. In this case, instead of passivating or partially passivating the hole surface, surface and bulk recombination is used. High doping greater than $10^{20} / \text{cm}^3$ can reduce the diffusion length to, for example, less than 0.1 μm (Auger recombination). In addition, ion implantation is used to introduce defects 3770 and 3772 into layers 3710 and 3706. Defects in the semiconductor can also reduce lifetime through a Shockley-Read-Hall recombination process. For example, ions such as Xe, Bi, Ti, Cr, Al, and H can be implanted into the I and / or P layers. In contrast to known structures where long minority carrier lifetimes are desired for device operation, the techniques described herein provide epitaxial growth and / or to increase the recombination rate due to the Shockley-Read-Hall effect. Alternatively, defects are introduced by either ion implantation of metal, non-metal and inert ions. Due to the defects, deep and / or shallow traps can be formed, which can shorten the lifetime of minority carriers. A short minority carrier lifetime is desirable in the P and I regions to minimize the contribution of diffusion currents that can contribute to the photocurrent through the high field region "I" layer. These "slow" diffusion currents that diffuse and / or travel into the "I" region cause degradation of the time response of the photodiode by contributing to a slow component to the photocurrent time response characteristics of the photodiode. There is a case to let you.

38A to 38C show various parameters for the simulated microstructure photodiode. FIG. 38A shows a hexagonal hole pattern having a distance "d" between the hole centers. FIG. 38B shows a square hole pattern having a distance "d" between the hole centers. FIG. 38C is a table of parameters used for the simulation using the FDTD method. SiO₂ having a thickness of 2-2.5 μm with a plurality of holes having a period of 2000 nm and a diameter of 1300 to 1500 nm in the holes of the hexagonal lattice for optical signal wavelengths in the range of 850 to 930 nm and, for example, 900 nm it has been found that it is possible to achieve greater than 90% absorption with a 2 μm thick silicon layer on SiO_2 layers. Furthermore, the wavelength can range from 750-1000 nm. The hole diameter can be larger than the sub-wavelength or the wavelength of the incident optical signal and spans a diameter range of 100 to 3000 nm. The thickness of the Si absorption layer can be in the range of 0.3 to 10 μm . The SiO₂ layer can range from 0.2 to 10 μm . According to some embodiments, a mixture of multiple hole diameters can be used to optimize the absorption of incident photons.

FIG. 39 is a graph plotting simulation results for a microstructured hole photodiode using FDTD versus absorption versus wavelength. The photodiode absorbing "I" layer was 2 μm thick and the hole diameters ranged from 1000 to 1500 nm. The incident energy wavelength was in the range of 850 to 950 nm. Three curves 3910, 3912, 3914 are plots of absorption for 1000 nm, 1300 nm and 1500 nm hole diameters, respectively. This simulation shows that for a 1500 nm hole diameter, greater than 90% absorption is achieved over the wavelength range of 850-930 nm, and for a 1000 nm hole diameter, a hole in a hexagonal lattice with a period of 2000 nm. It shows that it is possible to achieve an absorption greater than 80% over the wavelength range of 875 to 930 nm. SiO_2 is on the 2-2.5 μm SiO₂ layer. As will be appreciated, having a hole diameter larger than the incident wavelength can be used to improve absorption over that of conventional silicon layers without any features.

FIG. 40 is a schematic diagram illustrating a microstructured avalanche photodiode (APD) having a P-I-P-I-N epitaxial structure according to some embodiments. In the case of FIG. 40, all layers of APD 4060 are silicon, for example, for optical communication wavelengths in the range of 780 to 1000 nm. The APD 4060 can also operate in the visible light wavelength range. Data rates can range from 100 Mb / s to 50 Gb / s or more. A reverse bias voltage is applied between the P and N ohmic contacts 4026 and 4030 in the voltage range of -4 to -50 volts. The avalanche microstructure photodiode 4060 can have the following doping and thickness, for example, the doping of the P layer 4010 is greater than $1 \times 10^{18} / \text{cm}^3$ and the thickness is 0.0-1.0 μm , the doping of the I layer 4006 is less than $1 \times 10^{16} / \text{cm}^3$ and the thickness is 0.5-3 μm , and the doping of the P layer 4020 is $1-3 \times 10^{17} / \text{cm}^3$ and the thickness is 0.1-0.5 μm , the doping of the I layer 4018 is less than $1 \times 10^{16} / \text{cm}^3$ and the thickness is 0.3-1 μm , and the doping of the N layer 4008 is $1 \times 10^{19} / \text{cm}^3$ and the thickness is 0.5-3 μm . According to some embodiments, the top two layers 4010 and 4006 can be Ge instead of Si. Hole 4002 can be etched partially through the APD layer or completely etched into the SiO₂ layer 4004 as shown in FIG.

As in the case of microstructure photodiodes, in the case of APD, the optical signal can be incident from the front side (epitaxial layer side) or from the back side (substrate side). Furthermore, if there are vias in the substrate, a reflector can be deposited on the SiO₂, resulting in the optical signal bouncing or bounced twice or many times within the APD structure. According to some embodiments, P and N can be interchanged, resulting in a N-I-N-I-P microstructure APD.

FIG. 41 is a schematic diagram illustrating a microstructured avalanche photodiode (APD) having a P-I-P-I-N epitaxial structure, according to some other embodiments. The APD 4160 is the same as the APD 4060 shown in FIG. 40 except that the plurality of holes 4122 (or pillars) are partially etched. In the example shown in FIG. 41, the holes 4122 are partially etched in the P layer 4020 and / or stopped at the P layer 4020. According to some other embodiments, the holes 4122 can be partially etched into the I-absorption layer 4006.

FIG. 42 is a schematic diagram illustrating a microstructured APD comprising a Ge absorption layer and a GeP clapping layer according to some embodiments. APD 4260 is similar or identical to APD 4060 illustrated in FIG. 40 except that the top two layers are Ge instead of Si. The APD 4260 can have the same doping and thickness range as described above for the APD 4060, except that the PGe layer 4210 can have a doping level greater than $1 \times 10^{20} / \text{cm}^3$ is there. After the epitaxial growth of the APD structure P (Ge) -I (Ge) -P (Si) -N (Si) on a buried oxide (BOX) silicon substrate, the microstructure is etched. The microstructure can be a hole, a pillar, or a combination of the two. The etching is capable of performing up to the SiO₂ layer, or be partially etched to the previous depth reaching the SiO₂ layer 4004 are also possible, for example, holes or into its up PSi layer 4020 it is possible to etch. The Ge absorption layer 4208 comprising the microstructure is expected to allow optical signals to operate at wavelengths between 780 and 2000 nm at data rates of 100 Mb / s to 50 Gb / s or higher. The optical signal can be incident from the top surface (epitaxial surface) or from the bottom surface (substrate surface). If there are reflectors deposited on the vias and SiO₂, the optical signal incident from the top surface can be reflected to the absorbing I (Ge) layer 4208 a second time and / or multiple times. Since there is an optical refractive index difference between Si, Ge, and Ge, it is possible to establish a standing wave and the absorption layer of the peak intensity of the standing wave, also known as a standing wave or eigenmode. It is possible to optimize the thickness of the structure to have. In addition, at wavelengths where Si is transparent, microlenses can be etched into the Si substrate to help couple optical signals from the bottom surface into the APD. SiO₂ and a reflector can be placed on the P (Si) 4210 to reflect the optical signal incident from the bottom to the absorbing I (Ge) layer 4208. A reverse bias voltage in the range of -4 to -50 volts is applied between the P and N ohmic contacts 4026 and 4030.

FIGS. 43A to 43D show the polarization sensitivity of the microstructure photodiode and the APD based on some embodiments. FIG. 43A shows the geometric shape used for the simulation. These holes are symmetric in size and period, and the electric field polarization of the optical signal along either B or A shows a difference of less than 5% in the absorption characteristics of MS-PP / APD. Absorption is equal to incident light minus its transmission and reflection, and quantum efficiency is directly proportional to absorption. If the hole dimensions "a" and "b" are not the same, MS-PP / APD shows polarization sensitivity. In FIG. 43B, curve 4310 plots absorption versus wavelength, in which case the "a" and "b" dimensions are both equal to 1500 nm. The absorption characteristics show a difference of less than 5%. FIG. 43C shows the case where a = 1300 nm and b = 870 nm. Curves 4320 and 4322 show that it is possible to understand that the difference in absorption values in the case of some polarization along A or B is at most twice. FIG. 43D shows the result for the case where a = 1500 nm and b = 650 nm. Curves 4330 and 4332 show that the absorption difference due to polarization orientation is also at most twice. If there are further dimensional changes in both "a", "b", A and B, the absorption difference due

to polarization orientation may differ by 10 to 100 times or more. Both polarization "insensitive" (when the absorption change due to polarization orientation is less than 5%) and polarization sensitivity (when the absorption change due to polarization orientation is 10 times or more) are useful. In short, if the signal is not polarization multiplexed, e.g. using the same wavelength, it is possible to transmit two channels, where one channel is one polarization and another channel is the first it is orthogonal to the channel. For example, each channel can transmit at 25 Gb/s at a specific polarization at the same wavelength. At the receiver end, a polarization sensitive photodetector is used to demultiplex the signal. The total data rate is 50 Gb/s at a wavelength of 850 nm. In the direct modulation of a laser, the spectrum of the laser is always wider than for example a laser operating in CW mode. The spectrum can be broadened by at most several nanometers (e.g. 3 nm). Therefore, when the laser is directly modulated at 850 nm, the center frequency can be set to 850 nm by widening its laser to about 1.5 nm. In a vertical cavity surface emitting laser, the transverse mode can contribute significantly to a wider spectrum due to multiple transverse modes. In multi-mode systems this is desirable because it reduces mode selection loss.

FIG. 44 illustrates an MS-PD / APD integrated with mutual impedance and / or another ASIC (Application Specific Integrated Circuit) for data processing and / or routing, according to some embodiments. Yes, The process can be CMOS and / or BiCMOS. The MS-PD / APD 4420 is shown electrically connected to electronics 4450 (e.g. a mutual impedance amplifier (TIA) and / or another ASIC) via electrical leads 4422. All of the components are integrated on a single silicon substrate 4410. One advantage of integrating microstructured PD / APD with IC electronics is reduced packaging costs, in which case a single chip is used instead of two or more individual devices. It can also be placed directly on the circuit board without using a multi-chip ceramic carrier. Another advantage of integrating MS-PD / APD with electronics on a single chip is potentially lower capacitance due to the omission of relatively large bond pads connected to ohmic contacts. It is to become. The operating wavelength is in the range of 800-990 nm for all silicon microstructure PD / APD. The operating wavelength can be extended to 1800 nm when a Ge microstructured absorption layer is added. Operation at data rates of 10, 25, 50 Gb/s can be achieved alone or in an array. The data rate can also be 1, 5, 20, 25, 30, 40 Gb/s depending on the protocol and link application. Typically, high data rates over multimode fibers and / or multiple fibers are used at distances ranging from less than 1 meter to more than 100 meters. Multiple fiber and microstructured PD / APD (MS-PD / APD) arrays can be used to provide an overall data rate of 100 to 400 Gb/s. For example, each fiber operates at 10 Gb/s with a 10 MS-PD / APD array integrated with IC electronics such as a mutual impedance amplifier (TIA) and / or other signal processing / routing IC electronics on a single silicon chip. 10 fiber channels can have a total data rate of 100 Gb/s if each channel is 5 Gb/s, the 10 channels can have an overall data rate in excess of 500 Gb/s.

FIG. 45 shows some aspects of a flip chip arrangement for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, according to some embodiments. FIG. According to some embodiments, TIA and / or other signal processing integrated circuits 4550 are fabricated using CMOS and / or BiCMOS processes. A chip 4510 is attached to a PCB (Printed Circuit Board) 4550 using solder bumps 4512 and 4514 and / or similar bump technology. According to some embodiments, some or all of the solder bumps 4512 are used to make electrical connections between the chip 4510 and the PCB 4550, while the solder bumps 4514 provide physical mounting and / or stabilization. Used for. This is because a direct electrical connection between the MS-PD / APD 4520 and the PCB 4550 may not be necessary. According to some embodiments, chip 4510 is attached to another chip or multi-chip carrier instead of PCB 4550. Packaging the chip 4510 directly on the PCB 4550 is at least 80% compared to the known prior art where PD and IC electronics are first mounted on a multi-chip ceramic carrier before being placed on the PCB. Only reduce the packaging cost. Further, an integrated optical lens 4522 can be fabricated on the silicon chip 4510 to focus light from the optical fiber 4524 to the MS-PD / APD 4520. It should be noted that in this configuration, the optical signal enters from the substrate side of the MS-PD / APD 4520. An integrated lens 4522 on Si is used when a Ge microstructure can be used for absorption of incoming optical signals and the operating wavelength is greater than 1100 nm (e.g. 1100 nm to 1800 nm). It is possible.

FIG. 46 shows some aspects of a flip chip arrangement for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, based on some embodiments. FIG. The chip and mounting technique is similar or identical to that shown and described in FIG. In this case, chip 4510 includes via 4626 where most or all of the silicon in the optical path to MS-PD / APD 4520 has been removed. An integrated dielectric lens 4622 is provided to collect light and direct it to the MS-PD / APD 4520. According to some embodiments, a light pipe is used instead of lens 4622. The sidewalls of via 4626 can be coated with a dielectric and / or metal to aid in light collection. An anti-reflective coating may be provided on the lens 4622 to reduce the reflection of the optical signal back to the optical fiber 4524. In addition, the fiber 4524 or tip 4510 can be tilted to reduce reflection back to the fiber 4524. Optical fiber 4524 is used to provide optical signals from the laser source to integrated PD / APD and IC electronics circuit 4510 at data rates ranging from less than 1 Gb/s to more than 60 Gb/s. According to some embodiments, data rates of about 1, 5, 10, 20, 25, 30, 50, 56 Gb/s can be used. According to some embodiments, the optical signal wavelength may range from 800-990 nm for all-silicon microstructure PD / APD (MS-PD / APD) and microstructure Ge for the absorber layer. In this case, the wavelength can be extended to 1800 nm.

FIG. 47 shows some of the flip-chip arrangements for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, according to some other embodiments. It is the schematic which shows the side surface. The chip and mounting techniques are similar or identical to those shown and described in FIGS. 45 and 46. As in FIGS. 45 and 46, a single chip 4610 includes both optical and electronic elements. Vias 4626 are provided in the substrate of the chip 4510 to remove most or all of the Si in the optical path to the MS-PD / APD 4520 along with the integrated Fresnel lens 4722 so that optical signals are efficiently transmitted from the optical fiber 4524. To be collected. The collected optical signal is incident on the MS-PD / APD 4520. According to some embodiments, high contrast grating (HCG) is used instead of Fresnel lens 4722. According to some embodiments, HCG can have a filter effect, so that only certain optical wavelengths can be transmitted to MS-PD / APD while others can be reflected. This bandpass characteristic is useful for coarse wavelength division multiplexing (CWDM), where multiple wavelengths are used in a single fiber.

FIG. 48 illustrates some aspects of a flip chip arrangement for an MS-PD / APD integrated with a TIA and / or another signal processing IC on a single silicon chip, according to some other embodiments. It is the schematic which shows these. The chip and mounting techniques are similar or identical to those shown and described in FIGS. 45-47. The walls of via 4626 can be coated with a dielectric and / or metal to provide a light pipe for light to enter MS-PD / APD 4520. The optical fiber 4524 can then be inserted into the via 4626, in which case the via provides a guide for aligning the fiber 4524 with the MS-PD / APD 4520, thereby MS-PD / APD simplifies optical packing and alignment of the optical fiber to the APD, resulting in a cost reduction of about 30% or more. According to some embodiments, the fiber 4524 can be tapered and / or can have multiple diameters so that the via 4626 provides a step for the fiber 4524. For example, the via 4626 can be stepped to allow the end of the fiber 4524 to abut on that step and attach it to the silicon. This step configuration also provides a precise distance between the fiber and the MS-PD / APD for optimal light collection. According to some embodiments, in order to optimize the transfer of optical signals from the fiber to the MS-PD / APD, refraction in the via 4626, particularly in the space between the fiber 4524 and the MS-PD / APD 4520, it is possible to use rate matching fluids, gels and / or polymers and / or dielectric bulks or thin films.

As mentioned above, when light is incident from the substrate side (bottom illumination), MS-PD / APD can use double and / or multiple bounces of optical signals within the MS-PD / APD. It is. This makes it possible to achieve a high quantum efficiency and to make the absorption layer thinner. A thinner absorbent layer allows for faster travel times, thereby allowing MS-PD / APD to operate at higher data rates.

FIG. 49 illustrates some aspects of a flip chip arrangement for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, according to some other embodiments. It is the schematic which shows these. The chip and mounting techniques are similar or identical to those shown and described in FIGS. 45-48. In this example, a ball lens 4922 is positioned within the via 4626 to efficiently couple light from the optical fiber 4524 to the MS-PD / APD 4520. Ball lens 4922 may be located in via 4626 for alignment of the lens with respect to MS-PD / APD 4520.

FIG. 50 illustrates some aspects of a flip chip arrangement for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, according to some other embodiments. It is the schematic which shows these. The chip and mounting technique is similar or identical to that shown and described in FIGS. 45-49. In this example, the ball lens 5022 is located in the via 4626 where most or all of the silicon is etched away so that most of the light is in the air and / or fluid, gel, polymer,

solid, etc. It runs in the refractive index matching material. Further, the via 4626 acts as a guide and / or stop for alignment of the optical fiber 4626 with respect to the ball lens 5022 and further with respect to the MS-PD / APD 4520.

FIG. 51 shows some aspects of a flip chip arrangement for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, based on some embodiments. FIG. 51 shows the chip and mounting techniques are similar to those illustrated and described in FIGS. 45-50, but the MS-PD / APD 5120 and TIA and / or other signal processing integrated circuits 5130 are on the top surface of the silicon chip 5110. Or it is mounted in the vicinity. The metallic conductive conduits 5132 and 5134 can be made of Al, Cu, Mo, W, Ni, TiN or the like. Conduit 5132 connects MS-PD / APD 5120 to IC electronics 5130. Conduit 5134 connects IC electronics 5130 to traces to PCB 4552 (or chip carrier) using bump technology such as solder bumps, which is a good way to connect the chip to PCB and / or chip carrier. Allows alignment. According to some embodiments, other methods using wire bonding can be used to connect the IC electronics to the traces on the PCB and / or to the chip carrier. The fiber 4524 is located in the immediate vicinity of the MS-PD / APD 5120 and the configuration includes a ball lens on the tip of the fiber 4524 and / or a ball lens between the fiber and the MS-PD / APD, if possible. As described with respect to FIGS. 45-50, other light focusing elements such as gratings and Fresnel lenses may be used. According to some embodiments, there is a refractive index discontinuity such as buried silicon dioxide (BOX, buried oxide) and / or bulk material as shown in the MS-PD / APD structure described above. When there is a change in the effective refractive index of the microstructure with respect to the refractive index, the light irradiating from the epitaxial surface (top illumination type) is also reflected in the MS-PD / APD 5120 by the optical signal duplex and / or Or it may have multiple bounces. Double and / or multiple bounces of optical signals in MS-PD / APD allow for thinner absorption layers and shorter transit times without significantly sacrificing quantum efficiency, thereby allowing MS-PD / APD higher data rate operation. Double or multiple bounce of light means light that is not absorbed in the MS-PD / APD both and exits the MS-PD / APD structure, and these photons are MS-PD / APD Reflected back towards the structure. Within a microstructure consisting of a plurality of holes and pillars, light may be in a resonant and / or coupled resonant state, which can result in an improved effective absorption coefficient and / or improved effective absorption length. Is possible.

FIG. 52 is a schematic diagram showing an array of multiple MS-PD / APDs integrated with IC electronics such as TIA and / or other signal processing and routing electronics on a single Si chip. The array can include, for example, 2 to more than 10 MS-PD / APDs integrated with IC electronics such as TIA and / or ASIC for signal processing, routing, storage. In the illustrated example, four MS-PD / APDs 5220, 5222, 5224, and 5226 mounted on a single Si chip 5210 are shown. These MS-PD / APDs 5220, 5222, 5224, and 5226 are connected to IC electronics 5230, 5232, 5234, and 5236, respectively. However, according to some embodiments, multiple MS-PD / APDs are connected to a single IC electronics device on a Si chip, or multiple IC electronics devices are a single MS-PD / APD. Connected to. Multiple MS-PD / APDs in the array can be the same, for example, the hole diameter and period of the microstructure is optimized for the same wavelength, eg 850-870 nm. According to other embodiments, each MS-PD / APD in the array can be optimized for different frequency bands. For example, if there are four MS-PD / APDs in the array, by optimizing the hole diameter and period of each MS-PD / APD, the four MS-PD / APDs are respectively, 850-870 nm, 875-895 nm, 900-920 nm, 920-930 nm (or any combination thereof). See, for example, Molin et al., 350-950 nm wideband OMA multimode fiber for next generation WDM systems, OFC (2015), for next generation WDM systems, incorporate into this book. 1,3,10,16,20,25,28,32,40,56 and more and all ranges of data rates between them are standards and protocols for optical data links and applications it is possible depending on the. The optical fibers 5240, 5242, 5244, 5246 can be separate fibers or can be provided as parallel fiber ribbons. Optical fibers 5240, 5242, 5244, 5246 each carry a single band wavelength and / or multiple band wavelengths for WDM and DWDM to provide a combined data rate of 100 Gb / s to 1 Tb / s or higher. It is possible. For example, an array of 10 MS-PD / APD with 10 Fiber Channels, each of 10 Gb / s, gives a total data rate of 100 Gb / s. A 4MS-PD / APD array with 4 Fiber Channels each at 25-28 G / b/s gives a total data rate of 100 Gb / s, and 2MS-PD with 2 Fiber Channels each at 56 Gb / s The / APD array gives a total data rate of 100 + Gb / s. 4 fibers if each fiber channel can carry multiple wavelength bands, eg 850-870 nm and 875-895 nm, and each wavelength band can transmit at 25-28 Gb / s. The array can have an overall data rate that effectively exceeds 200 Gb / s.

FIG. 53 is a schematic diagram illustrating an epitaxial structure for high data rate MS-PD, according to some embodiments. The illustrated structure can be larger than 10 Gb / s. Holes 5322 can be etched to the SiO₂ BOX layer 5304, or the holes can be etched in the P layer 5306 and / or partially etched into the P layer 5306, for example. The doping and thickness are as follows: Si substrate 5302 is 150 μm thick, BOX layer 5304 is 2-4 μm thick, and P + layer 5306 is 0.2-1 μm thick. The doping is over $1 \times 10^{20} / \text{cm}^3$ and the I layer 5308 is 1.5-2 μm thick and is not intentionally doped (less than $5 \times 10^{18} / \text{cm}^3$). The N + layer 5310 is 0.2-0.5 μm thick and the doping exceeds $1 \times 10^{19} / \text{cm}^3$. High doping of the N and P layers 5310 and 5308 minimizes the diffusion current that may shorten the minority carrier lifetime and slow down the PD response. According to some embodiments, doping as high as greater than 1×10^{20} and $1 \times 10^{21} / \text{cm}^3$ is used such that minority carrier lifetime is on the order of picoseconds and series resistance is reduced.

FIG. 54 is a schematic diagram illustrating an epitaxial structure for high data rate MS-PD, according to some embodiments. This structure and doping is similar or identical to that illustrated and described in FIG. 53, but etched until hole 5422 reaches the top of P layer 5306 and / or just enters P layer 5306. It has been different.

FIG. 55 is a schematic diagram illustrating an epitaxial structure for high data rate MS-PD, according to some embodiments. This structure and doping is similar or identical to that illustrated and described in FIGS. 53 and 54 except that the hole 5522 is etched at least halfway into the P layer 5306.

FIG. 56 is a table showing mesa dimensions, hole diameters, hole period distances, and lattice patterns for MS-PDs based on some examples. In these examples, the grid can be hexagonal or square. The hole can be circular, elliptical or polygonal. The holes have a diameter of 1300 nm with a period of 2000 nm, a diameter of 1500 nm with a period of 2000 nm, a diameter of 700 nm with a period of 1000 nm, and a diameter of 650 nm with a period of 900 nm. The operating wavelength is 800-900 nm and the material is Si. It is possible to include a thin passivation layer 5612 with a thickness in the range of 3-100 nm. The mesa size partially determines the capacity of the MS-PD (excluding bond pads and contact metals), depending on the data rate of the MS-PD, 5 μm, 10 μm, 20 μm, 25 μm, 30 μm, 40 μm, ..., 50 μm, and 80 μm. Low capacity and short transit time make MS-PD with higher data rate.

FIGS. 57A and 57B are schematic diagrams illustrating hexagonal and square grid hole patterns according to some embodiments. FIG. 57 (A) shows a hexagonal lattice pattern, and FIG. 57 (B) shows a square pattern, and "d" is the period in each case. According to some embodiments, these layouts are used for the exemplary parameters for the MS-PD shown in FIG.

FIG. 58 is a schematic diagram illustrating an epitaxial layer structure for silicon MS-PD, according to some embodiments. The thickness and doping of this structure is as follows. Si substrate 5802 is 150 μm, BOX (buried oxide) layer 5804 is 2-4 μm thick, SP layer 5806 is 0.2 μm thick. At a thickness of ~0.5 μm the doping exceeds $2 \times 10^{20} / \text{cm}^3$ and the SN layer 5808 is about 1.5-2 μm thick and is not intentionally doped (5×10^{18} and a background doping of less than $10^{18} / \text{cm}^3$). SN layer 5810 is doped beyond $2 \times 10^{20} / \text{cm}^3$ with a thickness of about 0.2 μm. The high doping of the P and N layers can be, for example, greater than $1 \times 10^{19} / \text{cm}^3$. According to some embodiments, an etch stop layer made of a material such as SiGe₂, SiGeC, or SiGeBC and having a thickness of 5 nm to 50 nm may be processed during a microstructured hole and / or mesa etch period. To help, it can be included at the interface between P5806 and IS5808. If highly P-doped SiGe is used, the structure is preferably NIP. High doping in the P and N regions, in addition to reducing sheet resistance, also reduces the minority carrier lifetime, so photons absorbed in the P and N regions contribute minimally to the photocurrent. The reduced minority carrier lifetime in the P and N regions reduces the diffusion of photogenerated carriers into the high electric field "I" region, where minority carriers are swept to the anode and cathode to photocurrent. Contribute.

FIG. 59 is a schematic diagram illustrating certain aspects of an MS-PD, according to some embodiments. Its material structure, including thickness and doping, is similar or identical to that shown and described in FIG. In the case of FIG. 59, the P and N dopings in layers 5910 and 5906 are exchanged to form a P-I-N configuration. It

should be noted that in either FIG. 58 or 59, the arrangement can be P-I-N or N-I-P. Hole 5922 is etched into SiO₂ 5804 and P and N ohmic contacts 5926 and 5930 are formed for P and N layers 5910 and 5906, respectively. The mesa is etched to define the photosensitive area and to define the capacity of the PIN structure. The mesa diameter ranges from 10 μm to 80 μm depending on the data rate for which the MS-PD is designed (as described with respect to FIG. 56). For 20-40 Gb/s, the mesa diameter is typically 20-40 μm. A doping P layer 5910 greater than $2 \times 10^{20} / \text{cm}^3$ with a thickness of 0.2 μm can have a sheet resistance of less than about 50Ω. A doped N layer 5906 with a thickness of 0.2 μm and greater than $2 \times 10^{20} / \text{cm}^3$ can provide a sheet resistance of less than about 35Ω. The high doping of the P and N layers can also be set to $1 \times 10^{19} / \text{cm}^3$, for example. Thinner P and N layers allow a higher percentage of optical power to be in the "I" layer and a lower percentage in the P and N layers, thereby maximizing MS-PD quantum efficiency. Let For convenience of explanation, passivation, polyimide bridges, bond pads and other processing steps are not shown. A reverse bias voltage is applied between the P and N contacts to form a high field region in the "I" layer. The voltage is typically in the range of about 2-4V. In the case shown, the illumination is at an angle that is vertically above or offset from above. The wavelength is in the range of 800-990 nm, but other wavelengths such as 780 nm can also be used. The nominal wavelength is 850 nm, but can include wavelengths such as 810-830, 830-850, 850, 880, 930-950, 960-990, and the like.

FIG. 60 is a schematic diagram illustrating certain aspects of an MS-PD, according to some embodiments. The MS-PD, including material structure thickness and doping, is similar or identical to that illustrated and described in FIG. 58. In this case, the hole 6022 is etched up to and / or in the N layer 5906, but not to the SiO₂ layer 5804 as shown in FIG. Accordingly, the absorption in the "I" layer is not improved, and as a result, the percentage of optical power in the "I" layer may be higher. This tends to improve the quantum efficiency of the MS-PD. The SiO₂ layer 5804 may or may not be necessary.

FIG. 61 is a schematic diagram illustrating certain aspects of an MS-PD, according to some embodiments. The MS-PD is similar or identical to that illustrated and described in FIG. 58-61, including material structure thickness and doping. In this case, the MS-PD is irradiated from the substrate side (also referred to as a back irradiation type or a bottom irradiation type in this document). The silicon substrate was removed via 6170 is etched and penetrate up to the SiO₂ layer 5804 or most or the SiO₂ layer to the SiO₂ layer to or the SiO₂ layer in. The Si substrate 5802 is removed to minimize optical loss in the wavelength range of 800-990 nm. A reflector 6132 is fabricated on the surface of the P layer 5910, which uses a filler process such as polyimide, solid carbon dioxide, or spin-on-glass (SOG) to prevent the reflector 6132 from shorting the PIN diode. It is possible to include. It should be noted that the reflector 6132 need not be exactly planar and can be concave in the area with the holes, which may improve the trapping of the light wave. The reflector 6132 can be a metal or alloy, such as a dielectric, Bragg reflector, conductive transparent metal oxide, silver, gold, or any combination thereof. Indium tin oxide (ITO) can also be used with a non-conductive dielectric to form a Bragg reflector. Metals and / or conductive oxides can further reduce the sheet resistance of the P layer 5910, thereby reducing parasitic resistance and improving the modulated frequency response (data rate) of the MS-PD. According to some embodiments, the "I" layer 5908 can be made thinner in the case of backside illumination with a reflector. This is because light can travel through the "I" layer at least twice and possibly more times without degrading quantum efficiency, and at the same time the MS-PD modulation frequency (data rate). This is because it improves the response. The reason is that for the thinner "I" layer, the transit time of the photogenerated carrier is shorter. The frequency response of a photodiode is determined by its capacitance and resistance (RC time) and transit time. For example, the optical transit time may be important at a high improved effective absorption length that is greater than a factor of 100 or more for some high data rates.

FIG. 62 illustrates a Ge-on-Si PIN epitaxial layer structure for MS-PD, according to some embodiments. The material structure including thickness and doping is similar or identical to that illustrated and described on FIGS. 58-62. In this case, the NSi layer 6202 having a doping exceeding $2 \times 10^{19} / \text{cm}^3$ can have a thickness of 0.2-2 μm. A Ge "I" layer 6208 is also provided, which is not intentionally doped, the doping is less than $2 \times 10^{16} / \text{cm}^3$ and the thickness is 0.5-2 μm. The upper GeP layer 6210 with a doping exceeding $2 \times 10^{20} / \text{cm}^3$ is formed with a thickness of 0.1-0.2 μm. According to some embodiments, a thin Ge buffer layer (not shown) is used at the interface between the NSi layer 6206 and the "I" Ge layer 6208 to initiate good crystal growth of Ge on Si. It is possible. High doping of P and N also reduces minority carrier lifetime, thereby spreading photogenerated carriers that may be swept into the optical field "I" region that may contribute to the overall photocurrent is minimized.

FIG. 63 shows a Ge-on-SiMS-PD according to some embodiments. The MS-PD is similar or identical to that illustrated and described in FIGS. 58-62, including material structure thickness and doping. The hole 6322 has been etched to the SiO₂ layer 5804, or the hole can be etched to the NSi layer 6206, in which case the SiO₂ layer 5804 may or may not be necessary. And the MS-PD is irradiated from the top or from (epitaxial surface). Photon absorption in the wavelength range of 1100 to 1800 nm is mostly in the Ge region than in the Si region. By keeping the PGe layer 6210 thin, a large percentage of the photons are absorbed in the Ge "I" layer 6208, thereby increasing quantum efficiency. The high refractive index difference between Ge and Si may require that the hole only be etched to the top of the NSi layer 6206. However, in this example, the hole 6322 is etched down to the SiO₂ layer 5804. The NSi layer 6206 can be up to 2 μm thick in this example and can be doped in the range of $1 \times 10^{19} / \text{cm}^3$ to provide a sheet resistance of less than 50Ω. is there. For 850 nm operation, or for wavelengths in the range of 800-990 nm, a thin NSi layer can increase the percentage of photons absorbed in the Ge region. A 0.2 μm thick NSi layer with a doping of more than $2 \times 10^{20} / \text{cm}^3$ provides a sheet resistance of less than 50Ω and reduces minority carrier lifetime. A 2 μm thick NSi layer can also be used for the wavelength range of 800-990 nm or 800-1800 nm. This is because for wavelengths in the 800-990 nm range, Ge absorbs more than 90% of the photons over a length of 2 μm. Therefore, less than 5% of the photons reach the NSi layer. At a wavelength of 850 nm, less than 1% reaches the NSi layer, and at 990 nm, less than 3% reaches it.

In some cases, for a wavelength range of 800-990 nm, the microstructured hole may not be used predominantly to improve absorption, but rather partially or completely within the Ge layer. It may be used to reduce the volume at the etched hole. Furthermore, holes may not be necessary and bulk Ge may be used. According to some embodiments, the microstructure can also be used to reduce reflection.

FIG. 64 shows a Ge-on-SiMS-PD according to some embodiments. The MS-PD is similar or identical to that shown and described in FIGS. 58-63, including material structure thickness and doping. In this case, the hole 6422 is etched up to the Si layer 6206. The refractive index for Ge is about 4 and the refractive index for Si is about 3.45. This difference in refractive index may give sufficiently improved absorption in the Ge region. In this case, the SiO₂ layer 5804 may not be necessary and the MS-PD may be grown on the Si wafer without the SiO₂ layer 5804. For the 1100-1800 nm wavelength range, Si has an acceptable low optical loss and most of the absorption is in the Ge region. In the case of top illuminated MS-PD, the PGe layer can be made thin, so the bulk of the photons is absorbed in the Ge region, which increases the quantum efficiency. ITO (Indium Tin Oxide) may be used in conjunction with the PGe layer 6210 to further reduce the sheet resistance of the P layer.

FIG. 65 shows a Ge-on-SiMS-PD according to some embodiments. The MS-PD is similar or identical to that illustrated and described with respect to FIGS. 58-64, including material structure thickness and doping. In this case, the MS-PD is a back or bottom irradiation type. This structure is very good for a wavelength range of 800-1800 nm using a thin NSi layer of 0.2 μm. Less than 3% of photons having a wavelength at 800 nm are absorbed in the NSi layer 6206. Furthermore, in a single pass of 1 μm Ge, more than 85% of the 990 nm photons are absorbed. In double pass, more than 95% of 990 nm photons are absorbed. In back-illuminated MS-PD where Ge is grown on NSi, with the reflector 6532 on the PGe layer, double and / or multiple passes of the photons enable a thinner absorption layer 6208. This reduces the transit time of light-generated electrons and holes. It is possible to obtain a photodiode with a higher bandwidth of 40 Gb/s or higher. Hole 6322 can be etched into SiO₂ layer 5804 or can be etched into Si layer 6206 (as shown in FIG. 64). For microstructured hole arrays, improved absorption can occur at wavelengths between 1100-1800 nm. For example, at 1550 nm, less than 9% is absorbed in a double pass through a 1 μm thick bulk Ge, while greater than 30% if there is a microstructured hole in the Ge layer. Absorption can be achieved, and in some cases, absorption greater than 50% can be achieved. In some cases, absorption in MS-PD with a Ge layer is 20% at 1550 nm for double pass in 1 μm thick Ge or for single pass in 2 μm thick GeMS-PD. Larger things can be achieved.

The MS-PD can have the following layers: the Ge (or SiGe) P layer 6210 can be doped to a thickness of about 0.1 μm and greater than $2 \times 10^{20} / \text{cm}^3$. Yes, Ge (absorbing layer) 6208 can be 0.5-2.0 μm thick and intentionally undoped (less than $5 \times 10^{16} / \text{cm}^3$), and finally The SiN layer 6206 can be doped to a thickness of 0.2-0.8 μm and exceeding $2 \times 10^{19} / \text{cm}^3$. In addition, during the via etch to remove the Si substrate, the SiO₂ layer can be left unchanged, partially etched, or fully etched to remove the SiO₂ is there.

FIG. 66 is a schematic diagram showing Ge-on-SiPD according to some embodiments. The PD is similar to that illustrated and described in FIGS. 58-65, including material structure thickness and doping. FIG. 66 shows what is arranged as a flip chip, but although it slightly deteriorates due to the PGE layer, a front-illuminated arrangement is also possible. The PD is similar to the MS-PD shown in FIG. 64 without the microstructured hole array. Ge-on-Si photodiodes with an epitaxial structure as illustrated for operation at 800-1300 nm, particularly utilizing double bounce or double bounce for the 1300 nm wavelength region, yet high data rate operation, is maintained. The PD can be integrated with SiGeBiCMOS. According to some embodiments, the SiO₂ layer is omitted. With solder bump technology, the PD can be a flip chip mounted directly on a PCB, as described above for other embodiments, for example, as shown in FIGS. 44-52. According to some embodiments, the PD can have the following layers: Ge (or more than $2 \times 10^{20} / \text{cm}^3$ with a thickness of about 0.1 μm) (or SiGe) P layer 6210, 0.5-2.0 μm thick, intentionally undoped (less than $5 \times 10^{16} / \text{cm}^3$) Ge (absorbing layer) 6208, and finally 0.2-0.8 μm SiN layer 6206 doped with a thickness of $2 \times 10^{19} / \text{cm}^3$. Further, during the etching period of the via 6670 for removing the Si substrate, the SiO₂ layer 5804 is left unchanged (as shown in FIG. 66), partially etched, or the SiO₂ is removed. Therefore, it is possible to etch completely (as shown in FIG. 66). If the SiO₂ layer is completely etched away, an antireflection layer (not shown) can be applied to the SiN layer to minimize reflection.

FIG. 67 is a schematic diagram showing a Ge-on-SiPD according to some embodiments. The PD is similar to that illustrated and described in FIGS. 58-66, including material structure thickness and doping. In this case, a void 6722 is formed to reduce the device PIN junction capacitance. Void 6722 can be partially etched into the Ge layer to remove a sufficient amount of material to reduce the volume by a certain amount. The capacity reduction allows for a larger area PD while maintaining the same data rate bandwidth as a similar Ge-on-SiPD without voids. The larger area PD allows for greater tolerances in optical fiber and / or light source misalignment with respect to the photodiode. The data rate bandwidth is determined by RC time and travel time. Integration of all the structures described above is possible with electronics such as TIA that can be directly attached to the PCB along with solder bump technology. According to some embodiments, the operating wavelength for this structure is in the range of 800-1300 nm and the data rate is over 40 Gb / s.

Note that it is not necessary to use a BOX structure. This PD is possible to have a layer such as the following, namely: GEP layer is doped beyond the $2 \times 10^{20} / \text{cm}^3$ with a thickness of about 0.1 μm 6210, 0.5-1. Ge (absorbing layer) 6208 with a thickness of 0 μm and not intentionally doped (less than $5 \times 10^{16} / \text{cm}^3$), and finally $2 \times 10^{19} / \text{cm}^3$ with a thickness of 0.2-0.8 μm A SiN layer 6206 doped over $2 \times 10^{19} / \text{cm}^3$ and a 2-4 μm buried oxide layer 5804.

FIG. 68 is a schematic diagram illustrating certain aspects of a microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD can have the following layers: SiP layers 6810, P-doped with a thickness of about 0.1-0.2 μm and exceeding $2 \times 10^{19} / \text{cm}^3$ unintentionally doped with a thickness of 0.2-0.8 μm (less than $5 \times 10^{15} / \text{cm}^3$) Si (absorbing layer) 6808, 2×10^{19} with a thickness of 0.2-0.5 μm A SiN layer 6806 that is n-doped over $2 \times 10^{19} / \text{cm}^3$ and a 2-4 μm thick buried oxide layer 6804 on the Si substrate 6802. The MS-APD device has two additional layers: a charge layer and a multiplication layer. The charge layer 6820 is directly below the absorption layer 6808. The SiP charge layer 6820 is doped to about $1.8 \times 10^{17} / \text{cm}^3$ and has a thickness of about 0.1 μm , immediately below the charge layer is the MS-APD multiplication layer 6818. The Si layer 6818 is intentionally undoped (less than $1 \times 10^{16} / \text{cm}^3$) and has a thickness of about 0.5 μm . Via 6870 has been etched through the silicon substrate to the SiO₂ layer (anti-reflection coating can be applied to minimize reflection) and light having a wavelength in the range of 800-990 nm has passed through the via. Applied through. A reflector 6832 on the top surface of the MS-APD provides double / multiple passage of photons through an absorbing "I" layer 6808. One advantage is a thinner absorbent layer, which allows for shorter transit times. Therefore, the data rate bandwidth of the MS-APD is improved. Microstructure mold cavity array 6822 is etched until the SiO₂ layer 6804 and / or most the SiO₂ layer. P and N contacts 6828 and 6830 are shown on the same surface to be soldered, so that the MS-APD is flip chip mounted directly on a ceramic multichip carrier and / or on a printed circuit board. It is possible. For convenience of explanation, only the most basic processing steps are shown. Additional steps or elements such as passivation, bond pads, polyimide / spin on glass planarization, antireflective coating, etc. are not shown. Further, after the Si substrate is removed during the etch of via 6870, the SiO₂ layer may be partially etched away or completely etched away for either MS-APD or MS-PD structures. Is possible. In the absence of the reflector 6832, the optical signal can also be incident from the top surface.

FIG. 69 is a schematic diagram illustrating certain aspects of a microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD is similar to that illustrated and described in FIG. 68, including material structure thickness and doping. The microstructured hole array 6922 is etched down to the charge layer 6820, multiplication layer 6818, and / or N layer 6808 of the APD structure. The hole 6922 is not etched until the SiO₂ layer. Light is irradiated through the via 6970 from which the silicon substrate has been removed in the SiO₂. The SiO₂ layer can also be etched so that light is directly incident on the NSI layer 6806. This is applicable to all bottom-illuminated MS-PD and MS-APD devices, in which case the antireflection coating can be applied directly to Si. For wavelengths in the range of 800-990 nm, a thin NSI layer 6806 of about 0.2 μm is preferred to reduce absorption in regions away from the absorbing "I" layer 6808. Light can also be obtained from the top / front, in which case the reflector 6832 is eliminated. In such cases, vias may be omitted and the Si "I" layer may be increased to 1.5-2 μm for quantum efficiencies greater than 30%. In some cases, the quantum efficiency is over 50%, in some cases over 70%, and in some cases over 80%. The avalanche multiplication factor or gain can be greater than two. In some cases, the gain is greater than 5. In some cases it is more than 10. In some further cases, it is greater than 15 and in some other cases the gain is greater than 20. The data rate bandwidth can exceed 10 Gb / s. In some cases the bandwidth is greater than 15 Gb / s and in some cases greater than 30 Gb / s. Furthermore, the SiO₂ layer can be completely or partially removed and / or it can have voids that are filled or not filled with Si for MS-PD and MS-APD. It is possible to use an etch stop layer such as SiGeB, SiGeC or SiGeBC during the removal of the Si substrate to form was used for back / bottom illumination.

FIG. 70 is a schematic diagram showing an MS-APD without the SiO₂ layer according to some embodiments. The MS-APD is similar to that illustrated and described in FIGS. 68-69, including material structure thickness and doping. The etch stop layer 7034 is SiGe or SiGeC or SiGeB (the SiGe has about 1% Ge and is lightly doped with boron above $1 \times 10^{20} / \text{cm}^3$) and has a thickness of it is in the range of 0.1 to 2 μm . SiGeBC can be grown on a Si substrate 6802 and / or on a Si epitaxial layer such as NSI layer 6806. According to some embodiments, the MS-APD has the following thicknesses and doping levels: SiN layer 6806 has a thickness and doping level in the range of 0.2-1 μm . SiN layer 6806 has a thickness in the range of 0.2 to 1 μm and a doping in the range of greater than $2 \times 10^{19} / \text{cm}^3$ to greater than $2 \times 10^{20} / \text{cm}^3$, and Si The multiplication layer 6818 is intentionally undoped (less than $1 \times 10^{16} / \text{cm}^3$) and has a thickness of about 0.5 μm , and the SiP charge layer 6820 is about 1.8×10^{17} . Si absorption layer 6808 is intentionally undoped (less than $5 \times 10^{15} / \text{cm}^3$) and 0.5 $\mu\text{m} / \text{cm}^3$ and has a thickness of about 0.1 μm . -1.0 μm thick And which have and have SiP capping layer 6810 $2 \times 10^{20} / \text{cm}^3$ to beyond the thickness of and about 0.1 μm is doped. According to some embodiments, multiple etch stop layers can be used. For example, another etch stop layer can be formed at the interface between the Si multiplication layer 6818 and the SiN layer 6806. The thickness of the etch stop layer can range from 1 nm to 100 nm and should be doped to P- or N- or not intentionally doped to match the electrical properties of adjacent layers. It is possible. The wavelength of the optical signal can range from 800 to 990 nm, and when illuminated from the back side, the reflector can be formed from a dielectric such

as SiO_2 / Ag. According to some embodiments, the reflector 6832 is a Bragg reflector made of two dielectrics such as ITO with SiO_2 and HfO_2 , or Ag, Au and / or Pt with different refractive indices. The reflector 6832 is used to reflect the unabsorbed signal photons through the absorbing Si region 6808 for double and / or multiple passes. Furthermore, the device can be of the front-illuminated type, in which case the reflector 6832 is omitted and the absorbing Si layer 6808 is thickened to 1.5-2 μm to optimize quantum efficiency. According to some embodiments, the front / top illuminated MS-APD can also include via. Similarly, some MS-PDs can use this structure, omitting the SiP charge layer and Si multiplication layer. Front and back illuminated MS-PD may be beneficial. This is because removal of the Si substrate improves the refractive index contrast and has an improved absorption coefficient in the microstructure, which improves the quantum efficiency.

In the MS-PD / APD data rate response (also called frequency response), high doping of the P and N layers reduces sheet resistance and reduces the lifetime of minority carriers in the P and N layers. Reduces minority carrier diffusion into the high-field Si absorbing layer that may cause degradation. The microstructured hole array can be etched beyond the stop layer either up to the SiGeC and / or SiGeB stop layer and / or during the hole etch period and / or during the via etch period. The etch stop layer can also be completely or partially removed after the hole etch or during the via etch. Thus, there is no SiGeC, SiGeB or SiGeB layer in the optical path for back-illuminated MS-PD / APD. It should be noted that in SiGeB where Ge is about 1% (eg, $\text{Si}_{0.99}\text{Ge}_{0.01}$), its band gap is about the same as that of Si. Furthermore, as in FIG. 69, the microstructured hole array is etched to a depth corresponding to the absorbing Si layer and / or to a depth larger than the Si absorbing layer and partially into the avalanche region, is possible.

FIG. 71 is a schematic diagram illustrating a Ge-on-Si microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD is similar to that illustrated and described in FIGS. 68-70, including material structure thickness and doping. The GeI absorption layer 7108 is intentionally undoped (less than $5 \times 10^{15} / \text{cm}^3$) and has a thickness of 0.5-2.0 μm . The top GeP capping layer 7110 is doped in excess of $2 \times 10^{20} / \text{cm}^3$ and has a thickness of about 0.1 μm . The microstructured hole array 7122 has been etched to the SiP charge layer 6820 or just before the SiP layer. Alternatively, the holes 7122 can be etched into the SiP charge layer 6820 and / or into the Si multiplication layer 6818. Via 7270 is etched to remove the Si substrate from the optical path. The SiO_2 layer can be left unchanged, partially etched or etched completely through, or an NSI substrate without SiO_2 can be used. In the case where the SiN layer 6806 is exposed, an antireflection layer (not shown) can be provided to minimize reflection. The wavelength range can be, for example, 800-1800 nm, 1300-1600 nm, 810-860 nm, 950-990 nm. The hole size and period can be optimized for a range of wavelengths. A reflector 6832 can be formed on the Pile or SiGe layer 7118. The reflector 6832 can be composed of dielectric and metal, ITO (indium tin oxide or similar transparent conductive oxide) and metal, all dielectric such as Bragg reflector, or any combination thereof. i.e. Reflector 6832 reflects the photons that were not absorbed in the first pass back toward absorbing GeI layer 7108 for two or multiple passes. It is possible to use a thinner GeI absorber layer 7108 compared to a single pass photodiode. The thinner GeI layer results in shorter transit times and thus higher data rates. Ge-on-Si growth may use a Ge buffer layer, which is grown to initiate high quality crystal growth of Ge. See, for example, Kang et al., Epitaxially-grown Ge / Si avalanche photodiodes for 1.3 Em light detection, Vol. 16, no. 13 / OPTICS EXPRESS 9365 (2008) (hereinafter referred to as "Kang et al"), which is incorporated herein by reference. In the wavelength range of 1200-1750 nm, the via 7270 is not necessary because Si is almost transparent at these wavelengths. Further, in the absence of reflector 6832, the optical signal can be incident from the top surface and Ge "I" layer 7108 can increase the thickness to about 2 microns.

FIG. 72 is a schematic diagram illustrating a Ge-on-Si microstructure avalanche photodiode (MS-APD), according to some embodiments. The MS-APD is similar to that illustrated and described in FIGS. 68-71, including material structure thickness and doping. In this case, the microstructure hole array 7222 is etched down to the SiO_2 layer 6804. According to some embodiments, the holes 7222 are etched to a sufficient number of micrometers of the SiO_2 layer 6804 and the via 7270 is etched to the SiO_2 layer. The SiO_2 layer can remain unchanged during the via etch, can be partially etched, or can be etched completely through. The light incident from the back side has a wavelength in the range of 800-1800 nm. Other wavelengths such as 630-780 nm can also be used. There may be some photogenerated carrier in the Si layer, but the bulk of the photogenerated carriers is in the GeI layer 7108, especially in the wavelength range of 800-1800 nm, especially 1100 in the wavelength range of ~1800 nm. The epitaxial structure is similar to that shown in FIG. 71 because the reflector 6832 on the GeP layer reflects light back toward the GeI absorbing layer. The removal of the SiO_2 layer allows a high reflection index contrast between the microstructured semiconductor holes, which can improve the light collection characteristics of the microstructured hole array and air. Further, SiO_2 -air interface and SiO_2 -reflections that occur at the semiconductor interface has been removed. In the case of front-illuminated MS-APD, the reflector 6832 is removed and the GeI absorption layer 7108 is thickened to a range of 1-2 μm . The removal of the via and SiO_2 can be performed for front side irradiation type MS-APD. By removing the avalanche layer, P charge and I multiplication, the MS-APD becomes MS-PD.

FIG. 73 is a schematic diagram illustrating a Ge-on-Si microstructure avalanche photodiode (MS-APD) with an etch stop layer, according to some embodiments. The MS-APD is similar to that illustrated and described in FIGS. 68-72, including material structure thickness and doping. An etch stop layer 7334 such as SiGe, SiGeC, SiGeB, or SiGeB is grown on the Si wafer. It should be noted that the Si substrate (wafer) 6802 already has an NSI epitaxial layer, a subsequent APD layer, other buffer layers, spacer layers, or other etch stop layers (not shown). On the surface, which promote good crystal growth and process reproducibility. The basic APD layer has a SiI layer 6806 with a thickness ranging from 0.2 to 0.8 μm and a doping exceeding $2 \times 10^{19} / \text{cm}^3$ to exceeding $2 \times 10^{20} / \text{cm}^3$. SiI multiplication layer 6818, intentionally undoped and having a thickness of about 0.5 μm , doped to about $1.8 \times 10^{17} / \text{cm}^3$ and has a thickness of about 0.1 μm . SiP charge layer 6820, GeI absorption layer 7108 which is not intentionally doped and has a thickness of 0.5-1.0 μm , and the doping is greater than $2 \times 10^{20} / \text{cm}^3$ and the thickness is A Ge or SiGeP capping layer 7110 that is about 0.1 μm . Microstructured hole arrays are etched with hole diameters and periods that are optimized for specific wavelength ranges. Specific group length ranges include the following: 800-850, 860-880, 890-920, 920-950, 950-1100, 1100-1350, 1350-1450, 1450-1550, 1550-, 1650, 1650-1800 nm. Hole and mesa passivation are omitted for convenience of explanation, examples of which are shown in Kang et al. There are other methods of passivation in the literature. Light enters from the back side through the via 7370, and in this case, the etch stop layer can be removed. Although light can be incident from the front side, the thickness of the absorbing GeI layer 7108 is increased to a range of about 1-2 μm . In the case of front-illuminated MS-APD / PD, for example, the via can be implemented to increase the reflection index contrast between the semiconductor microstructure and air. Other layers such as passivation layers, bridge layers, bond pads, and fillers are not shown for convenience of explanation.

FIG. 74 is a schematic diagram illustrating a Ge-on-Si microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD is similar to that illustrated and described in FIGS. 68-73, including material structure thickness and doping, but to reduce absorption of photocarriers in the P contact layer. The difference is that the GeP layer is replaced with a P layer 7410 of SiGe or SiGeC. SiGe and / or SiGeC have a larger bandgap than Ge, so that for the same thickness, the absorption coefficient is smaller than in Ge. For example, Koldzay et al., "Optical and electronic properties of SiGeC alloys grown on Si substrates", Journal of Crystal Growth 157, 386-391 (1995) (hereinafter referred to as "Koldzay et al"), which is incorporated herein by reference. For example, from Koldzay et al, for SiGe, E_g is 1.3 eV (direct) compared to 1.11 eV for Si and 0.66 eV for Ge. In other words, SiGe alloys provide a band gap between Si and Ge, so any addition of Si to Ge will increase the band gap and reduce absorption in the P layer. According to some embodiments, this P layer replacement technique applies to all MS-PD / APD structures shown and described herein. In particular, the GeP layer is replaced with a SiGeP and / or SiGeCP layer. According to some further embodiments, in all MS-PD / APDs shown and described herein, the SiP and N layers can also be completely or partially replaced by SiGeCP and SiGeCN. Yes, which reduces the absorption of optical signals in the P- and N regions of the MS-PD / APD. In some cases, the APD multiplication region, which is Si, can also be replaced with SiGeC to reduce optical photon absorption in the present invention. At a wavelength of 1200-1750 nm, Si is almost transparent and either or both of via 7370 and etch stop layer 7334 are not needed. In this case, the back surface is polished using an NSI substrate and an antireflection coating is applied.

FIG. 75 is a schematic diagram illustrating another SiNP epitaxial layer structure for MS-PD, according to some embodiments. Hole 7522 has been etched to a depth of about 2.3 μm and can be terminated a few microns before and / or after SiP layer 7506. The doping and thickness are approximately as follows: SiP substrate 7502, which can exceed $1 \times 10^{19} / \text{cm}^3$, but with P doping exceeding $2 \times 10^{20} / \text{cm}^3$ is 0.2 μm (or 0.1-1 μm range) SiP layer 7506, intentionally undoped, background doping less than $5 \times 10^{16} / \text{cm}^3$ and in some cases $5 \times 10^{15} / \text{cm}^3$ Si layer 7508 that is less than $10^{15} / \text{cm}^3$ and has a thickness in the range of about 2 or 1-2.5 μm , the doping is greater than $2 \times 10^{19} / \text{cm}^3$ and the thickness is about 0.3 μm or 0 NSi layer 7510 in the range of 2-0.5 μm . N contact 7528 is on SiN layer 7510. The P contact may be on the top surface of the SiP substrate as in contact 7530 and / or on the bottom / back side of the substrate as in contact 7532. A mesa etch is used to define the PIN junction area and hence the capacitance. Mesa can be etched down to P layer 7506 and / or P substrate 7502 and P contact 7530 can be deposited on SiP layer 7506 and / or on the back side 7532 of SiP substrate 7502. According to some embodiments, other electrical isolations can be used, such as proton bombardment to define a PIN area or other doping such as PN junction doping or trench doping. Technology in this structure, light is incident from the front side at a wavelength in the range of about 800-900 nm. A period of 2000 nm and a hole diameter of 1500 nm and a period of 2000 nm and a hole diameter of 1500 nm can be used in either hexagonal and / or square lattice patterns. According to some embodiments, the hole diameter ranges from about 800 nm to 1500 nm and the period ranges from about 900 to 2500 nm.

76 (A)-(C) are schematic diagrams showing SiNP epitaxial layers on a buried oxide for MS-PD, according to some embodiments. In FIG. 76A, holes 7622 have been etched into the SiP layer 7606 and have been partially etched into the SiP layer and / or into the SiO₂ layer 7604. The doping and thickness are approximately as follows: SiBOX (buried oxide) 7604 in the substrate 7602, 1 μm (or 0.1-1 μm of P doping exceeding $2 \times 10^{20} / \text{cm}^3$) Range) SiP layer 7606, intentionally undoped and having a background doping of less than $5 \times 10^{16} / \text{cm}^3$ and in some cases less than $5 \times 10^{15} / \text{cm}^3$ A Si layer 7608 with a thickness in the range of 2 μm or 0.5-2.5 μm , and a doping greater than $2 \times 10^{19} / \text{cm}^3$ and a thickness of eg 0.3 μm or 0.2-0.5 μm The range is the NSi layer 7610. N and P contacts 7628 and 7630 can be on the front side, in which case the P contacts are formed after mesa etching to the P layer 7606. An etch stop layer such as SiGeB or SiGeC can be used at the interface between the P layer 7606 and the I layer 7608. If a reflector is placed on the top surface SiN layer 7610 so that light is incident from the back side and light can pass multiple times through the I layer 7608, the I layer 7608 is the thickness can be reduced, for example, 0.5-1 μm . P and N can be exchanged, and the microstructure photodiode (MS-PD) can be, for example, a PIN. When SiGeB is used as an etch stop layer, the SiGeB is highly P-type and the NIP structure is preferred. The etch stop layer can be, for example, 0.35 to 1 μm thick and can replace the SiP layer in whole or in part. With appropriate modification of the device or the epitaxial layer, light can be incident from the front side and / or from the back side. The wavelength range is about 800-900 nm.

In FIG. 76 (B), the PSI layer 7606 in FIG. 76 (A) has a P doping exceeding $2 \times 10^{20} / \text{cm}^3$ and a thickness in the range of 0.5 μm or 0.2-1 μm . It is replaced with a Si_{0.99}Ge_{0.01} B layer 7616. All other layers are as shown in FIG. Microstructure mold holes 7622 can be etched and stop in the SiGeB layer and / or pass through the SiGeB layer and stop in the SiO₂ layer and / or can enter the SiO₂ layer if it is. It is possible to etch a via 7670 that penetrates either or it stops at the SiO₂ layer in the stop in the SiO₂ layer. N and P ohmic contacts 7628 and 7630 are formed on the SiN layer and the SiGeBP layer, respectively. Light can be incident either from the top surface (epi surface) and / or from the bottom surface (substrate surface), and with a dielectric spacer layer to pass multiple times through the I absorbing layer it is possible to place a reflector on either the top or bottom. The wavelength is in the range of 800 to 1000 nm. Those not shown for convenience of explanation are other elements such as a passivation layer, a polyimide bridge layer, a mesa, and a bond metal.

In FIG. 76C, a PSI layer 7626 having a thickness of about 0.1 μm and a doping greater than $1 \times 10^{20} / \text{cm}^3$ is added as a first layer on SiO₂ 7604, and a Si_{0.99}Ge_{0.01} B layer 7616 with a doping greater than $1 \times 10^{20} / \text{cm}^3$ and a thickness of about 0.5 μm is grown. As in FIGS. 76A and 76B, light can be incident from the top and / or bottom surface where the via is etched. N and P ohmic contacts are respectively disposed on the N and P layers. Microstructured hole array 7622 is etched through SiO₂ layer 7604 and / or partially etched into P layer 7626. If light is incident from the bottom, the via 7670 can be etched into the silicon substrate 7602 and into the SiO₂ layer 7604, where the SiO₂ layer 7604 can be partially or fully etched. A reverse bias voltage of 1-10 volts is applied between the P and N contacts.

In some applications, light can be incident simultaneously from the top and bottom of the MS-PD / APD. The light can have the same or different wavelength, data rate, polarity, and amplitude for coherent optical communications. The advantage of light entering from both the top and bottom is that there is no need to use a beam splitter and a 3 dB savings in optical power loss can be made.

FIG. 77 is a schematic diagram illustrating an MS-PD comprising a SiNP epitaxial layer and a SiGeB etch stop layer on a PSI substrate, according to some embodiments. The etch stop layer 7716 can be comprised of about 1% Ge in Si_{0.99}Ge_{0.01} B or SiGe, in which case its band gap is substantially the same as Si and B doping is it exceeds $1 \times 10^{20} / \text{cm}^3$. This high degree of P doping may cause partial or complete replacement of the SiP layer 7706. These layers and thicknesses can be as follows: SiP substrate 7702, SiGeB layer 7716 with a thickness of 0.1-2 μm , P doping exceeding $2 \times 10^{20} / \text{cm}^3$ A 0.2 μm (or 0.1-1 μm range) SiP layer 7706, intentionally undoped, with a background doping of $5 \times 10^{16} / \text{cm}^3$ and in some cases $5 \times 10^{15} / \text{cm}^3$ A Si layer 7708 that is less than $10^{15} / \text{cm}^3$ and has a thickness in the range of 2 μm or 0.5-2.5 μm , and a doping that is greater than $2 \times 10^{19} / \text{cm}^3$ and a thickness of 0. The NSi layer 7710 is in the range of 3 μm or 0.2-0.5 μm . Both N and P contacts 7728 and 7730 can be on the front side. The P contact can also be on the back side of the PSI, as in contact 7732. Microstructured hole array 7722 can be etched into SiGeB etch stop layer 7716. Mesa is etched into the SiP and / or into the SiGeB layer to define the NIP area and thus the NIP capacity. P contact 7730 can be disposed on PSI layer 7706 or PSiGeB layer 7716. N contact 7728 is disposed on SiN layer 7710. To remove the Si substrate, a via 7770 can be etched down to and / or partially into the SiGeB layer using an etching process different from that for the Si and SiGeB. The SiGeB layer 7716 can also be etched away, in which case the via 7770 extends to the SiP layer 7706. Further, the SiP layer 7706 can be partially or entirely replaced with the SiGeB layer. In such a case, it is desirable that a SiGeB layer of at least 0.2 to 0.3 μm remains. Light can be incident from the front and / or back side. It is possible to provide a dielectric metal reflector with a dielectric in contact with the semiconductor and a thickness of 0.5-4 μm , in which case the dielectric is SiO₂, polyimide, SiO₂, Calcium fluoride. Alternatively, it can be silicon nitride, followed by a metal or alloy such as Ag, Au, Al, Ni or the like on either the front side or the back side. For example, when the dielectric metal reflector is disposed on the back side, light from the front side can be reflected many times through the absorbing I layer, and conversely, the reflector is arranged on the front side, the light from the back side can be reflected many times through the absorbing I layer. If there is a reflector, it is possible to use a thinner I layer, for example 1 μm or about half the thickness of MS-PD without a reflector, which means that it is possible to achieve a higher data rate for the MS-PD. In the case of the MS-PD, it is possible to use a wavelength range of 800-900 nm. In some cases, the reflector can simply be a metal such as a Bragg mirror. Furthermore, the via 7770 may not be necessary if the light is incident only from the front surface and two and / or multiple reflections are not realized.

FIG. 78 is a schematic diagram illustrating Ge-on-SiNP on a SiGeB epitaxial layer for MS-PD, according to some embodiments. Microstructured hole array 7822 has been etched in Ge layer 7810 and 7808 and into or to SiP layer 7806. The etch stop layer 7816 is composed of Si_{0.99}Ge_{0.01} B or about 1% Ge of SiGe, where the band gap is substantially the same as Si and B doping is $1 \times 10^{20} / \text{cm}^3$ is exceeded. This high degree of B doping may partially or fully replace the SiP layer 7806. These layers and thicknesses can be as follows: the SiP substrate 7802, the SiGeB layer 7816 is 0.1-2 μm thick, and the SiP layer 7806 is 0.2 μm (or 0.2 μm , 1-1 μm range). P doping is $1 \times 10^{19} / \text{cm}^3$. GeI layer 7808 is not intentionally doped and background doping is less than $5 \times 10^{16} / \text{cm}^3$ and several in this case, the thickness is less than $5 \times 10^{15} / \text{cm}^3$, the thickness is in the range of 2 μm or 0.5-2.5 μm , and the NSi layer 7810 has a doping exceeding $2 \times 10^{19} / \text{cm}^3$. The thickness is in the range of 0.2 μm or 0.2-0.5 μm . Both N and P contacts 7828 and 7830 can be on the front side. The P contact may be on the back side on the PSI substrate, as in contact 7832. A Ge buffer

layer of several nm can be grown between the Si layer and the Ge layer, and the growth conditions of the Ge buffer layer in that case are different from the growth conditions of the Ge layer. Via 7870 can be etched into the Si substrate 7902 to remove the Si up to the SiGe layer 7915. The SiGe layer 7916 can be partially and / or fully etched under different etch conditions. The light can be incident from either the front side or the back side, and in the presence of a reflector, the photons pass multiple times through the I absorption layer and the device operates at a higher data rate. It is possible to use thinner layers for the purpose. This is because the transit time of photogenerated carriers of electrons and holes is much shorter. The wavelength range is 800 to 1600 nm. The hole diameter and array period can be optimized for a range of wavelengths ranging from about 30-100 nm. Via 7870 may not be required if the optical signal is incident from the front / top surface. In addition, if the optical signal has wavelengths in the range of 1200-1750, the silicon is almost transparent at these wavelengths or the optical loss generated is very low, so in the case of bottom illumination. There may be no need for via.

FIG. 79 is a schematic diagram illustrating a Ge-on-Si epitaxial structure for MS-PD, according to some embodiments. Its material structure is as follows: SiN substrate 7902 (or alternatively NIP structure on PSi substrate), 0.2 μm (or 0.1 μm) with N doping exceeding $2 \times 10^{19} / \text{cm}^3$. SiN layer 7906 (in the range of $\sim 1 \mu\text{m}$), intentionally undoped, with background doping of less than $5 \times 10^{16} / \text{cm}^3$ and in some cases less than $5 \times 10^{15} / \text{cm}^3$. A Ge layer 7908 with a thickness of 2 μm or a thickness range of 0.5-2.5 μm , and a doping of $2 \times 10^{20} / \text{cm}^3$ and a thickness of 0.2 μm or 0.2-0.5 μm . The PGe layer 7910 is in the range of Both P and N contacts 7928 and 7930 can be on the front side. The microstructured hole array 7922 is etched in the NSI layer 7906, partially etched into it, or etched through it. A mesa etch defines the PIN area and volume. N contacts 7930 and 7932 are deposited after the mesa etch on either the front or back surface of the NSI substrate. Passivation is not shown, but Fang et al. Can be used to deposit amorphous Si on the exposed Ge surface sidewalls and anneal at high temperatures and / or SiGe on the exposed Ge sidewalls it can be deposited and annealed to reduce leakage current. The mesa diameter in the MS-PD and MS-APD can be in the range of 5 μm to 100 μm depending on the data rate. According to some embodiments, the mesa diameter range is 20-80 μm for a data rate of 30 Gb / s. Furthermore, a buffer Ge layer can be used between NSI 7906 and iGe 7908 to ensure high crystal quality. For example, Kang et al. Good to see. When light enters from the front side, the wavelength can be in the range of 800-1800 nm. In a preferred range, the wavelength can be 1450-1600 nm, and in another preferred range, for example, 1250-1600 nm. The MS-PD / APD can cover both data communication wavelengths and telecommunications wavelengths.

FIG. 80 is a schematic diagram illustrating another Ge-on-Si epitaxial structure according to some embodiments. The MS-PD, including the thickness and doping of its material structure, is similar or identical to that illustrated and described in FIG. 79, but it is a buried oxide having a thickness of 0.2-4 μm . The difference is that it is grown on a SiBOX wafer comprising a physical layer 8004. Microstructured hole array 8022 can be etched to NSI layer 7906 and etched into or until NSI layer 7906 or to SiO₂ layer 8004. A mesa etch defines the PIN capacity and the mesa diameter for the MS-PD / MS-APD is in the range of 5-100 μm depending on the data rate bandwidth of the MS-PD / APD. A mesa diameter of 20-50 μm is preferred for a data rate bandwidth of 20-35 Gb / s. Light can be incident from the front or back surface. At wavelengths above 1100 nm, the optical loss of Si is very low and the Si substrate can be used, for example, to etch lenses or gratings. Via 8070 can be etched to completely or partially remove SiO₂. Via 8070 can be used to guide light and / or fiber to, for example, the MS-PD. It is possible to deposit a reflector 8072 in the via 8070, in which case the SiO₂ is completely free so that light from the front side bounces off the reflector and traverses the iGe absorption region 7908 multiple times. No removal or no removal at all. If the reflector is on either the front side or the back side, iGe 7908 can be thinner, for example 1 μm , which reduces the electron hole transit time and the MS-PD / MS- increase APD data rate bandwidth. The wavelength can be in the range of 800-1800 nm, which covers both data communication and telecommunications wavelength ranges. In the case of a continuous NSI layer 7906, for example, if the SiO₂ layer is completely etched, an anti-reflective coating can be applied to the bottom surface of the NSI.

FIG. 81 is a schematic diagram illustrating a Ge-on-Si epitaxial structure according to some embodiments. The MS-PD is similar or identical to that illustrated and described in FIGS. 79-80, including the thickness and doping of its material structure, but the via 8170 has a SiO₂ BOX layer 8004, or the SiO₂ thickness or range of 0.2-4 μm The etched and 2-4 μm partially etched to either completely etched, or it may be one that does not etch is different. Further, it is possible to form a reflector 8172 made of a material such as Ag, Au, Cr, or Al. The reflector 8172 can also be a broadband, narrowband, or passband Bragg reflector. It should be noted that if the reflector 8172 is a dielectric, it can be deposited directly on the NSI layer 7906 by etching away the SiO₂ layer. Light incident from the front side that was not absorbed in the first pass through the iGe layer 7908 can be reflected back to the iGe layer for multiple passes through the iGe absorption layer. The iGe layer can be thinner, for example 1 μm , which makes the transit time for electrons and holes in the iGe layer shorter. This increases the data rate bandwidth of the MS-PD / MS-APD.

82A-82C relate to a simulation using finite difference time domain (FDTD) for a Ge-on-Si microstructured photodiode similar to the structure illustrated in FIG. FIG. 82A is a schematic diagram showing a Ge-on-Si microstructure photodiode subjected to simulation. The hole pattern is a square lattice pattern. Simulations are performed for two combinations of hole period and hole diameter: 2500 nm hole period and 1500 nm diameter and 2300 nm hole period and 1300 nm diameter. In FIGS. 82B and 82C, the horizontal axis is the wavelength in μm and the vertical axis is absorption, which is directly related to quantum efficiency. In each case, a square grid pattern of holes is simulated. In FIG. 82B, for an optical signal having a wavelength in the range of 800 nm to 1600 nm, curve 8210 is a plot of absorption versus 2300 nm hole period and 1300 nm diameter, and curve 8212 is 2500 nm hole period and 1500 nm. is a plot of absorption versus diameter. In FIG. 82C, for an optical signal having a wavelength in the range of 1000 nm to 1600 nm, curve 8220 is a plot of absorption versus 2300 nm hole period and 1300 nm diameter and curve 8222 is 2500 nm hole period and 1500 nm. It is a plot of absorption versus diameter. Absorption ranging from 0.4 (absorbs 40% of photons) to more than 0.9 (absorbs 90% of photons) in the wavelength range of 0.8 to 0.9 μm was determined. Absorption greater than 0.5 is seen for 1.55 μm and extends to 1.6 μm for an approximately 2 μm absorption layer of Ge. This is significantly larger than the 2 μm thick equivalent Ge layer without the microstructure, especially at 1550 nm and longer wavelengths.

83A-83C relate to a simulation using finite difference time domain (FDTD) for a Ge-on-Si microstructured photodiode similar to the structure in FIG. FIG. 83A is a schematic diagram showing a Ge-on-Si microstructure photodiode that is simulated with light incident from the top surface. In the graphs of FIGS. 83B and 83C, the horizontal axis is the wavelength in μm and the vertical axis is absorption, which has a period of 2500 nm and a diameter of 1500 nm (curves 8312 and 8322), a period of 2300 nm and a diameter of 1300 nm (curve 8310 and 8320) directly related to the quantum efficiency for a multi-hole square lattice. Absorption greater than 0.7 (absorbs 70% of photons) is seen for 1.55 μm and better than 0.8 absorption (absorbs 80% of photons) for an approximately 2 μm absorption layer of Ge it extends to 1.8 μm . This is significantly greater than, for example, an equivalent InGaAs layer lattice matched to InP having a thickness of 2 μm at 1550 nm and longer wavelengths.

84A and 84B show the results of a simulation using finite difference time domain (FDTD) for a Ge-on-Si microstructured photodiode. The simulated structure is shown in FIG. 82A. In FIGS. 84A and 84B, the horizontal axis of the graph is wavelength in μm and the vertical axis is absorption, which is directly related to quantum efficiency for both square and hexagonal lattices for the hole array. ing. FIG. 84A shows both a square lattice (curve 8410) and a hexagonal lattice (curve 8412) with a period of 2300 nm and a hole diameter of 1300 nm. Absorption greater than 0.9 (absorbing 90% of the photons) is shown for the 1.55 μm wavelength with the region where the absorption varies by less than 10% over the 50 nm wavelength span. FIG. 84B shows both a square (curve 8420) and hexagonal (curve 8422) lattice for a diameter of 1500 nm with a period of 2500 nm, which shows an absorption of 0.7 at 1.55 μm . Overall, the hexagonal lattice shows better photon absorption than the square lattice. Other combinations of period and hole diameter, hole shape and grating can be used to improve or optimize absorption in certain wavelength ranges.

FIG. 85 shows a schematic plan view of a microstructured photodiode chip, not to scale, according to some embodiments. The approximate dimensions of the chip 8560 are 350 μm $\times$ 300 μm $\times$ 150 μm . The mesa defined by mesa edge 8562 has a diameter of 30 μm . The mesa defines a NIP or PIN junction capacitance. An upper surface 8510 is visible at the top of the mesa (eg, an N layer taking NIPMS-PD / APD), and a microstructured hole 8522 is also visible. Near the outer edge of the mesa is an N ohmic contact ring 8528 (takes NIPMS-PD). There is a P-ohmic contact ring 8530 outside the mesa. N bond pad 8580 is electrically connected to N ohmic contact

8528 by bridge interconnect 8582. Similarly, P bond pad 8594 is connected to P ohmic contact by interconnect 8592. According to some embodiments, undesired shorts between the bridge interconnect 8582 and the area 8506 (which may be the P layer surface) use an insulator such as polyimide deposited between them. Has been prevented. It should be noted that the above description is also applicable to a PIN placement: MS-PD / APD where the N and P layers and contacts are reversed.

According to some embodiments, a simple process flow of the basic manufacturing steps of a NIPMS-PD structure on a BOXSi wafer consists of (1) masking and etching the hole array 8522 into the SiO₂ layer; (2) Mask and deposit N ohmic contact metal ring 8528 on N layer 8510; (3) Etch mesa defining mask and define junction capacitance; Etch to P layer 8506; (4) Mask and SiO₂; (5) Mask and deposit P ohmic contact metal 8530 on P layer 8506; (6) Mask polyimide bridge for contact to N ohmic ring 8528 by bond pad 8580; (7) Mask and bond pad 8594 for both P-ohm and N-ohm respectively. And depositing a 8580, it may consist: Since the bond and bond pad capacitances are parallel and are therefore additive, the bond pad is in contact with the N ohmic ring 8528 at approximately $100 \times 100 \mu\text{m}^2$. The RC time constant is determined by the total junction, pad, and fringe capacitance. Deleted from the above process are passivation, annealing, curing, antireflection, thinning, backside metallization, dicing, etc. The NIP / PIN mesa diameter can be in the range of 10-100 μm , and MS-PD / APD has less semiconductor material in the mesa compared to the conventional PD / APD, so it has less capacity, so can have a larger area mesa (or equivalently a larger photosensitive area) for the same data rate bandwidth compared to other PD / APDs, and therefore optical into MS-PD / APD signal alignment has a larger error margin, which further reduces the cost of packaging; 56 and 57, in the case of a hole having a period of 2000 nm and a diameter of 1300 nm in a square hole lattice, the capacity is the same as the case of mesa having the same diameter but the thickness of the i layer, and the fringe capacity is ignored. About 50% less than that of an equivalent structure. In the case of a hexagonal lattice hole with a period of 2000 nm and a hole diameter of 1300 nm, the area of the MS-PD may be about 35% larger than that of a PD without holes. Other gratings, periods, and hole diameters, holes for capacity reduction but not for absorption enhancement, to reduce capacity and / or increase absorption in, for example, MS-PD / APD structures or it can also be used to optimize. According to some embodiments, multiple periods and / or multiple hole diameters may be used. It is also possible to use holes that are spaced aperiodically.

FIG. 86 is a schematic plan view showing an MS-PD / APD integrated with a mutual impedance amplifier and / or other electronics on a single chip. On a single silicon chip 8600, an MS-PD / APD 8660 is shown connected to a TIA or other electronics 8690 using interconnect lines 8692. Although FIG. 86 shows a stand-alone MS-PD / APD that requires a bond pad to transmit electrical signals to other electronic components for further signal processing and transmission, FIG. 2 shows MS-PD / APD and electronics integrated on a chip. The bond pad adds unwanted capacitance, and this capacitance, along with the junction capacitance, is used to calculate the MS-PD data rate bandwidth. For example, an RC time with a bandwidth of 30 GHz (or about 30 Gb / s) is about 0.16 pF capacity and 50 Ω load resistance. A 30 μm diameter SiPIMP with a 2 μm i layer has a junction capacitance of 37 femtofarads (fF) with the i layer fully depleted by a reverse bias voltage. This allows a 90 $\mu\text{m} \times 90 \mu\text{m}$ bond pad on 2 μm polyimide to give a total capacitance of about 0.2 pF. If the MS-PD / APD is integrated with TIA and / or electronics, the bond pads are no longer used and the transmission line capacity from the MS-PD / APD to the TIA and / or electronics is reduced. Neglecting, the MS-PD / APD capacitance can be 0.16 pF, which is about 30 nm in diameter compared to 30 μm in diameter for a stand-alone device. The device becomes 60 μm . This increase in area increases the margin for optical beam alignment errors relative to MS-PD / APD and further reduces packaging costs. Including parasitic capacitance, the diameter of MS-PD is significantly larger than 30 μm of stand-alone MS-PD, and may be, for example, greater than 40 μm , and in some cases, greater than 50 μm in diameter. May be even larger.

It should be noted that, as described in this patent specification, a microstructured hole array (or column) having a diameter approximately the same (more or less) as the wavelength of light is a microstructured hole array (or absorption of photons over that of a similar substance that does not have a column). For example, in order for SiPIMP to operate at several tens of Gb / s, the thickness of the i layer must be about 2 μm , otherwise electrons and holes that are photogenerated carriers. In some cases, the run time of the system achieves a data rate bandwidth of tens of Gb / s and exceeds about 20% at a nominal wavelength of 850 nm, in some cases 880 nm, and in some cases 900 nm, is too long to have sufficient quantum efficiency above 30%. This is made possible with the techniques described herein using microstructured hole arrays (or columns), either with a single period and diameter and / or with multiple periods and diameters. The holes and / or holes (columns) of (or columns) can be periodic and / or non-periodic and the microstructure absorbs and / or emits. Can have a cross-sectional shape other than circular. In the absence of the microstructured hole array (or column), the 2 μm or less thick Si layer absorbs about 5% of 900 nm photons, while the microstructured hole array or column can be absorbed in excess of 20%, and in some cases it can exceed 50%. Furthermore, in some other cases, it is possible to exceed 40%, 50%, and 60% for 900 nm wavelength photons.

This is the same for Ge on Si, and by using this patent specification, for example, at wavelengths of 1550 nm and in some cases 1600 nm and in some cases 1700-1800 nm. Several tens of Gb / s data rate bandwidth can be achieved.

In known narrow wire photodiodes, there is no absorption enhancement such that a thin layer of about 2 μm or less over that of an equivalent bulk layer for high data rate bandwidths of tens of Gb / s. For example, a 2 μm long InP nanowire and a 2 μm bulk InP at wavelengths greater than the band gap are approximately equivalent, and the advantage of nanowire is only to reduce reflection.

FIG. 87 shows a simple epitaxial structure without any microstructure. The structure of FIG. 87 is used to compare with similar epitaxial structures with microstructures such as hole arrays for the absorption of incident photons having a wavelength range of 800-880 nm. For simulation purposes using FDTD (finite difference time domain), structures with microstructures without P and N contacts, mesa etching, passivation, planarization, and other processes to produce complete photodiodes. Only the structures that do not have are shown. The epitaxial structure in Case 1 is grown on a doped and thinned silicon substrate P8702 to about 150 μm , the first layer of which is about 0.2 μm thick using boron at $1 \times 10^{19} / \text{cm}^3$ / a Si intrinsic layer 8704 that is doped beyond cm³, then about 2 μm thick, intentionally undoped and having a doping level of less than $5 \times 10^{16} / \text{cm}^3$ And then a SiN layer 8710 having a thickness of about 0.3 μm and doping with a phosphorous dopant exceeding $1 \times 10^{17} / \text{cm}^3$.

FIG. 88 shows another simple epitaxial structure in which no microstructure is present. The structure of FIG. 88 is used to compare with a similar epitaxial structure having a microstructure such as a hole array with respect to absorption of incident photons in the wavelength range of 800-880 nm. For simulation purposes using FDTD (finite difference time domain), structures with microstructures without P and N contacts, mesa etching, passivation, planarization, and other processes to produce complete photodiodes. Only the structures that do not have are shown. The epitaxial structure in Case 2 is grown on a silicon substrate P8802 with a 2 μm buried oxide (BOX) layer 8804 on which a doping using boron with a thickness of about 0.1 μm is $1 \times 10^{20} / \text{cm}^3$ is SiP-layer 8806 has been extended and then the

layer 8816 which P doping is over $1 \times 10^{20} / \text{cm}^3$ Next, a Si intrinsic layer 8808 with a thickness of about 2 μm , which is not intentionally doped and has a doping level of less than $5 \times 10^{16} / \text{cm}^3$, and then with a phosphorous dopant with a thickness of about 0.3 μm and 1. This is a SiN layer 8810 doped in excess of $1 \times 10^{16} / \text{cm}^3$. For both Case 1 and Case 2, photons are incident from the top surface, ie the surface with the SiN epitaxial layers (8710 and 8810). For simulation studies.

FIG. 89 shows the same epitaxial structure as in FIG. 87 except that the microstructured hole array has been etched down to the SiP epitaxial layer according to some embodiments. In Case 3, the hole 8902 has a diameter of 1300 nm and a period of 2000 nm in a square grid array. Photons having a wavelength of 800-880 nm are incident on the upper surface, ie, the SiN epitaxial layer 8710. The N and P layers / substrates can be exchanged in certain applications and the absorption results are about the same.

FIG. 90 shows an epitaxial structure that is the same as in FIG. 88 except that a microstructured hole array has been etched into the BOXSiO₂ layer according to some embodiments. In Case 4, the holes 9002 have a diameter of 1300 nm and a period of 2000 nm in a square grid array. Photons having a wavelength of 800-880 nm are

incident on the top surface, i.e., the SiN epitaxial layer 8810. The N and P layers / substrate are interchangeable in certain applications and the absorption results are about the same.

Furthermore, the hole can be etched up to the etch stop layer SiGe8816. The etch stop layer 8816 is highly P-doped and can be used in a layer structure where a P layer and an etch stop layer are desired in the process, which can be used in photodiode and avalanche photodiode structures, is included.

91A-91E are plots showing the results of a simulation for the exemplary structure illustrated in FIGS. 87-90. FIG. 91A shows a comparison of cases 1-4 (FIGS. 87-90, respectively), in which case "1" is: each case for wavelengths shown over 800-900 nm using FDTD simulation. The absorption due to the intrinsic layer is calculated. In each case, the photons are incident on the top surface, the NSi epitaxial surface (layers 8710 and 8810 in FIGS. 87-90). Absorption due to other layers other than the "I" layer is not included. Curves 9110, 9112, 9114, 9116 show the results for cases 1, 2, 3, 4 (shown in FIGS. 87, 88, 89, 90), respectively. In cases 1 and 2, no microstructure is present and the absorption in the I layer is less than 40%. That means that 40% of the incident photons have been absorbed. In case 1 it is less than 15% and in case 2 it can be just less than 40%, for example at a certain wavelength of 885 nm and less than 20% at the longer wavelengths 890 nm and 900 nm. And less than 10% at 885 nm. Absorption is directly proportional to quantum efficiency. This is because photons are absorbed and converted to electrons and holes, which are then swept out of the "I" region under a bias voltage that depletes the "I" region. This is because when they are not coupled, these photogenerated electrons and holes swept to the N and P regions, respectively, contribute to the photocurrent, in cases 3 and 4, which contain microstructured holes with a diameter of 1500 nm and a period of 2000 nm in a square grating, an absorption level close to 100% is seen at certain wavelengths. In both cases 3 and 4, the absorption is greater than 40% at wavelengths between 890 and 900 nm. In the 800-850 nm range, it is an absorption greater than about 70%. In case 4, the absorption is better than 70% at 850 to 900 nm. At 855 nm in Case 4, the absorption is over 90%, which is in contrast to Case 2, which is less than 10%. The percentage of absorption in the "I" layer in the case of microstructures increases for high absorption at certain wavelengths, eg by changing the hole diameter, period and / or grating, eg from square to hexagonal grating or it is possible to optimize.

In the case of a silicon PIN photodiode with a microstructure as described herein, it has been found that the absorption does not necessarily decrease when the wavelength approaches 1.11 eV silicon band gap at 800 K, i.e., about 1117 nm. In comparison, for a PIN (or NIP) photodiode without a microstructure, the absorption decreases as the wavelength approaches 1117 nm. This increases the Q (quality factor) of the microstructure resonance and / or coupling resonance as the optical loss is reduced, so that more time is spent as the photons bounce back and forth within the microstructure. As a result, it is considered that the absorption may exceed 50% even when the wavelength approaches 1117 nm. The refractive index difference within the microstructure can be expressed as an effective index. For example, since the hole removes silicon material and is replaced, for example, with air, the effective index, or effective refractive index, of the region with the hole is less than the refractive index of the region without the hole. A simple estimate is the average of the refractive indices, but, for example, if the hole removes half of the silicon in the region where it has a hole, assuming that the hole is filled with air, its effective refraction The index is about $(1 + 3.44) / 2 = 2.22$, where the refractive index of bulk Si is about 3.44 at a wavelength of 1000 nm. Thus, the region with and without holes will see a refractive index discontinuity of approximately 1.22, is a refractive index change of about 35%. This discontinuity in refractive index may result in a high contrast grating with a Q that can approach 1,000,000 or more when the optical loss is low. This can explain the improved absorption in microstructured photodiodes and / or avalanche photodiodes. If photons stay in the microstructure for a time approaching the characteristic time, which is the transit time and RC time of the photodiode / avalanche photodiode, this will adversely affect the data rate bandwidth of the PD / APD. start. However, if the data rate bandwidth is low, a higher Q can be tolerated. The Q factor is defined as being proportional to the energy lost per stored energy / cycle. This is a probable explanation for improved absorption in the microstructure. The microstructure is composed of a lattice and thus is composed of a number of unit cells or cells, each having its set of resonances and closely coupled. Unlike a conventionally known resonant photodiode, which is a single resonator, its resonance is a sharp peak or valley and shows only a single resonance characteristic which is a periodic wave function. The structure has a region in the absorption for which the absorption varies slowly, for example, for wavelengths that vary by less than 10% over a wavelength range, for example 50-100 nm, and an aperiodic wave function. The microstructure PD / APD has a turn of a plurality of resonances, and thus has peaks and valleys that are not so conspicuous as compared to a conventionally known resonant photodiode. An aperiodic hole can also have a resonant cell that is itself aperiodic and can couple to an adjacent neighbor cell, which improves absorption and / or emissions. The coupling type resonance structure is possible.

As a rough estimate, the characteristic time is about 20 ps for about 20 GHz 3 dB bandwidth. At 20 ps, the light travels about 2000 μm in silicon, which means that the light can bounce about 1000 times in a 2 μm microstructure, so a 2 μm thick "I" layer is at an equivalent optical length. Meaning that it can be as thick as 2000 μm , so in the microstructure described in this patent, the light will bounce more and be improved above the bulk absorption coefficient. It is possible to give an effective absorption which can be written approximately as effective absorption = bulk absorption * number of bounces in the microstructure. The time that light spends in the microstructure is called optical transit time, which is another basic time for the MS-PD / APD. The sum of these three basic times, i.e., RC time, travel time, and optical transit time, squared, gives the square of the total time. For example, $T(\text{total time})^2 = T(\text{RC time})^2 + T(\text{travel time})^2 + T(\text{optical transit time})^2$. In the case of 20 GHz, the total time may be 20 ps and is simple. For simplicity, assuming that RC time, travel time, and optical transit time are all the same, each time may be only about 11.5 ps. 11.5 ps for the optical transit time is converted to an equivalent optical length of about 1000 μm , i.e. the optical transit time is longer than 11.5 ps, assuming that all three basic times are equal in some cases, the improved effective absorption length may be a Q of 1000 μm or approximately 250 before it begins to degrade the bandwidth of the MS-PD.

FIG. 91B shows the epitaxial structure in FIG. 90 (case 4) when the microstructured hole array is etched to different depths. Curve 9120 shows the absorption in the "I" Si layer as a function of wavelength from 800 to 900 nm when holes are etched into the SiO₂ layer 8804. Curve 9122 shows absorption versus wavelength for holes etched into the SiGeB layer 8816. In both cases, light is incident from the top or SiN surface 8810. Although the peaks and valleys are shifted, the overall etching to the SiO₂ layer is better than the etching of holes to the SiGeB layer at most wavelengths in the 800-900 range.

FIG. 92 is a schematic diagram illustrating a microstructured region in silicon when holes are etched into silicon, according to some embodiments. The exemplary structure includes a SiP substrate 9202, a SiP layer 9206, a Si layer 9208, and a SiN layer 9210, all of which have thicknesses and doping levels as shown. Hole 9222 is etched to a depth of about 2.3 μm and has a diameter of 1500 nm and a period of 2000 nm in a square grating. Region here there shown schematically dotted circle 9208 has an effective refractive index n_{eff} . It is smaller than the refractive index of the bulk Si is about 3.44 in 300K at 1000nm wavelength. This assumes that the etched region is in air, vacuum, or filled with a material such as polyimide having a refractive index lower than that of silicon. For the dimensions described above for the microstructure, the effective refractive index in the region with holes is approximately given by the air portion $0.44 \times 1 + \text{Si portion } 0.56 \times 3.44$, which is about 2.36. For example, photons incident on the upper surface 9210 are trapped in the microstructure and bounce between the two refractive index discontinuities. One discontinuity is the interface between air and microstructure, where the refractive index difference is about 1.36, and the other discontinuity is the interface between microstructure and silicon. The refractive index difference there is about 1.07. This refractive index difference makes it possible to view the microstructure as lossy high contrast grating, which can explain the improved absorption observed.

FIG. 93 is a schematic diagram illustrating an MS-PD structure with tapered holes, according to some embodiments. The tapered funnel-shaped hole 9322 gradually changes in the effective refractive index n_{eff} , which has no significant change in the hole diameter but is smaller than that in region 1. For example, the effective refractive index n_{eff} . The effective refractive index in region 1 is much smaller than the effective refractive index in region 2 due to the fact that it is much smaller than for the region it has, in which case it is simply less silicon material there. In region 1, the effective refractive index near the surface can be 40% or more voids (air or a low refractive index material such as polyimide) and 40% or less silicon, which The reflection is lower with respect to photons incident perpendicularly to the upper surface (in this case, the SiN layer). For photons incident off the vertical, the reflection may be even lower. As a further example, if the hole occupies 80% or more near the surface and Si occupies 10% or less, the Fresnel reflection for normal incidence photons is 1% or less, it may be. As the diameter of the hole gradually decreases with depth, the

effective refractive index in region 1 gradually changes. Although the illustrated example is a funnel, it can be, for example, simply a step with two separate hole diameters, or a plurality of hole diameters with each step diameter becoming smaller as the step moves away from the surface. It is possible to have a plurality of steps.

FIG. 94 is a schematic diagram illustrating an MS-PD structure with progressively tapered holes, according to some embodiments. Another configuration is illustrated with a hole 9422 having a gradual funnel shape extending over the entire length of the hole. Its effective refractive index also increases gradually as a function of depth. According to some embodiments, the holes can be provided with pseudo-random or random holes having multiple diameters, periods, and / or different lateral shapes. Various hole parameters can be used to improve or optimize the absorption characteristics in certain wavelength bands. According to some embodiments, the holes 9422 can be provided with a series of steps, each step having a different diameter. These steps can be uniformly spaced and / or non-uniformly spaced. Their spacing may be a quarter-wave, half-wave, or four to improve or optimize the absorption characteristics in a particular band of wavelengths, for example, to form a filter or coupled resonator. It can be a fraction of a half wavelength and a half wavelength. In the case of optical emitters, such a step in the diameter of the hole or column can improve, for example, the overlap of the light wave with the gain medium. According to some embodiments, the funnel shape of the hole 9422 can have any shape. For example, it can be V-shaped and the effective refractive index at the air-hole interface and at the hole-silicon interface can be optimized to improve reflection and absorption properties or emission properties.

Another explanation for the absorption enhancement associated with the microstructured PD / APD is that the microstructure is a metamaterial and can act as a broadband absorber. For example, G. Deval et al. "Broadband infrared metamaterial absorber with visible transparency using ITO as ground plane", OPTICS EXPRESS 18104 June 2014, N. Lie et al. "Infrared Perfect Absorber and Its Application As Plasmonic Sensor", Nano Lett., 2010, 10, 2342-2348, and L. Meng et al. "Polarization-sensitive perfect absorbers at far-infrared wavelengths", Optics Express, A111 Dec 2012 (hereinafter "Meng et al."), all of which are incorporated herein by reference.

For example, Meng et al. in the case where the plurality of grooves are intersected by a crossbar pattern, the absorption is polarity independent. Instead of long grooves, as disclosed herein, Meng et al. Au in the substrate is replaced by a semiconductor such as silicon and / or germanium, and the hole / groove is a void, which is an air, gas, vacuum, polyimide, and / or any coating that partially or completely covers the hole. It is possible to use a dielectric material. In particular, Meng et al. in FIG. 11, when the structure is a cross bar, a square array of dielectrics exists on the Au substrate. According to some embodiments, Au is filled with a semiconductor and a dielectric material such as air, gas, or silicon dioxide, silicon nitride, calcium fluoride, spin-on-glass, polyimide, or a passivation dielectric. It is replaced with a dielectric that has holes. Meng et al. FIG. 11 also shows absorption with respect to wavelength.

High contrast gratings can be considered a class of metamaterials. This, along with other effects, may be able to explain the observed absorption enhancement. Other effects include plasmons, nonlinearities, sub-wavelength and near-wavelength effects, photonic crystals, slow waves, coupled resonances, interference, field enhancement, and resonances with losses.

FIG. 95 is a schematic diagram illustrating a material structure with microstructured holes of different diameters, according to some embodiments. Holes 9522 and 9524 have different diameters. Smaller diameter holes remove less silicon material than larger diameter holes if the period is approximately the same. The effective index of the array of smaller diameter holes 9522 is the effective index n_1 and these holes can be clustered near the center of the MS-PD / APD. An array of larger diameter holes 9524 has an effective refractive index n_2 and can be clustered around the smaller diameter holes (e.g. in a ring-shaped pattern). For example, n_1 is greater than n_2 because less material is removed in the smaller diameter hole 9522 than in the larger diameter hole 9524. The light is guided into the n_1 region, so when light bounces back and forth between the hole / silicon (in this example P silicon) interface and the hole / air interface, for example due to diffraction. The amount of light lost is minimal. Further, the mesa etch removes most if not all of the N silicon layer and the "I" silicon layer in region 9530. Mesa 9540 is etched to define the capacity of the NIP junction as shown in this example. In some cases, ion implantation and / or diffusion can be used to define the NIP junction capacitance. And in some cases it is only necessary to remove only the NSI layer and / or convert it to low or opposite doping. The N and P can be exchanged, for example, MS-PD can be PIN and MS-APD can be NPNP or PNPN.

FIG. 96 shows a plan view of a material structure with microstructured holes of different diameters as illustrated in FIG. As can be seen, the smaller diameter holes 9522 are clustered within the larger diameter hole 9524. The resulting effective refractive index difference between the regions near the center of this microstructured photodiode / avalanche photodiode (MS-PD / APD) 9530 is more guided to the region where the light has a higher effective refractive index. The same light guiding effect as an optical fiber is generated. Also shown is a mesa 9540 defined by the etched away region 9530, which can further provide a light guiding effect. The mesa 9540 may also define a NIP junction capacitance and simply be etched completely through its N layer, "I" layer, or up to the P layer. Those not shown are ohmic contact metals, bond metals, passivation, planarization, polyimide, and other dielectrics. The numerical aperture of the MS-PD / APD adjusts the diameter of the holes in the core area (smaller diameter holes) compared to the cladding (larger diameter holes) according to some embodiments. It is possible to adjust by. To change the effective refractive index, the hole density and diameter are methods for adjusting the amount of silicon material in a region.

According to some embodiments, a guide structure having a higher refractive index core and lower refractive index cladding may be used to reduce or maximize optical loss due to diffraction, for example. It is possible to operate effectively as a light guide such as an optical waveguide. For example, a square hole grating with a period of 2300 nm and a hole diameter of 1500 nm can have an approximate effective refractive index of 2.63, and a square grating with a period of 2000 nm and a hole diameter of 1500 nm is approximate. The effective refractive index can be 2.36. A higher refractive index can be on the core side and a lower refractive index on the cladding side. A refractive index difference of about 10% between the core and the cladding can be achieved by changing the period of the square grating. Other combinations are possible. The cladding can have a hexagonal grid and the core can have a square grid, in which case the period and diameter can remain the same or can vary.

97A and 97B are graphs showing absorption with respect to light incident on a microstructure having a layer structure as shown in FIG. 92A. Holes are etched in the hexagonal and square grid arrays with a diameter of 1500 nm and a period of 2000 and 2500 nm, respectively. Curve 9712 is for a square grid with the same period and hole diameter. Its absorption is over 80% at wavelengths of 1.4 to 1.6 μm and over 90% for a hexagonal lattice at 1.55 μm . Curve 9714 is absorption without a microstructured hole, giving 10% or less absorption and only 1.5% absorption at 1.55 μm . Furthermore, for a hexagonal lattice, the absorption varies by less than 10% over the wavelength range of 1450 nm to 1600 nm. FIG. 97A also shows data and communication bands, S, C, L, U / XL. In the case of the structure as in FIG. 92A, MS-PD / APD can be used in all these bands from S to U / XL.

In FIG. 97B, curve 9720 shows the absorption for a wavelength of a hexagonal hole grating with a period of 2500 nm and a hole diameter of 1500 nm; and curve 9722 is for a square grating with the same period and diameter. It is less optimal, but at 1.55 μm wavelength, its absorption exceeds 90%. Curve 9714 is also shown for reference.

Absorption and quantum efficiency are directly proportional, and about 90% absorption with minimal reflection may be equivalent to about 90% quantum efficiency. For example, the external quantum efficiency can be defined as $QE = (1-R) (1-e^{-\alpha x})$, where R is the reflection from the surface of the MS-PD / APD, α is the absorption coefficient, X is the absorption length. Absorption can be given by $(1-e^{-\alpha x})$, which is the amount of photons absorbed at the absorption coefficient α and length x. The 90% absorption at 1.55 μm wavelength is converted to the product of the absorption coefficient and the absorption length, and αx is equal to about 2.3. If a bulk absorption coefficient is used, α is about 50 / cm since α is 460 / cm at 1.55 μm wavelength. Compared with the physical length of 2.2 μm of 0x, the light has passed through the absorption region about 23 times. Equivalently, if the physical absorption length is 2.2 μm , the improved effective absorption coefficient is about 10455 / cm at 1.55 μm wavelength, while the bulk absorption coefficient at 1.55 μm wavelength is about Contrast with 460 / cm. This also indicates that the improvement is about 23 times.

Furthermore, the quantum efficiency directly proportional to absorption is high over the range of data / telecommunications wavelengths. Standard bands are D (1460-1530 nm), C (1530-1565 nm), L (1565-1625 nm), and U / XL (1625-1675 nm). Other bands not shown can also have high absorption efficiency, such as O (1260-1360 nm) and E (1360-1460 nm). A single microstructured Ga-on-SiPC / APD can cover the entire data / telecommunications wavelength spectrum. For example, see Basca, "From C to L: The Future of Optical Wavelength Bands", www.greenbandproperties.com, GREENBAND PROPERTIES, June 2008. Well, that is incorporated into this book by citation.

FIG. 99 illustrates another preferred epitaxial structure for a Si avalanche photodiode for operation in the wavelength range of 800 to 1000 nm, based on some embodiments. In particular, the structure shown has been found to work very well around 850 nm with a 30 nm and for data rates of 5-40 Gb/s or higher where much of the data communication takes place. A microstructure is used to improve absorption, which can be either an improved absorption coefficient or an improved absorption length. The ASi substrate 9902 can be thinned to 150 μm after device processing. As an epitaxial layer, for example, an N contact with a thickness in the range of 0.1-4 μm and in some cases in the range of 0.3-2 μm and a doping exceeding $1 \times 10^{18} / \text{cm}^3$ nSi layer 9906, which is a layer, and also known as an avalanche layer with a thickness ranging from 0.2 to 1 μm , in some cases 0.5 μm and a background doping of less than $1 \times 10^{16} / \text{cm}^3$ A Si intrinsic or "I" layer 9918, which is a gain or gain layer, and a thickness of 0.02 to 0.3 μm , in some cases 0.1 μm and a doping of $1-6 \times 10^{17} / \text{cm}^3$ P Si layer 9920, which is a charge layer that is in the range of $1 / \text{cm}^3$ and in some cases $1.8 \times 10^{17} / \text{cm}^3$, and in some cases in the thickness range of 0.2 to 4 μm is a Si intrinsic "I" layer 9908, an absorption layer with a background doping of less than $1 \times 10^{16} / \text{cm}^3$, and a thickness of 0.1 to 2 μm and in some cases 0.5 μm and a P Si layer 9910 which is larger than $1 \times 10^{20} / \text{cm}^3$ and is a P contact layer.

FIG. 101 shows another suitable epitaxial structure for a Ge on Si avalanche photodiode for operation in the wavelength range of 885-1700 nm, based on some embodiments. In particular, the structure shown has been found to work well for data rates of 5-40 Gb/s or higher around 1550 + 200 nm where much of the telecommunications occurs. The microstructure can be used to improve absorption, which can be either an improved absorption coefficient and/or an improved absorption length. The NIS substrate 10102 can be thinned to 150 µm after device processing. The epitaxial layer has a thickness in the range of 0.4-4 µm. In some cases 0.3-2 µm and an NIS layer 10106 that is an N contact layer with a doping greater than $1 \times 10^{19} / \text{cm}^3$. A multiplication factor also known as an avalanche layer with a thickness in the range of 0.2 to 1 µm. In some cases 0.5 µm and a background doping of less than $1 \times 10^{16} / \text{cm}^3$ Si intrinsic or I^+ layer 10118 as a gain layer and a thickness in the range of 0.02 to 0.3 µm. In some cases 0.1 µm and a doping of $1-6 \times 10^{17} / \text{cm}^3$ a PSI layer 10120 which is a charge layer of cm^3 in some cases $1.8 \times 10^{17} / \text{cm}^3$ and a thickness in the range of 0.3 to 4 µm and in some cases 2 µm and Backy The Ge intrinsic I^+ layer 10138. Worked doping is an absorber layer is less than $1 \times 10^{15} / \text{cm}^3$ a 0.2µm when thickness of several in the range of 0.1 to 2µm and a PCLayer 10110 which is a P contact layer with a doping greater than $1 \times 10^{20} / \text{cm}^3$. Other it is possible to grow a low temperature Ge buffer layer at the interface between Si and Ge, prior to normal Ge epitaxial growth. In this regard, see, for example, Kang et al. cited to seek.

103 (A)–(C) show the diameter, period, and other parameters for microstructured silicon and germanium-on-Si photodiodes and avalanche photodiodes based on some examples. FIG. 103 (A) is a table showing various parameters used. According to some embodiments, both hexagonal and square grids can be used. Other lattice and / or non lattice arrangements of holes are possible, but are not shown. Mesa dimensions of 10, 25, 30, 40, 50, 60, and 80 μm are used to achieve capacity to support data rates of 5 to over 80 Gb / s. According to some embodiments, other methods of defining junction capacitance, such as ion implantation or diffusion can be used to deplete centers. The hole diameter and period for the operation of Si microstructured PDs and APDs in the wavelength range of 800–1000 nm, especially in the range of 850 nm $\pm$ 30 nm, for example 1310/2000, 1500 for either hexagonal and / or square gratings. / 2000, 700/1000, 630/900 (diameter / period in nm). In the case of Ge-on-Si microstructured PDs and APDs, examples of hole diameter and period combinations for either hexagonal or square gratings for operation in the wavelength range of 800–1700 nm, especially 1550 nm $\pm$ 200 nm, includes 1300 nm / 2000 nm, 1500 nm / 2000 nm, 1500 nm / 2500 nm, 1900 nm / 2500 nm. Other hole diameters and periods are possible. Absorption better than 90% and in some cases better than 70% or 80%, can be achieved with these diameters and periods of wavelengths of 800–1600 nm and 600–1700 nm, is there. FIG. 103 (B) and FIG. 103 (C), "d" is shown as a period for hexagonal and square lattice patterns. Although circular holes are illustrated, non-circular holes such as ellipses, rectangles polygons, and other irregular shapes are possible. Circular holes are only selected for simplicity of simulation using FDTD

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Hexagonal lattice, 1500 nm hole diameter, 2000 nm hole period, in which case the holes are etched into the SiN layer. In this simulation, the wavelength is centered on 1500 nm $\pm$ 10 nm (curve 10490 in FIG. 104A) and 1550 nm $\pm$ 1 nm (curve 10412 in FIG. 104B). The simulation mesh is finer than 0.1 nm, and from the curve 10412 in FIG. 104 (B), the absorption is higher than 0.9 (90% absorption) and 0.95 (absorption) over the wavelength 1540 to 1551 nm. It can be seen that the variation is less than 10% with a low absorption value exceeding 95% absorption. This property of absorption with respect to wavelength is important in optical telecommunications applications, in which case there is no rapid change in absorption within 2 nm of wavelength variations centered around 1550 nm, for example. A curve 10410 in FIG. 104A shows an absorption fluctuation of 0.8 to 0.99 exceeding a wavelength fluctuation of 20 nm centered on 1550 nm. Over any 2 nm wavelength variation, the absorption variation is less than 15%. In some cases it is less than 5%. The channel spacing in wavelength division multiplexing (WDM) for coarse WDM can be 2 nm or greater, while for dense WDM, the channel spacing is 0.8, 0.4 or less. Thus, for example, at 1550 nm, 3 or more channels can fit within the 2 nm spectral width, while for coarse WDM, 4 nm or more is required. Is done.

FIGS. 105A and 105B relate to eigenmodes for a square grid hole pattern, based on some embodiments. FIG. 105A shows a single unit cell 10510 in a square lattice arrangement. FIG. 105 (B) shows various 2D eigenmodes (stationary mode, standing wave mode, resonance mode) (from FDTD simulation using Maxwell equations) in a unit cell of a microstructured hole in Si (or Ge) material. Yes, The waves propagate, for example, between the air / semiconductor interface and the Ge / Si interface along the length of the microstructured hole array. A waveguide and / or resonator is defined by the region where the microstructured hole is etched. Semiconductor and hole lengths in the unit cell can be thought of as optical waveguides and / or resonators, and many parallel optical waveguides / resonators of adjacent unit cells can be combined to form: 2D it can be a coupled wave in the array, a coupled mode, and / or a coupled resonator. High contrast grating (HCG), photonic crystal, slow wave effect and coupled waveguide / resonator eigenmode, supermode, field enhancement, linear and nonlinear effects, transverse mode, guided resonant modes. The combination of the Bloch mode, and the combined Bloch mode can produce an observed improvement in the "ax" product in the equation for quantum efficiency proportional to absorption $(1 - e^{-\alpha x})$. Where α is the bulk material absorption coefficient and x is the absorption length. If α is constant, it is possible to improve x , if α is constant, it is possible to improve x , and in some cases between α and x it is possible to improve both. FIG. 105 (B) shows many complex eigenmodes of the unit cell 10510 of the square lattice in FIG. 105 (A). Each cell in the square grid can have any one or more of these eigenmodes and can be combined with the eigenmodes of adjacent cells, with a large amount of all these cells. The combined mode is called super mode. This large amount of coupling may result in a "smoother" absorption characteristic for the wavelength, even smoother in a certain wavelength range, eg 50 nm in some cases and 80 nm in some cases and 100 nm in some cases. Or, more than that, it can be defined as the variation in absorption properties over 10%.

FIG. 106 is a schematic diagram illustrating a microstructured hole in two square grids arranged in an overlapping manner according to some embodiments. A dotted square 10610 represents a unit cell of a square lattice having D1 as a hole diameter. Dashed square 10612 represents another square lattice with a similar period but D2 as the hole diameter, and D1 and D2 are not equal. If D1 is equal to D2, it is a square grid (tilted by 45 degrees). Or, equivalently, if the period of these two square gratings is similar, it can also be considered as a hexagonal grating with two different hole diameters. The grid pattern can have more than two different hole diameters, for example, three different hole diameters in a hexagonal grid. For example, in one preferred microstructure consisting of a plurality of holes, D1 can be 1300 nm in diameter and the square grating can have a period of 2000 nm. One advantage of having more than one hole diameter in a microstructure array is that the absorption curve with respect to wavelength is further flattened so that the variation in absorption is the wavelength for microstructured PD / APD configured in Si. Can be less than 20% for a wavelength of 1250-1750 nm for a microstructured PD / APD that spans 800-950 nm and is configured in Ge-on-Si as in FIG. It is, in some cases, the variation is less than 10% variation over these wavelength ranges, and in some cases less than 5%. It is also possible to improve the quantum efficiency of the microstructure PD / APD as a whole or equivalently.

Interspersing different hole diameters results in a quantum efficiency directly proportional to absorption at a wider range of wavelengths, particularly 800-950 nm for microstructured PD / APD in silicon and microstructured PD in Ge-on-Si / Allows further flattening over 1000-1800 nm for APD. Other hole diameters and periods are possible according to some embodiments.

Some embodiments improve the quantum efficiency of PD / APD when the bulk absorption coefficient is insufficient to maintain adequate quantum efficiency within design parameters such as the thickness of the absorbing material, for example, improvements in the absorption of microstructured holes and / or pillars used to make it possible to apply to other devices that use photon absorption such as solar cells, imaging sensors, radiation absorbers, etc. is there.

FIG. 107 is a schematic diagram showing an epitaxial structure of Ge-on-Si according to some embodiments. The structure is similar to that illustrated in FIG. 102A, but is grown on a 0.2 μ m (or 0.1-2 μ m range) SiN layer 10706 with N doping exceeding $1 \times 10^{19} / \text{cm}^3$. A Si layer 10718 with a background doping (which can be either N or P) of $1-5 \times 10^{16} / \text{cm}^3$ and a thickness of 0.1-0.5 μ m is added, and then intentionally is undoped, has a background doping of less than $5 \times 10^{16} / \text{cm}^3$, in some cases less than $5 \times 10^{15} / \text{cm}^3$ and a thickness in the range of 2 μ m or 0.5-2.5 μ m. Followed by a Ge layer 10709. The PGE layer 10710 is at the top, the doping is over $1 \times 10^{19} / \text{cm}^3$ and the thickness is in the range of 0.2 μ m or 0.2-0.5 μ m. All of these layers are grown on the HSi substrate 10702. The microstructured hole array 10722 can be formed using the parameters shown in FIGS. 103 (A)-(C). According to some embodiments, the hole diameter is 1300-1500 nm and the period is 2000 nm in a hexagonal or square grating, according to another embodiment, a layout as shown in FIG. 106 is used. In such a case, the holes having a plurality of diameters can be, for example, 1300 nm and 1550 nm square lattices with a period of 2000 nm that are nested in each other as shown in FIG.

The Si layer 10718 is used to lower the dopant in the Si so that dopant diffusion into the Ge layer 10709 is reduced or minimized to allow the Ge layer to grow.

According to some embodiments, the structure shown in FIG. 107 is for a micro structure type PD, and as shown in FIG. 101, it can be used for a micro structure type APD with a multiplication layer and a charge layer added. It is: The wavelength range for this structure is 800-1700 nm, and can be in particular about 1550 nm $\pm$ 200 nm.

The added Si "T" layer 10718 also contributes to reducing the capacity of the device. This is because the "T" layer is now the sum of the Ge layer and the Si layer. The decrease in capacity helps to increase the modulation bandwidth of PD / APD. The Si "T" layer may in some cases have a thickness in the range of, for example, 0.1 to 3 μ m. Hole 10722 can be etched, for example, to the Si "T" layer and / or in some cases can be etched into the Si "T" layer.

FIG. 108 is a schematic diagram showing the basic features of a Ge-on-Si microstructured photodiode based on some embodiments. The structure is similar or identical to that shown in FIG. The MS-PD has been found to work well in the 1300-1700 nm and 600-1300 nm wavelength ranges. As shown, light is incident from the top surface, where the hole array is etched. With some minor changes, if an opening is made in the N atomic contact 10832 on the bottom and the bottom of the Si substrate 10702 is polished with an anti-reflective coating, light can also be incident from the bottom of the substrate. Further, vias (not shown) can be formed on the bottom of the Si substrate 10702 so that a guide can be provided to align the optical fiber with the microstructured PD. In this example, hole 10722 is etched down to Si layer 10718. According to some embodiments, the holes can be etched into or through the Si layer, or not penetrated through to the Si layer. The hole array can have a plurality of hole dimensions and a plurality of periods, and can be non-periodic. The hole diameter can be in the range of 500-1700 nm and the period can be in the range of 1000-2500 nm. According to some embodiments, the hole diameter is 1300 and 1550 nm and the period in a square or hexagonal lattice is 2000 nm. Further, the 1300 and 1550 nm holes can be in a square grid with a period of 2000 nm nested within each other as shown in FIG. The hole diameter and period may vary by 10-50 nm and in some cases by 50-100 nm. Not shown is a passivation layer, which may have a thickness of 2-100 nm on the semiconductor wall. Passivation can be used in the high field region of the exposed mesa to reduce leakage current. A reverse bias of -2 to -12 volts is applied between P contact 10828 and N contact 10830 (and / or 10832). Reverse bias means that a negative voltage is applied to P (anode) relative to the N (cathode) contact. A voltage shown with or without a negative sign means that it is negative at the anode relative to the cathode. Furthermore, the plurality of holes can have different shapes, and not all have to be circular.

it is known to use nanowires in photodetectors. The nanowire is 10^6 and the photodetector is shown to be limited to approximately 30 GHz 3-dB modulation bandwidth in the frequency domain for Gaussian transformation, or 14 ps response time. V.J Logezwaran et al. "A 14 ps full width at half maximum high-speed photodetector fabricated with intersecting InP nanowires on an amorphous surface", Applied Physics, A81, 1-5 (2008) (hereinafter "Logezwaran et al."), which is incorporated herein by reference. Logezwaran et al., The incident photon was at 780 nm and the InP absorption coefficient at about 780 nm was about 35000 cm^{-1} , and neither improvement in absorption nor absorption length was required. Similarly, in another known technique, 850 nm photons are incident on the nanowire and the absorption coefficient of GaAs at about 850 nm is about 12000 cm^{-1} , again requiring improved absorption and / or length it wasn't. MA Szevali et al. "Efficient Schottky-like junction GaAs nanowire features with GHz modulation bandwidth with large active area", Applied Reference may be made to Physics Letters (APPLIED PHYSICS LETTERS), 105, 041105 (2014), which is incorporated herein by reference. In contrast, according to the techniques described herein, high speed photodiodes / avalanche photodiodes are described with ps response times and / or modulation bandwidths of 5 Gb / s or higher. For Si at 850 nm, the absorption efficiency is about 700 cm^{-1} and a quantum efficiency of 40% or better is achieved using improved absorption and / or absorption length. Similarly, at about 1550 nm for Ge, its absorption efficiency is about 450 cm^{-1} , which also uses enhanced absorption and / or absorption length.

For example, in the case of a 2 μm thick absorbing "Y" layer for typical high speed or high modulation bandwidth PD / APD for operation at about 10-30 Gb / s (the "Y" layer is the PG / APD About 13% of the photons at 850 nm are absorbed without improvement. For example, if the microstructured hole array (or column) described in this patent application has an absorption enhancement and / or absorption length that is about 12 times or more, then more than 80% of the photons can be 2 μm Can be absorbed at a physical "Y" absorption length. Adding microstructured holes and / or pillars when using weakly absorbing (about 1000 cm^{-1} or less) materials such as Si and Ge at data communication wavelengths and telecommunications wavelengths of 850 and 1550 nm, respectively. Absorption or absorption coefficient and / or absorption length, the material is strongly absorbing (approximately 2000 cm^{-1} or more) and the microstructured PD / APD is high speed or high modulation bandwidth data and telecommunications applications and systems. It has been proved here that it is possible to improve to the point that it can be used for.

In some cases, only about 40% absorption is sufficient for some optical data / telecommunications, and only about a 10x-fold increase in absorption and / or absorption length, eg. at 850 nm is needed only for a 2 μm Si "Y" layer, or an enhancement factor of 4.5 times the absorption coefficient or length for Ge at 1550 nm wavelength for a 2 μm Ge "Y" layer. Not too much. Higher enhancement factors are possible, with factors greater than 10 and in some cases greater than 20 and in some cases greater than 40. As the absorption coefficient of the semiconductor bulk material becomes smaller, the improvement coefficient becomes larger, 100 or more.

Absorption of Si nanowires is described in Lu Hu, Gang Chen, Nann Lei, "Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications", Vol. 7, No. 11, 2007 (hereinafter referred to as "Lu et al."), which is incorporated herein by reference. Absorption at 1.4e eV corresponding to 850 nm is not improved, compared to thin Si films, and for wavelengths above about 2.25 eV, ie about 550 nm or shorter, absorption is comparable to thin Si films. Improved. Hu et al. Added, "On the other hand, in the low frequency range, the extinction coefficient of silicon is so small that improvement cannot be achieved".

Similar conclusions have been reached in other publications, namely Chendi Lin, Michelle L. Provini, "Optical absorption enhancement in silicon nanowire arrays with a large lattice constant for photovoltaic applications", Vol. 17, No. 22 / OPTICS EXPRESS, 19371, October 26, 2009 (hereinafter referred to as "Lin et al."), which is also incorporated herein by reference. Lin et al. Shows an improvement in absorption resonance at about 1.5 eV, which is described in Lin et al. Is based on a guide resonance mode or a slow Bloch mode that increases the electromagnetic field strength in the nanostructure. Lin et al. States "Coupling of incident light from the air into the high Q leakage mode of 2D periodic structures". High Q mode sharp resonances are undesirable in the use of photodiodes for data and / or telecommunications applications. For example, JD Schaub et al. "Resonant-Cavity-Enhanced High-Speed Si Photodiode Grown by Epitaxial Lateral Overgrowth", IEEE Photonics Technology Letters, Vol. 11, No. 12, December 1999 (hereinafter referred to as "JD Schaub et al."). The literature is incorporated into this book by citation. Schaub et al. Shows a quantum efficiency of at most 40% at a wavelength of about 800 nm (see, for example, FIG. 3 in Schaub et al.). However, its sharp resonance is not desirable. This is because drift in transmitter wavelength due to temperature (eg 0.3 nm / degree for some diode lasers and laser internal temperature due to Joule heating and environment is (which may change as much as 80 ° C, or more) may cause significant changes in quantum efficiency, for example. Previously known resonant photodiodes with sharp resonances may also be temperature sensitive in terms of peak resonant wavelengths where quantum efficiency is highest. Furthermore, laser sources often have variations in laser wavelength due to manufacturing variations, and it is not desirable that the laser must be precisely matched in wavelength to the photodiode. Variations in the manufacture of resonant photodiodes can result in resonant peaks at varying wavelengths. This reduces yield and increases the cost of the optical system as it is necessary to maintain careful testing and temperature stability due to the need to match the wavelength of the laser source and detector. It will be.

Recent publications, Rui Ren, Yong-Xin Qiu, Ji-Hong Zhu "Enhanced absorption in elliptical silicon nanowire arrays for solar energy harvesting" Optical Engineering, Engineering, 53 (2), 0270102 (February 2014) show similar results that the improvement at 1.5 eV is weak or non-existent but the absorption at higher energy is much stronger. This document is incorporated by reference.

Donnelly et al., "Mode-based analysis of silicon nanohole arrays for photovoltaic applications", Vol. 22, no. 35, OPTICS EXPRESS, A1343, August 25, 2014 (hereinafter referred to as "Donnelly et al."), Nanoholes were analyzed for photovoltaic applications, and this document is incorporated herein by reference. Into "Since the solar spectrum is very wide (hundreds of nanometers), sharp resonances are not a problem in photovoltaic applications, while in optical data / telecommunications, the laser spectrum is very narrow, eg. distributed feedback. Types of lasers, such as shaped lasers, Fabry-Pérot lasers, vertical cavity surface emitting lasers (VCSELs), and whether they are single mode or multimode and CW with external or direct modulation Depending on whether or not it is operated, the range is considerably smaller than 1 nm to several nm, that is, narrower than 0.01 to 3 nm. Donnelly et al. Also shows a sharp resonance in the 850 nm wavelength region with variation in absorption of at most 75% or more over a 20 nm wavelength span at 800 nm in FIG. Donnelly et al. FIG. 5 shows an optimal period of 800 nm at various nanohole depths and also shows a sharp resonance at, for example, 850 nm wavelength, where the absorption is about 100 over a 10 nm wavelength span. % To 20% change, ie. about 80% change in absorption. In addition to the resonance guided mode, the document also includes a fundamental mode and a channeling mode capable of generating enhanced absorption.

Ripple in absorption directly proportional to quantum efficiency is about 30% -40%, and in some cases less than 20% or less than 10% is acceptable for data communication and telecommunications applications it is. In some cases, for a center wavelength of about 850 nm, eg. ± 5 , 10, 20, 50, or 100 nm, it is desirable that the quantum efficiency ripple be 5% or less.

Experimentally, light trapping and improved absorption are shown by Erik Garnett, Pingdong Yang "Light Trapping in Silicon Nanowire Solar Cells", Nanolett, 2013, 10, 10812, -10817 (hereinafter referred to as "Garnett et al."), which is incorporated herein by reference. Garnett et al. FIG. 4 shows less than 10% light transmission at wavelengths up to 1100 nm and about 5% light transmission at 850 nm wavelength, and if the reflection can be ignored, the absorption is from the equation $1 = T + R + A$. It is assumed that it is about 90-95%, where T is transmissive, R is reflective, A is absorption, and all light is collected.

Katherine T. Foutaine, Christian G. Rondelli, Harry A. Atwater, another recent publication, which is incorporated herein by reference. Near-one broadband absorption design for semiconductor nanowire arrays via localized radial mode excitation (Near-unity broadband absorption design for semiconducting nanowire arrays via localized radial mode excitation", Vol. 22, no. On OPTICS EXPRESS A930, May 5, 2014 (hereinafter referred to as "Foutaine et al."), The simulation results of GaAs nanowires on 3 μm high Si with different diameters are 5 it shows that it is possible to achieve absorption close to 1 with a filling factor of%. Foutaine et al. Please refer to FIG. The purpose of the simulation is to reduce the use of materials to achieve a high efficiency photovoltaic device, and a 5% filling rate with 3 μm GaAs nanowires is equivalent to 150 nm of a flat GaAs layer for the amount of material. is there. However, a good comparison of absorption enhancement is to compare 3 μm GaAs

nanowires with a 3 μm thick GaAs 1st layer. In this case, the planar GaAs 3 μm layer has an absorption of 1 until reaching the band gap end of 1.42 eV or 873 nm, and it drops sharply, and at 896 nm the absorption coefficient is about 247 / cm, in which case it is weakly absorbed compared to, for example, about 5917 / cm at 855 nm, which is strongly absorbing, and about 7% of the 3 μm thick layer is absorbed at 888 nm and about 855 nm 85% absorption and about 9% absorption at 827 nm. A 3 μm GaAs layer was formed by Fountain et al. Compared to FIG. 4, no improvement in absorption is observed. Without perpendicular absorption enhancement, there is no advantage to using nanowire photodiodes beyond that of bulk layer photodiodes. In this case, a bulk 3 μm GaAs photodiode will perform almost as well, even if not better than a 3 μm GaAs nanowire photodiode for data / telecommunications at 800-850 nm.

According to the technique described in this document, for example, a 2 μm microstructured hole in Si (possible to be a column and / or a column and a hole), for example, data / remote communication with a high data rate of 5 Gb / s or higher. Improvements in absorption (modulus and / or length) are provided to be significantly more absorptive than 2 μm Si bulk layer photodiodes at 800-900 nm wavelengths.

FIG. 109 (A) and (B) are graphs showing the results of FDTD simulations using Maxwell's equations for a microstructured hole array, based on some examples. The hole array has a hexagonal lattice with a 2000 nm period and has an epitaxial structure similar to FIG. 92 of 2 μm "I" thickness SiNP and the holes etched through the I layer. And has two hole diameters (as shown in FIG. 106). FIG. 109 (A) shows absorption versus wavelength for four cases including curve 10910 using 1670 and 1500 nm hole diameters, while FIG. 109 (B) uses 1670 and 1500 nm hole diameters. The absorption versus wavelength on an exaggerated scale is shown for two of the four cases involving curve 10910. The simulation shows less than 10% ripple over a wavelength of 840 to 860 nm with an average absorption of about 90%. Furthermore, the region between 835-875 nm wavelengths can have an absorption of 80% or more of incident photons. Adding more than one hole diameter and / or period reduces the ripple in the absorption curve for that wavelength. Coupling of eigenmodes of different structures with different resonant modes, different hole diameters and / or periods reduces ripple and improves absorption over a wider wavelength range and is approximately 2 μm thick. This contributes to achieving a high absorption efficiency that is directly proportional to a quantum efficiency greater than 80% at 850 nm. In some cases, it is possible to achieve greater than 90% at 850 nm $\pm$ 10 nm. In some cases, it is possible to achieve quantum efficiency greater than 70%, 60%, 50% or 40% at 850 nm $\pm$ 10 nm.

Other hole diameters are also shown, e.g. 1330 and 1500 nm, 1500 and 1500 nm, 1670 and 1670 nm all have a period of 2000 nm and ripple is better in certain wavelength ranges than others, so for example when designing a microstructure PD / APD for a certain wavelength range such as 850 nm $\pm$ 10 nm, the 1500 nm hole size in a hexagonal lattice with a period of 2000 nm is less than 10% ripple in a 2 μm Si "I" layer. It is possible to achieve an absorption greater than 80%. In addition, holes of 1330 nm and 1500 nm and, as mentioned above, holes of 1500 and 1670 nm diameter in a hexagonal lattice with a period of 2000 nm can almost achieve this performance. Thus, it is possible to design a specific wavelength range in the spectral range of 20 nm or higher using a hole size range of 800-1700 nm with a period range of 800-2000 nm. Other diameters and periods can also be used, and the described example shows that certain combinations of hole diameter and period will absorb less than 10%, 20%, 30%, 40%, 50% ripple. It shows that it can be improved.

The hole diameter can be greater than or less than the wavelength, and the period in free space is much greater than the wavelength. Subwavelength periods can also be used in conjunction with periods above a certain wavelength.

This example shows a useful spectral range of 20 nm and in some cases 10 nm and in some cases over 40 nm, 5 Gb / s, and in some cases 10 Gb / s and in some cases various hole diameters can be used with the same period to design an operable 850 nm PD / APD in Si, with data rates of 20 Gb / s and in some cases over 30-40 Gb / s it is shown that. For example, other hole diameters and periods can be used to optimize the absorption enhancement at 850 nm wavelength, 980 nm wavelength, in which case generally the hole diameter and correspondingly, the period is correspondingly larger. Multiple hole diameters and / or multiple periods can be used to extend the microstructured silicon PD / APD to longer wavelengths, for example, 40% improved absorption at wavelengths from 800 to 1000 nm And in some cases 50% or more, and in some cases 60% or more, and in some cases 70% or more, and some in some cases, it is 80% or more, and in some cases 90% or more at a certain wavelength. For longer wavelengths, for example at 1550 nm, the holes and period can be, for example, 1300 nm diameter and 1500 nm diameter with periods of 2300 and 2500 nm, in which case the period is increasing. Other hole diameter / period for 1550 nm wavelength in Ge-on-Si can be, for example, 2300/3100 (nm unit), 2000/3100 (nm unit), in which case the diameter and period both are increasing.

In addition, other shapes such as chevron or "V" shaped holes can be used to improve absorption. Other shapes can be "X" shapes, rectangular shapes, triangular shapes, polygonal shapes, and / or any combination of multiple shapes to achieve the desired absorption enhancement and spectral width and polarization sensitivity. is there.

FIG. 110 shows a plot of absorption versus wavelength for microstructured / avalanche photodiodes with different hole diameters and grating periods, based on some examples. The simulated MS-PD / APD had a square grid and photons were incident from either the top surface or the bottom surface. The absorption layer is about 2 μm thick with Ge. The structure is the same as that shown in FIG. 82A. In the absorption curve with respect to the wavelength, for example, a microstructure having a period of 2000 nm and a hole diameter of 1500 nm represented by the curve 11010 shows good absorption characteristics of incident photons in the wavelength range from 1300 nm to 1650 nm. Among the absorption curves for that wavelength, for example, a microstructure with a period of 3000 nm and a hole diameter of 2250 nm represented by curve 11012 shows good absorption properties for incident photons in the wavelength range from 1650 to 1700 nm, for example. The combination of these two hole diameters and gratings may result in better than 80% absorption for the wavelength range from 1500 to 1700 nm. To achieve good absorption properties, ng better than 50%, in some cases better than 40%, and in some cases better than 30% etc. It is also possible to use a combination of At some wavelengths, it is possible to achieve better than 80%, for example 1550 nm wavelength $\pm$ 10 nm or more. Further, 1669 nm can achieve 90% absorption efficiency better than a few nanometers at the wavelength. Other hole diameters / periods of 1675 nm / 2000 nm are also shown and are represented by curve 11014.

In some cases, the hole diameter can be greater than the wavelength of light incident on the microstructured PD / APD to be absorbed, and in some cases, the hole diameter. The diameter of the hole can be approximately the same as the wavelength of the incident photon, and in some cases the diameter of the hole can be smaller than the wavelength of the incident photon. The same can be said for the period of the grating, in which case the period may be smaller, substantially the same and / or larger than the incident wavelength of the light to be detected, is possible.

111A and 111B show a simulation using the FDTD method of the structure shown in FIG. 82A based on some examples, using two grids and two different hole diameters. Yes, FIG. 111A shows a hole pattern in which a hexagonal lattice having a hole diameter D1 of 1500 nm is combined with D2 of 2250 nm at the center and a square lattice having G1 at four corners. The G1 holes are separated by 3 μm (G2 = 3 μm) in the horizontal direction and about 3.46 μm in the vertical direction. The hexagonal lattice has a period of 2 μm (d1 = 2 μm). FIG. 111B shows a plot of absorption versus wavelength. The two different hole diameter cases for the two gratings. (Curve 11110) show that at some wavelengths, the absorption is better than that of single grating / hole microstructured PD / APD. It is possible to see what is shown. For example, in the L band of about 1570 nm to 1600 nm, the data / telecommunications wavelength, curve 11110 shows much better absorption. This is compared to, for example, a square grating with a 2 μm period (curve 11112) at a hole diameter of 1500 nm and a 2 μm period (curve 11114) at a hole diameter of 2250 nm. The result is that with different combinations of hole diameter and period, the absorption response can have less resonance and / or less sharp resonance and can be optimally tuned in a certain wavelength range it just shows that. This is just one example, to obtain the desired quantum efficiency polarization sensitivity, insensitivity, wavelength selectivity and / or nonselectivity, eg. broadband, ripple / resonance reduction, etc., grating, period, hole diameter And other combinations of shapes can be simulated. For example, the diameter or minimum diameter can range from 100 nm to 3000 nm, and the period and / or multiple periods can range from 150 nm to 4000 nm. Further, the hole pattern may not be a grid, for example, a plurality of holes may be non-periodically distributed and / or a spacing between the plurality of holes may be changed. Further, although the hole pattern may not need to be periodic, the pattern can be periodic, or aperiodic. Multiple holes can be distributed randomly or pseudo-randomly.

and the hole diameter can vary in a periodic, non-periodic manner, a random manner, or a pseudo-random manner. Further, for example, if the periods are the same, almost the same, or less than the diameter of the holes in a period, the holes can be connected at least at one point. The array of holes can have a plurality of periods, and at least one period can cause the holes to contact and / or overlap.

Using a coupling of a resonant cell with an adjacent neighboring resonant cell according to the techniques described herein, absorption response smoothing is achieved, which has only a single resonant and absorbs for that wavelength. In contrast to existing resonant photodiodes exhibiting sharp resonant operation. A population of resonant cells based on the techniques described herein results in a more tuned absorption response with controlled ripple and wavelength range. Further, the techniques described herein can be used to tune specific absorption characteristics at specific wavelengths for more optimal PD / APD performance at specific wavelengths.

In addition, other microstructures / nanostructures that do not participate in the absorption enhancement process can be used to reduce reflections, for example with dimensions (diameters etc.) in the range of tens to hundreds of nanometers. Sub-wavelength holes or pits on the surface, in which case the depth can be in the range of tens to hundreds of nanometers or more.

FIG. 112 is a schematic diagram illustrating another lattice structure in which two hexagonal lattices of the same period are combined and interlaced with each other according to some embodiments. The pattern can use holes of the same or different diameters. As shown, the pattern has two different diameters, for example, the period can be 2500 nm, and D1 can be 1500 nm and D2 can be 700 nm, is possible. Other combinations of period and diameter are possible, and to adjust the absorption characteristics, and thus the quantum efficiency for the incident photon wavelength, and the wavelength span where the absorption characteristics are acceptable for optical data / telecommunications purposes, and used to satisfy any particular application condition for that particular optical system or systems.

The unit cells as shown by the dotted lines of the two hexagonal grids overlap each other, so their eigenmodes also overlap each other, which further reduces the ripple of the absorption characteristics in a specific wavelength range. It is also possible to extend the wavelength range in which the ripple in the absorption characteristic is reduced. Sharp changes in the absorption characteristics within a certain wavelength range are undesirable in a photodiode / avalanche photodiode. This is because, for example, drift in the incoming optical signal wavelength and / or drift in the photodiode absorption characteristics with respect to temperature can cause significant changes in optical to electrical signal conversion. Changes of less than 5% are preferred, and in some other cases 10%, 20%, 30 within a wavelength range of 2 nm, 4 nm, 10 nm, 20 nm, 40 nm, 60 nm, 100 nm, or 250 nm. %, 40% or less than 50% is preferred.

FIG. 113 shows a hexagonal lattice with six unit cells, each cell having its own eigenmode, where any field propagation / distribution is an extension of that eigenmode. It may be. The eigenmodes of each cell can be combined with the eigenmodes of neighboring cells, thereby forming a composite coupled supermode, which is for visualization purposes only, but with multiple pendulums can be thought of as a 2D array of couplings, where each pendulum is connected to all its adjacent pendulums via a weak spring (the weak spring is a mechanical coupling mechanism). The response or motion of this massively coupled 2D array pendulum is very complex and not a simple oscillating motion of a single pendulum. In addition to the coupling, a second nested hexagonal lattice can be added as in FIG. In addition, holes in the cell and / or in any shape and of any depth, of any depth and of any diameter, and any of the parameters can have a plurality of values. It can be added to the boundary of an adjacent cell, which can affect its eigenmode and its coupling with the adjacent cell eigenmode. For example, for convenience of explanation, a plurality of holes of diameter X can be added as shown, where X can have a single value or multiple values and the holes can be Si or Ge. It is possible to each partially or completely at the surface and within the absorber layer. This can also be such that it does not penetrate the absorbing layer only on the surface. According to some embodiments, the holes can be partially or fully etched into the absorber layer.

The coupling of the cell, which becomes a complex standing wave or super eigenmode, results in a single resonator such as a resonant response as in previously known structures having sharp response characteristics in absorption response (proportional to quantum efficiency). It is possible to give a smoother absorption versus wavelength response compared to

FIG. 114 illustrates a SiNP microstructured photodiode having a hole array and a textured surface, according to some embodiments. The texture surface 11440 can be on the top surface and / or in the hole 11422 itself. Texturing can be performed at an angle off vertical, in which case the substrate can be rotated (or stationary) in a tilted manner with respect to the dry etching beam (direction), and the texture can be, for example, it is possible to make it partially on the side wall. According to some embodiments, texture 11440 reduces the reflection of incident illumination. This is because in an optical communication link, the optical signal reflected back to the optical source is undesirable and may cause signal to noise degradation in the data communication system. Texturing, such as black silicon, with or without masking and dry etching on the semiconductor surface can generate a forest of nanostructures that can trap photons and reduce reflections. In the absence of texturing, the reflection is less than 10% and in some cases less than 5% and in some cases less than 2%, for example as in FIG. It can be seen in the plot of absorption for various wavelengths, where the absorption is greater than 50-95% at certain wavelengths. From the equation $1 = T + R + A$, where T is transmitted light, R is reflected light, A is absorbed light, and when $A = 90-95\%$, $T + R$ is 5-10%. Thus, R is 10% or less, and in some cases 5% or less. Adding texture to the semiconductor surface can further reduce reflection to less than 1% at certain wavelengths. Furthermore, the optical signal can be incident on the microstructured PD / APD at an angle that is off-vertical and can further reduce reflection back into the optical data communication channel.

FIG. 115 is a graph showing absorption coefficients of Si and Ge with respect to wavelength. For example, FIG. 115 should be referred to and incorporated herein by reference. At 850 nm for Si and 1550 nm for Ge, both have an absorption coefficient of less than about 360 / cm. This weak absorption results in poor quantum efficiency for high speed photodiodes and / or avalanche photodiodes, for example, which typically have an absorption thickness of about 2 μ m for data rates above 10 Gb / s bandwidth. This is one reason why high-speed photodiodes exceeding the data rate of, for example, 5 Gb / s are not commercially available for the wavelength of 850 nm for Si and 1550 nm for Ge.

FIG. 116 is a graph illustrating the improved effective absorption coefficient of Ge due to a microstructured hole array, according to some examples. Curve 11610 shows the improved absorption coefficient for Ge in a hexagonal lattice with a 1.25 μ m hole diameter and a 1.65 μ m period for a 2 μ m thick layer of Ge. For comparison, curve 11612 shows the absorption coefficient of bulk Ge (without microstructured holes). According to some embodiments, other microstructures can provide an improved effective absorption coefficient that can be optimized for a wavelength band. For example, the microstructure can be holes or pillars, the spacing can be periodic or aperiodic, and the holes or pillars have a single or multiple diameters. And the shape can be circular or non-circular. As indicated above, absorption is the product of the absorption coefficient and the absorption length. Therefore, it is possible to make the absorption length an improved effective absorption length while maintaining the absorption coefficient as the absorption coefficient of the bulk material (curve 11612 in the case of Ge), that is, 5 or more than the physical absorption length. It can be 10, 20, or even longer. As can be seen from FIG. 116, the improved effective absorption coefficient is more than 10 times greater than the bulk absorption coefficient in Ge in many wavelength ranges. Improved effective absorption coefficient in Ge due to microstructure is greater than 30%, greater than 40%, greater than 50%, greater than 60%, greater than 70%, greater than 80%, greater than 90% knowledge. With quantum efficiency (directly proportional to absorption), typically the absorption length at 1550 nm wavelength and longer wavelengths is about 2 μ m or less, allowing the development of high-speed PD / APD. It is not known that such a combination of material, absorption length, wavelength, data rate, and quantum efficiency is commercially available for both Si and Ge. The same is true for high data rate bandwidths where the absorption length is typically about 2 μ m or less for data rates of 5, 10, 20 Gb / s and faster and for wavelength ranges of 800 nm and longer, for example. It can also be said about the Si microstructure type PD / APD for the operation in FIG.

In addition, the microstructure can be composed of a single element or cell and / or multiple elements or cells, and of a linear optical field effect, a nonlinear optical field effect, a coupled mode effect, and / or a slow wave effect. It is possible to have improved effective absorption and / or improved effective absorption length that may be

the result.

Improved absorption coefficient and / or absorption length using microstructures can be used to extend the operating wavelength of other materials such as III-V materials, GaAs, InP, GaIn, etc. at the edge of the band where the absorption coefficient is weaker. It is also possible to do, for example, see Figure 3 at http://www.hamamatsu.com/is/en/community/optical_sensor/tutorials/physics_of_mppc/index.html?utm_source=googleplus&utm_medium=social&utm_campaign=hc-social. It is for InGaAs in the vicinity of the 1.6 μm wavelength and is incorporated herein by reference. According to some embodiments, the microstructure can be used to extend operating wavelengths near 1.6 μm and longer.

In addition, the use of microstructures to improve absorption can be applied to amorphous materials such as amorphous Si and also other materials such as polymers, ceramics, graphene, alloys and oxides. It is also possible to apply to, in addition, other forms of energy propagation, such as acoustic, microwave, UV, X-ray, and pressure waves, can be converted from one form of energy to another. For example, structures with dimensions on the order of approximately acoustic wavelengths on piezoelectric ceramics and / or crystal can, for example, improve the conversion of acoustic energy to electrical energy. Using a structure with dimensions of approximately acoustic wavelengths can improve acoustic absorption, which can be, for example, a thinner piezoelectric material, which can be, for example, more. Making it possible to have a high acoustic frequency response.

FIG. 117 is a graph showing improved absorption of Si microstructure PD / APD based on some examples. The simulated MS-PD / APD has a hexagonal lattice hole array, a period of 2000 nm, a diameter of 1500 nm, and photons incident at a deviation of 10, 20, 40 degrees from the vertical, for example. FIG. 119 shows a simulation of improved absorption versus wavelength for a similar structure when photons are incident normal to the surface. As can be seen, photons that are off by 10 degrees from normal do not significantly change the absorption at a wavelength of 850 nm, which is still greater than 90%. At 40 degrees, the absorption at 850 nm is still above 90%, but at 20 degrees, the absorption appears to decrease to 85% at 850 nm. Overall, at certain wavelengths, changes in the incident angle of photons incident on the microstructure can have an absorption change of less than 10% over an angular range of 0-40 degrees, for example. By optimizing hole diameter, period, and non-periodic microstructure over a range of wavelengths, the change in quantum efficiency (directly proportional to absorption) with respect to the incident angle of incident photons can be made less than 10%. And in some cases less than 5% and in some cases less than 3%. This feature is important for minimizing reflected light back toward the laser source, which can transmit electrical signals for transmission in optical fibers and / or free space and / or optical waveguides. When an optical modulator is used to convert to an optical signal, it is modulated directly or indirectly at the data rate for transmitting the optical signal. Using a non-laser source, such as a light emitting diode, as an electrical signal to optical signal converter reduces the condition of the reflected power returned toward the optical source. This is because LEDs are less coherent and / or incoherent optical sources, and reflections at the same wavelength are less disruptive in integrity as electrical to optical signal converters.

Although this patent application refers to certain theories in describing the nature and operation of the device, these theories are based on current understandings, even if the theory is incorrect due to future progress. Obviously, even if it proves, it does not affect the actual operation of the device disclosed herein. This patent specification also refers to numerical ranges of parameters, and it should be understood that insubstantial deviations from such ranges are within the spirit of the progress disclosed herein.

The drawings illustrating the device are not to scale and are somewhat idealized, for example straight lines are sharp corners, etc., while the actual device is not very straight or smooth. It should be understood that there may be no walls and some rounded corners and there is a probability, in fact, depending on the processing parameters, walls such as holes or pillar walls in the microstructure may be uneven and have a rough surface with surface features such as depressions and dents. This may actually contribute to effects such as reduction of unwanted reflections.

Semiconductor layers for light sensing and / or signal processing and distribution integrated circuits may be vapor phase epitaxy, chemical vapor deposition, plasma enhanced chemical vapor deposition, atomic layer deposition, molecular beam epitaxy, etc. and / or, for example, selective area epitaxy can be grown epitaxially using techniques such as selective area epitaxial lateral overgrowth, epitaxial lateral overgrowth, heteroepitaxy, wafer bonding, epitaxial lift-off process, and any combination of growth, bonding, lift-off processes, etc. It is. A suitable process for the semiconductor layer is vapor phase epitaxy or chemical vapor deposition.

Further, the microstructure holes can only be in the high field "I" region for absorption and necessarily extend into and / or through the N and P regions of the PD / APD. is not. The holes can overlap over their entire length and / or adjacent holes can partially overlap along the length of the hole.

The doping of the P+ and N regions often has a gradual transition between different doping level regions due in part to dopant diffusion during epitaxial growth. The transition from high doping to low doping may occur over a distance of 1 to 1000 nm or more, depending on the dopant type, doping level, growth temperature and epitaxial deposition method. The PIN structure is often P+ PP-N-NH+, where P and P+ and N and N+ are transition regions and a very narrow transition region is desirable.

Although described above in some detail for purposes of clarity, it will be apparent that certain changes and modifications may be made without departing from the principles thereof. It should be noted that there are many alternative ways of implementing both the processes and apparatus described herein. Accordingly, this example should be considered as illustrative and not limiting, and the content of the performance described herein should not be limited to the details described herein. Changes may be made within the scope of the claims and their equivalents.

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CN101955362A *	2009-07-17	2011-01-26	北京邮电大学	Fabrication method for semiconductor photodetector with nano waveguide structure
US7971637B1	2009-08-20	2011-07-12	Hill Laboratories, LLC	Honeycomb infrared detector
WO2011203407A1	2010-09-10	2012-03-15	Shih-Ping Wang	Photovoltaic nanowire structures and related fabrication methods
US9349970B2 *	2009-09-29	2016-03-24	Research Triangle Institute	Quantum dot fullerene junction based photodetectors
US8187768B2 *	2010-06-04	2014-07-22	The Governing Council Of The University Of Toronto	Optical receiver with monolithically integrated photodetector
US8933506B2	2011-01-31	2015-01-13	Alpha And Omega Semiconductor Incorporated	Diode structures with controlled injection efficiency for fast switching
WO2012149441A2	2011-04-29	2012-11-01	The Regents Of The University Of California	High efficiency vertical optical coupler using sub-wavelength high contrast grating
US20120292676A1	2011-05-21	2012-11-22	James Pan	Novel Very Fast Optic Nonvolatile Memory with Alternative Carrier Lifetimes and Bandgap Energies, Optic Random Access, and Mirrored 'Fly-back' Configurations
US8868159B2 *	2011-07-08	2013-02-05	Excelitas Canada, Inc.	Photon counting UV-APD
JP5830852B2 *	2011-10-21	2015-12-16	浜松ホトニクス株式会社	Photodetector
DE103012201911B4	2012-02-09	2022-09-22	Robert Bosch GmbH	Super junction Schottky oxide PIN diode with thin p layers under Schottky contact
CN104303315B *	2012-05-29	2017-05-31	聚与芯微有源器件合伙企业	Uptake zero electric field and the device of multiplication region electric field including energy-independent control
JP6105258B2	2012-11-05	2017-03-29	住友電気工業株式会社	Semiconductor light receiving element, light receiving device
EP2600154B1	2013-05-22	2021-05-19	Shih-Yuan Wang	Microstructure enhanced absorption photosensitive devices
US9431490B2	2013-08-09	2016-08-30	Infinern Technologies Austria AG	Power semiconductor device and method
KR101896708B1	2014-01-09	2017-01-13	한국전자통신연구원	Semiconductor device and method of fabricating the same
US9518893B2	2014-11-19	2017-11-14	W&Wsens Devices, Inc.	Microstructure enhanced absorption photosensitive devices

* Claim by examiner, † Claim by third party

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Publication number	Priority date	Publication date	Assignee	Title
JP2020128689A *	2019-02-07	2020-08-27	株式会社東芝	Molecular detection device
JP2022517827A *	2018-12-20	2022-03-09	パナソニックエレクトロニクス株式会社	Semiconductor photodiodes that function over a wide band and how to obtain them
KR20220653092A *	2020-12-11	2022-06-20	한국과학기술원	Image sensor having hetero-junction structure according to morphologic integration and manufacturing method thereof
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WO2016089487A1 *	2017-10-30	2019-05-09	W&Wsens Devices, Inc.	Microstructure enhanced absorption photosensitive devices
US11121271B2	2013-05-22	2021-09-14	W&Wsens Devices, Inc.	Microstructure enhanced absorption photosensitive devices
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EP300134B1 *	2015-05-22	2021-03-10	Shih-Yuan Wang	Microstructure enhanced absorption photosensitive devices
US10468543B2	2013-05-22	2019-11-05	W&Wsens Devices, Inc.	Microstructure enhanced absorption photosensitive devices
US10197632B2 *	2013-05-22	2019-07-29	Hewlett Packard Enterprise Development Lp	Optical devices including a high contrast grating lens
CN105798578B	2013-10-29	2019-08-30	慈与友聚有限责任公司	High contrast grating opto-electronic device
WO2015112166A1	2014-01-24	2015-07-30	Hewlett-Packard Development Company, L.P.	Optical modulation employing high contrast grating lens
US9818893B2	2014-11-18	2017-11-14	W&Wsens Devices, Inc.	Microstructure enhanced absorption photosensitive devices
US10201273B2 *	2015-02-26	2019-04-16	Sumitomo Electric Industries, Ltd.	Bi-directional optical module communicating with single optical fiber and optical transceiver implementing the same
CH711000A1 *	2015-04-28	2016-10-31	Ian Lab GmbH	A lighting device and a method for controlling a lighting device
JP2017022175A *	2015-07-07	2017-01-26	ルネサスエレクトロニクス株式会社	Semiconductor device and manufacturing method of the same
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US10514296B2 *	2015-07-29	2019-12-24	Samsung Electronics Co., Ltd.	Spectrometer including metasurface
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JP2017076051A *	2015-08-13	2017-04-20	富士通株式会社	Semiconductor light-receiving device
US10097281B1	2015-11-18	2018-10-09	Hypres, Inc.	System and method for cryogenic optoelectronic data link
JP2017098305A *	2015-11-18	2017-06-01	シャープ株式会社	Photodetector
JP6790820B2 *	2016-03-10	2020-07-29	株式会社東芝	Photodetector and light device using the same
DE102015219236A1 *	2016-10-04	2018-04-05	TiConic GmbH & Co. KG	Integrated arrangement of modulated light points for communication by means of visible light
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US993724B1 *	2016-12-21	2018-05-22	PhantomField, Inc.	Augmented reality display system
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KR10201934881 *	2017-03-28	2021-10-29	삼성전자주식회사	Vertical Cavity Surface Emitting Laser including meta structure reflector and optical apparatus including the vertical cavity surface emitting laser

KR20200110717A *	2017-06-26	2020-09-25	소니 세미컨덕터 솔루션즈 가부시키가이샤	Single-photon avalanche diodes and methods for operating single-photon avalanche diodes
CN111138890B *	2017-07-21	2024-06-11	文和文森斯设备公司	Microstructure enhanced absorption photosensitive device
CN107408348B *	2017-09-08	2023-06-29	中国工程物理研究院电子工程研究所	Backside illuminated cascade multiplication avalanche photodiode
JP6990380B2 *	2017-09-27	2022-01-12	富士通株式会社	Infrared detector, image sensor, and image pickup system
CN109719000B *	2017-10-26	2021-12-10	上海新微电子科技有限公司	Light detection device and light detection device
US10418472B2 *	2017-11-30	2019-09-17	SiliconElectronics (Research & Development) Limited	Near ultraviolet photocell
EP3506020B1 *	2017-12-29	2022-06-08	iHP GmbH - innovations for High Performance Microelectronics / Leibniz-Institut für innovative Mikroelektronik	Electrooptical device
US10797193B2 *	2018-01-23	2020-10-06	Lumentum Operations LLC	Bias control structure for avalanche photodiodes
CN108507478A *	2018-03-01	2018-09-07	东京大学	A kind of adjustable ultraphotonic spectrum detection chip of plasmon multi-resonant mechanism enhancing
WO2019218022A1 *	2018-05-14	2019-11-21	The University Of Melbourne	A photodetector
KR102588638B1 *	2018-05-28	2023-07-21	코닝 인코포레이티드	Light extraction substrate of organic light emitting device and method of fabricating the same
KR102592498B1 *	2018-06-05	2023-10-24	삼성전자주식회사	Multi-wavelength light source device, multi-function projector and including the same and electronic apparatus including the multi-function projector
CN109713022A *	2018-07-27	2018-10-26	江苏奥普智能传感技术研究所有限公司	A kind of enhanced narrow band filter and its manufacturing method
US10964835B2 *	2018-08-29	2021-03-30	The Boeing Company	Universal broadband photodetector design and fabrication process
US10713000B2 *	2018-10-17	2020-07-14	Taiwan Semiconductor Manufacturing Company Ltd.	Semiconductor device and manufacturing method of the same
US1066853B1	2018-11-20	2020-01-26	Juniper Networks, Inc.	Normal incidence photodetector with self-test functionality
CN110880539B *	2018-12-06	2021-09-24	希烽光电科技(南京)有限公司	Waveguide integrated avalanche photodiode
WO2020134837A1	2018-12-25	2020-07-02	芯恩电子技术(深圳)股份有限公司	Photoelectric chip, manufacturing method and installation method
US11255724B2 *	2019-01-06	2023-02-22	Artix, Inc.	Photodetecting device for detecting different wavelengths
RU2732694C1 *	2019-03-12	2020-09-21	Общество С ограниченной ответственностью "Девиско-Фотонный Аварангел" (ООО "Девис")	Avalanche photodetector (embodiments) and method of manufacturing thereof (embodiments)
US10930747B2 *	2019-06-04	2021-02-23	Nxp B.V.	Semiconductor device with an etched electrode
CN110924548B *	2019-06-11	2022-01-28	Oppo广东移动通信有限公司	Pixel structure, image sensor and terminal
CN112880387A	2019-08-01	2021-03-30	文和文森斯设备公司	Microstructure enhanced absorption photosensitive device
CN112881325A *	2019-08-05	2021-02-05	上海新微技术研发中心有限公司	Waveguide type germanium photoelectric detector based on photonic crystal and preparation method
US11805792B2 *	2019-09-25	2023-03-14	Massachusetts Institute Of Technology	Resonance enhanced surface illuminated sub-bandgap infrared photodetectors
US11448801B2 *	2019-10-17	2022-09-20	Taiwan Semiconductor Manufacturing Co., Ltd.	Multifunctional collimator for contact image sensors
CN110864141A *	2019-11-21	2020-02-26	中国电子科技集团公司第四十四研究所	Monolithic integrated balanced photoelectric detector chip and manufacturing method thereof
US2022036856A1 *	2019-11-22	2022-12-08	The Board Of Trustees Of The Leland Stanford Junior University	High-quality-factor metasurface for phase contrast imaging and spatial frequency filtering
G825R0675A *	2019-11-26	2021-04-23	Smart Photonics Holding B.V.	Waveguide structure for a photonic integrated circuit
FR3109943B1	2020-05-11	2023-11-03	Maggioli Stéphane	Antifouling coating, biocide, antiseptic, ecological non-solvent, metalloplastic with lamellar structure
WO2020249541A1 *	2020-08-03	2022-02-10	株式会社京セラ コミュニケーション	Light receiving element unit

CN112018140A *	2020-08-14	2020-12-01	清华大学	Metallase spectrum chip based on random shape unit
CN112531073B *	2020-09-27	2022-09-20	北京工业大学	Preparation method of side-incident SOI (silicon on insulator) based Si/SiGe HPT (high-performance heterojunction bipolar transistor) with photonic crystal structure
CN112420857A *	2020-10-20	2021-02-25	北京工业大学	Photonic crystal SiGe/Si phototransistor detector
CN112302658B *	2020-10-29	2022-03-15	西安理工大学	Light adjustable four-frequency-band terahertz metamaterial absorber based on all-dielectric material
US11536914B2	2020-11-17	2022-12-07	Globalfoundries U.S. Inc.	Photodetector array with diffraction gratings having different pitches
US11482562B2	2020-12-30	2022-10-25	Applied Materials, Inc.	Methods for forming image sensors
FR3120139B1 *	2021-02-03	2023-11-03	St Microelectronics-Croles 2 Sas	Optical device
KR102307799B1 *	2021-03-24	2021-10-01	이성환	Backside illuminated avalanche photodiode and manufacturing method thereof
CN115005079B *	2021-03-09	2022-08-19	南京大學	Method for producing an absorber-emitter structure for solar thermal photovoltaic cells
CN113294973B *	2021-05-14	2022-07-05	长春理工大学	Avalanche photodiode structure with high responsivity
CN115700628A *	2021-07-15	2023-02-07	上海新微技术研发中心有限公司	Photodetector and method of manufacturing the same
CN113990983B *	2021-10-25	2023-07-04	西安微电子技术研究所	Photodiode with strong light absorption capacity and preparation method thereof
US11721790B2 *	2021-11-17	2023-08-08	Globalfoundries U.S. Inc.	Avalanche photodetectors with a multiple-thickness charge sheet
KR20230089137A *	2021-12-13	2023-06-20	삼성전기주식회사	Multi-layer capacitor
US11849036B2 *	2022-04-11	2024-04-02	Ciena Corporation	Suppression of phototransistor gain in an optical modulator
WO2023211261A1 *	2022-04-28	2023-11-02	Compoundtek Pte. Ltd.	Optical bench apparatus and fabrication method thereof for heterogeneous laser integration
CN114823941B *	2022-04-29	2024-04-02	锦城大學	Resonance enhanced photoelectric detection and manufacturing method thereof
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* Cited by examiner; † Cited by third party; ‡ Family to family citation.

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Fan et al.	2012	A monolithically integrated dual-wavelength photodetector with a step-shaped Fabry-Pérot filter

Priority And Related Applications

Applications Claiming Priority (39)

Application	Filing date	Title
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PCIT6/2015/061120	2015-11-17	Microstructure enhanced absorption photosensitive devices

Legal Events

Date	Code	Title	Description
2017-11-29	A711	Notification of change in applicant	Free format text: JAPANESE INTERMEDIATE CODE: A711 Effective date: 20171129
2017-12-15	A521	Request for written amendment filed	Free format text: JAPANESE INTERMEDIATE CODE: A521 Effective date: 20171215
2017-12-26	A521	Request for written amendment filed	Free format text: JAPANESE INTERMEDIATE CODE: A523 Effective date: 20170823
2018-01-26	A521	Request for written amendment filed	Free format text: JAPANESE INTERMEDIATE CODE: A523 Effective date: 20180110
2018-10-18	A621	Written request for application examination	Free format text: JAPANESE INTERMEDIATE CODE: A621 Effective date: 20181018
2019-10-15	A977	Report on retrieval	Free format text: JAPANESE INTERMEDIATE CODE: A971007 Effective date: 20191015
2019-12-08	A131	Notification of reasons for refusal	Free format text: JAPANESE INTERMEDIATE CODE: A131 Effective date: 20191208
2020-02-27	A601	Written request for extension of time	Free format text: JAPANESE INTERMEDIATE CODE: A601 Effective date: 20200227
2020-04-27	A521	Request for written amendment filed	Free format text: JAPANESE INTERMEDIATE CODE: A523 Effective date: 20200427
2020-09-29	A131	Notification of reasons for refusal	Free format text: JAPANESE INTERMEDIATE CODE: A131 Effective date: 20200929
2020-12-23	A601	Written request for extension of time	Free format text: JAPANESE INTERMEDIATE CODE: A601 Effective date: 20201223
2021-02-25	A521	Request for written amendment filed	Free format text: JAPANESE INTERMEDIATE CODE: A523 Effective date: 20210225
2021-03-31	TRDD	Decision of grant or rejection written	
2021-04-06	A01	Written decision to grant a patent or to grant a registration (utility model)	Free format text: JAPANESE INTERMEDIATE CODE: A01 Effective date: 20210406
2021-04-27	A51	First payment of annual fee (during grant procedure)	Free format text: JAPANESE INTERMEDIATE CODE: A51 Effective date: 20210423

2021-04-27	R150	Certificate of patent or registration of utility model	Ref document number: 5875087 Country of ref document: JP Free format text: JAPANESE INTERMEDIATE CODE: Ref document number: 5875087 Country of ref document: JP Free format text: JAPANESE INTERMEDIATE CODE: R150
2024-05-07	R250	Receipt of annual fees	Free format text: JAPANESE INTERMEDIATE CODE: R250

Concepts

machine-extracted

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Name	Image	Sections	Count	Query match
absorption reaction	title,claims,abstract,description	496	0.000	
silicon	claims,abstract,description	135	0.000	
silicon	claims,abstract,description	124	0.000	
silicon	claims,abstract,description	122	0.000	
method	claims,abstract,description	66	0.000	
semiconductor	claims,abstract,description	47	0.000	
reductive effect	claims,abstract,description	15	0.000	
optical effect	claims,description	170	0.000	
substrate	claims,description	112	0.000	
material	claims,description	102	0.000	
nitrogen	claims,description	70	0.000	
phosphorus	claims,description	68	0.000	
fiber	claims,description	40	0.000	
processing	claims,description	93	0.000	
communication	claims,description	29	0.000	
optical fiber	claims,description	29	0.000	
process	claims,description	28	0.000	
germanium	claims,description	27	0.000	
reversible effect	claims,description	27	0.000	
etching	claims,description	25	0.000	
germanium atom	claims,description	12	0.000	
overgrowth	claims,description	9	0.000	
light absorption	claims,description	9	0.000	
crystal	claims,description	8	0.000	
detection method	claims,description	8	0.000	
silicon-based material	claims,description	7	0.000	
integration	claims,description	6	0.000	
metal oxide	claims,description	6	0.000	
metal oxides	claims,description	5	0.000	
chemical reaction	claims,description	3	0.000	

✖ complement effect	claimdescription	3	0.000
✖ benefit	abstractdescription	18	0.000
✖ packaging method and process	abstractdescription	10	0.000
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(19) 日本国特許庁(JP)

(12) 公表特許公報(A)

(11) 特許出願公表番号

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G01J 1/02 (2006.01)	G01J 1/02 C	4M118
G01J 1/42 (2006.01)	G01J 1/42 H	5F849
G01J 1/04 (2006.01)	G01J 1/04 B	

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最終頁に続く

(54) 【発明の名称】 マイクロストラクチャ向上型吸収感光装置

(57) 【要約】

【課題】 マイクロストラクチャを使用して半導体におけるフォトンの吸収を向上させる技術を記載する。該マイクロストラクチャは、例えば穴であって、フォトンの吸収を実効的に増加させる。シリコンフォトダイオード及びシリコンアバランシェフォトダイオードに対して吸収向上のためにマイクロストラクチャを使用することは、約90%以上の量子効率で850nmの波長を有するフォトンにおいて10Gb/sを超える帯域幅となる場合がある。それらの厚さ寸法は、それらがCMOS、BiCMOS及びその他のエレクトロニクスと同一のSiチップ上に便利に集積化させることを可能とさせ、その結果パッケージング上の利点が得られ、容量が減少され、従って一層高速となる。

【解決手段】

【選択図】 図1

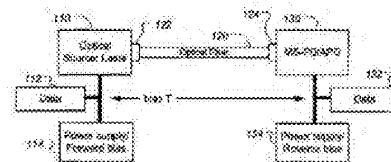


FIG. 1

【特許請求の範囲】

【請求項1】

単一半導体チップ内に形成されているマイクロストラクチャ向上型光吸収を具備する光検知器と電子的プロセッサとの両方を有しているデータ通信用の集積化検知器／プロセッサ回路において、

半導体基板上に形成されており且つデータ通信用に変調された光学ソース信号からのフォトン吸収し且つそれに対応する出力電気信号を供給する形態とされているフォトン吸収領域を有している光検知器が設けられており、

前記フォトン吸収領域はその中に複数の穴を有しており、該穴は前記基板へ向けて延在しており且つ複数の該穴において同一のソース信号を同時的に受け取る形態とされており、

電子的プロセッサも前記半導体基板上に形成されており且つ前記フォトン吸収領域と動作上関連されていて前記出力電気信号をそれから受け取り且つ処理済出力へ処理し、それにより該光学ソース信号を受け取り且つ該処理済出力を出力する単一の半導体チップを形成しており、

前記フォトン吸収領域及び前記電子的プロセッサは同じ程度の厚さである夫々の厚さを有しており、及び

カソード領域とアノード領域とが前記フォトン吸収領域と逆バイアス回路とに動作上関連されていて、前記逆バイアス回路は前記カソード領域が前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域と前記アノード領域との間に電圧を印加する形態とされている、

集積化検知器／プロセッサ回路。

【請求項2】

該フォトン吸収領域の厚さが0.5乃至5マイクロメートルの範囲内である請求項1記載の集積化検知器／プロセッサ回路。

【請求項3】

該電子的プロセッサが相補的金属酸化物半導体（CMOS）装置、バイポーラ（B1）装置、及びB1CMOS装置の内の少なくとも一つを有している応用特定集積回路（ASIC）を有している請求項1記載の集積化検知器／プロセッサ回路。

【請求項4】

該フォトン吸収領域は、800nm乃至900nmの波長において入射ソース信号を40%を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項1記載の集積化検知器／プロセッサ回路。

【請求項5】

該フォトン吸収領域は、800nm乃至900nmの波長において入射ソース信号を50%を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項1記載の集積化検知器／プロセッサ回路。

【請求項6】

該フォトン吸収領域は、800nm乃至900nmの波長において入射ソース信号を60%を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項1記載の集積化検知器／プロセッサ回路。

【請求項7】

該フォトン吸収領域は、1400nm乃至1700nmの波長において入射ソース信号を40%を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項1記載の集積化検知器／プロセッサ回路。

【請求項8】

該フォトン吸収領域は、1400nm乃至1700nmの波長において入射ソース信号を50%を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項1記載の集積化検知器／プロセッサ回路。

【請求項9】

該フォトン吸収領域は、1400nm乃至1700nmの波長において入射ソース信号を60%を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項1記載の集積化検知器／プロセッサ回路。

【請求項10】

該フォトン吸収領域は、800nm乃至900nmのソース信号波長の少なくとも20nmの選択した波長スパンに亘って20%未満だけ変化する吸収百分率において該入射ソース信号を吸収する形態とされている請求項1記載の集積化検知器／プロセッサ回路。

【請求項11】

該フォトン吸収領域は、1400nm乃至1700nmのソース信号波長の少なくとも20nmの波長スパンに亘って20%未満だけ変化する吸収百分率において該入射ソース信号を吸収する形態とされている請求項1記載の集積化検知器／プロセッサ回路。

【請求項12】

各穴は該基板の表面に平行な断面を有しており且つ該断面の最大寸法は400nmと2500nmとの間であり、及び各穴は該複数個の穴の最も近い隣接する穴の中心から3500nm未満だけ離隔されている中心を有している請求項1記載の集積化検知器／プロセッサ回路。

【請求項13】

前記光検知器は、更に、 $10^{19}/\text{cm}^3$ 又はそれを超えて高度にドーピングされており且つ前記フォトン吸収領域の側面に位置しているP層とN層とを有しており、及び該フォトン吸収領域は軽度ドーピングされているか又は意図的にはドーピングされておらず高々 $10^{19}/\text{cm}^3$ である請求項1記載の集積化検知器／プロセッサ回路。

【請求項14】

前記光検知器がアパランシェ光検知器を有している請求項1記載の集積化検知器／プロセッサ回路。

【請求項15】

該フォトン吸収領域がSiを有している請求項1記載の集積化検知器／プロセッサ回路。

【請求項16】

該フォトン吸収領域がGeを有している請求項1記載の集積化検知器／プロセッサ回路。

【請求項17】

該光検知器が、前記ソース信号を担持するオプティカルファイバーを受け付け且つ該ファイバーの一端部を前記フォトン吸収領域から選択した距離に維持する形態とされているテーパ付き又は段差付きの穴を有している請求項1記載の集積化検知器／プロセッサ回路。

【請求項18】

更に、該ファイバーの前記端部と該フォトン吸収領域との間にレンズを包含している請求項17記載の集積化検知器／プロセッサ回路。

【請求項19】

該光検知器が、該ソース信号の複数回の反射を発生させて前記ソース信号が該フォトン吸収領域を複数回横断する形態とされている反射構造を有している請求項1記載の集積化検知器／プロセッサ回路。

【請求項20】

該光検知器が、該フォトン吸収領域の2つの対向する側部から該ソース信号を受け取る形態とされている請求項1記載の集積化検知器／プロセッサ回路。

【請求項21】

前記穴が、該穴の複数のグループにおいて光信号から電気信号への変換において結合共振を発生させてソース信号の吸収を向上させる形態とされている請求項1記載の集積化検知器／プロセッサ回路。

【請求項22】

更に、一つ又はそれ以上の付加的な光検知器が前記半導体基板上に形成されており且つ夫々の付加的なソース信号を受け取り且つそれらに対応する夫々の出力電気信号を供給する夫々のフォトン吸収領域を有しており、及び一つ又はそれ以上の付加的な電子的プロセッサも前記半導体基板上に形成されており且つ前記付加的な光検知器の該夫々のフォトン吸収領域と動作上関連されていてそれから前記夫々の出力電気信号を受け取り且つ処理する請求項1記載の集積化検知器／プロセッサ回路。

【請求項23】

該複数個の穴は、前記ソース信号の波長を含む波長範囲において、穴は無いがその他は同じ光検知器と比較してフォトンの吸収を向上させる請求項1記載の集積化検知器／プロセッサ回路。

【請求項24】

該電子的プロセッサは、相互インピーダンス増幅器、信号処理エレクトロニクス、及びルーチングエレクトロニクスからなるグループから選択される一つ又はそれ以上のタイプを包含している請求項1記載の集積化検知器／プロセッサ回路。

【請求項25】

該光検知器と関連している容量が、そのアノード領域とカソード領域とを従来のボンダパッドへ動作接続させているその他は同じ光検知器と比較して減少されている請求項1記載の集積化検知器／プロセッサ回路。

【請求項26】

該光検知器は、更に、増倍領域を有しており且つ2より大きな利得を有しており800乃至900nmのソース信号波長において10Gb/sより大きなデータ帯域幅において該ソース信号を検知する形態とされているアバランシェフォトダイオードである請求項1記載の集積化検知器／プロセッサ回路。

【請求項27】

光学／電子システムにおいて、

光検知器とアクティブ電子回路とが、同一の半導体基板上に構築されており且つ互いに動作上関連されていて単一の集積回路チップを形成しており、

レーザーが、Gb/sのデータレートで変調されてGb/sレートで情報を担持する光学ソース信号を発生し、

オプティカルファイバーが、該レーザーと関連していてその入力端において該光学ソース信号を受け取り且つそれをその出力端へ運び、

該光検知器が、該オプティカルファイバーの該出力端と関連していてそれから該光学ソース信号を受け取り且つそれを電気出力信号へ変換させる形態とされており、及び

該アクティブ電子回路が該光検知器と関連していてそれから該出力電気信号を受け取り且つ該電気出力信号を処理して前記処理済電気信号を出力する形態とされている、システム。

【請求項28】

該ソース信号及び該電気出力信号の各々が、少なくとも5Gb/sのレートで変調されている請求項27記載のシステム。

【請求項29】

該光検知器及び該アクティブ電子回路が、同じ程度の大きさである厚さを有している請求項27記載のシステム。

【請求項30】

該光検知器が、該半導体基板へ向かって延在する複数個の穴を包含しているフォトン吸収領域を有しており、複数の穴が同じソース信号を同時に受け取る形態とされている請求項27記載のシステム。

【請求項31】

高度にドーピングされたP層及びN層が該フォトン吸収領域の側面に位置しており、及び該フォトン吸収領域は0.1〜5.0マイクロメートルの範囲内の厚さを有しており且つ意図的にはドーピングされていないか又は該P及びN領域と比較して軽度ドーピングされている請

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求項 27 記載のシステム。

【請求項 32】

該光検知器がバイアスされて電子又は正孔の内の少なくとも一方を該ソース信号が該光検知によって受け取られる方向に沿う方向に引きさせる請求項 27 記載のシステム。

【請求項 33】

該光検知器及び該アクティブ電子回路の各々がシリコンをベースとしている請求項 27 記載のシステム。

【請求項 34】

該光検知器がアバランシェ光検知器である請求項 27 記載のシステム。

【請求項 35】

マイクロストラクチャ向上型光吸収を有する光検知器において、

0.5 及び 5 マイクロメートルの間の厚さを持っており且つデータ通信用に変調されたソース信号から光子を吸収し且つそれに対応する出力電気信号を供給する形態とされている光子吸収領域が設けられており、

前記光子吸収領域は複数個の穴を有しており、該複数個の穴は該光子吸収領域の該厚さの少なくとも一部を介して延在しており且つ複数の該穴において同じソース信号を同時に受け取る形態とされており、及び

前記光子吸収領域は、800 nm 乃至 900 nm 及び 1400 nm 乃至 1700 nm の範囲の内の少なくとも一つにおける波長において該入射ソース信号を 40 % を越えて受け取り且つそれに対応する出力電気信号を供給する形態とされている。

光検知器。

【請求項 36】

該光子吸収領域は、800 nm 乃至 900 nm の波長において該入射ソース信号を 40 % を越えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項 35 記載の光検知器。

【請求項 37】

該光子吸収領域は、800 nm 乃至 900 nm の波長において該入射ソース信号を 50 % を越えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項 35 記載の光検知器。

【請求項 38】

該光子吸収領域は、800 nm 乃至 900 nm の波長において該入射ソース信号を 60 % を越えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項 35 記載の光検知器。

【請求項 39】

該光子吸収領域は、1400 nm 乃至 1700 nm の波長において該入射ソース信号を 40 % を越えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項 35 記載の光検知器。

【請求項 40】

該光子吸収領域は、1400 nm 乃至 1700 nm の波長において該入射ソース信号を 50 % を越えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項 35 記載の光検知器。

【請求項 41】

該光子吸収領域は、1400 nm 乃至 1700 nm の波長において該入射ソース信号を 60 % を越えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項 35 記載の光検知器。

【請求項 42】

該光子吸収領域は、800 nm 乃至 900 nm のソース信号波長の少なくとも 20 nm の波長スパンにわたって 20 % 未満だけ変化する吸収百分率において該入射ソース信号を吸収する形態とされている請求項 35 記載の光検知器。

【請求項 43】

該フォトン吸収領域は、1400nm乃至1700nmのソース信号波長の少なくとも20nmの波長スパンにわたって20%未満だけ変化する吸収百分率において該入射ソース信号を吸収する形態とされている請求項35記載の光検知器。

【請求項44】

各穴が該基板の上部表面に平行な断面を有しており且つ400nmと2500nmとの間の最大寸法を有しており、及び各穴は該複数個の穴の内の最も近くに隣接する穴の中心から3500nm未満だけ離隔されている中心を有している請求項35記載の光検知器。

【請求項45】

前記光検知器は、更に、 $10^{18}/\text{cm}^3$ において又はそれを越えて高度にドーピングされており且つ前記フォトン吸収領域の側面に位置しているP層とN層とを有しており、及び該フォトン吸収領域は軽度ドーピングされているか又は意図的にはドーピングされおらず高々 $10^{16}/\text{cm}^3$ である請求項35記載の光検知器。

【請求項46】

前記光検知器がアバランシェ光検知器を有している請求項35記載の光検知器。

【請求項47】

該フォトン吸収領域がSiを有している請求項35記載の光検知器。

【請求項48】

該フォトン吸収領域がGeを有している請求項35記載の光検知器。

【請求項49】

該光検知器が、前記ソース信号を担持するオプティカルファイバーを受け付け且つ該ファイバーの一端部を前記フォトン吸収領域から選択した距離に維持する形態とされているテーパ付き又は段差付きの穴を有している請求項35記載の光検知器。

【請求項50】

更に、該ファイバーの前記端部と該フォトン吸収領域との間にレンズを包含している請求項49記載の光検知器。

【請求項51】

該光検知器が、該ソース信号の複数の反射を発生させて前記ソース信号が該フォトン吸収領域を複数回横断する形態とされている反射構造を有している請求項35記載の光検知器。

【請求項52】

該光検知器が、該フォトン吸収領域の2つの対応する側部から該ソース信号を受け取る形態とされている請求項35記載の光検知器。

【請求項53】

マイクロストラクチャ向上型光吸収を具備する光検知器において、

カソード領域、

アノード領域、

前記カソード領域が前記アノード領域よりも一極正の電圧へ駆動されるように前記カソード領域と前記アノード領域との間に電圧を印加させる形態とされている逆バイアス回路

上部表面を持っている基板物質、及び

該カソード領域及び該アノード領域と動作上関連しており且つソース信号からのフォトンを吸収する形態とされておりシリコンから構成されているフォトン吸収領域であって、各々が該上部基板表面と平行であり400nmと2500nmとの間の最大寸法を持っている複数個の穴であって各穴が該複数個の穴の最も近い隣接した穴の中心から3500nm未満だけ離隔されている中心を持っている該複数個の穴を有している該フォトン吸収領域、

を有している光検知器。

【請求項54】

該ソース信号が800nmより大きく且つ1000nmより小さい波長を持っている請求項53記載の光検知器。

【請求項 5 5】

該複数個の穴が周期的に離隔されているアレイに配置されている請求項 5 3 記載の光検知器。

【請求項 5 6】

該周期的に離隔されているアレイが六角形又は正方形の格子パターンを有している請求項 5 5 記載の光検知器。

【請求項 5 7】

該複数個の穴が、前記ソース信号の波長を含む波長範囲において、穴は無いがその他は同一である光検知器と比較してフォトンの吸収を向上させる請求項 5 3 記載の光検知器。

【請求項 5 8】

該穴の各々が該上部基板表面と平行である支配的に円形状の断面を持っている請求項 5 3 記載の光検知器。

【請求項 5 9】

該カソード領域及び該アノード領域が集積回路エレクトロニクスへ動作接続されており、且つ該光検知器及び該集積回路エレクトロニクスが単一のシリコンチップに集積化されている請求項 5 3 記載の光検知器。

【請求項 6 0】

該集積回路エレクトロニクスが、相互インピーダンス増幅器、信号処理エレクトロニクス、及びルーチングエレクトロニクスからなるグループから選択される一つ又はそれ以上のタイプを包含している請求項 5 9 記載の光検知器。

【請求項 6 1】

該光検知器と関連している容量が、そのアノード領域とカソード領域とを従来のボンダパッドへ動作接続させているその他は同一の光検知器と比較して、減少されている請求項 5 9 記載の光検知器。

【請求項 6 2】

更に、シリコンから形成されている増倍領域を有しており、及び
該光検知器が、850nmのソース信号波長において5Gb/sよりも大きなデータ帯域幅で該ソース信号を検知する形態とされており、且つ2より大きな利得を有しているアバランシェフォトダイオードである、請求項 5 3 記載の光検知器。

【請求項 6 3】

前記光検知器が、少なくとも30%の量子効率で、850nmのソース信号波長において2、5Gb/sよりも大きなデータ帯域幅で前記ソース信号を検知する形態とされている請求項 5 3 記載の光検知器。

【請求項 6 4】

前記光検知器が、少なくとも50%の量子効率で、850nmのソース信号波長において2、5Gb/sよりも大きなデータ帯域幅で前記ソース信号を検知する形態とされている請求項 5 3 記載の光検知器。

【請求項 6 5】

前記光検知器が、少なくとも30%の量子効率で、850nmのソース信号波長において5Gb/s以上のデータ帯域幅で前記ソース信号を検知する形態とされている請求項 5 3 記載の光検知器。

【請求項 6 6】

前記光検知器が、少なくとも50%の量子効率で、850nmのソース信号波長において5Gb/s以上のデータ帯域幅で前記ソース信号を検知する形態とされている請求項 5 3 記載の光検知器。

【請求項 6 7】

該複数個の穴がシリコンの一部をエッチング除去することによって形成されている請求項 5 3 記載の光検知器。

【請求項 6 8】

該光検知器は、該ソース信号の一部が該フォトン吸収領域を1回目に通過し、或る表面

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で反射し、且つ、その後、該光吸収領域を2回目に通過する形態とされている請求項53記載の光検知器。

【請求項69】

更に、基板を包含しており、及び

該カソード領域、該吸収領域、及び該アノード領域が該基板の上方に形成されており且つ該光検知器が該基板と反対の該光検知器の側部に面する方向から該ソース信号を受け取る形態とされている、請求項53記載の光検知器。

【請求項70】

マイクロストラクチャ向上型光吸収を具備している光検知器において、

カソード領域、

アノード領域、

前記カソード領域が前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域と前記アノード領域との間に電圧を印加する形態とされている逆バイアス回路、上部表面を持っている基板物質、及び

前記カソード領域及び前記アノード領域と動作上関連しており且つソース信号からのフォトン吸収する形態とされているゲルマニウムを基礎とする物質から構成されているフォトン吸収領域であって、前記ゲルマニウムを基礎とする吸収領域は各々が該上部基板表面と平行で750nmと3000nmとの間の最大寸法を持っている断面を有している複数個の穴を包含しており、且つ各穴は該複数個の穴の内の最も近くに隣接する穴の中心から5000nm未満だけ離隔している中心を有している該フォトン吸収領域、を有している光検知器。

【請求項71】

該ゲルマニウムを基礎とするフォトン吸収層が、シリコンからなる物質の一つ又はそれ以上の層の上方に、エピタキシャル成長及びエピタキシャル横過剰成長プロセスの内の少なくとも一つによって形成されている請求項70記載の光検知器。

【請求項72】

更に、最上シリコン層の上にGeの結晶成長を開始させる形態とされているGeバッファ層を有している請求項71記載の光検知器。

【請求項73】

該アノード領域が、エピタキシャル成長及びエピタキシャル横過剰成長プロセスの内の少なくとも一つによって形成されているPドープゲルマニウム層を有している請求項70記載の光検知器。

【請求項74】

前記光検知器がアバランシェフォトダイオードであり、且つ、更に、シリコンから形成されている増倍領域を有している請求項70記載の光検知器。

【請求項75】

該ソース信号が1200nmよりも大きく且つ1900nmより小さな波長を有している請求項70記載の光検知器。

【請求項76】

該ソース信号が1400nmより大きな波長を有している請求項75記載の光検知器。

【請求項77】

前記光検知器が、少なくとも30%の量子効率で、1550nmのソース信号波長において、2Gb/sよりも大きなデータ帯域幅において、前記ソース信号を検知する形態とされている請求項70記載の光検知器。

【請求項78】

前記光検知器が、少なくとも50%の量子効率で、1550nmのソース信号波長において、2Gb/sよりも大きなデータ帯域幅において、前記ソース信号を検知する形態とされている請求項70記載の光検知器。

【請求項79】

前記光検知器が、少なくとも30%の量子効率で、1550nmのソース信号波長にお

いて、5 G b/sよりも大きなデータ帯域幅において、前記ソース信号を検知する形態とされている請求項70記載の光検知器。

【請求項80】

前記光検知器が、少なくとも50%の量子効率で、1550 nmのソース信号波長において、5 G b/sよりも大きなデータ帯域幅において、前記ソース信号を検知する形態とされている請求項70記載の光検知器。

【発明の詳細な説明】

【技術分野】

【0001】

本特許出願は以下の仮出願の各々の優先権を主張し且つ引用により本書に取り込むこととする。

【0002】

米国仮出願番号62/081, 538号；2014年11月18日出願
 米国仮出願番号62/090, 879号；2014年12月11日出願
 米国仮出願番号62/100, 025号；2015年1月5日出願
 米国仮出願番号62/111, 582号；2015年2月3日出願
 米国仮出願番号62/139, 511号；2015年3月27日出願
 米国仮出願番号62/153, 443号；2015年4月27日出願
 米国仮出願番号62/154, 675号；2015年4月29日出願
 米国仮出願番号62/157, 876号；2015年5月6日出願
 米国仮出願番号62/171, 915号；2015年6月5日出願
 米国仮出願番号62/174, 498号；2015年6月11日出願
 米国仮出願番号62/175, 855号；2015年6月15日出願
 米国仮出願番号62/182, 602号；2015年6月21日出願
 米国仮出願番号62/188, 876号；2015年7月6日出願
 米国仮出願番号62/197, 120号；2015年7月27日出願
 米国仮出願番号62/199, 607号；2015年7月31日出願
 米国仮出願番号62/205, 717号；2015年8月15日出願
 米国仮出願番号62/209, 311号；2015年8月24日出願
 米国仮出願番号62/213, 556号；2015年9月2日出願
 米国仮出願番号62/232, 716号；2015年9月25日出願

本特許出願は以下の仮及び非仮出願に関連しており、その各々を引用により本書に取り込むこととする。

【0003】

国際特許出願番号PCT/US13/39208；2014年5月22日出願
 米国仮出願番号61/826, 446号；2013年5月22日出願
 米国仮出願番号61/834, 873号；2013年6月13日出願
 米国仮出願番号61/843, 021号；2013年7月4日出願
 米国仮出願番号61/905, 109号；2013年11月15日出願
 米国仮出願番号62/017, 915号；2014年6月27日出願

上に引用した仮及び非仮特許出願の全ては、本書において、「共通に譲渡され組み込まれている出願」として集約的に引用される。

【0004】

本特許明細書は、大略、感光装置に主に関連する発明を提示する。更に詳細には、幾つかの実施例はマイクロストラクチャ向上型吸収特性を具備している感光装置に関連している。

【背景技術】

【0005】

オプティカルファイバー通信は、遠隔通信及び大型データセンター内の通信等の適用例において広く使用されている。一層短い光学的波長を使用した場合に関連する減衰損失のた

めに、殆どのオプティカルファイバー通信は800nm以上の光学的波長を使用している。一般的に使用される通信窓が800nmと1675nmとの間に存在している。オプティカルファイバー通信システムにおいて使用される光学的受信機の主要な部品は光検知器であって、それは、通常、フォトダイオード(PD)又はアバランシェフォトダイオード(APD)の形態である。

【0006】

高品質で低ノイズのAPDはシリコンから構成することが可能である。しかしながら、シリコンは可視光及び近赤外範囲における光を吸収するが、それは一層長い光学的波長において一層透明性となる。シリコンPD及びAPDは、該装置の吸収「1」領域の厚さを増加させることによって800nm以上の光学的波長用とさせることが可能である。しかしながら、適切な量子効率を得るためには、シリコン「1」領域の厚さが、該装置の最大帯域幅が多く現在の及び将来の遠隔通信及びデータセンター適用網に対して低すぎるものとなるほど非常に大きくなる。

【0007】

一層長い波長及び一層高い帯域幅の場合にシリコンPD及びAPDが有している本来的な問題を回避するために、その他の物質が使用される。ゲルマニウム(Ge)は1700nmの波長まで赤外を検知するが、比較的高い増倍ノイズ(multiplication noise)を有している。InGaAsは1600nmよりも一層長いもので検知することが可能であり且つGeよりも増倍ノイズは少ないが、シリコンよりもかなり一層大きな増倍ノイズを有している。InGaAsは、最も典型的には基板として且つ増倍層としてInPが関与するヘテロ構造ダイオードの吸収領域として使用されることが知られている。この物質系は略900乃至1700nmの吸収率と適合性がある。しかしながら、両方のInGaAs装置は比較的高価であると共にシリコンと比較した場合に比較的高い増倍ノイズを有しており、且つ単一チップとしてSiエレクトロニクスと集積化させることは困難である。

【0008】

光検知器の事業における主要な会社によって公表されている情報(http://files.shareholder.com/downloads/FN5R/0x0x382377/0b3893ea-fb06-417d-ac71-84f2f9084b0d/Finisar_Investor_Presentation.pdf参照)が10頁において示していることは、光学的通信装置用の現在の市場は70億米ドルを越えており複合年成長率は1.2%であることです。850nm波長用で使用されているフォトダイオード(PD)はGaAs物質を使用しており、且つ1550nm波長用には、フォトダイオードはInP物質をベースとしており、それは高価であると共にSiをベースとしたエレクトロニクスと集積化させることは困難である。従って、そこには大きな市場があり且つより良い装置の開発が満たされていない長きに亘る必要性が存在している。今日までのところ、850nm用のSi物質をベースとしたフォトダイオードもアバランシェフォトダイオード(APD)も存在しておらず、且つ上部又は底部照射型でデータレートが5Gb/s以上であり、本発明者等の知る限りによれば市販されている1550nm用のGe・オン・Si(Ge on Si)物質をベースとしたフォトダイオードもアバランシェフォトダイオードも存在しない。しかしながら、この様な大きな市場に対してより良い装置を開発しようとする努力が欠如していたわけでもない。例えば、Si物質内に製造される共振フォトダイオードに対する提案がなされている(エピタキシャル横過剰成長によって成長された共振キャビティ向上型高速Siフォトダイオード(Resonant Cavity Enhanced High-Speed Si Photodiodes Grown by Epitaxial Lateral Overgrowth), Schaub et al., IEEEフォトニクステクノロジーレターズ、11巻、No. 12、1999年12月)が、それは該市場で認知されるようになったものではない。導波路形態におけるその他の形式の高速フォトダイオードが提案されており、例えば、基準40GHz Si/Ge単一走行キャリア導波路フォトダイオード(Ref. 40 GHz Si/Ge uni-travelling carrier waveguide photodiode), Plets et al., DO I: 10.1109/JLT.2014.2310780、ジャーナル・オブ・ライトウエーブ・テクノロジー;モノリシックGe/Siアバランシェフォトダイオード(Monoli

thic Ge/Si Avalanche Photodiodes), Kang et al., 9 7 8—1—4 2 4 4—4 4 0 3—8 / 0 9 / \$ 2 5, 0 0 著作権 2 0 0 9 J E E E ; 大断面シリコン・オン・インシュレータ導波路とモノリシックに集積化された高速 Ge 光検知器 (High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide), Feng et al., アプライドフィジックスレターズ 9 5, 2 6 1 1 0 5 (2 0 0 9) ; doi : 1 0. 1 0 6 3 / 1. 3 2 7 9 1 2 9 ; におけるものがあり、その場合に、光は端部から光学的導波路内に結合され且つ吸収長は 1 5 5 0 nm における Ge の弱い吸収係数を補償するために 1 0 0 μ m 以上とさせることが可能である。これらの以前に提案されている導波路フォトダイオード構造においては、光は導波路の長さに沿って伝播し且つ光の伝播方向と電界の方向とが支配的に垂直であるように P I N 導波路を横断して電界が印加される。S i 内において光は電子／正孔の飽和速度よりも約 1 0 0 0 倍一瞬速く進行するので、導波路 P D は、例えば、2 0 0 ミクロンの長さとし且つ P I N における「I」は、例えば、2 ミクロンとすることが可能であり、且つ 1 0 G b / s を越える帯域幅を達成することが可能である。この様な光の端部結合は、この特許明細書に記載されるような表面照射と比較してパッケージングにおいてコスト高であり、その場合に、導波路断面の寸法は典型的に数ミクロンであるの対比して既知の表面照射型フォトダイオード又はアバランシェフォトダイオードの場合には数十ミクロンである。既知の導波路 P D / A P D は、しばしば、単一モード光学系であるに過ぎず、一方、本特許明細書に記載される表面照射型 P D / A P D は単一及びマルチモードの両方の光学系で使用することが可能である。更に、既知の導波路フォトダイオードはウエハレベルにおいてテストすることが困難であるが、一方、本特許明細書に記載される表面照射型フォトダイオードはウエハレベルにおいて容易にテストすることが可能である。既知の導波路フォトダイオード／アバランシェフォトダイオードは、殆どが、特別のフォトリソグラフィ回路において使用されるものであって広く市場で入手可能なものではない。S i と集積化させることが可能な上部又は底部照射型の S i 及び Ge・オン・S i の P D / A P D は、8 5 0 nm 及び 1 5 5 0 nm の波長において 5 G b / s 又はそれ以上のデータレートのものがあることは知られている。対照的に、この特許明細書に記載されている如く S i をベースとした物質上のフォトダイオードは、単一 S i チップ上の集積化電子回路とモノリシックに集積化させることが可能であり、その際にパッケージングのコストを著しく減少させる。更に、本特許明細書に記載される 8 5 0 nm の公称波長におけるマイクロストラクチャ型 P D / A P D は支配的に短距離用のものとすることが可能であり、例えば、1 メートル未満、及び或る場合には 1 0 メートル未満、及び或る場合には 1 0 0 メートル未満、及び或る場合には 1 0 0 0 メートル未満の光学的データ伝送の距離とすることが可能である。入射光学ビームのマイクロストラクチャ型 P D / A P D 方向及び P I N 又は N I P 構造の「I」領域における電界は支配的に共線状であるか及び／又は略共線状である。この特許明細書はこの様な装置を可能なものとさせ且つ現在のデータセンターをブレード間において及び／又は 1 個のブレード内において殆ど全てを光学的データ伝送へ変換させるものと予測され、そのことはデータ伝送帯域幅能力を著しく増加させると共に電力消費を著しく減少させるものである。

【0009】

本書の特許請求の範囲に記載される要旨はいずれか特定の欠点を解消する実施例又は上述したような環境においてのみ動作する実施例に限定されるものではない。そうではなく、この背景は、本書に記載される幾つかの実施例を実施することが可能な一つの例示的な技術分野を例示するために与えられているものである。

【先行技術文献】

【非特許文献】

【0010】

【非特許文献 1】エピタキシャル横過剰成長によって成長された共振キャビティ向上型高速 S i フォトダイオード (Resonant Cavity Enhanced High-Speed Si Photodiodes Grown by Epitaxial Lateral Overgrowth), Schaub et al., J E E E フォトニクステクノロ

ジャーナルズ、11巻、No. 12、1999年12月

【非特許文献2】基準40GHz Si/Ge単一進行キャリア導波路フォトダイオード (Ref. 40 GHz Si/Ge uni-travelling carrier waveguide photodiode)、Piels et al., DOI: 10.1109/JLT.2014.2310780、ジャーナル・オブ・ライトウェーブ・テクノロジー

【非特許文献3】モノリシックGe/Siアバランシェフォトダイオード (Monolithic Ge/Si Avalanche Photodiodes)、Kang et al., 978-1-4244-4403-8/09/\$25.00 著作権2009 IEEE

【非特許文献4】大断面シリコン・オン・インシュレータ導波路とモノリシックに集積化された高速Ge光検知器 (High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide)、Feng et al., アプライドフィジックスレターズ95、261105 (2009)

【非特許文献5】doi: 10.1063/1.3279129

【発明の概要】

【発明が解決しようとする課題】

【0011】

幾つかの実施例によれば、データ通信用の集積化検知器／プロセッサ回路が、マイクロストラクチャ向大型光吸収を具備する光検知器、及び単一の半導体チップに形成されている電子的プロセッサを有している。

【課題を解決するための手段】

【0012】

該単一チップには、データ通信用に変調された光学的ソース信号からの光子を吸収し且つそれに対応する出力電気信号を供給する形態とされている光子吸収領域を具備している半導体基板上に形成されている光検知器が設けられており、該光子吸収領域は前記基板へ向かってその中を延在している複数個の穴であって該穴の複数において該同一のソース信号を同時に受け取る形態とされている該複数個の穴を有しており、電子的プロセッサも前記半導体基板上に形成されていて前記光子吸収領域と動作上関連して前記出力電気信号を受け取ってそれを処理済出力へ処理し、それにより該光学的ソース信号を受け取り且つ該処理済出力を出力する単一の半導体チップを形成しており、前記光子吸収領域及び前記電子的プロセッサは同じ大きさの程度の夫々の厚さを有しており、且つカソード領域とアノード領域とが前記光子吸収領域及び逆バイアス回路と動作上関連しており、該逆バイアス回路は前記カソード領域が前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域とアノード領域との間に電圧を印加させる形態とされている。

【0013】

該光子吸収領域の厚さは、好適には、0.5乃至5 μm の範囲内である。該電子的プロセッサは、相補的金属酸化物半導体 (CMOS) 装置、バイポーラ (Bi) 装置、及びBi CMOS装置の内の少なくとも一つを有している応用特定集積回路 (ASIC) とすることが可能である。該光子吸収領域は、800 nm乃至900 nm、又は1400 nm乃至1700 nmの波長において入射ソース信号の40%、又は50%、又は60%を越えて吸収し、且つそれに対応する出力電気信号を供給する形態とさせることが可能である。該光子吸収領域は、800 nm乃至900 nm、又は1400 nm乃至1700 nmのソース信号波長の少なくとも20 nmの選択した波長範囲に亘って20%未満だけ変動する吸収百分率において該入射ソース信号を供給する形態とさせることが可能である。

【0014】

各穴は、400 nmと2500 nmとの間の最大寸法を有しており該基板の表面に対して平行な断面を有することが可能であり、且つ各穴は該複数個の穴の内の最も近い隣接する穴の中心から3500 nm未満だけ離隔されている中心を有することが可能である。該光検知器は、好適には、更に、 $10^{13}/\text{cm}^3$ において又はそれを越えて高度にドーブ

されており且つ前記フォトン吸収領域の側面に位置しているP層及びN層を有しており、且つ該フォトン吸収領域は、好適には、軽度ドーピングされているか又は意図的にドーピングされておらず高々 $10^{16}/\text{cm}^3$ である。該光検知器はアバランシェ光検知器を有することが可能であり、且つ該フォトン吸収領域はSi及びGeの内の少なくとも一つを有することが可能である。該光検知器は、前記ソース信号を担持するオプティカルファイバーを受け付け且つ該ファイバーの端部を前記フォトン吸収領域から選択した距離に維持する形態とされているテーパ付き又は段差付きの穴を有することが可能である。該ファイバーの前記端部と該フォトン吸収領域との間にレンズを包含させることが可能である。該光検知器は、更に、該ソース信号の多数回の反射を発生させそれにより前記ソース信号を該フォトン吸収領域を多数回横断させる形態とされている反射構造を有することが可能である。該光検知器は該フォトン吸収領域の2つの反対側から該ソース信号を受け取る形態とさせることが可能であり、且つ前記穴は、該穴の複数のグループにおいて光を電気信号へ変換させる場合の結合共振を発生させてそれによりソース信号吸収を向上させる形態とさせることが可能である。

【0015】

1個又はそれ以上の付加的な光検知器を前記半導体基板上に形成することが可能であり、それは夫々の付加的なソース信号を受け取り且つそれに対応する夫々の出力電気信号を供給する夫々のフォトン吸収領域を具備しており、又、1個又はそれ以上の付加的な電子のプロセッサを前記半導体基板上に形成し且つ前記夫々の出力電気信号をそれから受け取り且つ処理するために前記付加的な光検知器の夫々のフォトン吸収領域と動作上関連させることも可能である。該複数の穴は、前記ソース信号の波長を含む複数の波長の範囲において穴が無いがその他は同一の光検知器と比較してフォトンの吸収を向上させる形態とさせることが可能である。該電子のプロセッサは、相互インピーダンス増幅器、信号処理エレクトロニクス、及びルーチングエレクトロニクスからなるグループから選択した1個又はそれ以上のタイプを包含することが可能である。該光検知器と関連する容量は、アノード領域及びカソード領域を従来のボンダッドへ動作上接続させているその他は同一の光検知器と比較して減少されている。該光検知器は、更に、増倍領域を有することが可能であり、それはアバランシェフォトダイオードをして800乃至900nmのソース信号波長において10ギガビット/sよりも大きなデータ帯域幅で該ソース信号を検知する形態とさせ、且つ2よりも大きな利得を具備している。

【0016】

幾つかの実施例においては、光学的/電子的システムにおいて、光検知器とアクティブ電子回路とが設けられており、それらは同一の半導体基板上に構築されており且つ互いに動作上関連付けられていて単一の集積回路チップを形成しており、Gb/sレートでの情報を担持する該光学的ソース信号を発生させるためにデータのGb/sレートで変調されるレーザが設けられており、且つその入力端において該光学的ソース信号を受け取り且つそれをその出力端へ送るために該レーザと関連してオプティカルファイバーが設けられており、その場合に、該光検知器は該光学的ソース信号を受け取るために該オプティカルファイバーの該出力端と関連しており且つそれを電気的出力信号へ変換させる形態とされており、且つ該アクティブ電子回路は該出力電気信号を受け取るために該光検知器と関連しており且つ該電気出力信号を処理し且つ前記処理済の電気信号を出力する形態とされている。該ソース信号及び該電気的出力信号の各々は少なくとも5Gb/sのレートで変調させることが可能である。該光検知器及び該アクティブ電子回路は同じ程度の大きさの厚さを有することが可能である。該光検知器は、該半導体基板へ向かって延在している複数の穴を包含しているフォトン吸収領域を有することが可能であり、その場合に、複数の穴が同一のソース信号を同時的に受け取る形態とされている。高度にドーピングしたP層及びN層が該フォトン吸収領域の側面に位置することが可能であり、且つ該フォトン吸収領域は0、1乃至5、0µmの範囲内の厚さを有することが可能であり且つ、好適には、意図的にはドーピングされていないか又はP領域及びN領域と比較して軽度ドーピングされている。該光検知器は、該光検知器によって該ソース信号が受け取られる方向に沿う方向において電子又

は正孔を指引きさせるべくバイアスさせることが可能である。該光検知器及び該アクティブ電子回路の各々はシリコンをベースとしたものとすることが可能である。該光検知器はアバランシェ光検知器とすることが可能である。

【0017】

幾つかの実施例において、マイクロストラクチャ向上型光吸収を具備している光検知器が、好適には0.5 μm と5 μm との間の厚さを具備しており且つデータ通信用に変調されたソース信号からフォトンを吸収し且つそれに対応する出力電気信号を供給する形態とされているフォトン吸収領域を有しており、前記フォトン吸収領域は該フォトン吸収領域の厚さの少なくとも一部を介して延在している複数の穴であって該穴の複数において同一のソース信号を同時的に受け取る形態とされている該複数の穴を有しており、且つ前記フォトン吸収領域は800 nm乃至900 nm及び1400 nm乃至1700 nmの範囲の内の少なくとも一つにおける波長において入射ソース信号の40%を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている。該フォトン吸収領域は、800 nm乃至900 nm又は1400 nm乃至1700 nmのソース信号波長の少なくとも20 nmの波長範囲に亘り20%未満だけ変化する吸収百分率において入射ソース信号を吸収する形態とさせることが可能である。

【0018】

各穴は、好適には、400 nmと2500 nmとの間の最大寸法を有する該基板の上部表面と平行な断面を有しており、且つ各穴は、好適には、該複数の穴の内の最も近くに隣接する穴の中心から3500 nm未満だけ離隔されている中心を有している。該光検知器は、更に、P層及びN層を有しており、それらは、好適には、 $10^{18}/\text{cm}^3$ での又はそれを越えて高度にドーピングされており且つ前記フォトン吸収領域の側面に位置しており、且つ該フォトン吸収領域は、好適には、意図的にはドーピングされていないか又は高々 $10^{18}/\text{cm}^3$ で軽度ドーピングされている。該光検知器はアバランシェ光検知器を有することが可能である。該フォトン吸収領域はSi又はGeを有することが可能である。該光検知器は、前記ソース信号を担持しているオプティカルファイバーを受け付け且つ該ファイバーの端部を前記フォトン吸収領域から選択された距離に維持する形態とされているテーパ付き又は段差付きの穴を有することが可能であり、且つ該ファイバーの前記端部と該フォトン吸収領域との間にレンズを包含させることが可能である。該光検知器は、該ソース信号の多数回の反射を発生させそれにより該フォトン吸収領域を前記ソース信号で多数回横断させる形態とされている反射構造を有することが可能である。該光検知器は、該フォトン吸収領域の2つの反対側の側部から該ソース信号を受け取る形態とさせることが可能である。

【0019】

幾つかの実施例において、マイクロストラクチャ向上型光吸収を具備する光検知器は、カソード領域、アノード領域、前記カソード領域が前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域と前記アノード領域との間に電圧を印加する形態とされている逆バイアス回路、上部表面を具備している基板物質、及び該カソード領域とアノード領域とに動作上関連しており且つソース信号からフォトンを吸収する形態とされておりシリコンから構成されているフォトン吸収領域、を有しており、前記シリコン吸収領域は各々が400 nmと2500 nmとの間の最大寸法を持っている該上部基板表面と平行な断面を持っている複数の穴を包含しており、且つ各穴は該複数の穴の内の最も近くに隣接する穴の中心から3500 nm未満だけ離隔されている。該ソース信号は800 nmよりも大きく且つ1000 nmよりも小さい波長を有することが可能である。該複数の穴は、六角形又は正方形の格子パターンを有することが可能な周期的に離隔されたアレイに配列させることが可能である。該複数の穴は、穴の無いものと比較してフォトンの吸収を向上させるが、その他は、前記ソース信号の波長を含む波長の範囲において同じ光検知器である。該穴の各々は該上部基板表面と平行な支配的に円形状の断面を有することが可能である。該カソード領域及びアノード領域は集積回路エレクトロニクスへ動作接続させることが可能であり、且つ該光検知器及び集積回路エレクトロニクスは単一のシリ

コンチップに集積化させることが可能であり、その場合に、該集積回路エレクトロニクスは相互インピーダンス増幅器、信号処理エレクトロニクス、及びルーチングエレクトロニクスからなるグループから選択される一つ又はそれ以上のタイプを包含することが可能である。該光検知器と関連する容量は、そのアノード領域とカソード領域とを従来のボンダパッドへ動作接続させているその他は同じ光検知器と比較して、減少させることが可能である。該光検知器は、更に、シリコンから形成される増倍領域を有することが可能であり、その場合に、該光検知器は、2より大きい利得を持っており、850nmのソース信号波長において5Gb/sよりも大きなデータ帯域幅において該ソース信号を検知する形態とされているアバランシェフォトダイオードである。該光検知器は、量子効率が少なくとも30%又は50%で850nmのソース信号波長において2、5Gb/s以上か又は5Gb/s以上のデータ帯域幅において前記ソース信号を検知する形態とさせることが可能である。該複数個の穴はシリコンの一部をエッチング除去することによって形成させることが可能である。該光検知器は、該ソース信号の一部が最初に該フォトン吸収領域を通過し、表面から反射し、その後該フォトン吸収領域を再度通過するような形態とさせることが可能である。該光検知器は、更に、基板を包含することが可能であり、その場合に、該カソード、吸収及びアノード領域は該基板の上方に形成し且つ該光検知器は該基板と反対側の該光検知器の側部に面する方向から該ソース信号を受け取る形態とされる。

【0020】

幾つかの実施例においては、マイクロストラクチャ向上型光吸収を具備する光検知器は、カソード領域、アノード領域、前記カソード領域か前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域とアノード領域との間に電圧を印加する形態とされている逆バイアス回路、上部表面を具備している基板物質、及び該カソード領域及びアノード領域と動作上関連しており且つソース信号からのフォトンを取り込む形態とされておりゲルマニウムをベースとした物質から構成されているフォトン吸収領域、を有しており、前記ゲルマニウムをベースとした吸収領域は各々が750nmと3000nmとの間の最大寸法を持っており該上部基板表面と平行な断面を持っている複数個の穴を包含しており、且つ各穴は該複数個の穴の内の最も近くに隣接する穴の中心から5000nm未満だけ離隔されている中心を有している。該ゲルマニウムをベースとしたフォトン吸収層は、シリコンからなる物質の一つ又はそれ以上の層の上にエピタキシャル成長及びエピタキシャル横方向過剰成長(epitaxial lateral overgrowth)プロセスの内の少なくとも一つによって形成させることが可能である。該光検知器は、更に、最上シリコン層の上にGeの結晶成長を開始させる形態とされたGeバッファ層を有することが可能である。該光検知器のアノード領域は、エピタキシャル成長及びエピタキシャル横方向過剰成長プロセスの内の少なくとも一つによって形成されるpドープゲルマニウム層を有することが可能である。該光検知器はアバランシェフォトダイオードとすることが可能であり、且つ、更に、シリコンから形成される増倍領域を有することが可能である。該ソース信号は、1200nmよりも大きく且つ1900nmよりも小さいか、又は1400nmよりも大きな波長を有することが可能である。該光検知器は、量子効率が少なくとも30%か又は50%で1550nmのソース信号波長において2Gb/s又は5Gb/sよりも大きなデータ帯域幅において前記ソース信号を検知する形態とさせることが可能である。

【0021】

本書において使用されているように、「及び (and)」、「又は (or)」、及び「及び／又は (and/or)」等の文法上の接続詞は、全て、それらが接続する事例、客体、主体の内の一つ又はそれ以上が発生するか又は存在している場合があることを表すことを意図している。この様に、本書において使用されているように、全ての場合においての用語「又は (or)」は「排他的又は (exclusive or)」の意味ではなく「包括的又は (inclusive or)」の意味を表している。

【0022】

本書において使用されているように、「1個の穴 (hole)」又は「複数の穴 (holes)」という用語は一つの物質又は複数の物質の中へ又は貫通している何らかの開口のことを

意味している。一般的に、該開口は、円形、楕円、多角形、及びランダム形状を含む任意の形状及び断面を有することが可能である。

【0023】

この特許明細書の要旨の上述した及びその他の利点及び特徴を更に明確にさせるために、その実施形態の特定の例を添付図面に例示してある。理解すべきことであるが、これらの図面は単に例示的实施例を図示するに過ぎず、従ってこの特許明細書又は特許請求の範囲を制限するものと考えらるべきものではない。本書の要旨を添付図面の使用を介して付加的な特定性及び詳細と共に記載し且つ説明する。

【図面の簡単な説明】

【0024】

【図1】幾つかの実施例に基づいてマイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードを使用することが可能な光学的データ伝送システムを例示している概略図。

【図2】幾つかの実施例に基づいてマイクロストラクチャ型フォトダイオード（MS-PD）及びマイクロストラクチャ型アバランシェフォトダイオード（MS-APD）と共に包含される波長選択要素を示している概略図。

【図3】幾つかの実施例に基づいてマルチ波長選択要素を具備しているMS-PD／APDを示している概略図。

【図4】（A）乃至（D）は幾つかの実施例に基づく種々のバンドパスフィルタ特性を示している各プロット。

【図5】幾つかの実施例に基づく粗波長分割多重（CWDM）形態を示している概略図。

【図6】（A）及び（B）は幾つかの実施例に基づくマイクロストラクチャ型フォトダイオードの幾つかの基本的な部分を示している各概略図。

【図7】（A）及び（B）は幾つかの実施例に基づく底部照射型フォトダイオードの幾つかの基本的な部分を示している各概略図。

【図8】（A）及び（B）は幾つかの実施例に基づくMS-APD構造の幾つかの基本的な部分を示している各概略図。

【図9】（A）及び（B）は幾つかの実施例に基づくI-I'-V又はGeのSAG前後の選択的領域成長（SAG）APD構造の側面を示している各概略図。

【図10】幾つかの実施例に基づくPINエピタキシャル層を具備する簡単化したマイクロストラクチャ型シリコンフォトダイオードを示している概略図。

【図11】幾つかの実施例に基づくPINエピタキシャル層を具備する簡単化したマイクロストラクチャ型シリコンフォトダイオードを示している概略図。

【図12】（A）乃至（C）は幾つかの実施例に基づくPINエピタキシャル層を具備する簡単化したマイクロストラクチャ型シリコンフォトダイオードを示している各概略図。

【図13】幾つかの実施例に基づくP-I-Nドーピングを具備する高コントラストマイクロストラクチャ型フォトダイオード（PD）に対するエピタキシャル層構造を示している概略図。

【図14】幾つかの実施例に基づくP-I-Nドーピングを具備する高コントラストマイクロストラクチャ型フォトダイオード（PD）に対するエピタキシャル層構造を示している概略図。

【図15】幾つかの実施例に基づくP-I-Nドーピングを具備する高コントラストマイクロストラクチャ型フォトダイオード（PD）に対するエピタキシャル層構造を示している概略図。

【図16】幾つかの実施例に基づく高コントラストマイクロストラクチャ型フォトダイオード（PD）の製造の幾つかの側面を示している概略図。

【図17】（A）乃至（D）は幾つかの実施例に基づく穴配列、間隔、寸法、及びバッフレーション層の例を示している各概略図。

【図18】幾つかの実施例に基づく高コントラストマイクロストラクチャ型フォトダイオード（PD）の製造の幾つかの更なる側面を示している概略図。

【図 1 9】幾つかの実施例に基づく高コントラストマイクロストラクチャ型フォトダイオード (P D) の製造の幾つかの更なる側面を示している概略図。

【図 2 0】幾つかの実施例に基づく高コントラストマイクロストラクチャ型フォトダイオード (P D) の製造の幾つかの更なる側面を示している概略図。

【図 2 1】幾つかのその他の実施例に基づく高コントラストマイクロストラクチャ型フォトダイオード (P D) の製造の幾つかの側面を示している概略図。

【図 2 2】(A) 及び (B) は幾つかの実施例に基づく特定のマイクロストラクチャ型 P D のシミュレーションの側面を示している各概略図。

【図 2 3】幾つかの実施例に基づく高コントラストマイクロストラクチャ型 P D の成る側面を示している概略図。

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【図 2 4】幾つかの実施例に基づくヘテロエピタキシャルマイクロストラクチャ型 P D の成る側面を示している概略図。

【図 2 5】幾つかの実施例に基づく発光ダイオード (L E D) 又は垂直表面発光レーザ (V C S E L) 等の光学的発光器用の高コントラスト構造を示している概略図。

【図 2 6】幾つかの実施例に基づく、例えば、高コントラスト 1.3 ミクロン波長フォトエミッタ (photo emitter) 用の基本構造を示している概略図。

【図 2 7】幾つかの実施例に基づいてエッチング形成した穴を具備する高コントラストマイクロストラクチャ型フォトエミッタ (P E) の幾つかの基本的な特徴を示している概略図。

【図 2 8】幾つかのその他の実施例に基づく P E の幾つかの側面を示している概略図。

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【図 2 9】幾つかのその他の実施例に基づく P E の幾つかの側面を示している概略図。

【図 3 0】幾つかのその他の実施例に基づく P E の幾つかの側面を示している概略図。

【図 3 1】幾つかの実施例に基づくシンプル P I N フォトダイオード構造の幾つかの側面を示している概略図。

【図 3 2】幾つかの実施例に基づく M S - P D 製造の成る側面を示している概略図。

【図 3 3】幾つかの実施例に基づく M S - P D 製造の成る側面を示している概略図。

【図 3 4】幾つかの実施例に基づく M S - P D 製造の成る側面を示している概略図。

【図 3 5】幾つかの実施例に基づく M S - P D 製造の成る側面を示している概略図。

【図 3 6】幾つかの実施例に基づく M S - P D 製造の成る側面を示している概略図。

【図 3 7】幾つかのその他の実施例に基づいて少数キャリアライフタイムを減少させるための一つの技術を示している概略図。

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【図 3 8】(A) 乃至 (C) はシミュレーションした幾つかのマイクロストラクチャ型フォトダイオードに対する種々のパラメータを示している各説明図。

【図 3 9】マイクロストラクチャ型フォトダイオードのシミュレーション結果をプロットしたグラフ。

【図 4 0】幾つかの実施例に基づく P - I - P - I - N エピタキシャル構造を具備するマイクロストラクチャ型アバランシェフォトダイオード (A P D) を示している概略図。

【図 4 1】幾つかのその他の実施例に基づく P - I - P - I - N エピタキシャル構造を具備するマイクロストラクチャ型アバランシェフォトダイオード (A P D) を示している概略図。

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【図 4 2】幾つかの実施例に基づく G e 吸収層及び G e P キャッピング層を具備しているマイクロストラクチャ型 A P D を示している概略図。

【図 4 3】(A) 乃至 (D) は幾つかの実施例に基づくマイクロストラクチャ型フォトダイオード及び A P D の分極 (偏光) 感度を示した各説明図。

【図 4 4】幾つかの実施例に基づいて相互インピーダンス増幅器及び/又はその他の A S I C (応用特定集積回路) と集積化されている M S - P D / A P D を示している概略図。

【図 4 5】幾つかの実施例に基づいて単一シリコンチップ上に T I A 及び/又はその他の信号処理 I C を集積化させた M S - P D / A P D 用のフリップチップ配置の幾つかの側面を示している概略図。

【図 4 6】幾つかのその他の実施例に基づいて単一シリコンチップ上に T I A 及び/又は

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その他の信号処理 IC を集積化させた MS-PD/APD 用のフリップチップ配置の幾つかの側面を示している概略図。

【図 4 7】幾つかのその他の実施例に基づいて単一シリコンチップ上に TIA 及び／又はその他の信号処理 IC を集積化させた MS-PD/APD 用のフリップチップ配置の幾つかの側面を示している概略図。

【図 4 8】幾つかのその他の実施例に基づいて単一シリコンチップ上に TIA 及び／又はその他の信号処理 IC を集積化させた MS-PD/APD 用のフリップチップ配置の幾つかの側面を示している概略図。

【図 4 9】幾つかのその他の実施例に基づいて単一シリコンチップ上に TIA 及び／又はその他の信号処理 IC を集積化させた MS-PD/APD 用のフリップチップ配置の幾つかの側面を示している概略図。

【図 5 0】幾つかのその他の実施例に基づいて単一シリコンチップ上に TIA 及び／又はその他の信号処理 IC を集積化させた MS-PD/APD 用のフリップチップ配置の幾つかの側面を示している概略図。

【図 5 1】幾つかのその他の実施例に基づいて単一シリコンチップ上に TIA 及び／又はその他の信号処理 IC を集積化させた MS-PD/APD 用のフリップチップ配置の幾つかの側面を示している概略図。

【図 5 2】幾つかの実施例に基づいて単一シリコンチップ上に TIA 及び／又はその他の信号処理及びルーチングエレクトロニクスなどの IC エレクトロニクスと集積化させた MS-PD/APD のアレイを示している概略図。

【図 5 3】幾つかの実施例に基づく高データレート MS-PD 用のエピタキシャル構造を示している概略図。

【図 5 4】幾つかの実施例に基づく高データレート MS-PD 用のエピタキシャル構造を示している概略図。

【図 5 5】幾つかの実施例に基づく高データレート MS-PD 用のエピタキシャル構造を示している概略図。

【図 5 6】幾つかの実施例に基づく MS-PD 用のメサ寸法、穴直径、穴周期距離、及び格子パターンを示している表。

【図 5 7】(A) 及び (B) は幾つかの実施例に基づく六角形及び正方形の格子穴パターンを示している各概略図。

【図 5 8】幾つかの実施例に基づくシリコン MS-PD 用のエピタキシャル層構造を示している概略図。

【図 5 9】幾つかの実施例に基づく MS-PD の或る側面を示している概略図。

【図 6 0】幾つかの実施例に基づく MS-PD の或る側面を示している概略図。

【図 6 1】幾つかの実施例に基づく MS-PD の或る側面を示している概略図。

【図 6 2】幾つかの実施例に基づく MS-PD 用の Ge・オン・Si の PIN エピタキシャル層構造を示している概略図。

【図 6 3】幾つかの実施例に基づく Ge・オン・Si の MS-PD の或る側面を示している概略図。

【図 6 4】幾つかの実施例に基づく Ge・オン・Si の MS-PD の或る側面を示している概略図。

【図 6 5】幾つかの実施例に基づく Ge・オン・Si の MS-PD の或る側面を示している概略図。

【図 6 6】幾つかの実施例に基づく Ge・オン・Si の PD の或る側面を示している概略図。

【図 6 7】幾つかの実施例に基づく Ge・オン・Si の PD の或る側面を示している概略図。

【図 6 8】幾つかの実施例に基づく MS-APD の或る側面を示している概略図。

【図 6 9】幾つかの実施例に基づく MS-APD の或る側面を示している概略図。

【図 7 0】幾つかの実施例に基づく SiO₂ 層無し MS-APD を示している概略図。

【図 7 1】幾つかの実施例に基づく Ge・オン・Si マイクロストラクチャ型アバランシェフォトダイオード (MS-APD) を示している概略図。

【図 7 2】幾つかの実施例に基づく Ge・オン・Si マイクロストラクチャ型アバランシェフォトダイオード (MS-APD) を示している概略図。

【図 7 3】幾つかの実施例に基づくエッチストップ層を具備している Ge・オン・Si マイクロストラクチャ型アバランシェフォトダイオード (MS-APD) を示している概略図。

【図 7 4】幾つかの実施例に基づく Ge・オン・Si マイクロストラクチャ型アバランシェフォトダイオード (MS-APD) を示している概略図。

【図 7 5】幾つかの実施例に基づく MS-PD 用の別の SiNIP エピタキシャル層構造を示している概略図。

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【図 7 6】(A) 乃至 (C) は幾つかの実施例に基づく MS-PD 用の埋込酸化物上の SiNIP エピタキシャル層を示している各概略図。

【図 7 7】幾つかの実施例に基づく P Si 基板上の SiNIP エピタキシャル層及び SiGeB エッチストップ層を具備している MS-PD を示している概略図。

【図 7 8】幾つかの実施例に基づく MS-PD 用の SiGeB エピタキシャル層構造上の Ge・オン・Si の NIP を示している概略図。

【図 7 9】幾つかの実施例に基づく MS-PD 用の Ge・オン・Si エピタキシャル構造を示している概略図。

【図 8 0】幾つかの実施例に基づく別の Ge・オン・Si エピタキシャル構造を示している概略図。

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【図 8 1】幾つかの実施例に基づく Ge・オン・Si エピタキシャル構造を示している概略図。

【図 8 2 A】図 7 9 に図示した構造と類似した Ge・オン・Si マイクロストラクチャ型フォトダイオードに関する有限差分時間領域 (FDTD) を使用したシミュレーションに関する説明図。

【図 8 2 B】図 7 9 に図示した構造と類似した Ge・オン・Si マイクロストラクチャ型フォトダイオードに関する有限差分時間領域 (FDTD) を使用したシミュレーションに関する説明図。

【図 8 2 C】図 7 9 に図示した構造と類似した Ge・オン・Si マイクロストラクチャ型フォトダイオードに関する有限差分時間領域 (FDTD) を使用したシミュレーションに関する説明図。

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【図 8 3 A】図 8 0 における構造と類似した Ge・オン・Si マイクロストラクチャ型フォトダイオードに関する有限差分時間領域 (FDTD) を使用したシミュレーションに関する説明図。

【図 8 3 B】図 8 0 における構造と類似した Ge・オン・Si マイクロストラクチャ型フォトダイオードに関する有限差分時間領域 (FDTD) を使用したシミュレーションに関する説明図。

【図 8 3 C】図 8 0 における構造と類似した Ge・オン・Si マイクロストラクチャ型フォトダイオードに関する有限差分時間領域 (FDTD) を使用したシミュレーションに関する説明図。

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【図 8 4 A】図 7 9 における構造と類似した Ge・オン・Si マイクロストラクチャ型フォトダイオードに関する有限差分時間領域 (FDTD) を使用したシミュレーションの結果を示しているグラフ。

【図 8 4 B】図 7 9 における構造と類似した Ge・オン・Si マイクロストラクチャ型フォトダイオードに関する有限差分時間領域 (FDTD) を使用したシミュレーションの結果を示しているグラフ。

【図 8 5】幾つかの実施例に基づくマイクロストラクチャ型フォトダイオードチップの概略平面図。

【図 8 6】幾つかの実施例に基づいて単一チップ上に相互インピーダンス増幅器及び／又

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はその他のエレクトロニクスを集積化したMS-PD/APDを示している概略平面図。

【図87】マイクロストラクチャが無い状態の単純なエピタキシャル構造を示している概略図。

【図88】マイクロストラクチャが無い状態の別の単純なエピタキシャル構造を示している概略図。

【図89】幾つかの実施例に基づいてSiPエピタキシャル層へマイクロストラクチャ型穴アレイをエッチングした場合の図87におけるものと同じエピタキシャル構造を示している概略図。

【図90】幾つかの実施例に基づいてBOXSiO₂層へマイクロストラクチャ型穴アレイをエッチングした場合の図88におけるものと同じエピタキシャル構造を示している概略図。

【図91A】図87-90に図示した例示的構造に対するシミュレーション結果を示したプロット。

【図91B】図87-90に図示した例示的構造に対するシミュレーション結果を示したプロット。

【図92】幾つかの実施例に基づいてシリコン内へ穴をエッチングした場合のシリコン内のマイクロストラクチャ型領域を示している概略図。

【図93】幾つかの実施例に基づいてテーパ付き穴を具備するMS-PD構造を示している概略図。

【図94】幾つかの実施例に基づいて徐々にテーパが付けられた穴を具備するMS-PD構造を示している概略図。

【図95】幾つかの実施例に基づいて異なる直径のマイクロストラクチャ型穴を具備する物質構造を示している概略図。

【図96】図95に図示した如く異なる直径のマイクロストラクチャ型穴を具備する物質構造の平面図。

【図97A】図82Aに示した如き層構造を具備するマイクロストラクチャ上に入射する光に対する吸収を示しているグラフ。

【図97B】図82Aに示した如き層構造を具備するマイクロストラクチャ上に入射する光に対する吸収を示しているグラフ。

【図98】図82Aに示してあり且つ図97A及び97Bにおいてシミュレーションした構造に対するシミュレーションした吸収を示しているグラフ。

【図99】幾つかの実施例に基づいて800乃至1000nmの波長範囲における動作に対するSiアバランシェフォトダイオード用の別の好適なエピタキシャル構造を示している概略図。

【図100】幾つかの実施例に基づくマイクロストラクチャ型APDの幾つかの特徴を示している概略図。

【図101】

【図102】マイクロストラクチャ型Ge・オン・SiAPDの幾つかの特徴を示している概略図。

【図103】(A)乃至(C)は、幾つかの実施例に基づいて、マイクロストラクチャ型シリコン及びGe・オン・Siフォトダイオード及びアバランシェフォトダイオードに対する直径、周期、及びその他のパラメータを示している各説明図。

【図104】(A)及び(B)はマイクロストラクチャ型GeP-GeI-SiN・オン・SiN基板フォトダイオードである図82Aに示した構造に対する吸収-波長に対してFDTD(有限差分時間領域)を使用したシミュレーション結果を示している各グラフ。

【図105】(A)及び(B)は幾つかの実施例に基づく正方形格子穴パターンに対する固有モードを説明するための各説明図。

【図106】幾つかの実施例に基づいて互いにオーバーラップして配設された2個の正方形格子を具備しているマイクロストラクチャ型穴を示している概略図。

【図107】幾つかの実施例に基づくGe・オン・Siのエピタキシャル構造を示してい

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る概略図。

【図108】幾つかの実施例に基づくGe・オン・Siのマイクロストラクチャ型フォトダイオードの基本的な特徴を示している概略図。

【図109】(A)及び(B)は幾つかの実施例に基づいてマイクロストラクチャ型穴アレイに対してマクスウェル方程式を使用したFDTDシミュレーションの結果を示している各グラフ。

【図110】幾つかの実施例に基づいて異なる穴直径及び格子周期を有するマイクロストラクチャ型フォトダイオード／アパランシェフォトダイオードに対する吸収ー波長のプロット。

【図111A】幾つかの実施例に基づいて2つの格子及び2つの異なる穴直径が使用されている場合の図82Aにおけるような構造のFDTD方法を使用したシミュレーションを示している概略図。

【図111B】幾つかの実施例に基づいて2つの格子及び2つの異なる穴直径が使用されている場合の図82Aにおけるような構造のFDTD方法を使用したシミュレーションを示している概略図。

【図112】幾つかの実施例に基づいて同じ周期の2つの六角形状格子が結合され且つ互いにインターレースされている場合の別の格子構造を示している概略図。

【図113】各セルが固有モードを有しており何らかのフィールド伝播／分布がその固有モードの拡張である場合がある6単位セルを具備している六角形状格子を示している概略図。

【図114】幾つかの実施例に基づく穴アレイ及びテクスチャー表面を具備しているSiNIPマイクロストラクチャ型フォトダイオードを示している概略図。

【図115】波長に対してのSi及びGeの吸収係数を示しているグラフ。

【図116】幾つかの実施例に基づいてマイクロストラクチャ型穴アレイに起因するGeの向上された実効吸収係数を示しているグラフ。

【図117】幾つかの実施例に基づいてSiマイクロストラクチャ型PD/APDの向上された吸収を示しているグラフ。

【発明を実施するための形態】

【0025】

好適実施例の幾つかの例の詳細な説明を以下に与える。幾つかの実施例について説明するが、本特許明細書において記載する新たな要旨はここに記載されるいずれか一つの実施例又は幾つかの実施例の組合せに制限されるものではなく、多数の代替物、修正物、及び均等物を包含することを理解すべきである。更に、完全なる理解を与えるために以下の説明においては多数の特定の詳細を記述するが、幾つかの実施例はこれらの詳細の幾つか又は全てが無い状態で実施することが可能である。更に、説明の便宜上、本書に記載する新たな要旨が不必要にぼかされることを回避するために、関連技術において既知である或る技術的物質については詳細に記載していない。本書に記載する特定の実施例の内の一つ又は幾つかの個々の特徴を他の記載する実施例の特徴と結合して使用することが可能であることは明らかである。更に、種々の図面における同様の参照番号及び記号は同様の要素を表している。

【0026】

幾つかの実施例によれば、半導体物質のバンドギャップの近傍における波長において物質のバルク吸収定数又は吸収を改善するためにマイクロストラクチャが使用される。このことは、光センサーの動作光学的波長及び／又は動作スペクトルを拡張することを可能とする。向上されたバルク吸収定数（即ち、係数）は実効吸収定数（即ち、係数）と呼称される。「実効」という用語が使用される理由は、吸収定数即ち係数は固有の物質特性だからである。しかしながら、共振効果、結合型共振効果、遅波効果、プラズモン効果、フィールドエンハンスメント効果、散乱効果、近場及びサブ波長効果、線形及び非線形効果がある場合、実効吸収定数即ち係数はバルク即ち物質吸収定数即ち係数よりも一層大きい場合がある。吸収は吸収係数と吸収長との積に指数的に依存するので、バルク吸収係数を維

持することによって、実効吸収長は、量子効率に比例する同一の吸収を達成するために $P D / A P D$ の「1」吸収領域の物理的な長さよりも一層大きなものである場合がある。本書において使用されているように、以下の用語は交換可能に使用されており、即ち、向上された吸収定数、向上された吸収係数、向上された実効吸収定数、向上された実効吸収係数、及び実効吸収定数、及び実効吸収係数、向上された吸収長、実効吸収長、向上された実効吸収長である。向上された吸収即ち実効吸収は、向上された吸収係数及び／又は向上された吸収長のいずれが又は両方に起因する場合がある。

【0027】

幾つかの実施例によれば、向上された吸収は経路長に関して劇的な効果を有する場合がある。一つのバルク吸収例において、その元の振幅の $1/e$ に対して吸収すべきフォトンに対する経路長は $100 \mu m$ であり、一方、この特許明細書において記載される幾つかの実施例に基づく向上された吸収の下では、その経路長はその元の振幅の $1/e$ へ減衰するための光学振幅に対して $1 \mu m$ である。等価的に、経路長を $1 \mu m$ に一定に維持する場合には、向上された吸収係数はバルク吸収係数よりも 100 倍大きく及び／又は向上された実効吸収長は実際の物理的長さよりも 100 倍大きい。

【0028】

このことは $A = A_0 e^{-\alpha L}$ の関係から理解されるが、尚 A は入射フォトンフラックス A_0 の減衰振幅であり、 α は吸収係数であり、 L は吸収が行われる経路長である。従って、 L を 100 倍一層長いものとする代わりに、実効 α がバルク吸収係数等の向上されていない吸収係数よりも 100 倍一層大きなものであるように実効 α を定義することが可能である。例えば、マイクロストラクチャの共振／結合共振／散乱／近場効果が 100 倍一層長い経路長の均等性を与え、その場合に該共振／散乱／近場マイクロストラクチャは 1 ミクロンの長さであるに過ぎない。このことの一層簡単な記述は、共振／結合共振構造内のフォトンはその元の振幅の $1/e$ の値に到達する前に 50 回の往復を行い、従ってその均等線形長さは結合共振構造の長さの 100 倍であるということである。説明の便宜上、共振／結合共振／線形及び非線形フィールドエンハンスメント／散乱／近場効果をここでは集約的に「共振 (resonant)」として言及することとし、そのことは、共振、結合共振、遅波、散乱、近場、プラズモン、非線形及び線形光学場効果を包含することが可能である。

【0029】

本書において使用されているように、「マイクロストラクチャ」及び「マイクロストラクチャ型」という用語は、少なくとも一つの寸法がミクロン尺度、サブミクロン尺度、及び／又はサブ波長尺度及び／又は波長尺度である寸法及び種々の形状の柱体、ポイド、穴及びメサのことを意味している。

【0030】

幾つかの実施例によれば、実効吸収を向上させるための本技術は、シリコン、ゲルマニウム、 InP と $GaAs$ と GaN と GaN と $InGaAs$ 等の $III-V$ 物質、及び $III-V$ 物質群の任意の組合せを包含する種々の物質へ適用することが可能である。本明細書において使用されるように、 $III-V$ 物質の「物質群」という用語は、 $GaAs$ 、 InP 、 GaN 、 $InSb$ 半導体に対して格子整合しているか又はほぼ格子整合 (数%以内) している任意の物質として定義される。例えば、 InP 物質群は $InGaAs$ 、 $InGaAsP$ 、 $InAlAs$ 、 $InAs$ を包含することが可能である。幾つかの実施例によれば、マイクロストラクチャの場合、選択区域成長 (SAG)、エピタキシャル横方向過剰成長 (ELOG)、 Ge が $InGaAs$ か又はシリコンマイクロストラクチャにおけるその他の $III-V$ 物質の薄いバッファ層が有るか又は無いエピタキシャル成長 (EG) 等の再成長を格子不整合の有害な影響無しに実施することが可能である。何故ならば、シリコン上の格子不整合物質のフットプリントの寸法が小さいからである (約数ミクロン乃至サブミクロン)。このことは、従来のバッファ層 ($Ge \cdot$ オン Si 成長の場合における非晶質 Ge 等) を使用すること無しに Ge 及びその他の $III-V$ 物質をシリコンと集積化させることを可能とさせる。複数物質の不均一集積化は、ホモ又はヘテロ構造、結晶性

及び微結晶性及び非晶質半導体の組合せ、炭素等の導体、グラフェン、絶縁体、誘電体、固体、気体、ガラス等の液体、又は半導電性とする事が可能なポリマーとすることが可能である。Ge及びIII-V物質は、ミクロン尺度より大きな面積からウエハ尺度をカバーする面積を被覆することが可能なSOG、ELOG、EC方法を使用するパッファ層と共に又は無しでSi上に成長させることも可能である。

【0031】

幾つかの実施例によれば、実効屈折率を低下させるために、埋込酸化物(BOX)、シリコン・オン・インシュレータ(SOI)、シリコン・オン・サファイア(SOS)、非晶質半導体等の低密度半導体、ナノワイヤ半導体、ポイド及び穴等の低指数物質が使用される。屈折率は物質の固有の特性である。しかしながら、幾つかの実施例によれば、ポイド、空隙、及び／又は穴(低屈折率物質で充填又は部分的に充填させることが可能)等の構造が光学波長程度の寸法を有している場合には、光学的電磁界が物質屈折率と該構造(低屈折率物質で充填又は部分的に充填させることが可能)とからなる平均屈折率を見ることがとなる。この平均は、ここでは、実効屈折率と呼称する。幾つかの実施例によれば、低指数又は低実効指数物質をマイクロストラクチャにおいて使用することは必要ではない。

【0032】

幾つかの実施例によれば、実効吸収を向上させる技術をシリコン、ゲルマニウム、InPやGaAsやGaNやInGaAs等のIII-V物質、及びIII-V物質群の任意の組合せを含む種々の物質へ適用することが可能である。

【0033】

マイクロストラクチャに起因して、容量も実効容量によって表すことが可能であり、それは、(1)一つの半導体の誘電率と、(2)半導体、誘電体、気体、真空、部分的真空、ガラス又はポリマー(ポリイミド、マイラー、又はその他の有機化合物)等の液体、とすることが可能な別の物質の誘電率との並列容量である。本装置の実効容量は、2つ又はそれ以上とすることが可能な並列コンデンサの容量の結合である。幾つかの実施例によれば、マイクロストラクチャを使用する利点は、その実効容量を半導体等の均一物質の容量よりも著しく低下させることが可能であるということである。RC時間(抵抗容量)はフォトダイオード及びアバランシェフォトダイオードの帯域幅を決定する基本的な時間の内の一つである。より低い容量は、装置をして、適切に高いデータレート帯域幅を維持しながら一層大きな面積を有することを可能とし、及び／又はPD/APDの帯域幅を決定する基本的な時間である電子及び／又は正孔の走行時間(transit time)を減少させるために該装置の厚さを減少させることによってデータレート帯域幅を増加させることを可能とする。

【0034】

幾つかの実施例によれば、本光センサーはフォトダイオード(PD)、アバランシェフォトダイオード(APD)、光電池(PV)又は太陽電池、又はフォトン電子へ変換させる任意のオプトエレクトロニクス装置とすることが可能である。幾つかの実施例によれば、レーザー及び発光ダイオード等の電子／正孔をフォトンへ変換させるエミッター即ち発光体もマイクロストラクチャを使用して実現することが可能である。

【0035】

幾つかの実施例によれば、向上させた吸収はAPD/PDを、(1)バルク吸収係数が弱い、例えば、QE(量子効率)が30%より大きい又は50%より大きく且つデータ帯域幅が3Gb/sよりも大きい状態で約1000 1/cm又はそれ以下である場合にAPD/PDの感度を物質バンドギャップに近いエネルギー(又は波長)を有するフォトンへ拡張させ、(2)一層短い吸収長従って一層短い走行時間に起因して高データレート帯域幅(例えば、10Gb/sを越える)で動作させ、(3)向上させた吸収で量子効率を増加させ、(4)アバランシェフォトダイオードに対して低過剰ノイズで優れた増倍特性を有するシリコンで製造させ、(5)Siフォトンクス及びCMOSプロセスと適合性があるものとさせることを可能とする。幾つかの実施例によれば、PD/APDは、信号処理、信号増幅、メモリ、CPU、電気的送信機、光学的導波路、集積化オプティックス、

及び特定適用例のためのその他のIC等のASIC（応用特定集積回路）と集積化させることが可能である。このことはCMOSファブリーを使用する大量生産に有益である。更に、エレクトロニクスと共に又は無しで集積化されている表面（又は底部）照射型PD/APDはウエハレベルプロービングでテストすることが可能であり、更に、単一モード及びマルチモードの両方を取り扱うことが可能である。単一の光学的及び電気的チップはセラミックマルチチップキャリアの必要性をバイパスし且つ組立及びパッケージングのコストを著しく減少させる。シリコンベンチは必要とされる場合のレンズ、ファイバー等の光学的部品に対する光学的アライメントに関連して使用することも可能である。

【0036】

幾つかの実施例によれば、シリコンはアバランシェ利得のために使用される。シリコンはアバランシェフォトダイオードに対して過剰ノイズが一層低い。Geをシリコンと統合させることによって、吸収はGe物質内において行われ且つ電子的利得はシリコン内において発生する。光学的波長、例えば1100nm未満、に依存して、シリコンは、マイクロストラクチャの使用と共に、吸収及び電子的利得の両方のために使用することが可能である。

【0037】

幾つかの実施例によれば、半導体におけるフォトンの吸収はマイクロストラクチャを使用して向上される。該マイクロストラクチャは、共振、結合共振、フィールドエンハンスメント、近場及びサブ波長効果、散乱、プラズモン、線形及び非線形光学的場、フォトニック結晶、与えられた物理的長さに対するフォトンの一層大きな吸収となる実効吸収長を効果的に増加させることが可能であり及び／又は該吸収係数を実効係数へ向上させることが可能な線形及び非線形の両方の効果である近場領域においての高コントラストグレーティングにおける吸収モード又は損失モード等の効果を有することが可能である。

【0038】

幾つかの実施例によれば、シリコンフォトダイオード及び／又はアバランシェフォトダイオードのための吸収向上のために使用されるマイクロストラクチャは、長さ及び／又は係数の向上に起因して、量子効率が約50%以上で、幾つかの場合にはQEが70%以上で波長が約850nm（それは現在のデータ通信の好適な波長である）で帯域幅が10Gb/s（又は、等価的に、デジタルコーディングフォーマットに依存して、約6,75GHz）を越えているシリコンPD及びAPDとなる場合がある。

【0039】

シリコン光学的検知器は、物質及び処理技術の成熟性に起因して、非常にロバスト即ち堅牢であり、その表面は表面状態及びキャリア再結合中心を発生させる場合があるダングリングボンドを取り除くために容易にパッシベーションすることが可能であり、且つ、APD適用例の場合、正孔と電子との間のイオン化比（k係数、シリコンほどのIII-V物質よりも低いk係数を有している）が小さいのでノイズが低く、且つこの様な検知器は信号処理用エレクトロニクス及びSIフォトリクスとの集積化に対してCMOS適合性を有している。

【0040】

幾つかの実施例によれば、光発生されたキャリアーは、高変調帯域幅（10Gb/s帯域幅以上）及び高量子効率のため及び利得が3dBより大きな高電流利得用のAPDのためのP-I-Nダイオード（PD）又はP-I-P-I-Nダイオード（APD）の吸収用「I」（時々「I」と言及される）領域における外部逆バイアスでスイープアウト即ち一掃される。

【0041】

10Gb/sよりも大きな帯域幅を有するマイクロストラクチャ型フォトダイオード及びアバランシェフォトダイオードは通信において使用される。光学信号は、バイナリー（強度）、位相／周波数偏移（コヒーレント、ヘテロダイン通信）、分極（偏光）コーディング（polarization coding）、波長分割多重化等の多波長、及び分極多重化等の技術を使用して光に刻印された情報を有している。該光学信号は、空中及び／又はファイバーを介

して走行してマイクロストラクチャフォトダイオード及び／又はアバランシェフォトダイオード上に突き当たり、そこで該光学信号上に刻印されている情報を電気信号として抽出することが可能である。幾つかの場合においては、ヘテロダイン又はホモダインにおけるように、別の一つ又は複数の光学的供給源を混合させることが必要である。

【0042】

図1は、幾つかの実施例に基づいて、本マイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードを使用することが可能な光学データ伝送システムを例示している概略図である。光学データ伝送システム100は、光学的供給源（ソース）110、空気及び／又はオプティカルファイバー等の伝送媒体120、及びマイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードMS-PD/APDから構成されている。幾つかの実施例によれば、光学的供給源110はレーザーとすることが可能である。電気データ112が、直接の変調のためにレーザー110を順方向バイアスしている電源114で光学信号上に刻印される。レーザー110の出力は、ボールレンズ等の結合器122を介してオプティカルファイバー120へ結合させることが可能である。該光学信号はファイバー120（又は空気）を介して伝播し且つファイバー120から例えばレンズ124を介して高速マイクロストラクチャフォトダイオード／アバランシェフォトダイオード130へ結合させることが可能であり、そこで、該光学信号は電気信号へ変換され且つその結果得られるデータ132（データ112と一致する）が回復される。該マイクロストラクチャフォトダイオード／アバランシェフォトダイオードは電源134を使用して逆バイアスされる。

【0043】

幾つかの実施例によれば、波長選択要素を該マイクロストラクチャ型フォトダイオード及びマイクロストラクチャ型アバランシェフォトダイオードと集積化させることが可能である。特に、マイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードのアレイを、例えばCMOS、b1-CMOS、パイボラ装置及び回路を具備している応用特定集積回路を包含することが可能な単一のチップ上に製造させることが可能である。バンドパスフィルタ等の波長選択要素は、粗波長分割多重化（CWDM）のために使用することが可能であり、その場合に、例えば、各々が10-40Gb/sの変調データを担持している810、820、830、840、850、860、870、880nmの波長は、単一伝送媒体内において80-320Gb/sの総合データレートを有することが可能である。

【0044】

波長選択要素の例は、高コントラストサブ波長グレーチング、金属膜又は誘電体膜におけるサブ波長穴からなるアレイ、及びブラック反射器におけるような交番する屈折率を有している誘電体層、を包含している。該波長選択要素は、空洞共振器を形成するための多数の高コントラストグレーチングを包含しているバンドパスフィルタとすることが可能である。該要素は、グレーチングと、金属膜又は半金属膜上のサブ波長穴アレイ及び／又はブラックミラー等のその他の波長選択要素との結合とすることも可能である。

【0045】

更に、フォトダイオード／アバランシェフォトダイオードのマイクロストラクチャはそれ自身、波長選択性及び吸収長向上の両方とすることが可能であるように高コントラストグレーチング等の反射器を形成することが可能である。特に、該フォトダイオード／アバランシェフォトダイオードのフォトン吸収領域を向上させることが可能である。幾つかの実施例によれば、波長選択性のために共振光学空洞を形成するために、マイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードの上に付加的な高コントラストグレーチングを製造することが可能である。該高コントラストグレーチングの内の一つが該2つの波長選択要素の間で電圧を発生させるように電気的にバイアスさせることが可能である場合には、同調可能なオプティカルファイバーの如く選択された波長を同調させることが可能である。

【0046】

図2は、幾つかの実施例に基づいて、マイクロストラクチャ型フォトダイオード(MS-PD)及びマイクロストラクチャ型アバランシェフォトダイオード(MS-APD)と共に包含されている波長選択要素を示している概略図である。波長選択要素220を使用して、選択波長範囲内の波長のみがMS-PD/APD130上に入射する。幾つかの実施例によれば、その窓は幅を1-20nmとすることが可能である(例えば、820nmの中心波長±5nmで、その場合バンドパスは820nmを中心にした10nmである)。図2に示した場合、シリコンMS-PD/APD130と集積化させることが可能なシリコンから構成されている高コントラストグレーチング220である。幾つかの実施例によれば、マイクロストラクチャ型フォトダイオード/アバランシェフォトダイオード130のマイクロストラクチャ特徴部210は、該フォトダイオード/アバランシェフォトダイオードの吸収特性を向上させる機能に加えて、それ自身が波長選択器として動作することも可能である。MS-PD/APD130のマイクロストラクチャ210が波長選択器として構成される場合には、高コントラストグレーチング220の付加はバンドパスフィルタとして機能することが可能な共振空洞を形成する。

【0047】

図3は、幾つかの実施例に基づいて、複数の波長選択要素を具備しているMS-PD/APDを示している概略図である。この場合には、複数の波長選択要素320及び322が製造され且つMS-PD/APD130内に集積化されている。波長選択要素320及び322は、バンドパスフィルタとして機能するデュアル高コントラストグレーチングである。幾つかの実施例によれば、他のものと相対的に一つの波長選択要素へ或る電圧を印加すると、同調可能なバンドパスフィルタを製造することが可能である。

【0048】

図4(A)乃至(D)は、幾つかの実施例に基づいて、種々のバンドパスフィルタ特性を示しているグラフである。図4(A)、(B)、(C)、(D)におけるプロットは、夫々、中心波長が820、830、840、850nmであり、尚「R」は反射率である。例えば、10nmの帯域幅の場合の中心波長において、反射率は実際上ゼロであって殆どの光が透過され、一方、その帯域幅の外側においては、反射率は殆ど100%であり透過は実際上ゼロである。

【0049】

図5は、幾つかの実施例に基づく、粗波長分割多重化(CWDM)形態を示している概略図である。この場合に、中心波長が820、830、840、850nmで各々が100Gb/s総合データレートに対して25Gb/sの変調データレートを有しているような伝送媒体内を4つの波長が伝播する。各波長選択MS-PD/APDで反射することによりMS-PD/APD530、532、534、546上のバンドパスフィルタによって光学バンドが分離される。各反射の後、その光は反射器550を介して次の波長選択MS-PD/APDへ反射され、全ての光学バンドが指定されたMS-PD/APDによって吸収されるまで、以下同様に行われる。各中心波長は一つのデータチャンネルを担持しており、例えば、820nmは25Gb/sのデータレートにおいてチャンネル1を担持しており、且つ820nmにおけるバンドパスフィルタを有するMS-PD530は820nm信号を光学信号の残部から分離し且つ集積化したCMOSASIC(不図示)によって更なる信号処理を行うために回復されたデータチャンネル1を発生させる。

【0050】

幾つかの実施例によれば、MS-PD/APDエピタキシャル層厚さは、エピタキシャル層厚さ及びCMOS(相補的半導体)プロセスの構造と適合性があり、従ってCMOSASICと集積化させることが可能である。対照的に、1、25Gb/sのデータレートを有する850nmにおける従来のシリコンフォトダイオードは10μm厚さよりも大きなエピタキシャル層及び53%量子効率を有している。従って従来のシリコンフォトダイオードの比較的厚い層はCMOSプロセスと容易に適合可能なものではない。

【0051】

幾つかの実施例によれば、該光吸収層は非結晶性のものとするのが可能である。特に、それは、例えば、プラズマエンハンスド化学蒸着（PECVD）及び／又はホットワイヤ化学蒸着（HWCVD）によって付着される水素化非晶質Si（a-Si:H）とすることが可能である。その層は、典型的に、0.3〜3 μm厚さの程度である。該光吸収領域（即ち、pinフォトダイオード構造のi領域）を横断して逆バイアスで電圧を印加して光発生されたキャリアを一掃して高速データ通信適用例のための高効率及び高帯域幅を可能とさせる。該非結晶性層上の層は透明又は半透明の導電性金属又はインジウムスズ酸化物等の導電性酸化物とすることが可能である。該上部層はpin構造を形成するためにドーブした非結晶性物質の薄い層とすることが可能である。

【0052】

図6（A）及び（B）は、幾つかの実施例に基づく、マイクロストラクチャ型フォトダイオードの幾つかの基本的な部品を示している概略図である。図6（A）はマイクロストラクチャをエッチングする前の物質構造600を示しており、且つ図6（B）はエッチング後のMS-PD660を示している。注意すべきであるが、幾つかの実施例によれば、該マイクロストラクチャは穴622であり、且つ幾つかのその他の実施例においては、該マイクロストラクチャは柱体である。幾つかのその他の実施例において、該マイクロストラクチャは穴と柱体との結合である。「Ia」層608は、結晶性又は非結晶性N層上に成長させた非結晶性（例えば、水素化非晶質Si（a-Si:H））とすることが可能である。P層610は非結晶性及び高度にドーブしたP又は導電性酸化物又は金属とすることも可能である。N層606も金属又は導電性酸化物とすることが可能である。オーミックコンタクト628及び630を使用してP層とN層との間にバイアスを印加させて、水素化キャリアを一掃する高電界をI層608内に形成させる。基板602は、例えば、非結晶性及び／又は石英等の誘電体、ガラス、セラミック、及び／又は金属等の導体、シリサイド、導電性ポリマーとすることが可能である。幾つかの実施例によれば、「I」層608としても知られる「Ia」は0.3乃至3 μmの厚さ範囲を有することが可能である。

【0053】

図7（A）及び（B）は、幾つかの実施例に基づく底部照射型フォトダイオードの幾つかの基本的な部品を示している概略図である。図7（A）はマイクロストラクチャをエッチングする前の物質構造700を示しており、且つ図7（B）はマイクロストラクチャ（穴722等）をエッチングした後の底部照射型MS-PD760を示している。底部照射型PD/APDの場合、「Ia」即ち「I」領域708はa-Si:H等の非結晶性とすることが可能であり且つ「N」層710も非結晶性とすることが可能であり、一方、「P」層706はBOX/SOI704上で結晶性か又は非結晶性とすることが可能であり且つ結晶性又は非結晶性基板702とすることが可能である。しかしながら、光学損失を最小とさせるために、基板702及びP層706が結晶性であることが望ましい。何故ならば、それは800乃至1100 nmの波長において非晶質シリコンよりも吸収性が少ないからである。「ダブル又はマルチバウンス（bounce）」のPD/APDの場合、吸収領域「Ia」層708は0.2乃至2 μmの厚さ範囲を有することが可能である。何故ならば、光学信号はN金属コンタクト726で反射し且つ「Ia」吸収層708へ戻るからである。「Ia」層708の厚さは減少させることが可能であり、従って、走行時間を減少させ且つフォトダイオード又はアバランシェフォトダイオードの帯域幅を増加させることが可能である。

【0054】

図8（A）及び（B）は、幾つかの実施例に基づく、MS-APD構造の幾つかの基本的な部品を示している概略図である。図8（A）はマイクロストラクチャをエッチングする前の物質構造800を示しており、且つ図8（B）はエッチング後のMS-APD860を示している。光吸収用の「Ia」領域808は結晶性又はa-Si:Hなどの非結晶性とすることが可能である。PINシリコン（820、818、及び806）の結晶性アバランシェ利得領域をシリコン基板又はBOX/SOI（埋込酸化物／シリコン・オン・

インシュレータ) 基板 802 上に成長させる。Pa 上部層 810 は結晶性又は非結晶性とすることが可能である。PSI 層 810 とオーミックコンタクトを形成するため及び／又はシート抵抗を減少させるために、透明な金属酸化物層 826 を設けることが可能である。注意すべきことであるが、光学信号は上部表面へ真っ直ぐ(垂直)に来るか、又はそれはフォトン矢印で示したように角度をもって来る場合がある。マイクロストラクチャ 822 は穴、柱体、又はこれらの組合せとすることが可能である。図 8 (B) に示したものは上部照射型 APD 860 であるが、幾つかの実施例によれば、BOX/SOI を使用して、基板のバルクを除去することが可能であり、且つ該 APD は 800-1100 nm の波長範囲で底部から照射させることが可能である。P 層 810 を介しての P オーミック及びボン

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ンド金属 828 と N 基板 806 を介しての N オーミック及びボン

ンド金属 830 との間に逆バイアスを印加させる。その逆バイアスは水素化キャリアを一掃すると共に電子的利得を与える。PD 用の典型的なバイアス電圧は 1 乃至 10 ボルトの逆バイアスであり、且つ APD の場合には、その範囲はほぼ 5 乃至 50 ボルトの逆バイアスである。ここに記載する全ての PIN、PIPIN 装置における如く、P と N とは交換可能であり、例えば、フォトダイオード及びアバランシェフォトダイオードに対して、PIN は NIP とすることが可能であり且つ PIPIN は NIPIN とすることが可能である。アノード即ち P 層はカソード N 層に関して負にバイアスされる。

【0055】

図 9 (A) 及び (B) は、幾つかの実施例に基づいて、III-V 又は Ge 物質の SAG 前後の選択区域成長 (SAG) APD 構造の或る側面を示している各概略図である。図 9 (A) はエッチングした穴 922 (又は柱体周りの区域) を有する Si APD 構造を示している。III-V 物質又は Ge の選択区域成長 (SAG) エピタキシャル成長を実施することが可能であり、図 9 (B) に示した如く、その場合には、Pa 層 910 及び Ia 層 908 は a-Si:H 等の非結晶性とすることが可能であり、又はそれは結晶性シリコンとすることが可能である。特に、マイクロストラクチャの I 区域 934 は InGaAs 又は Ge とすることが可能であり、且つ P 区域 932 は InGaAs とすることが可能である。幾つかの実施例によれば、アバランシェ利得層 (P 層 920 及び I 層 918) を除去した PD 構造で開始して、InGaAs 又は Ge を具備する SAG PD を製造することが可能である。GaN, ZnSe, InP, GaAs 等のその他の物質も SAG において使用することが可能である。幾つかの実施例によれば、非品質 Ge 等のその他の非品質半導体を使用することも可能である。幾つかの実施例によれば、間接遷移を超えるエネルギーを有するフォトンの結晶シリコンよりも一層高い吸収係数に起因して非品質シリコンを使用することが可能である。

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【0056】

図 10 は、幾つかの実施例に基づく PIN エピタキシャル層を具備する簡単化したマイクロストラクチャ型シリコンフォトダイオードを示している概略図である。0.2 乃至 10 μm の厚さとすることが可能な埋込酸化物層 (BOX) 1004 へ穴 1022 がエッチングされている。この構造 1060 は、シリコンと二酸化シリコンとの間の屈折率において高コントラストを提供しており、そのことは吸収を向上させることが可能である。I 層 1008 は 0.5 乃至 5 μm の範囲内の厚さとすることが可能であり、且つ P 層 1010 及び N 層 1006 は 0.1 乃至 5 μm の範囲内の厚さとすることが可能である。吸収の向上は 800 乃至 900 nm 又はそれ以上の波長範囲において 50% を越えるものとしてすることが可能である。その向上された吸収は、垂直共振器面発光レーザー等のレーザーを直接的に変調させることによるか、又は光学的変調器がレーザー光を変調させる間接的変調によって発生される光学信号の或る波長範囲に対して最適化させることが可能である。Gb/s でのその変調されたレーザー光が該光学信号である。該光学信号は垂直入射で又は垂直入射に対して或る角度でのいずれかでマイクロストラクチャ型フォトダイオード 1060 上に入射する。マイクロストラクチャ型フォトダイオード 1060 の高速度動作のために P オーミックコンタクトのアノード 1028 と N オーミックコンタクトのカソード 103

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0との間に逆バイアスを印加させる。図示していないものはシリコン表面上の10乃至100nmの厚さのパッシベーション層で、それは、表面再結合において発生するダンダリングボンドを減少させるために、例えば、Siのウェット（蒸気）又はドライ酸化、二酸化シリコンの原子層付着、蒸着、によって成長される。

【0057】

図11は、幾つかの実施例に基づくPINエピタキシャル層を具備している簡単化したマイクロストラクチャ型シリコンフォトダイオードを示している概略図である。MS-PD1160は、マイクロストラクチャ型穴1122がBOX層1004へ完全に貫通してエッチングされていないことを除いて、MS-PD1060と同一である。幾つかの実施例によれば、0.01乃至2μmのN層1006を残存させることが可能である。

【0058】

図12(A)〜(C)は、幾つかの実施例に基づいて、特定のマイクロストラクチャ型穴パターンのマクスウェル伝播方程式方法の有限差分時間領域(FDTD)を使用するシミュレーションの状況を示している。図12(A)は六角形穴パターンを示しており、その穴の中心間距離がx方向において495nmでy方向において860nmである。図12(B)に示してあるように、該穴は2μmの深さまで完全に貫通してエッチングされており、その穴の直径は上部において385nmであり底部において430nmである。図12(C)は、有限差分時間領域技術を使用したシミュレーションの結果を示しているプロットである。曲線1210、1212、1214は、夫々、吸収率、反射率、及び透過率を示している。この特定の例においては、2μmの厚さのシリコンの場合、805乃至830nmの波長範囲の光の60%を超えるものを吸収させることが可能であることが理解される。穴直径、間隔、エッチング深さを変えることによって、光学信号の特定の波長に対して吸収を最適化させることが可能である。幾つかの実施例によれば、穴直径は200乃至1800nmで変化させることが可能であり、間隔は200乃至3500nmで変化させることが可能であり、且つ深さは0.1乃至2μmで変化させることが可能である。

【0059】

図13は、幾つかの実施例に基づいて、P-I-Nドーピングを有する高コントラストマイクロストラクチャ型フォトダイオード(PD)用のエピタキシャル層構造を示している概略図である。Si1302におけるBOX（埋込酸化物）1304で開始して、尚該酸化物層の厚さは0.1乃至10ミクロン又はそれ以上の範囲であり、薄いGeパッド層1370をNSi1302の上に成長させることが可能である。Geパッド層1370を設けるか又は設けずに、その後のN、I、P層1306、1308、1310はGe及び/又はInGaAs、InP、InGaAsP、GaAs、AlGaAs、GaN、InGaN、AlGaN等のIII-V物質群とすることが可能である。N、I、P層1306、1308、1310がSiである場合、Geパッド層1370は省略することが可能である。該PDの高速動作のために、該N層1306は0.1乃至5ミクロンの範囲とすることが可能であり、該I層1308は0.2乃至3ミクロンの厚さ範囲とすることが可能であり、且つ該P層1310は0.1乃至2ミクロンの範囲とすることが可能である。最後の層、この例においてはP層1310、は薄いInGaAsのキャッピングを具備するInPとP層等の複数の層の結合とすることが可能である。

【0060】

図14は、幾つかの実施例に基づいて、P-I-Nドーピングを有する高コントラストマイクロストラクチャ型フォトダイオード(PD)用のエピタキシャル層構造を示している概略図である。該PINヘテロ構造は、Geパッド層1470がI層1408とN層1406との間の界面又はその近くにおけるものとしてすることが可能であり、その場合にI層1408及びP層1410はGe及び/又はIII-V物質群とすることが可能であるということを除いて、図13のものと同様である。この構造例の利点は、Siのバンドギャップ未満の光子エネルギーの場合に、N層1406においてより少ない数の電子・正孔対が発生され、そこで発生されたキャリアーはI層1408内の高電界領域へ拡散

することが可能であり、その結果該PDの高速応答における低速成分となる。該Geバッファ層はヘテロ成長のためには必要ではない場合もある。

【0061】

図15は、幾つかの実施例に基づいて、P-I-Nドーピングを有する高コントラストマイクロストラクチャ型フォトダイオード(PD)用のエピタキシャル層構造を示している概略図である。該PINヘテロ構造は、I領域1508のみがGe及び/又はInGaAs、InSb、InGaAsP、InAs等のIII-V物質群等の一層低いバンドギャップ物質であることを除いて、図13及び14のものと同様である。P層1510及びN層1506の両方が一層高いバンドギャップ物質から構成されている。幾つかの実施例によれば、P層1510及びN層1506はフォトンエネルギーよりも一層高いバンドギャップエネルギーを有しており、且つI層1508はフォトンエネルギーと等しいか又はそれより低いバンドギャップエネルギーを有している。例えば、N層1506はSiとすることが可能であり、I層1508はInGaAs及び/又はGeとすることが可能であり、且つP層1510はSi及び/又はInPとすることが可能である。Geバッファ層はヘテロ成長のためには必要である場合も必要でない場合もある。P領域及びN領域において一層高いバンドギャップ物質を有することの利点は、これらの領域において発生される光キャリアを最小とさせることである。P領域及びN領域において発生される光キャリアは高電界領域へ拡散することが可能であり、その結果短い光学パルスに対してのフォトダイオードの応答における比較的遅い成分となる。したがって、P領域及びN領域において発生される光キャリアを減少させることは「テール効果(tail effect)」、即ちデータを光学的に送信するためのビットストリームにおける如く光学的入力パルス又は1組のパルスにตอบสนองしてPDの電気的パルス出力の下降時間を減少させる。P領域及びN領域の高ドーピングも、これらの領域において発生された光キャリアが高電界「I」領域へ拡散する前に再結合することが可能であるように、少数キャリア寿命を減少させる。

【0062】

図16は、幾つかの実施例に基づいて、高コントラストマイクロストラクチャ型フォトダイオード(PD)の製造の幾つかの側面を示している概略図である。図13に図示した例示的構造が、シリコン層1302内に埋め込まれている酸化層1304までずーとPIN層1310、1308、1306を貫通してエッチングされている穴1622と共に示されている。ドライ及び/又はウェットエッチを使用することが可能であり、原子層付着によって露出表面へパッシベーション層を付加させることが可能である。この例においては、Geバッファ層1370がN層1306とSi層1302との界面に設けられている。幾つかの実施例によれば、図14及び15に示した構造に対して同様の製造方法が使用される。

【0063】

図17(A)-(D)は、幾つかの実施例に基づいて、穴配置、間隔、寸法、及びパッシベーション層の例を示している各概略図である。図17(A)は280nmの間隔でパッシベーション層厚さが50nmである六角形レイアウトを示している。図17(B)は正方形レイアウトを示している。図17(C)及び(D)は、夫々、テーパ付き及び垂直の穴形状を示している。これらの図示例はシリコン用であるが、寸法を多少修正すれば、該技術はGe及びIII-V物質群に対しても適用可能である。該穴は円形断面を有することが可能であり、又は、幾つかの実施例によれば、たとえば、楕円、矩形等のその他の形状とすることが可能である。

【0064】

図18は、幾つかの実施例に基づいて、高コントラストマイクロストラクチャ型フォトダイオード(PD)の製造の更なる側面を示している概略図である。マイクロストラクチャ型穴1622をエッチングし、且つPオーミックコンタクト層1828を付着させ且つアニールさせた後の図13及び16に図示した例示的構造を示してある。

【0065】

図19は、幾つかの実施例に基づいて、高コントラストマイクロストラクチャ型フォト

ダイオード（PD）の製造の幾つかの更なる側面を示している概略図である。図13、16、18に図示した例示的構造が示されている。Pオーミックコンタクト1828を付着させ且つアニールさせた後に、メサをエッチングして物質1972を除去してPDの容量を画定させることが可能である。該メサの直径は該PDに対して望ましいRC時間に依存して5ミクロンから100ミクロンを超える範囲とすることが可能である。露出されたP、I、N領域のパッシベーションを実施して、例えば、ダングリングボンドに起因する漏洩電流を最小とさせる。幾つかの実施例によれば、電氣的に半絶縁性又は絶縁性の領域を発生させることによってPIN構造の容量を画定させるために、メサエッチングの代わりにプロトン衝撃等のイオン注入を使用することも可能である。

【0066】

図20は、幾つかの実施例に基づいて、高コントラストマイクロストラクチャ型フォトダイオード（PD）の製造の幾つかの更なる側面を示している概略図である。図13、16、18、19に図示した例示的構造が示されている。メサエッチングの後に、N層1306上にリング又は部分的リング形状のNオーミックコンタクト2030を形成する。P領域1310へ電氣的なバイアスを印加するためにPオーミックコンタクト1828からボンドパッド（不図示）へのメタリゼーションを接続させるために架橋経路が形成されるようにポリイミド等の物質から絶縁層を形成すること等のPDを完成させるための付加的な処理ステップは図示していない。又、簡単化のための、Nオーミックコンタクト2030をNボンドパッドとの間の接続用金属は図示していない。1層1308内に高電界を形成させるためにP及びNオーミックコンタクト1828と2030とに逆電氣バイアスを印加させる。幾つかの実施例によれば、負の1乃至負の10ボルトの電圧を印加させることが可能である。

【0067】

図21は、幾つかの実施例に基づいて、損失性高コントラストマイクロストラクチャ型フォトダイオード（PD）の幾つかの側面を示している概略図である。図21は、光が吸収層1308内を2度走行するマイクロストラクチャ型PPDを示している。このことは、Si基板1302の一部2174を酸化物層1304まで除去し且つ該酸化物をAu、Ag、Al又はCu等の金属反射器2176でコーティングすることによって達成される。幾つかの実施例によれば、ブロードバンド又は波長選択性のいずれかのためにブラッグ反射器の形態とすることが可能である。幾つかの実施例によれば、特に、粗波長分割多重化、又は波長分割多重化において使用するために更に波長選択性を与えるためにP層1310の上部表面上にブラッグ層を包含させることも可能である。

【0068】

図22（A）及び（B）は、幾つかの実施例に基づいて、特定のマイクロストラクチャ型PDのFDTD方法を使用するシミュレーションの状況を示している。図22（B）は、図21に図示した如きダブルバウンス構造に対するフォtonsの波長に対してのフォtonsの吸収のシミュレーション結果を示しているプロットである。該シミュレーションにおいて使用された例示的な厚さは以下の通りであり、即ち、酸化物1304は2ミクロン、Pシリコン1310は300nm、ISI1308は2ミクロン、及びNシリコン1302は300nmであり、反射器2176は100nm厚さのAuである。図22（A）に示した如く、六角形マイクロストラクチャ型穴を採用している。図22（A）に示されている如く、該穴は中心間六角形周期が600nmであり、穴直径が480nmであり、SiO₂パッシベーションが30nmである。これらの寸法は、波長に対する吸収特性の対応するシミュレーションを有するマイクロストラクチャ型穴に対する単なる一つの例である。図22（B）の曲線2210（吸収）及び2212（反射）から理解することが可能であるように、マイクロストラクチャ型穴の無いSiの場合におけるよりも吸収が著しく一層高いものであることが判明した。例えば、850nm波長の近傍において、吸収は70%よりも一層良い。

【0069】

図23は、幾つかの実施例に基づいて、高コントラストマイクロストラクチャ型PDの

或る側面を示している概略図である。下部構造は図20の構造と類似しており、即ち、Si基板2302、SiO₂層2304、及びSiN層2306である。下部Si層2308を設けることも可能である。この場合、Geは上部I層2309及びP層2310として使用される。P層2310は、GeI層2309上に成長させることが可能なInPから構成することも可能である。InP層2310の利点は、それが0.9乃至2μmの波長においての吸収性がより低いということである。P層2310はGeI層2309上に成長されるGaAsから構成することも可能である。更に、マイクロストラクチャ穴2322、Pオーミックコンタクト2328、Nオーミックコンタクト2330も示されている。注意すべきことであるが、光はP層2310の上部表面上及び／又はSi基板表面2302上に入射することが可能である。

【0070】

図24は、幾つかの実施例に基づいて、ヘテロエピタキシャルマイクロストラクチャ型PDの状況を示している概略図である。この場合に、I領域は、Ge層2470によって分離されているSi（下部層2408）とInGaAs（上部I層2409）との複合体とすることが可能である。P領域2410はInPである。幾つかの実施例によれば、該I領域は、その全体をバッファGe層2470の薄い層の上に成長させたInGaAsとすることが可能である。更に、Si基板2402、酸化物層2404、N層2408、マイクロストラクチャ穴2422、Pオーミックコンタクト2428、及びNオーミックコンタクト2430も示されている。これは、高コントラストマイクロストラクチャ型PD構造の1例である。それは、更に、図21における如き金属反射器を組み込むことが可能であり、その場合には、該PD下側の酸化物層へエッチングすることによってSiを除去し且つAu、Ag、Al又はCu金属層を付着させて光をI吸収層へ向けて反射させることが可能である。上述した如くブラック反射器を使用することも可能である。光は、この例においては、P層側からやってくる。光はSi基板側から来ることも可能であり、その場合には、I層を二度走行させるために反射器が該P層上に配置される。このような構成の利点は、I層を単一走行の場合のものから不変のまま維持しながら、吸収領域を二度又はそれ以上走行させることによって吸収が著しく改善されるということを含む。吸収領域厚さを、例えば、単一走行PDのものの半分へ減少させることによって、PDの速度が増加する。何故ならば、光発生されたキャリアーに対する走行時間は単一走行PDの距離の半分だけ走行することが必要であるに過ぎないからである。高コントラストマイクロストラクチャとは、該マイクロストラクチャ及び一つの表面界面における空間又は大気及びSiO₂及び／又は別の表面界面におけるバルク半導体物質の間の屈折率差のことを意味している。光は結合型固有セル又は共振器セルの複雑な態様で該マイクロストラクチャと相互作用を行い、その場合に、格子内の各六角形又は正方形セルは、発生する場合がある線形及び非線形の光学的フィールド向上に加えて、その隣接するセル又は共振器と結合されている個別的な共振器として考えることが可能である。光学的損失が存在しないか又は殆ど存在しない場合には、その結合型共振器構造は高いQ（共振器の品質係数）を有することが可能であり、即ち、光は、例えば、消失する前に10⁴乃至10⁸回を越えて該マイクロストラクチャ内において繰り返しバウンス即ち跳ね返ることが可能である。しかしながら、弱い吸収に起因する等の光学的損失が或る場合、Qは低い場合があり且つ光は100回未満、又は20〜30回未満だけ該マイクロストラクチャ内で繰り返し跳ね返る場合がある。PD/APDにおけるマイクロストラクチャは低Q高コントラスト構造又は損失性高コントラスト構造であり、各セルのQは隣接するセルに結合されている。

【0071】

図25は、幾つかの実施例に基づいて、発光ダイオード（LED）又は垂直表面発光レーザー（VCSEL）等の光学的発光器に対する高コントラスト構造を示している。光学的発光器2500はヘテロエピタキシャル層構造である。Si層2506をSi基板2502及びBOX/SiO₂層2504上に形成する。バッファGe層2570をSi層2506上に形成することが可能であり、続いて層2510を形成することが可能であり、該層2510はInAs量子ドット2572とし、GaAs及びAlGaAsで被覆させ

ることが可能である。更に、「I」層を約1000nm以下の薄いものとすることが可能であり且つ順方向バイアスさせる簡単なSiPINマイクロストラクチャはフォトン射出体とすることが可能である。

【0072】

図26は、例えば、幾つかの実施例に基づき、高コントラスト1.3ミクロン波長フォトエミッタ(PE)用の基本的な構造を示している。1.3ミクロン波長エミッタ用のアクティブ層は、InAs量子ドット層2570(図25に図示)又は図26における2670をGaAsP層2604とN層2606との間に挟み込み、それらをAlGaAsP層2608とN層2602との間に挟み込み、且つPGaAsキャッピング層2610を最終層として使用して形成される。典型的な厚さは文献中に見出すことが可能である。例えば、AY Lin, S Srinivasan, J Norman, AC Gossard, JE Bowers等のシリコンフォトニクス用量子ドットレーザー(Quantum Dot Lasers For Silicon Photonics)、フォトニクスリサーチ3(5)、B1-B9(2015)を参照すると良く、この文献を引用により本書に取り込む。更に、量子ドット及び/又は被覆層の複数の層がある場合がある。該マイクロストラクチャは、利得及び光学的フィールドオーバーラップを最適化させるために、QD層の内の一つ又はそれ以上に定常波ピークが位置されるように構成することが可能である。MS-PP/APDの場合、該マイクロストラクチャの長さは、特定の波長において、整数個の波長が往復して、例えば、その特定の波長においての吸収の向上を最適化させるようなものとさせることが可能である。更に、単一のマイクロストラクチャ、例えば、単一の穴が、マイクロストラクチャの無い同様の構造のものと比較して、PE又はMS-PP/APDのいずれかに対して吸収又はエミッションの向上を有することが可能である。

【0073】

図27は、幾つかの実施例に基づいて、エッチングした穴を具備する高コントラストマイクロストラクチャ型フォトエミッタ(PE)構造の幾つかの基本的な特徴を示している概略図である。その物質構造は図25に示したPE2500のものと同様である。マイクロストラクチャ穴2722はアクティブ層2510内にエッチングされている。P及びNオーミックコンタクト2728及び2730を使用して、装置2700を順方向にバイアスさせ、即ちNに対してPを正とさせてアクティブ層2510からフォトンが発生させ、該アクティブ層2510は、本例においては、1.3ミクロンの波長においてのInAs量子ドット2572を有している。可視光から赤外光のその他の波長において光を発生させるために、その他のアクティブ層、被覆層を使用することが可能である。光の波長に依存して、光は上部表面から及び/又は酸化層2504を介して底部表面から射出させることが可能である。マイクロストラクチャ型高コントラストフォトンエミッタの利点は、フォトンが該アクティブ層及び/又はレーザーの場合には利得層と一層長く相互作用を行うことである。何故ならば、該高コントラスト構造は非常に高いQを有することが可能であり、そのQは 10^3 乃至百万以上の範囲に亘り、というのも、該構造は殆ど光学的損失を有するものではなく且つ該量子ドットが光学的利得を与えるからである。該高コントラスト低損失マイクロストラクチャ型フォトエミッタはLEDとして、VCSELとして、及び/又はレーザー及び/又は高出力LEDとして動作することが可能である。該PEは順方向バイアスされ、Nオーミック即ちN層であるカソード2730に対してPオーミック即ちP層は正電圧にある。

【0074】

図28は、幾つかの実施例に基づいて、PEの幾つかの側面を示している概略図である。PE2800は、基板2502の一部2874が光射出領域下側で酸化層2504へ除去されていることを除いて、図27に示したPE2700と同様である。金属及び/又は分散型ブラッグ反射器(DBR)2504等のブラッグからなる反射器を該酸化層上に形成してアクティブ層内で発生された光をP層2510表面へ反射して戻させる。幾つかの実施例によれば、装置2800はLEDモード及び/又はレーザーモードで動作する。

【0075】

図29は、幾つかの実施例に基づいて、PEの幾つかの側面を示している概略図である。PE2900は、金属とすることが可能であり且つ、所望により、Pオーミックコンタクトとしても動作することが可能な反射器2928を包含している点を除いて、図28のPE2800と同様である。幾つかの実施例によれば、別体のPオーミックを設けることが可能である。反射器2928は分散型ブラッグ反射器及び／又は部分的に金属及び部分的にDBRとすることも可能である。光は酸化物質層2504の下部表面から且つ一部2874が除去されている基板2502を介して射出される。フォトエミッタ即ち光射出器2900は、LED及び／又はVCSELモード等のレーザーモードで動作することが可能である。幾つかの実施例によれば、フォトエミッタ2900はエッジモードで動作することが可能であり、その場合に光はアクティブ層の面に対して垂直ではなく面内において射出され、射出エッジに沿ってDBR又は金属等のミラーが存在する場合も存在しない場合もある。

【0076】

図30は、幾つかの実施例に基づいて、PEの幾つかの側面を示している概略図である。PE3000は図29のPE2900と同様であるが、VCSEL（垂直共振器面発光レーザー）として構成されている。PE3000は高コントラストマイクロストラクチャ型穴（又は柱体）を具備しておりSi上にヘテロエピタキシャル成長されている。注意すべきことであるが、簡潔性のために非常に基本的な部品のみが示されているに過ぎない。該高コントラスト構造は反射器2928及び3076によって挟み込むことが可能である。P層2510は半導体エピタキシーによって成長されたDBRとすることが可能であり、それに続いてPオーミックメタリゼーション層2928を設けることが可能である。幾つかの実施例によれば、DBRは導電性酸化物又は非導電性酸化物から形成することが可能であり、DBR上にP金属を設けるか及び／又は図28における如くその側部上に設けることが可能である。酸化物質層2504の底部側上のミラー3076は金属及び／又は異なる屈折率の誘電体層のDBRとすることが可能である。図示した如き光出力は底部からのものであるが、上部からのものとすることも可能である。

【0077】

図31は、幾つかの実施例に基づいて、簡単なPINフォトダイオード構造の幾つかの側面を示している概略図である。高電界領域外側の領域において発生された光キャリアーに起因する拡散電流を最小とさせるために、「I」層3108、P及びN層3110及び3106は高度にドーピングさせ及び／又は縮退的にドーピングさせて少数キャリアーの寿命を減少させる。N及びPドーピングは 1×10^{18} 乃至 $8 \times 10^{21} / \text{cm}^3$ 以上の範囲とすることが可能である。I層3108は意図的にドーピングしておらず且つ $5 \times 10^{16} / \text{cm}^3$ 未満とすることが可能である。更に、酸化物質層3104とSi基板3102とが示されている。前の例におけるように、Geバッファ層を付加するかしないかに拘わらず、Ge及び／又はIII-V物質を成長させることが可能であり且つP及びN層も高度にドーピングさせるか及び／又は縮退的にドーピングさせることも可能である。そのドーピングは一種なものであることは必要ではなくグラデーションを有することが可能であり、例えば、エピタキシャル成長期間中に「I」層内へのドーパントの拡散を最小とさせるために「I」層界面近くのP又はN層においてドーピングを減少させる。

【0078】

P及びN層における少数キャリアーの寿命を減少させることによって、これらの層内の光発生されたキャリアーは拡散し及び／又は高電界「I」内に移動する前に再結合することが可能であり、該高電界「I」においては、電子及び／又は正孔が光電流に貢献してフォトダイオード変調型周波数応答の劣化となる場合がある。従って、高電界領域外側で発生されたキャリアーに起因する光電流の寄与を最小とさせることが望ましい。

【0079】

少数キャリアーの寿命を減少させるその他の方法は、P及び／又はN領域における部分的及び／又は完全なパイオン注入等の欠陥を導入することを包含している。導入される

イオンは不活性イオン及び／又は活性イオンとすることが可能であり、部分的な又は完全な熱アニーリングを行うか又は行わないことが可能である。更に、該マイクロストラクチャ型穴（及び／又は柱体）は部分的なパッシベーションを行うか又は行わないものとすることが可能であり、従って、N及びP層の低電界領域はキャリアシンクとして作用することが可能であり、一方、「I」層の高電界領域においては、該キャリアーは迅速に一掃される。パッシベーションは「I」層上において目だって選択的とすることが可能である。

【0080】

図32は、幾つかの実施例に基づく、MS-PD製造の幾つかの側面を示している概略図である。開始物質構造は図31の構造3100に図示した如きものとすることが可能である。簡単なNIP（N及びPはPINに対しては交換可能である）マイクロストラクチャ型フォトダイオードが示されており、その場合に、穴3222がP層3106の上部へエッチングされている。その目的はN及び「I」層の壁をパッシベーションし且つP層の壁をパッシベーションせずにおいてそれにより、例えば、780乃至980nmの波長を有する光で発生されるP層内の少数キャリアーの寿命を減少させる。パッシベーションされていないP壁の表面状態は少数キャリアー用の潜在的なシンクとして作用することが可能であり、そこで該キャリアーは再結合される。

【0081】

図33は、幾つかの実施例に基づいて、MS-PD製造の或る側面を示している概略図である。N及び「I」層の穴3222の側壁のパッシベーションが示されており、結果的にパッシベーション層3324が形成されている。該パッシベーションは熱酸化及び／又はSiO₂の原子層付着を使用して実施することが可能である。5〜50nm厚さの熱酸化物3324を、例えば、該側壁上に成長させることが可能である。その他の厚さのものを成長させることも可能である。熱酸化の後に、穴のエッチングを継続して行い、例えば、P層3106を貫通してSiO₂層3104へエッチングすることが可能である。全ての処理ステップが示されているわけではなく、例えば、穴のエッチングを継続する期間中に不図示の熱酸化物によってN層を保護することが可能である。

【0082】

図34は、幾つかの実施例に基づいて、MS-PD製造の側面を示している概略図である。パッシベーションの後に、穴3222は区域3422で示した如くに更にエッチングされる。注意すべきことであるが、N及びP層は交換させることが可能であり、従ってこの例において示されている如きNIP構造の代わりに、PIN構造とすることも可能である。穴3222はSiO₂層3104へエッチングさせることが可能であり、及び／又はそれらはP層3106を介して部分的にのみエッチングさせ、薄いP層が残存するようにさせることが可能である。P層3106内の穴3222の側部は、この例においては、パッシベーションされておらず、その表面状態が光によって発生される何らかの少数キャリアーをその潜在的なシンクへと引き込んで再結合させることを可能としている。幾つかの実施例によれば、P層3106もパッシベーションさせ及び／又は部分的にパッシベーションさせることが可能である。層3106も高度にドーブさせることが可能であるので、少数キャリアーの寿命は数十ピコ秒以下である可能性がある。

【0083】

図35は、幾つかの実施例に基づいて、MS-PDの或る側面を示している概略図である。マイクロストラクチャ型NIPフォトダイオード3560は、N及び「I」層のパッシベーションされた側壁を具備しているがP層の側壁はパッシベーションされていないマイクロストラクチャ穴3222を有している。N及びP層の夫々へのオーミックコンタクト3528及び3530が付加されてフォトダイオード3560の高速動作のための逆バイアスを与えている。該フォトダイオードのN側上に入射する光は垂直であるか及び／又はN層面に対して垂直からずれたもののいずれかである。

【0084】

図36は、幾つかの実施例に基づいて、MS-PDの或る側面を示している概略図であ

る。マイクロストラクチャ型穴フォトダイオード3660はS i N i P層を有しており、その場合に、パッシベーションは図35に示したPD3560と同様に側壁上で部分的である。しかしながら、PD3660の場合には、光はS i基板側からオプティカルファイバー3680を介してやってくるが、そこではピア3672がエッチングされているので自己整合プロセスを可能とさせ、その場合に、ファイバー3680は、レンズ3682と共に又は無しで、ピア3672に沿って光のマイクロストラクチャ型フォトダイオード3660内への光学的結合を行うための正しい位置へ案内される。略0.1-10 μm 厚さの誘電体層3676を穴3222上方のN層3110上に位置決めさせることが可能である。誘電体層3676上にはA g又はA u（又は任意のその他の適宜の金属又は合金で、例えば、A l、N i、C r等）等の金属反射器3678及び／又は吸収用「I」層3108へ向けて光を反射させるためにブラッグ反射器（BR）等の誘電体積層体を設けることが可能である。反射防止コーティング3674を設けることも可能である。先の例における如く、Geパッファ層を付加するか又は付加せずにGe及び／又はI I I-V物質を成長させることも可能である。

【0085】

図37は、幾つかの実施例に基づいて、少数キャリアの寿命を減少させるための技術を示している概略図である。この場合には、穴表面をパッシベーションするか又は部分的にパッシベーションする代わりに、表面及びバルクの再結合が使用される。 $10^{20}/\text{cm}^3$ より大きな高ドーピングは拡散長を例えば0.1 μm （オーガ（Auger）再結合）未満へ減少させることが可能である。更に、層3710及び3706内に欠陥3770及び3772を導入させるためにイオン注入が使用される。半導体内の欠陥はショックリーリード-ホール（Shockley-Read-Hall）再結合プロセスを介して寿命を減少させることも可能である。例えばX e、B i、T i、C r、A r、N等のイオンをN及び／又はP層内に注入させることが可能である。装置動作のために長い少数キャリアの寿命が望ましい場合の既知の構造と逆に、本書に記載する技術は、ショックリーリード-ホール効果に起因する再結合率を増加させるために、エピタキシャル成長及び／又は金属、非金属及び不活性イオンのイオン注入のいずれかによって欠陥を導入させる。該欠陥に起因して深い及び／又は浅いトラップを形成させることが可能であり、それらは少数キャリアの寿命を短くさせることが可能である。少数キャリアの寿命が短いことは、高電界領域「I」層へ通じて光電流に寄与することが可能な拡散電流の寄与を最小とさせるためにP及びN領域において望ましいものである。該「I」領域内へ拡散及び／又は走行するこれらの「遅い」拡散電流は、フォトダイオードの光電流時間応答特性に対しての遅い成分に寄与することによってフォトダイオードの時間応答の劣化を発生させる場合がある。

【0086】

図38（A）乃至（C）は、シミュレーションしたマイクロストラクチャ型フォトダイオードに対する種々のパラメータを示している。図38（A）は穴中心間の距離「d」を有している六角形穴パターンを示している。図38（B）は穴中心間の距離「d」を有している正方形穴パターンを示している。図38（C）はFDTD方法を使用したシミュレーションに対して使用したパラメータの表である。850乃至950 nm及び、例えば、980 nmの範囲の光学信号の波長に対して六角形状格子の穴における周期が2000 nmで直径が1300乃至1500 nmの範囲の複数の穴で2-2.5 μm の厚さのS i O₂層上の2 μm 厚さのシリコン層で90%より大きな吸収を達成することが可能であることが判明した。更に、波長は750-1000 nmの範囲に亘ることが可能である。穴直径は、サブ波長乃至入射光学信号の波長より大きなものとすることが可能であり、100乃至3000 nmの直径の範囲に亘る。S i吸収層の厚さは0.3乃至10 μm の範囲とすることが可能である。S i O₂層は0.2乃至10 μm の範囲に亘ることが可能である。幾つかの実施例によれば、入射フォtonsの吸収を最適化させるために複数の穴直径の混合を使用することも可能である。

【0087】

図39は、波長に対する吸収に対してのFDTDを使用するマイクロストラクチャ型穴

フォトダイオードのシミュレーション結果をプロットしたグラフである。フォトダイオード吸収「1」層は $2\mu\text{m}$ 厚さであり、穴直径は 1000 乃至 1500nm の範囲にわたるものであった。入射エネルギー波長は 850 乃至 950nm の範囲であった。3つの曲線3910、3912、3914は、夫々、 1000nm 、 1300nm 、 1500nm の穴直径に対しての吸収のプロットである。このシミュレーションは、 1500nm の穴直径の場合、 $850-870\text{nm}$ の波長範囲にわたって90%より大きな吸収が達成されており、且つ、 1300nm の穴直径の場合、 2000nm の周期での六角形状格子での穴で 875 乃至 950nm の波長範囲にわたって80%より大きな吸収を達成することが可能であることを示している。 $2\mu\text{mSi}$ は $2-2.5\mu\text{mSiO}_2$ 層の上にある。理解されるように、何らの特徴無しでの従来のシリコン層のものを越えて吸収を向上させるために、入射波長よりも一層大きな穴直径を有することを使用することが可能である。

【0088】

図40は、幾つかの実施例に基づいて、P-I-P-I-Nエピタキシャル構造を具備するマイクロストラクチャ型アバランシェフォトダイオード(APD)を示している概略図である。図40の場合には、APD4060の全ての層は、例えば、 780 乃至 1000nm の範囲の光学的通信波長に対してシリコンである。APD4060は可視光波長範囲においても動作可能である。データレートは 100Mb/s 乃至 50Gb/s 又はそれ以上の範囲に置ることが可能である。 -4 乃至 -50 ボルトの電圧範囲でP及びNオーミックコンタクト4028及び4030間に逆バイアス電圧を印加させる。アバランシェマイクロストラクチャ型フォトダイオード4060は以下のようなドーピング及び厚さを有することが可能であり、即ち、例えば、P層4010のドーピングは $1\times 10^{18}/\text{cm}^3$ を越えるもので且つ厚さは $0.1-1.0\mu\text{m}$ であり、I層4008のドーピングは $1\times 10^{15}/\text{cm}^3$ 未満であって且つ厚さは $0.5-3\mu\text{m}$ であり、P層4020のドーピングは $1-3\times 10^{17}/\text{cm}^3$ であって且つ厚さは $0.1-0.5\mu\text{m}$ であり、I層4018のドーピングは $1\times 10^{16}/\text{cm}^3$ 未満であって且つ厚さは $0.3-1\mu\text{m}$ であり、及びN層4006のドーピングは $1\times 10^{19}/\text{cm}^3$ であって且つ厚さは $0.5-3\mu\text{m}$ である。幾つかの実施例によれば、上の2つの層4010及び4008はSiの代わりにGeとすることも可能である。穴4002はAPD層を部分的に貫通してエッチングさせるか又は図40に示されている如く SiO_2 層4004へ完全にエッチングさせることが可能である。

【0089】

マイクロストラクチャフォトダイオードの場合における如く、APDの場合に、光学信号は正面側(エピタキシャル層側)から入射するか又は背面側(基板側)から入射することが可能である。更に、基板内にピアがある場合、反射器を SiO_2 上に付着させることが可能であり、その結果、APD構造内において光学信号を2回又は多数回バウンス即ち跳ね返させることとなる。幾つかの実施例によれば、PとNとは交換可能であり、その結果N-I-N-I-Pマイクロストラクチャ型APDとなる。

【0090】

図41は、幾つかのその他の実施例に基づいて、P-I-P-I-Nエピタキシャル構造を具備するマイクロストラクチャ型アバランシェフォトダイオード(APD)を示している概略図である。APD4160は、複数の穴4122(又は柱体)が部分的にエッチングされていることを除いて、図40に図示したAPD4060と同一である。図41に示した例においては、穴4122はP層4020内に部分的にエッチングされており及び/又はP層4020で停止している。幾つかのその他の実施例によれば、穴4122はI吸収層4008内に部分的にエッチングさせることが可能である。

【0091】

図42は、幾つかの実施例に基づいて、Ge吸収層及びGePキャッピング層を具備しているマイクロストラクチャ型APDを示している概略図である。APD4260は、上の2つの層がSiの代わりにGeであるという点を除いて、図40に図示したAPD4060と同様又は同一である。APD4260は、PGe層4210が $1\times 10^{20}/\text{cm}^3$

より大きなドーピングレベルを有することが可能であるという点を除いて、APD 4060に対して上述した如き同じドーピング及び厚さ範囲を有することが可能である。埋込酸化物(BOX)シリコン基板上のAPD構造 $P(Ge)-I(Ge)-P(Si)-I(Si)-N(Si)$ のエピタキシャル成長の後に、該マイクロストラクチャをエッチングする。該マイクロストラクチャは穴、柱体又はこれら2つの結合とすることが可能である。該エッチングは SiO_2 層まで行うことが可能であり、又は SiO_2 層4004に到達する前の深さへ部分的にエッチングすることも可能であり、例えば、穴は PSi 層4020まで又はその中へエッチングさせることが可能である。マイクロストラクチャを具備しているGe吸収層4208は、100Mb/s乃至50Gb/s又はそれ以上のデータレートにおいて780乃至2000nmの波長で光学信号が動作することを可能とさせるものと期待されている。該光学信号は上部表面(エピタキシャル表面)から又は底部表面(基板表面)から入射することが可能である。ピア及び SiO_2 上に付着させた反射器がある場合には、上部表面から入射する光学信号を、2回目及び/又は多数回にわたり吸収 $I(Ge)$ 層4208へ反射させることが可能である。 Si と、空気と、 Ge との間には光学的屈折率差があるので、定常波を確立させることが可能であり、且つ定在波又は固有モードとしても既知の定常波のピーク強度において吸収層を有するべく該構造の厚さを最適化させることが可能である。更に、 Si がトランスペアレント即ち透明である波長において、光学信号が底部表面からAPD内へ結合することを助けるためにマイクロレンズを Si 基板内にエッチングさせることが可能である。底部から入射する光学信号を吸収 $I(Ge)$ 層4208へ反射させるために $P(Ge)$ 4210上に SiO_2 及び反射器を配置させることが可能である。-4乃至-50ボルトの範囲の逆バイアス電圧をP及びNオーミックコンタクト4028と4030との間に印加させる。

[0092]

図43(A)乃至(D)は、幾つかの実施例に基づいて、マイクロストラクチャ型フォトダイオード及びAPDの分極感度を示している。図43(A)はシミュレーション用に使用した幾何学的形状を示している。これらの穴は寸法及び周期において対称的であり、B又はAのいずれかに沿っての光学信号の電界分極は $MS-PD/APD$ の吸収特性において5%未満の差を示している。吸収は、入射光からその光の透過及び反射を差し引いたものと等しく、且つ量子効率は吸収に直接的に比例する。穴寸法「a」及び「b」が同じでない場合には、 $MS-PD/APD$ は分極感度を示す。図43(B)において、曲線4310は波長に対しての吸収をプロットしており、その場合、「a」及び「b」寸法は両方共1000nmに等しい。該吸収特性は5%未満の差異を示している。図43(C)は $a=1300nm$ で $b=870nm$ の場合を示している。曲線4320及び4322は、A又はBに沿っての分極が或る場合の吸収値における差異は高々2倍であることを理解することが可能であることを示している。図43(D)は $a=1500nm$ で $b=650nm$ である場合に対する結果を示している。曲線4330及び4332は、分極配向(polarization orientation)に起因する吸収差も高々2倍であることを示している。「a」、

「b」、A及びBの両方における異なる寸法変化がある場合に、分極配向に起因する吸収差は10乃至100倍、又はそれ以上異なる場合がある。分極「不感受性」(分極配向に起因する吸収変化が5%未満の場合)及び分極感受性(分極配向に起因する吸収変化が10倍又はそれ以上の場合)の両方のフォトダイオード及びAPDが有用である。信号が分極多重化されていない場合、例えば、同じ波長を使用する場合、2つのチャンネルを送信することが可能であり、その場合に一つのチャンネルは一つの分極で且つ別のチャンネルは第1のチャンネルに対して直交している。例えば、各チャンネルは同じ波長において特定の分極において25Gb/sで送信することが可能である。受信機端において、該信号をデマルチプレクス、即ち脱多重化、させるために分極感受性光検知器を使用する。総合データレートは850nmの波長において50Gb/sである。レーザーの直接変調において、該レーザーのスペクトルは、例えば、CWモードで動作しているレーザーよりも常に一層幅広である。該スペクトルは高々数ナノメートル(例えば、3nm)だけ広くさせることが可能である。従って、850nmにおいて、レーザーが直接的に変調される場合

には、高々±約1.5nm広げて中心周波数は850nmとすることが可能である。垂直共振器面発光レーザーにおいては、マルチな横モードに起因して、横モードは一層幅広のスペクトルに対して著しく寄与することが可能である。マルチモードシステムにおいては、このことはモード選択損失を減少させるので望ましいことである。

【0093】

図44は、幾つかの実施例によれば、データ処理及び／又はルーチングのために相互インピーダンス及び／又は別のASIC（応用特定集積回路）と集積化されているMS-PD/APDを示している。そのプロセスはCMOS及び／又はBiCMOSとすることが可能である。MS-PD/APD4420は電気的リード4422を介してエレクトロニクス4430（例えば、相互インピーダンス増幅器（TIA）及び／又は別のASIC）へ電気的に接続されていることが示されている。その部品は全て単一のシリコン基板4410上に集積化されている。マイクロストラクチャ型PD/APDをICエレクトロニクスと集積化させることの一つの利点はパッケージングコストの低下であり、その場合に、2個又はそれ以上の個別的な装置の代わりに、単一のチップが使用され、それは又マルチチップセラミック担体を使用すること無しに回路ボード上に直接的に配置させることも可能である。単一チップ上にMS-PD/APDをエレクトロニクスと集積化させることの別の利点は、オーミックコンタクトへ接続されている比較的大きなボンダパッドを省略することによって、潜在的に容量が低くなることである。動作波長は、全てのシリコンマイクロストラクチャ型PD/APDに対して800-990nmの範囲である。動作波長はGeマイクロストラクチャ型吸収層を付加した場合には1800nmへ拡張させることが可能である。10、28、56Gb/sのデータレートでの動作は単独で又はアレイで達成させることが可能である。該データレートは、又、プロトコル及びリンク適用例に依存して1、5、20、25、30、40Gb/sとすることも可能である。典型的に、マルチモードファイバー及び／又は複数のファイバにわたっての高データレートは1メートル未満から100メートルを超える長さにもわたる距離で使用される。複数のファイバ及びマイクロストラクチャ型PD/APD（MS-PD/APD）のアレイを使用して100乃至400Gb/sの総合データレートを与えることが可能である。例えば、単一シリコンチップ上の相互インピーダンス増幅器（TIA）及び／又はその他の信号処理／ルーチングICエレクトロニクス等のICエレクトロニクスと集積化されている10MS-PD/APDアレイと共に各ファイバーが10Gb/sで動作している10ファイバーチャンネルは100Gb/sの総合データレートを有することが可能である。各チャンネルが56Gb/sである場合には、該10チャンネルは500Gb/sを超える総合データレートを有することが可能である。

【0094】

図45は、幾つかの実施例に基づいて、単一シリコンチップ上のTIA及び／又は別の信号処理ICと集積化されているMS-PD/APDに対するフリップチップ配置の幾つかの側面を示している概略図である。幾つかの実施例によれば、TIA及び／又はその他の信号処理集積回路4530はCMOS及び／又はBiCMOSプロセスを使用して製造される。半田パンプ4512及び4514及び／又は同様のパンプ技術を使用してチップ4510をPCB（プリント回路基板）4550へ取り付け。幾つかの実施例によれば、半田パンプ4512の幾つか又は全てを使用してチップ4510とPCB4550との間の電気的接続を行い、一方、半田パンプ4514は物理的マウンティング及び／又は安定化のために使用される。何故ならば、MS-PD/APD4520とPCB4550との間の直接的な電気的接続は必要ではない場合があるからである。幾つかの実施例によれば、チップ4510を、PCB4550の代わりに、別のチップ又はマルチチップ担体へ取り付け。チップ4510をPCB4550上に直接的にパッケージングすることは、PCB上に配置させる前にPD及びICエレクトロニクスを最初にマルチチップセラミック担体上にマウントさせるという既知の従来技術と比較して、高々80%だけパッケージングコストを減少させる。更に、オブチカルファイバー4524からMS-PD/APD4520へ光をフォーカスさせるためにシリコンチップ4510上に集積化光学レンズ452

2を製造させることが可能である。注意すべきことであるが、この構成においては、光信号はMS-PD/APD 4520の基板側から入る。S1上の集積化レンズ4522は、入ってくる光学信号の吸収のためにGeマイクロストラクチャを使用することが可能であり動作波長が1100nmより大きい(例えば、1100nm乃至1800nm)である場合に、使用することが可能である。

【0095】

図46は、幾つかの実施例に基づいて、単一シリコンチップ上にTIA及び/又は別の信号処理ICと集積化されているMS-PD/APDに対するフリップチップ配置の幾つかの側面を示している概略図である。該チップ及びマウント技術は図45に図示し且つそれについて説明したものと同様か又は同一である。この場合に、チップ4510はビア4626を包含しており、そこではMS-PD/APD 4520への光学経路における殆ど又は全てのシリコンは除去されている。光を収集し且つそれをMS-PD/APD 4520へ指向させるために集積化誘電体レンズ4622が設けられている。幾つかの実施例によれば、レンズ4622の代わりに光パイプが使用される。ビア4626の側壁は光の収集を助けるために誘電体及び/又は金属でコーティングすることが可能である。光学信号がオプティカルファイバー4524へ反射して戻ること減少させるためにレンズ4622上に反射防止コーティングを設けることが可能である。更に、ファイバー4524又はチップ4510を傾斜させてファイバー4524へ戻る反射を減少させることが可能である。オプティカルファイバー4524は、1Gb/s未満から60Gb/sを越える範囲のデータレートでレーザー光源からの光学信号を集積化PD/APD及びICエレクトロニクス回路4510へもたらすために使用される。幾つかの実施例によれば、約1、5、10、20、28、50、56Gb/sのデータレートを使用することが可能である。幾つかの実施例によれば、光学信号波長は全シリコンマイクロストラクチャ型PD/APD(MS-PD/APD)に対して800-990nmの範囲にわたる場合があり、且つ吸収層用のマイクロストラクチャ型Geの場合には、該波長は1800nmへ拡張させることが可能である。

【0096】

図47は、幾つかのその他の実施例に基づいて、単一シリコンチップ上のTIA及び/又は別の信号処理ICと集積化されているMS-PD/APD用のフリップチップ配置の幾つかの側面を示している概略図である。そのチップ及びマウント技術は図45及び46に図示し且つそれらについて説明したものと同様であるか又は同一である。図45及び46におけるように、単一のチップ4510は光学的要素と電子的要素との両方を包含している。集積化フレネルレンズ4722と共にMS-PD/APD 4520への光学経路におけるS1の殆ど又は全てを除去するためにチップ4510の基板内にビア4626が設けられているので、光学信号はオプティカルファイバー4524から効率的に収集される。収集された光学信号はMS-PD/APD 4520上に入射する。幾つかの実施例によれば、フレネルレンズ4722の代わりに、高コントラストグレーティング(HCG)が使用される。幾つかの実施例によれば、HCGはフィルタ効果をも有することが可能であり、従って特定の光学波長のみをMS-PD/APDへ透過させ、一方その他を反射させることが可能である。この帯域通過特性は単一のファイバーにおいて複数の波長が使用される粗波長分割多重化(CWDM)にとって有用である。

【0097】

図48は、幾つかのその他の実施例に基づいて、単一シリコンチップ上のTIA及び/又は別の信号処理ICと集積化されているMS-PD/APDに対するフリップチップ配置の幾つかの側面を示している概略図である。該チップ及びマウント技術は、図45-47に図示し且つそれらについて説明したものと同様であるか又は同一である。ビア4626の壁は、光がMS-PD/APD 4520へ入射するための光パイプを提供するために誘電体及び/又は金属でコーティングすることが可能である。次いで、オプティカルファイバー4524をビア4626内へ挿入させることが可能であり、その場合に該ビアはファイバー4524をMS-PD/APD 4520に対して整合させるためのガイドを提供し

、それによりMS-PD/APDに対するオプティカルファイバーの光学的バックリング及びアライメントを単純化させて約30%又はそれ以上のコスト低下を生じさせる。幾つかの実施例によれば、ファイバー4524はテーパ付きとさせることも可能であり、及び／又はビア4626がファイバー4524に対するストップを与えるように複数の直径を有することが可能である。例えば、ビア4626にステップ即ち段差を設けてファイバー4524の端部をそのステップ上に当接させることが可能であり、それをシリコンへ取り付けることが可能である。このステップ構成は、又、最適な光収集のためのファイバーとMS-PD/APDとの間の精密な距離を与える。幾つかの実施例によれば、ファイバーからMS-PD/APDへの光学信号の転送を最適化させるために、ビア4626において、特にファイバー4524とMS-PD/APD4520との間の空間において、屈折率整合流体、ゲル及び／又はポリマー及び／又は誘電体バルク又は薄膜を使用することが可能である。

【0098】

上述した如く、基板側から光が入射する場合（底部照射）、MS-PD/APDは該MS-PD/APD内における光学信号の二重及び／又は多重のバウンス即ち跳ね返りを使用することが可能である。このことは、高い量子効率を達成すると共に吸収層を一層薄くさせることを可能とさせる。一層薄い吸収層は一層高速の走行時間とすることを可能とさせ、それによりMS-PD/APDが一層高いデータレートで動作することを可能とさせる。

【0099】

図49は、幾つかのその他の実施例に基づいて、単一シリコンチップ上のTIA及び／又は別の信号処理ICと集積化されたMS-PD/APD用のフリップチップ配置の幾つかの側面を示している概略図である。該チップ及びマウント技術は図45-48に図示し且つそれらについて説明したものと同様であるか又は同一である。この例においては、ボールレンズ4922がビア4626内に位置されていて、オプティカルファイバー4624からの光を効率的にMS-PD/APD4520へ結合させる。ボールレンズ4922はMS-PD/APD4520に対しての該レンズのアライメントのためにビア4626内に位置することが可能である。

【0100】

図50は、幾つかのその他の実施例に基づいて、単一シリコンチップ上のTIA及び／又は別の信号処理ICと集積化されたMS-PD/APD用のフリップチップ配置の幾つかの側面を示している概略図である。該チップ及びマウント技術は図45-49に図示し且つそれらについて説明したものと同様であるか又は同一である。この例においては、ボールレンズ5022がビア4626内に位置しており、該ビアにおいてはシリコンの殆ど又は全てがエッチング除去されているので光は殆どが空中及び／又は流体、ゲル、ポリマー、固体等の屈折率整合物質内を走行する。更に、ビア4626は、オプティカルファイバー4626のボールレンズ5022に対しての且つ更にMS-PD/APD4520に対してのアライメントに対するガイド及び／又はストップとして作用する。

【0101】

図51は、幾つかの実施例に基づいて、単一シリコンチップ上のTIA及び／又は別の信号処理ICと集積化されているMS-PD/APDに対するフリップチップ配置の幾つかの側面を示している概略図である。該チップ及びマウント技術は図45-50に図示し且つそれらについて説明したものと同様であるが、MS-PD/APD5120及びTIA及び／又はその他の信号処理集積回路5130がシリコンチップ5110の上部表面上又はその近くにマウントされている点が異なる。金属性導体導管5132及び5134はAl, Cu, Mo, W, Ni, TiN等から構成することが可能である。導管5132はMS-PD/APD5120をICエレクトロニクス5130へ接続させている。導管5134はICエレクトロニクス5130を、半田バンプ等のバンプ技術を使用してPCB4550（又はチップ担体）へのトレースへ接続させており、そのことは、該チップのPCB及び／又はチップ担体への良好なアライメントを可能とさせる。幾つかの実施例によ

れば、ICエレクトロニクスをPCB上のトレース及び／又はチップ担体へ接続させるために、ワイヤボンディングを使用するその他の方法を使用することも可能である。ファイバー4524はMS-PD/APD5120の直ぐ近くに位置され、且つその構成は、ファイバー4524の先端部上のボールレンズ、及び／又はファイバーとMS-PD/APDとの間のボールレンズを包含することが可能である。図45-50に関して説明した如くに、グレーチング、フレネルレンズ等のその他の光をフォーカスさせる要素を使用することも可能である。幾つかの実施例によれば、上述したMS-PD/APD構造に示した如く埋込二酸化シリコン(BOX、埋込酸化物)等の屈折率の不連続が存在するか及び／又はハルク物質の屈折率に対しての該マイクロストラクチャの実効屈折率における変化が存在している場合には、エピタキシャル表面から照射する光(上部照射型)もMS-PD/APD5120内において光学信号の二重及び／又は多重のバウンス即ち跳ね返りを有する場合がある。MS-PD/APD内の光学信号の二重及び／又は多重のバウンスは、量子効率を著しく犠牲にすること無しに一層薄い吸収層及び短い走行時間を可能とさせ、それによりMS-PD/APDの一層高いデータレート動作を可能とさせる。光の二重又は多重のバウンスとは、MS-PD/APDのパスにおいて吸収されず且つ該MS-PD/APD構造から出る光のことを意味しており、これらの光子はMS-PD/APD構造に向けて反射されて戻される。複数の穴及び柱体からなるマイクロストラクチャ内において、光は共振及び／又は結合共振状態となる場合があり、そのことは向上された実効吸収係数及び／又は向上された実効吸収長とさせることが可能である。

【0102】

図52は、単一Siチップ上にTIA及び／又はその他の信号処理及びルーチングエレクトロニクス等のICエレクトロニクスと集積化された複数のMS-PD/APDからなるアレイを示している概略図である。アレイは、例えば、TIA及び／または信号処理、ルーチング、格納用のASIC等のICエレクトロニクスと集積化された2個乃至10個を超える数のMS-PD/APDを包含することが可能である。図示例においては、単一のSiチップ5210上にマウントされている4個のMS-PD/APD5220、5222、5224、5226が示されている。これらのMS-PD/APD5220、5222、5224、5226はICエレクトロニクス5230、5232、5234、5236へ夫々接続されている。しかしながら、幾つかの実施例によれば、複数のMS-PD/APDがSiチップ上の単一のICエレクトロニクス装置へ接続されているか、または複数のICエレクトロニクス装置が単一のMS-PD/APDへ接続されている。アレイ内の複数のMS-PD/APDは同一のものとすることが可能であり、例えば、マイクロストラクチャの穴直径及び周期は同一の波長、例えば850-870nm、に対して最適化される。その他の実施例によれば、アレイ内の各MS-PD/APDは周波数の異なる帯域に対して最適化させることが可能である。例えば、アレイ内に4個のMS-PD/APDが存在している場合、各MS-PD/APDの穴直径及び周期を最適化させることによって、該4個のMS-PD/APDは、夫々、850-870nm、875-895nm、900-920nm、920-950nm(又はその任意の組合せ)において最適化させることが可能である。例えば、Molin et al., 次世代WDMシステム用の850-950nm広帯域OM4マルチモードファイバー(850-950nm wideband OM4 multimode fiber for next generation WDM systems)、OFC(2015)、を参照すると良く、それを引用により本書に取り込む。1、5、10、16、20、25、28、32、40、56及びそれよりも大きなもの及びそれらの間の全ての範囲のデータレートは、光学的データリンク用の標準及びプロトコル及び適用例に依存して可能である。オプティカルファイバー5240、5242、5244、5246は別々のファイバーとすることが可能であり、又は並列ファイバーストリップとして設けることが可能である。オプティカルファイバー5240、5242、5244、5246は各々が単一帯域の波長及び／又は100Gb/s乃至1Tb/s又はそれ以上の総合データレートを与えるためにWDM及びCWDM用の複数帯域の波長を担持することが可能である。例えば、各々が100Gb/sである10個のファイバーチャンネルを有する10個のMS-PD/APDからなるアレイは1000Gb/s

／sの総合データレートを与える。各々が25～28Gb/sにある4個のファイバーチャンネルを有する4MS-PD/APDアレイは100Gb/sの総合データレートを与え、各々が56Gb/sにある2個のファイバーチャンネルを有する2MS-PD/APDアレイは100Gb/sの総合データレートを与える。各ファイバーチャンネルが複数の波長帯域、例えば850～870nm及び875～895nm、を担持することが可能であり且つ各波長帯域が25～28Gb/sにおいて送信することが可能である場合には、4ファイバーアレイは実効的に200Gb/sを超える総合データレートを有することが可能である。

【0103】

図53は、幾つかの実施例に基づく、高データレートMS-PD用のエピタキシャル構造を示している概略図である。図示した構造は10Gb/sよりも一層大きなものとする事が可能である。穴5322がSiO₂BOX層5304までエッチングするか、又は該穴をP層5306までエッチングして及び／又は、例えば、P層5306内へ部分的にエッチングさせることが可能である。ドーピング及び厚さは次の通りであり、即ち、Si基板5302は150μmの厚さであり、BOX層5304は2～4μmの厚さであり、P層5306は0.2～1μmの厚さであってドーピングは $1 \times 10^{18} / \text{cm}^3$ を超えており、I層5308は1.5～2μmの厚さであって意図的にはドーピングされておらず($5 \times 10^{18} / \text{cm}^3$ 未満)、且つN層5310は0.2～0.5μmの厚さであってドーピングは $1 \times 10^{18} / \text{cm}^3$ を超えるものである。N及びP層5310及び5308の高ドーピングは少数キャリア寿命を短縮させてPDの応答を遅くさせる場合がある抵抗電流を最小とさせる。幾つかの実施例によれば、 1×10^{19} 及び $1 \times 10^{20} / \text{cm}^3$ を超える程度の高いドーピングは、少数キャリア寿命がピコ秒程度であり且つ直列抵抗が減少されるように使用される。

【0104】

図54は、幾つかの実施例に基づく、高データレートMS-PD用のエピタキシャル構造を示している概略図である。この構造及びドーピングは図53に図示しかつそれについて説明したものと同様であるか又は同一であるが、穴5422がP層5306の上部まで及び／又はP層5306内へ丁度入りかけるまでエッチングされていることが異なっている。

【0105】

図55は、幾つかの実施例に基づく、高データレートMS-PD用のエピタキシャル構造を示している概略図である。この構造及びドーピングは図53及び54に図示し且つそれらについて説明したものと同様であるか又は同一であるが、穴5522がP層5306内の少なくとも中間までエッチングされている点が異なっている。

【0106】

図56は、幾つかの実施例に基づいて、MD-PDに対するメサ寸法、穴直径、穴周期距離、及び格子パターンを示している表である。これらの例においては、該格子は六角形又は正方形とすることが可能である。該穴は円形、楕円、多角形とすることが可能である。該穴は、2000nmの周期で1300nmの直径、2000nmの周期で1500nmの直径、1000nmの周期で700nmの直径、900nmの周期で630nmの直径である。動作波長は800～990nmで且つその物質はSiである。厚さが3～100nmの範囲の薄いバッジ層SiO₂を包含させることが可能である。該メサ寸法は、部分的にはMS-PD（ボンダパッド及びコンタクト金属を除く）の容量を決定し、該MS-PDのデータレートに依存して、5μm、10μm、20μm、25μm、30μm、40μm、50μm、及び80μmである。低容量及び短い走行時間は一層高いデータレートのMS-PDとさせる。

【0107】

図57(A)及び(B)は、幾つかの実施例に基づく、六角形及び正方形の格子穴パターンを示している概略図である。図57(A)は六角形格子パターンを示しており、且つ図57(B)は正方形パターンを示しており、「d」は各場合における周期である。幾つ

かの実施例によれば、これらのレイアウトは図56に示したMS-PDに対する例示的パラメータに対して使用される。

【0108】

図58は、幾つかの実施例に基づく、シリコンMS-PD用のエピタキシャル層構造を示している概略図である。この構造の厚さ及びドーピングは以下の通りであり、即ち、Si基板5802は150 μm であり、BOX（埋込酸化層）層5804は2-4 μm の厚さであり、SiP層5806は0.2-0.5 μm の厚さでドーピングは $2 \times 10^{20}/\text{cm}^3$ を超えており、SiI層5808は約1.5-2 μm の厚さで且つ意図的にはドーピングされておらず（ $5 \times 10^{16}/\text{cm}^3$ 未満のバックグラウンドドーピングを有している）、SiN層5810は約0.2 μm の厚さで且つ $2 \times 10^{20}/\text{cm}^3$ を超えてドーピングされている。該P及びN層の高ドーピングは、例えば、 $1 \times 10^{19}/\text{cm}^3$ を超えるものとするのが可能である。幾つかの実施例によれば、SiGeB、SiGeC、SiGeBC等の物質から構成されており厚さが5nm乃至50nmであるエッチストップ層を、マイクロストラクチャ型穴及び／又はメサのエッチング期間中に処理を助けるために、PSI5806とISI5808との間の界面に包含させることが可能である。高度にPドーピングされているSiGeBが使用される場合、構造はN-I-Pとすることが望ましい。P及びN領域の高ドーピングは、シート抵抗を減少させるに加えて、少数キャリア寿命も減少させ、従ってP及びN領域において吸収された光子は光電流に対しての寄与は最小とされる。P及びN領域における減少された少数キャリア寿命は光発生されたキャリアの高電界「I」領域への拡散を減少させ、尚該領域においては、少数キャリアはアノード及びカソードへ掃引されて光電流に寄与する。

【0109】

図59は、幾つかの実施例に基づく、MS-PDの或る側面を示している概略図である。厚さ及びドーピングを含むその物質構造は、図58に図示し且つそれについて説明したものと同様であるか又は同一である。図59の場合には、層5910及び5906におけるP及びNドーピングが交換されてP-I-N配置となっている。注意すべきことであるが、図58又は59のいずれかにおいて、その配置はP-I-N又はN-I-Pとすることが可能である。穴5922はSiO₂5804へエッチングされており、且つP及びNオーミックコンタクト5928及び5930が、夫々、P及びN層5910及び5906に対して形成されている。メサをエッチングして感光区域を画定し且つPIN構造の容量を画定している。メサ直径は、MS-PDが設計されている（図56に関して説明した如く）データレートに依存して10 μm 乃至80 μm の範囲である。20-40Gb/sの場合、該メサの直径は、典型的に、20-40 μm である。0.2 μm の厚さで $2 \times 10^{20}/\text{cm}^3$ を超えるドーピングP層5910は、約50 Ω 未満のシート抵抗を有することが可能である。0.2 μm の厚さで $2 \times 10^{20}/\text{cm}^3$ を超えるドーピングのN層5906は約35 Ω 未満のシート抵抗を与えることが可能である。該P及びN層の高ドーピングも、例えば、 $1 \times 10^{19}/\text{cm}^3$ とすることも可能である。一層薄いP及びN層は一層高い百分率の光学パワーが該「I」層内となり且つ該P及びN層内において一層低い百分率となることを可能とし、それによりMS-PDの量子効率を最大とさせる。説明の便宜上、パッシベーション、ポリイミドブリッジ、ボンドパッド及びその他の処理ステップは図示していない。逆バイアス電圧がP及びNコンタクト間に印加されて該「I」層内に高電界領域を形成する。電圧は、典型的に、約2-6Vの範囲である。図示した場合には、照射は上から垂直に又は垂直からずれた角度においてである。波長は800-990nmの範囲であるが、780nm等のその他の波長を使用することも可能である。公称波長は850nmであるが、810-830、830-850、850、880、930-960、960-990などの波長を包含することも可能である。

【0110】

図60は、幾つかの実施例に基づく、MS-PDの或る側面を示している概略図である。物質構造の厚さ及びドーピングを含む該MS-PDは図58及び60に図示し且つそれらについて説明したものと同様であるか又は同一である。この場合に、穴6022がN層

5906まで及び／又はその中にエッチングされているが、図59におけるようにSiO₂層5804までずーとエッチングされるものではない。従って、該N層における吸収は向上されておらず、その結果該「I」層における光学パワーの百分率を一層高いものとする場合がある。このことは該MS-PDの量子効率を改善する傾向となる。SiO₂層5804は必要な場合と必要ではない場合とがある。

【0111】

図61は、幾つかの実施例に基づく、MS-PDの或る側面を示している概略図である。該MS-PDは、物質構造の厚さ及びドーピングを包含して、図58-61に図示し且つそれらについて説明したものと同様であるか又は同一である。この場合に、該SiMS-PDは基板側から照射される（本書においては、背面照射型又は底部照射型とも呼称される）。ビア6170がエッチングされてシリコン基板を除去し、且つSiO₂層5804まで又は殆ど該SiO₂層まで又は該SiO₂層内へ又は該SiO₂層を貫通してエッチングされる。Si基板5802を除去して800-990nmの波長範囲における光学損失を最小とさせる。P層5910表面上に反射器6132を製造し、それは該反射器6132がPINダイオードを短絡させないようにポリイミド、固体二酸化炭素、又はスピン・オン・ガラス（SOC）等の充填プロセス（filler process）を包含することが可能である。注意すべきことであるが、反射器6132は正確に平面状であることは必要ではなく、穴を有する領域において凹状とさせることが可能であり、そのことは光波のトラップングを向上させる場合がある。反射器6132は誘電体、ブラッグ反射器、導電性透明金属酸化物、銀、金又はその任意の組合せ等の金属又は合金とすることが可能である。インジウム錫酸化物（ITO）を、ブラッグ反射器を形成するために非導電性誘電体と共に、使用することも可能である。金属及び／又は導電性酸化物は、更に、P層5910のシート抵抗を減少させることが可能であり、それにより寄生抵抗を減少させ且つMS-PDの変調型周波数応答（データレート）を改善させる。幾つかの実施例によれば、「I」層5808は反射器を具備する背面照射の場合に一層薄くさせることが可能である。何故ならば、光は量子効率を劣化させること無しに「I」層を介して少なくとも2回及び多分それ以上の回数走行することが可能であり、しかも同時にMS-PDの変調型周波数（データレート）応答を改善させるからである。その理由は、一層薄い「I」層の場合に、光発生されたキャリアの走行時間は一層短いからである。フォトダイオードの周波数応答は、その容量及び抵抗（RC時間）及び走行時間（transit time）によって決定される。例えば或る高データレートに対して100又はそれ以上のファクターより一層大きな高い向上された実効吸収長において光学的走行時間が重要となる場合がある。

【0112】

図62は、幾つかの実施例に基づく、MS-PD用のGe・オン・SiPINエピタキシャル層構造を示している。厚さとドーピングとを含む物質構造は、図58-62に図示し且つそれらに基づいて説明したものと同様であるか又は同一である。この場合には、 $2 \times 10^{19} / \text{cm}^3$ を超えるドーピングを有するNSi層6202は0.2-2 μm の厚さを有することが可能である。Ge「I」層6208も設けられており、それは意図的にはドーピングされておらず、ドーピングは $2 \times 10^{16} / \text{cm}^3$ 未満であり且つ厚さは0.5-2 μm である。ドーピングが $2 \times 10^{19} / \text{cm}^3$ を超える上部GeP層6210は0.1-0.2 μm の厚さで形成される。幾つかの実施例によれば、Si上のGeの良好な結晶成長を開始させるためにNSi層6206と「I」Ge層6208との間の界面において薄いGeバッファ層（不図示）を使用することが可能である。P及びNの高ドーピングも少数キャリア寿命を減少させ、それにより全体的な光電流に対して寄与する場合がある光電界「I」領域内へ捕引される場合がある光発生されたキャリアの拡散を最小とさせる。

【0113】

図63は、幾つかの実施例に基づく、Ge・オン・SiMS-PDを示している。物質構造の厚さとドーピングとを含んで、該MS-PDは図58-62に図示し且つそれらについて説明したものと同様であるか又は同一である。穴6322がSiO₂層5804ま

でエッチングされており、又は該穴はN S i層6208までエッチングさせることが可能であり、その場合には、S i O₂層5804は必要である場合と必要ではない場合とがあり、且つ該M S - P Dは上部即ち正面（エピタキシャル表面）から照射される。1100乃至1800 nmの波長範囲におけるフォトン吸収は該S i領域よりも殆どが該G e領域においてである。P G e層6210を薄く維持することによって、該フォトンの大きな百分率がG e「1」層6208において吸収され、それにより量子効率を増加させる。G eとS iとの間の高い屈折率差は、該穴をS i N層6206の上部までエッチングさせるに過ぎないことを必要とする場合がある。しかしながら、本例においては、穴6322はS i O₂層5804までエッチングされている。N S i層6206は、本例においては、最大で2 μ mの厚さとすることが可能であり、且つ50 Ω 未満のシート抵抗を与えるために $1 \times 10^{13} / \text{cm}^2$ の範囲のドーピングとすることが可能である。850 nm動作の場合、又は800-990 nmの範囲における波長の場合、薄いN S i層は該I G e領域において吸収されるフォトンの百分率を増加させることが可能である。ドーピングが $2 \times 10^{20} / \text{cm}^3$ を超える0.2 μ m厚さのN S i層は50 Ω 未満のシート抵抗を与え且つ少数キャリア寿命を減少させる。2 μ mの厚いN S i層も800-990 nm又は800-1800 nmの波長範囲に対して使用することが可能である。何故ならば、800-990 nmの範囲における波長に対しては、G eは2 μ mの長さにより該フォトンの90%を超えるものを吸収するからである。従って、該フォトンの5%未満が該N S i層に到達する。850 nmの波長において、1%未満が該N S i層へ到達し、且つ990 nmにおいては3%未満がそれに到達する。

【0114】

或る場合には、800-990 nmの波長範囲に対して、マイクロストラクチャ型穴は吸収を向上させるために支配的に使用することができない場合があり、率るG e層内に部分的に又は完全にエッチングされた穴での容量を減少させるために使用される場合がある。更に、穴が必要ではない場合があり且つバルクG eが使用される場合がある。幾つかの実施例によれば、マイクロストラクチャは反射を減少させるためにも使用することが可能である。

【0115】

図64は、幾つかの実施例に基づく、G e・オン・S i M S - P Dを示している。物質構造の厚さ及びドーピングを含んで、該M S - P Dは図58-63に図示し且つそれらについて説明したものと同様のものであるか又は同一のものである。この場合には、穴6422がS i層6206までエッチングされている。G eに対する屈折率は約4であり且つS iに対する屈折率は約3.45である。この屈折率における差異は該G e領域において十分に向上された吸収を与える場合がある。この場合に、S i O₂層5804は必要でない場合があり且つ該M S - P DはB O X層5804無しでS iウエハ上に成長させる場合がある。1100-1800 nmの波長範囲に対して、S iは許容可能に低い光学損失を有しており且つ該吸収の殆どは該G e領域においてのものである。上部照射型M S - P Dの場合、該P G e層は薄くさせることが可能であり、従って該フォトンのバルクは該I G e領域において吸収され、そのことは量子効率を増加させる。該P層のシート抵抗を更に減少させるためにP G e層6210に関連してI T O（インジウム錫酸化物）を使用する場合がある。

【0116】

図65は、幾つかの実施例に基づく、G e・オン・S i M S - P Dを示している。該M S - P Dは、物質構造の厚さ及びドーピングを含んで、図58-64に関して図示し且つそれらについて説明したものと同様であるか又は同一である。この場合には、該M S - P Dは背面即ち底部照射型である。この構造は0.2 μ mの薄いN S i層を使用して800-1800 nmの波長範囲に対して非常に良好である。800 nmにおける波長を有するフォトンの3%未満がN S i層6206において吸収される。更に、1 μ mのG eの単一パス即ち通過において、990 nmフォトンの85%を超えるものが吸収される。ダブルパス即ち二重通過においては、990 nmフォトンの95%を超えるものが吸収される。

GeIがNSI上に成長されている背面照射型MS-PDにおいては、該PGe層上の反射器6532と共に、該フォトン²の二重及び／又は多重の通過が一層薄い1吸収層6208を可能とさせ、そのことは光発生された電子及び正孔の走行時間を減少させる。40Gb/s又はそれ以上の一層高い帯域幅を有するフォトダイオードを得ることが可能である。穴6322はSiO₂層5804へエッチングさせることが可能であり、又はSi層6206へエッチングさせることが可能である（図64に示した如く）。マイクロストラクチャ型穴アレイの場合、向上された吸収は1100-1800nmの波長において発生することが可能である。例えば、1550nmにおいて、1μm厚さのバルクGeを介してのダブルパス即ち二重通過で、9%未満が吸収され、一方、該Ge層内にマイクロストラクチャ型穴がある場合には、30%より大きな吸収を達成することが可能であり、且つ、幾つかの場合においては、50%より大きな吸収を達成することが可能である。或る場合には、GeI層を具備するMS-PDにおける吸収は、1μm厚さのGeにおける二重通過に対して又は2μm厚さのGeMS-PDにおける単一通過に対して、1550nmにおいて70%より大きなものを達成することが可能である。

【0117】

該MS-PDは次の層を有することが可能であり、即ち、Ge（又はSiGe）P層6210は約0.1μmの厚さで $2 \times 10^{20} / \text{cm}^3$ を超えるものへドーピングさせることが可能であり、GeI（吸収層）6208は0.5-2.0μmの厚さで意図的にドーピングしないものとすることが可能であり（ $5 \times 10^{18} / \text{cm}^3$ 未満）、且つ、最後に、SiN層6206は0.2-0.5μmの厚さで $2 \times 10^{19} / \text{cm}^3$ を超えるものへドーピングさせることが可能である。更に、Si基板を除去するためのピアエッチング期間中、該SiO₂層は不変のままとさせるか、部分的にエッチングさせるか、又は該SiO₂を除去するために完全にエッチングさせることが可能である。

【0118】

図66は、幾つかの実施例に基づく、Ge・オン・SiPDを示している概略図である。該PDは、物質構造の厚さ及びドーピングを含めて、図58-65に図示し且つそれらについて説明したものと同様である。図66はフリップチップとして配置されたものを示しているが、該PGe層に起因して僅かに劣化するが正面照射型配置とすることも可能である。該PDは、マイクロストラクチャ型穴アレイが無い場合の図64に示したMS-PDと類似している。800-1300nmにおける動作のために図示した如きエピタキシャル構造を具備するGe・オン・Siフォトダイオードは、特に1300nm波長領域に対してのダブルバウンス即ち二重跳ね返しを利用しており尚且つ高いデータレート動作を維持している。該PDはSiGeBiCMOSと集積化させることが可能である。幾つかの実施例によれば、該SiO₂層が省略される。半田ハンパ技術で、該PDは、例えば図44-52に示した如く、その他の実施例に対して上述したと如くに、PCB上に直接マウントさせたフリップチップとさせることが可能である。幾つかの実施例によれば、該PDは次の層を有することが可能であり、即ち、約0.1μmの厚さで $2 \times 10^{20} / \text{cm}^3$ を超えてドーピングされているGe（又はSiGe）P層6210、0.5-2.0μmの厚さで意図的にはドーピングしていない（ $5 \times 10^{18} / \text{cm}^3$ 未満）GeI（吸収層）6208、及び最後に0.2-0.5μmの厚さで $2 \times 10^{19} / \text{cm}^3$ を超えてドーピングされているSiN層6206である。更に、Si基板を除去するためのピアエッチング期間中に、SiO₂層5804は不変のままとさせるか（図65に示した如く）、部分的にエッチングするか、又はSiO₂を除去するために完全にエッチング（図66に示した如く）させることが可能である。該SiO₂層が完全にエッチング除去される場合には、反射を最小とするために反射防止層（不図示）を該SiN層へ付与することが可能である。

【0119】

図67は、幾つかの実施例に基づく、Ge・オン・SiPDを示している概略図である。該PDは、物質構造の厚さ及びドーピングを含んで、図58-66に図示し且つそれらについて説明したものと同様である。この場合には、装置PIN接合容量を減少させるた

めにボイド6722が形成されている。ボイド6722は、或る量だけ容量を減少させるために十分な量の物質を除去するために、該Ge層内に部分的にエッチングさせることが可能である。該容量減少は、ボイドが無い同様のGe・オン・SiPDと同じデータレート帯域幅を維持しながら一層大きな面積のPDとすることを可能とする。その一層大きな面積のPDは、フォトダイオードに対するオプティカルファイバー及び／又は光源のミスマイメント即ち不整合において一層大きな公差を可能とさせる。データレート帯域幅はRC時間と走行時間とによって決定される。この構造の説明してきた全ての構造との統合は、半田バンプ技術と共にPCBへ直接取り付けることが可能なTIA等のエレクトロニクスで可能である。幾つかの実施例によれば、この構造に対する動作波長は800-1300nmの範囲であり且つデータレートは40Gb/sを超えるものである。

【0120】

注意すべきことであるが、BOX構造を使用することは必要ではない。本PDは次のような層を有することが可能であり、即ち、約0.1μmの厚さで $2 \times 10^{18} / \text{cm}^3$ を超えてドーピングされているGe層6210、0.5-1.0μmの厚さで意図的にはドーピングしていない($5 \times 10^{15} / \text{cm}^3$ 未満)Ge1(吸収層)6208、及び最後に0.2-0.5μmの厚さで $2 \times 10^{19} / \text{cm}^3$ を超えてドーピングされているSiN層6206、及び2-4μmの埋込酸化層6804である。

【0121】

図68は、幾つかの実施例に基づく、マイクロストラクチャ型アバランシェフォトダイオード(MS-APD)の或る側面を示している概略図である。該MS-APDは次の層を有することが可能であり、即ち、約0.1-0.2μmの厚さで $2 \times 10^{19} / \text{cm}^3$ を超えてPドーピングされているSiP層6810、0.5-2.0μmの厚さで意図的にはドーピングされていない($5 \times 10^{15} / \text{cm}^3$ 未満)SiI(吸収層)6808、0.2-0.5μmの厚さで $2 \times 10^{19} / \text{cm}^3$ を超えてnドーピングされているSiN層6806、及びSi基板6802上の2-4μmの厚さの埋込酸化層6804、である。該MS-APD装置は2つの付加的な層、即ち電荷層及び増倍層、を有している。電荷層6820は吸収層6808の直下である。SiP電荷層6820は約 $1.8 \times 10^{17} / \text{cm}^3$ へドーピングされており且つ約0.1μmの厚さを有している。該電荷層の直下は該MS-APDの増倍層6818である。SiI層6818は意図的にはドーピングされておらず($1 \times 10^{15} / \text{cm}^3$ 未満)且つ約0.5μmの厚さを有している。ビア6870がシリコン基板内を該SiO₂層までエッチングされており(反射を最小とさせるために反射防止コーティングを適用することが可能)、且つ800-990nmの範囲の波長を有する光が該ビアを介して適用される。該MS-APDの上部表面上の反射器6832は吸収層「I」層6808を介してのフォトン多重通過を与える。一つの利点は一層薄い吸収層であり、それは一層短い走行時間とさせる。従って、該MS-APDのデータレート帯域幅は向上される。マイクロストラクチャ型アレイ6822はSiO₂層6804まで及び／又は殆ど該SiO₂層までエッチングされる。P及びNコンタクト6828及び6830は半田バンプが付与されるべき同一の表面上に示されており、従って、該MS-APDはセラミックマルチチップ担体上及び／又はプリント回路基板上に直接フリップチップマウントさせることが可能である。説明の便宜上、最も基本的な処理ステップのみが示されている。パッシベーション、ボンドパッド、ポリイミド/スピンドット・オン・ガラス平坦化、反射防止コーティング、等の付加的なステップ又は要素は図示していない。更に、ビア6870のエッチング期間中、Si基板を除去した後に、該SiO₂層はMS-APD又はMS-PDのいずれかの構造のために部分的にエッチング除去するか又は完全にエッチング除去することが可能である。反射器6832が無い場合には、光学信号は上部表面から入射することも可能である。

【0122】

図69は、幾つかの実施例に基づく、マイクロストラクチャ型アバランシェフォトダイオード(MS-APD)の或る側面を示している概略図である。該MS-APDは、物質構造の厚さ及びドーピングを含んで、図68に図示し且つそれについて説明したものと同

様である。マイクロストラクチャ型穴アレイ6922は、該APD構造の電荷層6820、増倍層6818、及び／又はN層6806までエッチングされる。穴6922は該SiO₂層までずーとエッチングされるものではない。光が該SiO₂までシリコン基板が除去されているピア6970を介して照射される。光がNSi層6806上に直接入射するように該SiO₂層もエッチングすることが可能である。このことは全ての底部照射型MS-APD及びMS-A-PD装置に対して適用可能であり、その場合には反射防止コーティングを直接Siへ適用することが可能である。800〜990nmの範囲の波長の場合、約0.2μmの薄いNSi層6806が吸収層「1」層6808から離れた領域における吸収を減少させるために好適である。光は上部／正面から入射することも可能であり、その場合には反射器6832は除去される。このような場合には、ピアを省略する場合があります。且つ該Si「1」層は30%を超える量子効率のために1.5〜2μmへ増加させる場合がある。幾つかの場合においては、量子効率は50%を超えるものであり、幾つかの場合には、70%を超えるものであり、且つ幾つかの場合には、80%を超えるものである。該アバランシェの増倍係数即ち利得は2を超えるものとすることが可能である。幾つかの場合には、その利得は5を超えるものである。幾つかの場合には、それは10を超えるものである。更なる幾つかの場合には、それは15を超えるものであり、且つ更に幾つかの場合には、該利得は20を超えるものである。データレート帯域幅は10Gb/sを超えることが可能である。幾つかの場合には、該帯域幅は15Gb/sを超えるものであり、且つ幾つかの場合には、30Gb/sを超えるものである。更に、該SiO₂層は完全に又は部分的に除去することが可能であり、及び／又はそれはMS-APD及びMS-A-PDのためにSiで充填されているか又はされていないポイドを有することが可能であり、且つ背面／底部照射用に使用されるピアを形成するためのSi基板の除去期間中にSiGeB、SiGeC又はSiGeBC等のエッチストップ層を使用することが可能である。

【0123】

図70は、幾つかの実施例に基づき、該SiO₂層が無いMS-A-PDを示している概略図である。該MS-A-PDは、物質構造の厚さ及びドーピングを含んで、図68〜69に図示し且つそれらについて説明したものと同様である。エッチストップ層7034はSiGe又はSiGeC又はSiGeB（該SiGeは約1%のGeを有しており且つ $1 \times 10^{20} / \text{cm}^3$ を越えてボロンで高度にドーピングされている）で、且つ厚さは0.1乃至2μmの範囲である。SiGeBCはSi基板6802上、及び／又はNSi層6806等のSiエピタキシャル層上に成長させることが可能である。幾つかの実施例によれば、該MS-A-PDは次のような厚さ及びドーピングレベルを有しており、即ち、SiN層6806は0.2乃至1μmの範囲の厚さ及びドーピングレベルを有しており、SiN層6806は 0.2 乃至 $1 \mu\text{m}$ の範囲の厚さ及び $2 \times 10^{18} / \text{cm}^3$ を越えるものから $2 \times 10^{20} / \text{cm}^3$ を越えるものの範囲のドーピングを有しており、SiI増倍層6818は意図的にはドーピングされておらず（ $1 \times 10^{18} / \text{cm}^3$ 未満）且つ約0.5μmの厚さを有しており、SiP電荷層6820は約 $1.8 \times 10^{17} / \text{cm}^3$ にドーピングされており且つ約0.1μmの厚さを有しており、SiI吸収層6808は意図的にはドーピングされおらず（ $5 \times 10^{18} / \text{cm}^3$ 未満）且つ0.5〜1.0μmの厚さを有しており、且つSiPキャッピング層6810は $2 \times 10^{20} / \text{cm}^3$ を越えてドーピングされており且つ約0.1μmの厚さを有している。幾つかの実施例によれば、複数のエッチストップ層を使用することが可能である。例えば、SiI増倍層6818とSiN層6806との界面に別のエッチストップ層を形成することが可能である。該エッチストップ層の厚さは1nm乃至100nmの範囲に亘ることが可能であり、且つ隣接する層の電気的特性と一致させるためにP又はNへドーピングさせるか又は意図的にドーピングしないものとすることが可能である。光学信号の波長は800乃至990nmの範囲にわたることが可能であり且つ背面側から照射される場合には、SiO₂/Ag等の誘電体から反射器を形成することが可能である。幾つかの実施例によれば、反射器6832は、SiO₂とHfO₂、又はAg、Au及び／又はPtと共にITO等の屈折率が異なる2つの誘電

体からなるブラッグ反射器である。反射器6832は吸収されなかった信号フォトンを受
 取用Si1領域6808を介して二重及び／又は多重回通過させるべく反射させるために
 使用される。更に、該装置は正面照射型とすることが可能であり、その場合には反射器6
 832は省略され且つ吸収用Si1層6808は量子効率を最適化させるために1.5-
 2 μm へ厚くされる。幾つかの実施例によれば、該正面／上部照射型MS-APDにピア
 を包含させることも可能である。同様に、或るMS-PDは、該SiP電荷層及びSi1
 増倍層を省略して、この構造を使用することも可能である。正面及び背面照射型MS-P
 Dが有益である場合がある。何故ならば、Si基板の除去は屈折率コントラストを改善
 し且つ該マイクロストラクチャにおいて改善された吸収係数を有しており、そのことは
 量子効率を改善させるからである。

[0124]

該P及びN層の高ドーピングは、シート抵抗を減少させると共に該P及びN層内の少数
 キャリアの寿命を減少させて、MS-PD/APDのデータレート応答（周波数応答と
 も呼称される）において劣化を発生される場合がある高電界Si1吸収層内への少数キャ
 リアの拡散を減少させる。該マイクロストラクチャ型穴アレイは、該SiGeC及び／
 又はSiGeBストップ層まで及び／又は穴エッチング期間中及び／又はピアエッチング
 期間中のいずれかで該ストップ層を超えてエッチングさせることが可能である。該エッ
 チストップ層も該穴エッチングの後又は該ピアエッチング期間中に完全に又は部分的に除去
 することも可能である。この様に、SiGeC、SiGeBC又はSiGeB層は背面照
 射型MS-PD/APD用の光学系路中には無い。注意すべきことであるが、Geが約1
 %（例えば、Si_{0.99}Ge_{0.01}）であるSiGeBにおいては、そのバンドギャ
 ップはほぼSiのものと同じである。更に、図69における如く、該マイクロストラク
 チャ型穴アレイは、該吸収用Si1層に対応する深さへ及び／又は該Si1吸収層より大き
 く且つ部分的にアバランシェ領域内へ入る深さへエッチングさせることが可能である。

[0125]

図71は、幾つかの実施例に基づき、Ge・オン・Siマイクロストラクチャ型アバ
 ランシェフォトダイオード（MS-APD）を示している概略図である。該MS-APDは
 、物質構造の厚さ及びドーピングを含んで、図68-70に図示し且つそれらについて説
 明したものと同様である。Ge1吸収層7108は意図的にはドーピングされておらず（
 $5 \times 10^{13} / \text{cm}^2$ 未満）且つ0.5-2.0 μm の厚さを有している。上部GePキ
 ャッピング層7110は $2 \times 10^{19} / \text{cm}^3$ を超えてドーピングされており且つ約0.
 1 μm の厚さを有している。マイクロストラクチャ型穴アレイ7122は、SiP電荷層
 6820まで又は該SiP層直前までエッチングされている。代替的に、穴7122はS
 iP電荷層6820内へ及び／又はSi1増倍層6818内へエッチングさせることが可能
 である。ピア6970がエッチングされて光学経路からSi基板を除去している。該Si
 O₂層は不変のままとするか、部分的にエッチングさせるか又は完全に貫通してエッチン
 グさせることが可能であり、又はSiO₂の無いN₂Si基板を使用することが可能である
 。Si1N層6806が露出される場合には、反射を最小とさせるために反射防止層（不図
 示）を付与することが可能である。波長範囲は、例えば、800-1800 nm, 130
 0-1600 nm, 810-880 nm, 930-990 nmとすることが可能である。
 穴寸法及び周期は或る波長範囲に対して最適化させることが可能である。PGe又はSi
 Ge層7110上に反射器6832を形成することが可能である。該反射器6832は誘
 電体及び金属、ITO（インジウム錫酸化物又は同様の透明導電性酸化物）及び金属、ブ
 ラッグ反射器のような全誘電体、又はそれらの任意の組合せから構成することが可能であ
 る。反射器6832は、1回目の通過で吸収されなかったフォトンに2回又は多数回の通
 過のために吸収用Ge1層7108へ向かって反射させて戻す。単一通過でのフォトダイ
 オードと比較して一層薄いGe1吸収層7108を使用することが可能である。該一層薄
 いGe1層は一層短い走行時間とさせ、従って一層高いデータレートとさせる。Ge・オ
 ン・Siの成長はGeバッファ層を使用する場合があり、それはGeの高品質結晶成長を
 開始させるために成長される。例えば、Kang et al.の1.3 A E m光検知用のエピタキ

シャル的に成長されたGe/Siアバランシェフォトダイオード(Epitaxially-grown Ge/Si avalanche photodiodes for 1.3Eμ light detection)、Vol. 16, No. 13 / オプティクスエクスプレス(OPTICS EXPRESS) 9365 (2008) (以後、「Kang et al.」と呼称する)を参照すると良く、尚それを引用により本書に取り込む。1200-1750 nmの波長範囲の場合、Siはこれらの波長においては殆ど透明であるからビア7270は必要ではない。更に、反射器6832が無い場合には、光学信号は上部表面から入射することが可能であり且つGe「1」層7108は厚さを約2ミクロンへ増加させることが可能である。

【0126】

図72は、幾つかの実施例に基づく、Ge・オン・Siマイクロストラクチャ型アバランシェフォトダイオード(MS-APD)を示している概略図である。該MS-APDは、物質構造の厚さ及びドーピングを含んで、図68-71に図示し且つそれらについて説明したものと同様である。この場合には、マイクロストラクチャ穴アレイ7222がSiO₂層6804までエッチングされている。幾つかの実施例によれば、穴7222はSiO₂層6804の十分の数μm内までエッチングされ且つビア7270は該SiO₂層までエッチングされる。該SiO₂層は該ピアエッチング期間中に不変のままであるか、部分的にエッチングされるか、又は完全に貫通してエッチングさせることが可能である。背面側から入射する光は800-1800 nmの範囲の波長を有している。例えば630-780 nmなどのその他の波長を使用することも可能である。該Si層内において幾らかの光発生されたキャリアが存在する場合があるが、光発生されたキャリアのバルクはGe I層7108においてであり、とりわけ800-1800 nmの波長範囲においてであって、特に1100-1800 nmの波長範囲においてである。該エピタキシャル構造は図71に示したものに類似しており、というのも、該Ge P層上の反射器6832が光をGe I吸収層へ向けて反射して戻すからである。該SiO₂層の除去は該マイクロストラクチャ型半導体穴間に高い反射指数コントラストを可能とさせ、そのことは該マイクロストラクチャ型穴アレイと空気的光収集特性を改善させることを可能とする。又、SiO₂-空気界面及びSiO₂-半導体界面において発生する場合がある反射が取り除かれている。正面照射型MS-APDの場合、反射器6832は除去され且つGe I吸収層7108が1-2 μmの範囲へ厚くされる。該ピア及びSiO₂の除去は正面側照射型MS-APDのために行うことが可能である。該アバランシェ層、P電荷及びI増倍、を除去することによって、該MS-APDはMS-PDとなる。

【0127】

図73は、幾つかの実施例に基づく、エッチストップ層を具備するGe・オン・Siマイクロストラクチャ型アバランシェフォトダイオード(MS-APD)を示している概略図である。該MS-APDは、物質構造の厚さ及びドーピングを含んで、図68-72に図示し且つそれらについて説明したものと同様である。SiGe、SiGeC、SiGeB、SiGeBC等のエッチストップ層7334をSiウエハ上に成長させる。注意すべきことであるが、Si基板(ウエハ)6802は、既に、N Siエピタキシャル層、その後のAPD層、その他のバッファ層、スペーサ層、又はその他のエッチストップ層等の夫々の層(不図示)をその上に有している場合があり、それらは良好な結晶成長及び処理再現性を促進させるものである。基本的なAPD層は、厚さが0.2乃至0.5 μmの範囲でドーピングが $2 \times 10^{19} / \text{cm}^3$ をこえるものから $2 \times 10^{20} / \text{cm}^3$ を越えるものの範囲であるSiN層6806、意図的にはドーピングされておらず且つ厚さが約0.5 μmであるSi I増倍層6818、約 $1.8 \times 10^{17} / \text{cm}^3$ へドーピングされており且つ厚さが約0.1 μmであるSi P電荷層6820、意図的にはドーピングされておらず且つ厚さが0.5-1.0 μmであるGe I吸収層7108、及びドーピングが $2 \times 10^{20} / \text{cm}^3$ を越えており且つ厚さが約0.1 μmであるGe又はSiGe Pキャッピング層7110である。マイクロストラクチャ型穴アレイは特定の波長範囲に対して最適化されている穴直径及び周期でエッチングされている。特定の波長範囲は次のものを包含しており、即ち、800-860、860-880、880-920、920-990

、990-1100、1100-1350、1350-1450、1450-1550、1550-1650、1650-1800 nmである。穴及びメサのパッシベーションは説明の便宜上割愛してあるが、Kang et al.の中にそれらの例が示されている。文献においてはその他のパッシベーション方法が存在している。光はビア7370を介して背面側から入射し、その場合は該エッチストップ層を除去することが可能である。光は正面側から入射することも可能であるが、吸収Ge層7108の厚さは約1-2 μmの範囲に増加される。正面側照射型MS-APD/PDの場合、例えば、半導体マイクロストラクチャと空気との間の反射指数コントラストを増加させるために該ビアを実現させることも可能である。平坦化層、ブリッジ層、ボンダパッド、及び充填物等のその他の層も説明の便宜上図示していない。

【0128】

図74は、幾つかの実施例に基づく、Ge・オン・Siマイクロストラクチャ型アバランシェフォトダイオード(MS-APD)を示している概略図である。該MS-APDは、物質構造の厚さ及びドーピングを含んで、図68-73に図示し且つそれらについて説明したものと同様であるが、Pコンタクト層における光キャリアーの吸収を減少させるために該Ge層がSiGe又はSiGeCのP層7410で置換されている点が異なっている。SiGe及び/又はSiGeCはGeよりも一層大きなバンドギャップを有しており、従って同じ厚さの場合に吸収係数はGeにおける場合よりも一層小さい。例えば、Kolodzey et al.の「Si基板上に成長させたSiGeC合金の光学的及び電子的特性(Optical and electronic properties of SiGeC alloys grown on Si substrates)」、ジャーナルオブクリスタルグロース(Journal of Crystal Growth)157、386-391(1995)(以後「Kolodzey et al.」と呼称する)を参照すると良く、尚それを引用により本書に取り込む。例えば、Kolodzey et al.から、SiGe_{0.2}C_{0.1}の場合、バンドギャップは、Siが1.11 eVであり且つGeが0.66 eVであるのと比較して、1.3 eV(直接)である。SiGe合金はSiとGeとの間のバンドギャップを与え、従ってGeに対してのSiの何らかの付加はバンドギャップを増加させ且つ該P層における吸収を減少させる。幾つかの実施例によれば、このP層置換技術はここに示し且つ記載した全てのMS-PD/APD構造に対して適用される。特に、Ge層はSiGeP及び/又はSiGeCP層で置換される。幾つかの異なる実施例によれば、ここに示し且つ記載した全てのMS-PD/APDにおいて、該SiP及びN層も完全に又は部分的にSiGeC-P及びSiGeC-Nで置換させることが可能であり、そのことは該MS-PD/APDのP及びN領域における光学信号の吸収を減少させる。幾つかの場合には、本発明における光学フォトン吸収を減少させるために、Siである該APDの増倍領域もSiGeC-Iで置換させることが可能である。或る波長1200-1750 nmにおいては、Siは殆ど透明であり、ビア7370及びエッチストップ層7334のいずれか一方又は両方が必要ではない。この場合には、NSi基板を使用してその背面を研磨し且つ反射防止コーティングを行う。

【0129】

図75は、幾つかの実施例に基づく、MS-PD用の別のSiNIPエピタキシャル層構造を示している概略図である。穴7522が約2.3 μmの深さまでエッチングされており且つSiP層7506の前及び/又は後の十分の数ミクロンで終端することが可能である。ドーピング及び厚さはほぼ次の通りであり、即ち、SiP基板7502、 $1 \times 10^{19} / \text{cm}^3$ を越えるものとすることも可能であるが $2 \times 10^{20} / \text{cm}^3$ を越えるPドーピングで0.2 μm(又は0.1-1 μmの範囲)のSiP層7506、意図的にはドーピングされておらずバックグラウンドドーピングが $5 \times 10^{16} / \text{cm}^3$ 未満であり且つ幾つかの場合には $5 \times 10^{15} / \text{cm}^3$ 未満であって厚さが約2又は1-2.5 μmの範囲内であるSiI層7508、ドーピングが $2 \times 10^{19} / \text{cm}^3$ を越えており且つ厚さが約0.3 μm又は0.2-0.5 μmの範囲内であるNSi層7510である。Nコンタクト7528はSiN層7150上にある。Pコンタクトは、コンタクト7530における如くSiP基板の上部表面上とすることが可能であり、及び/又はコンタクト75

3.2における如く該基板の底部／背面側上とすることが可能である。P I N 接合区域、従って容量、を測定するためにメサエッチングが使用される。メサはP層7506まで及び／又はP基板7502までエッチングされ且つPコンタクト7530はS i P層7506上及び／又はS i P基板7502背面側7532上にデポジット即ち付着させることが可能である。幾つかの実施例によれば、その他の電気的分離を使用することも可能であり、例えば、P I N区域を測定するための陽子衝撃（proton bombardment）又はP N接合ドーピング又はトレンチドーピング等のその他のドーピング技術である。この構造において、光は約800-990 nmの範囲の波長で正面側から入射する。周期が2000 nmで穴直径が1300 nm、及び周期が2000 nmで穴直径が1500 nmを六角形及び／又は正方形格子パターンのいずれかで使用することが可能である。幾つかの実施例によれば、穴直径の範囲は約600 nm乃至1500 nmであり且つ周期の範囲は約900乃至2500 nmである。

【0130】

図76(A)-(C)は、幾つかの実施例に基づく、MS-PD用の埋込酸化物上のS i N-1-Pエピタキシャル層を示している各概略図である。図76(A)において、穴7622がS i P層7606へエッチングされており、該S i P層内へ部分的に及び／又はS i O₂層7604へエッチングされている。ドーピング及び厚さはほぼ次の通りであり、即ち、基板7602内のS i B O X（埋込酸化物）7604、Pドーピングが $2 \times 10^{19} / \text{cm}^3$ を超えている $1 \mu\text{m}$ （又は0.1- $1 \mu\text{m}$ の範囲）のS i P層7606、意図的にはドーピングしておらず且つバックグラウンドドーピングが $5 \times 10^{16} / \text{cm}^3$ 未満であり且つ幾つかの場合には $5 \times 10^{15} / \text{cm}^3$ 未満であって厚さが $2 \mu\text{m}$ 又は0.5-2.5 μm の範囲であるS i I層7608、及びドーピングが $2 \times 10^{18} / \text{cm}^3$ を超えており且つ厚さが例えば0.3 μm 又は0.2-0.5 μm の範囲であるN S i層7610である。N及びPコンタクト7628及び7630は正面側上とすることが可能であり、その場合に、PコンタクトはP層7606に対するメサエッチングの後に形成される。S i G e B又はS i G e C等のエッチストップ層をP層7606とI層7608との間の界面において使用することが可能である。光が背面側から入射し且つ光がI層7608を介して複数回の通過をすることが可能であるように上部表面S i N層7610上に反射器が配置される場合には、I層7608は薄くすることが可能であり、例えば0.5- $1 \mu\text{m}$ とすることが可能である。PとNとは交換可能であり、且つ該マイクロストラクチャ型フォトダイオード（MS-PD）は、例えば、P I Nとすることが可能である。S i G e Bがエッチストップ層として使用される場合には、該S i G e Bは高度にP型であり且つ該N I P構造が好適である。該エッチストップ層は、例えば、0.05乃至 $1 \mu\text{m}$ の厚さとすることが可能であり且つ該S i P層を全体的に又は部分的に置換させることが可能である。適切に装置又はエピタキシャル層を修正して、光は正面側から及び／又は背面側から入射することが可能である。波長範囲は約800-990 nmである。

【0131】

図76(B)においては、図76(A)におけるP S i層7606は、Pドーピングが $2 \times 10^{19} / \text{cm}^3$ を超えており且つ厚さが0.5 μm 又は0.2- $1 \mu\text{m}$ の範囲であるS i_{0.95}G e_{0.05}B層7616で置換されている。その他の全ての層は図76(A)における通りである。マイクロストラクチャ型穴7622がエッチングされ且つ該S i G e B層において停止するか及び／又は該S i G e B層を貫通して通過し且つ該S i O₂層において停止するか及び／又は該S i O₂層内に入ることが可能である。該S i O₂層において停止するか又は該S i O₂層内で停止するか又はそれを貫通するピア7670をエッチングすることが可能である。S i N層及びS i G e B P層の夫々の上にN及びPオーミックコンタクト7628及び7630が形成されている。光は上部表面（エピ表面）から及び／又は底部表面（基板表面）からのいずれかから入射することが可能であり、及び該I吸収層を介して複数回通過させるために誘電体スペーサ層と共に上部が又は底部のいずれかの上に反射器を配置させることが可能である。波長は800乃至1000 nmの範囲である。説明の便宜上図示していないものは、パッシベーション層、ポリイミド

ブリッジ層、メサ、ボンドメタル等のその他の要素である。

【0132】

図76(C)においては、約0.1 μm の厚さで且つドーピングが $1 \times 10^{19}/\text{cm}^3$ より大きいP Si層7626がSiO₂層7604上の第1層として付加されており、その上にPドーピングが $1 \times 10^{19}/\text{cm}^3$ より大きく且つ厚さが約0.3 μm のSi_{0.95}Ge_{0.05}B層7616が成長される。図76(A)及び(B)における如く、光はビアがエッチングされている上部及び／又は底部表面から入射することが可能である。N及びPオーミックコンタクトが該N及びP層の上に夫々配置されている。マイクロストラクチャ型穴アレイ7622がSiO₂層7604を貫通してエッチングされ及び／又はP層7626内に部分的にエッチングされる。光が底部から入射する場合には、ビア7670をシリコン基板7602内へ及びSiO₂層7604内へエッチングし、尚SiO₂層7604は部分的に又は完全にエッチングさせることが可能である。1-10ボルトの逆バイアス電圧を該P及びNコンタクトの間に印加させる。

【0133】

幾つかの適用例においては、光はMS-PD/APDの上部及び底部から同時的に入射することが可能である。該光は、同一の又は異なる波長、データレート、極性、及びコヒーレント光学通信用の振幅を有することが可能である。光が上部と底部の両方から入射することの利点はビームスプリッターを使用することの必要性が無く且つ光学パワー損失において3 dB節約することが可能であるということである。

【0134】

図77は、幾つかの実施例に基づく、SiNIPエピタキシャル層とP Si基板上のSiGeBエッチストップ層とを具備しているMS-PDを示している概略図である。エッチストップ層7716はSi_{0.95}Ge_{0.05}B又はSiGeにおいて約1% Geから構成することが可能であり、その場合に、そのバンドギャップは実質的にSiと同じであり且つBドーピングは $1 \times 10^{19}/\text{cm}^3$ を超えるものである。この高度のPドーピングはSiP層7706を部分的に又は全体的に置換させる場合がある。これらの層及び厚さは次の通りとすることが可能であり、即ち、SiP基板7702、厚さが0.1-2 μm のSiGeB層7716、Pドーピングが $2 \times 10^{19}/\text{cm}^3$ を超えている0.2 μm （又は0.1-1 μm の範囲）のSiP層7706、意図的にはドーピングされておらずバックグラウンドドーピングが $5 \times 10^{13}/\text{cm}^3$ であり且つ幾つかの場合には $5 \times 10^{15}/\text{cm}^3$ 未満であって厚さが2 μm 又は0.5-2.5 μm の範囲内であるSiI層7708、及びドーピングが $2 \times 10^{18}/\text{cm}^3$ を超えており且つ厚さが0.3 μm 又は0.2-0.5 μm の範囲内であるNSi層7710である。N及びPコンタクト7728及び7730は両方共正面側とすることが可能である。該Pコンタクトは、又、コンタクト7732におけるように該P Siの背面側上とすることも可能である。マイクロストラクチャ型穴アレイ7722はSiGeBのエッチストップ層7716へエッチングさせることが可能である。該SiP内へ及び／又は該SiGeB層へメサをエッチングさせて該NIP区域、従ってNIP容量を画定する。Pコンタクト7730はP Si層7706又はP SiGeB層7716の上に配置させることが可能である。Nコンタクト7728がSiN層7710上に配置される。該Si基板を除去するために、該Si及びSiGeBに対するものとは異なるエッチングプロセスを使用して、該SiGeB層まで及び／又は部分的に該SiGeB層内へビア7770をエッチングさせることが可能である。SiGeB層7716もエッチング除去することが可能であり、その場合には、ビア7770はSiP層7706まで延在される。更に、SiP層7706は部分的に又は全体的に該SiGeB層で置換させることが可能である。そのような場合には、少なくとも0.2乃至0.3 μm のSiGeB層が残存することが望ましい。光は正面及び／又は背面側から入射することが可能である。誘電体が半導体と接触しており厚さが0.5-4 μm の誘電体金属反射器を設けることが可能であり、その場合に、該誘電体はSiO₂、ポリイミド、SiO₂、フッ化カルシウム、又は窒化シリコンとすることが可能であり、それに続いて、正面が又は背面側のいずれかの上にAg、Au、Al、Ni等の金属又は合金

を設ける。例えば、該誘電体金属反射器が背面側に配置される場合には、正面側からの光を該吸収用層を介して多数回反射させることが可能であり、且つ逆に、該反射器が正面側に配置される場合には、背面側からの光は該吸収用層を介して多数回反射させることが可能である。反射器がある場合には、一層薄い層を使用することが可能であり、それは、例えば、 $1\text{ }\mu\text{m}$ であるか又は反射器が無いMS-PDの厚さの約半分であって、そのことは該MS-PDに対して一層高いデータレートとさせることが可能である。該MS-PDの場合に $800\text{--}990\text{ nm}$ の波長範囲を使用することが可能である。幾つかの場合において、該反射器は、単純に、ブラッグミラー等の金属とすることが可能である。更に、光が正面の表面からのみ入射するものであって2回及び／又は多数回の反射が実現されない場合には、ビア7770は必要ではない場合がある。

【0135】

図78は、幾つかの実施例に基づく、MS-PD用のSiGeBエピタキシャル層上のGe・オン・SiNIPを示している概略図である。マイクロストラクチャ型穴アレイ7822がGe層7810及び7808において且つSiP層7806内へ又はそこまでエッチングされている。エッチストップ層7816はSi_{0.99}Ge_{0.01}B又は約1%のGeのSiGeから構成されており、その場合にバンドギャップはSiと実質的に同じであり且つドーピングは $1\times 10^{18}/\text{cm}^3$ は越えている。この高度のドーピングはSiP層7806を部分的に又は全体的に置換させる場合がある。これらの層及び厚さは次の通りとすることが可能であり、即ち、SiP基板7802、SiGeB層7816は $0.1\text{--}2\text{ }\mu\text{m}$ の厚さであり、SiP層7806は $0.2\text{ }\mu\text{m}$ （又は $0.1\text{--}1\text{ }\mu\text{m}$ の範囲）でありドーピングは $1\times 10^{18}/\text{cm}^3$ であり、Ge層7808は意図的にドーピングされておらずバックグラウンドドーピングが $5\times 10^{18}/\text{cm}^3$ 未満であって且つ幾つかの場合においては $5\times 10^{18}/\text{cm}^3$ 未満であり厚さが $2\text{ }\mu\text{m}$ 又は $0.5\text{--}2.5\text{ }\mu\text{m}$ の範囲であり、且つNGe層7810はドーピングが $2\times 10^{18}/\text{cm}^3$ を越えるものであって厚さが $0.2\text{ }\mu\text{m}$ 又は $0.2\text{--}0.5\text{ }\mu\text{m}$ の範囲内である。N及びPコンタクト7828及び7830の両方を正面側とすることが可能である。該Pコンタクトは、コンタクト7832における如く、PSi基板の背面側とすることも可能である。数nmのGeバッファ層をSi層とGe層との間に成長させることが可能であり、且つその場合のGeバッファ層の成長条件は該Ge層の成長条件とは異なっている。ビア7870をSi基板7802内にエッチングして該SiをSiGeB層7816まで除去することが可能である。異なるエッチ条件で、SiGeB層7816を部分的に及び／又は全体的にエッチングすることが可能である。光は正面側又は背面側のいずれかから入射することが可能であり、反射器がある場合には、光子は吸収層を介して複数回の通過を行い且つ本装置は一層高いデータレート動作のために一層薄い層を使用することが可能である。何故ならば、電子及び正孔の光発生されたキャリアの走行時間は一層短いからである。波長範囲は 800 乃至 1800 nm である。穴直径及びアレイ周期は約 $30\text{--}100\text{ nm}$ に亘る或る波長範囲に対して最適化させることが可能である。光学信号が正面／上部表面から入射する場合にはビア7870は必要ではない場合がある。更に、光学信号が $1200\text{--}1750$ の範囲内の波長を有している場合には、これらの波長においてシリコンは殆どトランスパレント即ち透明であるか又は発生する光学損失は非常に低いので底部照射の場合にはビアが必要ではない場合がある。

【0136】

図79は、幾つかの実施例に基づく、MS-PD用のGe・オン・Siエピタキシャル構造を示している概略図である。その物質構造は次の通りであり、即ち、SiN基板7902（又は代替的にPSi基板のNIP構造）、Nドーピングが $2\times 10^{18}/\text{cm}^3$ を越えている $0.2\text{ }\mu\text{m}$ （又は $0.1\text{--}1\text{ }\mu\text{m}$ の範囲）のSiN層7906、意図的にはドーピングされておらずバックグラウンドドーピングが $5\times 10^{18}/\text{cm}^3$ 未満であり且つ幾つかの場合には $5\times 10^{18}/\text{cm}^3$ 未満であって厚さが $2\text{ }\mu\text{m}$ 又は厚さ範囲が $0.5\text{--}2.5\text{ }\mu\text{m}$ であるGe層7908、及びドーピングが $2\times 10^{18}/\text{cm}^3$ であり且つ厚さが $0.2\text{ }\mu\text{m}$ 又は $0.2\text{--}0.5\text{ }\mu\text{m}$ の範囲内であるPGe層7910である。

P及びNコンタクト7928及び7930は両方共正面側とすることが可能である。マイクロストラクチャ型穴アレィ7922をNSi層7906までエッチングするか、部分的にその中へエッチングするか、又はそれを貫通してエッチングする。メサエッチングがP1N区域及び容量を画定する。Nコンタクト7930及び7932を該NSi基板の正面側表面上又は背面側表面上のいずれかに該メサエッチングの後に付着させる。パッシベーションは図示されていないが、Kang et al. を使用して、非晶質Siを露出されたGe表面の側壁上に付着させることが可能であり且つ高温でアニールさせることが可能であり、及び／又はSiGeを露出されたGeの側壁上に付着させ且つアニールして漏洩電流を減少させることが可能である。該MS-PD及びMS-APDにおけるメサ直径は、データレートに依存して、 $5\mu\text{m}$ 乃至 $100\mu\text{m}$ の範囲とすることが可能である。幾つかの実施例によれば、該メサ直径範囲は 30Gb/s のデータレートの場合に $20\text{--}40\mu\text{m}$ である。更に、高結晶品質を確保するために、NSi7906とIGe7908との間にバッファGe層を使用することが可能である。例えば、Kang et al. を参照すると良い。正面側から光が入射する場合には、波長は $800\text{--}1800\text{nm}$ の範囲とすることが可能である。好適な範囲においては、該波長は $1450\text{--}1600\text{nm}$ とすることが可能であり、且つ別の好適な範囲においては、例えば、 $1250\text{--}1600\text{nm}$ とすることが可能である。該MS-PD/APDはデータ通信波長及び遠隔通信波長の両方をカバーすることが可能である。

【0137】

図80は、幾つかの実施例に基づく、別のGe・オン・Siエピタキシャル構造を示している概略図である。該MS-PDは、その物質構造の厚さ及びドーピングを含んで、図79に図示し且つそれについて説明したものと同様又は同一であるが、それは 0.2 乃至 $4\mu\text{m}$ の厚さの埋込酸化物層8004を具備するSiBOXウエハ上に成長されることが異なっている。マイクロストラクチャ型穴アレィ8022をNSi層7906までエッチングし且つNSi層7906内へ又はそれまで又はSiO₂層8004までエッチングさせることが可能である。メサエッチングがP1N容量を画定し且つ該MS-PD/MS-APD用のメサ直径は該MS-PD/APDのデータレート帯域幅に依存して $5\text{--}100\mu\text{m}$ の範囲である。 $20\text{--}50\mu\text{m}$ のメサ直径が $20\text{--}35\text{Gb/s}$ のデータレート帯域幅に対して好適である。光は前部表面又は後部表面から入射することが可能である。 1100nm を越える波長において、Siの光学損失は非常に低く且つ該Si基板は、例えば、レンズ又はグレーチングをエッチングするために使用することが可能である。SiO₂を全体的に又は部分的に除去するためにピア8070をエッチングすることが可能である。ピア8070は、光及び／又はファイバーを、例えば、該MS-PDへ案内するために使用することが可能である。ピア8070内に反射器8070を付着させることが可能であり、その場合に、正面側からの光が該反射器で跳ね返り且つIGe吸収領域7908を複数回横断するように該SiO₂は完全には除去しないか又は全く除去することはない。反射器が正面側か又は背面側のいずれかにある場合、IGe7908は一層薄く、例えば $1\mu\text{m}$ とすることが可能であり、そのことは電子正孔走行時間を減少させ且つ該MS-PD/MS-APDのデータレート帯域幅を増加させる。波長は $800\text{--}1800\text{nm}$ の範囲とすることが可能であり、それはデータ通信及び遠隔通信波長範囲の両方をカバーしている。連続的なNSi層7906の場合、例えば該SiO₂層が完全にエッチングされている場合には、該NSiの底部表面へ反射防止コーティングを付与することが可能である。

【0138】

図81は、幾つかの実施例に基づく、Ge・オン・Siエピタキシャル構造を示している概略図である。該MS-PDは、その物質構造の厚さ及びドーピングを含んで、図79-80に図示し且つそれらについて説明したものと同様であるか又は同一であるが、ピア8170がSiO₂BOX層8004へエッチングされており且つ $2\text{--}4\mu\text{m}$ の厚さ又は $0.2\text{--}6\mu\text{m}$ の範囲の該SiO₂を部分的にエッチングするか、完全にエッチングするか、又はエッチングしないものとすることが可能であることが異なっている。更に、Ag

、Au、Cr、Al等の物質からなる反射器8172を形成することが可能である。該反射器8172は、又、ブロードバンド、ナローバンド、又はバズバンドブラッグ反射器とすることが可能である。注意すべきことであるが、反射器8172が誘電体である場合には、それは、該SiO₂層をエッチング除去して、NSi層7906上に直接的に付着させることも可能である。IGe層7908を介しての1回目の通過で吸収されなかった正面側から入射する光は、該IGe吸収層を介して複数回通過するために該IGe層へ反射して戻ることが可能である。該IGe層は一層薄く、例えば1μm、することが可能であり、そのことは該IGe層においての電子及び正孔に対する走行時間を一層短いものとさせる。このことは該MS-PD/MS-APDのデータレート帯域幅を増加させる。

【0139】

図82A-82Cは、図79に図示した構造に類似したGe・オン・Siマイクロストラクチャ型フォトダイオードに関しての有限差分時間領域(FDTD)を使用してのシミュレーションに関するものである。図82Aは、シミュレーションを行ったGe・オン・Siマイクロストラクチャ型フォトダイオードを示している概略図である。その穴パターンは正方形格子パターンである。穴周期と穴直径との2つの組合せについてシミュレーションを行っており、即ち2500nmの穴周期と1500nmの直径、及び2300nmの穴周期と1300nmの直径である。図82B及び82Cにおいて、水平軸はμmでの波長であり且つ垂直軸は吸収であってそれは量子効率に直接的に関係している。各場合において、穴の正方形格子パターンをシミュレーションしている。図82Bにおいて、800nm乃至1000nmの範囲の波長を有する光学信号に対して、曲線8210は2300nmの穴周期及び1300nmの直径に対しての吸収のプロットであり、且つ曲線8212は2500nmの穴周期及び1500nmの直径に対しての吸収のプロットである。図82Cにおいて、1000nm乃至1800nmの範囲の波長を有する光学信号に対して、曲線8220は2300nmの穴周期及び1300nmの直径に対しての吸収のプロットであり且つ曲線8222は2500nmの穴周期及び1500nmの直径に対しての吸収のプロットである。0.8乃至0.98μmの波長範囲に対して0.4(フォトンの40%を吸収)を超えるものから高々0.9(フォトンの90%を吸収)を超えるものまでの吸収が判別された。0.5より大きな吸収は1.55μmに対して見られ且つGeの約2μmの吸収層に対して1.8μmへ延在している。これはマイクロストラクチャの無い2μm厚さの同等のGe層よりも著しく一層大きく、特に1550nm及びそれより一層長い波長においてそうである。

【0140】

図83A-83Cは、図80における構造に類似したGe・オン・Siマイクロストラクチャ型フォトダイオードに関して有限差分時間領域(FDTD)を使用したシミュレーションに関するものである。図83Aは、上部表面から入射する光でシミュレーションを行ったGe・オン・Siマイクロストラクチャ型フォトダイオードを示している概略図である。図83B及び83Cのグラフにおいて、水平軸はμmでの波長であり且つ垂直軸は吸収であって、それは2500nmの周期及び1500nmの直径(曲線8312及び8322)と2300nmの周期及び1300nmの直径(曲線8310及び8322)を有する複数の穴の正方形格子に対する量子効率に直接的に関係している。0.7より大きな吸収(フォトンの70%を吸収)が1.55μmに対して見られ且つGeの約2μmの吸収層に対して0.5吸収(フォトンの50%を吸収)よりも良い状態で1.8μmへ延在している。このことは、例えば、1550nm及びそれより長い波長において2μm厚さを有するInPと格子整合された同等のInGaAs層よりも著しく一層大きい。

【0141】

図84A及び84Bは、Ge・オン・Siマイクロストラクチャ型フォトダイオードに関して有限差分時間領域(FDTD)を使用したシミュレーションの結果を示している。シミュレーションした構造は図82Aに示されている。図84A及び84Bにおいて、グラフの水平軸はμm単位での波長であり且つ垂直軸は吸収であって、それは該穴アレイに対しての正方形及び六角形の両方の格子に対する量子効率に直接関係している。図84A

は、2300 nmの周期及び1300 nmの穴直径を有する正方形格子（曲線8410）及び六角形格子（曲線8412）の両方を示している。0.9（フォトンの90%を吸収）より大きな吸収が、50 nm波長スパンにわたって吸収が10%未満だけ変化している領域と共に1.55 μm 波長に対して示されている。図84Bは、2500 nmの周期で1500 nmの直径に対しての正方形（曲線8420）及び六角形（曲線8422）の格子の両方を示しており、それは1.55 μm において0.7の吸収を示している。全体的に、六角形格子は正方形格子よりも一層良好なフォトン吸収を示している。或る波長範囲においての吸収を改良又は最適化させるために周期及び穴直径、穴形状及び格子のその他の組合せを使用することが可能である。

【0142】

図85は、幾つかの実施例に基づく、縮尺通りではないが、マイクロストラクチャ型フォトダイオードチップの概略平面図を示している。チップ8560の近似的な寸法は350 μm ×300 μm ×150 μm である。メサエッジ8562によって画定されるメサは30 μm の直径を有している。該メサはNIP又はPIN接合容量を画定する。該メサの上部には上部表面8510が見えており（例えば、NIPMS-PD/APDを取るN層）、マイクロストラクチャ型穴8522も見えている。該メサの外側エッジ近くにはNオーミックコンタクトリング8528（NIPMS-PDを取る）がある。該メサの外側にはPオーミックコンタクトリング8530がある。Nボンドパッド8580がブリッジ相互接続8582によってNオーミックコンタクト8528へ電気的に接続されている。同様に、Pボンドパッド8590が相互接続8592によってPオーミックコンタクトへ接続されている。幾つかの実施例によれば、ブリッジ相互接続8582と区域8506（P層表面である場合がある）との間の不所望の短絡は、それらの間に付着されたポリイミド等の絶縁体を使用して防止されている。注意すべきことであるが、上述した説明は、N及びP層及びコンタクトが逆にされる場合に、PIN配置型MS-PD/APDに対しても適用可能である。

【0143】

幾つかの実施例によれば、BOXSiウエハ上のNIPMS-PD構造の基本的な製造ステップの簡単な処理フローは、（1）マスクし且つSiO₂層への穴アレイ8522をエッチングし、（2）マスクし且つN層8510上にNオーミックコンタクト金属リング8528を付着させ、（3）マスクし且つ接合容量を画定するメサをエッチングし、P層8506へエッチングし、（4）マスクし且つSiO₂へPメサをエッチングし、（5）マスクし且つP層8506上にPオーミックコンタクト金属8530を付着させ、（6）ボンドパッド8580によってNオーミックリング8528へのコンタクト用のポリイミドブリッジをマスクし、（7）マスクし且つ夫々Pオーミック及びNオーミックの両方に対してのボンドパッド8590及び8580を付着させる、ことからなる場合がある。接合及びボンドパッド容量は並列であり、従って、加法型であるので、該ボンドパッドは約100×100 μm^2 でNオーミックリング8528とコンタクトしている。RC時定数は全接合、パッド、ブリッジ容量によって決定される。上記したプロセスから削除したものは、パッシベーション、アニール、キュア、反射防止、薄層化（thinning）、背面側メタリゼーション、ダイシング等である。NIP/PINメサ直径は10乃至100 μm の範囲とすることが可能であり、MS-PD/APDは従来のPD/APDと比較してメサにおける半導体物質はより少ないので、容量はより少なく、従って従来のPD/APDと比較して同じデータレート帯域幅に対して一層大きな面積のメサ（又は等価的に一層大きな感光性面積）を有することが可能であり、従ってMS-PD/APD内への光学信号のアライメントは一層大きな誤差余裕を有しており、そのことはパッケージングにおいて一層コストを低下させることとなる。図56及び図57から、正方形穴格子で2000 nmの周期及び1300 nmの直径の穴の場合、その容量は、穴が無いが同じ直径のメサで1層の厚さで、ブリッジ容量を無視した場合の同等の構造のものよりも約30%一層少ない。周期が2000 nmで穴直径が1300 nmである六角形格子穴の場合、該MS-PDの面積は穴が無いPDの場合よりも約35%一層大きい場合がある。その他の格子、周期

、及び穴直径、吸収向上のためではないが容量減少のための穴、は容量を減少させるため、及び／又は、例えば、MS-PD/APD構造における吸収を増加させるか又は最適化させるために使用することも可能である。幾つかの実施例によれば、複数の周期及び／又は複数の穴直径を使用することも可能である。更に、非周期的に離隔させた穴を使用することも可能である。

【0144】

図86は、単一チップ上に相互インピーダンス増幅器及び／又はその他のエレクトロニクスと共に集積化させたMS-PD/APDを示している概略平面図である。単一シリコンチップ8600上に、MS-PD/APD8660が相互接続線8692を使用してTIA又はその他のエレクトロニクス8690へ接続して示されている。図85は、更なる信号処理及び送信のために電気信号を他の電子部品へ送信するためにボンドパッドを必要とするスタンドアロンMS-PD/APDを示しているが、図86は、単一チップに集積化されたMS-PD/APD及びエレクトロニクスを示している。ボンドパッドは不所望の容量を付加し、且つこの容量は、接合容量と共に、MS-PDのデータレート帯域幅を計算するために使用される。例えば、20GHz（又は約30Gb/s）の帯域幅を有するRC時間は約0.16pFの容量と50Ωの負荷抵抗とである。2μm層を有する30μm直径のSiPINPDは、I層が逆バイアス電圧によって完全に空乏化された状態で37フェムトファラッド（fF）の接合容量を有している。このことは、2μmのポリイミドの上に90μm×90μmのボンドパッドを可能とさせて約0.2pFの全容量を与える。該MS-PD/APDをTIA及び／又はエレクトロニクスと集積化させるとすると、ボンドパッドは最早使用されることは無く且つ該MS-PD/APDから該TIA及び／又はエレクトロニクスへの送信線の容量を無視すると、該MS-PD/APD容量は0.16pFとなることが可能であり、そのことは、MS-PDの場合、スタンドアロン装置に対する直径において30μmであるのと比較して、直径において約60μmの装置となる。この面積における増加は、MS-PD/APDに対する光学ビームのアライメント誤差における余裕を一層大きなものとさせ且つパッケージングにおけるコストを一層低下させることとなる。寄生容量を含むと、MS-PDの直径はスタンドアロンMS-PDの30μmよりも著しく一層大きく、且つ、例えば、40μmよりも大きい場合があり、且つ幾つかの場合においては、直径において50μmよりも一層大きい場合がある。

【0145】

注意すべきことであるが、本特許明細書に記載されるように、光の波長とほぼ同じ（多かれ少なかれ）直径を有するマイクロストラクチャ型穴アレイ（又は柱体）は、マイクロストラクチャ型穴アレイ（又は柱体）を有することの無い同様の物質のものよりも、フォトンの吸収を向上させる。例えば、SiPINPDが数十Gb/sで動作するためには、I層の厚さは必ず約2μmの程度でなければならない。そうでない場合には、光発生されたキャリアである電子及び正孔の走行時間が数十Gb/sのデータレート帯域幅を達成し且つ850nm、或る場合には880nm、そして或る場合には980nmの公称波長において約20%を超える、幾つかの場合には40%を超える十分な量子効率を有するためには長過ぎるものとなる。このことは、単一の周期及び直径で、及び／又は複数の周期及び直径でのいずれかによって、マイクロストラクチャ型穴アレイ（又は柱体）を使用する本書に記載した技術で可能とされる。該穴及び／又は複数の穴（柱体及び／又は複数の柱体）は周期的及び／又は非周期的なものとするのが可能であり、且つ該マイクロストラクチャが吸収及び／又はエミッション（emission）を向上させるためには円形以外の断面形状を有することが可能である。該マイクロストラクチャ型穴アレイ（又は柱体）が存在しない場合には、該2μm又はそれ未満の厚さのSi層は900nmフォトンの約5%を吸収し、一方、マイクロストラクチャ型穴アレイ又は柱体が存在する場合には、20%を超えて吸収させることが可能であり、幾つかの場合においては、30%を超えるものである。更に幾つかのその他の場合においては、900nm波長のフォトンにおいて40%、50%、及び80%を超えることが可能である。

【0146】

このことはGe・オン・Siの場合でも同じであり、この特許明細書を使用することによって、例えば、1550 nm、且つ幾つかの場合においては1600 nm及び幾つかの場合においては1700～1800 nmの波長において数十Gb/sデータレート帯域幅を達成することが可能である。

【0147】

既知のナノワイヤーフोटダイオードにおいては、数十Gb/sの高データレート帯域幅に対する約2 μm又はそれ未満の薄い層が同等のバルク層のものを越えるというような吸収の向上は存在しない。例えば、バンドギャップよりも大きな波長における2 μm長さの1 n Pナノワイヤーと2 μmバルク1 n Pとはほぼ同等であり、1 n Pナノワイヤーの利点は反射を減少させることのみにある。

【0148】

図87は、何らマイクロストラクチャが存在しない単純なエピタキシャル構造を示している。図87の構造は、800～880 nmの波長範囲を有する入射光子の吸収に関して、穴アレイ等のマイクロストラクチャを有する同様のエピタキシャル構造と比較するために使用される。FDTD（有限差分時間領域）を使用するシミュレーション目的のために、P及びNコンタクト、メサエッチング、パッシベーション、平坦化、及び完全なフोटダイオードを製造するためのその他のプロセス無しで、マイクロストラクチャを有する構造と有さない構造のみが示される。ケース1におけるエピタキシャル構造は、ドーピングされており且つ約150 μmへ薄膜化されたシリコン基板P8702上に成長され、その第1層は約0.2 μmの厚さでボロンを使用して $1 \times 10^{19} / \text{cm}^3$ を越えてドーピングされているSiP層8706であり、次いで約2 μmの厚さで意図的にはドーピングされておらず且つドーピングレベルが $5 \times 10^{15} / \text{cm}^3$ 未満であるSiイントリンシック層8708であり、次いで約0.3 μmの厚さで燻ドーパントでのドーピングが $1 \times 10^{19} / \text{cm}^3$ を越えているSiN層8710である。

【0149】

図88は、何らマイクロストラクチャが存在しない別の単純なエピタキシャル構造を示している。図88の構造は、800～880 nmの波長範囲での入射光子の吸収に関して穴アレイ等のマイクロストラクチャを有する同様のエピタキシャル構造と比較するために使用する。FDTD（有限差分時間領域）を使用するシミュレーション目的のために、P及びNコンタクト、メサエッチング、パッシベーション、平坦化、及び完全なフोटダイオードを製造するためのその他のプロセス無しで、マイクロストラクチャを有する構造と有さない構造のみが示される。ケース2におけるエピタキシャル構造は、2 μmの埋込酸化物（BOX）層8804を具備するシリコン基板8802上に成長され、該BOX層上には約0.1 μmの厚さでボロンを使用したドーピングが $1 \times 10^{19} / \text{cm}^3$ を越えているSiP層8806であり、次いでPドーピングが $1 \times 10^{19} / \text{cm}^3$ を越えているSiGeB（Si_{0.95}Ge_{0.05}B_{0.01}）層8816であり、次いで約2 μmの厚さで意図的にドーピングされておらずドーピングレベルが $5 \times 10^{15} / \text{cm}^3$ 未満であるSiイントリンシック層8808であり、次いで約0.3 μmの厚さで燻ドーパントで $1 \times 10^{19} / \text{cm}^3$ を越えてドーピングされているSiN層8810である。ケース1及びケース2の両方に対して光子は、シミュレーション研究のために、上部表面即ちSiNエピタキシャル層（8710及び8810）を有する表面から入射する。

【0150】

図89は、幾つかの実施例に基づいて、マイクロストラクチャ型穴アレイが該SiPエピタキシャル層までエッチングされていること以外は図87におけるものと同じエピタキシャル構造を示している。このケース3においては、穴8922は1500 nmの直径及び正方形格子アレイにおいて2000 nmの周期を有している。800～880 nmの波長を有する光子が上部表面即ちSiNエピタキシャル層8710上に入射する。該N及びP層／基板は或る適用例においては交換させることが可能であり、その吸収結果はほぼ同じである。

【0151】

図90は、幾つかの実施例に基づいて、マイクロストラクチャ型穴アレイが該BOXSiO₂層へエッチングされていること以外図88におけるものと同じであるエピタキシャル構造を示している。このケース4においては、穴9022は1500nmの直径及び正方形格子アレイにおいて2000nmの周期を有している。800-880nmの波長を有する光子が上部表面即ちSiNエピタキシャル層8810上に入射する。該N及びP層/基板は或る適用例においては交換可能であり且つその吸収結果はほぼ同じである。

【0152】

更に、該穴は該エッチストップ層SiGeB8816までエッチングさせることが可能である。エッチストップ層8816は高度にPドーピングされており且つP層とエッチストップ層とが処理において所望される場合の層構造において使用することが可能であり、このことはフォトダイオード及びアバランシェフォトダイオード構造を包含している。

【0153】

図91A-91Bは、図87-90に図示した例示的構造に対するシミュレーションの結果を示しているプロットである。図91Aはケース1-4（夫々、図87-90）の比較を示しており、その場合に、FDTDシミュレーションを使用して800-900nmにわたって示した波長に対しての各ケースにおける「I」Siイントリンシック層に起因する吸収を計算している。各ケースにおいて、光子は上部表面即ちNSiエピタキシャル表面へ入射している（図87-90における層8710及び8810）。該「I」層以外のその他の層に起因する吸収は包含されていない。曲線9110、9112、9114、9116は、ケース1、2、3、4（図87、88、89、90に示してある）に対する結果を夫々示している。ケース1及び2においては、マイクロストラクチャは存在しておらず、該1層における吸収は40%未満である。そのことは、入射光子の内の40%が吸収されたことを意味している。ケース1においては、それは15%未満であり、且つケース2においては、例えば805nmの或る波長において、それは丁度40%未満とすることが可能であり且つ一層長い波長の880nm及び850nmにおいて20%未満へ減少し且つ885nmにおいては10%未満である。吸収は量子効率に直接比例している。何故ならば、光子が吸収され且つ電子及び正孔へ変換されそれらの電子及び正孔が「I」領域を空乏化させるバイアス電圧の下で該「I」領域の外へ掃引される前に再結合しない場合には、これらの光発生されN及びP領域へ夫々掃引された電子及び正孔は光電流に寄与するからである。直径が1500nmで正方形格子における周期が2000nmであるマイクロストラクチャ型穴を包含しているケース3及び4において、或る波長においては100%に近い吸収レベルが見られている。ケース3及び4の両方において、800乃至900nmの波長において吸収は40%よりも大きい。800-850nmの範囲において、それは約70%よりも大きい吸収である。そして、ケース4においては、880乃至900nmにおいてその吸収は70%よりも良い。ケース4での855nmにおいては、吸収は95%を越えており、それは10%未満であるケース2と対比される。マイクロストラクチャの場合における「I」層におけるの吸収百分率は、穴直径、周期、及び/又は格子を変化させる、例えば正方形格子から六角形格子へ、ことによって或る波長において高吸収のために増加又は最適化させることが可能である。

【0154】

本書に記載する如きマイクロストラクチャを具備するシリコンPINフォトダイオードの場合に、波長が300Kにおける1.11eVのシリコンバンドギャップ、即ち約1117nmに近づく場合に吸収は必ずしも減少するものではないことが判明した。それと比較して、マイクロストラクチャの無いPIN（又はNIP）フォトダイオードの場合、波長が1117nmに近づくにつれて吸収は減少する。このことは、光学損失が減少するにつれてマイクロストラクチャの共振及び/又は結合共振のQ（品質係数）が増加し、従って光子が該マイクロストラクチャ内を行ったり来たりして跳ね返ることによりより多くの時間にわたり滞在し、その結果、波長が1117nmに近づく場合でも50%を超える場合がある吸収となっていることに起因しているものと考えられる。該マイクロストラ

クチャ内の屈折率差は実効指数で表すことが可能である。例えば、該穴はシリコン物質を取り除き且つ、例えば、空気で置換されるので、穴を具備する該領域の実効指数、即ち実効屈折率は、穴が無い場合の該領域の屈折率未満である。単純な評価は屈折率の平均であるが、例えば、該穴が穴を具備する該領域におけるシリコンの半分を除去する場合には、該穴が空気で充填されるものと仮定すると、その実効屈折率は約 $(1 + 3.44) / 2 = 2.22$ であり、その場合にバルク Si の屈折率は 1000 nm の波長において約 3.44 である。従って、穴を具備しており且つ穴を具備していない該領域は、ほぼ 1.22 の屈折率不連続性、即ち約 35% の屈折率変化、を見ることとなる。この屈折率における不連続性は、光学損失が低い場合に $1.000, 0.00$ 又はそれ以上に近づく場合がある Q を有する高コントラストグレーチングとなる場合がある。このことはマイクロストラクチャ型フォトダイオード及び／又はアバランシェフォトダイオードにおける吸収の向上を説明することが可能である。フォトンが該フォトダイオード／アバランシェフォトダイオードの走行時間及び RC 時間である特性時間に近づく時間の間該マイクロストラクチャ内に滞在する場合には、そのことは PD / APD のデータレート帯域幅に悪影響を与え始める。しかしながら、データレート帯域幅が低い場合には、一層高い Q を許容することが可能である。該 Q 係数は、格納されたエネルギー／サイクル当たりのエネルギー損失に比例するものとして定義される。これは該マイクロストラクチャにおける吸収向上に対する蓋然性のある説明である。該マイクロストラクチャは格子から構成されており、従って各々がその組の共振を有しており且つ密接に結合されている多数の単位セル又はセルから構成されている。単一共振器であるのでその共振はシャープなピークや谷であり且つ周期的な波動関数である単一の共振特性のみを示す従来既知の共振フォトダイオードとは異なり、結合共振セルを具備するマイクロストラクチャは、吸収がゆっくりと変化する、例えば、或る波長範囲、例えば $50 - 100 \text{ nm}$ 、に亘って 10% 未満だけ変化する波長に対する吸収における領域、及び非周期的な波動関数を有している。該マイクロストラクチャ型 PD / APD は複数列の共振の総和を有しており、従って従来既知の共振フォトダイオードと比較してそれほど際立っていないピーク及び谷を有している。非周期的な穴は、又、それ自身が非周期的であり且つ隣接する隣のセルと結合することが可能な共振セルを有することが可能であり、それは吸収及び／又はエミッションを向上させることが可能な結合型共振構造とさせる。

【0155】

概算見積もりとして、該特性時間は約 20 GHz 3 dB 帯域幅に対して約 20 ps である。 20 ps において、光はシリコン内を約 $2000 \mu\text{m}$ 走行し、そのことは、光が $2 \mu\text{m}$ マイクロストラクチャ内で約 1000 回バウンスすることが可能であり、従って $2 \mu\text{m}$ 厚さの「1」層は同等の光学長において $2000 \mu\text{m}$ の厚さとすることが可能であることを意味しており、従って、本特許明細書において記載するマイクロストラクチャにおいては、光は一層多くのバウンスを行い且つバルク吸収係数を上回らって向上されており且つ近似的に実効吸収＝バルク吸収×マイクロストラクチャ内のバウンス数として書くことが可能な実効吸収を与えることが可能である。光が該マイクロストラクチャ内において費やす時間は光学的走行時間と呼称され、それは該 MS-PD / APD に対する別の基本的な時間である。これら3つの基本的な時間、即ち RC 時間、走行時間、及び光学的走行時間を夫々二乗したものの和は全時間を二乗したものを与える。例えば、 $T(\text{全時間})^2 = T(\text{RC 時間})^2 + T(\text{走行時間})^2 + T(\text{光学的走行時間})^2$ であり、 20 GHz の場合には、全時間は 20 ps となる場合があり、且つ簡単化のために、RC 時間、走行時間、及び光学的走行時間は全て同じであると仮定すると、各時間は約 11.5 ps に過ぎない場合がある。光学的走行時間に対する 11.5 ps は約 $1000 \mu\text{m}$ の等価な光学長へ変換され、即ち、3つの基本的な時間の全てが等しいと仮定した場合に、該光学的走行時間が 11.5 ps よりも長い場合にそれが MS-PD の帯域幅を劣化させることを開始する前に、該向上された実効吸収長は $1000 \mu\text{m}$ 又はほぼ 250 の Q である場合がある。

【0156】

図91Bは、マイクロストラクチャ型穴アレイが異なる深さにエッチングされた場合の

図90(ケース4)におけるエピタキシャル構造を示している。曲線9120は、穴がSiO₂層8804へエッチングされた場合の800乃至900nmの波長の関数としての「1」Si層における吸収を示している。曲線9122は、SiGeB層8816へエッチングした穴について波長に対する吸収を示している。両方の場合に、光は上部表面即ちSiN表面8810から入射する。ピーク及び谷がシフトしているが、800-900の範囲における殆どの波長において該SiO₂層への全体的なエッチングは、該SiGeB層への穴のエッチングよりも良好である。

【0157】

図92は、幾つかの実施例に基づいて、穴をシリコン内へエッチングした場合のシリコンにおけるマイクロストラクチャ型領域を示している概略図である。その例示的な構造は、SiP基板9202、SiP層9206、SiI層9208及びSiN層9210を包含しており、それら全ての厚さ及びドーピングレベルは図示した如くである。穴9222が約2.3µmの深さへエッチングされており且つ1500nmの直径及び正方形格子において2000nmの周期を有している。概略点線の円9280で示した該穴が存在する領域は、実効屈折率 n_{eff} を有しており、それは1000nm波長で300Kにおいて約3.44であるバルクSiの屈折率よりも小さい。これは、該エッチングした領域は空気、真空にあるか、又はシリコンの屈折率よりも低い屈折率を有するポリイミド等の物質で充填されていることを前提としている。該マイクロストラクチャに対して上述した寸法に対して、穴を具備する該領域における実効屈折率は近似的に空気部分 $0.44 \times 1 + \text{Si}$ 部分 0.56×3.44 によって与えられ、それは約2.36である。例えば、上部表面9210に入射する光子は、該マイクロストラクチャ内にトラップされ且つ該2つの屈折率不連続部の間でバウンス即ち跳ね返る。一方の不連続部は空気とマイクロストラクチャとの間の界面であり、そこでの屈折率差は約1.36であり、且つ他方の不連続部はマイクロストラクチャとシリコンとの間の界面であって、そこでの屈折率差は約1.07である。この屈折率差は該マイクロストラクチャを損失性高コントラストグレーティングとみなすことを可能としており、そのことは観測される吸収の向上を説明することが可能である。

【0158】

図93は、幾つかの実施例に基づいて、テーパ付き穴を具備するMS-PD構造を示している概略図である。テーパの付いた漏斗形状の穴9322は実効屈折率 n_{eff} において次第に変化しており、それは穴の直径において著しい変化が無いが領域1におけるよりも一層小さい直径で、例えば、実効屈折率 n_{eff} を有している領域に対するものよりも一層小さく、その場合に、単にそこでのシリコン物質がより少ないという事実に起因して、領域1における実効屈折率は領域2における実効屈折率よりも一層小さい。領域1において、表面近くの実効屈折率は60%又はそれ以上のポイド(空気又は例えばポリイミド等の低屈折率物質)と40%又はそれ以下のシリコンとすることが可能であり、そのことは該上部表面(この場合にはSiN層)へ垂直に入射する光子に対して一層低い反射とさせる。垂直からずれて入射する光子においては、その反射は更に低いものとなる場合がある。更なる例として、該表面近くにおいて該穴が90%又はそれ以上を占有し且つSiが10%又はそれ以下を占有する場合には、垂直入射光子に対してのフレネル反射は1%又はそれ以下である場合がある。該穴の直径は深さに関して次第に減少しているので、領域1における実効屈折率は次第に変化する。図示例は漏斗であるが、それは、例えば、単に2つの別個の穴直径でのステップ即ち段差とするか、又は段差が該表面から遠ざかるに従い各段差直径が一層小さくなる複数の穴直径での複数の段差とすることが可能である。

【0159】

図94は、幾つかの実施例に基づいて、次第にテーパが付いた穴を具備しているMS-PD構造を示している概略図である。穴の全長にわたり延在している漸次的漏斗形状を有する穴9422で別の形態が図示されている。その実効屈折率も深さの関数として次第に増加する。幾つかの実施例によれば、穴は複数の直径、周期、及び/又は異なる漏斗形

状を有する擬似ランダム又はランダム穴で設けることが可能である。種々の穴パラメータは或る波長帯域において吸収特性を改善するか又は最適化させるために使用することが可能である。幾つかの実施例によれば、穴 9422 は各段差が異なる直径を有している一連の段差を設けることが可能である。これらの段差は均一の間隔とさせるか及び／又は不均一の間隔とさせることが可能である。それらの間隔は、波長の特定の帯域において吸収特性を改善させるか又は最適化させるために、例えば、フィルター又は結合型共振器等を形成するために、四分の一波長、半波長、又は四分の一波長及び半波長の倍数とすることが可能である。光学的発光体の場合、該穴又は柱体の直径におけるこの様な段差は、例えば、利得媒体との光波のオーバーラップを改善させることが可能である。幾つかの実施例によれば、穴 9422 の漏斗形状は任意の形状を有することが可能である。例えば、V 形状とすることが可能であり且つ空気・穴界面においての及び穴・シリコン界面においての実効屈折率は反射及び吸収特性又はエミッション特性における向上のために最適化させることが可能である。

【0160】

該マイクロストラクチャ型 PD/APD と関連する吸収向上に対する別の説明は、該マイクロストラクチャはメタマテリアルであり且つブロードバンド吸収体として振舞うことが可能である。例えば、G. Bayal et al. 「ITO を接地面として使用した可視透過性のブロードバンド赤外メタマテリアル吸収体 (Broadband infrared metamaterial absorber with visible transparency using ITO as ground plane)」、オブティックスエクスプレス (OPTICS EXPRESS)、15104 June 2014、N. Lie et al. 「赤外完全吸収体及びそのプラズモニクセンサとしての適用 (Infrared Perfect Absorber and Its Application As Plasmonic Sensor)」、ナノレター (Nano Lett.)、2010.10.2342-2348、及び L. Meng et al. 「近赤外波長における極性感応性完全吸収体 (Polarization-sensitive perfect absorbers at near-infrared wavelengths)」、オブティックスエクスプレス (OPTICS EXPRESS)、A111 Dec 2012 (以後、「Meng et al.」を呼称) を参照すると良く、これら全ての文献は引用により本書に取り込む。

【0161】

例えば、Meng et al. において、複数の溝がクロスパターンで交差される場合、吸収は極性独立性である。長尺溝の代わりに、本書において記載するように、Meng et al. における Au はシリコン及び／又はゲルマニウム等の半導体で置換されており、且つ穴／溝はボイドであってそれは空気、気体、真空、ポリイミド、及び／又は該穴を部分的に又は完全に被覆する任意の誘電体とすることが可能である。特に、Meng et al. の図 11 においては、その構造がクロスバーである場合には、Au 基板上に誘電体の正方形アレイが存在している。幾つかの実施例によれば、Au は、半導体及び空気、気体、又は二酸化シリコン、窒化シリコン、フッ化カルシウム、スピリン・オン・ガラス、ポリイミド、又はパッシベーション誘電体などの誘電体物質で充填されている穴を具備している誘電体で置換されている。Meng et al. における図 11 も波長に対する吸収を示している。

【0162】

高コントラストグレーチングは或るクラスのメタマテリアルと考えることが可能である。このことは、その他の効果と共に、観察された吸収向上を説明することが可能な場合がある。その他の効果は、プラズモン、非線形、サブ波長及び近波長効果、フォトリソニック結晶、遅波、結合型共振、干渉、フィールド向上、及び損失を伴う共振を包含している。

【0163】

図 95 は、幾つかの実施例に基づいて、異なる直径のマイクロストラクチャ型穴を具備している物質構造を示している概略図である。穴 9522 及び 9524 は異なる直径を有している。周期が近似的に同じである場合には、より小さな直径の穴はより大きな直径の穴よりも除去するシリコン物質は一層少ない。より小さな直径の複数の穴 9522 からなるアレイの実効屈折率は実効屈折率 n_{eff} であり、且つこれらの穴は MS-PD/APD の中心近くにクラスター即ち集めることが可能である。一層大きな直径の複数の穴 9524

からなるアレイは実効屈折率 n_{eff} を有しており、該一層小さな直径の穴の周りにクラスターすることが可能である（例えば、リング形状パターンで）。一層大きな直径の穴 9524 におけるよりも一層小さな直径の穴 9522 において除去される物質は一層少ないので、例えば、 n_1 は n_2 よりも一層大きい。光は n_2 領域内に案内され、従って光が該穴・シリコン（この例においては P シリコン）界面と該穴・空気界面との間で行ったり来たりバウンスする場合に、例えば回折に起因して失われる光は最小である。更に、メサエッチングは該 N シリコン層及び領域 9530 における「I」シリコン層の全部ではないにしても殆どを除去する。メサ 9540 がエッチングされてこの例に示した如く NIP 接合の容量を測定する。或る場合には、該 NIP 接合容量を測定するためにイオン注入及び／又は拡散を使用することが可能である。そして、或る場合には、該 N S i 層のみを除去し及び／又は低ドーピング又は反対のドーピングへ変換させることが必要であるに過ぎない。該 N 及び P は交換可能であり、例えば、MS-PD は PIN とし且つ MS-APD を NIP 又は PIPIN とすることが可能である。

【0164】

図 96 は、図 95 に図示した如く、異なる直径のマイクロストラクチャ型穴を具備する物質構造の平面図を示している。見えるように、より小さな直径の穴 9522 はより大きな直径の穴 9524 の中にクラスターしている。その結果得られるこのマイクロストラクチャ型フォトダイオード／アバランシェフォトダイオード (MS-PD/APD) 9600 の中心近くにおける領域間での実効屈折率差は、光が一層高い実効屈折率の領域へより一層案内されるというようなオブチカルファイバーと同様の光案内効果を生じさせることとなる。エッチング除去された領域 9530 によって測定されているメサ 9540 も示されており、それは更に光案内効果を与えることが可能である。メサ 9540 は、又、NIP 接合容量を測定し、且つ単にその N 層、「I」層を介して、又は P 層まで完全にエッチングさせることも可能である。図示していないものは、オーミックコンタクト金属、ボンド金属、パッシベーション、平坦化、ポリイミド、及びその他の誘電体等である。該 MS-PD/APD の開口数は、幾つかの実施例によれば、クラディング（一層大きな直径の穴）と比較してコア区域（一層小さな直径の穴）内の穴の直径を調節することによって調節することが可能である。実効屈折率を変更させるためには、穴の密度及び直径が或る領域内のシリコン物質の量を調節するための方法である。

【0165】

幾つかの実施例によれば、一層高い屈折率のコアと一層低い屈折率のクラディングとを有する案内構造は、例えば、回折に起因する光損失を減少させるか又は最小とさせるために、光学的導波路等の光案内器として効果的に動作することが可能である。例えば、周期が 2300 nm で穴直径が 1500 nm である正方形穴格子は近似的な実効屈折率を 2.63 とすることが可能であり、及び周期が 2000 nm で穴直径が 1500 nm である正方形格子は近似的な実効屈折率を 2.36 とすることが可能である。一層高い屈折率のコア側で且つ一層低い屈折率をクラディング側とすることが可能である。該コアとクラディングとの間の約 10% の屈折率差は該正方形格子の周期を変えることによって達成することが可能である。その他の組合せとすることも可能である。該クラディングは六角形格子を有することが可能であり且つ該コアは正方形格子を有することが可能であり、その場合に周期及び直径は同じままでも又は変化するものであっても良い。

【0166】

図 97A 及び 97B は、図 82A に示した如き層構造を具備するマイクロストラクチャ上に入射する光に対する吸収を示しているグラフである。六角形及び正方形の格子アレイ内に穴を 1500 nm の直径で且つ夫々 2000 及び 2500 nm の周期でエッチングしている。曲線 9712 は同一の周期及び穴直径を有する正方形格子に対するものである。その吸収は 1.4 乃至 1.6 μm の波長において 80% を越えており、且つ 1.55 μm においては六角形格子に対して 90% を越えている。曲線 9714 は、マイクロストラクチャ型穴無しでの吸収であり、10% 又はそれ未満の吸収を与えており且つ 1.55 μm においては数% の吸収に過ぎない。更に、六角形格子の場合、吸収は 1450 nm 乃至 1

600 nmの波長範囲に亘り10%未満だけ変化している。図97Aは、又、データ及び通信帯域、S、C、L、U/XL、を示している。図82Aにおけるような構造の場合、MS-PPD/APDはS乃至U/XLのこれら全ての帯域において使用することが可能である。

【0167】

図97Bにおいて、曲線9720は、周期が2500 nmの六角形穴格子であり且つ穴直径が1500 nmの場合の波長に対する吸収を示しており、且つ曲線9722は同じ周期及び直径の正方形格子に対するものである。それは最適性がより低いものであるが、1.55 μ m波長においては、その吸収は90%を越えている。曲線9714も参照のために示されている。

【0168】

吸収と量子効率とは直接的な比例関係にあり、且つ最小の反射での約90%の吸収は約90%の量子効率と同等である場合がある。例えば、外部量子効率を $QE = (1 - R)(1 - e^{-\alpha x})$ として定義することが可能であり、尚RはMS-PPD/APDの表面からの反射であり、 α は吸収係数であり、且つxは吸収長である。吸収は $(1 - e^{-\alpha x})$ で与えることが可能であり、それは吸収係数が α で長さがxにおいて吸収されるフォトン量である。1.55 μ m波長での90%の吸収は吸収係数と吸収長との積へ変換され、 αx は約2.3に等しい。バルク吸収係数が使用される場合には、1.55 μ m波長において460/cmであるから、xは約50 μ mである。Geの物理的長さ2.2 μ mと比較して、光は吸収領域を約23回通過したこととなる。等価的に、物理的な吸収長が2.2 μ mである場合には、向上される実効吸収係数は1.55 μ m波長において約10455/cmであり、一方1.55 μ m波長においてのバルク吸収係数が約460/cmであるのと対比される。このことも向上が約23倍であることを示している。

【0169】

該吸収向上は以下の事項のいずれか又は組合せによって発生させることが可能であり、即ち、フィールド向上、干渉、プラズモン、メタマテリアル吸収体、高コントラストグレーチング、波長及びサブ波長特徴寸法、非線形効果、共振効果、損失を伴う高コントラストグレーチング、遅波、結合波、結合型共振、結合モード、及びフォトニック結晶である（例えば、Krauss, J. 「フォトニック結晶導波路における低速光 (Slow light in photonic crystal waveguides)」, Phys. D: Appl. Phys. 40 2666-2670(2007)を参照すると良く、それを引用により本書に取り込む）。

【0170】

更に、吸収に直接的に比例する量子効率はデータ/遠隔通信波長の範囲に亘って高い。標準的な帯域はS (1460-1530 nm)、C (1530-1565 nm)、L (1565-1625 nm)、及びU/XL (1625-1675 nm)である。示していないその他の帯域も高い吸収効率を有することが可能であり、例えばO (1260-1360 nm)及びE (1360-1460 nm)等である。単一のマイクロストラクチャ型Ge・オン・SiPPD/APDは全体的なデータ/遠隔通信波長スペクトルをカバーすることが可能である。例えば、Gasca, 「OからLへ：光学的波長帯域の未来 (From O to L: The Future of Optical-Wavelength Bands)」, www.broadbandproperties.com、BROADBAND PROPERTIES、2008年6月、を参照すると良く、それを引用により本書に取り込む。

【0171】

図98は、図82Aに示してあり且つ図97A及び97Bにおいてシミュレーションした構造に対するシミュレーションした吸収を示しているグラフである。曲線9810及び9812は六角形格子及び正方形格子の夫々に対する吸収を示している。各場合において、穴周期は2000 nmであり且つ直径は1500 nmであった。該構造は850 nm波長範囲において良く吸収しており、830乃至1000 nmの間では80%より良い吸収であることが理解できる。一つの利点は、単一の装置で、70%より良い吸収及び/又は量子効率で、波長のカバレッジは800乃至1700 nm及びそれ以上にわたることが可

能であることである。この様なGe・オン・SiMS-APDはエレクトロニクスと集積化させることが可能であり、従ってMS-APDと相互インピーダンス増幅器又は信号処理用のその他の集積回路エレクトロニクスとを有する単一チップとすることが可能であり、そのことは組立コストやパッケージングコストを著しく低下させる。

【0172】

図99は、幾つかの実施例に基づいて、800乃至1000nmの波長範囲において動作するためのSiアバランシェフォトダイオード用の別の好適なエピタキシャル構造を示している。特に、図示した構造は、データ通信の多くが行われる850nm±30nm回りで且つ5-40Gb/s又はそれ以上のデータレートに対して非常に良く動作することが判明している。吸収を向上させるためにマイクロストラクチャが使用され、それは向上された吸収係数及び/又は向上される吸収長のいずれかとすることが可能である。NSi基板9902は、装置処理の後に、150μmへ薄くさせることが可能である。エピタキシャル層としては、例えば、厚さが0.1-4μmの範囲で且つ幾つかの場合においては0.3乃至2μmの範囲であり且つドーピングが $1 \times 10^{19}/\text{cm}^3$ を越えているNコンタクト層であるNSi層9906と、厚さが0.2乃至1μmの範囲で幾つかの場合には0.5μmであり且つバックグラウンドドーピングが $1 \times 10^{15}/\text{cm}^3$ 未満でありアバランシェ層としても知られる増倍即ち利得層であるSiイントリンシック即ち「I」層9918と、厚さが0.02乃至0.3μmで幾つかの場合には0.1μmであり且つドーピングが $1-6 \times 10^{17}/\text{cm}^3$ の範囲であり且ついくつかの場合には $1.8 \times 10^{17}/\text{cm}^3$ である電荷層であるPSi層9920と、厚さが0.3乃至4μmの範囲で幾つかの場合には2μmであり且つバックグラウンドドーピングが $1 \times 10^{15}/\text{cm}^3$ 未満である吸収層であるSiイントリンシック「I」層9908と、厚さが0.1乃至2μmで幾つかの場合には0.3μmであり且つドーピングが $1 \times 10^{20}/\text{cm}^3$ より大きくPコンタクト層であるPSi層9910とである。

【0173】

図100は、幾つかの実施例に基づいて、マイクロストラクチャ型APDの幾つかの特徴を示している概略図である。該MS-APDは図99に図示した物質構造を使用している。マイクロストラクチャ型穴アレィ10022はPSiコンタクト層9920内へ及び「I」Si吸収層9918内へ部分的か又は完全にのいずれかでエッチングされる。光は上部表面即ちPSi層9910から該表面へ垂直に及び/又は該表面に対して垂直からずれて入射する。メサエッチングをNコンタクト層9906まで実施して該装置の容量を測定する。Pオーミックコンタクト10028及びNオーミックコンタクト10030をPSiコンタクト層9910及びNSiコンタクト層9906上に夫々形成させる。10-60ボルトの逆バイアスを該P及びNオーミックコンタクトへ印加させる。Nコンタクト（カソード）と相対的に負電圧がPコンタクト（アノード）へ印加される。簡単化のために示していないものは、ハッシュン層、平坦化層、ブリッジング層、ボンドメタリゼーション層、及びガードリング等の要素である。吸収を向上させたマイクロストラクチャ型フォトダイオードとSiアバランシェ即ち利得層との結合は、該マイクロストラクチャ型SiAPDが5Gb/sより大きく且つ幾つかの場合には10Gb/sよりも大きなデータレートで800-1000nmの波長範囲で特に850nm±30nmにおいて動作することを可能とさせる。その他の場合には、該データレートを増倍係数が2、4、6、8、10又はそれ以上で15-40Gb/sとすることが可能である。Siマイクロストラクチャ型APDの一つの利点は過剰ノイズが低いことであり、それは、例えば、GaAs及び/又はInPをベースとしたAPDよりも一層低い。

【0174】

図101は、幾つかの実施例に基づいて、800乃至1700nmの波長範囲においての動作のためのGe・オン・Siアバランシェフォトダイオード用の別の好適なエピタキシャル構造を示している。特に、図示した該構造は、遠隔通信の多くが行われる1550±200nm回りで5-40Gb/s又はそれ以上のデータレートに対して良好に動作することが判明している。吸収を向上させるためにマイクロストラクチャを使用することが

可能であり、それは向上された吸収係数及び／又は向上された吸収長のいずれかとする
ことが可能である。N S i 基板 1 0 1 0 2 は装置処理の後に $150\text{ }\mu\text{m}$ へ薄くさせることが
可能である。該エピタキシャル層は、厚さが $0.1\text{--}4\text{ }\mu\text{m}$ の範囲で幾つかの場合には 0.3
乃至 $2\text{ }\mu\text{m}$ であって且つドーピングが $1\times 10^{18}/\text{cm}^3$ より大きな N コンタクト
層である N S i 層 1 0 1 0 6 と、厚さが 0.2 乃至 $1\text{ }\mu\text{m}$ の範囲で幾つかの場合には 0.5
 μm であり且つバックグラウンドドーピングが $1\times 10^{18}/\text{cm}^3$ 未満であるアバラ
ンシェ層としても知られている増倍即ち利得層である S i イントリニシック即ち「I」層
1 0 1 1 8 と、厚さが 0.02 乃至 $0.3\text{ }\mu\text{m}$ の範囲であり幾つかの場合には $0.1\text{ }\mu\text{m}$
であり且つドーピングが $1\text{--}6\times 10^{17}/\text{cm}^3$ で幾つかの場合には 1.8×10^{17}
 $/\text{cm}^3$ である電荷層である P S i 層 1 0 1 2 0 と、厚さが 0.3 乃至 $4\text{ }\mu\text{m}$ の範囲で幾
つかの場合には $2\text{ }\mu\text{m}$ であり且つバックグラウンドドーピングが $1\times 10^{18}/\text{cm}^3$ 未
満である吸収層である G e イントリニシック「I」層 1 0 1 0 8 と、厚さが 0.1 乃至 2
 μm の範囲で幾つかの場合には $0.2\text{ }\mu\text{m}$ であり且つドーピングが $1\times 10^{20}/\text{cm}^3$
より大きな P コンタクト層である P G e 層 1 0 1 1 0 とである。しばしば、S i と G e と
の間の界面において、通常の G e エピタキシャル成長の前に、低温 G e バッファ層を成長
させることが可能である。この点については、例えば、K a n g e r a l を参照す
ると良い。

【0175】

図 1 0 2 は、幾つかの実施例に基づいて、マイクロストラクチャ型 G e ・オン・S i A
P D の幾つかの特徴を示している概略図である。該 M S - A P D は図 1 0 1 に図示した物
質構造を使用している。マイクロストラクチャ型穴アレイ 1 0 2 2 2 は、図 9 7 A におけ
る如き寸法、直径及び六角形格子で、P G e コンタクト層 1 0 1 1 0 内及び部分的に又は
完全に「I」G e 吸収層 1 0 1 0 8 内にエッチングされている。光は上部表面即ち P S i
層から該表面に対し垂直及び／又は該表面に対して垂直からずれてのいずれかで入射する
。N コンタクト層 1 0 1 0 6 に対するメサエッチングが本装置の容量を画定し、且つ P オ
ーミックコンタクト 1 0 2 2 8 及び N オーミックコンタクト 1 0 2 3 0 が P G e コンタ
クト層及び N S i コンタクト層の上に夫々形成される。 $10\text{--}60$ ボルトの逆バイアスを該
P 及び N オーミックコンタクトへ印加させる。簡単化のために図示していないものは、バ
ッシャー層、平坦化層、ブリッジング層、ボンドメタリゼーション層、及びガード
リング等である。吸収が向上されているマイクロストラクチャ型 G e フォトダイオードと
S i アバランシェ即ち利得層との結合は、マイクロストラクチャ型 G e ・オン・S i A P
D が、2 より大きく且つ幾つかの場合には 4 より大きく且つ更に幾つかの場合には $8\text{--}10$
より大きな増倍係数で 5 Gb/s より大きく且つ幾つかの場合には 10 Gb/s より大
きく且つ更に幾つかの場合には $15\text{--}40\text{ Gb/s}$ より大きなデータレートで $800\text{--}1700\text{ nm}$
で特に $1550\text{ nm}\pm 200\text{ nm}$ の波長範囲において動作することを可能とさせ
る。G e ・オン・S i マイクロストラクチャ型 A P D の一つの利点は過剰ノイズが一層
低いことであり、それは、例えば、G a A s 及び／又は I n P をベースとした A P D より
も一層低い。

【0176】

図 1 0 3 (A) - (C) は、幾つかの実施例に基づいて、マイクロストラクチャ型シリ
コン及びゲルマニウム・オン・S i フォトダイオード及びアバランシェフォトダイオード
に対する直径、周期、及びその他のパラメータを示している。図 1 0 3 (A) は、使用し
た種々のパラメータを示している表である。幾つかの実施例によれば、六角形及び正方形
の両方の格子を使用することが可能である。複数の穴のその他の格子及び／又は非格子配
置も可能であるが、図示してはいない。 $10, 25, 30, 40, 50, 60, 80\text{ }\mu\text{m}$
のメサ寸法は 5 乃至 80 を越える Gb/s のデータレートをサポートするための容量を達
成するために使用される。幾つかの実施例によれば、キャリアを枯渇させるためにイオ
ン注入又は拡散などの接合容量を画定するその他の方法を使用することが可能である。 $800\text{--}1000\text{ nm}$
で特に $850\text{ nm}\pm 30\text{ nm}$ の波長範囲における S i マイクロストラ
クチャ型 P D 及び A P D の動作のための穴直径及び周期は、例えば、六角形及び／又は正

方形格子のいずれかに対して1300/2000、1500/2000、700/1000、630/900（nm単位での直径/周期）の範囲にわたることが可能である。Ge・オン・Siマイクロストラクチャ型PD及びAPDの場合、800-1700nmで特に1550nm±200nmの波長範囲における動作に対して、六角形又は正方形のいずれかの格子に対する穴直径と周期との組合せの例は、1300nm/2000nm、1500nm/2000nm、1500nm/2500nm、1300nm/2300nmを包含している。その他の穴直径及び周期とすることも可能である。50%よりも良好な、及び、幾つかの場合には、70%又は90%よりも良好な吸収は、800-1000nm及び800-1700nmの波長においてこれらの直径及び周期で達成することが可能である。図103（B）及び（C）において、「d」は六角形及び正方形の格子パターンに対する周期として示されている。円形状の穴が図示されているが、楕円、矩形、多角形、及び／又はその他の不規則形状等の非円形状の穴も可能である。円形状の穴はFDTDを使用するシミュレーションの簡単化のために選択されているに過ぎない。

【0177】

図104（A）及び（B）は、マイクロストラクチャ型GeP-Ge1-SiN・オン・SiN基板フォトダイオードである図82Aに示した構造に関して波長に対しての吸収についてFDTD（有限差分時間領域）を使用したシミュレーション結果を示しているグラフである。注意すべきことであるが、このシミュレーション結果はマイクロストラクチャ型GePGe1SiPSi1SiNAPDへ適用することも可能である。該シミュレーションは六角形格子、1500nmの穴直径、2000nmの穴周期を使用しており、その場合に、該穴は該SiN層へエッチングされる。このシミュレーションにおいては、波長は1500nm±10nm（図104（A）における曲線10410）を且つ1550nm±1nm（図104（B）における曲線10412）を中心としている。そのシミュレーションメッシュは0.1nmよりも一層細かく、且つ図104（B）における曲線10412から、吸収は、1549乃至1551nm波長にわたって、0.9（90%吸収）を越える高吸収値及び0.85（85%吸収）を越える低吸収値で、10%未満の変動であることを理解することが可能である。波長に対する吸収におけるこの特性は光学的遠隔通信適用例において重要であり、その場合には、例えば、1550nmを中心とした波長変動の2nm以内の吸収において迅速な変化は存在しない。図104（A）における曲線10410は、1550nmを中心とする20nmの波長変動をこえる0.8乃至0.99の吸収変動を示している。どの2nmの波長変動にわたっても、その吸収変動は15%未満である。或る場合には、それは5%未満である。粗WDMに対する波長分割多重化（WDM）におけるチャンネル間隔は2nm又はそれより大きいものとすることが可能であり、一方密WDMに対しては、チャンネル間隔は0.8、0.4又はそれ未満とすることが可能であり、従って、例えば、1550nmにおいて、3個又はそれ以上のチャンネルが2nm分光幅内に適合することが可能であり、一方粗WDMに対しては、4nm又はそれ以上が必要とされる。

【0178】

図105（A）及び（B）は、幾つかの実施例に基づいて、正方形格子穴パターンに対する固有モードに関するものである。図105（A）は正方形格子配置における単一の単位セル10510を示している。図105（B）は、Si（又はGe）物質におけるマイクロストラクチャ型穴の単位セルにおける種々の2D固有モード（静止モード、定常波モード、共振モード）（マクスウェル方程式を使用するFDTDシミュレーションから）を示している。波は、例えば、空気／半導体界面とGe／Si界面との間を、該マイクロストラクチャ型穴アレイの長さに沿って伝播する。該マイクロストラクチャ型穴がエッチングされている領域によって導波路及び／又は共振器が画定されている。該単位セルにおける半導体及び穴の長さは光学的導波路及び／又は共振器と考えることが可能であり、且つ隣接する単位セルの多くの並列光学的導波路／共振器は結合されて、2Dアレイにおける結合された波、結合されたモード、及び／又は結合された共振器となることが可能である。高コントラストグレーチング（HCG）、フォトニック結晶、遅波効果及び結合された

導波路／共振器の固有モード、スーパーモード、フィールド向上、線形及び非線形効果、横モード、導波共振モード (guided resonant modes)、ブロッホ (Bloch) モード、及び結合されたブロッホモードの組合せは吸収である ($1 - e^{-\alpha x}$) に比例する量子効率に対する式における「 αx 」積の観察される向上を発生させることが可能であり、尚 α はバルク物質吸収係数であり且つ x は吸収長である。 x が一定である場合には、 α を向上させることが可能であり、 α が一定である場合には、 x を向上させることが可能であり、且つ幾つかの場合には、 α と x の両方を向上させることが可能である。図 105 (B) は、図 105 (A) における正方形格子の単位セル 10510 の多くの複雑な固有モードを示している。該正方形格子における各セルはこれらの固有モードの内のいずれか一つ又は複数を有することが可能であり且つ隣接するセルの固有モードと結合することが可能であり、これら全てのセルの大量に結合されたモードはスーパーモードと呼ばれる。この大量の結合は、波長に対して「一層滑らかな」吸収特性となる場合があり、尚一層滑らかとは或る波長範囲、例えば 200 nm で或る場合には 500 nm で且つ或る場合には 1000 nm 又はそれ以上、にわたっての吸収特性においての変動が 10% 未満であるものとして定義することが可能である。

【0179】

図 106 は、幾つかの実施例に基づいて、互いにオーバーラップして配置された 2 個の正方形格子でのマイクロストラクチャ型穴を示している概略図である。点線の正方形 10610 は穴直径として D1 を有する正方形格子の単位セルを表している。破線の正方形 10612 は同様の周期であるが穴直径として D2 を有している別の正方形格子を表しており、D1 と D2 とは等しくない。もしも D1 が D2 と等しい場合には、それは正方形格子 (45 度だけ傾斜) である。又は、等価的に、これら 2 つの正方形格子の周期が同様のものである場合には、2 つの異なる穴直径を有する六角形格子として考えることも可能である。該格子パターンは、2 つを越えて異なる穴直径を有することも可能であり、例えば、六角形格子において 3 つの異なる穴直径を有することが可能である。例えば、複数の穴からなる一つの好適なマイクロストラクチャにおいて、D1 は 1300 nm 直径とすることが可能であり且つ該正方形格子は 2000 nm の周期を有することが可能である。マイクロストラクチャアレイにおいて一つを越える穴直径を有することの一つの利点は、波長に対する吸収の曲線が更に平坦化されて、吸収における変動が、Si 内に構成されるマイクロストラクチャ型 PD/APD に対する波長において 800–990 nm にわたり、且つ図 101 におけるような Ge・オン・Si 内に構成されるマイクロストラクチャ型 PD/APD に対する 1250–1750 nm の波長に対して、20% 未満とすることが可能であるということである。幾つかの場合において、該変動はこれらの波長範囲に亘っての変動は 10% 未満であり、且つ幾つかの場合には、5% 未満である。又、全体的な吸収又は等価的に該マイクロストラクチャ型 PD/APD の量子効率を改善させることが可能である。

【0180】

異なる穴直径を散在させることは吸収に直接比例する量子効率を一層広い範囲の波長、特に、シリコンにおけるマイクロストラクチャ型 PD/APD に対して 800–990 nm で且つ Ge・オン・Si におけるマイクロストラクチャ型 PD/APD に対して 1000–1800 nm、にわたって更に平坦化させることを可能とする。幾つかの実施例によれば、その他の穴直径及び周期とすることも可能である。

【0181】

幾つかの実施例によれば、例えば吸収用物質の厚さなどの設計パラメータ内において適切な量子効率を維持するのにバルク吸収係数が不十分である場合に、PD/APD の量子効率を向上させるために使用されるマイクロストラクチャ型穴及び／又は柱体の吸収における改良は、太陽電池、イメージング用センサー、ラディエーション吸収体等のフォトンの吸収を使用するその他の装置へ適用させることが可能である。

【0182】

図 107 は、幾つかの実施例に基づく、Ge・オン・Si のエピタキシャル構造を示し

ている概略図である。該構造は図82Aに図示したものと同様であるが、Nドーピングが $1 \times 10^{18} / \text{cm}^3$ を越えている $0.2 \mu\text{m}$ (又は $0.1 - 2 \mu\text{m}$ の範囲)のSiN層10706上に成長されたバックグラウンドドーピング (N又はPのいずれかとすることが可能) が $1 - 5 \times 10^{18} / \text{cm}^3$ で $0.1 - 0.5 \mu\text{m}$ 厚さのSi層10718が付加されており、次いで意図的にはドーピングされておらずバックグラウンドドーピングが $5 \times 10^{15} / \text{cm}^3$ 未満で幾つかの場合には $5 \times 10^{13} / \text{cm}^3$ 未満であり且つ厚さが $2 \mu\text{m}$ 又は $0.5 - 2.5 \mu\text{m}$ の範囲であるGe層10708がそれに続いている。PGe層10710が最上部でドーピングが $1 \times 10^{18} / \text{cm}^3$ を越えており且つ厚さが $0.2 \mu\text{m}$ 又は $0.2 - 0.5 \mu\text{m}$ の範囲である。これらの層の全てがNSi基板10702上に成長される。マイクロストラクチャ型穴アレイ10722は図103(A) - (C) に示したパラメータを使用して形成することが可能である。幾つかの実施例によれば、穴直径は $1300 - 1500 \text{nm}$ であり且つ周期は六角形又は正方形の格子において 2000nm である。その他の実施例によれば、図106に示したようなレイアウトが使用される。その様な場合には、複数の直径を有する穴は、例えば、図106に示した如く互いに入れ子構造とさせた周期 2000nm の 1300nm 及び 1500nm の正方形格子とすることが可能である。

【0183】

Si層10718は、Ge層を成長させることを可能とさせるためにGe層10708内へのドーパント拡散が減少されるか又は最小とされるようにSiにおけるドーパントを低いレベルとさせるために使用される。

【0184】

幾つかの実施例によれば、図107に示した構造はマイクロストラクチャ型PD用であり且つ、図101における如く、増倍層と電荷層とを付加したマイクロストラクチャ型APD用とすることも可能である。この構造に対する波長範囲は $800 - 1700 \text{nm}$ で、特に約 $1550 \text{nm} \pm 200 \text{nm}$ とすることが可能である。

【0185】

付加したSi「I」層10718は本装置の容量を減少させることにも寄与する。何故ならば、該「I」層は今や該Ge層と該Si層との総和だからである。容量における減少はPD/APDの変調帯域幅を増加させることを助ける。該Si「I」層は、幾つかの場合において、その厚さが、例えば 0.1 乃至 $3 \mu\text{m}$ の範囲である場合がある。穴10722は、例えば、該Si「I」層までエッチングすることが可能であり、及び/又は幾つかの場合においては該Si「I」層内へエッチングすることが可能である。

【0186】

図108は、幾つかの実施例に基づいて、Ga・オン・Siのマイクロストラクチャ型フォトダイオードの基本的な特徴を示している概略図である。該構造は図107に図示したものと同様であるか又は同一である。該MS-PDは $1300 - 1700 \text{nm}$ 及び $600 - 1300 \text{nm}$ の波長範囲において良好に動作することが判明している。図示した如く、光は穴アレイがエッチングされている上部表面から入射する。幾らかのマイナーチェンジでもって、底部上のNオーミックコンタクト10832に開口を設け且つSi基板10702の底部を反射防止コーティングでポリッシュした場合には、光は該基板の底部から入射することも可能である。更に、オブチカルファイバーを該マイクロストラクチャ型PDに対してアライメント即ち整合させるためのガイドを与えることが可能であるようにSi基板10702の底部上にビア (不図示) を形成することが可能である。この例においては、穴10722はSi層10718までエッチングされる。幾つかの実施例によれば、該穴は該Si層内へ又はそれを通してエッチングさせるか、又は該Si層まで貫通してエッチングさせないことが可能である。穴アレイは複数の穴寸法及び複数の周期を有することが可能であり、且つ非周期的なものとさせることが可能である。穴直径は $500 - 1700 \text{nm}$ の範囲とすることが可能であり、且つ周期は $1000 - 2500 \text{nm}$ の範囲とすることが可能である。幾つかの実施例によれば、穴直径は 1300 及び 1500nm で、正方形又は六角形の格子における周期が 2000nm である。更に、 1300

及び1500 nmの穴は、図106に示した如くに互いに入れ子とされている周期が2000 nmの正方形格子内のものとする事が可能である。穴直径及び周期は10-50 nmだけ、且つ幾つかの場合においては50-100 nmだけ変化する場合がある。図示していないものとしては、パッシベーション層であって、それは該半導体の壁上に2-100 nmの厚さを有する場合がある。パッシベーションは漏れ電流を減少させるために露出されているメサの高電界領域において使用することが可能である。-2乃至-12ボルトの逆バイアスがPコンタクト10828とNコンタクト10830（及び／又は10832）との間に印加される。逆バイアスとは、負電圧がN（カソード）コンタクトと相対的なP（アノード）へ印加されることを意味している。負記号を付けて又は付けずに示されている電圧は、カソードと相対的にアノードにおいて負であることを意味している。更に、複数の穴は異なる形状を有することが可能であり、必ずしも全てが円形状であることは必要ではない。

【0187】

光検知器においてナノワイヤーを使用することは既知である。該ナノワイヤーはInPであり且つ該光検知器は14 ps応答時間、又は等価的に、ガウス変換に対する周波数領域において、約30 GHz 3 dB変調帯域幅に制限されることを示している。V.J. Logeeswaran et al.「非晶質表面上の交差するInPナノワイヤーで製造された14 ps半値全幅高速光導電体 (A 14-ps full width at half maximum high-speed photoconductor fabricated with intersecting InP nanowires on an amorphous surface)」, アプライドフィジックス (Appl. Phys.), A 91, 1-5 (2008) (以後、「Logeeswaran et al.」) というを参照すると良く、これを引用により本書に取り込む。Logeeswaran et al. においては、入射する光子は780 nmにおいてであり且つ約780 nmにおけるInP吸収係数は約 35000 cm^{-1} であり且つ吸収の向上も吸収長も必要なものではなかった。同様に、別の既知の技術において、850 nm光子がナノワイヤー上に入射され且つ約850 nmにおけるGaAsの吸収係数は約 12000 cm^{-1} であり、その場合も吸収の向上及び／又は長さが必要なものではなかった。M.A. Seyedi et al.「大活性区域で9 GHz変調帯域幅での効率的なショットキー状接合GaAsナノワイヤー光検知器 (Efficient Schottky-like junction GaAs nanowire photodetector with 9GHz modulation bandwidth with large active area)」, アプライドフィジックスレターズ (APPLIED PHYSICS LETTERS), 105, 041105 (2014)を参照すると良く、これを引用により本書に取り込む。対照的に、本書に記載する技術によれば、高速フォトダイオード／アバランシェフォトダイオードがps応答時間及び／又は5 Gb/s又はそれ以上にの変調帯域幅で記載されている。850 nmにおけるSiにおいて、吸収効率は約 700 cm^{-1} であり且つ吸収の向上及び／又は吸収長を使用して40%又はそれより良い量子効率を達成している。同様に、Geに対して約1550 nmにおいて、その吸収効率は約 459 cm^{-1} であり、それもまた吸収の向上及び／又は吸収長を使用している。

【0188】

例えば、約10-30 Gb/sにおける動作のための典型的な高速又は高変調帯域幅PD/APD用の2 μm 厚さの吸収用「I」層の場合（該「I」層は該PD/APDの変調帯域幅に依存して0.3-3.5 μm 変化することが可能）、850 nmにおける光子の約13%が向上無しで吸収される。例えば、本特許出願において記載するマイクロストラクチャ型穴アレイ（又は柱体）によって約12倍又はそれ以上だけの吸収の向上及び／又は吸収長がある場合には、光子の80%を超えるものを2 μm の物理的な「I」吸収長において吸収させることが可能である。夫々850及び1550 nmのデータ通信波長及び遠隔通信波長においてSi及びGe等の弱い吸収性（約 1000 cm^{-1} 又はそれ未満）物質を使用する場合にマイクロストラクチャ型穴及び／又は柱体を付加すると、その吸収即ち吸収係数及び／又は吸収長を、該物質が強く吸収性となり（約 2000 cm^{-1} 又はそれ以上）且つ該マイクロストラクチャ型PD/APDを高速又は高変調帯域幅データ及び遠隔通信適用例及びシステムのために使用することが可能である点まで向上さ

せることが可能であることがここで証明された。

【0189】

幾つかの場合においては、或る光学的データ／遠隔通信のためには単に約40%の吸収で十分であり、且つ単に約3倍の吸収の向上及び／又は吸収長が、例えば、850nmにおいての2 μ m Si「1」層に対して必要とされるに過ぎず、又は2 μ m Ge「1」層に対しての1550nm波長におけるGeに対する吸収係数又は吸収長の4、5倍の向上係数が必要であるに過ぎない。一層高い向上係数が可能であり、10より大きな係数、且つ幾つかの場合においては20より大きなもの及び幾つかの場合においては40より大きいものとすることが可能である。半導体バルク物質の吸収係数が一層小さくなるに従い、向上係数は一層大きくなり、100又はそれ以上となる。

【0190】

Siナノワイヤーの吸収は、Lu Hu, Gang Chen, ナノレターズ (Nano Lett.) 「光電池適用例に対するシリコンナノワイヤーアレイにおける光学的吸収の解析 (Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications)」, Vol. 7, No. 11, 2007 (以後、「Hu et al.」と呼称する) において討論されており、それを引用により本書に取り込む。850nmに対応する1.46eVにおいての吸収は薄いSi膜と比較して向上されず、且つ約2.25eVの上即ち約550nm又はそれより短い波長の場合には、吸収は薄いSi膜と比較して向上される。Hu et al. は、更に、「一方、低周波数範囲においては、シリコンの吸収係数 (extinction coefficient) は小さいために改良を達成することは不可能である」と付け加えている。

【0191】

同様の結論は別の刊行物においても到達されており、即ち、Chenxi Lin, Michelle L. Provinelli 「光電池適用例に対する大きな格子定数を有するシリコンナノワイヤーアレイにおける光吸収の向上 (Optical absorption enhancement in silicon nanowire arrays with a large lattice constant for photovoltaic applications)」, Vol. 17, No. 22 / オプティクスエクスプレス (OPTICS EXPRESS), 19371, 2009年10月26日 (以後、「Lin et al.」と呼称する) があり、それも引用により本書に取り込む。Lin et al. は約1.5eVにおいての吸収の共振向上を示しており、そのことをLin et al. はナノ構造において電磁界強度の増大となるガイド共振モード (guides resonance mode) 又は遅ブロッホモード (slow Bloch mode) によるものであるとしている。Lin et al. は「空中からの入射光を2D周期的構造の高Q漏洩モードへの結合」と述べている。高Qモードのシャープな共振はデータ及び／又は遠隔通信適用例に対するフォトダイオードの使用において望ましいものではない。共振フォトダイオードの特性は、例えば、J. D. Schaub et al. 「エピタキシャル横方向過剰成長により成長された共振空洞向上型高速Siフォトダイオード (Resonant-Cavity-Enhanced High-Speed Si Photodiode Grown by Epitaxial Lateral Overgrowth)」, IEEE フォトニクステクノロジーレターズ (IEEE PHOTONICS TECHNOLOGY LETTERS), VOL. 11, No. 12,

1999年12月 (以後、「J. D. Schaub et al.」と呼称する) において討論されており、尚その文献を引用により本書に取り込む。Schaub et al. は約800nm波長において高々40%の量子効率を示している (例えば、Schaub et al. における図3を参照)。しかしながら、そのシャープな共振は望ましいものではない。何故ならば、温度に起因する送信機の波長におけるドリフト (例えば、或るダイオードレーザーに対して0.3nm/度であり、且つジュール加熱及び環境に起因するレーザー内部温度は、例えば、データセンターにおいて高々80℃又はそれ以上変化する可能性がある) は、例えば、量子効率において著しい変化を発生させる可能性がある。シャープな共振を有する従前に既知の共振フォトダイオードも量子効率が最高であるピーク共振波長の点で温度に敏感である場合がある。更に、レーザー源は、しばしば、製造上の変動に起因してレーザー波長において変動を有しており、レーザーをフォトダイオードに対して波長において精密に整合させねばならないことは望ましいことではない。共振フ

フォトダイオードの製造における変動は変化する波長における共振ピークとなる場合もある。このことは、該レーザー源と検知器の波長を整合させることの必要性のために注意深いテスト及び温度安定性を維持することが必要であるので、歩留まりを低下させ且つ光学システムのコストを増加させることとなる。

【0192】

最近の文献であるRui Ren, Yong-Xin Guo, Ri-Hong Zhu「太陽エネルギー収穫用楕円シリコンナノワイヤーアレイにおける向上された吸収 (Enhanced absorption in elliptical silicon nanowire arrays for solar energy harvesting)」オプティカルエンジニアリング (Optical Engineering) 53 (2)、027102 (2014年2月) も1.5 eV 10 においての向上が弱い又は存在しないが一層高いエネルギーにおける吸収の向上が一層強いという同様の結果を示しており、尚その文献を引用により本書の取り込む。

【0193】

Donnelly et al.「光電池適用例用シリコンナノホールアレイのモードに基づく解析 (Mode-based analysis of silicon nanohole arrays for photovoltaic applications)」Vol. 22, No. 55、オプティクスエクスプレス (OPTICS EXPRESS)、A1343 2014年8月25日、(以後「Donnelly et al.」と呼称する) において、ナノホールが光電池適用例について解析されており、尚その文献を引用により本書に取り込む。太陽のスペクトルは非常に広い(数百nm)ので、シャープな共振は光電池適用例においては問題ではないが、一方光学的データ/遠隔通信においては、レーザーのスペクトルは非常に狭く、例えば、分布帰還形レーザー、フアブリー・ペローレーザー、垂直共振器面発光レーザー (VCSEL) 等のレーザーのタイプ、及びそれが単一モードであるか又はマルチモードであるか、及びそれが外部変調又は直接変調でのCWで動作されるか否かに依存して、1nmよりもかなり小さいものから数nm、即ち0.01未満〜3nmと狭いものである。Donnelly et al. は、又、例えば、その図4 20 において800nmにおいて20nmの波長スパンに亘って高々7.5%又はそれ以上だけの吸収における変動と共に850nm波長領域においてシャープな共振を示している。Donnelly et al. の図5は、種々のナノホール深さでの500nmの最適な周期を示しており、又、例えば、850nm波長においてシャープな共振を示しており、その場合に吸収は10nm波長スパンに亘って約100%乃至20%変化、即ち吸収において約80%の変化する場合がある。共振導波モード (resonance guided mode) に加えて、該文献は基本モード及び吸収向上を発生させることが可能なチャネルリングモードも 30 包含している。

【0194】

量子効率に直接的に比例する吸収におけるリップルが約30%〜40%、及び幾つかの場合においては20%以下又は10%以下はデータ通信適用例及び遠隔通信適用例に対して許容可能なものである。幾つかの場合において、約850nmの中心波長、例えば、±5、10、20、50又は100nmに対して、量子効率のリップルは5%以下が望ましい。

【0195】

実験的には、光トラッピング及び向上された吸収はErik Garnett, Peidong Yang「シリコンナノワイヤー太陽電池における光トラッピング (Light Trapping in Silicon Nanowire Solar Cells)」、ナノレター (Nano Lett.)、2010, 10, 1082-1087 (以後、「Garnett et al.」と呼称する) において観察されており、尚該文献を引用により本書に取り込む。Garnett et al. の図4は、1100nm 40 までの波長において10%未満で且つ850nm波長において約5%の光透過を示しており、反射を無視することが可能である場合には、吸収は $I = T + R + A$ の式から約90-95%であり、尚Tは透過で、Rは反射で、Aは吸収であり、全ての光が回収されるものと仮定している。

【0196】

別の最近の文献であり引用により本書に取り込むKatherine T. Fountaine, Christian 50

G. Kendall, Barry A. Atwater「局所化したラジアルモード励起を介しての半導体ナノワイヤーアレイ用の1に近いブロードバンド吸収デザイン (Near-unity broadband absorption design for semiconducting nanowire arrays via localized radial mode excitation)」Vol. 22, No. オプティクスエクスプレス (OPTICS EXPRESS) A 930, 2014年5月5日(以後、「Fountain et al.」と呼称する)において、異なる直径を有する3 μm 高さのSi上のGaAsナノワイヤーのシミュレーション結果は、5%の充填率で1に近い吸収を達成することが可能であることを示している。Fountain et al.の図4を参照すると良い。該シミュレーションの目的は、高効率光電池装置を達成するために物質の使用を減少させることであり、3 μm GaAsナノワイヤーでの5%の充填率は物質の量について平坦状のGaAs層の150 nmと等価である。しかしながら、吸収向上の適切な比較は、3 μm GaAsナノワイヤーを3 μm 厚さのGaAsの平坦状の層と比較することである。この場合には、該平坦状GaAs 3 μm 層は、1.42 eVのバンドギャップ端部又は873 nmに到達するまでは1の吸収を有し、且つそれは急激に降下し、886 nmにおいては吸収係数は約241/cmであり、その場合に、例えば強い吸収性である855 nmにおいての約5917/cmと比較して弱い吸収性であり、及び3 μm 厚さの層の約7%が886 nmにおいて吸収され、855 nmにおいて約83%の吸収であり、且つ827 nmにおいて約99%の吸収である。3 μm GaAs層をFountain et al.の図4と比較すると、何ら吸収の向上は認められない。知覚しうる吸収向上無しでは、バルク層フォトダイオードのものを越えてナノワイヤーフォトダイオードを使用することの利点は無い。この場合には、800-850 nmにおけるデータ/遠隔通信用の3 μm GaAsナノワイヤーフォトダイオードよりも一層良いものではないとしても、バルク3 μm GaAsフォトダイオードはほぼ同程度に良く動作する。

【0197】

本書に記載する技術によれば、例えばSiにおける2 μm マイクロストラクチャ型穴(柱体及び/又は柱体と穴とすることも可能)が、例えば、5 Gb/s以上の高いデータレートのためデータ/遠隔通信のための800-900 nm波長において2 μm Siバルク層フォトダイオードよりも著しく一層吸収性であるように吸収(係数及び/又は長さ)の向上が提供される。

【0198】

図109(A)及び(B)は、幾つかの実施例に基づいて、マイクロストラクチャ型アレイに対してマクスウエルの式を使用したFDTDシミュレーションの結果を示しているグラフである。該穴アレイは、2000 nm周期の六角形格子を有しており且つ2 μm の「I」厚さのSiNIPの図92に類似したエピタキシャル構造を有しており且つ穴は該I層を貫通してエッチングされており且つ2つの穴直径(図106に示した如く)を有している。図109(A)は、1670及び1500 nmの穴直径を使用する曲線10910を含む4つのケースについて波長に対する吸収を示しており、一方、図109(B)は、1670及び1500 nmの穴直径を使用する曲線10910を含む該4つのケースの内の2つのケースについて誇張した尺度での波長に対する吸収を示している。該シミュレーションは、840乃至860 nmの波長に亘って10%未満のリップルを示しており、平均吸収は約90%である。更に、835-875 nm波長の間の領域は入射光子の80%以上の吸収を有することが可能である。1個を超える穴直径及び/又は周期の付加は該波長に対する吸収の曲線におけるリップルを減少させる。異なる共振モード、異なる穴直径及び/又は周期を有している異なる構造の固有モードの結合は、リップルを減少させ且つ一層広い波長範囲に亘っての吸収の向上を改善させ、且つ約2 μm 厚さのSi物質において850 nmにおいて80%よりも大きな量子効率に直接比例する高い吸収効率を達成することに貢献する。幾つかの場合において、850 nm $\pm$ 10 nmにおいて90%より大きなものを達成することが可能である。幾つかの場合において、850 nm $\pm$ 10 nmにおいて、70%、60%、50%又は40%より大きな量子効率を達成することが可能である。

【0199】

その他の穴直径も示されており、例えば1330及び1500 nm、1500及び1500 nm、1670及び1670 nmは全て周期が2000 nmであり且つリップルは他の場合よりも或る波長範囲において一層良好であり、従って、例えば850 nm±10 nm等の或る波長範囲に対してマイクロストラクチャ型PD/APDを設計する場合に、周期が2000 nmの六角形格子における該1500 nm穴寸法は、2 μ m Si「I」層においてリップルが10%未満で80%より大きな吸収を達成することが可能である。更に、1330 nm及び1500 nmの穴、及び、前述した如く、周期が2000 nmの六角形格子での1500及び1670 nm直径の穴もこの性能をほぼ達成することが可能である。従って、900乃至2000 nmの周期の範囲で600乃至1700 nmの穴寸法の範囲を使用して20 nm又はそれ以上のスペクトル範囲での特定の波長範囲を設計することが可能である。その他の直径及び周期を使用することも可能であり、記載した例は、穴直径と周期との或る組合せは、リップルが10%、20%、30%、40%、50%未満で吸収を向上させることが可能であることを示している。

【0200】

該穴直径は波長より大きいものとするか又は波長未満とすることが可能であり、且つ自由空間における該周期は波長よりも一層大きい。サブ波長周期も或る波長以上の周期と関連して使用することが可能である。

【0201】

この例は、20 nm及び幾つかの場合には10 nm及び幾つかの場合には40 nm以上の有用なスペクトル範囲で、5 Gb/s、及び幾つかの場合には10 Gb/s及び幾つかの場合には20 Gb/s、及び幾つかの場合には30-40 Gb/s以上を超えるデータレートで、Siにおける操作可能な850 nm PD/APDを設計するために、同じ周期で多様な穴直径を使用することが可能であることを示している。例えば880 nm波長、980 nm波長における吸収向上を最適化させるために、その他の穴直径及び周期を使用することが可能であり、その場合に、一般的には、波長が一層長くなるに従って穴直径及び/又は周期は対応して一層大きくなる。複数の穴直径及び/又は複数の周期を使用して該マイクロストラクチャ型シリコンPD/APDを一層長い波長へ拡張させることが可能であり、例えば、800から1000 nmの波長で向上される吸収は40%以上であり、且つ幾つかの場合においては、50%以上であり、且つ幾つかの場合においては、60%以上であり、且つ幾つかの場合においては、70%以上であり、且つ幾つかの場合においては80%以上であり、且つ或る場合には或る波長において90%以上である。一層長い波長の場合、例えば1550 nmでは、該穴及び周期は、例えば、1300 nm直径及び1500 nm直径で周期が2300及び2500 nmとすることが可能であり、その場合には周期が増加している。Ge・オン・Siにおける1550 nm波長に対するその他の穴直径/周期は、例えば、2300/3100 (nm単位)、2000/3100 (nm単位)とすることが可能であり、その場合には直径と周期の両方が増加している。

【0202】

更に、吸収向上のために山形又は「V」形状の穴等のその他の形状を使用することも可能である。その他の形状は、「X」形状、矩形状、三角形状、多角形状、及び/又は所望の吸収向上及びスペクトル幅及び分極感度を達成するための複数の形状の任意の組合せとすることが可能である。

【0203】

図110は、幾つかの実施例に基づいて、異なる穴直径と格子周期とを有するマイクロストラクチャ型フォトダイオード/アバランシェフォトダイオードに対しての波長に対する吸収のプロットを示している。シミュレーションしたMS-PD/APDは正方形格子を有しておりフォトンが上部表面か又は底部表面のいずれかから入射していた。吸収層はGeで約2 μ mの厚さである。該構造は図82Aに示したものと同様である。該波長に対する吸収の曲線において、例えば曲線11010で表されている周期が2000 nmで穴直径が1500 nmのマイクロストラクチャは、1500 nmから1650 nmへの波長

範囲での入射光子の良好な吸収特性を示している。該波長に対する吸収の曲線の中で、例えば、曲線11012によって表される周期3000 nmで穴直径2250 nmのマイクロストラクチャは、例えば、1650から1700 nmへの波長範囲で入射光子に関して良好な吸収特性を示している。これら2つの穴直径及び格子の組合せは1500から1700 nmへの波長範囲に対して60%よりも良い吸収となる場合がある。例えば、50%よりも良い。幾つかの場合においては40%よりも良い、及び幾つかの場合においては30%よりも良い等の良好な吸収特性を達成するために、穴直径/周期のその他の組合せを使用することも可能である。或る波長においては、80%よりも良いものを達成することが可能であり、例えば、1550 nm波長±10 nm以上である。更に、1669 nmも80%吸収効率±波長における数ナノメートルよりも良いものを達成することが可能である。1875 nm/2500 nmのその他の穴直径/周期も示されており且つ曲線11014で表されている。

【0204】

或る場合においては、穴直径は吸収されるべく該マイクロストラクチャ型PD/APDへ入射する光の波長よりも一層大きいものとすることが可能であり、且つ、幾つかの場合においては、該穴の直径は入射する光子の波長とほぼ同じとすることが可能であり、且つ幾つかの場合には、該穴の直径は入射する光子の波長よりも小さいものとすることが可能である。同じことが格子の周期についても言うことが出来、その場合に、該周期は検知されるべき光の入射波長よりも一層小さいか、ほぼ同じであるか、及び/又は一層大きいものとすることが可能である。

【0205】

図111A及び111Bは、幾つかの実施例に基づいて、図82Aに示した構造のFDTD方法を使用したシミュレーションを示しており、その場合に、2つの格子及び2つの異なる穴直径を使用している。図111Aは穴パターンを示しており、そこでは1500 nmの穴直径D1を有する六角形格子が中心において2250 nmのD2と4つの角部においてD1とを有する正方形格子とが結合されている。D1穴は水平方向に3 µm (d2 = 3 µm) だけ且つ垂直方向に約3.46 µmだけ離隔されている。該六角形格子は周期が2 µmである (d1 = 2 µm)。図111Bは波長に対する吸収のプロットを示している。該2つの格子で2つの異なる穴直径のケース (曲線11110) は、或る幾つかの波長において、吸収が単一格子/穴のマイクロストラクチャ型PD/APDのものよりも一層良好であることを示していることを見る事が可能である。例えば、約1570 nm乃至1600 nm、即ちデータ/遠隔通信波長のL帯域、において、曲線11110はかなり一層良好な吸収を示している。このことは、例えば、1500 nmの穴直径での2 µm周期 (曲線11112) と2250 nmの穴直径での2 µm周期 (曲線11114) とを有する正方形格子と比較される。この結果は、穴直径と周期との異なる組合せで、吸収応答はより少ない共振及び/又はよりシャープでない共振を有することが可能であり且つ又ある波長範囲において吸収応答を最適に調整することが可能であることを示しているだけである。これは単に一つの例であり、所望の量子効率、分極感度、非感受性、波長選択性及び/又は非選択性、例えば、ブロードバンド、リップル/共振減少等を得るために、格子、周期、穴直径及び形状のその他の組合せをシミュレーションすることが可能である。例えば、直径又は最小直径は100 nmから3000 nmの範囲にわたることが可能であり、且つ該周期及び/又は複数の周期は150 nmから4000 nmの範囲にわたることが可能である。更に、穴パターンは格子ではない場合もあり、例えば複数の穴が非周期的に分布されたり、及び/又は複数の穴の間の間隔がチャープされる場合がある。更に、穴のパターンは周期的である必要が無い場合があるが、該パターンは周期的であるか又は非周期的とすることが可能である。複数の穴をランダムに又は擬似ランダムに分布させることが可能であり、且つ穴直径は周期的、非周期的な態様、ランダムな態様、又は擬似ランダムな態様で変化することが可能である。更に、例えば、周期が同じか、殆ど同じか、或る周期において穴の直径未満である場合には、複数の穴は少なくとも一点で接続させることが可能である。穴のアレイは複数の周期を有することが可能であり、且つ少なくとも

一つの周期は穴が接触するか及び／又はオーバーラップするようにすることが可能である。

【0206】

本書に記載する技術に従って共振セルを隣接する隣の共振セルとの結合を使用して、吸収応答の平滑化が達成され、そのことは単一の共振器を有するのみであり且つその波長に対する吸収においてシャープな共振動作を示す既存の共振フォトダイオードと対比される。本書に記載する技術に基づく共振セルの集団は、制御されたリップルと波長範囲とを有する一層調節された吸収応答となる。更に、本書に記載する技術は、特定の波長において一層最適なPD/APD性能のために特定の波長において特定の吸収特性を調節するために使用することが可能である。

【0207】

更に、吸収向上プロセスに参画することの無いその他のマイクロストラクチャ／ナノストラクチャを使用して反射を減少させることが可能であり、例えば、数十nm乃至数百nmの範囲の寸法（直径等）の表面上のサブ波長の穴又はピット等であり、その場合は、その深さは数十nm乃至数百nm又はそれ以上の範囲とすることが可能である。

【0208】

図112は、幾つかの実施例に基づいて、同じ周期の2つの六角形格子が結合され且つ互いにインターレースされている別の格子構造を示している概略図である。該パターンは同一又は異なる直径の穴を使用することが可能である。図示した如く、該パターンは2つの異なる直径を有しており、例えば、その周期は2000nmとすることが可能であり、且つD1は1500nmとすることが可能であり且つD2は700nmとすることが可能である。周期及び直径のその他の組合せも可能であり、且つ吸収特性、従って入射光子波長に対する量子効率、及び光学的データ／遠隔通信目的に対して吸収特性が許容可能である波長スパンを調節するため、及びその特定の一つ又は複数の光学システムに対するいかなる特定の適用条件を満足させるために使用される。

【0209】

2つの六角形格子の点線によって示した如き単位セルは互いにオーバーラップしており、従ってそれらの固有モードも互いにオーバーラップし、そのことは特定の波長範囲においての吸収特性のリップルを更に減少させることが可能であり且つ該吸収特性におけるリップルが減少される波長範囲を拡張させることも可能である。或る波長範囲内においての吸収特性におけるシャープな変化はフォトダイオード／アバランシェフォトダイオードにおいて望ましいものではない。何故ならば、例えば、入ってくる光学信号波長におけるドリフト及び／又は温度に関してのフォトダイオード吸収特性のドリフトは光学から電気への信号変換において著しい変化をもたらす場合があるからである。5%未満の変化が好適であり、且つ幾つかのその他の場合においては、2nm、4nm、10nm、20nm、40nm、60nm、100nm、又は250nmの或る波長範囲内において10%、20%、30%、40%又は50%未満であることが好適である。

【0210】

図113は、6個の単位セルを有している六角形格子を示しており、各セルはその自身の固有モードを有しており、その場合にいかなるフィールド伝播／分布はその固有モードの拡張である場合がある。各セルの固有モードは隣接セルの固有モードと結合させることが可能であり、それにより複合結合型スーパーモードが形成され、そのことは、単なる観測化の目的のためだけであるが、複数の振子からなる2Dアレイのカップリングとして考えることが可能であり、その場合に、各振子が弱いスプリング（該弱いスプリングは機械的カップリング機構である）を介してその隣接する全ての振子に接続されているこの大量に結合された2Dアレイの振子の応答即ち運動は非常に複雑であり且つ単一の振子の単純な振動運動ではない。該カップリングに加えて、第2の入れ子型の六角形格子を図112における如くに付加させることが可能である。更に、円形状又は任意の形状で且つ任意の深さのもので且つ任意の直径のものであり該パラメータの内のいずれもが複数の値を有することが可能な穴を該セル内及び／又は隣接するセルの境界に付加させること

が可能であり、そのことは該セルの固有モード及び隣接するセルの固有モードとのその結合に影響を与えることが可能である。例えば、説明の便宜上、直径 X の複数の穴を図示した如くに付加させることが可能であり、その場合に X は単一又は複数の値を有することが可能であり且つ該穴は Si 又は Ge 表面において及び該吸収層内に部分的に又は完全にエッチングさせることが可能である。このことは、単に該表面上だけで該吸収層を侵入するものではないものとするのも可能である。幾つかの実施例によれば、該穴は該吸収層内に部分的に又は完全にエッチングさせることが可能である。

【0211】

複雑な定在波即ちスーパー固有モードとなる該セルのカップリングは、吸収応答（量子効率に比例）がシャープな応答特徴を有している従来既知の構造における如き共振応答などの単一共振器のものと比較して、一層滑らかな吸収対波長応答を与えることが可能である。

【0212】

図114は、幾つかの実施例に基づいて、バレイとテクスチャー表面とを有する $SiNIP$ マイクロストラクチャ型フォトダイオードを示している。テクスチャー表面11440は上部表面上及び／又は穴11422自身内とすることが可能である。テクスチャー付けは垂直からずれた角度において行うことが可能であり、その場合に基板をドライエッチングビーム（方向）に関して傾斜した状態で回転させる（又は静止）ことが可能であり、且つテクスチャーは、例えば、側壁上に部分的にさせることが可能である。幾つかの実施例によれば、テクスチャー11440は入射照射の反射を減少させる。何故ならば、光学的通信リンクにおいて、光学的供給源へ反射して戻される光学信号は望ましいものではなく且つデータ通信システムの信号対ノイズの劣化を発生させる場合がある。マスキングを行うか又は行うこと無しに半導体表面上でドライエッチを実施するブラックシリコン等のテクスチャー付けは光子をトラップし反射を減少させることが可能なナノ構造体の森を発生させることが可能である。テクスチャリングが無い場合には、反射は10%未満であり且ついくつかの場合においては5%未満であり且つ幾つかの場合においては2%未満であり、そのことは、例えば、図39におけるような波長に対する吸収のプロットにおいてみることが可能であり、その場合に、吸収は或る波長において90-95%よりも大きい。 $1 = T + R + A$ の式から、尚 T は透過光であり、 R は反射光であり、 A は吸収光である。 $A = 90 - 95\%$ の場合には、 $T + R$ は5-10%である。従って、 R は10%以下であり、且つ幾つかの場合には、5%以下である。半導体表面にテクスチャーを付加すると、反射を或る波長において1%未満に更に減少させることが可能である。更に、光学信号は垂直からずれた或る角度でマイクロストラクチャ型 PD/APD 上に入射することが可能であり、且つ光学データ通信チャンネル内へ反射して戻ることを更に減少させることが可能である。

【0213】

図115は、波長に対しての Si 及び Ge の吸収係数を示したグラフであり、例えば、http://www.silvaco.com/tech_lib_TCAD/simulationstandard/2010/apr_may_jun/a1/a1.htmlの図6を参照すると良く、それを引用により本書に取り込む。 Si の場合は850nmにおいて且つ Ge の場合には1550nmにおいて、両者は約300/cm未満の吸収係数を有している。この弱い吸収は、例えば10Gb/s帯域幅を超えるデータレートに対して典型的に約2 μm の吸収厚さを有している高速フォトダイオード及び／又はアバランシェフォトダイオードに対して不良な量子効率とさせる。このことは、例えば、 Si の場合は850nmの波長で Ge の場合は1550nmの波長に対して、例えば5Gb/sのデータレートを越える高速のフォトダイオードが現在市販されていない理由の一つである。

【0214】

図116は、幾つかの実施例に基づいて、マイクロストラクチャ型穴アレイに起因する Ge の向上された実効吸収係数を示しているグラフである。曲線11610は、 Ge の2 μm 厚さの層に対して1、25 μm の穴直径で1、65 μm の周期を有する六角形格子で

のGeに対する向上された吸収係数を示している。比較のために、曲線11612はバルクGe（マイクロストラクチャ型穴無し）の吸収係数を示している。幾つかの実施例によれば、その他のマイクロストラクチャも或る波長帯域に対して最適化させることが可能な向上された実効吸収係数を与えることが可能である。例えば、該マイクロストラクチャは穴又は柱体とすることが可能であり、その間隙は周期的又は非周期的とすることが可能であり、該穴又は柱体は単一又は複数の直径を有することが可能であり、且つその形状は円形状又は非円形状とすることが可能である。先に示した如く、吸収は吸収係数と吸収長との積である。従って、吸収係数をバルク物質の吸収係数（Geの場合は曲線11612）として維持しながら、吸収長を向上された実効吸収長とさせることが可能であり、即ち、物理的吸収長よりも5、10、20又はそれ以上一層長いものとさせることが可能である。図116から理解される如く、向上された実効吸収係数は、多くの波長範囲において、Geにおけるバルク吸収係数よりも10倍を超えて一層大きい。マイクロストラクチャに起因するGeにおける向上された実効吸収係数は、30%より大きな、40%より大きな、50%より大きな、60%より大きな、70%より大きな、80%より大きな、90%知より大きな量子効率（吸収に直接比例する）で、典型的に、1550nm波長及び一層長い波長においての吸収長が約 $2\mu\text{m}$ 以下である場合には、高速PD/APDの開発を可能とさせる。この様な物質、吸収長、波長、データレート、及び量子効率の組合せはSiでもGeでも市販されていることが既知ではない。同じことは、例えば、5、10、20Gb/s及びそれより一層早いデータレートに対して吸収長が典型的に約 $2\mu\text{m}$ 以下である場合の高データレート帯域幅において且つ805nm及びそれより長い波長範囲においての動作のためのSiマイクロストラクチャ型PD/APDについても言うことが可能である。

【0215】

更に、マイクロストラクチャは単一の要素又はセル及び／又は複数の要素又はセルから構成することが可能であり、且つ線形光学フィールド効果、非線形光学フィールド効果、結合モード効果、及び／又は遅波効果の結果である場合がある向上された実効吸収及び／又は向上された実効吸収長を有することが可能である。

【0216】

マイクロストラクチャを使用する吸収係数及び／又は吸収長の向上は、吸収係数が一層弱くなる帯域端部においてIII-V物質、GaAs、InP、GaN等のその他の物質の動作波長を拡張させるために使用することも可能である。例えば、Slawomir S. Piatek、http://www.hamanatsu.com/us/en/community/optical_sensors/tutorials/physics_of_mppc/indexx.html?utm_source=googleplus&utm_medium=social&utm_campaign=hc-socialにおける図3を参照すると良く、それは1.6 μm 波長の近傍におけるInGaAsに対するものであり、又それを引用により本書に取りこむ。幾つかの実施例によれば、マイクロストラクチャは1.6 μm 近く及びそれより長い動作波長を拡張させるために使用することが可能である。

【0217】

更に、吸収の向上のためのマイクロストラクチャの使用は、例えば非晶質Si等の非晶質物質へ適用することも可能であり且つ又ポリマー、セラミックス、グラフェン、合金及び酸化物等のその他の物質へ適用することも可能である。更に、音響、マイクロ波、UV、X線、及び圧力波等のその他のエネルギー伝播形式を一つの形式のエネルギーから別の形式へ変換させることが可能である。例えば、ピエゾ電気セラミック及び／又は結晶上の略音響波長程度の寸法の構造は、例えば、音響エネルギーから電氣的エネルギーへの変換を向上させることが可能である。略音響波長の寸法の構造を使用することは音響吸収を向上させることが可能であり、そのことは、例えば、一層薄いピエゾ電気物質とさせることが可能であり、更にそのことは、例えば、一層高い音響周波数応答を有することを可能とさせる。

【0218】

図117は、幾つかの実施例に基づいて、Siマイクロストラクチャ型PD/APDの

向上された吸収を示しているグラフである。シミュレーションしたMS-PD/APDは六角形格子穴アレイと、2000nmの周期と、1500nmの直径と、垂直から、例えば、10、20、40度ずれて入射する光子とを有している。図39は、光子が表面に対して垂直に入射する場合の同様の構造に対しての波長に対する向上された吸収のシミュレーションを示している。理解されるように、垂直から10度ずれた光子は850nmの波長においての吸収を著しく変化させるものではなく、該吸収は未だに90%よりも一層大きい。40度において、850nmにおける吸収は未だに90%を越えているが、20度において、吸収は850nmにおいて85%へ減少するようである。全体的に、或る波長においては、マイクロストラクチャに入射する光子の入射角度における変化は、例えば、0-40度の角度範囲にわたって10%未満の吸収変化を有することが可能である。或る波長範囲において穴直径、周期、非周期的マイクロストラクチャ、を最適化すると、入射光子の入射角度に関しての量子効率（吸収に直接比例する）における変化は10%未満とさせることが可能であり、且つ或る場合には、5%未満、且つ或る場合には、3%未満とさせることが可能である。この特徴はレーザー供給源へ向かって戻される反射光を最小とさせるために重要であり、該レーザー供給源は、オプティカルファイバー及び／又は自由空間及び／又は光学導波路における送信のために電気信号を光学信号へ変換させるために光学変調器が使用される場合に該光学信号を送信するためのデータレートにおいて直接的に又は間接的に変調される。電気信号から光学信号への変換器として発光ダイオード等のレーザーではない供給源を使用することは、該光学供給源へ向かって戻される反射パワーの条件を低下させることとなる。何故ならば、LEDはコヒーレント性がより低く及び／又はインコヒーレントな光学供給源だからであり、且つ同じ波長における反射は電気信号から光学信号への変換器として完全性においての崩壊の発生はより少ない。

【0219】

本特許出願は装置の性質及び動作を説明する上で或る理論に言及しているが、これらの理論は現在の理解に基づくものであって、たとえ将来の進展によりその理論が正しくないものであると証明されたとしても、ここに開示されている装置の実際の動作に影響を与えるものではないことは明らかである。本特許明細書は、又、パラメータの数値範囲に言及しており、この様な範囲からの実質的ではない逸れはここに開示された進歩の精神内のものであることを理解すべきである。

【0220】

装置を図示している図面は縮尺通りのものではなく幾分理想化されており、例えば直線は尖った角部等であり、一方、実際の装置はそれほど直線的ではないか又は滑らかなものではない壁や幾分丸められている角部を有している場合があり且つ蓋然性があることを理解すべきである。実際に、処理パラメータに依存して、マイクロストラクチャにおける穴又は柱体の壁などの壁は不均一で且つ窪みやへこみ等の表面特徴を具備している粗い表面を有している蓋然性があり、そのことは実際に不所望な反射の減少等の効果を奏することに寄与する場合がある。

【0221】

光の検知及び／又は信号処理及びディストリビューション集積回路用の半導体層は、気相エピタキシー、化学蒸着、プラズマエンハンス化学蒸着、原子層付着、分子ビームエピタキシーなど、及び／又は、例えば、選択的領域エピタキシー、選択的領域エピタキシャルラテラルオーバーエッチ、エピタキシャルラテラル過剰成長、ヘテロエピタキシー、ウェハーボンディング、エピタキシャルリフトオフプロセス、及び成長、ボンディング、リフトオフプロセスの任意の組合せ等の技術を使用してエピタキシャル的に成長させることが可能である。該半導体層に対する好適なプロセスは気相エピタキシー又は化学蒸着である。

【0222】

更に、該マイクロストラクチャ穴は吸収用の高電界「I」領域においてのみとすることが可能であり且つ必ずしも該PD/APDのN及びP領域内へ及び／又はそれを貫通して

延在するものではない。該穴はその全長にわたってオーバーラップすることが可能であり及び／又は隣接する穴は該穴の長さに沿って部分的にオーバーラップすることが可能である。

【0223】

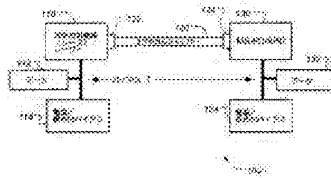
P、I及びN領域のドーピングは、しばしば、エピタキシャル成長期間中のドーパントの拡散に一部起因して異なるドーピングレベル領域の間で漸次的な遷移を有している。高ドーピングから低ドーピングへの遷移は、ドーパントタイプ、ドーピングレベル、成長温度及びエピタキシャル付着方法に依存して、1乃至1000nm又はそれ以上の距離にわたって発生する場合がある。PIN構造は、しばしば、P+PP-I NN+であり、その場合に、P及びP-及びN及びN-は遷移領域であり且つ非常に狭い遷移領域が望ましい。

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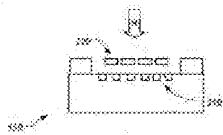
【0224】

以上明確性の目的のために幾らか詳細に説明したが、その原理から逸脱すること無しに或る変更及び修正を行うことが可能であることは明らかである。注意すべきことであるが、本書に記載したプロセス及び装置の両方を実施する場合に多くの代替的方法がある。従って、本実施例は例示的なものであって制限的なものではないとして考えるべきであり、且つ本書に記載した業績の内容は本書に記載されている詳細に制限されるべきものではなく、特許請求の範囲及びその均等物内において修正することが可能なものである。

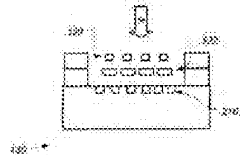
【図1】



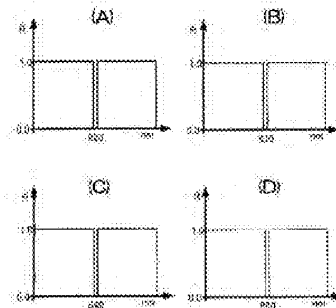
【図2】



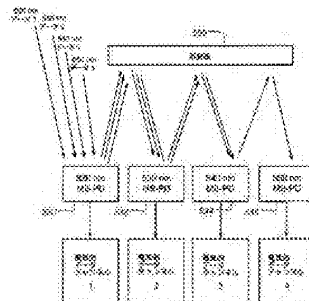
【図3】



【図4】

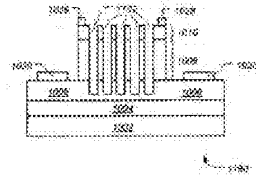


【図5】

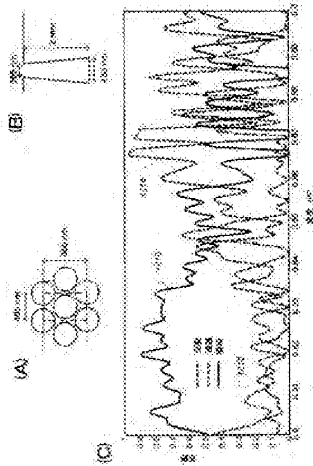


40

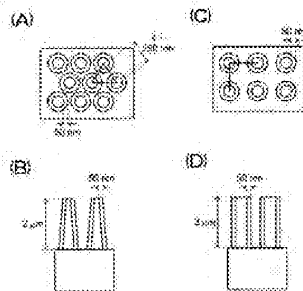
【例 1-1】



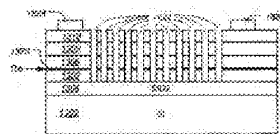
【X : Z】



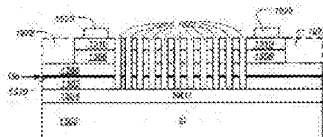
【 17 】



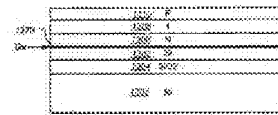
【例 18】



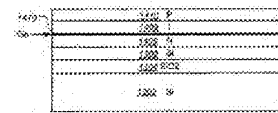
【圖 10】



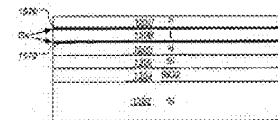
【例 1-3】



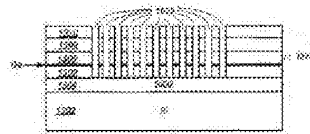
【例 1-4】



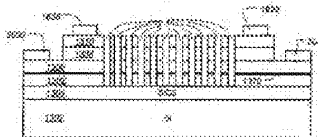
【例 1.5】



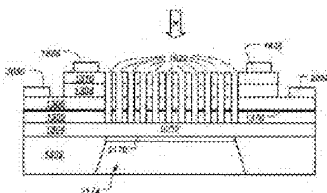
【例 1-6】



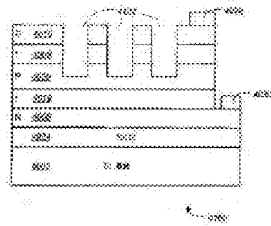
【图 20】



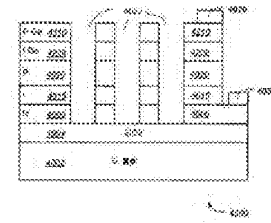
【图 2-1】



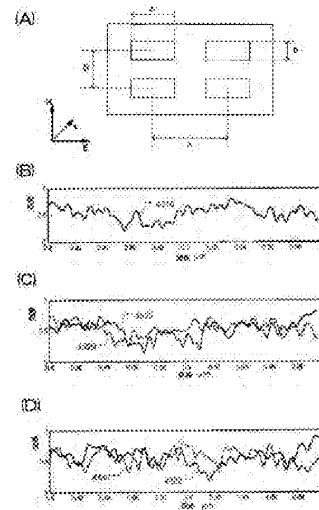
【例 4-1】



【例 4-2】



【例 4-3】



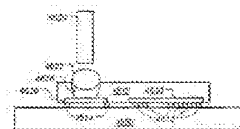
【例 4-4】



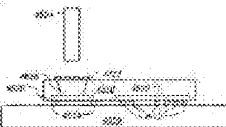
【 4 5 】



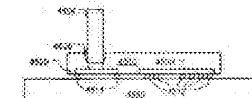
【X 4 6】



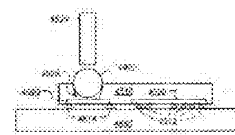
【例 4-7】



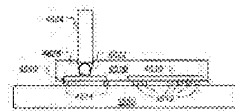
【例 4-8】



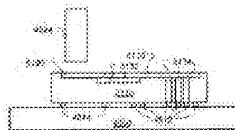
【例49】



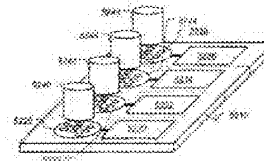
【250】



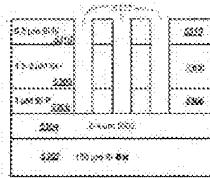
【例 5-1】



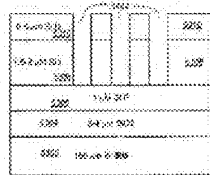
【例 5-2】



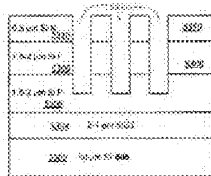
【図 5.3】



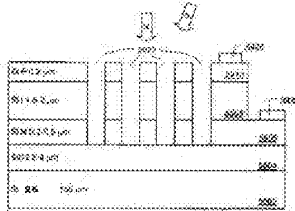
【図 5.4】



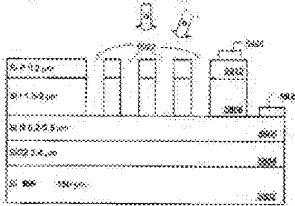
【図 5.5】



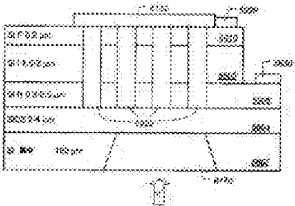
【図 5.9】



【図 6.0】



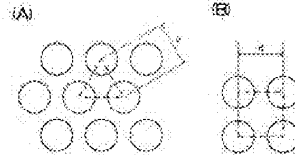
【図 6.1】



【図 5.6】

Layer	1050-1060 nm	1060-1070 nm	1070-1080 nm	1080-1090 nm	1090-1100 nm
10	1050-1060 nm	1060-1070 nm	1070-1080 nm	1080-1090 nm	1090-1100 nm
20	1050-1060 nm	1060-1070 nm	1070-1080 nm	1080-1090 nm	1090-1100 nm
30	1050-1060 nm	1060-1070 nm	1070-1080 nm	1080-1090 nm	1090-1100 nm
40	1050-1060 nm	1060-1070 nm	1070-1080 nm	1080-1090 nm	1090-1100 nm
50	1050-1060 nm	1060-1070 nm	1070-1080 nm	1080-1090 nm	1090-1100 nm
60	1050-1060 nm	1060-1070 nm	1070-1080 nm	1080-1090 nm	1090-1100 nm
70	1050-1060 nm	1060-1070 nm	1070-1080 nm	1080-1090 nm	1090-1100 nm
80	1050-1060 nm	1060-1070 nm	1070-1080 nm	1080-1090 nm	1090-1100 nm
90	1050-1060 nm	1060-1070 nm	1070-1080 nm	1080-1090 nm	1090-1100 nm

【図 5.7】



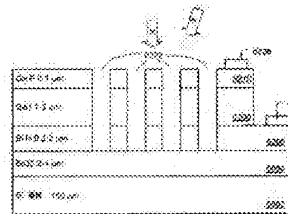
【図 5.8】

1050-1060 nm	1050-1060 nm
1060-1070 nm	1060-1070 nm
1070-1080 nm	1070-1080 nm
1080-1090 nm	1080-1090 nm
1090-1100 nm	1090-1100 nm
1100-1110 nm	1100-1110 nm
1110-1120 nm	1110-1120 nm
1120-1130 nm	1120-1130 nm
1130-1140 nm	1130-1140 nm
1140-1150 nm	1140-1150 nm

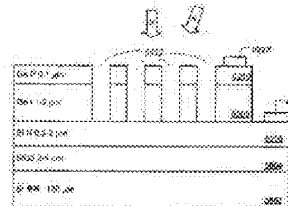
【図 6.2】

1050-1060 nm	1050-1060 nm
1060-1070 nm	1060-1070 nm
1070-1080 nm	1070-1080 nm
1080-1090 nm	1080-1090 nm
1090-1100 nm	1090-1100 nm
1100-1110 nm	1100-1110 nm
1110-1120 nm	1110-1120 nm
1120-1130 nm	1120-1130 nm
1130-1140 nm	1130-1140 nm
1140-1150 nm	1140-1150 nm

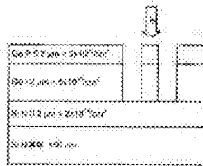
【図 6.3】



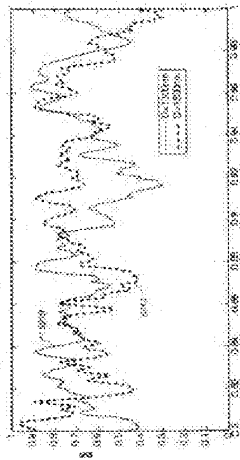
【図 6.4】



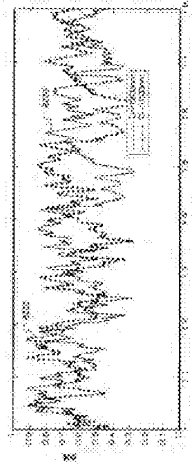
【図 8 2 A】



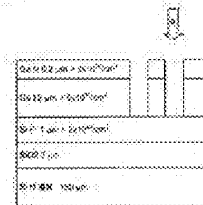
【図 8 2 B】



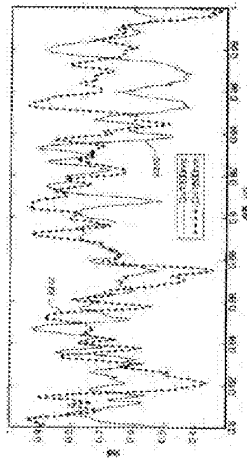
【図 8 2 C】



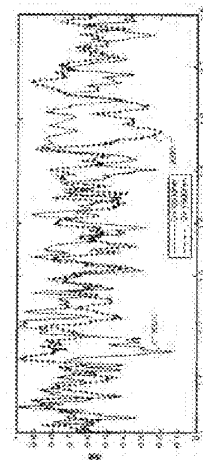
【図 8 3 A】



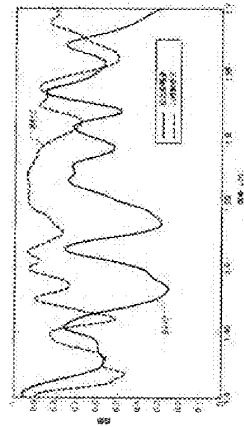
【図 8 3 B】



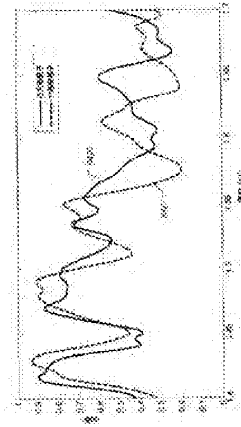
【図 8 3 C】



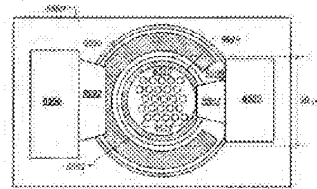
【図 8 4 A】



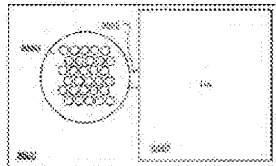
【図 8 4 B】



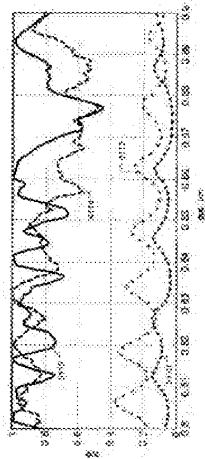
【図 8 5】



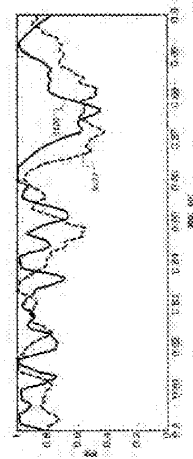
【図 8 6】



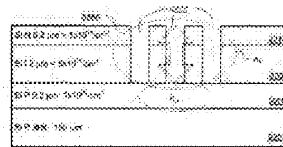
【図 9 1 A】



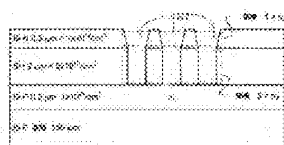
【図 9 1 B】



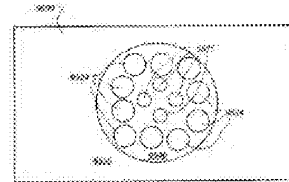
【図 9 2】



【図 9 3】



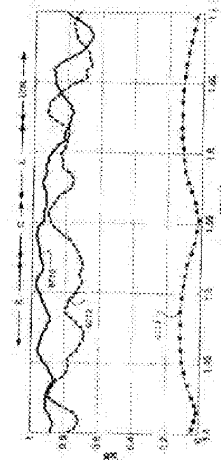
【図 9 6】



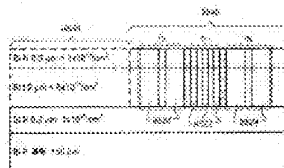
【図 9 4】



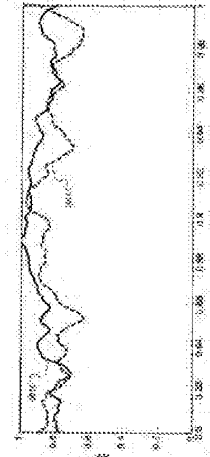
【図 9 7 A】



【図 9 5】



【例 9-8】

[illegible]

【例 103】

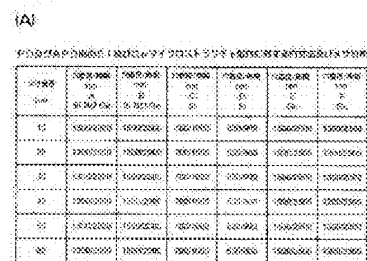
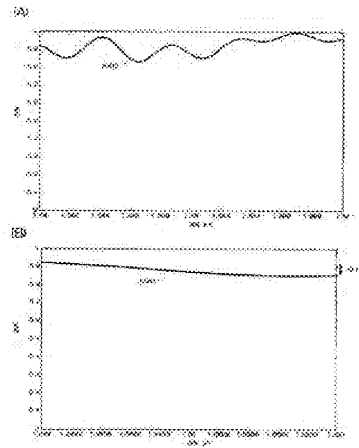
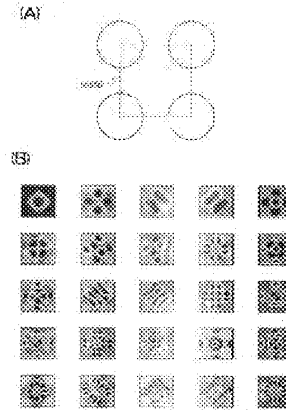


Figure 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 100 with a top layer 101. A layer 102 is formed on top of layer 101. Layer 102 is divided into a central region 102a and two side regions 102b. A gate stack 103 is formed on top of region 102a. Two side gate stacks 104 are formed on top of regions 102b. The device is surrounded by a passivation layer 105. Labels 100, 101, 102, 102a, 102b, 103, 104, 105 are used to identify the various components.

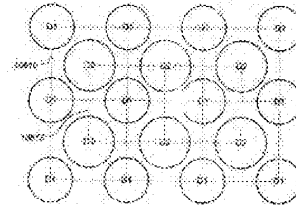
【図 1 0 4】



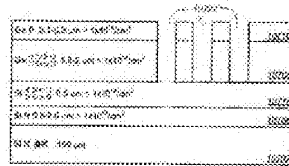
【図 1 0 5】



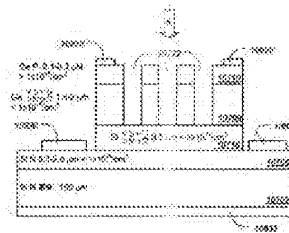
【図 1 0 6】



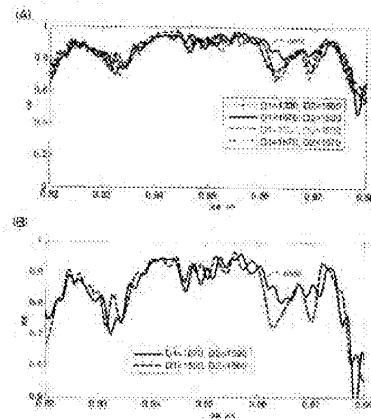
【図 1 0 7】



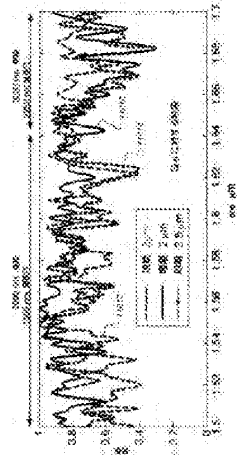
【図 1 0 8】



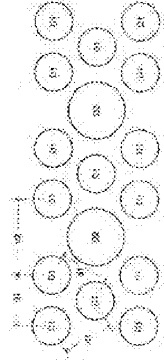
【図 1 0 9】



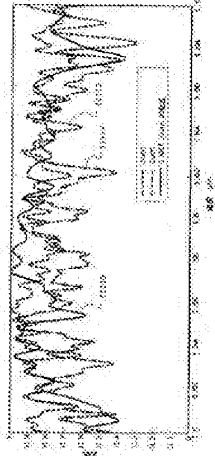
【図 110】



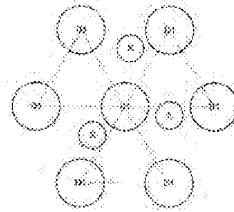
【図 111 A】



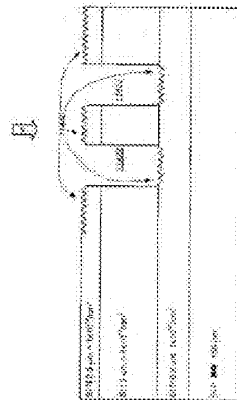
【図 111 B】



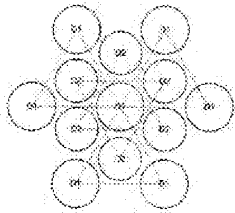
【図 113】



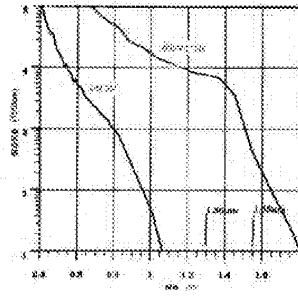
【図 114】



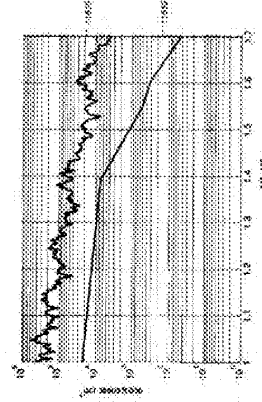
【図 112】



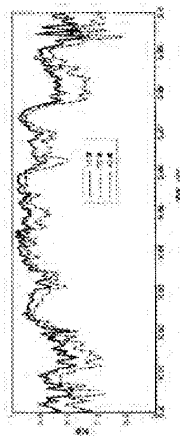
【図 115】



【図 116】



【図 117】



【國際調查報告】

INTERNATIONAL SEARCH REPORT		International application No. PCT/US 15/01120																					
A. CLASSIFICATION OF SUBJECT MATTER IPC(B) - H01L 27/148 (2018.01) CPC - H01L 27/14843; H01L 27/14865; H01L 27/148; H01L 27/15; B82Y 2000 According to International Patent Classification (IPC) or to both national classification and IPC																							
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC(B): H01L 27/148 (2018.01) CPC: H01L 27/14843; H01L 27/14865; H01L 27/148; H01L 27/15; B82Y 2000 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched IPC(B): H01L 27/148 (2018.01) CPC: H01L 27/14843; H01L 27/14865; H01L 27/148; H01L 27/15; B82Y 2000; USPC: 43848, 80, 83, 85 Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) Patbase, Google Web, Google Scholar Search terms used: Photon, absorption, photodetector, photodiode, data, communication, signal, hole, recess, aperture, nanoscale, bias, circuit, voltage, reverse, substrate, semiconductor, array, monolithic, integrated, processor, microprocessor, dsn, efficiency, rate, percentage, nm, nanometer																							
C. DOCUMENTS CONSIDERED TO BE RELEVANT <table border="1"> <thead> <tr> <th>Category*</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>Y - A</td> <td>US 7,977,837 B1 (YAP et al.) 12 July 2011 (12.07.2011), col 5, ln 15-33; col 5, ln 43-84, col 8, ln 42-48, ln 15; col 9, ln 30-67, Figures 14-15</td> <td>1-15, 18, 22, 24-26, 35-48, 51, 53-56, 58-60 17, 18, 20, 21, 23, 49, 50, 52, 57</td> </tr> <tr> <td>Y - A</td> <td>US 2012/0141122 A1 (CARUSONE et al.) 27 June 2012 (07.06.2012), para [0005], [0052]</td> <td>1-15, 18, 22, 24-26, 35-48, 51, 53-56, 58-60 17, 18, 20, 21, 23, 49, 50, 52</td> </tr> <tr> <td>Y - A</td> <td>US 2013/0206265 A1 (DAUTET et al.) 10 January 2013 (10.01.2013), para [0016], [0327], [0329], [0337], [0338]</td> <td>14, 15, 46, 47, 53-56, 58-60 57</td> </tr> <tr> <td>Y - A</td> <td>US 7,349,708 B1 (MASINI et al.) 24 March 2008 (04.03.2008), col 5, ln 20-27; col 7, ln 28-37; col 7, ln 54-58, ln 8</td> <td>18, 46, 70-80</td> </tr> <tr> <td>Y - A</td> <td>US 2014/0225083 A1 (KLEW et al.) 14 August 2014 (14.08.2014), para [0010], [0052], [0054], [0059], [0060]</td> <td>1-15, 18, 22, 24-26, 60 17, 18, 20, 21, 23</td> </tr> <tr> <td>Y</td> <td>WO 2013/180690 A1 (HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.) 05 December 2013 (05.12.2013), para [0011], [0042], [0044]</td> <td>13, 45</td> </tr> </tbody> </table>			Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	Y - A	US 7,977,837 B1 (YAP et al.) 12 July 2011 (12.07.2011), col 5, ln 15-33; col 5, ln 43-84, col 8, ln 42-48, ln 15; col 9, ln 30-67, Figures 14-15	1-15, 18, 22, 24-26, 35-48, 51, 53-56, 58-60 17, 18, 20, 21, 23, 49, 50, 52, 57	Y - A	US 2012/0141122 A1 (CARUSONE et al.) 27 June 2012 (07.06.2012), para [0005], [0052]	1-15, 18, 22, 24-26, 35-48, 51, 53-56, 58-60 17, 18, 20, 21, 23, 49, 50, 52	Y - A	US 2013/0206265 A1 (DAUTET et al.) 10 January 2013 (10.01.2013), para [0016], [0327], [0329], [0337], [0338]	14, 15, 46, 47, 53-56, 58-60 57	Y - A	US 7,349,708 B1 (MASINI et al.) 24 March 2008 (04.03.2008), col 5, ln 20-27; col 7, ln 28-37; col 7, ln 54-58, ln 8	18, 46, 70-80	Y - A	US 2014/0225083 A1 (KLEW et al.) 14 August 2014 (14.08.2014), para [0010], [0052], [0054], [0059], [0060]	1-15, 18, 22, 24-26, 60 17, 18, 20, 21, 23	Y	WO 2013/180690 A1 (HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.) 05 December 2013 (05.12.2013), para [0011], [0042], [0044]	13, 45
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.																					
Y - A	US 7,977,837 B1 (YAP et al.) 12 July 2011 (12.07.2011), col 5, ln 15-33; col 5, ln 43-84, col 8, ln 42-48, ln 15; col 9, ln 30-67, Figures 14-15	1-15, 18, 22, 24-26, 35-48, 51, 53-56, 58-60 17, 18, 20, 21, 23, 49, 50, 52, 57																					
Y - A	US 2012/0141122 A1 (CARUSONE et al.) 27 June 2012 (07.06.2012), para [0005], [0052]	1-15, 18, 22, 24-26, 35-48, 51, 53-56, 58-60 17, 18, 20, 21, 23, 49, 50, 52																					
Y - A	US 2013/0206265 A1 (DAUTET et al.) 10 January 2013 (10.01.2013), para [0016], [0327], [0329], [0337], [0338]	14, 15, 46, 47, 53-56, 58-60 57																					
Y - A	US 7,349,708 B1 (MASINI et al.) 24 March 2008 (04.03.2008), col 5, ln 20-27; col 7, ln 28-37; col 7, ln 54-58, ln 8	18, 46, 70-80																					
Y - A	US 2014/0225083 A1 (KLEW et al.) 14 August 2014 (14.08.2014), para [0010], [0052], [0054], [0059], [0060]	1-15, 18, 22, 24-26, 60 17, 18, 20, 21, 23																					
Y	WO 2013/180690 A1 (HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.) 05 December 2013 (05.12.2013), para [0011], [0042], [0044]	13, 45																					
☒ Further documents are listed in the continuation of Box C. ☐																							
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "Z" document member of the same patent family																							
Date of the actual completion of the international search 29 February 2016		Date of mailing of the international search report 11 MAR 2016																					
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No.: 571-273-8300		Authorized officer: Lee W. Young PCT No.: 15/01120-200 PCT Date: 2015-03-27																					

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP 15/01120

C (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014/0167107 A1 (YONEGA et al.) 18 June 2014 (19.06.2014) para [0066]	18, 61, 68
Y	JOSEPH et al., "26 Gbps 850 nm photodiode for emerging 100 Gb ethernet applications," SPIE Proceedings Vol. 8054, 04 May 2011, [04.05.2011], Abstract [online] <URL: http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1351039 >	26, 62-66
Y	DOSUNMUJ et al., "Germanium on double-SOI photodetectors for 1550 nm operation," Conference: Lasers and Electro-Optics Society, November 2003, [11.2003], pp. 2, 4-5, 6 [online] <URL: https://www.researchgate.net/publication/224745293 >	71-73, 77-80
Y	US 2014/0263975 A1 (NAGANO et al.) 18 September 2014 (18.09.2014), para [0015], [0054]	3
Y	US 2006/0186501 A1 (ISHIMURA) 24 August 2006 (24.08.2006), para [0010], [0036]	28, 81
Y	ACKERT, "10 Gbps silicon waveguide-integrated infrared avalanche photodiode," Optics Express, 12 August 2013, [12.08.2013], Abstract, pp. 19535 [online] <URL: <a >https:="" href="https://www.opticsexpress.net/view_article.cfm?getout=H06%3A%2F%2Fwww%2Eopenpublishing%2Eorg%2FDirectPDFAccess%2FD0C4EF6B-A4CA-4F6D-9BA8957C57E791AC_260182%2Fow-21-17-15533%2Epdf%3Fde%3D1%26d%3D260182%2Bseq%3D0%28mobile%3Dno&org=" view_article.cfm?getout="H06%3A%2F%2Fwww%2Eopenpublishing%2Eorg%2FDirectPDFAccess%2FD0C4EF6B-A4CA-4F6D-9BA8957C57E791AC_260182%2Fow-21-17-15533%2Epdf%3Fde%3D1%26d%3D260182%2Bseq%3D0%28mobile%3Dno&org=</a" www.opticsexpress.net="">>	26, 62
A	US 4,352,512 A (WALLER et al.) 29 September 1981 (29.09.1981), col 4, ln 12-15	17, 18, 49, 50

Form PCT/ISA/210 (continuation of second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 15/81428

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(3)(a) for the following reasons:

1. ☐ Claims Nos. _____
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos. _____
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos. _____
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional examination fees must be paid:

Group I: claims 1-26 and 35-80; drawn to an integrated detector/processor circuit for data communication and photodetector with microstructure-enhanced photoabsorption.

Group II: claims 27-34; drawn to an optical/electronic system.

The inventions listed as Groups I and II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

--please see continuation on extra page--

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos. _____.
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos. 1-26, 35-80.

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

Form PCT/ISA/210 (continuation of first sheet (2)) (January 2013)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 15/61120

Continuation of Box No. III - Observations where unity of invention is lacking

Special technical features:

Group I requires a photon absorbing region comprising a plurality of holes, not found in the other groups.

Group II requires a laser modulated at Gb/s rates of data to thereby generate the optical source signal carrying information at Gb/s rates; and an optical filter associated with the laser to receive the optical source signal, not found in the other groups.

Shared Features:

The only technical features shared by Groups I-II that would otherwise unify the groups are an integrated electronic processor circuit and a photodetector formed on a substrate.

However, these shared technical features do not represent a contribution over prior art, because the shared technical features are disclosed by US 2003/0039820 A1 to Vo-Oinh 27 March 2003 (97.03.3003), which discloses an integrated electronic processor circuit and a photodetector formed on a substrate (para [0020], [0073]). The integrated circuit detection system can include at least one photodetector. Photodetectors can be selected from photodiodes, avalanche photodiodes, phototransistors, photomultipliers, CCDs, CIDs and hybrid photomultipliers. Since the anode of the diode is the p-type substrate material, which is common to every circuit on the IC chip, only the cathode is available for monitoring the photocurrent and the photodiode is constrained to operate with a reverse bias.

As the shared technical features were known in the art at the time of the invention, they cannot be considered special technical features that would otherwise unify the groups.

Groups I and II therefore lack unity under PCT Rule 13 because they do not share a same or corresponding special technical feature.

フロントページの続き

(51)Int.Cl.			F I		テーマコード (参考)
G 0 1 J	3/36	(2006.01)	G 0 1 J	3/36	
H 0 1 L	27/144	(2006.01)	H 0 1 L	27/144	1

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 (32)優先日 平成27年4月27日(2015.4.27)
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 (31)優先権主張番号 62/154,675
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 (33)優先権主張国 米国(US)
 (31)優先権主張番号 62/157,876
 (32)優先日 平成27年5月6日(2015.5.6)
 (33)優先権主張国 米国(US)
 (31)優先権主張番号 62/171,915
 (32)優先日 平成27年6月5日(2015.6.5)
 (33)優先権主張国 米国(US)
 (31)優先権主張番号 62/174,498
 (32)優先日 平成27年6月11日(2015.6.11)
 (33)優先権主張国 米国(US)
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 (32)優先日 平成27年6月15日(2015.6.15)
 (33)優先権主張国 米国(US)
 (31)優先権主張番号 62/182,602
 (32)優先日 平成27年6月21日(2015.6.21)
 (33)優先権主張国 米国(US)
 (31)優先権主張番号 62/188,876
 (32)優先日 平成27年7月6日(2015.7.6)
 (33)優先権主張国 米国(US)
 (31)優先権主張番号 62/197,120
 (32)優先日 平成27年7月27日(2015.7.27)

(33)優先権主張国 米国(US)
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(81)指定国 AP(BW,CH,CM,KE,LR,LS,MW,MZ,NA,RW,SD,SL,ST,SZ,TZ,UG,ZM,ZW),EA(AM,AZ,BY,KG,KZ,RU,TJ,TN),EP(AL,AT,BE,BG,CH,CY,CZ,DE,DK,EE,ES,FI,FR,GB,GR,HR,HU,IE,IS,IT,LT,LU,LV,MC,MK,MT,NL,NO,PL,PT,RD,RS,SE,SI,SK,SM,TR),DA(BF,BJ,CF,CG,CI,CM,CA,CN,CQ,CW,KM,ML,MR,NE,SN,TD,TG),AE,AG,AL,AM,AQ,AT,AU,AZ,BA,BB,BG,BH,BN,BR,BW,BY,BZ,CA,CH,CL,CN,CO,CR,CU,CZ,DE,DK,DM,DO,DZ,EC,EE,EG,ES,FI,GB,GD,GE,GR,GM,GT,HK,HU,IE,IL,IN,IR,IS,JP,KE,KG,KN,KP,KR,KZ,LA,LC,LK,LI,LS,LU,LV,MA,MD,ME,MG,MK,MN,MW,MX,MY,MZ,NA,NG,NL,NO,NZ,OM,PA,PE,PG,PH,PL,PT,QA,RD,RS,RU,RW,SA,SC,SD,SE,SG,SK,SL,SM,ST,SV,SY,TH,TJ,TN,TN,TR,TT,TZ,UA,UG,US

(72)発明者 ワン、 シー—ピン
 アメリカ合衆国、 カリフォルニア 94022, ロス アルトス, サード ストリート 38, スイート 307

データベース(参考) 2C020 AA03 BA20 CB23 CB42 CB54 CC02 CC31 CC63 CB06 CD12
 CD24
 2C065 AB02 AB09 AB22 BA09 BA10 BA33 BA36 BB02 BB08 BB15
 BB25 BB27 BB28 BF08 DA05 DA13
 4B118 AA01 AB05 BA14 BA19 CA05 CB02 CB06 CA02 CA08 CD03
 CD16 BA31
 5F849 AA04 AA07 AB03 AB05 AB07 AE17 BA01 BA03 BA04 BB01
 CA02 CB06 CB10 CB11 CB14 CB20 DA03 DA28 DA44 EA13
 GA01 GA02 GA04 GA05 HA07 JA02 JA10 JA11 JA12 JA14
 JA19 KA20 LA01 LA09 XB01 XB05 XB37 XB38



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APPLICATION #
18/822,880

RECEIPT DATE / TIME
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ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68240468	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 6

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
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JPA02502326.pdf	13	Foreign Reference	715 KB
JapaneseOfficeActionWithTranslation2020-131831.pdf	21	Non Patent Literature	446 KB
JPA2018508970-.pdf	141	Foreign Reference	17822 KB
309-0015USCIPDIV_1449-Final.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	1010 KB
WO1989005043A1.pdf	20	Foreign Reference	942 KB

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WO1989005043A1.pdf	3D40088EC454A61274BE224417E066CB0F33BD728AAB609B7BBBEEBA3ACA9844EEC41A5FF0BF89326951FE0AA286AD9538DD039FC5027FD2ECD02EB2B804EF62

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	Filing Date		2024-09-03	
	First Named Inventor	Shih-Yuan WANG		
	Art Unit	2893		
	Examiner Name	EDUARDO A RODELA		
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Infrared radiation detection device

Abstract

translated from Japanese

(57) [Summary] This bulletin contains application data before electronic filing, so abstract data is not recorded

Classifications

⚡ H01L31/0046 Inorganic materials including, apart from doping materials or other impurities, only AHBV compounds including ternary or quaternary compounds, e.g. GaAlAs, InGaAs, InGaAsP

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JPH02502326A

Patent

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Other languages: Japanese

Inventor: アールグレン, ウィリアム・エル, シュルテ, エリク・グ・エフ

Worldwide applications

1988 [EP](#) [JP](#) [WO](#) [EP](#) [W](#)

Application JP1501415A events 📅

1988-10-28 Application filed by サイタ・パーソナル・リサーチ・センター

1990-07-26 Publication of JPH02502326A

1996-08-28 Application granted

1996-08-28 Publication of JP2502191B2

2011-08-28 Anticipated expiration

Status Expired - Lifetime

Info: Patent citations (10), Cited by (5), Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Claims (20)

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[Claims] (1) Readout and signal processing circuits are integrated, and silicon, gallium arsenide or a substrate formed of a material selected from the group consisting of or germanium, mercury/cadmium/tellurium, mercury/zinc/tellurium, mercury/cadmium/selenium mercury, zinc, selenium, mercury, cadmium, sulfur, mercury, zinc, sulfur, lead - Tin/tellurium, lead/tin/selenium, lead/tin/sulfur, indium/arsenic/anti mon, gallium indium antimony, or gallium antimony arsenic a first half grown on said substrate comprising a material selected from the group consisting of a conductor layer; a second semiconductor layer grown on the first semiconductor layer; the readout in the substrate in response to infrared radiation waves received by the first and second semiconductor layers; infrared radiation waves operable to transmit electrical signals to signal processing circuits. Monolithic structure for detection (2) a first passivation provided between the base and the first semiconductor layer; 2. The device of claim 1, further comprising a coating layer. (3) a second passivation layer provided between the first passivation layer and the first semiconductor layer; 3. The device of claim 2, comprising a passivation layer of. (4) The first and second passivation layers form the first semiconductor layer. 4. The apparatus of claim 3, including a plurality of nuclear windows operable to control. (5) The nucleation of the first semiconductor layer occurs only within the nucleation window. equipment. (6) a third semiconductor layer provided on the second semiconductor layer; The conductor layer reduces the surface recombination rate of free charge carriers in the second semiconductor layer. 5. The device of claim 4, wherein the device is operable to reduce (7) The first, second and third semiconductor layers are formed by metallic vapor phase epitaxy. 7. The device of claim 6, wherein the device has a length. (8) A layer of antireflection material provided on the third semiconductor layer. equipment. (9) Mercury/cadmium/tellurium, mercury/zinc/tellurium, mercury/cadmium/se Rhenium, mercury/zinc/selenium, mercury/cadmium/sulfur, mercury/zinc/sulfur From the group consisting of yellow, lead/tin/tellurium, lead/tin/selenium, lead/tin/sulfur first and second layers of semiconductor material formed from selected materials as an infrared radiation source; exposed to generating a photocurrent in the first and second layers of semiconductor material; The first and second semiconductor layers are grown thereon and are made of silicon, gallium arsenide or is installed in a substrate formed from a material selected from the group consisting of germanium, sensing the photocurrent by a readout and signal processing circuit How to detect external radiation. (10) the first semiconductor material layer; the second semiconductor material layer and the base 10. The method of claim 9, wherein comprises a monolithic structure. (11) The layer of the first semiconductor material is arranged on the substrate by a first passivation layer. 10. The method of claim 9, wherein the method is isolated from the body. (12) The first passivation layer is half-layered by a second passivation layer. 12. The method of claim 11, wherein the method is separate from the first layer of conductive material. (13) The first and second passivation layers are layers of the first semiconductor material. 13 The nuclear window of claim 12, comprising a plurality of nuclear windows operable to control the formation of the nuclear window. Method. (14) providing a layer of the third semiconductor material on the layer of the second semiconductor material. The surface recombination rate of free charge carriers in the layer of second semiconductor material by 10. The method of claim 9, including the additional step of reducing . (15) The first, second and third semiconductor layers are formed by metallic vapor phase epitaxy. 15. The method of claim 14, wherein: (16) an additional layer of antireflection material that allows infrared radiation to pass through the layer of antireflection material 16. The method of claim 9, comprising the steps of: (17) A readout and signal processing circuit is integrated, and the readout and signal processing circuit is integrated. a substrate formed of a material selected to optimize the properties of the circuit; a first layer grown on said substrate from a material selected to optimize infrared detection; a semiconductor layer of a plurality of passivations provided between the substrate and the layer of first semiconductor material; layer and in response to infrared radiation received by the first and second semiconductor layers. said first operable to transmit an electrical signal to a readout and signal processing circuit; a second semiconductor layer provided on the semiconductor layer; actuated to reduce the surface recombination rate of free charge carriers in the second semiconductor layer; a third semiconductor layer provided on the second semiconductor layer that can be provided on the third semiconductor layer, with a refractive index between the refractive index of the atmosphere and the third semiconductor layer; a monolithic structure for detecting infrared radiation waves comprising an anti-reflection coating having a array of. (18) The plurality

of passivation layers control the growth of the first semiconductor layer. 18. The array of claim 17, comprising a plurality of nuclear windows operable to. (19) One of the nuclear windows is connected to the first semiconductor layer and the readout and signal 19. The array of claim 18, wherein the array enables electrical coupling to and from processing circuitry. (20) The monolithic structure further includes the first and second semiconductor layers and the Contains ohmic contacts to allow electrical coupling to readout and signal processing circuits. 20. The array of claim 19.

Description

translated from Japanese

[Detailed description of the invention] Infrared radiation detection method and device 1. Field of invention The present invention relates to the field of infrared sensing, and in particular to methods and apparatus for detecting infrared radiation.

2. Description of conventional technology Basic infrared detectors have wavelengths from 1 to 30 μm for survey, target investigation and Often used in exploration and tracking imaging systems that detect the presence of electromagnetic radiation be done. These basic detectors to detect infrared radiation are triglycine Temperature sensation like phated and lanthanum-topped lead zirconate titanate crystals Responsive thermoelectric and ferroelectric materials are often used. Such crystals are momentarily in response to an incident infrared radiation wave that causes a potential drop across the attached electrodes. Indicates intermediate electrical polarization. Sulfidation where the resistance of the material changes as a function of the incident radiation Photoconductive materials such as lead and mercury, cadmium, and tellurium may be used.

Finally, the intrinsic band-to-band electron-hole excitation is proportional to the incident infrared flux. mercury, cadmium, tellurium, indium, anti Photovoltaic devices such as those constructed from mono or similar materials may be used.

Arrays of such elementary detectors are used to form thermal imaging systems. Good too. In real-time, A thermal imaging system with rotating rhythmic reflectors spans a one-dimensional array of elementary detectors. used to scan the radiation emitted by the source. basic detector When used in this way, the temporal output of the detector produces a two-dimensional representation of the image. may be used as such. Using either observation or scanning arrays in a two-dimensional detection array imaging system capable of A suitable readout such as a charge-coupled device ("CCD") It may be monitored by an integrated circuit. The output from the CCD is time delayed and can be processed by various techniques such as minute or parallel to serial scan conversion. , frame rate, signal-to-noise ratio, etc. , are selected according to system requirements. the Other reading devices may also be used.

Although the above detector structures are efficient, they generally have some manufacturing related it has some drawbacks. First, the detector and readout device are configured separately and then A number of such detector structures that are mechanically coupled are formed in a hybrid manner

Because the formation of hybrid structures involves additional processing steps, such structures Monolithic devices (i.e. the detector and readout and signal processing circuitry are in one material) The production efficiency tends to be lower compared to other systems (equipment formed in the system). difference Furthermore, there is a possibility that unintended defects may be induced during formation, reducing reliability and impairing properties. High potential. Monolithic detectors eliminate additional processing steps required for hybridization. avoid topography, but use the same material as the infrared detector for the signal processing circuitry. There is a need. This material (e.g. Hg, Cd, Te or InSb) is it is usually better than circuits formed from well-developed silicon or gallium arsenide. According to a preferred embodiment of the present invention, a low characteristic signal processing circuit detects infrared radiation. A method and apparatus are disclosed. The device has integrated readout and signal processing circuits including the base body. Substrate consists of silicon, gallium arsenide and germanium Formed from materials selected from the group. The first semiconductor layer is made of mercury and carbon. Domium/tellurium, mercury & zinc/tellurium, mercury & cadmium, selenium, mercury - Zinc/Selenium, Mercury/Cadmium/Sulfur, Mercury/Zinc/Sulfur, Lead/Tin/Te Lutu, lead, tin, selenium, lead, tin, sulfur, indium, arsenic, antimony, gas Glue consisting of lithium indium-antimony or gallium antimony arsenic A material selected from the loop is grown on the substrate. Is that the second semiconductor layer? are formed on the first semiconductor layer.

Brief description of the drawing Various advantages of the invention will become apparent to those skilled in the art from the following description and drawings. .

The drawing is a sectional view of a preferred embodiment of a device for detecting infrared radiation according to the invention. .

Description of the preferred embodiment According to a preferred embodiment of the invention, the structure 10 for detecting infrared radiation is indicated by 4 in the figure. Provided as shown. Structure 10 may be used as a single sensing element Alternatively, it may be part of a multi-element video device. Structure 10 is silicon, it includes a substrate 12 which may be formed from gallium arsenide or germanium. but it should be understood that other suitable materials may be used. The base 12 is , by reference numeral 14 which converts the output of the semiconductor layer described below into a usable form. including appropriate readout and signal processing circuitry as shown. Readout and signal processing circuits Route 14 is described by Blazer, N., herein referred to.

and Stehlae, R. ("Buffered Direct Injection of Photocurrents Into Charge-Coupled Device", IEEE Transactions on Electron Devices.

ED25, n, 2, p. 160, February 1978) You may do so. Any other suitable means of processing the output from the semiconductor layer may be used. You may be

A first passivation layer 16 is provided to control the electrical properties of the substrate surface. ing. The first passivation layer 16 has an optimal passivation shape for the substrate 12. selected from materials that provide a Such materials include SiO₂ or SiN. include.

However, it should be understood that other suitable materials may be used. Second A passivation layer 18 is deposited on the first passivation layer 16. No. The passivation layer 18 of No. 2 is made of a material suitable for the infrared active semiconductor layer described below. Provides an ossivation state and prevents nucleation of the infrared active semiconductor layer.

formed from one of a plurality of materials forming a deep surface. Such materials are SiO₂ or ZnS. However, other suitable materials may be used. should be understood. The first and second passivation layers 16 and 18 are It has an ohmic contact 20 and a plurality of nuclear windows 22-28. ohmic contact The child 20 includes a second semiconductor layer and a readout and signal processing circuit 14, which will be described below. Used to make electrical connections between The nuclear window 22 to 28 is the first half. Used to provide seed locations for the core of the conductor layer. Furthermore, the nuclear window 24 enabling electrical coupling between the first semiconductor layer and the readout and signal processing circuitry 14 .

Structure 10 includes a first semiconductor layer for generating a photocurrent in response to incident infrared radiation, 28 and a second semiconductor layer 30. First and second semiconductor layers 28 and 30 both include the base and collector layers of the Peter junction photodiode. first The semiconductor layer 28 is made of water having a stoichiometric relationship defined by Hg_x-xCl₂Te. It is composed of layers of silver, cadmium, and tellurium. The composition value of X is the first semiconductor layer 28 is selected to be sensitive to infrared radiation at a particular wavelength in the infrared spectrum. . For example, if the composition value of X is selected to be approximately 0.2, then the first semiconductor layer 28 has a cutoff of about 10 to 12 μm at the desired operating temperature (e.g. 77 degrees absolute). It is sensitive to long-wavelength infrared radiation waves that have long wavelengths.

However, the first semiconductor layer 28 is mercury/zinc/tellurium, mercury/cadmium/ selenium, mercury/cadmium/sulfur, mercury/zinc/sulfur, mercury/zinc/selenium lead, tin, tellurium, lead, tin, selenium, lead, tin, sulfur, indium, arsenic - Antimony, gallium indium antimony, or gallium antimony it should be understood that other suitable materials may also be included, such as be.

The second semiconductor layer 30 has a stoichiometric relationship defined by Hg, Te, and Cd. Contains layers of mercury, cadmium, and tellurium.

The composition value of y is selected to be larger than the composition value X of the first semiconductor layer 28, and is typically has a value of 0.3. However, any other suitable value of y may be selected or mercury, cadmium, tellurium, mercury, zinc, tellurium, mercury, cadmium, selenium um, mercury, zinc, selenium, mercury, cadmium, sulfur, mercury, zinc, sulfur, Lead/tin/tellurium, lead/tin/selenium, lead/tin/sulfur, indium/arsenic/anium Timon, gallium indium antimony or gallium antimony arsenic it should be understood that other suitable materials may be selected, including.

The first semiconductor layer 28 acts as a photodiode base layer while the second semiconductor layer 28 acts as a photodiode base layer. Body layer 30 acts as a photodiode collector layer. However, structure 10 The roles of the first and second semiconductor layers 28 and 30 are reversed to increase the collection efficiency of (i.e., the second semiconductor layer 30 becomes the base layer and the first semiconductor layer 30 layer 28 becomes the collector layer). In this case, the composition value of y is approximately 0.2, and the composition value of The closing price is approximately 0.3. However, generally the second semiconductor layer 30 has a narrow barrier. and the first semiconductor layer 28 is a wide bandgap material. . Layers 28 and 30 are doped to have a mixture of opposite types.

That is, the first semiconductor layer 28 is doped p-type, and the second semiconductor layer 28 is doped n-type, and vice versa. However, the same type of heterojunction has also been used Good things should be understood.

When a photon of light in the infrared spectrum is absorbed by device structure 10, an electric charge is generated. Child hole pairs are generated Before the electron-hole pair recombines, the first and second semiconductor When the junction between the body layers 28 and 30 is reached, the first and second semiconductor layers 2 The electric field at the junction between 8 and 30 moves electrons into the n-type semiconductor layer, The holes are moved into the p-type semiconductor layer. This electron hole movement causes the received photon to Generates a photocurrent proportional to the number.

sensing the photocurrent generated in the first and second semiconductor layers 28 and 30; To this end, substrate 12 further includes heavily doped regions 32 and 34. heavily The looped area 32 is connected to the readout and signal processing circuitry 14 through the nuclear window 24 and the first semiconductor layer 28 . Attached to nuclear window 24 The material to be used has a crystal structure and lattice constant similar to HgTe or the semiconductor layer 28. (i.e., HgSe, Hg S, PbTe.

PbSe, PbS, and Gray Sn can be selected instead). child This provides good ohmic contact between the heavily doped region 32 and the first semiconductor layer 28. I will provide a. Although the same material is deposited in nuclear windows 22 and 26 at the same time, , it is made with respect to the first semiconductor layer 28 only as a nucleation point and not as an ohmic contact. use Furthermore, the heavily doped region 34 is connected to the metallization layer 36 and the ohmic contact. 20 between the readout and signal processing circuit 14 and the second semiconductor layer 30. Provide a bond. Ohmic contacts 20 and 36 can be two different metals. , and the ohmic contact 20 makes good ohmic contact with the heavily doped region 34. metallization layer 36 is selected such as platinum for n-type and gold for p-type. is selected to form a good ohmic contact with the second semiconductor layer 30. metal The chemical layer 36 is also selected to be a material in which the nuclei of the first semiconductor layer 28 are suppressed. There must be.

If the second semiconductor layer 30 acts as the base of the photodiode, the second half Free charge carriers inside the conductor layer 30 are present at the interface with the second semiconductor layer 28. Diff towards them and recombine. As a result of this recombination, free charge carriers become The efficiency collected by passivation layer 16 is reduced second semiconductor layer in order to reduce the rate of recombination of free charge carriers in the second semiconductor layer 3 A third semiconductor layer 38 is provided when 0 acts as the base of a photodiode. It will be done. The third semiconductor layer 38 has H selected such that the composition value of 2 is larger than y Mercury and cadmium with the stoichiometric relationship defined by $g = \frac{1}{2}Cd \frac{1}{2}Te$ It may be formed from umQ tellurium. However, mercury, cadmium, tellurium , mercury/zinc/tellurium, mercury/cadmium/selenium, mercury/zinc/selenium mercury, cadmium, sulfur, mercury, zinc, sulfur, lead, tin, tellurium, lead, tin, steel Rhenium, lead, tin, sulfur, indium, arsenic, antimony, gallium Mu antimony or other suitable materials such as gallium antimony arsenic It should be understood that may also be used.

Additionally, structure 10 includes an anti-reflective coating 40. Anti-reflection coating 40 is the third semiconductor layer 38 and is used to reduce reflection of incident infrared radiation. anti The anti-radiation coating 40 is made of a material having a refractive index between the refractive index of the atmosphere and the third semiconductor layer 38. formed from. The anti-reflective coating 40 is made of zinc sulfide, zinc selenide or zinc telluride. It may be formed from lead, or other suitable materials may be used. Structure 10 is Also, the first passivation layer 18 and the first and second semiconductor layers 28 and includes a field plate region 42 used to control the relative potential of 30 . Field plate 42 has first and second semiconductor layers 28 and 30 in a first It is provided under the region intersecting the passivation layer 16. field plate Region 42 may be doped into substrate 12 or deposited with metal on the surface of substrate 12. You may wear it.

Control of the potential in the region where layers 28, 30 and 16 intersect is important for device performance. is important. A first passivation is applied to control the potential in this region. Layer 16 is near a flat band potential in first and second semiconductor layers 28 and 30. In order to optimize the photodiode characteristics in current operation, Any deviation from the flat band condition due to the use of the supply potential as used Provides a stable surface potential by using a compensating field region 42 (i.e., the first passivation layer 18 is selected as (selected to passivate the semiconductor layers 28 and 30).

First and second semiconductor layers 28 and 30 are formed on first passivation layer 16. The growth automatically results in a self-passivating buried bond. centre The presence of the field plate region 42 increases the surface voltage in the junction region by gate voltage control. This allows optimization of position.

By giving the above structure, the properties of structure 10 can be determined by signal processing and infrared detection. can be optimized from both perspectives.

The substrate 12 is made of silicon or arsenide on which a signal processing circuit with optimal characteristics can be formed. It may be gallium or germanium.

the first and second semiconductors 2 selected from materials that optimize infrared detection; 8 and 30 are provided on substrate 12 by heteroepitaxial selective region deposition. It will be done. Therefore, this combination of detector structure and substrate 12 is a monolithic heterogeneous Construct an epitaxial focal plane array and associate the hybridized structure with Not affected by shortcomings.

Structure 10 may be formed in the manner described below.

After substrate 12 is formed with readout and signal processing circuitry 14, it is heavily doped. regions 32 and 34 and field plate region 42 are formed. Or is it? Passivation layers 16 and 18 are provided on substrate 12 . then contact The window is a passivation layer covering the heavily doped region 34 by the photolith graph. drilled into the vation layers 18 and 18. the first metal layer is heavily doped. The ohmic contacts 20 are provided by vacuum evaporation to form the ohmic contacts 20 to the areas 34. Lifted off. A second photolithographic process is then carried out to form the metallization layer 36. A rough step is executed. The morphology of the metallization layer 36 forms the boundaries of the structure 10 and 2 is selected to be in ohmic contact with the semiconductor layer 30 of No. 2.

Thereafter, nuclear windows 22-26 are opened in passivation layers 16 and 18. A third photolithographic step is used to increase the thickness. Nuclear window 22~ The configuration, dimensions, and spacing of the 26 will depend on the desired detector geometry and the epitome used. Determined by the characteristics of the taxial

growth process. For example, laterally from the nuclear window If the vertical growth occurs at the same rate as the vertical growth, the window will grow as fast as the vertical growth. They should be widely spaced apart. Too many nuclear windows are To provide spatial constraints for the readout and signal processing circuits 14 in 12. The number of windows should also be minimized. Number of nuclear windows 22 to 26 The number and dimensions are determined by the lateral growth rate relative to the vertical growth rate of the first semiconductor layer 28. It can be minimized by maximizing the speed ratio. Furthermore, the second The ratio of the lateral growth rate to the vertical growth rate of the semiconductor layer 30 is also the first and a maximum between the junction between the second semiconductor layers 2g and 3C and the metallization layer 36. should be maximized to give the possible distance of The thickness of the first semiconductor layer 28 is By forming a thinner layer, the number of required nuclear windows 22 to 26 is reduced. be done. By forming the second semiconductor layer 30 even thicker, the metallization layer 36 and The distance between the junction between the first and second semiconductor layers 28 and 30 is greater. This gives more tolerance to variations in lateral growth rate. Ru.

After opening the nuclear windows 22 to 26 in the passivation layers 28 and 30, the remaining The remaining photoresist is removed from passivation layer 16 and substrate 12 is removed from its surface. located in a low temperature metallic vapor phase epitaxial reactor such that in-situ cleaning of surfaces is performed. it will be done. On-site surface cleaning can be done by ultraviolet ozone etching, atomic hydrogen etching or ultraviolet radiation or other free radicals generated from appropriate reactants in the plasma field, including etching.

The nucleation crystals are located within the nucleation windows 22 to 26 of the passivation layers 16 and 18, grow up. The material from which the passivation layer 18 and the metallization layer 36 are formed is nucleated. To prevent crystal formation, nucleation occurs only in the nucleation windows 22-26. Money The flow of reactants into the gas phase epitaxial reactor is carried out through nuclear windows 22 to 2. The first semiconductor layer 28 is changed to grow a first semiconductor layer 28 that nucleates on the nucleated crystals in 6.

The reactant flow is further varied to grow the second semiconductor layer 30 reaction The final change in the material flow causes the third semiconductor layer 38 to grow. Ru. Finally, a third antireflection layer 40 is applied by vacuum deposition outside the metallic vapor phase reactor, is formed on the semiconductor layer 38 of.

Therefore, the present invention provides that the infrared material is selected to optimize infrared detection, - infrared signal processing materials can be selected to optimize the power signal processing circuit. It will be appreciated that an apparatus can be provided for detecting radiation. that Therefore, the invention is not limited to the particular embodiments shown. example For example, another suitable region-selective epitaxial growth technique may be used to form the first semiconductor layer. It may also be used for the relative doping of the first and second semiconductor layers; The function they perform (ie base or collector) may also be varied. the Other modifications may occur upon consideration of the specification, drawings, and following claims. This will be made clear to the dealer.

international search report 1***-^"-"-I@PCT/US If/n17Q5 International Search Report SA 26299

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Publication number	Priority date	Publication date	Assignee	Title
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Priority And Related Applications

Applications Claiming Priority (2)

Application	Filing date	Title
US12384287A	1987-11-23	
US123,842	1987-11-23	

Concepts

machine extracted

Download Filter table

Name		Image	Sections	Count	Query match
☛ radiation	title,claims,description	23	0.000		
☛ detection method	title,claims,description	8	0.000		
☛ semiconductor	claims,description	103	0.000		
☛ material	claims,description	50	0.000		
☛ mercury	claims,description	40	0.000		
☛ mercury	claims,description	39	0.000		
☛ passivation	claims,description	31	0.000		
☛ cadmium	claims,description	23	0.000		
☛ tellurium	claims,description	23	0.000		
☛ substrate	claims,description	22	0.000		
☛ cadmium atom	claims,description	21	0.000		
☛ tellurium atom	claims,description	21	0.000		
☛ Sulfur	claims,description	18	0.000		
☛ Zinc	claims,description	18	0.000		
☛ sulfur	claims,description	18	0.000		
☛ sulfur	claims,description	18	0.000		
☛ tin	claims,description	18	0.000		
☛ zinc	claims,description	18	0.000		
☛ zinc	claims,description	18	0.000		
☛ Selenium	claims,description	16	0.000		
☛ selenium	claims,description	16	0.000		
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☛ lead	claims,description	15	0.000		
☛ method	claims,description	15	0.000		
☛ Gallium	claims,description	10	0.000		
☛ gallium	claims,description	10	0.000		
☛ nucleation	claims,description	8	0.000		
☛ nucleation	claims,description	8	0.000		
☛ charge carrier	claims,description	6	0.000		
☛ indium	claims,description	6	0.000		
☛ indium atom	claims,description	6	0.000		
☛ silicon	claims,description	6	0.000		
☛ silicon	claims,description	6	0.000		
☛ AsGa	claims,description	5	0.000		
☛ Gallium arsenide	claims,description	5	0.000		
☛ antimony arsenic	claims,description	5	0.000		
☛ antimony atom	claims,description	5	0.000		
☛ conductor	claims,description	5	0.000		
☛ germanium	claims,description	5	0.000		

⌘ germanium atom	claims,description	5	0.500
⌘ recombination	claims,description	5	0.000
⌘ recombination	claims,description	5	0.000
⌘ arsenic	claims,description	4	0.500
⌘ biosynthetic process	claims,description	4	0.000
⌘ indium antimonide	claims,description	4	0.000
⌘ response	claims,description	4	0.000
⌘ coating agent	claims,description	3	0.000
⌘ coating method	claims,description	3	0.500
⌘ coupling	claims,description	3	0.000
⌘ coupling process	claims,description	3	0.000
⌘ coupling reaction	claims,description	3	0.500
⌘ rhenium	claims,description	2	0.000
⌘ rhenium atom	claims,description	2	0.000
⌘ layer	claims	53	0.000
⌘ vapour-phase epitaxy	claims	2	0.000
⌘ coating layer	claims	1	0.500
Show all concepts from the description section			

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⑫ 公表特許公報(A)

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⑬ 公表 平成2年(1990)7月26日

⑭ Int.Cl.⁵

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予備審査請求

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部門(区分) 7(2)

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31/10

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(全 6 頁)

⑮ 発明の名称 赤外線放射検出方法および装置

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⑱ 翻訳文提出日 平1(1989)7月21日

⑲ 国際出願 PCT/US88/03792

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㉔ 指 定 国 DE(広域特許), FR(広域特許), GB(広域特許), IT(広域特許), JP, NL(広域特許)

請求の範囲

(1) 読出しおよび信号処理回路が集積されており、シリコン、ヒ化ガリウムまたはゲルマニウムから成るグループから選択された材料で形成された基体と、

水銀・カドミウム・テルル、水銀・亜鉛・テルル、水銀・カドミウム・セレンウム、水銀・亜鉛・セレンウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、鉛・錫・テルル、鉛・錫・セレンウム、鉛・錫・硫黄、インジウム・ヒ素・アンチモン、ガリウム・インジウム・アンチモン、またはガリウム・アンチモン・ヒ素から成るグループから選択された材料から成る前記基体上に成長された第1の半導体層と、

前記第1の半導体層上に成長された第2の半導体層とを含み、前記第1および第2の半導体層が受けた赤外線放射波にตอบสนองして前記基体中の前記読出しおよび信号処理回路に電気信号を伝送するように動作可能である赤外線放射波検出用のモノリシック構造。

(2) 前記基体と前記第1の半導体層との間に設けられた第1のパッシベーション層を含む請求項1記載の装置。

(3) 前記第1のパッシベーション層と第1の半導体層との間に設けられた第2のパッシベーション層を含む請求項2記載の装置。

(4) 前記第1および第2のパッシベーション層は、前記第1の半導体層の形成を制御するように動作可能な複数の核ウインドウを含む請求項3記載の装置。

(5) 前記第1の半導体層の核化は前記核ウインドウ中での

み生じる請求項4記載の装置。

(6) 前記第2の半導体層上に設けられた第3の半導体層を含み、前記第3の半導体層は前記第2の半導体層中における自由電荷キャリアの表面再結合速度を減少するように動作することができる請求項4記載の装置。

(7) 前記第1、第2および第3の半導体層は金属的気相エピタキシによって成長される請求項6記載の装置。

(8) 前記第3の半導体層上に設けられた反射防止材料の層を含む請求項1記載の装置。

(9) 水銀・カドミウム・テルル、水銀・亜鉛・テルル、水銀・カドミウム・セレンウム、水銀・亜鉛・セレンウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、鉛・錫・テルル、鉛・錫・セレンウム、鉛・錫・硫黄から成るグループから選択された材料から形成された第1および第2の半導体材料の層を赤外線放射源に露出し、

前記半導体材料の第1および第2の層において光電流を発生し、

その上に前記第1および第2の半導体層が成長し、シリコン、ヒ化ガリウムまたはゲルマニウムから成るグループから選択された材料から形成された基体内に設けられた読出しおよび信号処理回路によって前記光電流を感知することを含む赤外線放射を検出する方法。

(10) 前記第1の半導体材料の層、前記第2の半導体材料の層および前記基体はモノリシック構造を含む請求項9記載の方法。

(11) 前記第1の半導体材料の層は第1のバッシベーション層によって前記基体から分離されている請求項9記載の方法。

(12) 前記第1のバッシベーション層は第2のバッシベーション層によって半導体材料の前記第1の層から分離されている請求項11記載の方法。

(13) 前記第1および第2のバッシベーション層は前記第1の半導体材料の層の形成を制御するように動作可能な複数の核ウインドウを含む請求項12記載の方法。

(14) 前記第2の半導体材料の層上に前記第3の半導体材料の層を設けることによって前記第2の半導体材料の層における自由電荷キャリアの表面再結合速度を減少する付加的なステップを含む請求項9記載の方法。

(15) 前記第1、第2および第3の半導体層は金属的気相エピタキシによって形成される請求項14記載の方法。

(16) 赤外線放射に反射防止材料の層を通過させることを可能にする付加的なステップを含む請求項9記載の方法。

(17) 読出しおよび信号処理回路が集積されており、前記読出しおよび信号処理回路の特性を最適化するように選択された材料で形成された基体と、

赤外線検出を最適化するように選択された材料から前記基体上に成長された第1の半導体層と、

前記基体と前記第1の半導体材料の層との間に設けられた複数のバッシベーション層と、

前記第1および第2の半導体層が受けた赤外線放射波にตอบสนองして前記基体中の前記読出しおよび信号処理回路に電気信

号を伝送するように動作可能な前記第1の半導体層上に設けられた第2の半導体層と、

第2の半導体層における自由電荷キャリアの表面再結合速度を減少するように動作可能な前記第2の半導体層上に設けられた第3の半導体層と、

前記第3の半導体層上に設けられ、大気と第3の半導体層の屈折率の間の屈折率を有する反射防止被覆とを含む赤外線放射波を検出するためのモノリシック構造のアレイ。

(18) 前記複数のバッシベーション層は前記第1の半導体層の成長を制御するように動作可能な複数の核ウインドウを含む請求項17記載のアレイ。

(19) 前記核ウインドウの1つは前記第1の半導体層と前記読出しおよび信号処理回路との間における電気結合を可能にする請求項18記載のアレイ。

(20) 前記モノリシック構造は、さらに前記第1および第2の半導体層と前記読出しおよび信号処理回路との間における電気結合を可能にするオーム接触を含む請求項19記載のアレイ。

明 細 書

赤外線放射検出方法および装置

1. 発明の分野

本発明は赤外線感知の分野、特に赤外線放射検出方法および装置に関する。

2. 従来技術の説明

基本的な赤外線検出器は、調査、目標捜査および1乃至30 μm の波長を有する電磁放射波の存在を感知する捜査および追跡映像システムにおいてしばしば使用される。赤外線放射を検出するためにこれらの基本検出器は、トリグリシンサルフェートおよびランタンドープされたジルコン酸チタン酸鉛結晶のような温度感応性熱電気および強誘電材料をしばしば使用する。このような結晶は、結晶に取付けられた電極に対して電位降下をもたらす入射した赤外線放射波にตอบสนองして瞬間的な電気偏波を示す。材料の抵抗が入射した放射線の関数として変化する碲化鉛および水銀・カドミウム・テルルのような光導電性材料が使用されてもよい。最後に、固有のバンド・トウ・バンド電子ホール励起が入射した赤外線束に比例する電流または電圧を発生する水銀・カドミウム・テルル、インジウム・アンチモンまたは類似した材料から構成されるような光起電装置が使用されてもよい。

このような基本的検出器のアレイは熱映像システムを形成するために使用されてもよい。実時間において前方観察赤外線 ("FLIR") 映像センサのようなプリズム反射鏡を回動する熱映像システムは基本検出器の1次元のアレイにわた

ってソースによって放出された放射線を走査するために使用される。基本的検出器がこのように使用された場合、検出器の一時的な出力は映像の2次元表示を生成するように使用されてもよい。観察または走査アレイのいずれかを使用することができる2次元検出アレイ映像システムにおいて、基本的検出器は自由電荷キャリアまたは電流を生成し、それは電荷結合装置 ("CCD") のような適切な読出し集積回路によって監視されてもよい。CCDからの出力は時間遅延および積分または並列直列走査変換等の種々の技術によって処理されることが可能であり、フレーム速度、信号・雑音比等のシステム要求にしたがって選択される。その他の読出し装置が使用されてもよい。

上記の検出器構造は能率的であるが、それらは一般的にくつかの製造に関連する欠点を有する。第1に、検出器および読出し装置が別々に構成され、その後機械的に結合される多数のこのような検出器構造はハイブリッド的に形成される。ハイブリッド構造の形成は付加的な処理ステップを含むため、このような構造はモノリシック装置 (すなわち、検出器と読出しおよび信号処理回路が1つの材料のシステム中に形成されている装置) と比較して生産効率が低い傾向がある。さらに、形成中に意図しない欠陥が誘起されて信頼性を低め、特性を損うという可能性が高い。モノリシック検出器はハイブリッド形成に必要な付加的な処理ステップを回避するが、信号処理回路のために赤外線検出器と同一の材料を使用する必要がある。この材料 (例えば Hg Cd Te または In Sb)

は製造技術が充分に開発されているシリコンまたはヒ化ガリウムから形成される回路よりも常に低い特性の信号処理回路となる。

発明の要約

本発明の好ましい実施例によると、赤外線放射を検出する方法および装置が開示されている。装置は読出しおよび信号処理回路が集積された基体を含む。基体はシリコン、ヒ化ガリウムおよびゲルマニウムから成るグループから選択された材料から形成されている。第1の半導体の層は水銀・カドミウム・テルル、水銀・亜鉛・テルル、水銀・カドミウム・セレンウム、水銀・亜鉛・セレンウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、鉛・錫・テルル、鉛・錫・セレンウム、鉛・錫・硫黄、インジウム・ヒ素・アンチモン、ガリウム・インジウム・アンチモンまたはガリウム・アンチモン・ヒ素から成るグループから選択された材料から基体上に成長される。第2の半導体の層がそれから第1の半導体の層上に形成される。

図面の簡単な説明

本発明の種々の利点が以下の説明および図面から当業者に明らかになるであろう。

図面は本発明による赤外線放射を検出する装置の好ましい実施例の断面図である。

好ましい実施例の説明

本発明の好ましい実施例によると、赤外線放射を検出する構造10は図中で4で示されるように設けられる。構造10は半

一の検出素子として使用されてもよいし、もしくは多数素子の映像装置の一部であってもよい。構造10はシリコン、ヒ化ガリウムまたはゲルマニウムから形成されてもよい基体12を含む。しかしその他の適切な材料が使用されてよいことが理解されるべきである。基体12は、以下に説明される半導体の層の出力を使用可能な形態に変換する符号14によって示された適切な読出しおよび信号処理回路を含む。読出しおよび信号処理回路14は、ここで参照されているBlazer, N., およびStehlae, R. による文献(“Buffered Direct Injection of Photocurrents into Charge-Coupled Device”, IEEE Transactions on Electron Devices, ED25, n.2, p.160, 1978年2月)に記載されたものに類似していてもよい。半導体の層からの出力を処理するその他の適切な手段が使用されてもよい。

基体表面の電気特性を制御するために第1のバッシベション層16が設けられている。第1のバッシベション層16は基体12に最適なバッシベション状態を提供する材料から選択される。このような材料はSiO₂またはSiN₄を含む。しかしその他の適切な材料が使用されてよいことが理解されるべきである。第2のバッシベション層18は第1のバッシベション層16上に付着される。第2のバッシベション層18は以下に説明される赤外線能動半導体層に最適なバッシベション状態を提供し、赤外線能動半導体層の核が発生しない面を形成する複数の材料の1つから形成される。このような材料はSiO₂またはZnSを含んでもよい。しかしその

他の適切な材料が使用されてよいことが理解されるべきである。第1および第2のバッシベション層16および18はオーム接触子20および複数の核ウインドウ22乃至26を有する。オーム接触子20は、以下に説明される第2の半導体層と読出しおよび信号処理回路14との間に電気結合を行うために使用される。核ウインドウ22乃至26は第1の半導体層の核にシード位置を与えるために使用される。さらに核ウインドウ24は第1の半導体層と読出しおよび信号処理回路14との間の電気結合を可能にする。

入射した赤外線に反応して光電流を発生するために構造10は、第1の半導体層28および第2の半導体層30を含む。第1および第2の半導体層28および30は共にベースおよびヘテロ接合フォトダイオードのコレクタ層を含む。第1の半導体層28はHg_{1-x}Cd_xTeで定められた化学量的関係を有する水銀・カドミウム・テルルの層から構成される。xの組成値は、第1の半導体層28が赤外線スペクトル中の特定の波長の赤外線放射に感応するように選択される。例えば、xの組成値が約0.2であるように選択された場合、第1の半導体層28は所望の動作温度(例えば絶対温度77度)で約10乃至12mのカットオフ波長を有する長い波長の赤外線放射波に感応する。しかしながら、第1の半導体層28は水銀・亜鉛・テルル、水銀・カドミウム・セレンウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、水銀・亜鉛・セレンウム、鉛・錫・テルル、鉛・錫・セレンウム、鉛・錫・硫黄、インジウム・ヒ素・アンチモン、ガリウム・インジウム・アンチモン、またはガリ

ウム・アンチモン・ヒ素、のようなその他の適切な材料を含んでもよいことが理解されるべきである。

第2の半導体層30はHg_{1-y}Cd_yTeで定められる化学量的な関係を有する水銀・カドミウム・テルルの層を含む。yの組成値は第1の半導体層28の組成値xよりも大きいように選択され、典型的に0.3の値を有する。しかしながら、その他の適切なyの値が選択され、また水銀・カドミウム・テルル、水銀・亜鉛・テルル、水銀・カドミウム・セレンウム、水銀・亜鉛・セレンウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、鉛・錫・テルル、鉛・錫・セレンウム、鉛・錫・硫黄、インジウム・ヒ素・アンチモン、ガリウム・インジウム・アンチモンまたはガリウム・アンチモン・ヒ素を含むその他の適切な材料が選択されてもよいことが理解されるべきである。

第1の半導体層28はフォトダイオードベース層として動作し、一方第2の半導体層30はフォトダイオードコレクタ層として動作する。しかしながら構造10の収集効率を高めるために第1および第2の半導体層28および30の役割が逆にされてもよい(すなわち第2の半導体層30がベース層になり、第1の半導体層28がコレクタ層になる)。この場合、yの組成値は約0.2であり、xの組成値は約0.3である。しかしながら、一般的には第2の半導体層30は狭いバンドギャップ材料となり、第1の半導体層28は広いバンドギャップ材料となる。層28および30は反対の型の混合物を有するようにドーパされる。すなわち第1の半導体層28はp型にドーパされ、第2の半導

体層はn型にドーパされ、その逆も可能である。しかしながら、同じ型のヘテロ接合も使用されてよいことが理解されるべきである。

赤外線スペクトルにおける光の光子が装置構造10によって吸収されたとき、電子ホール対が発生される。電子ホール対が再結合する前に第1および第2の半導体層28および30の間の接合部に到達した場合、第1および第2の半導体層28および30の間の接合部における電界は電子をn型半導体層の中に移動させ、ホールをp型半導体層中に移動させる。この電子ホール移動は受光された光子の数に比例する光電流を生成する。

第1および第2の半導体層28および30において発生された光電流を感知するために、基体12はさらに重くドーパされた領域32および34を含む。重くドーパされた領域32は核ウインドウ24を通して読出しおよび信号処理回路14と第1の半導体層28との間に電気結合を可能にする。核ウインドウ24に付着される材料はHgTeまたは半導体層28に類似した結晶構造および格子定数を有する類似した半金属性の材料であることができる(すなわち、HgSe, HgS, PbTe, PbSe, PbS, およびGraySnが代わりに選択されることができる)。これは重くドーパされた領域32と第1の半導体層28との間に良好なオーム接触を提供する。同一の材料は同時に核ウインドウ22および26中に付着されるが、それは第1の半導体層28に対して、オーム接触ではなく核位置としてのみ作用する。さらに、重くドーパされた領域34は金属化

アンチモン・ヒ素のようなその他の適切な材料が使用されてもよいことが理解されるべきである。

さらに構造10は反射防止被覆40を含む。反射防止被覆40は第3の半導体層38上に設けられ、入射した赤外線放射の反射を減少するために使用される。反射防止被覆40は大気と第3の半導体層38の屈折率の間の屈折率を有する材料から形成される。反射防止被覆40は硫化亜鉛、セレン化亜鉛またはテルル化亜鉛から形成されてもよく、その他の適切な材料が使用されてもよい。構造10はまた第1のバッシェイション層16並びに第1および第2の半導体層28および30の相対電位を制御するために使用されるフィールドプレート領域42を含む。フィールドプレート42は第1および第2の半導体層28および30が第1のバッシェイション層16と交差する領域の下に設けられる。フィールドプレート領域42は基体12中にドーパされるか、もしくは基体12の表面上に金属を付着させてもよい。

層28, 30および16が交差する領域における電位の制御は装置特性にとって重要である。この領域における電位を制御するために、第1のバッシェイション層16は第1および第2の半導体層28および30の中の平坦なバンド電位の近くにおいて、電流動作におけるフォトダイオード特性を最適化するためにゲートが使用されるように供給電位の使用による平坦なバンド状態からの任意の偏差を補償するフィールド領域42を使用することによって安定した表面電位を与えるように選択される(すなわち、第1のバッシェイション層16は第1および第2の半導体層28および30をバッシェイション化するように選

層36およびオーム接触子20を通じて読出しおよび信号処理回路14と第2の半導体層30との間に電気結合を提供する。オーム接触子20および36は2つの異なる金属であることができ、オーム接触子20は重くドーパされた領域34との良好なオーム接触を生じるように選択され、金属化層36はn型用のプラチナおよびp型用の金のように第2の半導体層30との良好なオーム接触を形成するように選択される。金属化層36はまた第1の半導体層28の核が抑制される材料であるように選択されなければならない。

第2の半導体層30がフォトダイオードのベースとして動作する場合、第2の半導体層30の内部における自由電荷キャリアは第2の半導体層28との境界面に向かってドリフトし再結合する。この再結合の結果、自由電荷キャリアが第1のバッシェイション層16によって収集される効率が減少される。第2の半導体層30中の自由電荷キャリアの再結合の速度を減少するために、第2の半導体層30がフォトダイオードのベースとして動作するとき第3の半導体層38が設けられる。第3の半導体層38はzの組成値がyよりも大きいように選択されたHg_{1-x}Cd_xTeで定められた化学量的関係を有する水銀・カドミウム・テルルから形成されてもよい。しかしながら、水銀・カドミウム・テルル、水銀・亜鉛・テルル、水銀・カドミウム・セレンウム、水銀・亜鉛・セレンウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、鉛・錫・テルル、鉛・錫・セレンウム、鉛・錫・硫黄、インジウム・ヒ素・アンチモン、ガリウム・インジウム・アンチモンまたはガリウム・

砒される)。

第1のバッシェイション層16上で第1および第2の半導体層28および30が成長することにより自動的に自己バッシェイション埋設接合がもたらされる。フィールドプレート領域42の存在はゲート電圧制御による接合領域中の表面電位の最適化を可能にする。

上記の構造を与えることによって、構造10の特性は信号処理および赤外線検出の両観点から最適化されることができる。基体12は最適な特性の信号処理回路が形成されることができるシリコン、ヒ化ガリウムまたはゲルマニウムであってよい。それから赤外線検出を最適化する材料から選択された第1および第2の半導体28および30がヘテロエピタキシャル選択領域付着によって基体12上に設けられる。したがって、この検出器構造と基体12との組合せはモノリシックヘテロエピタキシャル焦点平面アレイを構成し、ハイブリッド化された構造に関連した欠点の弊害を受けない。

構造10は以下に説明された方法で形成されることができる。基体12が読出しおよび信号処理回路14と共に形成された後、重くドーパされた領域32および34並びにフィールドプレート領域42が形成される。それからバッシェイション層16および18が基体12上に設けられる。それから接触ウインドウはフォトリソグラフによって重くドーパされた領域34を覆うバッシェイション層16および18中に開けられる。第1の金属層は、重くドーパされた領域34に対するオーム接触子20を形成するために真空蒸着により供給されリフトオフされる。その後、

金属化層36を形成するために第2のフォトリソグラフィステップが実行される。金属化層36の形態は構造10の境界を形成し、第2の半導体層30とオーミック接触するように選択される。

その後、パッシベーション層16および18中に核ウインドウ22乃至26を開くために第3のフォトリソグラフィステップが使用される。核ウインドウ22乃至26の形態、寸法および間隔は所望の検出器の幾何学形状および使用されるエピタキシャル成長過程の特性によって決定される。例えば、核ウインドウから横方向の成長が垂直方向の成長と同じ速度で生じた場合、ウインドウはそれらと同程度広く離されて位置されているべきである。多過ぎる個数の核ウインドウは基体12中の脱出しおよび信号処理回路14に対して空間的な制限を与えるため、核ウインドウの数はまた最小にされるべきである。核ウインドウ22乃至26の個数および寸法は第1の半導体層28の垂直方向の成長速度に対する横方向の成長速度の比率を最大にすることによって最小化されることができる。さらに第2の半導体層30の垂直方向の成長速度に対する横方向の成長速度の比率はまた第1および第2の半導体層28および30の間の接合部と金属化層36との間に最大の可能な距離を与えるように最大にされるべきである。第1の半導体層28を厚い層に形成することによって、要求される核ウインドウ22乃至26の数は減少される。第2の半導体層30をさらに厚く形成することにより、金属化層36と第1および第2の半導体層28および30間の接合部との間の距離がより大きくなるので、横方向の成長速度のバリエーションに対してさらに許容性を与えられる。

パッシベーション層28および30に核ウインドウ22乃至26を開けた後、残りのフォトリソグラフィステップはパッシベーション層16から除去され、基体12はその表面の現場浄化が行われるように低温金属的気相エピタキシャル反応器中に位置される。現場表面浄化は紫外線オゾンエッチング、原子水素エッチングまたは紫外線またはプラズマフィールド中の適切な反応物から生じたその他の遊離基によるエッチングを含む。

核結晶はパッシベーション層16および18の核ウインドウ22乃至26の中で成長する。パッシベーション層18および金属化層36が形成される材料は核結晶の形成を妨げるため、核結晶は核ウインドウ22乃至26中でのみ生じる。金属的気相エピタキシャル反応器中への反応物の流入は、核ウインドウ22乃至26中の核結晶上で核化する第1の半導体層28を成長させるように変化される。反応物流入はさらに第2の半導体層30を成長させるように変化される。反応物流入における最終変化により第3の半導体層38が成長させられることができる。最後に、反射防止層40が金属的気相反応器の外側で真空蒸着によって第3の半導体層38上に形成される。

したがって、本発明は赤外線検出を最適にするように赤外線材料が選択され、一方信号処理回路を最適化するように信号処理材料が選択されることができる赤外線放射を検出する装置を提供することができることが理解されるであろう。それ故、本発明はここに示された特定の実施例により限定されるものではない。例えば、別の適切な領域選択エピタキシャル成長技術が第1の半導体層を形成するために使用されても

よい。第1および第2の半導体層の相対的ドーピング並びにそれらが実行する作用（すなわちベースまたはコレクタ）も変化されてよい。その他の修正は明細書、図面および以下の請求の範囲の各項を検討することにより当業者に明らかになるであろう。

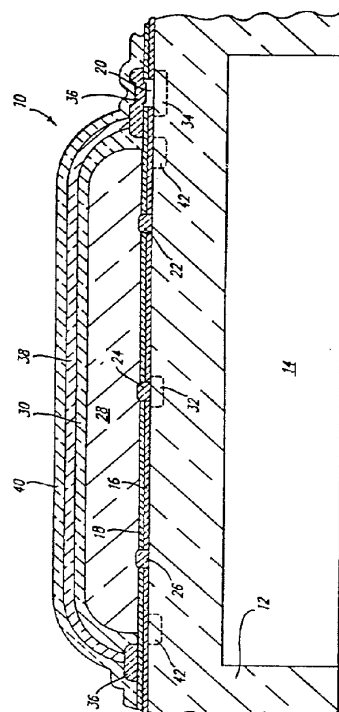


FIG. 1.

國際調查報告

PCT/US 88/03792

I. CLASSIFICATION OF SUBJECT MATTER of International Application No. PCT/US 88/03792
 According to International Patent Classification (IPC) or to any other classification system, indicate any IPC Class: H 01 L 31/08, 27/14, G 01 J 5/20

II. FIELD SEARCHED
 Minimum Documentation Searched:
 Classification System: IPC4 H 01 L, G 01 J
 Documentation Searched other than Minimum Documentation:
 to the extent that such documents are included in the Field Searched:

III. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of Document, with indication, where appropriate, of the relevant passages	Relevance to Claim No. 1
X	US, A, 4559695 (I.M. BAKER) 24 December 1985, see column 3, line 8 - column 6, line 34; abstract; figures 1,6	1,17
A	---	9
X	US, A, 4521798 (I.M. BAKER) 4 June 1985, see column 3, line 6 - column 6, line 34; abstract; figures 1,6	1,17
A	---	9
A	EP, A2, 0137988 (TEXAS INSTRUMENTS INCORPORATED) 24 April 1985, see abstract; figure 1	1-3,8,9, 16,17
A	US, A, 4614960 (N. BLUZER) 30 September 1985, see abstract; figures 3,4	1,9, 17

IV. CERTIFICATION
 Date of the Actual Completion of the International Search: 14th April 1989
 Date of Mailing of the International Search Report: 28. 04. 89
 International Searching Authority: EUROPEAN PATENT OFFICE
 Signature of the International Searching Authority: P.C. VAN DER PUTTEN

International Application No. PCT/US 88/03792

II. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category	Citation of Document, with indication, where appropriate, of the relevant passages	Relevance to Claim No. 1
A	US, A, 4549195 (N. BLUZER) 22 October 1985, see abstract; figures 2,3,5	1,9, 17
A	US, A, 4313127 (S.C. SU ET AL) 26 January 1982, see abstract; figure 1	1,17
A	US, A, 4053919 (A.M. ANDREWS, II ET AL) 11 October 1977, see abstract; figure 2	1,9, 17
A	IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. ED-25, No. 2, February 1978, N. Bluzer et al: "Buffered Direct Injection of Photocurrents into Charge-Coupled Devices", see page 160 - page 166 cited in the application	1,9, 17

國際調查報告

PCT/US 88/03792

SA 26299

This search was the parent family document relating to the parent documents cited in the above-mentioned international search report.
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Parent document cited in search report	Publication date	Parent family members	Publication date
US-A- 4559695	24/12/85	EP-A-B- 0061803	06/10/82
		GB-A-B- 2095905	06/10/82
		JP-A- 57171226	21/10/82
		US-A- 4521798	04/06/85
US-A- 4521798	04/06/85	EP-A-B- 0061803	06/10/82
		GB-A-B- 2095905	06/10/82
		JP-A- 57171226	21/10/82
		US-A- 4559695	24/12/85
EP-A2- 0137988	24/04/85	US-A- 4447291	08/05/84
		EP-A- 0268792	02/11/88
		JP-A- 60594764	27/05/85
		US-A- 4684812	04/08/87
		US-A- 4686373	11/08/87
US-A- 4614960	30/09/85	NONE	
US-A- 4549195	22/10/85	NONE	
US-A- 4313127	26/01/82	NONE	
US-A- 4053919	11/10/77	NONE	

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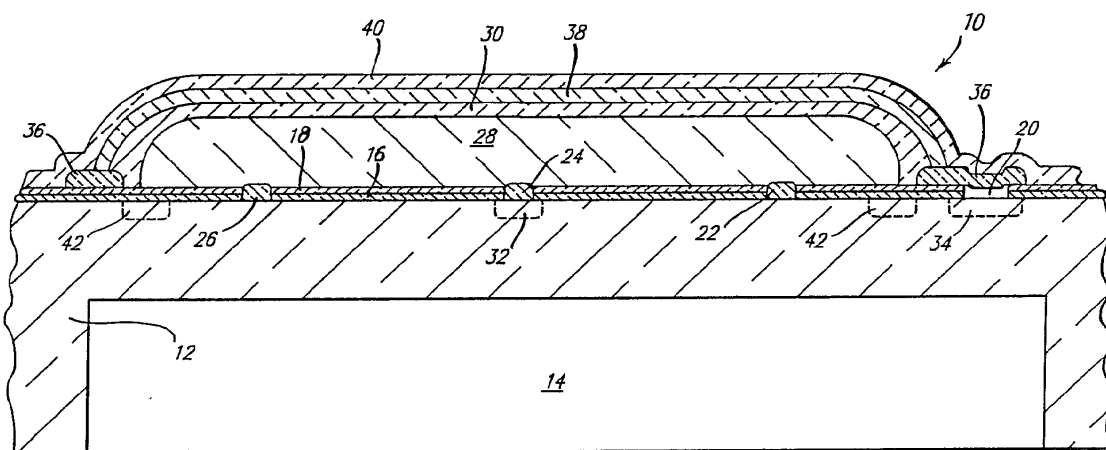
For more details about this report, see Official Journal of the European Patent Office, No. 12/89



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(21) International Application Number: PCT/US88/03792 (22) International Filing Date: 28 October 1988 (28.10.88) (31) Priority Application Number: 123,842 (32) Priority Date: 23 November 1987 (23.11.87) (33) Priority Country: US (71) Applicant: SANTA BARBARA RESEARCH CENTER [US/US]; 75 Coromar Drive, Goleta, CA 93117 (US). (72) Inventors: AHLGREN, William, L. ; 365 Hillsboro Way, Goleta, CA 93117 (US). SCHULTE, Eric, F. ; 2427 Calle Montilla, Santa Barbara, CA 93117 (US). (74) Agents: SCHUBERT, William, C. et al.; Hughes Aircraft Company, Post Office Box 45066, Bldg. C1, M/S A-126, Los Angeles, CA 90045-0066 (US).		(81) Designated States: DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, NL (European patent). Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>	

(54) Title: METHOD AND APPARATUS FOR DETECTING INFRARED RADIATION



(57) Abstract

A method and apparatus for detecting infrared radiation is disclosed. The apparatus comprises a substrate (12) having readout and signal processing circuits (14) integrated therein. The substrate (12) is formed from a material selected from the group consisting of silicon, gallium arsenide, or germanium. A first semiconductor layer (28) is grown on the substrate (12) from a material selected from the group consisting of mercury-cadmium-telluride, mercury-zinc-telluride, mercury-cadmium-selenide, mercury-zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide. A second semiconductor layer (30) is then grown on the first semiconductor layer (28).

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METHOD AND APPARATUS FOR
DETECTING INFRARED RADIATION

1 BACKGROUND OF THE INVENTION

1. Field of the Invention

 This invention relates to the field of infrared sensing, and
5 more particularly concerns a method and apparatus for detecting
infrared radiation.

2. Description of Related Art

 Elemental infrared detectors are often used in surveillance,
10 target seeking, and search and tracking imaging systems to sense the
presence of electromagnetic radiation having wavelengths from 1-30 μ m.
To detect infrared radiation, these elemental detectors often use
temperature sensitive pyroelectric and ferroelectric materials such as
triglicine sulfate and lanthanum doped lead zirconate titanate
15 crystals. Such crystals exhibit spontaneous electrical polarization
in response to incident infrared radiation which creates a potential
drop across electrodes attached to the crystals. Photoconductive
materials such as lead-sulfide and mercury-cadmium-telluride may also
be used in which the resistance of the material changes as a function
20 of incident radiation. Finally, photovoltaic devices such as those
fabricated from mercury-cadmium-telluride, indium antimonide, or
similar materials may be used in which intrinsic band-to-band
electron-hole excitation generates a current or voltage which is
proportional to the incident radiation flux.

25 Arrays of such elemental detectors may be used to form
thermal imaging systems. In real-time thermal imaging systems such as
forward looking infrared ("FLIR") imaging sensors, oscillating prism

1 mirrors are used to scan radiation emitted by a source across a
one-dimensional array of elemental detectors. When the elemental
detectors are used in this manner, the temporal outputs of the
detectors may be used to generate a two-dimensional representation of
5 the image. In two-dimensional detector array imaging systems which
can utilize either staring or scanning arrays, the elemental detectors
produce free charge carriers or currents which may then be monitored
by an appropriate readout integrated circuit such as a charge-coupled
device ("CCD"). The output from the CCD can be processed by various
10 techniques such as time delay and integration or parallel-to-serial
scan conversion, with the choice depending on the system requirements
of frame rate, signal-to-noise ratios, etc. Other readout devices may
also be used.

While the detector structures described above are effective,
15 they generally have several drawbacks in terms of fabrication. First,
many of such detector structures are hybridized in which the detector
and the readout device are separately fabricated and then mechanically
bonded. Because the formation of hybridized structures involves
additional processing steps, such structures tend to have lower yield
20 during production when compared to monolithic devices (i.e., devices
in which the detector and the readout and signal processing circuit
are fabricated in one material system). In addition, there is a
greater likelihood that defects will be unintentionally introduced
during fabrication resulting in lower reliability and reduced
25 performance. Monolithic detectors, while avoiding the additional
processing steps required for hybridization, suffer from the necessity
of using the same material as the infrared detector for the signal
processing circuits. This material (e.g., HgCdTe or InSb) invariably
leads to lower performance signal processing circuits than circuits
30 formed from silicon or gallium arsenide, for which the fabrication
technology is well-developed.

SUMMARY OF THE INVENTION

1 According to the preferred embodiment of the present invention, a method and apparatus for detecting infrared radiation is disclosed. The apparatus comprises a substrate having readout and
5 signal processing circuits integrated therein. The substrate is formed from material selected from the group consisting of silicon, gallium arsenide, and germanium. A first semiconductor layer is grown on the substrate from a material selected from the group consisting of mercury-cadmium-telluride, mercury-zinc-telluride, mercury-cadmium-
10 selenide, mercury-zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-tin-telluride, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide. A second semiconductor layer is then formed on the first semiconductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

15 The various advantages of the present invention will become apparent to one skilled in the art upon reading the following specification and by reference to the following drawing in which:
20 The FIGURE is a cross-sectional view of the preferred embodiment of the apparatus for detecting infrared radiation according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

25 According to the preferred embodiment of the present invention, a structure 10 for detecting infrared radiation is provided as shown 4 in the FIGURE. The structure 10 may be used as a single detection element, or be part of a multiple-element imaging device. The structure 10 comprises a substrate 12 which may be made of
30 silicon, gallium arsenide, or germanium, though it is to be understood that other suitable materials may be used. The substrate 12 comprises suitable readout and signal processing circuits, generally designated by the numeral 14, for converting the output of the semiconductor layers described below into useable form. The readout and signal
35 processing circuits 14 may be similar to that disclosed in Bluzer, N., and Stehlac, R., "Buffered Direct Injection of Photocurrents into

1 Charge-Coupled Devices", IEEE Transactions on Electron Devices, ED 25,
n.2 p. 160 February 1978, which is hereby incorporated by reference.
It should be understood that other suitable means for processing the
output from the semiconductor layers may be used.

5 To control the electrical properties of the surface of the
substrate, a first passivation layer 16 is provided. The first
passivation layer 16 is selected from materials which provide optimum
passivation for the substrate 12. Such materials may include SiO_2 or
 SiN_4 , though it is to be understood that other suitable materials may
10 be used. A second passivation layer 18 is deposited on the first
passivation layer 16. The second passivation layer 18 is formed of
one of several materials which provide optimum passivation for the
infrared-active semiconductor layers described below and forms a
surface on which nucleation of the infrared-active semiconductor
15 layers does not occur. Such materials may include SiO_2 or ZnS , though
it is to be understood that other suitable materials may be used. The
first and second passivation layers 16 and 18 have a ohmic contact 20
and a plurality of nucleation windows 22-26. The ohmic contact 20 is
used for providing electrical communication between the second
20 semiconductor layer described below and the readout and signal
processing circuits 14. The nucleation windows 22-26 are used for
providing seed locations for nucleation of the first semiconductor
layer. In addition, the nucleation window 24 allows electrical
communication between the first semiconductor layer and the readout
25 and signal processing circuits 14.

To generate a photocurrent in response to incident
radiation, the structure 10 further comprises a first semiconductor
layer 28 and a second semiconductor layer 30. The first and second
semiconductor layers 28 and 30 together comprise the base and
30 collector layers of a heterojunction photodiode. The first
semiconductor layer 28 comprises a layer of mercury-cadmium-telluride
having a stoichiometric relationship defined by $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$. The
composition value of x is chosen so that the first semiconductor layer
28 is sensitive to infrared radiation of a particular wavelength in
35 the infrared spectrum. For example, if the composition value of x is
chosen to be approximately 0.2, the first semiconductor layer 28 will

1 be sensitive to long wavelength infrared radiation having a cut-off
wavelength of approximately 10-12 μ m at the desired operating
temperature (e.g., 77 Kelvin). It is to be understood, however, that
the first semiconductor layer 28 may comprise other suitable materials
5 such as mercury-zinc-telluride, mercury-cadmium-selenide, mercury-
zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-
tin-telluride, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-
antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide.

The second semiconductor layer 30 comprises a layer of
10 mercury-cadmium-telluride having a stoichiometric relationship defined
by $\text{Hg}_{1-y}\text{Cd}_y\text{Te}$. The composition value of y may be chosen to be larger
than the composition value x of the first semiconductor layer 28, and
may typically have a value of 0.3. It is to be understood, however,
that other suitable values of y may be chosen and other suitable
15 materials may also be chosen including mercury-cadmium-telluride,
mercury-zinc-telluride, mercury-cadmium-selenide, mercury-zinc-
selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-tin-
telluride, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-
antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide.

20 The first semiconductor layer 28 acts as a photodiode base
layer while the second semiconductor layer 30 acts as a photodiode
collector layer. To increase the collection efficiency of the
structure 10, however, the roles of the first and second semiconductor
layers 28 and 30 may be reversed (i.e., the second semiconductor layer
25 30 becoming the base layer and the first semiconductor layer 28 the
collector layer). In this case, the composition value of y will be
approximately 0.2 and the composition value of x will be approximately
0.3. More generally, however, the second semiconductor layer 30 will
become the narrow bandgap material and the first semiconductor layer
30 28 will become the wide bandgap material. The layers 28 and 30 are
doped to have impurities of opposite type, i.e., the first
semiconductor layer 28 being doped p-type and the second semiconductor
layer 30 being doped n-type, or vice-versa. It will be appreciated,
however, that isotype heterojunctions may also be employed.

35 When a photon of light in the infrared spectrum of interest
is absorbed by the apparatus structure 10, an electron/hole pair is

1 generated. If the electron/hole pair arrives at the junction between
the first and second semiconductor layers 28 and 30 before
recombining, the electric field at the junction between the first and
second semiconductor layers 28 and 30 will cause the electron to move
5 into the n-type semiconductor layer and the hole to move into the
p-type semiconductor layer. This electron/hole migration produces a
photocurrent which is proportional to the number of photons received.

To sense the photocurrent generated in the first and second
semiconductor layers 28 and 30, the substrate 12 further comprises the
10 heavily doped regions 32 and 34. The heavily doped region 32 allows
electrical communication between the readout and signal processing
circuits 14 and the first semiconductor layer 28 through the
nucleation window 24. The material deposited in the nucleation window
24 can be HgTe or a similar semi-metallic material with crystal
15 structure and lattice constant similar to the semiconductor layer 28
(thus, HgSe, HgS, PbTe, PbSe, PbS, and grey Sn could be alternative
choices). This will provide a better ohmic contact between the
heavily doped region 32 and the first semiconductor layer 28. The
same material is simultaneously deposited in nucleation windows 22 and
20 26, but there it serves only as a nucleation site for first
semiconductor layer 28, not as an ohmic contact. In addition, the
heavily doped region 34 allows electrical communication between the
readout and the signal processing circuits 14 and the second
semiconductor layer 30 through a metallization layer 36 and the ohmic
25 contact 20. The ohmic contact 20 and 36 can be two different metals,
the ohmic contact 20 chosen to make good ohmic contact with the
heavily doped region 34, and the metallization layer 36 chosen to make
good ohmic contact with the second semiconductor layer 30, such as
platinum for n-type and gold for p-type. The metallization layer 36
30 must also be chosen to be a material on which nucleation of first
semiconductor layer 28 is suppressed.

When the second semiconductor layer 30 acts as the base of
the photodiode, the free charge carriers in the interior of the second
semiconductor layer 30 drift toward the interface with second
35 semiconductor layer 28 and recombine. The result of this
recombination is to reduce the efficiency with which free charge

1 carriers are collected by the first passivation layer 16. To reduce
the recombination velocity of the free charge carriers in the second
semiconductor layer 30 when the second semiconductor layer 30 acts as
the base of the photodiode, a third semiconductor layer 38 is
5 provided. The third semiconductor layer 38 may be fabricated from
mercury-cadmium-telluride having a stoichiometric relationship defined
by $\text{Hg}_{1-z}\text{Cd}_z\text{Te}$, in which the composition value of z is chosen to be
greater than y . It is to be understood, however, that other suitable
materials may be used such as mercury-cadmium-telluride, mercury-zinc-
10 telluride, mercury-cadmium-selenide, mercury-zinc-selenide, mercury-
cadmium-sulfide, mercury-zinc-sulfide, lead-tin-telluride, lead-tin-
selenide, lead-tin-sulfide, indium-arsenide-antimonide, gallium-
indium-antimonide, or gallium-antimonide-arsenide.

The structure 10 further includes an anti-reflection coating
15 40. The anti-reflection coating 40 is located on the third
semiconductor layer 38 and is used to reduce the reflection of
incident infrared radiation. The anti-reflection coating 40 is
manufactured from a material which has an index of refraction between
that of air and the third semiconductor layer 38. While the
20 anti-reflection coating 40 may be fabricated from zinc sulfide, zinc
selenide, or zinc telluride, other suitable materials may be used.
The structure 10 also comprises the field plate regions 42 which are
used to control the relative potential of the first and second
semiconductor layers 28 and 30 as well as the first passivation layer
25 16. The field plates 42 are located below the region where the first
and second semiconductor layers 28 and 30 intersect the first
passivation layer 16. The field plate regions 42 may either be doped
regions in the substrate 12 or metal deposited on the surface of the
substrate 12.

30 Control of electrical potential in the region where layers
28, 30 and 16 intersect is essential to device performance. To
control the electric potential in this region, the first passivation
layer 16 is chosen to provide stable surface potentials, near the flat
band potential, in the first and second semiconductor layers 28 and 30
35 (i.e., the first passivation layer 16 is chosen to passivate the first
and second semiconductor layers 28 and 30) and by using the field

1 plate regions 42 to compensate for any deviation from the flat band
condition by the use of an applied potential, in the same way as gates
are used to optimize photodiode performance in current practice.

5 The growth of the first and second semiconductor layers 28
and 30 over the first passivation layer 16 provides automatically a
self-passivated buried junction. The existence of field plate region
42 permits optimization of surface potential in the junction region by
gate-voltage control.

10 By providing a structure as described above, the performance
of the structure 10 may be optimized both from the signal processing
viewpoint as well as from that of infrared detection. The substrate
12 may be silicon, gallium arsenide, or germanium from which signal
processing circuits of optimum performance can be fabricated. The
first and second semiconductor layers 28 and 30 which are chosen from
15 a material which optimizes infrared detection are then deposited on
the substrate by heteroepitaxial selected area deposition. The
combination of this detector structure and the substrate 12 thus
constitute a monolithic heteroepitaxial focal plane array, and does
not suffer from the disadvantages associated with hybridized
20 structures.

The structure 10 may be fabricated in the manner described
below. Once the substrate 12 has been formed with the readout and
signal processing circuit 14, the heavily doped regions 32 and 34 as
well as the field plate regions 42 are formed. The passivation layers
25 16 and 18 are then deposited on the substrate 12. A contact window is
then opened by photolithography in the passivation layers 16 and 18
over the heavily doped region 34. A first layer of metal is applied
by vacuum deposition and lift-off so as to form the ohmic contact 20
for the heavily doped region 34. A second photolithographic step is
30 then performed to form the metallization layer 36. The shape of the
metallization layer 36 is chosen to form the boundary of the structure
10 and is selected to make ohmic contact with the second semiconductor
layer 30.

A third photolithographic step is then used to open the
35 nucleation windows 22-26 in the passivation layers 16 and 18. The
shape, size and spacing of the nucleation windows 22-26 are to be

1 determined by the desired detector geometry and characteristics of the
epitaxial growth process used. For example, if the lateral growth
from the nucleation window occurs at the same rate as the vertical
growth, then the windows should be spaced as far apart as they are
5 wide. The number of nucleation windows should also be minimized as an
excessive number of nucleation windows may place spacial constraints
on the readout and signal processing circuits 14 in the substrate 12.
The number and size of the nucleation windows 22-26 can be minimized
by maximizing the ratio of the lateral growth rate to the vertical
10 growth rate of the first semiconductor layer 28. In addition, the
ratio of the lateral growth rate to the vertical growth rate of the
second semiconductor layer 30 should also be maximized so as to
provide the largest possible distance between the junction between the
first and second semiconductor layers 28 and 30 and the metallization
15 layer 36. By making the first semiconductor layer 28 a thick layer,
the number of nucleation windows 22-26 required is reduced. Making
the second semiconductor layer 30 thicker allows more tolerance for
lateral growth rate variation since the distance between the
metallization layer 36 and the junction between the first and second
20 semiconductor layers 28 and 30 become larger.

After opening the nucleation windows 22-26 in the
passivation layers 28 and 30, the remaining photoresist is removed
from the passivation layer 16 and the substrate 12 is placed in a
low-temperature metallorganic vapor phase epitaxial reactor so that
25 in-situ clean-up of the surface of the substrate 12 can be performed.
The in-situ surface clean-up may involve ultraviolet ozone etching,
atomic hydrogen etching, or etching by other free radicals generated
from suitable reactant sources in an ultraviolet or plasma field.

Nucleation crystals are then grown in the nucleation windows
30 22-26 of the passivation layers 16 and 18. Because the material from
which the passivation layer 18 and the metallization layer 36 are
formed resist the formation of nucleation crystals, the nucleation
crystals only form in the nucleation windows 22-26. Reactant flow
into the metallorganic vapor phase epitaxial reactor is then changed
35 to grow the first semiconductor layer 28 which nucleates on the
nucleation crystals in the nucleation windows 22-26. The reactant

1 flow is then further changed to grow the second semiconductor layer
30. A final change in the reactant flow permits the growth of the
third semiconductor layer 38. Finally, the anti-reflection layer 40
is formed on the third semiconductor layer 38 by vacuum evaporation
5 outside the metallorganic vapor phase reactor.

It will therefore be seen that the present invention is able
to provide an apparatus for detecting infrared radiation in which the
infrared material can be selected to optimize infrared detection,
while the signal-processing material may be selected to optimize the
10 signal processing circuits. The present invention should therefore
not be judged in accordance with this specific example presented
herein. For example, other suitable area selective epitaxial growth
techniques may be used for forming the first semiconductor layer. The
relative doping of the first and second semiconductor layers may also
15 change, as well as the function which they perform (i.e., base or
collector). Other modifications will become apparent to the skilled
practitioner upon a study of the specification, drawings and
following claims.

CLAIMSWhat is Claimed is:

1 1. A monolithic structure for detecting infrared radiation comprising:

 a substrate having readout and signal processing circuits integrated therein, said substrate formed from a material selected
5 from the group consisting of silicon, gallium arsenide, or germanium;

 a first semiconductor layer grown on said substrate from a material selected from the group consisting of mercury-cadmium-telluride, mercury-zinc-telluride, mercury-cadmium-selenide, mercury-zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-
10 tin-telluride, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide;
and

 a second semiconductor layer grown on said first semiconductor layer, said first and second semiconductor layers
15 operable to deliver an electrical signal to said readout and signal processing circuits in said substrate in response to the infrared radiation received by said first and second semiconductor layers.

1 2. The apparatus of Claim 1, further comprising a first passivation layer disposed between said substrate and said first semiconductor layer.

1 3. The apparatus of Claim 2, further comprising a second passivation layer disposed between said first passivation layer and said first semiconductor layer.

1 4. The apparatus of Claim 3, wherein said first and second passivation layers comprises a plurality of nucleation windows operable to control the formation of said first semiconductor layer.

1 5. The apparatus of Claim 4, wherein nucleation of said
first semiconductor layer occurs only in said nucleation windows.

1 6. The apparatus of Claim 4, further comprising a third
semiconductor layer disposed on said second semiconductor layer, said
third semiconductor layer operable to reduce the surface recombination
velocity of the free charge carriers in said second semiconductor
5 layer.

1 7. The apparatus of Claim 6, wherein said first, second and
third semiconductor layers are grown by metallorganic vapor phase
epitaxy.

1 8. The apparatus of Claim 1, further comprising a layer of
anti-reflection material disposed on said third semiconductor layer.

1 9. A method for detecting infrared radiation comprising:
 exposing a first layer and a second layer of semiconductor
material to a source of infrared radiation, said first and second
semiconductor layers being formed from a material selected from the
5 group consisting of mercury-cadmium-telluride, mercury-zinc-telluride,
mercury-cadmium-selenide, mercury-zinc-selenide, mercury-cadmium-
sulfide, mercury-zinc-sulfide, lead-tin-telluride, lead-tin-selenide,
lead-tin-sulfide;
 generating a photocurrent in said first and second layers of
10 semiconductor material; and
 sensing said photocurrent by readout and signal processing
circuits disposed within a substrate upon which said first and second
semiconductor layers are grown, said substrate being formed of a
material selected from the group consisting of silicon, gallium
15 arsenide, or germanium.

1 10. The method of Claim 9, wherein said first layer of
semiconductor material, said second layer of semiconductor material
and said substrate comprise a monolithic structure.

1 11. The method of Claim 9, wherein said first layer of semiconductor material is separated from said substrate by a first passivation layer.

1 12. The method of Claim 11, wherein said first passivation layer is separated from said first layer of semiconductor material by a second passivation layer.

1 13. The method of Claim 12, wherein said first and second passivation layers comprise a plurality of nucleation windows operable to control formation of said first layer of semiconductor material.

1 14. The method of Claim 9, comprising the additional step of reducing the surface recombination velocity of free charge carriers in said second layer of semiconductor material by disposing a third layer of semiconductor material on said second layer of semiconductor material.
5

1 15. The method of Claim 14, wherein said first, second, and third semiconductor layers are formed by metallorganic vapor phase epitaxy.

1 16. The method of Claim 9, further comprising the additional step of allowing infrared radiation to pass through a layer of anti-reflection material.

1 17. An array of monolithic structures for detecting infrared radiation, each of said monolithic structures comprising:

5 a substrate having readout and signal processing circuits integrated therein, said substrate formed from a material selected to optimize performance of said readout and signal processing circuits;

a first semiconductor layer grown on said substrate from a material selected to optimize infrared detection;

a plurality of passivation layers disposed between said substrate and said first layer of semiconductor material;

10 a second semiconductor layer disposed on said first semiconductor layer operable to deliver an electrical signal to said readout and signal processing circuits in said substrate in response to the infrared radiation received by said first and second semiconductor layers;

15 a third semiconductor layer disposed on said second semiconductor layer operable to reduce the surface recombination velocity of the free charge carriers in said second semiconductor layer; and

20 an anti-reflection coating disposed on the third semiconductor layer, said anti-reflection coating having an index of refraction between that of air and the third semiconductor layer.

1 18. The array of Claim 17, wherein said plurality of passivation layers comprise a plurality of nucleation windows operable to control the growth of said first semiconductor layer.

1 19. The array of Claim 18, wherein one of said nucleation windows permits electrical communication between said first semiconductor layer and said readout and signal processing circuits.

1 20. The array of Claim 19, wherein said monolithic structure further comprises an ohmic contact permitting electrical communication between said first and second semiconductor layers and said read out and signal processing circuits.

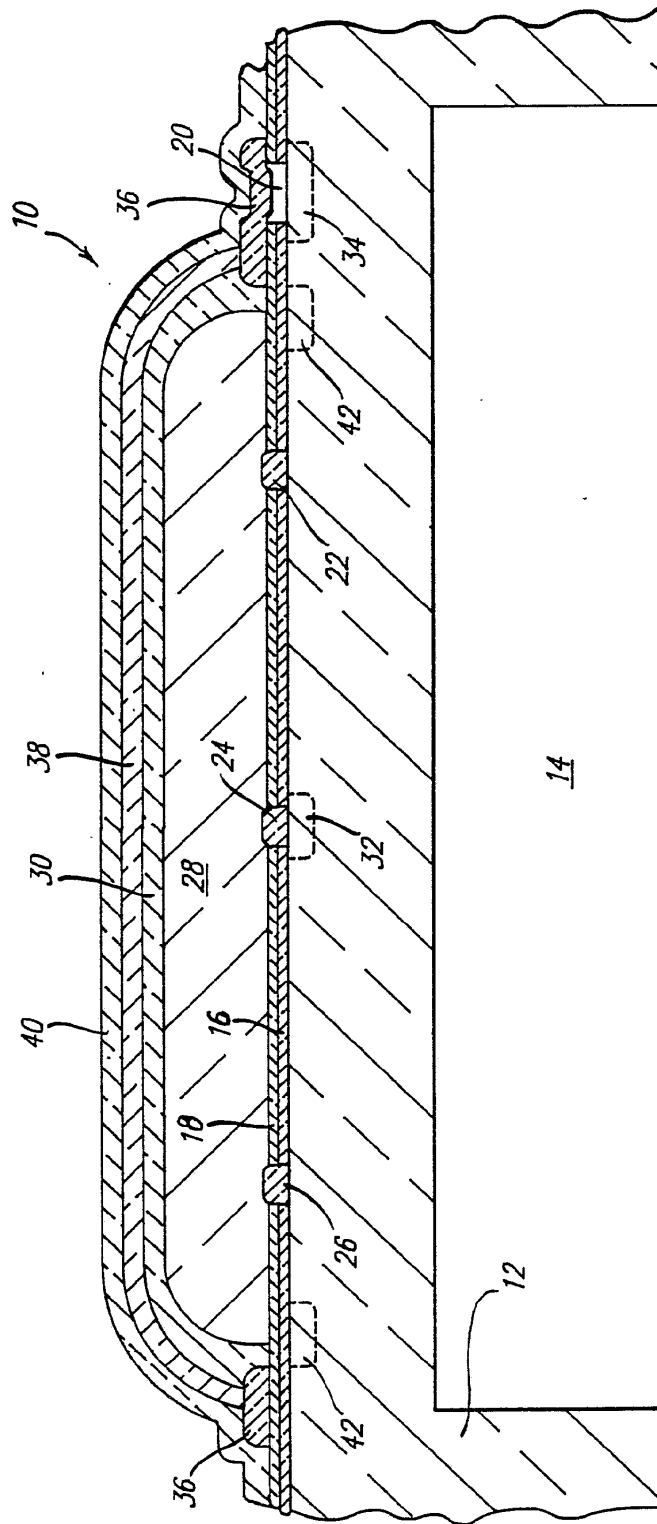
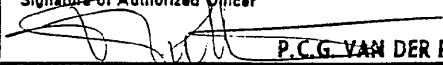


FIG. 1.

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 88/03792

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) *		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC4: H 01 L 31/08, 27/14, G 01 J 5/20		
II. FIELDS SEARCHED		
Minimum Documentation Searched *		
Classification System	Classification Symbols	
IPC4	H 01 L, G 01 J	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched *		
III. DOCUMENTS CONSIDERED TO BE RELEVANT *		
Category *	Citation of Document, ** with indication, where appropriate, of the relevant passages **	Relevant to Claim No. **
X	US, A, 4559695 (I.M. BAKER) 24 December 1985, see column 3, line 8 - column 6, line 34; abstract; figures 1,6	1,17
A	--	9
X	US, A, 4521798 (I.M. BAKER) 4 June 1985, see column 3, line 6 - column 6, line 34; abstract; figures 1,6	1,17
A	--	9
A	EP, A2, 0137988 (TEXAS INSTRUMENTS INCORPORATED) 24 April 1985, see abstract; figure 1	1-3,8,9, 16,17
A	US, A, 4614960 (N. BLUZER) 30 September 1986, see abstract; figures 3,4	1,9, 17
<p>* Special categories of cited documents: **</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&" document member of the same patent family</p>		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	
14th April 1989	28. 04. 89	
International Searching Authority	Signature of Authorized Officer	
EUROPEAN PATENT OFFICE	 P.C.G. VAN DER PUTTEN	

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)		
Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	US, A, 4549195 (N. BLUZER) 22 October 1985, see abstract; figures 2,3,5 --	1,9, 17
A	US, A, 4313127 (S.C. SU ET AL) 26 January 1982, see abstract; figure 1 --	1,17
A	US, A, 4053919 (A.M. ANDREWS, II ET AL) 11 October 1977, see abstract; figure 2 --	1,9, 17
A	IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. ED-25, No. 2, February 1978, N. Bluzer et al: "Buffered Direct Injection of Photocurrents into Charge-Coupled Devices ", see page 160 - page 166 cited in the application -- -----	1,9, 17

ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO.

PCT/US 88/03792

SA 26299

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on 03/03/89
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4559695	24/12/85	EP-A-B- 0061803 GB-A-B- 2095905 JP-A- 57171226 US-A- 4521798	06/10/82 06/10/82 21/10/82 04/06/85
US-A- 4521798	04/06/85	EP-A-B- 0061803 GB-A-B- 2095905 JP-A- 57171226 US-A- 4559695	06/10/82 06/10/82 21/10/82 24/12/85
EP-A2- 0137988	24/04/85	US-A- 4447291 EP-A- 0288792 JP-A- 60094764 US-A- 4684812 US-A- 4686373	08/05/84 02/11/88 27/05/85 04/08/87 11/08/87
US-A- 4614960	30/09/86	NONE	
US-A- 4549195	22/10/85	NONE	
US-A- 4313127	26/01/82	NONE	
US-A- 4053919	11/10/77	NONE	

EPO FORM P079

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

Attorney Docket No.: 309-0015USCIPDIV
Confirmation No.: 5818

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shih-Yuan WANG	Examiner: EDUARDO A RODELA
Application No.: 18/822,880	Art Unit: 2893
Filed: September 3, 2024	CERTIFICATE OF TRANSMISSION
Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 /Mary Ellen Finnegan/ Date: December 5, 2024 Name: Mary Ellen Finnegan

VIA EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

A copy of the non-U.S. patent document is enclosed herewith, in compliance with 37 CFR 1.98.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov
Registration No. 25,161
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Attorney's E-mail: ikavrukov@wissingmiller.com

Application Number * 18/822,880 *	Application/Control No. 18/822,880	Applicant(s)/Patent under Reexamination WANG et al.	
	Examiner RODELA, EDUARDO A	Art Unit 2893	
Document Code - DISQ		Internal Document - DO NOT MAIL	

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed: <u>22 November 2024</u>	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
/JEAN PROCTOR/ Technology Center: <u>OPLC</u> Telephone: <u>(571)272-1040</u> <u>16 td's</u>



UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
18/822,880

RECEIPT DATE / TIME
11/22/2024 10:17:10 AM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68074993	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_ResponseToFirstOfficeActionDated19Nov2024-Final.pdf	6	Amendment Copy Claims/Response to Suggested Claims	494 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV_ResponseToFirstOfficeActionDated19Nov2024-Final.pdf	5F24725AB9DFFD839699EE2DBC51A2C5C44DB3BC415D1991 CCEE2CE6808BCB6C616C6869DD7D1F11E150B30BE0520523 1FC184D2A67088158A39000F92CE5809

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Shih-Yuan WANG et al.
Serial No.: 18/822,880
Examiner: EDUARDO A RODELA
Group Art Unit 2893
Filing Date: 09/03/2024
For: MICROSTRUCTURE ENHANCED ABSORPTION
PHOTOSENSITIVE DEVICES
Conf. No. 5818

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: November 22, 2024

I hereby certify that this correspondence is being transmitted via
Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the non-final Office Action dated 11/19/2024, please amend the above-
identified application as follows:

Amendments to the Claims:

Please rewrite the claims as follows. These amended claims replace all previously filed claims:

1. (currently amended) An integrated structure comprising:
 - an array of pillars comprising Si, Ge, and/or SiGe alloy semiconductor material,
 - wherein at least some of the pillars are configured to include photodetectors and have respective light-receiving surfaces and respective sides;
 - wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;
 - one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other shapes at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;
 - ~~wherein at least some of the holes are elongated along the respective light-receiving surfaces;~~
 - side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;
 - a solid dielectric material forming a base dielectric region for the array;
 - electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;
 - wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes.
2. (previously presented) The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices.

3. (canceled) The integrated circuit of claim 1, in which at least some of the holes are elongated along the respective light-receiving surfaces.
4. (currently amended) The integrated structure of claim ~~3~~1, wherein each of at least some of the pillars has a plurality of the elongated holes.
5. (currently amended) The integrated structure of claim ~~3~~1, wherein each of at least some of the pillars has only one of the elongated holes.
6. (currently amended) The integrated structure of claim ~~3~~1, in which the light-receiving surfaces have respective widths, and the elongated holes extend along less than the widths of the light-receiving surfaces of at least some of the pillars in which the holes are fabricated.
7. (currently amended) The integrated structure of claim 6 in which each of at least some of the elongated holes has at least one closed contour remote from respective side edges of the light-receiving surface in which the hole is fabricated.
8. (previously presented) The integrated structure of claim 1, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors.
9. (previously presented) The integrated structure of claim 1, in which two or more of the photodetectors share one of the electrical contacts.
10. (previously presented) The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission.

11. (previously presented) The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors.
12. (previously presented) The integrated structure of claim 1, in which each of at least some of the photodetectors is configured such that the light passes through at least a part of the one of the P-doped region and N-doped region of the photodetector before reaching any part of the other doped region of the photodetector.
13. (previously presented) The integrated structure of claim 1, in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the P-doped region before reaching any part of the N-doped region.
14. (previously presented) An integrated structure comprising:
 - an array of pillars comprising Si, Ge, and/or alloyed SiGe semiconductor material, wherein at least some of the pillars have respective sides and respective light-receiving surfaces with selected widths and comprise at least one photodetector;
 - wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;
 - one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars,
 - wherein each of the holes (i) has an elongated shape extending in length over less than the width of the light-receiving surface in which the hole is fabricated, (ii) has at least one closed contour at the light-receiving surface in which the hole is fabricated, (ii) extends into the pillar in which the hole is fabricated to a depth of 100 to 10000 nm, and (iv) is filled at least partly with solid dielectric material;

side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;
a solid dielectric material forming a base dielectric region for the array;
electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;
wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the holes; and
wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission.

15. (previously presented) The integrated structure of claim 14, in which each of at least some of the pillars has only one of the elongated holes fabricated therein.
16. (previously presented) The integrated structure of claim 14, in which each of at least some of the pillars has at least two of the elongated holes.
17. (previously presented) The integrated structure of claim 14, in which each of at least some of the photodetectors includes at least one of the holes.

REMARKS

Applicant submits that the application is in condition for allowance because claim 1 has been combined with the subject matter of claim 3 (now canceled), which the Office Action stated would be allowable if placed in independent form. Dependent claims 2 and 4-13 claims now depend on amended claim 1 that includes the subject matter of allowable claim 3. The Office Action states that the remaining claims, which are claims 14-17, are allowed.

Applicant believes that the rejected claims patentably differ from the applied references but, for the sake of having the subject application lead to a patent as soon as possible, plans to take up that question in a future divisional application.

Applicant hereby makes of record a brief communication with the Examiner on 11/12/2024 to identify a 2013 priority provisional application and two papers filed in the immediate parent of the subject application, and another brief communication on 11/22/2024 advising the Examiner of the filing of Terminal Disclaimers.

Applicant invites the Examiner to telephone the undersigned if it appears that a call may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

WISSING MILLER LLP
Attorney for Applicants

By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel.: (917) 945-0121

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV
<p>In re Application of: Shih-Yuan WANG</p> <p>Application No.: 18/822,880</p> <p>Filed: September 3, 2024</p> <p>For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES</p> <p>The applicant, <u>W&WSENS DEVICES, INC.</u>, owner of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. <u>11,309,444</u> as the term of said prior patent is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.</p> <p>In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:</p> <ul style="list-style-type: none">expires for failure to pay a maintenance fee;is held unenforceable;is found invalid by a court of competent jurisdiction;is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;has all claims canceled by a reexamination certificate;is reissued; oris in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. <p>Check either box 1 or 2 below, if appropriate.</p> <p>1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.</p> <p>I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p>2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>25,161</u></p> <div style="margin-top: 20px;"><div style="display: flex; justify-content: space-between;"><div style="width: 60%; text-align: center;"><u>/Ivan S. Kavrukov/</u> Signature</div><div style="width: 35%; text-align: center;"><u>November 22, 2024</u> Date</div></div><div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Ivan S. Kavrukov</u> Typed or printed name</div><div style="width: 35%;"></div></div><div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Attorney of Record</u> Title</div><div style="width: 35%; text-align: center;"><u>917-945-0121</u> Telephone Number</div></div></div> <p>☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.</p> <p style="text-align: center;">WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</p>	

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT		Docket Number (Optional) 309-0015USCIPDIV
<p>In re Application of: Shih-Yuan WANG</p> <p>Application No.: 18/822,880</p> <p>Filed: September 3, 2024</p> <p>For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES</p> <p>The applicant, <u>W&WSENS DEVICES, INC.</u>, owner of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. <u>11,830,954</u> as the term of said prior patent is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.</p> <p>In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:</p> <ul style="list-style-type: none">expires for failure to pay a maintenance fee;is held unenforceable;is found invalid by a court of competent jurisdiction;is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;has all claims canceled by a reexamination certificate;is reissued; oris in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. <p>Check either box 1 or 2 below, if appropriate.</p> <p>1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.</p> <p>I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p>2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>25,161</u></p> <div style="display: flex; justify-content: space-between; margin-top: 20px;"><div style="width: 60%; text-align: center;"><u>/Ivan S. Kavrukov/</u> Signature</div><div style="width: 35%; text-align: center;"><u>November 22, 2024</u> Date</div></div> <div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Ivan S. Kavrukov</u> Typed or printed name</div><div style="width: 35%;"></div></div> <div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Attorney of Record</u> Title</div><div style="width: 35%; text-align: center;"><u>917-945-0121</u> Telephone Number</div></div> <p>☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.</p> <p style="text-align: center; font-weight: bold; margin-top: 10px;">WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</p>		

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<p>In re Application of: Shih-Yuan WANG</p> <p>Application No.: 18/822,880</p> <p>Filed: September 3, 2024</p> <p>For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES</p> <p>The applicant, <u>W&WSENS DEVICES, INC.</u>, owner of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. <u>10,622,498</u> as the term of said prior patent is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.</p> <p>In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:</p> <ul style="list-style-type: none">expires for failure to pay a maintenance fee;is held unenforceable;is found invalid by a court of competent jurisdiction;is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;has all claims canceled by a reexamination certificate;is reissued; oris in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. <p>Check either box 1 or 2 below, if appropriate.</p> <p>1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.</p> <p>I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p>2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>25,161</u></p> <div style="display: flex; justify-content: space-between; margin-top: 20px;"><div style="width: 60%; text-align: center;"><u>/Ivan S. Kavrukov/</u> Signature</div><div style="width: 35%; text-align: center;"><u>November 22, 2024</u> Date</div></div> <div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Ivan S. Kavrukov</u> Typed or printed name</div><div style="width: 35%;"></div></div> <div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Attorney of Record</u> Title</div><div style="width: 35%; text-align: center;"><u>917-945-0121</u> Telephone Number</div></div> <p>☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.</p> <p style="text-align: center;">WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</p>	

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**TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING
REJECTION OVER A PENDING "REFERENCE" APPLICATION**

Docket Number (Optional)
309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending **reference** Application Number 18/113,474 filed, February 23, 2023, as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the **reference** application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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2. ☒ The undersigned is an attorney or agent of record. Reg. No. 25,161

_____ Signature	_____ Date
Ivan S. Kavrukov Typed or printed name	
_____ Title	_____ Telephone Number
Attorney of Record 917-945-0121	

- ☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV
<p>In re Application of: Shih-Yuan WANG</p> <p>Application No.: 18/822,880</p> <p>Filed: September 3, 2024</p> <p>For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES</p> <p>The applicant, <u>W&WSENS DEVICES, INC.</u>, owner of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. <u>9,818,893</u> as the term of said prior patent is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.</p> <p>In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:</p> <ul style="list-style-type: none">expires for failure to pay a maintenance fee;is held unenforceable;is found invalid by a court of competent jurisdiction;is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;has all claims canceled by a reexamination certificate;is reissued; oris in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. <p>Check either box 1 or 2 below, if appropriate.</p> <p>1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.</p> <p>I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p>2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>25,161</u></p> <div style="display: flex; justify-content: space-between; margin-top: 20px;"><div style="width: 60%; text-align: center;"><u>/Ivan S. Kavrukov/</u> Signature</div><div style="width: 35%; text-align: center;"><u>November 22, 2024</u> Date</div></div> <div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Ivan S. Kavrukov</u> Typed or printed name</div><div style="width: 35%;"></div></div> <div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Attorney of Record</u> Title</div><div style="width: 35%; text-align: center;"><u>917-945-0121</u> Telephone Number</div></div> <p>☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.</p> <p style="text-align: center;">WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</p>	

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV
<p>In re Application of: Shih-Yuan WANG</p> <p>Application No.: 18/822,880</p> <p>Filed: September 3, 2024</p> <p>For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES</p> <p>The applicant, <u>W&WSENS DEVICES, INC.</u>, owner of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. <u>11,621,360</u> as the term of said prior patent is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.</p> <p>In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:</p> <ul style="list-style-type: none">expires for failure to pay a maintenance fee;is held unenforceable;is found invalid by a court of competent jurisdiction;is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;has all claims canceled by a reexamination certificate;is reissued; oris in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. <p>Check either box 1 or 2 below, if appropriate.</p> <p>1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.</p> <p>I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p>2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>25,161</u></p> <div style="display: flex; justify-content: space-between; margin-top: 20px;"><div style="width: 60%; text-align: center;"><u>/Ivan S. Kavrukov/</u> Signature</div><div style="width: 35%; text-align: center;"><u>November 22, 2024</u> Date</div></div> <div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Ivan S. Kavrukov</u> Typed or printed name</div><div style="width: 35%;"></div></div> <div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Attorney of Record</u> Title</div><div style="width: 35%; text-align: center;"><u>917-945-0121</u> Telephone Number</div></div> <p>☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.</p> <p style="text-align: center; font-weight: bold; margin-top: 10px;">WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</p>	

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<p>In re Application of: Shih-Yuan WANG</p> <p>Application No.: 18/822,880</p> <p>Filed: September 3, 2024</p> <p>For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES</p> <p>The applicant, <u>W&WSENS DEVICES, INC.</u>, owner of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. <u>9,525,084</u> as the term of said prior patent is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.</p> <p>In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:</p> <ul style="list-style-type: none">expires for failure to pay a maintenance fee;is held unenforceable;is found invalid by a court of competent jurisdiction;is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;has all claims canceled by a reexamination certificate;is reissued; oris in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. <p>Check either box 1 or 2 below, if appropriate.</p> <p>1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.</p> <p>I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p>2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>25,161</u></p> <div style="margin-top: 20px;"><div style="display: flex; justify-content: space-between;"><div style="width: 60%; text-align: center;"><u>/Ivan S. Kavrukov/</u> Signature</div><div style="width: 35%; text-align: center;"><u>November 22, 2024</u> Date</div></div><div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Ivan S. Kavrukov</u> Typed or printed name</div><div style="width: 35%;"></div></div><div style="display: flex; justify-content: space-between; margin-top: 10px;"><div style="width: 60%; text-align: center;"><u>Attorney of Record</u> Title</div><div style="width: 35%; text-align: center;"><u>917-945-0121</u> Telephone Number</div></div></div> <p>☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.</p> <p style="text-align: center;">WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</p>	

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<p>In re Application of: Shih-Yuan WANG</p> <p>Application No.: 18/822,880</p> <p>Filed: September 3, 2024</p> <p>For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES</p> <p>The applicant, <u>W&WSENS DEVICES, INC.</u>, owner of <u>100</u> percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent No. <u>12,094,903</u> as the term of said prior patent is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.</p> <p>In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:</p> <ul style="list-style-type: none">expires for failure to pay a maintenance fee;is held unenforceable;is found invalid by a court of competent jurisdiction;is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;has all claims canceled by a reexamination certificate;is reissued; oris in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer. <p>Check either box 1 or 2 below, if appropriate.</p> <p>1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.</p> <p>I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p>2. ☒ The undersigned is an attorney or agent of record. Reg. No. <u>25,161</u></p> <div style="margin-top: 20px;"><div style="display: flex; justify-content: space-between;"><div style="width: 60%; text-align: center;"><u>/Ivan S. Kavrukov/</u> Signature</div><div style="width: 35%; text-align: center;"><u>November 22, 2024</u> Date</div></div><div style="display: flex; justify-content: center; margin-top: 10px;"><u>Ivan S. Kavrukov</u> Typed or printed name</div><div style="display: flex; justify-content: space-between; margin-top: 20px;"><div style="width: 40%; text-align: center;"><u>Attorney of Record</u> Title</div><div style="width: 20%;"></div><div style="width: 35%; text-align: center;"><u>917-945-0121</u> Telephone Number</div></div></div> <p>☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.</p> <p style="text-align: center;">WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</p>	

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UNITED STATES
PATENT AND TRADEMARK OFFICE

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Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
18/822,880

RECEIPT DATE / TIME
11/22/2024 09:56:49 AM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 5818

FILED BY Mary Ellen Finnegan

PATENT CENTER # 68074574

FILING DATE 09/03/2024

CUSTOMER # 139982

FIRST NAMED
INVENTOR Shih-Yuan WANG

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 16

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_TerminalDisclaimer_9496435.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIPDIV_TerminalDisclaimer_9525084.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIPDIV_TerminalDisclaimer_9530905.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIPDIV_TerminalDisclaimer_10446700.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIPDIV_TerminalDis	2	Terminal Disclaimer Filed	157 KB

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309-0015USCIPDIV_TerminalDisclaimer_9818893.pdf	2	Terminal Disclaimer Filed	157 KB
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309-0015USCIPDIV_TerminalDisclaimer_10700225.pdf	2	Terminal Disclaimer Filed	157 KB
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309-0015USCIPDIV_TerminalDisclaimer_11309444.pdf	2	Terminal Disclaimer Filed	157 KB
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309-0015USCIPDIV_TerminalDisclaimer_11791432.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIPDIV_TerminalDisclaimer_11830954.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIPDIV_TerminalDisclaimer_12094903.pdf	2	Terminal Disclaimer Filed	152 KB
309-0015USCIPDIV_TerminalDisclaimer_12087871.pdf	2	Terminal Disclaimer Filed	152 KB
309-0015USCIPDIV_TerminalDisclaimer_18113474.pdf	2	Terminal Disclaimer Filed	240 KB

Digest

DOCUMENT

MESSAGE DIGEST(SHA-512)

309-	2B4147910C8282F7BF1EB7C64080B3F21C4817E2045762CB36
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0015USCIPDIV_TerminalDiscla imer_9496435.pdf	7508CAF35772E8599D6B989038764B76C28EDDA911FBE8527 77BA54BE1AAB5615C28249F43937F
309- 0015USCIPDIV_TerminalDiscla imer_9525084.pdf	DFFD012C3F11DFD75DAB7246539DAF1967949DBC04F4A5EE 3F635C199060BC23C1733A863EB7C5721D233B131A50EC1D5 12C464D3D639E5FE767B1BE7EA0030F
309- 0015USCIPDIV_TerminalDiscla imer_9530905.pdf	5BFD4C8AD03BDA433B3855E7FA65DD53B24CD91DC3134DE 2C79FAF1FB05A7F725F1CDE3088966AFE0CA7886678446770 5FCC01BD6E200CFA63BF0E2FCD32E13C
309- 0015USCIPDIV_TerminalDiscla imer_10446700.pdf	16A8600C4B26EC603F9A31B872386FEBDD8BA56F5BA2EFE 727E7B1B4C6ACC80BB1623C9F8EE90E21B50ACF9AA93831E 545B755E5218312CE7DB7C56616570C2
309- 0015USCIPDIV_TerminalDiscla imer_10468543.pdf	7E1A5AB5AB6E14B1966B54F34B313DEE181AFB71E12FD026 BA915CBD0098F2467B7D574F2F4F33B8DCE59F9B8057D543D 5696157F3A213B1C5C623C46790778C
309- 0015USCIPDIV_TerminalDiscla imer_9818893.pdf	D97F8DF91003DE105C7FEE03A0D4E97DFFA8AAF973A1D5AB D7468DD5560B133A6AAE5E75CA683FE88EB0B781A940A6C8 A0F96CD3CDA81B29C454D0B903FBCB2C
309- 0015USCIPDIV_TerminalDiscla imer_10622498.pdf	29BF8C32E0D35C827ABCF33683A26A4BAF4E343FF533ADE4 2F82198E87C008B6919871B49FD3D29A980D8C24710B7575E8 F42AAAD987D4A12954A5EEDF42EB0E
309- 0015USCIPDIV_TerminalDiscla imer_10700225.pdf	7FBEA9021B4D966A3D1C8CBA38CC168531F1BE8D689714A0 768C606FFCBC13895640F7354AE66049903E6E06F31ADFA4C DFA8245C18EC596D4B3964E1D2CBD9E
309- 0015USCIPDIV_TerminalDiscla imer_11121271.pdf	08824038B7C3EC8DA5CA8E836285B9E4CE47772CC2EE41D0 4A39815505292AA8D1AA751285F7397A3C6BEDD61EC796C0C E1B9ABBB9C7E95F8122B5930F4C385D
309- 0015USCIPDIV_TerminalDiscla imer_11309444.pdf	6343B871F1F9FEF984598EB96CAD0033A4D89C66BAD825573 EA0CF64F9EE1A7BD186E841B6CAB2B4AD6ECF903DC9B1C8 021480EAB78DFAC227FB9EE65B3566D3
309- 0015USCIPDIV_TerminalDiscla imer_11621360.pdf	49D6090A9231CA6F7070E240A154459E2808B4A24125C9D532 8619642D3B392BFB7CE10433CE3451AF44B61BD4163C43E15 D9A0184142169055AE03C4BB7DAFD
309- 0015USCIPDIV_TerminalDiscla imer_11791432.pdf	308A7842FD3538142FEC0D215BAE467182DDDBEB3DF56A8F EBE61FE474CAEF6CF772A784D4F1AD57DC8231AF93AF939F DBF77651286238694B9A1F5C4722DA20
309- 0015USCIPDIV_TerminalDiscla imer_11830954.pdf	8AED14F22C0CCEF2EAC478BE1D91B0243E2AAB8D54A22435 3548E3872AB63E907B720AABE7F70454D4A5731C525317BBD 406F120E4452643278F4D8959E99D9A
309- 0015USCIPDIV_TerminalDiscla imer_12094903.pdf	596F5B5ADDB216438FBD1FCDB19B80EACDE0949FA8FF9FB E229A3F79AA2464CEBAEB4C01A34DDD5EBFEE4C6A7E6CF9 639657ECA37DAA98932753F44B9DC27EDD

309-0015USCIPDIV_TerminalDiscla mer_12087871.pdf	8EF2A5E88259C2F89D7F0F7745C5E7B9096A773FE1A463B00 3CCEA5487F54EB7CD7FE76BE8999E1673913EDE84CA0DAE CC34CAB5F35408E47DB9073319FC1ED5
309-0015USCIPDIV_TerminalDiscla mer_18113474.pdf	FA49F2D7A3014A5C6B006FA9D067E0C21E8D548FABB034280 A21A8AF1ECB901D8A61B539799C7FC1E7A20761B076E90A49 C3A50A5139D473D306CA70FC5F0B20

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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ELECTRONIC PAYMENT RECEIPT

APPLICATION #
18/822,880

RECEIPT DATE / TIME
11/22/2024 09:56:49 AM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68074574	AUTHORIZED BY	Ivan Kavrukov
CUSTOMER #	139982	FILING DATE	09/03/2024
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Shih-Yuan WANG

Payment Information

PAYMENT METHOD CARD / 2892	PAYMENT TRANSACTION ID E2024AL057568526	PAYMENT AUTHORIZED BY Mary Ellen Finnegan
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PRE-AUTHORIZED ACCOUNT 600125	PRE-AUTHORIZED CATEGORY 37 CFR 1.21 (Miscellaneous fees and charges)
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FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
2814	STATUTORY DISCLAIMER, INCLUDING TERMINAL DISCLAIMER	170.00	16	2720.00
TOTAL AMOUNT:				\$2,720.00

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 18/822,880	Filing Date 09/03/2024	☐ To be Mailed	
ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO							
APPLICATION AS FILED - PART I							
FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x \$40 =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x \$ 192 =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL			
APPLICATION AS AMENDED - PART II							
	(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	11/22/2024	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 17	Minus ** 20	= 0	x \$40 =	0	
	Independent (37 CFR 1.16(h))	* 2	Minus *** 3	= 0	x \$ 192 =	0	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0	
	(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x \$0 =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x \$0 =		
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.					LIE		
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".					/VICTORIA JOHNSON/		
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".							
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818
139982	7590	11/19/2024	EXAMINER	
Wissing Miller LLP			RODELA, EDUARDO A	
Industrious at Hudson Yards			ART UNIT	
31 Hudson Yards, 11th Floor			PAPER NUMBER	
New York, NY 10001			2893	
			NOTIFICATION DATE	
			DELIVERY MODE	
			11/19/2024	
			ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

DETAILED ACTION

This correspondence is in response to the communications received October 31, 2024. Claims 1-17 are pending. This office action is being examined under an expedited “special” status due to Applicant’s Age, see “Petition Decision” document dated October 28, 2024 in the file wrapper.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority

The first instance of pillars having recesses formed therein can be found in provisional application 61/834,873 (dated June 13, 2013), on pg. 39. Therefore, the instant application’s effective date is **June 13, 2013**.

Relevant Prior Art

Yu et al. (US 9,515,218) Fig. 8A, shown below. This reference alone cannot be used to reject claim 1, but has similar structures depicting the state of the art at the time of the invention.

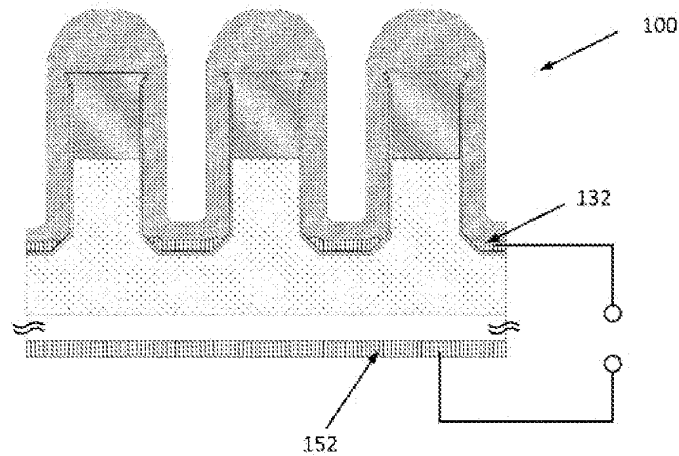


Fig. 8A

Hazeghi et al. (US 2013/0125965) Fig. 1 shown below. This reference alone cannot be used to reject claim 1, but has similar structures depicting the state of the art at the time of the invention.

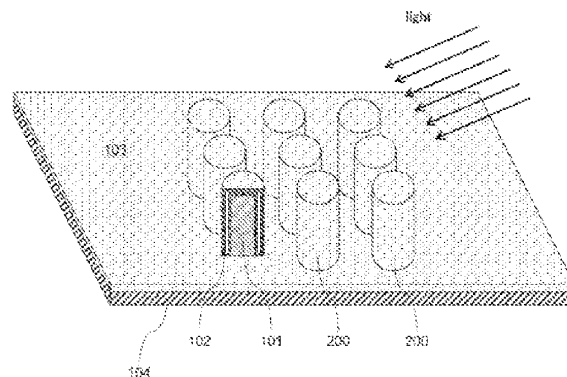
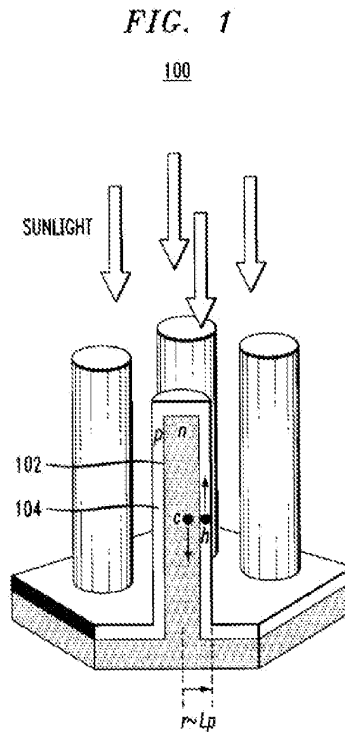
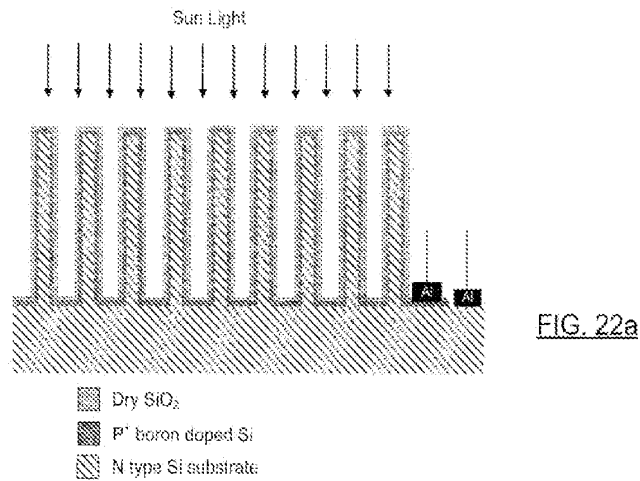


FIG. 1

Graham et al. (US 2012/0196401) Fig. 1, shown below. This reference alone cannot be used to reject claim 1, but has similar structures depicting the state of the art at the time of the invention.



Lal et al. (US 9,263,519) Fig. 22a shows the specifics about electrical connections, see below. This reference alone cannot be used to reject claim 1, but has similar structures depicting the state of the art at the time of the invention.



Applicant's Claim to Figure Comparison

It is noted that this comparison is merely for the benefit of reviewers of this office action during prosecution, to allow for an understanding of the examiner's interpretation of the Applicant's independent claims as compared to disclosed embodiments in Applicant's Figures. No response or comments are necessary from Applicant.

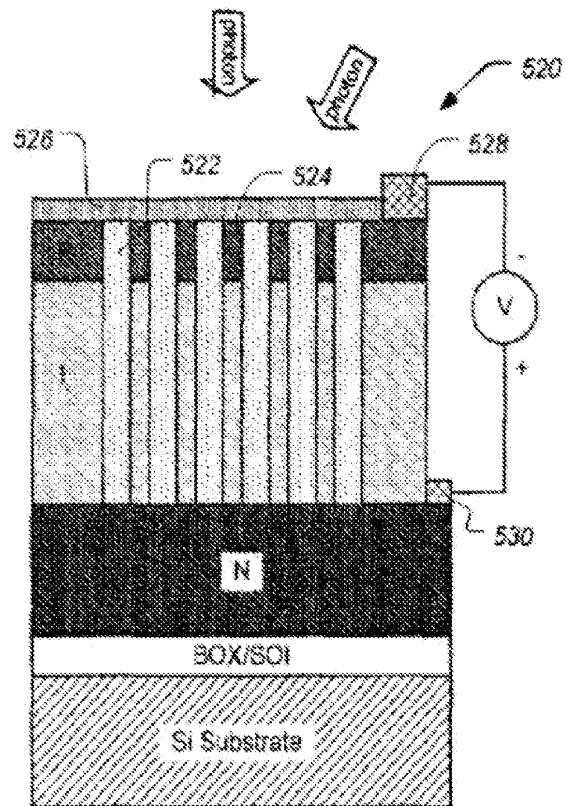


FIG. 5B

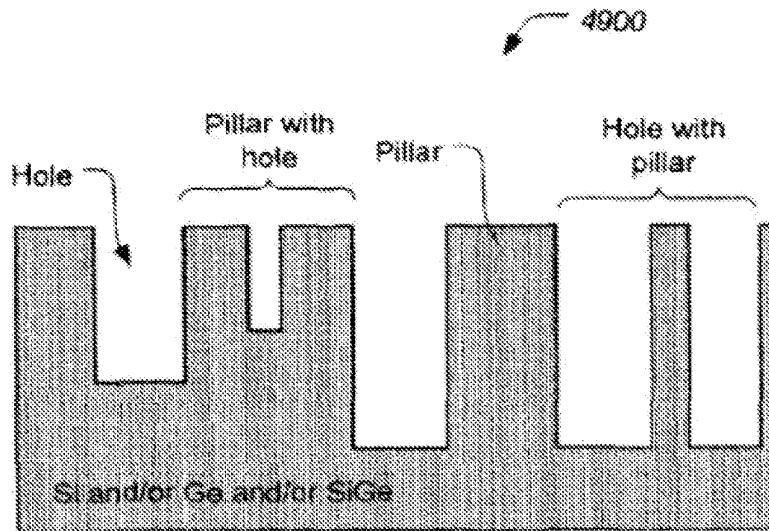


FIG. 49

Regarding claim 1, the Applicant discloses in Figs. 5B and 49, an integrated structure comprising:

an array of pillars (“pillars 524”, ¶ 0132) comprising Si, Ge, and/or SiGe alloy semiconductor material, wherein at least some of the pillars are configured to include **photodetectors** and have respective light-receiving surfaces and respective sides (“The PD (and APO) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area)”, ¶ 0132);

wherein at least some of the pillars comprise P-doped and N- doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers (“The PD (and APO) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area)”, ¶ 0132);

one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other shapes at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;

side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;

a solid dielectric material forming a base dielectric region for the array;

electrical contacts configured to provide electrical pathways coupled electrically to at least some of the **photodetectors**, including for selected reverse-biasing thereof;

wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the **photodetectors** relative to like **photodetectors** lacking said holes.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 8, 9 and 12 are rejected under 35 U.S.C. 103 as being unpatentable over Yu et al. (US 2011/0309331) in view of Lunev et al. (US 2014/0016660, used to represent the provisional application 61/670,808 whose effective date is July 12, 2012) in view of Counil et al. (US 2010/0116332) in view of Arimoto et al. (US 5,759,292).

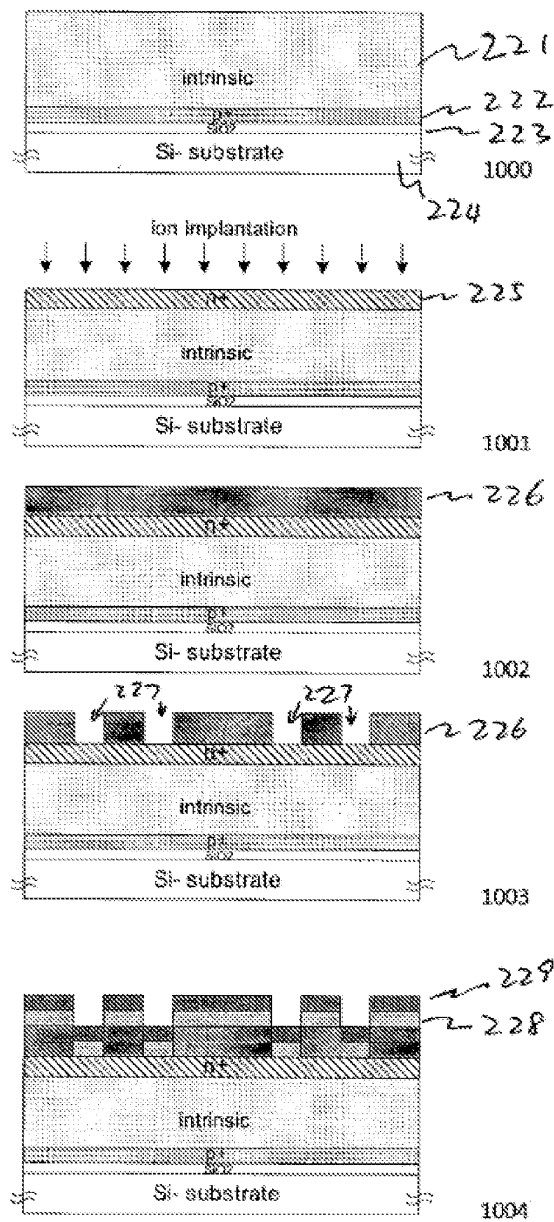
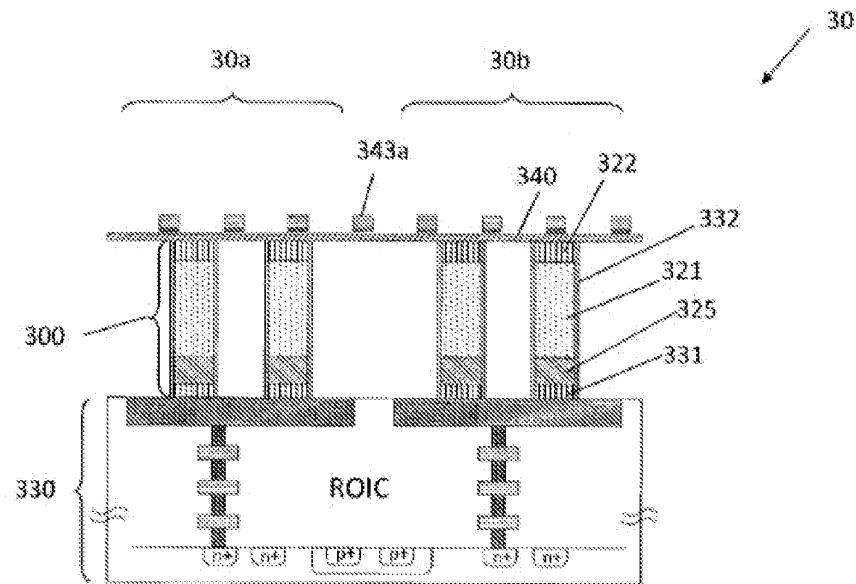


Fig. 4



Regarding claim 1, the prior art of Yu discloses in Figs. 4 and 5, an integrated structure comprising:

an array of pillars (“nanowires 300”, ¶ 0079) comprising Si, Ge, and/or SiGe alloy semiconductor material (“wherein the silicon substrate 224 comprises an silicon oxide layer 223 thereon and the first heavily doped semiconductor layer 222 (e.g. heavily doped p type silicon) on the silicon oxide layer 223.”, ¶ 0050, and layers 221 and 225 are silicon as well, “the second heavily doped semiconductor layer 225 (e.g. heavily doped n type silicon) is fabricated on the layer 221 by a method such as ion implantation and subsequent annealing.”, ¶ 0051), wherein at least some of the pillars are configured to include photodetectors (¶ 0025) and have respective light-receiving surfaces and respective sides (top of and side surfaces of nanowires 300);

wherein at least some of the pillars (300/200) comprise P-doped (222, shown to be p-type in Fig. 4) and N- doped (225, shown to be n-type in Fig. 4) regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers (§ 0005, “An APD is a highly sensitive semiconductor electronic device that exploits the photoelectric effect to convert light to electricity.”);

side-isolation (236, Fig. 4 cont’d) comprising solid material between at least portions of the sides of at least some of the pillars (“Space between the nanowires 200 is preferably filled with an oxide layer 236.”, § 0048);

a solid dielectric material (part of the base is made up of “SiO₂”) forming a base dielectric region for the array (array of 300/200 are formed on “SiO₂” layer);

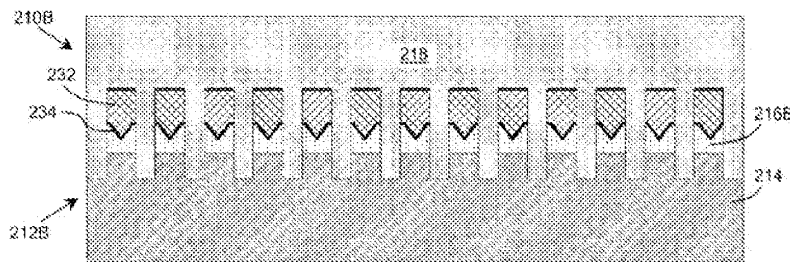
electrical contacts (top electrode is 340, § 0079, and bottom electrode is “The metal silicide layer 231 forms electrical contact to any electrical components of the substrate 230”, § 0048) configured to provide electrical pathways coupled electrically to at least some of the photodetectors (noted electrical contact provide electrical signals to pillars 200/300), including for selected reverse-biasing thereof (“By applying a high reverse bias voltage (typically 100-200 V in silicon), APDs show an internal current gain (around 100).”, § 0005).

First, Yu does not disclose, “one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other shapes

at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material”.

Lunev discloses in Fig. 4B (provided below), where pillars are formed with “recesses” in the top surfaces, as disclosed in ¶ 0051, “The conducting layer of the ohmic contact 218 is separated from the corresponding semiconductor contact structure 212A, 212B by a filler material 232 (e.g., silicon dioxide or the like). In FIG. 4B, **a top surface 234 of the top semiconductor layer 216B is roughened or patterned, e.g., by including pyramids, holes, etched roughness, or the like, which can be configured to scatter light, e.g., generated in the semiconductor contact structure 212B.**” From ¶ 0075, “As described herein, a device including an ohmic contact described herein can comprise a light emitting device, such as a light emitting diode (LED), a laser diode (LD), a **photodiode**, and/or the like.”

FIG. 4B



Counil discloses in ¶ 0016, where texture surface height ‘h’ can be formed in dimensions between 20nm to 1μm, 30nm to 500nm and 50 nm to 200nm.

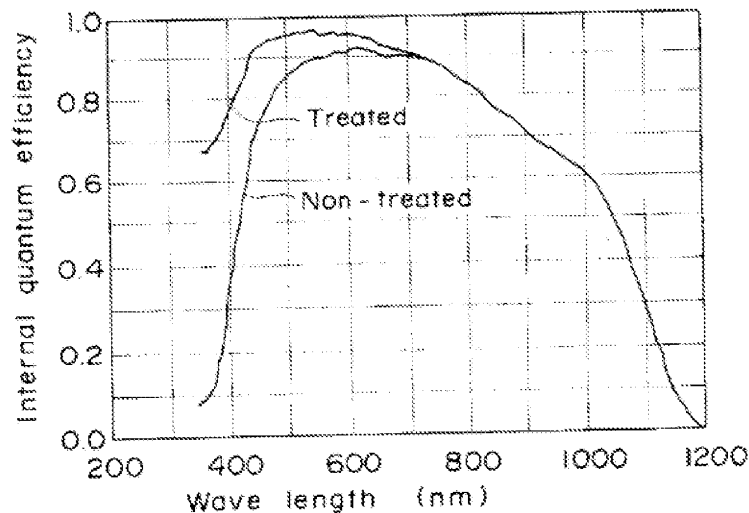
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to use the “one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other

shapes at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material”, as disclosed by Lunev and Counil in the system of Yu, for the purpose of improving the light extraction efficiency. *G. TSM: Teaching, Suggestion, Motivation Test.*

Second, Yu does not disclose, “wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes.”

Arimoto shows in Fig. 5 (provided below), where at least 10% efficiency is gained by texturizing the light incident surface.

Fig. 5



Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to use the “wherein the presence of said one or more holes

increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes”, as disclosed by Arimoto in the system of Yu, for the purpose of improving the internal quantum efficiency which is to say more light is converted with the textured surface. *G. TSM: Teaching, Suggestion, Motivation Test.*

Regarding claim 2, the prior art of Yu et al. disclose the integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices (Yu shows in Fig. 5, where the noted pillars 200/300 are formed in a system that includes devices in a silicon substrate).

Regarding claim 8, the prior art of Yu et al. disclose the integrated structure of claim 1, and Yu discloses, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors (top electrode is 340, ¶ 0079, and bottom electrode is “The metal silicide layer 231 forms electrical contact to any electrical components of the substrate 230”, ¶ 0048, and these noted electrodes provide access to electrical signal for all of the pillars 200/300).

Regarding claim 9, the prior art of Yu et al. disclose the integrated structure of claim 1, and Yu discloses, in which two or more of the photodetectors share one of the electrical contacts (see Fig. 5, where plural 200/300 share noted electrodes).

Regarding claim 12, the prior art of Yu et al. disclose the integrated structure of claim 1, in which each of at least some of the photodetectors is configured such that the light passes

through at least a part of the one of the P-doped region and N-doped region of the photodetector before reaching any part of the other doped region of the photodetector (the 200/300 above the circuitry below, and thus receive light first from external to the overall device system).

Claims 10 and 11 are rejected under 35 U.S.C. 103 as being unpatentable over Yu et al. (US 2011/0309331) in view of Lunev et al. (US 2014/0016660, used to represent the provisional application 61/670,808 whose effective date is July 12, 2012) in view of Counil et al. (US 2010/0116332) in view of Arimoto et al. (US 5,759,292) in view of Martin et al. (US 7,276,749).

Regarding claims 10 and 11, the prior art of Yu et al. disclose the integrated structure of claim 1, and Yu does not specify,

“wherein the array monolithically integrated with Si electronic devices for signal processing and transmission”,

“wherein the array is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors”.

Sensor Array Circuitry

400

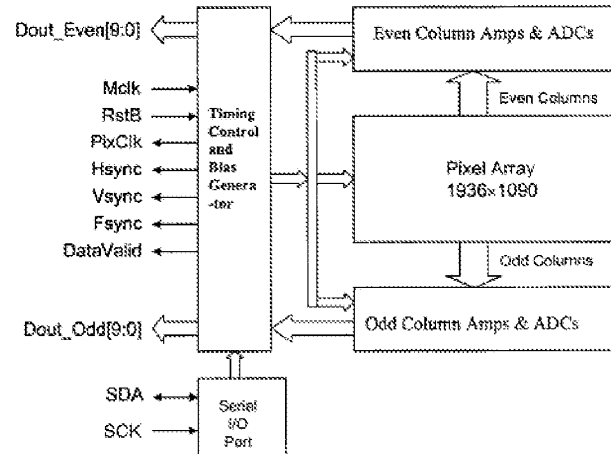


FIG. 1C

Martin discloses in Fig. 1C (provide above), wherein the array monolithically integrated with Si electronic devices for signal processing and transmission (the pixel array is supported by the signal processing elements “Even/Odd Column Amps & ADS’s” and “Timing Control and Bias Generator” and the transmission section “Serial I/O Port”),

wherein the array is monolithically integrated with Si electronic devices (Si devices already shown in ROIC of Yu) for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors (Martin discloses the pixel array is supported by the signal processing elements “Even/Odd Column Amps & ADS’s” and “Timing Control and Bias Generator” and the transmission section “Serial I/O Port”).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to use the,

“wherein the array monolithically integrated with Si electronic devices for signal processing and transmission”,

“wherein the array is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors”, as disclosed by Martin in the system of Yu, for the purpose of providing the necessary device components to make the light signals gathered into usable electrical data signals and for distributing the gathered electrical data. *G. TSM: Teaching, Suggestion, Motivation Test.*

Claim 13 is rejected under 35 U.S.C. 103 as being unpatentable over Yu et al. (US 2011/0309331) in view of Lunev et al. (US 2014/0016660, used to represent the provisional application 61/670,808 whose effective date is July 12, 2012) in view of Counil et al. (US 2010/0116332) in view of Arimoto et al. (US 5,759,292) in view of Kim et al. (US 2011/0297214).

Regarding claim 13, the prior art of Yu et al. disclose the integrated structure of claim 1, and Yu discloses the opposite orientation to, “in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the P-doped region before reaching any part of the N-doped region.”

Kim et al. (US 2011/0297214) Fig. 2A (shown below) discloses the limitation of, in which the doped regions of each of at least some of the photodetectors are configured such that

the light passes through at least a part of the P-doped region before reaching any part of the N-doped region (where p-type is above the n-type part of the pillars).

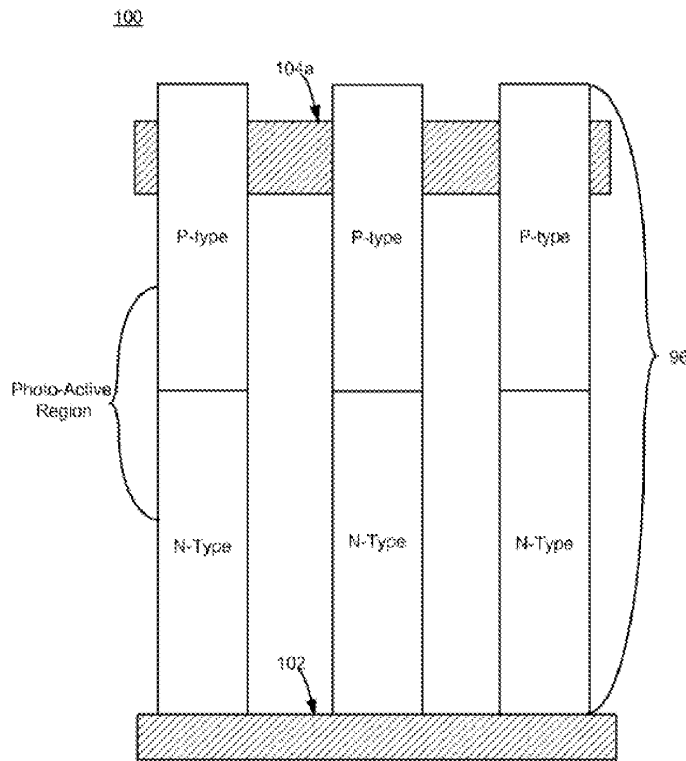


FIGURE 2A

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to use the,

“in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the P-doped region before reaching any part of the N-doped region”, as disclosed by Kim in the system of Yu, for the purpose of providing the practical construction of a light converting diode to create electrical signals from light signals. *G. TSM: Teaching, Suggestion, Motivation Test.*

Allowable Subject Matter

Claims 3-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 4-7 are objected to because of their dependency on claim 3.

Claims 14-17 are allowed.

The following is an Examiner's statement of reasons for allowance: The integrated structure as recited in the claims of the instant invention fail to be taught by the prior art cited of interest.

Regarding claim 14, the prior art of Yu et al. (US 2011/0309331) discloses in Figs. 4 and 5, a integrated photoconversion array, but fails to disclose the specific characteristic recited in the claims of the instant invention e.g. the combination of claimed features of an array of pillars comprising Si, Ge, and/or alloyed SiGe semiconductor material, the pillars comprise p-type and n-type doped regions for generating charge carriers, holes in the light receiving surface of at least some of the pillars, the holes are filled with solid dielectric material, side isolation, solid dielectric material forming a base dielectric region for the array, electrical contacts, the presence of holes increases absorption of light by factor of 1.1, and the array is monolithically integrated with electronic devices for signal processing and transmission, in conjunction with the feature of,

“each of the holes has an elongated shape extending in length over less than the width of the light receiving surface in which the hole is fabricated”.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A Rodela whose telephone number is (571)272-8797. The examiner can normally be reached M-F, 8:30-5:00pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yara B Green can be reached on (571) 270-3035. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/EDUARDO A RODELA/
Primary Examiner, Art Unit 2893

<i>Notice of References Cited</i>	Application/Control No. 18/822,880	Applicant(s)/Patent Under Reexamination WANG et al.	
	Examiner Eduardo A Rodela	Art Unit 2893	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Name	CPC Classification	US Classification
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*	B	US-20130125965-A1	2013-05-23	Hazeghi; Arash	H01L31/18	438/57
*	C	US-20120196401-A1	2012-08-02	Graham; William	H01L31/035227	977/840
*	D	US-9263519-B2	2016-02-16	Lal; Amit	B82Y10/00	1/1
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Search Notes 	Application/Control No. 18/822,880	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

CPC - Searched*		
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H01L31/02019; H01L31/022408; H01L31/02327; H01L31/02363; H01L31/028; H01L31/035281; H01L31/105; H01L31/107; H01L31/0236,02363,0352	11/14/2024	EAR

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Class	Subclass	Date	Examiner

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Search Notes	Date	Examiner
PE2E search - see history for complete details	11/14/2024	EAR
Applicant & Inventor search	11/14/2024	EAR

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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Receipt date: 09/03/2024

18/822,880 -- GAU: 2893

Doc code: IDS

PTO/SB/08a (02-18)

Doc description: Information Disclosure Statement (IDS) Filed

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1	11309444		2022-04-19	Wang et al.		
	2	8558336		2013-10-15	Su		
	3	10411053		2019-09-10	Yokogawa		
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

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	10	8357960		2013-01-22	Dutta	
	11	8946675		2015-02-03	Yu	
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	1	20100320444		2010-12-23	Dutta	
	2	20110309331		2011-12-22	Yu et al.	
	3	20180182806		2018-06-28	Jin et al.	

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	5	20120153127		2012-06-21	Hirigoyen et al.	
	6	20180012918		2018-01-11	Na et al.	
	7	20190166317		2019-05-30	Tanaka et al.	
	8	20120012741		2012-01-19	Vasylyev	
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	14	20200006416		2020-01-02	Baba et al.	

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	1	20080101301	KR		2008-11-21	Dongbu Hitek Co. Ltd.		☐
	2	2002314116	JP		2002-10-25	Seiko Epson Corp.		☐
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	4	2019018846	WO		2019-01-24	W&W Sens Devices Inc.		☐
	5	09040854	EP		1999-09-08	IBM United Kingdom Limited		☐
	6	2007013065	JP		2007-01-18	Matsushita Electric Works Ltd.		☐
	7	103956403	CN		2017-02-15	Suzhou Beipeng Photoelectric Technology Co. Ltd.		☐

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	1	Copy of International Search Report and Written Opinion for PCT/US2020/051733 mailed December 17, 2020.	☐
	2	Copy of Written Opinion of International Search Report for PCT/US2020/051733 dated December 17, 2020.	☐
	3	BEAUSOLEIL, Nanoelectronic and Nanophotonic Interconnect, The emerging integrated circuit interconnection bottleneck may be overcome if tiny, efficient photon-transport waveguides and small transceivers for photon-electron information exchange can be developed, 18 pages, January 29, 2007; revised September 25, 2007.	☐
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	6	GAO YANG et al., Photon-trapping Microstructures Enable High-speed High-efficiency Silicon Photodiodes, Nature Photonics, Vol. 11, No. 5, April 3, 2017, Pages 301-308.	☐
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-09-03
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L3	862	((("WANG") near3 ("Shih-Yuan")) OR ((("WANG") near3 ("Shih-Ping"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2024/11/08 02:39 PM
L5	83304	(H01L31/02019 OR H01L31/022408 OR H01L31/02327 OR H01L31/02363 OR H01L31/028 OR H01L31/035281 OR H01L31/105 OR H01L31/107).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/08 02:40 PM
L6	2267779	(light OR infrared OR "IR") WITH (pillar OR column\$2 OR cylinder)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/08 02:41 PM
L7	30593495	(aperture\$1 OR gaps OR void OR divot)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2024/11/08 02:59 PM

L9	191	("20050092925" "20050184354" "20070092192" "20070190434" "20080047604" "20080218740" "20080248608" "20080265449" "20081012582" "20090188557" "20090267049" "20100029067" "20100126548" "20100193768" "20100197068" "20100221866" "20100313941" "20120193676" "20120292676" "20130207222" "20140001528" "20150041965" "20160225631" "4571559" "4637129" "4716449" "5451767" "5457327A" "5625636" "5757057" "5886374" "6027956" "6177289" "6667528" "7115971" "7397101" "7495306" "7601597" "7674563" "7772615" "7795064" "7893348" "7898052" "7972934" "8114695" "8129710" "8436370" "8357960" "20050092925" "20050184354" "20060218740" "20070092192" "20080265449" "20090188557" "20100126548" "20100193766" "20100197068" "4637129" "5457327" "7115971" "7397101" "7501597" "7674563" "7795064" "7893346" "8129710"). PN.	RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/08 03:14 PM
L10	101	("20070190434" "20080047604" "20080248608" "20081012582" "20090267049" "20100029067" "20100221866" "20100313941" "20120193676" "20120292676" "20130207222" "20140001528" "20150041965" "20160225631" "4571559" "4716449" "5451767" "5625636" "5757057" "5886374" "6027956" "61	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA,	OR	ON	ON	2024/11/08 03:15 PM

L12	1	77289" "6667528" "7495306" "7772615" "7898052" "7972934" "8114695" "8357960" "8436370").PN. "20070007621"	VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB)	OR	ON	ON	2024/11/12 12:42 PM
L14	31331	H01L31/0236,02363,0352.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/12 04:50 PM
L15	94829	L5 OR L14	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/12 04:51 PM
L16	1103	(@rtpd<="20131115" OR @rtad<="20131115" OR @pd<="20131115" OR @ad<="20131115") AND L15 AND L7 AND L6	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/12 04:52 PM
L17	390	(@rtpd<="20131115"	(US-PGPUB; USPAT;	OR	ON	ON	2024/11/12

L18	508	OR @rlad<="20131115" OR @pd<="20131115" OR @ad<="20131115") AND L15 AND L7 AND L6 ("1918848" "3903427" "4017332" "4292512" "4316048" "4357415" "4387265" "4394571" "4400221" "4443890" "4513168" "4531055" "4620237" "4678772" "4827335" "4846556" "4857973" "4876586" "4880613" "4896941" "4950625" "4971928" "4972244" "4990988" "5071490" "5081049" "5096520" "5124543" "5217911" "5247349" "5272518" "5311047" "5347147" "5362972" "5374841" "5391896" "5401968" "5449626" "5468652" "5602661" "5612780" "5671914" "5696863" "5723945" "5747796" "5767507" "5798535" "5844290" "5853446" "5857053" "5877492" "5880495" "5885881" "5900623" "5943463" "5968528" "6013871" "6033582" "6037243" "6046466" "6074892" "6100551" "6270548" "6301420" "6326649" "6388243" "6388648" "6407439" "6459034" "6463204" "6542231" "6563995" "6566723" "6680216" "6709929" "6720594" "6771314" "6805139" "6812473" "6904187" "6927145" "6960526" "6967120" "6969899" "6987258" "6996147" "7052927" "7064372" "7105428" "7106938" "7109517" "7153720" "7163659" "7192533" "7208783" "7230286" "7235475" "7241434" "7253017" "7254151" "7262400" "7265328"	USOCR) (US-PGPUB; USPAT; USOCR)	OR	ON	ON	04:52 PM 2024/11/12 05:05 PM
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		"7272287" "7285812" "7306963" "7307327" "7311889" "7326915" "7330404" "7335962" "7336860" "7339110" "7358583" "7381966" "7388147" "7416911" "7446025" "7462774" "7471428" "7491269" "7507293" "7521322" "7524694" "7582587" "7582857" "7598482" "7622367" "7626685" "7646138" "7646943" "7647695" "7649665" "7655860" "7663202" "7692860" "7704806" "7713779" "7719678" "7719688" "7732769" "7732839" "7736954" "7740824" "7790495" "7872324" "7888155" "7902540" "7948555" "8030729" "8035184" "8049203" "8063450" "8067299" "8067736" "8084728" "8093675" "8118170" "8143658" "8154127" "8193524" "8208776" "8212136" "8212138" "8222705" "8242353" "8269985" "8274039" "8299472" "8330090" "8384007" "8455857" "8471190" "8514411" "8546742" "8748799" "8766272" "8791470" "8810808" "8835831" "8866065" "9000353" "20020003201" "20020020846" "20020021879" "20020071468" "20020104821" "20020109082" "20020117675" "20020130311" "20020172820" "20030003300" "20030006363" "20030077907" "20030089899" "20030103744" "20030132480" "20030160176" "20030189202" "20030227090"				
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		"20040011975"					
		"20040021062"					
		"20040026684"					
		"20040058058"					
		"20040065362"					
		"20040075464"					
		"20040095658"					
		"20040109666"					
		"20040114847"					
		"20040118337"					
		"20040118377"					
		"20040122328"					
		"20040124366"					
		"20040155247"					
		"20040156610"					
		"20040160522"					
		"20040180461"					
		"20040213307"					
		"20040217086"					
		"20040223681"					
		"20040241965"					
		"20040252957"					
		"20040261840"					
		"20050009224"					
		"20050035381"					
		"20050082676"					
		"20050087601"					
		"20050095699"					
		"20050109388"					
		"20050116271"					
		"20050133476"					
		"20050161662"					
		"20050164514"					
		"20050190453"					
		"20050201704"					
		"20050218468"					
		"20050224707"					
		"20050242409"					
		"20050284517"					
		"20060011362"					
		"20060027071"					
		"20060038990"					
		"20060113622"					
		"20060115230"					
		"20060121371"					
		"20060146323"					
		"20060162766"					
		"20060180197"					
		"20060208320"					
		"20060257071"					
		"20060260674"					
		"20060273262"					
		"20060273389"					
		"20060284118"					
		"20070012980"					
		"20070012985"					
		"20070023799"					
		"20070025504"					

		"20070029545"					
		"20070052050"					
		"20070076481"					
		"20070082255"					
		"20070099292"					
		"20070104441"					
		"20070107773"					
		"20070108371"					
		"20070114622"					
		"20070120254"					
		"20070126037"					
		"20070137697"					
		"20070138376"					
		"20070138380"					
		"20070138459"					
		"20070139740"					
		"20070140638"					
		"20070145512"					
		"20070148599"					
		"20070152248"					
		"20070155025"					
		"20070164270"					
		"20070170418"					
		"20070172623"					
		"20070172970"					
		"20070187787"					
		"20070196239"					
		"20070200054"					
		"20070205483"					
		"20070217754"					
		"20070228421"					
		"20070238265"					
		"20070238285"					
		"20070241260"					
		"20070246689"					
		"20070248958"					
		"20070272828"					
		"20070278500"					
		"20070285378"					
		"20070290193"					
		"20070290265"					
		"20080001498"					
		"20080006319"					
		"20080006891"					
		"20080029701"					
		"20080036038"					
		"20080044984"					
		"20080047601"					
		"20080047604"					
		"20080055451"					
		"20080065451"					
		"20080073742"					
		"20080079022"					
		"20080079076"					
		"20080083963"					
		"20080088014"					
		"20080090401"					
		"20080092938"					

		"20080096308"					
		"20080108170"					
		"20080116537"					
		"20080128760"					
		"20080137188"					
		"20080143906"					
		"20080145965"					
		"20080149914"					
		"20080149944"					
		"20080157253"					
		"20080166883"					
		"20080169017"					
		"20080169019"					
		"20080173615"					
		"20080178924"					
		"20080188029"					
		"20080191278"					
		"20080191298"					
		"20080211945"					
		"20080218740"					
		"20080224115"					
		"20080225140"					
		"20080233280"					
		"20080237568"					
		"20080246020"					
		"20080246123"					
		"20080248304"					
		"20080251780"					
		"20080258747"					
		"20080260225"					
		"20080264478"					
		"20080266556"					
		"20080266572"					
		"20080271783"					
		"20080277646"					
		"20080283728"					
		"20080283883"					
		"20080297281"					
		"20080311693"					
		"20080311712"					
		"20090001498"					
		"20090020150"					
		"20090020687"					
		"20090032687"					
		"20090046362"					
		"20090046749"					
		"20090050204"					
		"20090052029"					
		"20090057650"					
		"20090072145"					
		"20090104160"					
		"20090120498"					
		"20090121136"					
		"20090127442"					
		"20090146198"					
		"20090151782"					
		"20090152664"					
		"20090153961"					

		"20090165844"					
		"20090173976"					
		"20090179225"					
		"20090179289"					
		"20090188552"					
		"20090189144"					
		"20090189145"					
		"20090194160"					
		"20090199597"					
		"20090201400"					
		"20090206405"					
		"20090211622"					
		"20090223558"					
		"20090224245"					
		"20090224349"					
		"20090230039"					
		"20090233445"					
		"20090242018"					
		"20090243016"					
		"20090244514"					
		"20090260687"					
		"20090261438"					
		"20090266418"					
		"20090266974"					
		"20090272423"					
		"20090278998"					
		"20090289320"					
		"20090305454"					
		"20100006817"					
		"20100019252"					
		"20100019296"					
		"20100019355"					
		"20100025710"					
		"20100078055"					
		"20100078056"					
		"20100090341"					
		"20100101633"					
		"20100104494"					
		"20100110433"					
		"20100116976"					
		"20100126573"					
		"20100127153"					
		"20100132779"					
		"20100133986"					
		"20100136721"					
		"20100148221"					
		"20100163714"					
		"20100163941"					
		"20100178018"					
		"20100186809"					
		"20100187404"					
		"20100200065"					
		"20100207103"					
		"20100218816"					
		"20100229939"					
		"20100230653"					
		"20100237454"					
		"20100240104"					

		"20100244108"					
		"20100244169"					
		"20100249877"					
		"20100258184"					
		"20100276572"					
		"20100277607"					
		"20100282314"					
		"20100295019"					
		"20100302440"					
		"20100304061"					
		"20100308214"					
		"20100313952"					
		"20100319763"					
		"20100320444"					
		"20110018424"					
		"20110036396"					
		"20110037133"					
		"20110049572"					
		"20110050042"					
		"20110057231"					
		"20110057234"					
		"20110057286"					
		"20110080508"					
		"20110084212"					
		"20110127490"					
		"20110133060"					
		"20110133160"					
		"20110135814"					
		"20110139176"					
		"20110146771"					
		"20110147870"					
		"20110180894"					
		"20110195577"					
		"20110220191"					
		"20110226937"					
		"20110248315"					
		"20110249219"					
		"20110249322"					
		"20110253982"					
		"20110272014"					
		"20110297214"					
		"20110309237"					
		"20110309240"					
		"20110309331"					
		"20110315988"					
		"20110316106"					
		"20120006390"					
		"20120009714"					
		"20120014837"					
		"20120029328"					
		"20120031454"					
		"20120060905"					
		"20120075513"					
		"20120153124"					
		"20120192939"					
		"20120196383"					
		"20120196401"					
		"20120240999"					

		"20120258563" "20120280345" "20120298843" "20120313078" "20120318336" "20120322164" "20130000704" "20130020620" "20130037100" "20130112256" "20130125965" "20130174904" "20130220406" "20130341749" "20140045209" "20140096816" "20140117401" "20150171272").pn. AND (PGPB USPT USOC).dbnm.					
L19	1	"9312448".pn.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/13 09:38 AM
L20	385	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L15 AND L7 AND L6	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/13 10:43 AM
L21	38	("6946682" "7601993" "7923753" "8525227" "8604511" "8735941" "8941146" "8969198" "9660043" "20020142548" "20070187677" "20080173898" "20080217625" "20080258150" "20090035884" "20090127575" "20090212276" "20100059781" "20110018024" "20110143507" "20110198641" "20110233520" "20110233596" "20120049152" "20120119189" "20120235204" "20120248500" "20130026519" "20130320352" "20140016660" "20140264454").pn. OR ("9793439").urpn. AND	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/13 10:51 AM

L22	36	(PGPB USPT USOC).dbnm. (@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L21	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/13 10:52 AM
L23	1	"20110309331"	(US-PGPUB)	OR	ON	ON	2024/11/14 09:38 AM
L24	1	"20140016660"	(US-PGPUB)	OR	ON	ON	2024/11/14 02:11 PM
L25	212	(texture OR recesses OR divots OR holes) WITH surface WITH (diode) WITH (absorb\$3 OR absorption OR efficiency) WITH light	(US-PGPUB)	OR	ON	ON	2024/11/14 02:34 PM
L26	277	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L25	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 02:34 PM
L27	1974	(textur\$3 OR texturized) WITH ("1" OR "10" OR "20" OR "30 OR "40 OR "50") NEAR (nanometer\$1 OR "nm"))	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 03:29 PM
L28	245	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L27 AND L14	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/14 03:30 PM
L29	76	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L27 AND L14	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 03:30 PM
L30	590	(textur\$3 OR texturized) WITH surface WITH (increas\$3 NEAR	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:11 PM

L31	78	(efficiency OR absorb\$3 OR absorption)) (@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND L14	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:11 PM
L32	36	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND L14 AND (percent\$3 OR "%")	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:13 PM
L33	0	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND (L14 SAME (percent\$3 OR "%"))	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:13 PM
L34	0	(@rtpd<="20130613" OR @rtad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND (L14 SAME (percent\$3 OR "%"))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/14 04:14 PM
L35	7573011	(signal NEAR process\$3) AND (output OR transmission)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/14 04:36 PM

L36	244	(@rldp<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L14 AND L35	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:37 PM
L37	4526	(@rldp<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND (cmos NEAR imager) AND L35	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:44 PM
L38	747	(@rldp<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND (cmos NEAR imager) AND ((signal NEAR process\$3) AND (output OR transmission)) AND monolithic\$4	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:44 PM
L39	0	(L2 OR L3 OR L15) AND ((integrated NEAR structure)(array)(pillars) (holes)(p-doped)(n- doped)(light NEAR receiving NEAR surfaces)(visible)(infrare d)(wavelengths)(photos ensitive NEAR area)(charge NEAR carriers)(holes)(recesse s)(side NEAR isolation)(base NEAR dielectric)(electrical NEAR contacts)(factor)(increa se)(abosorption)("1.1"). clm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2024/11/14 05:22 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

Attorney Docket No.: 309-0015USCIPDIV
Confirmation No.: 5818

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shih-Yuan WANG	Examiner: EDUARDO A RODELA
Application No.: 18/822,880	Art Unit: 2893
Filed: September 3, 2024	CERTIFICATE OF TRANSMISSION
Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
	/Mary Ellen Finnegan/ Date: November 18, 2024 Name: Mary Ellen Finnegan

VIA EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov
Registration No. 25,161
Attorney for Applicant

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Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001
Attorney's Telephone No.: 917-945-0121
Attorney's E-mail: ikavrukov@wissingmiller.com

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		18822880
	Filing Date		2024-09-03
	First Named Inventor	Shih-Yuan WANG	
	Art Unit	2893	
	Examiner Name	EDUARDO A RODELA	
	Attorney Docket Number	309-0015USCIPDIV	

	1		☐
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Examiner Signature		Date Considered	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			
<small> ¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached. </small>			

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		18822880
	Filing Date		2024-09-03
	First Named Inventor	Shih-Yuan WANG	
	Art Unit	2893	
	Examiner Name	EDUARDO A RODELA	
	Attorney Docket Number	309-0015USCIPDIV	

CERTIFICATION STATEMENT			
Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):			
☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).			
OR			
☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).			
☐ See attached certification statement.			
☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.			
☒ A certification statement is not submitted herewith.			
SIGNATURE			
A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.			
Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-11-18
Name/Print	Ivan S. Kavrukov	Registration Number	25,161
<p>This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</p>			

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
18/822,880

RECEIPT DATE / TIME
11/18/2024 01:48:39 PM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68003337	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_IDSTransmittal-Final.pdf	1	Transmittal Letter	446 KB
309-0015USCIPDIV_1449-Final.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	1010 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV_IDSTransmittal-Final.pdf	BBBC9ADD8C833A72A2D351F384B1286893606CC11F4FEED79FA801DD068A7381310DF936C33CE4C327CDFA69984DC04D600646B4107A66985EF7FA5DA27DFC39

309-0015USCIPDIV_1449-
Final.pdf

BBAB28011A89FD0AE2EC6E41C6EDE85C82FBAB494A37EAD
386F1DB469484D4148247AC44C214C24498A14EE398452985E
A5068B3F124F216D6F8ED4C1B3E3334

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If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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APPLICATION #
18/822,880

RECEIPT DATE / TIME
10/31/2024 04:04:48 PM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	67799981	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309- 0015USCIPDIV_SecondPreliminary Amendment-Final.pdf	6	Preliminary Amendment	496 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309- 0015USCIPDIV_SecondPreliminary Amendment-Final.pdf	7066265F1E919EC95FE66C4CA20E8B613EE267CF34BB44794 1B3387A71C6BC77970325D8EA990F3EE087557AEFEC13E6C D085B7B13821A7DF60125EB4A483A2F

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Shih-Yuan WANG et al.
Serial No.: 18/822,880
Examiner: EDUARDO A RODELA
Group Art Unit 2893
Filing Date: 09/03/2024
For: MICROSTRUCTURE ENHANCED ABSORPTION
PHOTOSENSITIVE DEVICES
Conf. No. 5818

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

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I hereby certify that this correspondence is being transmitted via
Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

SECOND PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Prior to examination and the issuance of the first Office Action, please amend the above-
identified application as follows:

Amendments to the Claims:

Please rewrite the claims as follows. These amended claims replace all previously filed claims:

1. (currently amended) An integrated structure comprising:
 - an array of pillars comprising ~~SiSi~~, Ge, and/or SiGe alloy semiconductor material, wherein at least some of the pillars are configured ~~as to include~~ photodetectors ~~that and~~ have respective light-receiving surfaces and respective sides;
 - wherein at least some of the ~~photodetectors-pillars~~ comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;
 - one or more holes that are ~~deliberately formed~~~~fabricated as recesses at or under~~ the light-receiving surface of each of at least some of the ~~photodetectors-pillars~~, have elongated or other shapes ~~at or parallel to the~~ light-receiving surfaces, extend into the ~~photodetectors-pillars~~ to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;
 - side-isolation comprising solid material between at least portions of the sides of at least some of the ~~photodetectors-pillars~~;
 - a solid dielectric material forming a base dielectric region for the array;
 - electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;
 - wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes.
2. (currently amended) The integrated structure of claim 1, wherein the array ~~of~~ ~~photodetectors~~ is monolithically integrated with ~~Si-Si~~ electronic devices.

3. (currently amended) The integrated circuit of claim 1, in which at least some of ~~the~~ holes are elongated along the respective light-receiving surfaces.
4. (currently amended) The integrated structure of claim 3, wherein each of at least some of the ~~photodetectors-pillars~~ has a plurality of the elongated holes.
5. (currently amended) The integrated structure of claim 3, wherein each of at least some of the ~~photodetectors-pillars~~ has only one of the elongated holes.
6. (currently amended) The integrated structure of claim 3, in which the light-receiving surfaces have respective widths, and the elongated holes extend along less than the widths of the light-receiving surfaces of at least some of the ~~photodetectors-pillars in which the holes are fabricated.~~
7. (currently amended) The integrated structure of claim 6 in which each of ~~at least some of~~ the elongated holes has at least one closed contour remote from respective side edges of the light-receiving ~~surface in which the hole is fabricated-surfaces of at least some of the photodetectors.~~
8. (previously presented) The integrated structure of claim 1, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors.
9. (previously presented) The integrated structure of claim 1, in which two or more of the photodetectors share one of the electrical contacts.
10. (currently amended) The integrated structure of claim 1, wherein the array of ~~photodetectors~~ is monolithically integrated with ~~Si-Si~~ electronic devices for signal processing and transmission.

11. (currently amended) The integrated structure of claim 1, wherein the array of ~~photodetectors~~ is monolithically integrated with ~~Si-Si~~ electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors.
12. (currently amended) The integrated structure of claim 1, in which ~~each of at least some of the photodetectors is configured~~ ~~the doped regions of each of at least some of the photodetectors are configured~~ such that the light passes through at least a part of the ~~one of the P-doped region and N-doped region of the photodetector~~ before reaching any part of the ~~N- other doped region of the photodetector~~.
13. (currently amended) The integrated structure of claim 1, in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the ~~NP~~-doped region before reaching any part of the ~~NP~~-doped region.
14. (currently amended) An integrated structure comprising:
an array of pillars comprising ~~SiSi~~, Ge, and/or alloyed SiGe semiconductor material, wherein at least some of the pillars ~~are configured as photodetectors that have~~ respective sides and ~~respective~~ light-receiving surfaces with selected widths ~~and comprise at least one photodetector~~;
wherein at least some of the ~~photodetectors pillars~~ comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;
one or more holes that are ~~deliberately formed~~ ~~fabricated as recesses~~ at or under the light-receiving surface of each of at least some of the ~~photodetectors pillars~~,
wherein each of the holes (i) has an elongated shape extending in length over less than the width of the light-receiving surface in which the hole is

~~formed/fabricated~~, (ii) has at least one closed contour at the light-receiving surface in which the hole is ~~formed/fabricated~~, (ii) extends into the ~~photodetector-pillar~~ in which the hole is ~~formed-fabricated~~ to a depth of 100 to 10000 nm, and (iv) is filled at least partly with solid dielectric material;

side-isolation comprising solid material between at least portions of the sides of at least some of the ~~photodetectors/pillars~~;

a solid dielectric material forming a base dielectric region for the array;

electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;

wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the holes; and

wherein the array ~~of photodetectors~~ is monolithically integrated with ~~Si-Si~~ electronic devices for signal processing and transmission.

~~15.~~ (currently amended) The integrated structure of claim 14, in which each of at least some of the ~~photodetectors/pillars~~ has only one of the elongated holes ~~fabricated therein~~.

~~15-16.~~ (new) The integrated structure of claim 14, in which each of at least some of the pillars has at least two of the elongated holes.

~~16-17.~~ (new) The integrated structure of claim 14, in which each of at least some of the photodetectors includes at least one of the holes.

REMARKS

This patent application is a divisional of and incorporates by reference parent application Ser. Nos. 18/385,213 filed October 30, 2023, which is expected to issue as U.S. Patent No. 12,087,871 on September 10, 2024, according to Issue Notification dated 08/21/2024.

Applicant submits that the same examples of support discussed in the immediate parent application apply to the claims above, which are entitled to the same 2014 and 2013 filing dates through the same chain of continuing applications as the immediate parent of which the subject application is a division.

Applicant invites the Examiner to telephone the undersigned if it appears that a call may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

WISSING MILLER LLP

Attorney for Applicants

By: /Ivan S. Kavrukov/

Ivan S. Kavrukov

Reg. No. 25,161

Tel.: (917) 945-0121

REMARKS

This patent application is a divisional of and incorporates by reference parent application Ser. Nos. 18/385,213 filed October 30, 2023, which is expected to issue as U.S. Patent No. 12,087,871 on September 10, 2024, according to Issue Notification dated 08/21/2024.

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Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

WISSING MILLER LLP

Attorney for Applicants

By: /Ivan S. Kavrukov/

Ivan S. Kavrukov

Reg. No. 25,161

Tel.: (917) 945-0121

PATENT APPLICATION FEE DETERMINATION RECORD				Application or Docket Number 18/822,880		Filing Date 09/03/2024		☐ To be Mailed	
Substitute for Form PTO-875									
ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO									
APPLICATION AS FILED - PART I									
FOR		(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A	N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A	N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A	N/A					
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*	x \$40 =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*	x \$ 192 =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL					
APPLICATION AS AMENDED - PART II									
		(Column 1)		(Column 2)	(Column 3)				
AMENDMENT	10/31/2024	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 17	Minus	** 20	= 0	x \$40 =		0	
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0	x \$ 192 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/CAROLYN E THOMAS/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".									
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818
139982	7590	10/28/2024	EXAMINER	
Wissing Miller LLP			CENTRAL, DOCKET	
Industrious at Hudson Yards			ART UNIT	
31 Hudson Yards, 11th Floor			PAPER NUMBER	
New York, NY 10001			OPAP	
			NOTIFICATION DATE	
			DELIVERY MODE	
			10/28/2024	
			ELECTRONIC	

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The time period for reply, if any, is set in the attached communication.

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WMDocket@wissingmiller.com



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Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Application of :
WANG et al. :
Application No. 18/822,880 :
Filed: September 3, 2024 : **DECISION ON PETITION**
For: MICROSTRUCTURE ENHANCED :
ABSORPTION PHOTOSENSITIVE :
DEVICES :

This is a decision on the petition under 37 CFR 1.102(c)(1), filed September 3, 2024, to make the above-identified application special based on applicant's age as set forth in MPEP § 708.02, Section II.

The petition is **GRANTED**.

A grantable petition to make an application special under 37 CFR 1.102(c)(1) and MPEP § 708.02, Section II: Applicant's Age, must be accompanied by evidence showing that the applicant is 65 years of age, or more, such as applicant's statement or a statement from a registered practitioner that he or she has evidence that the applicant is 65 years of age or older. No fee is required.

The instant petition includes a statement from the registered attorney or agent attesting to having evidence of the joint inventor's age being 65 years of age or more. Accordingly, the above-identified application has been accorded "special" status.

Telephone inquiries concerning this decision should be directed to Paralegal Specialist Lara Willsey at 571-270-1501. All other inquiries concerning the examination or status of the application are accessible in the Patent Center at <https://patentcenter.uspto.gov>.

/Lara C. Willsey/
Lara C. Willsey
Paralegal Specialist
Office of Petitions



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
18/822,880	09/03/2024	OPAP	992	309-0015USCIPDIV	15	2

139982

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Industrious at Hudson Yards

31 Hudson Yards, 11th Floor

New York, NY 10001

CONFIRMATION NO. 5818

REPLACEMENT FILING RECEIPT



00000000/8142610

Date Mailed: 09/20/2024

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

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Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;

Shih-Ping WANG, Los Altos, CA;

Applicant(s)

W&W Sens Devices, Inc., Los Altos, CA;

Power of Attorney: The patent practitioners associated with Customer Number 139982

Domestic Priority data as claimed by applicant

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 and claims benefit of 62/175,855 06/15/2015
 and claims benefit of 62/174,498 06/11/2015
 and claims benefit of 62/171,915 06/05/2015
 and claims benefit of 62/157,876 05/06/2015
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 and claims benefit of 61/905,109 11/15/2013
 and claims benefit of 61/834,873 06/13/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.
 Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/12/2024

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 18/822,880**

Projected Publication Date: 12/26/2024

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

136

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184
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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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 and claims benefit of 62/197,120 07/27/2015
 and claims benefit of 62/188,876 07/06/2015
 and claims benefit of 62/182,602 06/21/2015
 and claims benefit of 62/175,855 06/15/2015
 and claims benefit of 62/174,498 06/11/2015
 and claims benefit of 62/171,915 06/05/2015
 and claims benefit of 62/157,876 05/06/2015
 and claims benefit of 62/154,675 04/29/2015
 and claims benefit of 62/153,443 04/27/2015
 and claims benefit of 62/139,511 03/27/2015
 and claims benefit of 62/111,582 02/03/2015
 and claims benefit of 62/100,025 01/05/2015
 and claims benefit of 62/090,879 12/11/2014
 and claims benefit of 62/081,538 11/18/2014
 and said 14/943,898 11/17/2015 claims benefit of 62/232,716 09/25/2015
 and claims benefit of 62/213,556 09/02/2015
 and claims benefit of 62/209,311 08/24/2015
 and claims benefit of 62/205,717 08/15/2015
 and claims benefit of 62/199,607 07/31/2015
 and claims benefit of 62/197,120 07/27/2015
 and claims benefit of 62/188,876 07/06/2015
 and claims benefit of 62/182,602 06/21/2015
 and claims benefit of 62/175,855 06/15/2015
 and claims benefit of 62/174,498 06/11/2015
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 and claims benefit of 62/153,443 04/27/2015
 and claims benefit of 62/139,511 03/27/2015
 and claims benefit of 62/111,582 02/03/2015
 and claims benefit of 62/100,025 01/05/2015
 and claims benefit of 62/090,879 12/11/2014
 and claims benefit of 62/081,583 11/19/2014 ABN
 and said 14/947,718 11/20/2015 is a CON of PCT/US2014/039208 05/22/2014
 which claims benefit of 61/826,446 05/22/2013
 and claims benefit of 61/843,021 07/04/2013
 and claims benefit of 61/905,109 11/15/2013
 and claims benefit of 61/834,873 06/13/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.
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If Required, Foreign Filing License Granted: 09/12/2024

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 18/822,880**

Projected Publication Date: 12/26/2024

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 18/822,880				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA		RATE(\$)	FEE(\$)	RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	64	N/A				
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A		N/A	280	N/A				
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	320	N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	15	minus 20 =	*	x	=	0	OR			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 =	*	x	=	0				
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				168					
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					0					
				TOTAL	832	TOTAL				
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED - PART II										
AMENDMENT A	(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
AMENDMENT B	(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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Derrick Brent

Deputy Under Secretary of Commerce for Intellectual Property and
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Sale Accounting Date:09/18/2024

Sale Item Reference Number	Effective Date
18822880	09/03/2024

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I20249HL14266827	2054	Non-DOCX Filing Surcharge	\$160.00	Deposit Account



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Sale Item Reference Number	Effective Date
18822880	09/03/2024

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I20249CG28029412	2081	UTILITY APPL SIZE FEE PER 50 SHEETS >100	\$168.00	Deposit Account



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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
18/822,880

RECEIPT DATE / TIME
09/03/2024 03:22:37 PM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	67024254	FILING DATE	-
CUSTOMER #	139982	FIRST NAMED INVENTOR	SHIH-PING Wang
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309- 0015USCIPDIV_PetitionToM akeSpecialBasedOnAge- Final.pdf	2	Petition to make special based on Age/Health	188 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309- 0015USCIPDIV_PetitionToMak eSpecialBasedOnAge-Final.pdf	0076F8C2BE0DC6DFD62872CF3C23801956A97A6EA976B90FF 7568BD68A8FD641ECFCD7EF8B96F3B215DAAC3ED09E2E752 C920A63AF82A816BE4A90FD76D1C564

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described in MPEP 503.

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