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PETITION TO MAKE SPECIAL BASED ON AGE FOR ADVANCEMENT OF EXAMINATION UNDER 37 CFR 1.102(c)(1)					
Application Information					
Application Number	TBD	Confirmation Number	n/a	Filing Date	TBD
Attorney Docket Number (optional)	309-0015USCIPDIV	Art Unit	n/a	Examiner	n/a
First Named Inventor	Shih-Yuan WANG				
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES				
Attention: Office of Petitions An application may be made special for advancement of examination upon filing of a petition showing that the applicant is 65 years of age, or more. No fee is required with such a petition. See 37 CFR 1.102(c)(1) and MPEP 708.02 (II). APPLICANT HEREBY PETITIONS TO MAKE SPECIAL FOR ADVANCEMENT OF EXAMINATION IN THIS APPLICATION UNDER 37 CFR 1.102(c)(1) and MPEP 708.02 (II) ON THE BASIS OF THE APPLICANT'S AGE. A grantable petition requires one of the following items: (1) Statement by one named inventor in the application that he/she is 65 years of age, or more; or (2) Certification by a registered attorney/agent having evidence such as a birth certificate, passport, driver's license, etc. showing one named inventor in the application is 65 years of age, or more.					
Name of inventor who is 65 years of age, or older					
Given Name	Middle Name	Family Name	Suffix		
Shih-Ping		WANG			
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Signature	/Ivan S. Kavrukov/		Date (YYYY-MM-DD)	2024-09-03	
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SUBJECT OF THE INVENTION

SUBJECT OF THE INVENTION

Improvement in the speed of a response speed can be achieved, and manufacture provides an easy near-infrared-light sensing element.

PROBLEM to be solved

The photoelectric-conversion part 6 which has a photodiode structure of a pin photodiode which forms in 1 surface side of the semiconductor substrate 1, and the i layer 62 which is a drift area|region interposes between the p form area|region 61 and the n form area|region 63, absorbs near infrared light, and an electronic * hole pair generate|occur|produces,

With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked on the light-receiving surface of the photoelectric-conversion part 6, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface

The slab type|mold photonic crystal 7 by which the refractive-index period structure was designed have a resonance peak is provided.

DETAILED DESCRIPTION of the INVENTION

[0001] TECHNICAL FIELD

This invention relates to the near-infrared-light sensing element which detects near infrared light.

DESCRIPTION OF RELATED ART

[0002] Conventionally, in the optical communication, the near-infrared-light sensing element is used as a light receiving element for receiving a light signal.

As this kind of a near-infrared-light sensing element, the photodiode (pn photodiode, a pin photodiode, an avalanche photo-diode, the Schottky photodiode, etc.) in which the pn junction and the schottky junction were formed is widely used for a semiconductor crystal.

It utilizes that the electric current which the electronic-hole pair generate|occur|produced when the light which has the photon energy more than a band gap injects is isolate|separated, travel|drive| works in a depletion layer (drift), and flows into an external circuit changes,

A light signal is detected as electric current change or voltage change.

As a semiconductor crystal material used for a near-infrared-light sensing element in here, there exists compound-semiconductor crystal|crystallization material (InGaAs, InGaAsP, etc.) other than Si or Ge,

However,

It is properly used by the wavelength range of the light used by an optical communication, the transmission speed request|required, the price, etc.

[0003] By the way, the optical communication is already widely used as a communication network between cities and in a city,

However,

In recent years, the motion which employ|adopts an optical communication also, for example in field|areas, such as SAN(Storage Area Network) which connects a highly efficient server and a router, DVI(Digital Visual Interface) which connects what is called an information appliance and a peripheral device, in-vehicle LAN(Local Area Network), a mobile phone, is activating.

The high-speed optical communication is required also in such a field|area,

Progress of improvement in the speed of transmission speed changes with applicable fields,

It is estimated that the transmission speed of 1Gbps or more is request|required also in either field| area.

- [0004] Improvement in the speed and a lowering of cost of a response speed will be request|required of the photodiode for optical communications used in the above various field|areas from now on. In here, it is known that the response speed of a photodiode will be fundamentally limited with two elements with the transit time t of the career|carrier (an electron, a hole) which carries out the drift of the inside of a depletion layer to CR time constant of a photodiode. In order to raise quantum efficiency (light-reception sensitivity) while making CR time constant small when the pin photodiode using Si as a semiconductor crystal material is considered for an example, the wide depletion layer is formed, Therefore It becomes impossible for the transit time t of the electron which carries out the drift of the inside of a depletion layer to ignore at the time of a high-speed response.
- [0005] For example, in order for quantum efficiency to be 80 % or more by the pin photodiode of Si, a depletion-layer width W of about 30 micrometer is needed, However, When cut-off-frequency f_c (CR) decided by CR time constant sets the diameter of a light reception to 250 micrometer, the pn-junction area A will become $A=4.9 \times 10^{-4} \text{ cm}^2$, 30 micrometer, then junction-capacitance C_j of a pn junction are set to $C_j=0.17 \text{ pF}$ by the depletion-layer width W , Therefore It will become $f_c(\text{CR})=1/(2(\pi)C_jR)=18 \text{ GHz}$ when the external resistance R shall be $50 \text{ } \Omega$.
- [0006] On the other hand, it will become $f_c(t_{tr})=0.44/t_{tr}$ when the frequency from which the amplitude of a photoelectric current becomes $1/2$ of the amplitude of a low-frequency area|region, and electric power becomes $1/2$ (-3 dB) is defined as cut-off-frequency $f(t_{tr})$, However, Since saturated-drift-velocity $(\nu)_{ds}$ of the electron which carries out the drift of during Si crystal|crystallization is $(\nu)_{ds}=1 \times 10^7 \text{ cm/sec}$, transit-time t_{tr} of the electron which carries out the drift of the inside of a depletion layer becomes $t_{tr}=W/(\nu)_{ds}=0.3 \text{ nsec}$, Cut-off-frequency $f_c(t_{tr})$ becomes $f_c(t_{tr})=1.5 \text{ GHz}$. As mentioned above, the diameter of a light reception about 250 micrometer and the pin photodiode of Si whose depletion-layer width W is 30 micrometer Since cut-off-frequency f_c (CR) decided from CR time constant was 18GHz, in this pin photodiode, above-mentioned transit-time t_{tr} will limit a cut off frequency, It understand|indicate|reveals that the 1.5GHz vicinity is a limit of an operating frequency.

- [0007] Here, in order to achieve improvement in the speed of the response speed of a pin photodiode, it is necessary to enlarge a cut off frequency,
Therefore
The drift velocity in a semiconductor crystal should just use compound-semiconductor material, Ge, etc. which are a quick semiconductor crystal material compared with Si,
However,
Like a silicon-semiconductor process, it is not excellent in mass-production property, and since the diameter of a wafer is also small, a lowering of cost is difficult.
- [0008] On the other hand, let the photoelectric-conversion part which has a pin photodiode structure of Si be a basic composition in recent years,
Quantum efficiency can be improved though thickness reduction of i layer which is a drift area| region in which a career|carrier carries out a drift in a photoelectric-conversion part is achieved,
The near-infrared-light sensing element which can achieve improvement in the speed by shortening of transit-time t_{tr} of the career|carrier which furthermore carries out the drift of the inside of i layer is proposed (a nonpatent literature 1, 2).
- [0009] This kind of near-infrared-light sensing element as shown in FIG. 4
DBR(Distributed Bragg Reflector)152 which consists of laminated film of the 1st SiO₂ layer 152a, the Si layer 152b, and the 2nd SiO₂ layer 152c, and reflects near infrared light on the 1 surface of the Si board|substrate 151 is provided.
The photoelectric-conversion part 160 which consists of a pin photodiode structure of Si which the i layer 162 interposes between the n<+> area|region 163 and the p<+> area|region 161 is provided on DBR152,
A surface with the light-receiving surface which consists of a surface of air and the p<+> area| region 161 forms the reflective surface which faces DBR152 (each other) on both sides of the photoelectric-conversion part 160 in the thickness direction (vertical direction) of the Si board| substrate 151,
The vertical resonator which consists of Fabry Perot type resonator (Fabry-Perot Resonator) by said reflective surface and DBR152 is formed.
Therefore, even if it makes thickness of the i layer 162 in the photoelectric-conversion part 160 small (it is small about the width of the i layer 162 in other words), a light-reception sensitivity can

be improved, and the distance of a carrier can also be shortened by making thickness of the i layer 162 thin,

Therefore

Improvement in the speed of a response speed can be achieved.

In addition, the p<+> area/region 161 is electrically connected with the p electrode 165 by 1 said surface side of the Si board/substrate 151, and the n<+> area/region 163 is electrically connected with the n electrode 163 by 1 said surface side of the Si board/substrate 151.

M.K. Emsley, et al, Silicon Resonant Cavity Enhanced Photodetector Arrays for Optical Interconnects, Proc. of SPIE Vol.5246,p409-421,2003

M.K. Emsley, et al, Silicon Substrates With Buried Distributed Bragg Reflectors for Resonant Cavity-Enhanced Optoelectronics, IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS,VOL.8,NO.4,p948-955,JULY/AUGUST 2002

DISCLOSURE OF THE INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0010] However,

In order to manufacture the near-infrared-light sensing element of the structure shown in FIG. 4, it is necessary to repeat twice basic process (Hydrogen-ion injection|grouting work is a bonding process, a peeling|exfoliation process, and a surface grinding|polishing process.) required of the hydrogen injection|pouring peel|exfoliating method known as one of the formation methods of an SOI wafer before formation of the photoelectric-conversion part 160,

The manufacture process was complicated and cost reduction was difficult.

Moreover, the manufacturing method of the above-mentioned infrared-light sensing element cannot be applied when employ|adopting semiconductor crystal materials other than Si as a material of the photoelectric-conversion part 160.

[0011] This invention was comprised in view of said reason,

The objective is to be able to achieve improvement in the speed of a response speed, and for manufacture to provide an easy near-infrared-light sensing element.

MEANS TO SOLVE THE PROBLEM

[0012] The photoelectric-conversion part which has a photodiode structure where invention of Claim 1 was formed in 1 surface side of a semiconductor substrate, and the drift area|region was provided

between p form area|region and n form area|region, absorbs near infrared light, and an electronic * hole pair generate|occur|produces,

With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked on the light-receiving surface of a photoelectric-conversion part, or is formed in said light-receiving-surface side in the inside of a photoelectric-conversion part, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface

The slab type|mold photonic crystal by which the refractive-index period structure was designed have a resonance peak is comprised,
It is characterized by the above-mentioned.

[0013] According to this invention

To 1 surface side of a semiconductor substrate

To the light-receiving surface of the formed photoelectric-conversion part

With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked, or is formed in said light-receiving-surface side in the inside of a photoelectric-conversion part, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface

By providing the slab type|mold photonic crystal by which the refractive-index period structure was designed have a resonance peak

Quantum efficiency can be raised even if it makes thin the thickness of the drift area|region of the photoelectric-conversion part of photodiode structures, such as a pin photodiode and an avalanche photo-diode, without providing a conventional vertical resonator,

Therefore

Can achieve improvement in the speed of a response speed, without making a light-reception sensitivity reduce, and again

The slab type|mold photonic crystal which was laminated|stacked on the photoelectric-conversion part or was formed in said light-receiving-surface side in the inside of a photoelectric-conversion part can be formed using the thin film coating technology, lithography technology, and etching technique which are general semiconductor manufacture process techniques,

Therefore

It can manufacture easily.

[0014] The near-infrared-light reflection part which invention of Claim 2 surrounds said photoelectric-conversion part in 1 said surface side of said semiconductor substrate in invention of Claim 1 by

two dimensional surface inside parallel to said light-receiving surface, and reflects the near infrared light of said wavelength range in said photoelectric-conversion part side is comprised,
It is characterized by the above-mentioned.

[0015] By providing the near-infrared-light reflection part which surrounds said photoelectric-conversion part by two dimensional surface inside parallel to said light-receiving surface, and reflects the near infrared light of said wavelength range in said photoelectric-conversion part side according to this invention

It can prevent that the near infrared light of said wavelength range that injected on said photoelectric-conversion part through said light-receiving surface leaks to the side of said photoelectric-conversion part,

Therefore

Quantum efficiency can be raised more and a light-reception sensitivity can be raised further.

[0016] In invention of Claim 2, invention of Claim 3 said near-infrared-light reflection part

It is a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and consists of a two dimensional photonic crystal by which the refractive-index period structure was designed reflect the near infrared light of said wavelength range in said photoelectric-conversion part side,
It is characterized by the above-mentioned.

[0017] According to this invention, said near-infrared-light reflection part can be easily formed using the lithography technology and etching technique which are general semiconductor manufacture process techniques.

[0018] In invention of Claim 1 thru|or Claim 3, the shape of invention of Claim 4 of said p form area|region in two dimensional surface inside with said photoelectric-conversion part parallel to said light-receiving surface and each said n form area|region is comb-shaped,
Said p form area|region and said n form area|region are mutually complex,
The said drift area|region consists of an i layer interposed between said p form area|region and said n form area|region,
It is characterized by the above-mentioned.

[0019] According to this invention

The thickness (width of i layer) of said drift area|region that consists of an i layer which interposes the mask at the time of forming said p form area|region with a spreading|diffusion or an ion implantation and said n form area|region between said p form area|region and said n form area|

region with relative position accuracy with the mask at the time of forming with a spreading| diffusion or an ion implantation is decided,

Therefore

The precision of the thickness dimension of said drift area|region can be raised.

[0020] ADVANTAGE OF THE INVENTION

Invention of Claim 1 can achieve improvement in the speed of a response speed, and is effective in the ability to manufacture easily.

PREFERRED EMBODIMENT OF THE INVENTION

[0021] (Embodiment 1)

As shown to FIG. 1 (a), (b), the near-infrared-rays sensing element of this embodiment

While the semiconductor layer 3 which consists of a single-crystal Si layer of low concentration (For example, 10^{13} ~ 10^{16} cm⁻³ extent) via the 1st dielectric layer 2 which consists of a SiO₂ film|membrane on the 1 surface of the semiconductor substrate 1 which consists of a Si board| substrate is provided

The 2nd dielectric layer 4 which consists of a SiO₂ film|membrane is provided on said semiconductor layer 3,

The photoelectric-conversion part 6 which has a photodiode structure of a pin photodiode, absorbs near infrared light, and an electronic * hole pair generate|occur|produces is formed in the center section of the semiconductor layer 3.

In the center section of the 2nd dielectric layer 4, the light-receiving surface of the photoelectric-conversion part 6

With respect to the wavelength range of the near infrared light of the detection target by which injection|incidence (In this embodiment, it injected from the reverse side with the semiconductor substrate 1 side.) is carried out from the direction which is a slab type|mold photonic crystal which has a refractive-index period structure in two dimensional surface inside parallel to (the upper surface in FIG.1(b)), and intersects said light-receiving surface

The slab type|mold photonic crystal 7 by which the refractive-index period structure was designed have a resonance peak is formed.

In addition, in this embodiment, the material of the 1st dielectric layer 2 and the 2nd dielectric layer 4 is SiO₂,

The semiconductor crystal material of the photoelectric-conversion part 6 is Si,

Therefore

The refractive index of the semiconductor layer 3 becomes a high value rather than each refractive index of the 1st dielectric layer 2 and the 2nd dielectric layer 4, and in (The refractive index of

about 1.5 and Si of the refractive index of SiO₂ is about 3.4.) and the photoelectric-conversion part 6

The waveguide mode which confines the near infrared light which injected from the light-receiving surface in the photoelectric-conversion part 6 according to a refractive-index difference with the medium of the both sides of the photoelectric-conversion part 6, and waveguides it exists, Quantum efficiency can be raised.

[0022] In here, the near-infrared-light sensing element of this embodiment is used as a light receiving element of an optical communication,

A 0.8-micrometer belt|band|zone is assumed as a wavelength range of the near infrared light (input-signal light) of a detection target,

Si is employ|adopted as a semiconductor crystal material of the photoelectric-conversion part 6, Si board|substrate is used as a semiconductor substrate 1.

[0023] The photoelectric-conversion part 6 is with the p form area|region 61 where the shape in two dimensional surface inside parallel to said light-receiving surface consists of a comb-shaped p<+> layer, as shown to FIG.1(b) and (c),

The n form area|region 63 where the shape in two dimensional surface inside parallel to said light-receiving surface consists of a comb-shaped n<+> layer is mutually complex,

In the shape in surface inside parallel to said light-receiving surface, the i layer 62 of an undulation state (the shape of a winding path) is interposing between the p form area|region 61 and the n form area|region 63.

In here, the comb-tooth parts 61b and 63b of multiple (the example of illustration three) which it was equally spaced and were spaced apart are continuously formed in the left-right direction of FIG.1(c) at each of comb bone 61a, 63a with circular arc-shaped p form area|region 61 and n form area|region 63,

In the left-right direction of FIG.1(c), the comb-tooth part 61b of the p form area|region 61 and the comb-tooth part 63b of the n form area|region 63 are alternately located in a line.

In addition, the shape in two dimensional surface inside with the photoelectric-conversion part 6 parallel to said light-receiving surface is formed in circular as a whole.

Moreover, in this embodiment, the i layer 62 is comprising the drift area|region provided between the p form area|region 61 and the n form area|region 63.

- [0024] Moreover, the contact hole is formed in the region to which the near-infrared-light sensing element of this embodiment overlaps with the p form area|region 61 in the 2nd dielectric layer 4,
The contact electrode 8a which consists of a metal material which was embedded at said contact hole and was electrically connected with the p form area|region 61 is electrically connected via Pad 10a and the metal wiring 9a which were formed on the 2nd dielectric layer 4.
Similarly, the contact hole is formed in the region which overlaps with the n form area|region 63 in the 2nd dielectric layer 4,
The contact electrode 8b which consists of a metal material which was embedded at said contact hole and was electrically connected with the n form area|region 63 is electrically connected via Pad 10b and the metal wiring 9b which were formed on the 2nd dielectric layer 4.
- [0025] Moreover, the slab type|mold photonic crystal 7 is arranged so that it may have a 2-dimensional period structure by surface inside (Two dimensional surface inside parallel to the light-receiving surface of the photoelectric-conversion part 6 in other words) which many holes 72 orthogonally cross in the thickness direction of slab 71 which consists of a region currently laminated|stacked on the photoelectric-conversion part 6 among the 2nd dielectric layers 4,
The slab type|mold photonic crystal 7 which has said refractive-index period structure by the low-refractive-index medium which consists of air in the high refractive index medium which comprises slab 71, and hole 72 is comprised.
When a unit cell specifically forms hole 72 in each location corresponding to each lattice point of the hypothetical|virtual two dimensional triangular grating|lattice of an equilateral triangle in slab 71, the slab type|mold photonic crystal 7 is formed.
If it paraphrases, hole 72 is arranged by triangular grating|lattice shape in surface inside orthogonally crossed in the thickness direction of slab 71.
In addition, the refractive index of about 1.5 and air of the refractive index of SiO₂ which is the material of the 2nd dielectric layer 4 is 1.
- [0026] The said refractive-index period structure is designed in design of the slab type|mold photonic crystal 7 have a resonance peak in the wavelength range of the near infrared light of a detection target as mentioned above.
Specifically, a, then Period a should just set period (It is a period of the refractive-index period structure of the slab type|mold photonic crystal 7, and is the distance during the lattice point of a two dimensional triangular grating|lattice.) of the sequence direction of hole 72 in the slab type|

mold photonic crystal 7 to the half-wave-length extent (For example, $1/2$ of the wavelength of an infrared-light) of the infrared-light of said wavelength range, for example.

In addition, about the optical propagation part which is the principal part comprised in the slab type|mold photonic crystal 7 and the photoelectric-conversion part 6 among the near-infrared-light sensing elements of this embodiment

The semiconductor substrate 1 and a reverse side have a refractive-index difference with the air (refractive-index =1) which is a medium of slab type|mold photonic-crystal 7 and slab type|mold photonic-crystal 7 just overhead,

The semiconductor substrate 1 side has the 1st dielectric layer (refractive-index =1.5) 2 and 1st refractive-index difference which are the mediums of photoelectric-conversion part 6 directly under.

When there exist the medium and the above refractive-index differences which said optical propagation part is touching by each of up-and-down both sides (both sides of the thickness direction of the semiconductor substrate 1) in such an optical propagation part

There exist waveguide mode in which the near infrared light which propagates an optical propagation part satisfy|fills the total-reflection conditions of a up-down direction, and is completely

confined in an optical propagation part, and a mode (It calls in-plane resonance mode hereafter) which does not satisfy total-reflection conditions but can be couple|bonded with ambient light. When near infrared light is injected on such an optical propagation part from the exterior, one part near infrared light will couple|bond with in-plane resonance mode, Any of in-plane resonance mode and waveguide mode, may not couple|bond another one part and it may be permeate|transmitted.

However,

As negate / after couple|bonding with in-plane resonance mode / the near infrared light re-radiated and the near infrared light to permeate|transmit

In this case, all the near infrared light which injected on the optical propagation part couple|bonds with in-plane resonance mode.

Thus, the light couple|bonded with in-plane resonance mode propagates the inside of an optical propagation part according to Q value of a resonance peak,

Therefore

Without providing a vertical resonator like the conventional structure of FIG. 4, in the thickness of the i layer 62 in the photoelectric-conversion part 6, even if thin, near infrared light is efficiently absorbed in the i layer 62.

Moreover, in this embodiment, all the near infrared light of said wavelength range that injects on an optical propagation part couple|bonds with in-plane resonance mode,

Therefore

It is not necessary to provide a reflection layer like DBR at a reverse side separately with the light-receiving surface in the photoelectric-conversion part 6.

In addition, in-plane resonance mode is reported as guided resonances in publication 1 (Shanhui Fan, et al, Analysis of guided resonances in photonic crystal slabs, PHYSICAL REVIEW B, VOLUME 65, 235112).

[0027] By the way, the near-infrared-light sensing element of this embodiment is formed in the middle of the thickness direction what is called using SOI(Silicon On Insulator) board|substrate which has a SiO₂ film|membrane,

Si board|substrate of the back side in an SOI board|substrate comprises the semiconductor substrate 1,

The SiO₂ film|membrane of an SOI board|substrate comprises the 1st dielectric layer 2,

Si layer of the main surface side of an SOI board|substrate is comprising the semiconductor layer 3.

That is, the photoelectric-conversion part 6 in a near-infrared-light sensing element is formed by introduce|transducing an impurity to the region corresponding to the each of the p form area|region 61 and the n form area|region 63 with a spreading|diffusion or an ion implantation in the

semiconductor layer 3 which consists of a Si layer of the main surface side of an SOI board| substrate,

Therefore

With relative position accuracy with the mask at the time of forming the mask at the time of forming the p form area|region 61 with a spreading|diffusion or an ion implantation, and the n form area| region 63 with a spreading|diffusion or an ion implantation

The thickness (It is the width of the i layer 62,

Comprising:

The distance of a career|carrier) of the i layer 62 which consists of a region interposed between the p form area|region 61 and the n form area|region 63 among the semiconductor layers 3 is decided, Therefore

The precision of the thickness dimension of the i layer 62 can be raised.

[0028] Moreover, after the slab type|mold photonic crystal 7 forms the photoelectric-conversion part 6 in the semiconductor layer 3 which consists of a Si layer of the main surface side of an SOI board| substrate

After forming the 2nd dielectric layer 4 into a film with thin-film formation methods, such as CVD method, to the whole surface of the main surface side of an SOI board|substrate, the resist layer by which the region corresponding to each hole 72 was pierced using the lithography technology is formed on the 2nd dielectric layer 4,

It can form by etching the region corresponding to each hole 72 by the dry etching apparatus among the 2nd dielectric layers 4 by setting said resist layer as a mask.

In addition, not only SiO₂ but Si₃N₄ may be sufficient as the medium which comprises slab 71, for example.

[0029] The near-infrared-light sensing element of this embodiment demonstrated above The slab type|mold photonic crystal 7 by which the refractive-index period structure of two dimensional surface inside parallel to said light-receiving surface was designed have a resonance peak with respect to the wavelength range of the near infrared light of the detection target which is

laminated|stacked on the light-receiving surface of the photoelectric-conversion part 6, and injects from a reverse side with the photoelectric-conversion part 6 side is provided,

Therefore

Quantum efficiency can be raised even if it makes thin thickness (width) of the i layer 62 of the photoelectric-conversion part 6 of the photodiode structure of a pin photodiode, without providing a vertical resonator like a structure before shown in FIG. 4,

Therefore

Improvement in the speed of a response speed can be achieved without making a light-reception sensitivity reduce.

Moreover, the slab type|mold photonic crystal 7 laminated|stacked on the photoelectric-conversion part 6 can be formed using the thin film coating technology, lithography technology, and etching technique which are general semiconductor manufacture process techniques,

Therefore

It can manufacture easily.

[0030] (Embodiment 2)

The basic composition of the near-infrared-light sensing element of this embodiment is substantially the same as Embodiment 1,

Comprising:

The point currently formed as shown in FIG. 2 in the form where the p form area|region 61 and the i layer 62 in the photoelectric-conversion part 6, and the n form area|region 63 are located in a line with the thickness direction of the semiconductor substrate 1 is different.

In addition, the same code is attached to the same component as Embodiment 1, and description is abbreviate|omitted.

- [0031]** The p form area|region 61 and the n form area|region 63 of the photoelectric-conversion part 6 in this embodiment are formed in the shape where the shape in two dimensional surface inside parallel to said light-receiving surface notched partial circle as shown in FIG.2(c), (d),
The region interposed between the p form area|region 61 and the n form area|region 63 among the semiconductor layers 3 is comprising the i layer 62.
In addition, the p form area|region 61 and the n form area|region 63 are formed by introduce|transducing an impurity to the region corresponding to the each of the p form area|region 61 and the n form area|region 63 with a spreading|diffusion or an ion implantation in the semiconductor layer 3.

- [0032] Moreover, the p form area|region 61 and the n form area|region 63 space apart the near-infrared-light sensing element of this embodiment in the thickness direction of the semiconductor substrate 1, and it is formed,
The n form area|region 63 is formed in the position distant from the 2nd dielectric layer 4,
Therefore
The spreading|diffusion wiring 63c (refer FIG.2(c)) for connecting electrically the n form area|region 63 and the contact electrode 8b is formed in the semiconductor layer 3.
In addition, each contact electrode 8a, 8b are formed in the region which overlaps with each circumference of the p form area|region 61 and the n form area|region 63 in the 2nd dielectric layer 4.
- [0033] Thus, without making a light-reception sensitivity reduce, improvement in the speed of a response speed can be achieved, and the near-infrared-light sensing element of this embodiment as well as Embodiment 1 can be manufactured easily.
- [0034] (Embodiment 3)
The basic composition of the near-infrared-light sensing element of this embodiment is substantially the same as Embodiment 1,
Comprising:
A point provided with the near-infrared-light reflection part 11 which surrounds the photoelectric-conversion part 6 in 1 said surface side of the semiconductor substrate 1 by two dimensional surface inside parallel to the light-receiving surface of the photoelectric-conversion part 6, and, as shown in FIG. 3, reflects the near infrared light of the wavelength range of a detection target in the photoelectric-conversion part 6 side is different.
In addition, the same code is attached to the same component as Embodiment 1, and description is abbreviate|omitted.

[0035] By the way, the near-infrared-light reflection part 11 in this embodiment is a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside with the near-infrared-light reflection part 11 parallel to said light-receiving surface, It arranges so that it may have a 2-dimensional period structure by two dimensional surface inside which many holes 11a orthogonally cross in the thickness direction of slab 11b which consists of some semiconductor layers 3,

The two dimensional photonic crystal which has said refractive-index period structure by the low-refractive-index medium which consists of air in the high refractive index medium (here Si) which comprises Slab 11b, and Hole 11a is comprised.

Specifically, when a unit cell forms Hole 11a in Slab 11b at each lattice point of the hypothetical virtual two dimensional triangular grating|lattice of an equilateral triangle, the two dimensional photonic crystal 11 is formed.

If it paraphrases, Hole 11a is arranged by triangular grating|lattice shape in surface inside orthogonally crossed in the thickness direction of Slab 11b.

[0036] The said refractive-index period structure is designed reflect the near infrared light of the wavelength range of a detection target in the photoelectric-conversion part 6 side as mentioned above in design of the two dimensional photonic crystal 11 in here.

Specifically, b, then Period b should just set period (It is a period of the refractive-index period structure of the two dimensional photonic crystal 11, and is the distance during the lattice point of a two dimensional triangular grating|lattice.) of the sequence direction of hole 11a in the two dimensional photonic crystal 11 to the half-wave-length extent (For example, 1/2 of the wavelength of an infrared-light) of the infrared-light of said wavelength range, for example.

[0037] Thus, in the near-infrared-light sensing element of this embodiment, it can prevent that the near infrared light of said wavelength range that injected on the photoelectric-conversion part 6 through said light-receiving surface leaks to the side of the photoelectric-conversion part 6 by providing the above-mentioned near-infrared-light reflection part 11,

Therefore

Quantum efficiency can be raised more and a light-reception sensitivity can be raised further.

Moreover, it comprises the two dimensional photonic crystal by which the refractive-index period structure was designed so that the near-infrared-light reflection part 11 might be a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside

parallel to said light-receiving surface and might reflect the near infrared light of said wavelength range in the photoelectric-conversion part 6 side,

Therefore

The near-infrared-light reflection part 11 can be easily formed using the lithography technology and etching technique which are general semiconductor manufacture process techniques.

In addition, in this embodiment, the two dimensional photonic crystal 11 is comprised according to the period structure of two kinds of mediums of Si and air,

However,

It is substantial with the dielectric material (For example, SiO₂ etc.) into which a refractive index differs Hole 11a from Si, and it is sufficient to make it form the two dimensional photonic crystal 11 by said dielectric material and Si.

By the way, in each said Embodiment, Si is employ|adopted as a semiconductor crystal material of the photoelectric-conversion part 6,

Si board|substrate is used as a semiconductor substrate 1,

However,

Not only Si but Ge and compound-semiconductor crystal|crystallization material may be sufficient as the semiconductor crystal material of the photoelectric-conversion part 6, for example,

Not only Si board|substrate but Ge board|substrate, a GaAs board|substrate, etc. may be sufficient as the semiconductor substrate 1, for example.

Moreover, in each said Embodiment, the slab type|mold photonic crystal 7 was comprised according to the period structure of two kinds of mediums of SiO₂ and air,

However,

It is substantial with the dielectric material into which a refractive index differs the inside of hole 72 from SiO₂, and it is sufficient to make it form the slab type|mold photonic crystal 7 by said dielectric material and SiO₂.

Or it is good also as a period structure of the medium of 3 or more type,

For example

By forming Si₃N₄ film|membrane which coat|covers the internal peripheral surface of hole 72 provided at slab 71 which consists of SiO₂

It is sufficient to make it comprise the slab type|mold photonic crystal 7 by three kinds such as SiO₂, Si₃N₄, and air.

- [0038] Moreover, in each said Embodiment, the slab type|mold photonic crystal 7 is laminated|stacked on the light-receiving surface of the photoelectric-conversion part 6,
 However,
 Instead of laminating|stacking the slab type|mold photonic crystal 7 on the photoelectric-conversion part 6, it is sufficient to make it form in the light-receiving-surface side in the inside of the photoelectric-conversion part 6.
 Moreover, in each said Embodiment, the photoelectric-conversion part 6 has a photodiode structure of a pin photodiode where i layer was provided as a drift area|region 62 between the p form area|region 61 and the n form area|region 63,
 However,
 As long as the drift area|region is provided between the p form area|region 61 and the n form area|region 63, the photodiode structure of an avalanche photo-diode may be sufficient as the photoelectric-conversion part 6.
- [0039] Moreover, to slab 71, the slab type|mold photonic crystal 7 in each said Embodiment is formed, when a unit cell forms hole 72 in each location corresponding to each lattice point of the hypothetical|virtual two dimensional triangular grating|lattice of an equilateral triangle,
 However,
 Not only an equilateral triangle but a square may be sufficient as a unit cell, for example,
 In this case, a unit cell should just form hole 72 in the region corresponding to each lattice point of a square hypothetical|virtual two dimensional tetragonal lattice.
 Moreover, in each said Embodiment, in order to form the refractive-index period structure of the slab type|mold photonic crystal 7, many holes 72 are formed in slab 71,
 However,
 Instead of providing hole 72, it is sufficient to provide holes of another aperture|opening shape, such as a triangular-shaped hole and a rectangular hole, for example.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0040] FIG. 1: Embodiment 1 is shown,
 (a) is a schematic plan view,
 (b) is the schematic perspective view fractured by A-A' of (a),
 (c) is a horizontal sectional view.

FIG. 2: Embodiment 2 is shown,

- (a) is a schematic plan view,
- (b) is the schematic perspective view fractured by A-A' of (a),
- (c) is a horizontal sectional view,
- (d) is an another horizontal sectional view.

FIG. 3: Embodiment 3 is shown,

- (a) is a schematic plan view,
- (b) is the schematic perspective view fractured by A-A' of (a),
- (c) is a horizontal sectional view.

FIG. 4: It is a schematic sectional drawing which shows a prior art example.

DESCRIPTION OF SYMBOLS

- [0041] One semiconductor substrate
 The dielectric layer of 2 1st
 Three semiconductor layers
 The dielectric layer of 4 2nd
 Six photoelectric-conversion parts
 Seven slab type|molds photonic crystal
 8a,
 8b contact electrode
 9a,
 9b metal wiring
 10a,
 10b pad
 61 P form area|region
 62 I layer
 63 N form area|region
 71 slabs
 72 holes

1. 1. The photoelectric-conversion part which has a photodiode structure where formed in 1 surface side of a semiconductor substrate, and the drift area|region was provided between p form area|region and n form area|region, absorbs near infrared light, and an electronic * hole pair generate|occur|produces, With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked on the light-receiving

surface of a photoelectric-conversion part, or is formed in said light-receiving-surface side in the inside of a photoelectric-conversion part, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface
The slab type|mold photonic crystal by which the refractive-index period structure was designed have a resonance peak is comprised,

The near-infrared-light sensing element characterized by the above-mentioned.

2. 2. The near-infrared-light reflection part which surrounds said photoelectric-conversion part in 1 said surface side of said semiconductor substrate by two dimensional surface inside parallel to said light-receiving surface, and reflects the near infrared light of said wavelength range in said photoelectric-conversion part side is comprised,

The near-infrared-light sensing element of Claim 1 characterized by the above-mentioned.

3. 3. The said near-infrared-light reflection part is a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and it consists of a two dimensional photonic crystal by which the refractive-index period structure was designed reflect the near infrared light of said wavelength range in said photoelectric-conversion part side,

The near-infrared-light sensing element of Claim 2 characterized by the above-mentioned.

4. 4. The said photoelectric-conversion part has a comb-shaped shape of said p form area|region in two dimensional surface inside parallel to said light-receiving surface, and each said n form area|region, Said p form area|region and said n form area|region are mutually complex,

The said drift area|region consists of an i layer interposed between said p form area|region and said n form area|region,

The near-infrared-light sensing element in any one of Claim 1 thru|or Claim 3 characterized by the above-mentioned.

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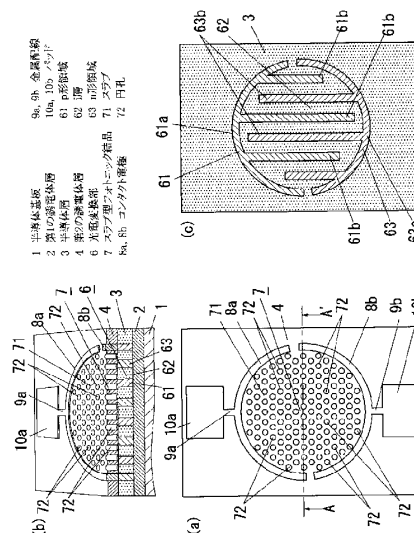
(54) 【発明の名称】 近赤外光検出素子

(57) 【要約】

【課題】 応答速度の高速化を図れ且つ製造が容易な近赤外光検出素子を提供する。

【解決手段】 半導体基板1の一表面側に形成されp形領域61とn形領域63との間にドリフト領域であるi層62が介在するpinフォトダイオードのフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部6と、光電変換部6の受光面に積層され当該受光面に平行な2次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって上記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶7とを備えている。

【選択図】 図1



【特許請求の範囲】

【請求項 1】

半導体基板の一表面側に形成され p 形領域と n 形領域との間にドリフト領域が設けられたフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部と、光電変換部の受光面に積層され若しくは光電変換部内における前記受光面側に形成され前記受光面に平行な 2 次元面内に屈折率周期構造を有するスラブ型フォトリック結晶であって前記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトリック結晶とを備えていることを特徴とする近赤外光検出素子。

【請求項 2】

前記半導体基板の前記一表面側において前記受光面に平行な 2 次元面内で前記光電変換部を囲み前記波長帯の近赤外光を前記光電変換部側へ反射する近赤外光反射部を備えていることを特徴とする請求項 1 記載の近赤外光検出素子。

【請求項 3】

前記近赤外光反射部は、前記受光面に平行な 2 次元面内に屈折率周期構造を有する 2 次元フォトリック結晶であって前記波長帯の近赤外光を前記光電変換部側へ反射するように屈折率周期構造が設計された 2 次元フォトリック結晶からなることを特徴とする請求項 2 記載の近赤外光検出素子。

【請求項 4】

前記光電変換部は、前記受光面に平行な 2 次元面内における前記 p 形領域および前記 n 形領域それぞれの形状が楕円形状であり、前記 p 形領域と前記 n 形領域とが互いに入り組んでおり、前記ドリフト領域が前記 p 形領域と前記 n 形領域との間に介在する i 層からなることを特徴とする請求項 1 ないし請求項 3 のいずれかに記載の近赤外光検出素子。

【発明の詳細な説明】

【技術分野】

【0001】

本発明は、近赤外光を検出する近赤外光検出素子に関するものである。

【背景技術】

【0002】

従来から、光通信では、光信号を受信するための受光素子として近赤外光検出素子が用いられている。この種の近赤外光検出素子としては、半導体結晶に p n 接合やショットキ接合を形成したフォトダイオード（p n フォトダイオード、p i n フォトダイオード、アバランシェフォトダイオード、ショットキフォトダイオードなど）が広く用いられ、バンドギャップ以上の光子エネルギーを有する光が入射された時に発生する電子・正孔対が分離されて空乏層内を走行（ドリフト）し外部回路に流れる電流が変化することを利用して、光信号を電流変化あるいは電圧変化として検出する。ここにおいて、近赤外光検出素子に用いられる半導体結晶材料としては、Si や Ge の他に、化合物半導体結晶材料（InGaAs、InGaAsP など）があるが、光通信で用いられる光の波長帯、要求されている通信速度、価格などにより使い分けられている。

【0003】

ところで、光通信は、都市間、都市内の通信網として既に広く使われているが、近年では、例えば高性能サーバとルータとをつなぐ SAN（Storage Area Network）、いわゆる情報家電と周辺機器とをつなぐ DVI（Digital Visual Interface）、車載 LAN（Local Area Network）、携帯電話機などの分野においても光通信を採用する動きが活発化している。このような分野でも高速の光通信が必要とされており、応用分野によって通信速度の高速化の進展は異なるが、いずれの分野においても 1 Gbps 以上の通信速度を要求されることが予測されている。

【0004】

上述のような各種分野で用いられる光通信用のフォトダイオードには今後、応答速度の高速化や低価格化が要求される。ここにおいて、フォトダイオードの応答速度は基本的に

はフォトダイオードのCR時定数と、空乏層内をドリフトするキャリア（電子、正孔）の走行時間 t との2つの要素で制限されることが知られている。半導体結晶材料としてSiを用いたpinフォトダイオードを例に考えると、CR時定数を小さくするとともに量子効率（受光感度）を高めるために、広い空乏層が形成されているので、空乏層内をドリフトする電子の走行時間 t が高速応答時には無視できなくなる。

【0005】

例えば、Siのpinフォトダイオードで量子効率を80%以上とするためには、30 μ m程度の空乏層幅 W が必要となるが、CR時定数で決まる遮断周波数 f_c (CR)は、受光径を250 μ mとすると、pn接合面積 A が $A=4.9 \times 10^{-4} \text{ cm}^2$ となり、空乏層幅 W が30 μ mとすればpn接合の接合容量 C_j が $C_j=0.17 \text{ pF}$ となるから、外部抵抗 R を50 Ω とすると、 $f_c(\text{CR})=1/(2\pi C_j R)=18 \text{ GHz}$ となる。

【0006】

一方、光電流の振幅が低周波領域の振幅の $1/2^{1/2}$ 、すなわち、電力が $1/2$ （-3dB）になる周波数を遮断周波数 $f(t_{tr})$ と定義すると、 $f_c(t_{tr})=0.44/t_{tr}$ となるが、Si結晶中をドリフトする電子の飽和ドリフト速度 v_{ds} が $v_{ds}=1 \times 10^7 \text{ cm/sec}$ であるため、空乏層内をドリフトする電子の走行時間 t_{tr} が $t_{tr}=W/v_{ds}=0.3 \text{ nsec}$ となり、遮断周波数 $f_c(t_{tr})$ は、 $f_c(t_{tr})=1.5 \text{ GHz}$ となる。上述のように、受光径が250 μ m、空乏層幅 W が30 μ mのSiのpinフォトダイオードについては、CR時定数から決まる遮断周波数 f_c (CR)が18GHzであったから、このpinフォトダイオードでは上述の走行時間 t_{tr} が遮断周波数を制限することとなり、1.5GHz近辺が動作周波数の限界であることが分かる。

【0007】

ここで、pinフォトダイオードの応答速度の高速化を図るには、遮断周波数を大きくする必要があるので、半導体結晶中のドリフト速度がSiに比べて速い半導体結晶材料である化合物半導体材料やGeなどを用いればよいが、シリコン半導体プロセスほどは量産性に優れておらず、また、ウェハ径も小さいので、低価格化が難しい。

【0008】

これに対して、近年、Siのpinフォトダイオード構造を有する光電変換部を基本構成とし、光電変換部においてキャリアがドリフトするドリフト領域であるi層の薄型化を図りながらも量子効率を向上することができ、しかもi層中をドリフトするキャリアの走行時間 t_{tr} の短縮による高速化を図れる近赤外光検出素子が提案されている（非特許文献1, 2）。

【0009】

この種の近赤外光検出素子は、図4に示すように、Si基板151の一表面上に第1のSiO₂層152aとSi層152bと第2のSiO₂層152cとの積層膜からなり近赤外光を反射するDBR（Distributed Bragg Reflector）152が設けられ、DBR152上にn⁺領域163とp⁺領域161との間にi層162が介在するSiのpinフォトダイオード構造からなる光電変換部160が設けられており、空気とp⁺領域161の表面からなる受光面との界面がSi基板151の厚み方向（縦方向）において光電変換部160を挟んでDBR152に対向する反射面を形成し、当該反射面とDBR152とでファブリペロー共振器（Fabry-Perot Resonator）からなる縦型の共振器を形成している。したがって、光電変換部160におけるi層162の厚みを小さく（つまり、i層162の幅を小さく）しても受光感度を向上することができ、i層162の厚みを薄くすることでキャリアの走行距離も短くできるので、応答速度の高速化を図ることができる。なお、p⁺領域161はSi基板151の上記一表面側でp電極165と電気的に接続され、n⁺領域163はSi基板151の上記一表面側でn電極163と電気的に接続されている。

【非特許文献1】M.K.Emsley, et al, 「Silicon Resonant Cavity Enhanced Photodetector Arrays for Optical Interconnects」, Proc. of SPIE Vol.5246, p409-421, 2003

【非特許文献2】M.K.Emsley, et al, 「Silicon Substrates With Buried Distributed Br

agg Reflectors for Resonant Cavity-Enhanced Optoelectronics」, IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, VOL.8, NO.4, p948-955, JULY/AUGUST 2002

【発明の開示】

【発明が解決しようとする課題】

【0010】

しかしながら、図4に示した構成の近赤外光検出素子を製造するには、光電変換部160の形成前に、SOIウェハの形成方法の1つとして知られている水素注入剥離法で必要な基本工程（水素イオン注入工程、貼り合わせ工程、剥離工程、表面研磨工程）を2回繰り返す必要があり、製造プロセスが複雑で低コスト化が難しかった。また、上述の赤外光検出素子の製造方法はSi以外の半導体結晶材料を光電変換部160の材料として採用する場合には適用することができない。

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【0011】

本発明は上記事由に鑑みて為されたものであり、その目的は、応答速度の高速化を図れ且つ製造が容易な近赤外光検出素子を提供することにある。

【課題を解決するための手段】

【0012】

請求項1の発明は、半導体基板の一表面側に形成されp形領域とn形領域との間にドリフト領域が設けられたフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部と、光電変換部の受光面に積層され若しくは光電変換部内における前記受光面側に形成され前記受光面に平行な2次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって前記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶とを備えてなることを特徴とする。

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【0013】

この発明によれば、半導体基板の一表面側に形成された光電変換部の受光面に積層され若しくは光電変換部内における前記受光面側に形成され前記受光面に平行な2次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって前記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶を備えていることにより、従来のような縦型の共振器を設けることなくpinフォトダイオードやアバランシェフォトダイオードなどのフォトダイオード構造の光電変換部のドリフト領域の厚さを薄くしても量子効率を高めることができるので、受光感度を低下させることなく応答速度の高速化を図れ、また、光電変換部に積層され若しくは光電変換部内における前記受光面側に形成されたスラブ型フォトニック結晶は一般的な半導体製造プロセス技術である薄膜形成技術とリソグラフィ技術とエッチング技術とを利用して形成することができるので、容易に製造することができる。

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【0014】

請求項2の発明は、請求項1の発明において、前記半導体基板の前記一表面側において前記受光面に平行な2次元面内で前記光電変換部を囲み前記波長帯の近赤外光を前記光電変換部側へ反射する近赤外光反射部を備えてなることを特徴とする。

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【0015】

この発明によれば、前記受光面に平行な2次元面内で前記光電変換部を囲み前記波長帯の近赤外光を前記光電変換部側へ反射する近赤外光反射部を備えていることにより、前記受光面を通して前記光電変換部へ入射された前記波長帯の近赤外光が前記光電変換部の側方へ漏れるのを防止することができるので、量子効率をより高めることができ、受光感度をより一層高めることができる。

【0016】

請求項3の発明は、請求項2の発明において、前記近赤外光反射部は、前記受光面に平行な2次元面内に屈折率周期構造を有する2次元フォトニック結晶であって前記波長帯の近赤外光を前記光電変換部側へ反射するように屈折率周期構造が設計された2次元フォト

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ニック結晶からなることを特徴とする。

【0017】

この発明によれば、前記近赤外光反射部を一般的な半導体製造プロセス技術であるリソグラフィ技術とエッチング技術とを利用して容易に形成することができる。

【0018】

請求項4の発明は、請求項1ないし請求項3の発明において、前記光電変換部は、前記受光面に平行な2次元面内における前記p形領域および前記n形領域それぞれの形状が櫛形状であり、前記p形領域と前記n形領域とが互いに入り組んでおり、前記ドリフト領域が前記p形領域と前記n形領域との間に介在するi層からなることを特徴とする。

【0019】

この発明によれば、前記p形領域を拡散もしくはイオン注入により形成する際のマスクと前記n形領域を拡散もしくはイオン注入により形成する際のマスクとの相対的な位置精度により前記p形領域と前記n形領域との間に介在するi層からなる前記ドリフト領域の厚み(i層の幅)が決まるので、前記ドリフト領域の厚み寸法の精度を高めることができる。

【発明の効果】

【0020】

請求項1の発明は、応答速度の高速化を図れ且つ容易に製造することができるという効果がある。

【発明を実施するための最良の形態】

【0021】

(実施形態1)

本実施形態の近赤外線検出素子は、図1(a)、(b)に示すように、Si基板からなる半導体基板1の一表面上にSiO₂膜からなる第1の誘電体層2を介して低濃度(例えば、 $10^{13} \sim 10^{16} \text{ cm}^{-3}$ 程度)の単結晶Si層からなる半導体層3が設けられるとともに、当該半導体層3上にSiO₂膜からなる第2の誘電体層4が設けられており、半導体層3の中央部にpinフォトダイオードのフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部6が形成され、第2の誘電体層4の中央部に光電変換部6の受光面(図1(b)における上面)に平行な2次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって上記受光面に交差する方向から入射(本実施形態では、半導体基板1側とは反対側から入射)される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶7が形成されている。なお、本実施形態では、第1の誘電体層2および第2の誘電体層4の材料がSiO₂であり、光電変換部6の半導体結晶材料がSiであるので、第1の誘電体層2および第2の誘電体層4それぞれの屈折率よりも半導体層3の屈折率が高い値となっており(SiO₂の屈折率は1.5程度、Siの屈折率は3.4程度である)、光電変換部6には、受光面から入射された近赤外光を光電変換部6の両側の媒質との屈折率差により光電変換部6内に閉じ込めて導波する導波モードが存在しており、量子効率を高めることができる。

【0022】

ここにおいて、本実施形態の近赤外光検出素子は、光通信の受光素子として用いるものであり、検出対象の近赤外光(入力信号光)の波長帯として0.8μm帯を想定しており、光電変換部6の半導体結晶材料としてSiを採用し、半導体基板1としてSi基板を用いている。

【0023】

光電変換部6は、図1(b)、(c)に示すように、上記受光面に平行な2次元面内における形状が櫛形状のp⁺層からなるp形領域61と、上記受光面に平行な2次元面内における形状が櫛形状のn⁺層からなるn形領域63とが、互いに入り組んでおり、p形領域61とn形領域63との間に上記受光面に平行な面内における形状が蛇行状(つづら折れ状)のi層62が介在している。ここにおいて、p形領域61およびn形領域63は円

弧状の櫛歯部 61a, 63a それぞれに、図 1 (c) の左右方向に等間隔で離間した複数 (図示例では、3つ) の櫛歯部 61b, 63b が連続して形成されており、図 1 (c) の左右方向において p 形領域 61 の櫛歯部 61b と n 形領域 63 の櫛歯部 63b とが交互に並んでいる。なお、光電変換部 6 は、上記受光面に平行な 2 次元面内における形状が、全体として円形状に形成されている。また、本実施形態では、i 層 62 が p 形領域 61 と n 形領域 63 との間に設けられたドリフト領域を構成している。

【0024】

また、本実施形態の近赤外光検出素子は、第 2 の誘電体層 4 において p 形領域 61 に重なる部位にコンタクト孔が形成されており、当該コンタクト孔に埋め込まれ p 形領域 61 と電氣的に接続された金属材料からなるコンタクト電極 8a が、第 2 の誘電体層 4 上に形成されたパッド 10a と金属配線 9a を介して電氣的に接続されている。同様に、第 2 の誘電体層 4 において n 形領域 63 に重なる部位にコンタクト孔が形成されており、当該コンタクト孔に埋め込まれ n 形領域 63 と電氣的に接続された金属材料からなるコンタクト電極 8b が、第 2 の誘電体層 4 上に形成されたパッド 10b と金属配線 9b を介して電氣的に接続されている。

【0025】

また、スラブ型フォトリソニック結晶 7 は、多数の円孔 72 が、第 2 の誘電体層 4 のうち光電変換部 6 に積層されている部位からなるスラブ 71 の厚み方向に直交する面内 (つまり、光電変換部 6 の受光面に平行な 2 次元面内) で 2 次元的な周期構造を有するように配列されており、スラブ 71 を構成する高屈折率媒質と円孔 72 内の空気からなる低屈折率媒質とで上記屈折率周期構造を有するスラブ型フォトリソニック結晶 7 を構成している。具体的には、スラブ 71 において、単位格子が正三角形の仮想的な 2 次元三角格子の各格子点に対応する各部位に円孔 72 を形成することにより、スラブ型フォトリソニック結晶 7 を形成してある。言い換えれば、円孔 72 はスラブ 71 の厚み方向に直交する面内において三角格子状に配列されている。なお、第 2 の誘電体層 4 の材料である SiO_2 の屈折率は 1.5 程度、空気の屈折率は 1 である。

【0026】

スラブ型フォトリソニック結晶 7 の設計にあたっては、上述のように検出対象の近赤外光の波長帯に共振ピークを有するように上記屈折率周期構造が設計されている。具体的には、例えば、スラブ型フォトリソニック結晶 7 における円孔 72 の配列方向の周期 (スラブ型フォトリソニック結晶 7 の屈折率周期構造の周期であって 2 次元三角格子の格子点間の距離) を a とすれば、周期 a は上記波長帯の赤外光の半波長程度 (例えば、赤外光の波長の 2 分の 1) に設定すればよい。なお、本実施形態の近赤外光検出素子のうちスラブ型フォトリソニック結晶 7 と光電変換部 6 とで構成された主要部である光伝搬部については、半導体基板 1 と反対側はスラブ型フォトリソニック結晶 7 とスラブ型フォトリソニック結晶 7 直上の媒質である空気 (屈折率 = 1) との屈折率差があり、半導体基板 1 側は光電変換部 6 直下の媒質である第 1 の誘電体層 (屈折率 = 1.5) との屈折率差がある。このような光伝搬部では、当該光伝搬部が上下両側 (半導体基板 1 の厚み方向の両側) それぞれで接している媒質と上述のような屈折率差があることにより、光伝搬部を伝搬する近赤外光が上下方向の全反射条件を満たして完全に光伝搬部内に閉じ込められる導波モードと、全反射条件を満たさず外部光と結合可能なモード (以下、面内共振モードと呼ぶ) とがある。このような光伝搬部に外部から近赤外光を入射すると、一部の近赤外光が面内共振モードに結合し、別の一部は面内共振モードおよび導波モードのいずれにも結合せず透過する場合もあるが、面内共振モードに結合した後に再放射される近赤外光と透過する近赤外光とが打ち消されるような場合も存在し、この場合には光伝搬部に入射された全ての近赤外光が面内共振モードに結合する。このように面内共振モードに結合した光は、共振ピークの Q 値に応じて光伝搬部内を伝搬していくことになるので、図 4 の従来構成のような縦型の共振器を設けることなく光電変換部 6 における i 層 62 の厚みを薄くても i 層 62 にて近赤外光が効率良く吸収されることになる。また、本実施形態では、光伝搬部に入射される上記波長帯の近赤外光の全てが面内共振モードに結合するので、光電変換部 6 における受光面とは反対側に D

B Rのような反射層を別途設ける必要もない。なお、面内共振モードは、刊行物 1 (Shan hui Fan, et al, 「Analysis of guided resonances in photonic crystal slabs」, PHYSICAL REVIEW B, VOLUME 65, 235112) において「guided resonances」として報告されている。

【0027】

ところで、本実施形態の近赤外光検出素子は、厚み方向の中間に SiO_2 膜を有する所謂 SOI (Silicon On Insulator) 基板を用いて形成してあり、SOI 基板における裏面側の Si 基板が半導体基板 1 を構成し、SOI 基板の SiO_2 膜が第 1 の誘電体層 2 を構成し、SOI 基板の主表面側の Si 層が半導体層 3 を構成している。すなわち、近赤外光検出素子における光電変換部 6 は、SOI 基板の主表面側の Si 層からなる半導体層 3 において p 形領域 61 および n 形領域 63 それぞれに対応する部位に不純物を拡散もしくはイオン注入によって導入することにより形成されているので、p 形領域 61 を拡散もしくはイオン注入により形成する際のマスクと n 形領域 63 を拡散もしくはイオン注入により形成する際のマスクとの相対的な位置精度により、半導体層 3 のうち p 形領域 61 と n 形領域 63 との間に介在する部位からなる i 層 62 の厚さ (i 層 62 の幅であって、キャリアの走行距離) が決まるので、i 層 62 の厚み寸法の精度を高めることができる。

【0028】

また、スラブ型フォトニック結晶 7 は、SOI 基板の主表面側の Si 層からなる半導体層 3 に光電変換部 6 を形成した後で、SOI 基板の主表面側の全面に第 2 の誘電体層 4 を例えば CVD 法などの薄膜形成方法により成膜してから、第 2 の誘電体層 4 上にリソグラフィ技術を利用して各円孔 72 に対応する部位が開孔されたレジスト層を形成し、当該レジスト層をマスクとして第 2 の誘電体層 4 のうち各円孔 72 に対応する部位をドライエッチング装置によりエッチングすることによって形成することができる。なお、スラブ 71 を構成する媒質は SiO_2 に限らず、例えば、 Si_3N_4 でもよい。

【0029】

以上説明した本実施形態の近赤外光検出素子は、光電変換部 6 の受光面に積層され光電変換部 6 側とは反対側から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように上記受光面に平行な 2 次元面内の屈折率周期構造が設計されたスラブ型フォトニック結晶 7 を備えているので、図 4 に示した従来構成のような縦型の共振器を設けることなく pin フォトダイオードのフォトダイオード構造の光電変換部 6 の i 層 62 の厚み (幅) を薄くしても量子効率を高めることができるので、受光感度を低下させることなく応答速度の高速化を図れる。また、光電変換部 6 に積層されたスラブ型フォトニック結晶 7 は一般的な半導体製造プロセス技術である薄膜形成技術とリソグラフィ技術とエッチング技術とを利用して形成することができるので、容易に製造することができる。

【0030】

(実施形態 2)

本実施形態の近赤外光検出素子の基本構成は実施形態 1 と略同じであって、図 2 に示すように、光電変換部 6 における p 形領域 61 と i 層 62 と n 形領域 63 とが半導体基板 1 の厚み方向に並ぶ形で形成されている点が相違する。なお、実施形態 1 と同様の構成要素には同一の符号を付して説明を省略する。

【0031】

本実施形態における光電変換部 6 の p 形領域 61 および n 形領域 63 は、図 2 (c), (d) に示すように、上記受光面に平行な 2 次元面内における形状が円の一部分を切り欠いた形状に形成されており、半導体層 3 のうち p 形領域 61 と n 形領域 63 との間に介在する部位が i 層 62 を構成している。なお、p 形領域 61 および n 形領域 63 は、半導体層 3 において p 形領域 61 および n 形領域 63 それぞれに対応する部位に不純物を拡散もしくはイオン注入によって導入することにより形成されている。

【0032】

また、本実施形態の近赤外光検出素子は、p 形領域 61 と n 形領域 63 とが半導体基板 1 の厚み方向に離間して形成されており、n 形領域 63 が第 2 の誘電体層 4 から離れた位

置に形成されているので、n形領域63とコンタクト電極8bとを電氣的に接続するための拡散配線63c(図2(c)参照)を半導体層3に形成してある。なお、各コンタクト電極8a, 8bは、第2の誘電体層4において、p形領域61およびn形領域63それぞれの周部に重なる部位に形成されている。

【0033】

しかし、本実施形態の近赤外光検出素子も、実施形態1と同様に、受光感度を低下させることなく応答速度の高速化を図れ且つ容易に製造することができる。

【0034】

(実施形態3)

本実施形態の近赤外光検出素子の基本構成は実施形態1と略同じであって、図3に示すように、半導体基板1の上記一表面側において光電変換部6の受光面に平行な2次元面内で光電変換部6を囲み検出対象の波長帯の近赤外光を光電変換部6側へ反射する近赤外光反射部11を備えている点が相違する。なお、実施形態1と同様の構成要素には同一の符号を付して説明を省略する。

【0035】

ところで、本実施形態における近赤外光反射部11は、近赤外光反射部11が上記受光面に平行な2次元面内に屈折率周期構造を有する2次元フォトリソニック結晶であり、多数の円孔11aが半導体層3の一部からなるスラブ11bの厚み方向に直交する2次元面内で2次元的な周期構造を有するように配列されており、スラブ11bを構成する高屈折率媒質(ここでは、Si)と円孔11a内の空気からなる低屈折率媒質とで上記屈折率周期構造を有する2次元フォトリソニック結晶を構成している。具体的には、スラブ11bに、単位格子が正三角形の仮想的な2次元三角格子の各格子点に円孔11aを形成することにより、2次元フォトリソニック結晶11を形成してある。言い換えれば、円孔11aはスラブ11bの厚み方向に直交する面内において三角格子状に配列されている。

【0036】

ここにおいて、2次元フォトリソニック結晶11の設計にあたっては、上述のように検出対象の波長帯の近赤外光を光電変換部6側へ反射するように上記屈折率周期構造が設計されている。具体的には、例えば、2次元フォトリソニック結晶11における円孔11aの配列方向の周期(2次元フォトリソニック結晶11の屈折率周期構造の周期であって2次元三角格子の格子点間の距離)をbとすれば、周期bは上記波長帯の赤外光の半波長程度(例えば、赤外光の波長の2分の1)に設定すればよい。

【0037】

しかし、本実施形態の近赤外光検出素子では、上述の近赤外光反射部11を備えていることにより、上記受光面を通して光電変換部6へ入射された上記波長帯の近赤外光が光電変換部6の側方へ漏れるのを防止することができるので、量子効率をより高めることができ、受光感度をより一層高めることができる。また、近赤外光反射部11が上記受光面に平行な2次元面内に屈折率周期構造を有する2次元フォトリソニック結晶であって上記波長帯の近赤外光を光電変換部6側へ反射するように屈折率周期構造が設計された2次元フォトリソニック結晶により構成されているので、近赤外光反射部11を一般的な半導体製造プロセス技術であるリソグラフィ技術とエッチング技術とを利用して容易に形成することができる。なお、本実施形態では、2次元フォトリソニック結晶11をSiと空気との2種類の媒質の周期構造により構成しているが、円孔11aをSiとは屈折率の異なる誘電体材料(例えば、SiO₂など)により充実して当該誘電体材料とSiとで2次元フォトリソニック結晶11を形成するようにしてもよい。

ところで、上記各実施形態では、光電変換部6の半導体結晶材料としてSiを採用し、半導体基板1としてSi基板を用いているが、光電変換部6の半導体結晶材料はSiに限らず、例えば、Geや化合物半導体結晶材料でもよく、半導体基板1もSi基板に限らず、例えば、Ge基板やGaAs基板などでもよい。また、上記各実施形態では、スラブ型フォトリソニック結晶7をSiO₂と空気との2種類の媒質の周期構造により構成していたが、円孔72内をSiO₂とは屈折率の異なる誘電体材料により充実して当該誘電体材料と

SiO_2 とでスラブ型フォトリック結晶 7 を形成するようにしてもよいし、あるいは 3 種類以上の媒質の周期構造としてもよく、例えば、 SiO_2 からなるスラブ 7 1 に設けた円孔 7 2 の内周面を被覆する Si_3N_4 膜を形成することによって SiO_2 と Si_3N_4 と空気との 3 種類でスラブ型フォトリック結晶 7 を構成するようにしてもよい。

【0038】

また、上記各実施形態では、スラブ型フォトリック結晶 7 を光電変換部 6 の受光面に積層してあるが、スラブ型フォトリック結晶 7 を光電変換部 6 に積層する代わりに、光電変換部 6 内における受光面側に形成するようにしてもよい。また、上記各実施形態では、光電変換部 6 が p 形領域 6 1 と n 形領域 6 3 との間にドリフト領域 6 2 として i 層が設けられた p i n フォトダイオードのフォトダイオード構造を有しているが、光電変換部 6 は p 10
形領域 6 1 と n 形領域 6 3 との間にドリフト領域が設けられていればアバランシェフォトダイオードのフォトダイオード構造でもよい。

【0039】

また、上記各実施形態におけるスラブ型フォトリック結晶 7 は、スラブ 7 1 に対して、単位格子が正三角形の仮想的な 2 次元三角格子の各格子点に対応する各部位に円孔 7 2 を形成することにより形成されているが、単位格子は正三角形に限らず、例えば正方形でもよく、この場合には単位格子が正方形の仮想的な 2 次元正方格子の各格子点に対応する部位に円孔 7 2 を形成すればよい。また、上記各実施形態では、スラブ型フォトリック結晶 7 の屈折率周期構造を形成するためにスラブ 7 1 に多数の円孔 7 2 を形成してあるが、円孔 7 2 を設ける代わりに、例えば三角形の孔や四角形の孔など別の開口形状の孔を設けてもよい。 20

【図面の簡単な説明】

【0040】

【図 1】実施形態 1 を示し、(a) は概略平面図、(b) は (a) の A-A' で破断した概略斜視図、(c) は水平断面図である。

【図 2】実施形態 2 を示し、(a) は概略平面図、(b) は (a) の A-A' で破断した概略斜視図、(c) は水平断面図、(d) は他の水平断面図である。

【図 3】実施形態 3 を示し、(a) は概略平面図、(b) は (a) の A-A' で破断した概略斜視図、(c) は水平断面図である。

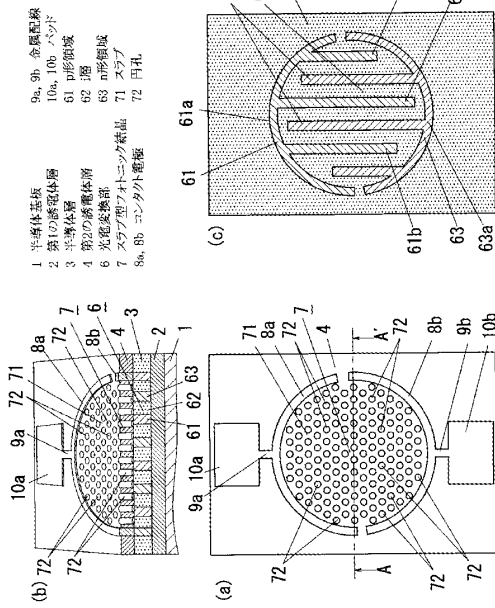
【図 4】従来例を示す概略断面図である。 30

【符号の説明】

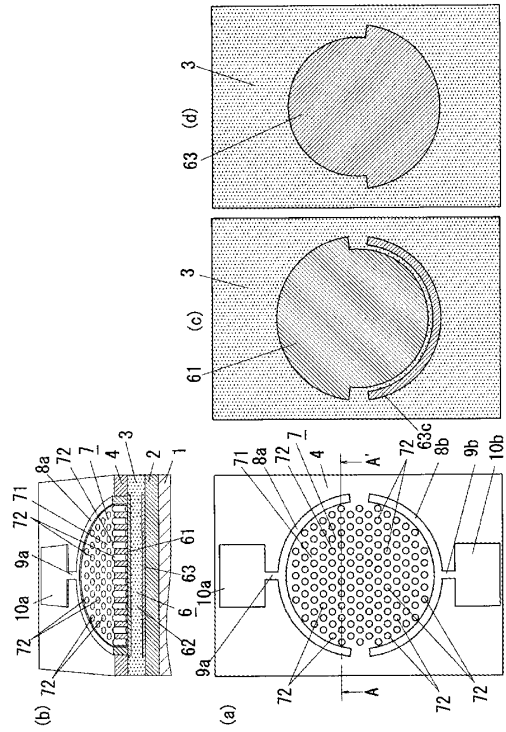
【0041】

- 1 半導体基板
- 2 第 1 の誘電体層
- 3 半導体層
- 4 第 2 の誘電体層
- 6 光電変換部
- 7 スラブ型フォトリック結晶
- 8 a, 8 b コンタクト電極
- 9 a, 9 b 金属配線
- 10 a, 10 b パッド
- 6 1 p 形領域
- 6 2 i 層
- 6 3 n 形領域
- 7 1 スラブ
- 7 2 円孔

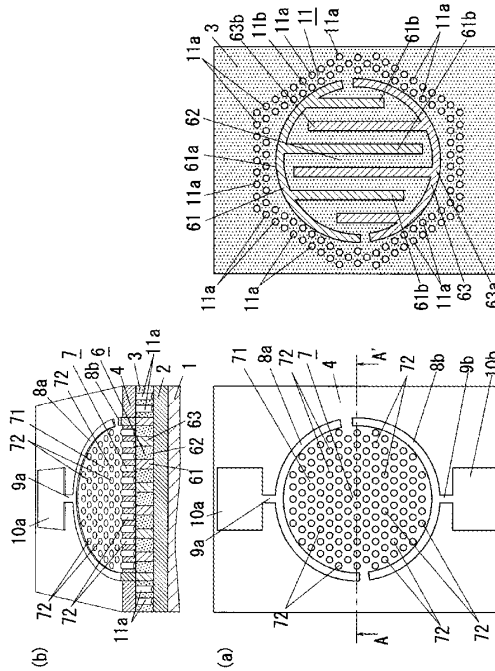
【図 1】



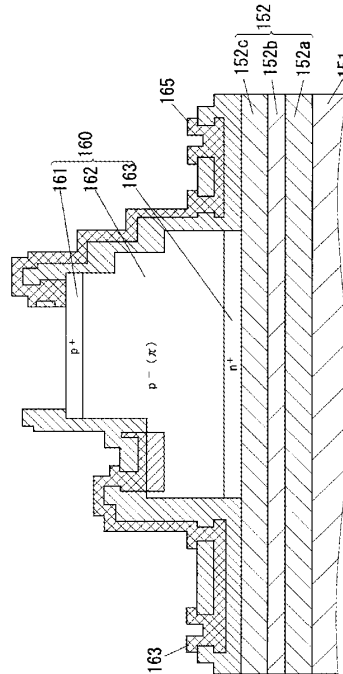
【図 2】



【図 3】



【図 4】



Lateral semiconductor photodetector of pin structure

Abstract

PROBLEM TO BE SOLVED: To provide a PIN structure lateral semiconductor photodetector which is improved in sensitivity for detecting light without deteriorating its response speed. **SOLUTION:** A lateral semiconductor photodetector of PIN structure has interfaces at an I layer 15, a P layer 5, and an N layer, the interfaces are set vertical to the surface of a semiconductor substrate, light impinging on the I layer 15 is converted into a current, and the current is detected. A hole 4 is bored in a light receiving region 2 from a light receiving surface 3 to a certain point as deep as prescribed inside the I layer 15

JP2002314116A

Japan

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Other languages: Japanese

Inventor: Atsushi Harada, 髙 原 田, Tsugio Ide, 次 男 井 田, Shojiro Kitamura, 喜 二 郎 北 村

Current Assignee : Seiko Epson Corp

Worldwide applications

2001 [JP](#)

Application JP2001110168A events ⓘ

2001-04-09 Application filed by Seiko Epson Corp

2001-04-09 Priority to JP2001110168A

2002-10-25 Publication of JP2002314116A

Status Withdrawn

Info: Cited by (7), Legal events, Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Claims (1)

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translated from Japanese

[Claims] 1. A lateral semiconductor light receiving device wherein an interface between an i-layer, a p-layer, and an n-layer having a PIN structure is formed perpendicular to a surface of a semiconductor substrate, and converts light incident on the i-layer into current and detects the current. A lateral semiconductor light-receiving element having a PIN structure, wherein a hole extending from the light-receiving surface to a predetermined depth of the i-layer is provided in the light-receiving region.

Description

translated from Japanese

DETAILED DESCRIPTION OF THE INVENTION

[0001]

The present invention relates to a lateral semiconductor light receiving device having a PIN structure.

[0002]

2. Description of the Related Art In a vertical photodiode in which a pn junction surface is formed parallel to a semiconductor substrate surface, light is incident on a depletion layer through a p-layer or an n-layer.
In a lateral photodiode in which the n-junction surface is formed perpendicular to the semiconductor substrate surface, light is directly incident on the depletion layer (not through the p-layer or the n-layer). For this reason, lateral photodiodes are better than vertical photodiodes.
This is advantageous in light receiving efficiency.

Conventionally, in a photodiode,

An i-layer (intrinsic layer) is provided between a p-layer and an n-layer to increase the thickness of a depletion layer. In a vertical photodiode having such a PIN structure, the i-layer is formed to have a thickness equal to or more than the absorption length in order to increase the light receiving sensitivity. As a result, a quantum efficiency of 70% or more can be obtained at a wavelength of about 700 nm to 870 nm.

Lateral photodiode having a PIN structure (a photodiode in which an interface between an i-layer, a p-layer, and an n-layer having a PIN structure is formed perpendicular to a semiconductor substrate surface)

For example, after a region having an extremely low impurity concentration forming an i-layer is provided in a surface layer portion of a semiconductor substrate, a p-type impurity and an n-type impurity are added to respective positions of this region at predetermined intervals from an upper surface. To form a p-layer and an n-layer, and leave an i-layer between both layers

Therefore, in the case of a lateral photodiode having a PIN structure, the thickness of the i-layer (depth from the light incident surface) in order to increase p, it is necessary to form the p-layer and the n-layer deeply. In order to form the p-layer and the n-layer deep while keeping the width of the i-layer (the distance between the p-layer and the n-layer) uniform in the thickness direction of the substrate, the p-layer and the n-layer on the substrate surface must be 1) is

necessary to increase the distance. When the distance between the p-layer and the n-layer on the substrate surface is increased, the width of the i-layer increases. If the width of the i-layer is large, the movement distance of electrons generated on the p-layer side of the i-layer to reach the electrode of the n-layer increases, and the response speed decreases.

Therefore, in the lateral type photodiode having the PIN structure, as a method for increasing the light receiving sensitivity, simply increasing the thickness of the i-layer (the depth from the light incident surface) cannot be simply employed. Therefore, PIN

As a method for increasing the light receiving sensitivity of the lateral type photodiode having the structure, it is effective to provide an antireflection film on the upper surface of the i-layer to increase the efficiency of incidence on the i-layer.

[0007]

However, a lateral type photodiode having a PIN structure having an antireflection film on the upper surface of the i-layer has a problem that the response speed is low when an element for receiving a high-speed signal is used. There is. SUMMARY OF THE INVENTION The present invention has been made in view of such a problem of the related art, and it is an object of the present invention to improve the light receiving sensitivity without lowering the response speed in a lateral semiconductor light receiving element having a PIN structure.

[0008]

In order to solve the above-mentioned problems, the present invention provides a semiconductor device having an i-layer having a PIN structure in which an interface between a p-layer and an n-layer is formed perpendicular to a semiconductor substrate surface. In a lateral type semiconductor light receiving element for detecting incident light by converting the light into a current, a hole extending from the light receiving surface to a predetermined depth of the i-layer (a position shallower than the depths of the p-layer and the n-layer) is provided in the light receiving region. A lateral type semiconductor light receiving element having a PIN structure is provided.

[0009]

Embodiments of the present invention will be described below. FIG. 1 is a sectional view showing a photodiode corresponding to one embodiment of the present invention. FIG. 2 is a diagram showing an example of a planar shape when the photodiodes of this embodiment are formed in an array. FIG. 1 corresponds to a sectional view taken along line AA of FIG.

This photodiode is a lateral photodiode (semiconductor light receiving element) having a PIN structure formed perpendicular to the substrate surface of a silicon substrate (semiconductor substrate) 1 and has a light receiving region (p-layer of i-layer 15). A hole 4 extending in a direction perpendicular to the surface of the silicon substrate 1 from the light receiving surface 3 to a predetermined depth of the i-layer 15 is provided in a region (a region between the n-layer 5 and the n-layer 7).

On the upper surfaces of the p-layer 5 and the n-layer 7, a p-electrode 6 and an n-electrode 8 are formed. On the lower surface of the silicon substrate 1, a p-electrode 11 is formed. An element protection layer 9 made of a silicon oxide film or the like is provided on the upper surface of the silicon substrate 1 except for the positions of the electrodes 6 and 8 and the hole 4. is formed with a predetermined thickness. This photodiode can be manufactured, for example, by the following method.

First, n is added to the surface layer of the p-type silicon substrate 1.

A well (a region having an extremely low impurity concentration) 10 is provided.

Next, a p-type impurity is added to one of the two regions of the n-well 10 at a predetermined interval, and an n-type impurity is added to the other, and diffused. As a result, the p-layer 5 and the n-layer 7 are formed in the n-well 10, and the portion between the p-layer 5 and the n-layer 7 of the n-well 10 remains as the i-layer 15. Next, after forming the electrodes 6 and 8 on the p-layer 5 and the n-layer 7, the element protection layer 9 is formed.

Next, a focused ion beam processing apparatus (F)

Using B), a portion of the upper surface of the silicon substrate 1 sandwiched between the electrodes 6 and 8 is irradiated with an ion beam, and the element protection layers 9 and 1 are irradiated.

By etching the layer 15, a hole 4 extending in the thickness direction of the silicon substrate 1 from the light receiving surface 3 to a predetermined depth of the i-layer 15 (a position shallower than the depths of the p-layer 5 and the n-layer 7) is formed.

Here, the dimension of the hole 4 in the direction between the p-layer 5 and the n-layer 7 is determined between the hole 4 and the p-layer 5 and between the hole 4 and the n-layer 7. is set to the dimension where exists. When the light receiving surface 3 between each pair of electrodes is large, it is preferable to provide a plurality of holes 4 in the light receiving surface 3 as shown in FIG. in this case, for example, the width W of the electrodes 6 and 8 is 1 μ m, the interval W2 between the electrodes 6 and 8 is 2 to 4 μ m, and the hole 4 is 2 to 4 μ m, and the diameter of the hole 4 is 1 μ m.

In this photodiode, a power supply is connected between the n-electrode 8 in contact with the upper surface of the n-layer 7 and the p-electrode 11 on the lower surface of the substrate 1 with the n-layer 7 side being positive and a reverse bias voltage applied. Then, by connecting the n-electrode 6 in contact with the upper surface of the p-layer 5 to the output circuit, light incident on the i-layer 15 from the light receiving surface 3 can be converted into a current and detected. Also,

In this photodiode, the light (partially shown by a two-dot chain line in FIG. 1) that has entered the hole 4 from the light receiving surface 3 directly enters the light receiving region 2 from the bottom or side surface of the hole 4 and By being reflected on the side surface, the light is incident on the light receiving region 2 from the bottom surface to the side surface, or is incident on the light receiving region 2 from the side surface toward the opposing side surface. Therefore, the light receiving efficiency in the light receiving region 2 is higher than in the case where there is no hole 4.

If the light receiving surface 3 is simply enlarged without providing the hole 4 in order to increase the light receiving area, it takes a long time for electrons generated on the p-layer side of the i-layer to reach the electrode of the n-layer. As the parasitic capacitance increases, the response speed decreases. In contrast, in this photodiode, by providing the hole 4, the light receiving area is larger by the side surface of the hole 4 than when no hole 4 is provided. Therefore, in this photodiode, electrons generated on the p-layer side of the i-layer are n

The movement time until reaching the electrode of the layer is not longer than when the light receiving surface 3 is the same size and the hole 4 is not provided.

The parasitic capacitance of the photodiode is smaller than that in the case where the light receiving surface 3 has the same size and the hole 4 is not provided. For these reasons, according to this photodiode, the light receiving area can be increased and the light receiving efficiency can be increased without reducing the response speed

Further, since the photodiode has the hole 4, the intensity of the electric field applied to the peripheral portion of the hole 4 of the i-layer 15 is locally increased. This allows

Since holes and electrons generated by absorbing light in the peripheral portion of the hole 4 of the i-layer 15 can move at high speed through the i-layer 15,

The response speed is faster than the case without the hole 4. Therefore, according to this photodiode, by providing the hole 4, the light receiving efficiency in the light receiving region 2 is increased, the light receiving sensitivity is improved, and the response speed is also increased.

in this embodiment, a lateral type photodiode having a PIN structure is described. However, the lateral type semiconductor light receiving element having a PIN structure of the present invention is not limited to this. It is also applied to the lateral type phototransistor and the like.

[0019]

As described above, according to the lateral semiconductor light receiving device having the PIN structure of the present invention, the light receiving sensitivity can be improved without lowering the response speed.

[Brief description of the drawings]

FIG. 1 is a cross-sectional view showing a photodiode corresponding to an embodiment of the present invention, and is a view corresponding to a cross-sectional view taken along line AA of FIG.

FIG. 2 is a diagram showing an example of a planar shape when the photodiodes of FIG. 1 are formed in an array.

[Explanation of symbols]

REFERENCE SIGNS LIST 1 silicon substrate (semiconductor substrate) 10 n-well 11 p-electrode 15 layer 2 light-receiving area 3 light-receiving surface 4 hole 5 p-layer 6 p-electrode 7 n-layer 8 n-electrode 9 element protection layer

----- Continuing on the front page (72) Inventor Shojiro Kitamura 3-3-5 Yamato, Suwayama, Nagano F-term (reference) in Seiko Epson Corporation 5F049 MA04 MB03 NA01 NA03 NA15 PA14 PA20 QA01 QA20 SZ13

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JP2007214495A *	2006-02-10	2007-08-23	Epson Imaging Devices Corp	Light receiving apparatus, electro-optical apparatus, and electronic appliance
JP2009130276A *	2007-11-27	2009-06-11	Hitachi Displays Ltd	Optical sensor device and image display device
US7936648B2	2004-06-23	2011-05-03	Lg Electronics Inc.	Method and apparatus for overwriting data on recording medium and the recording medium
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JP2020537816A *	2017-07-21	2020-12-24	ダブルリュアンドダブルリュセンス デバイシーズ, インコーポレイテッド W&W s e n s D e v i c e s , I n c .	Microstructure improved absorption photosensitizer
Family To Family Citations				

* Cited by examiner, † Cited by third party, ‡ Family to family citation

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JPH10190041A	1998-07-21	Photodiode
JP2020161739A	2020-10-01	Photodetector
JP4951552B2	2012-06-13	Semiconductor photodetection device

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
JP2001110158A	2001-04-09	2001-04-09	Lateral semiconductor photodetector of pin structure

Applications Claiming Priority (1)

Application	Filing date	Title
JP2001110158A	2001-04-09	Lateral semiconductor photodetector of pin structure

Legal Events

Date	Code	Title	Description
2003-07-01	A300	Withdrawal of application because of no request for examination	Free format text: JAPANESE INTERMEDIATE CODE: A300 Effective date: 20030701

Concepts

machine-extracted

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Name	Image	Sections	Count	Query match
 semiconductor		title,claims,abstract,description	22	0.000
 substrate		claims,abstract,description	22	0.000
 sensitivity		abstract,description	7	0.000
 deteriorative		abstract	1	0.000
Show all concepts from the description section				

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【特許請求の範囲】

【請求項 1】 P I N 構造の i 層と p 層および n 層との界面が半導体基板面に対して垂直に形成され、i 層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、
受光領域に、受光面から i 層の所定深さまで延びる穴を設けたことを特徴とする P I N 構造のラテラル型半導体受光素子。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、P I N 構造のラテラル型半導体受光素子に関する。

【0002】

【従来の技術】p n 接合面が半導体基板面に対して平行に形成されている縦型フォトダイオードでは、p 層または n 層を通して空乏層に光が入射されるのに対して、p n 接合面が半導体基板面に対して垂直に形成されているラテラル型フォトダイオードでは、空乏層に直接（p 層や n 層を介さずに）光が入射される。そのため、ラテラル型フォトダイオードは縦型フォトダイオードよりも、受光効率の点で有利である。

【0003】従来より、フォトダイオードにおいては、p 層と n 層との間に i 層（真性層）を設けて、空乏層を厚くすることが行われている。このような P I N 構造を有する縦型フォトダイオードでは、受光感度を高くするために、i 層を吸収長以上の厚さに形成することが行われている。これにより、波長 700 nm～870 nm 前後において、70%以上の量子効率が得られるようになる。

【0004】P I N 構造のラテラル型フォトダイオード（P I N 構造の i 層と p 層および n 層との界面が半導体基板面に対して垂直に形成されたフォトダイオード）は、例えば、i 層をなす不純物濃度の極めて薄い領域を半導体基板の表層部に設けた後、この領域の所定間隔を開けた各位置に、上面から p 型不純物及び n 型不純物をそれぞれ添加して拡散させることにより p 層及び n 層を形成し、両層の間を i 層として残すことによって作製される。

【0005】そのため、P I N 構造のラテラル型フォトダイオードの場合に i 層の厚さ（光入射面からの深さ）を大きくしようとすると、p 層及び n 層を深く形成する必要がある。基板の厚さ方向で i 層の幅（p 層と n 層との距離）を均一に保持しながら、p 層及び n 層を深く形成するためには、基板表面での p 層と n 層との距離を大きくとる必要がある。基板表面での p 層と n 層との距離を大きくすると i 層の幅が大きくなる。i 層の幅が大きいと、i 層の p 層側で生じた電子が n 層の電極に達するまでの移動距離が長くなって、応答速度が遅くなる。

【0006】したがって、P I N 構造のラテラル型フォトダイオードでは、受光感度をより高くする方法とし

て、i 層の厚さ（光入射面からの深さ）を大きくすることを単純に採用することができない。そのため、P I N 構造のラテラル型フォトダイオードの受光感度をより高くする方法としては、i 層の上面に反射防止膜を設けて i 層への入射効率を高くすることが有効である。

【0007】

【発明が解決しようとする課題】しかしながら、i 層の上面に反射防止膜を有する P I N 構造のラテラル型フォトダイオードには、高速の信号を受光する素子とした場合に応答速度が低くなるという問題点がある。本発明は、このような従来技術の問題点に着目してなされたものであり、P I N 構造のラテラル型半導体受光素子において、応答速度を低下させることなく受光感度を向上させることを課題とする。

【0008】

【課題を解決するための手段】上記課題を解決するために、本発明は、P I N 構造の i 層と p 層および n 層との界面が半導体基板面に対して垂直に形成され、i 層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域に、受光面から i 層の所定深さ（p 層および n 層の深さより浅い位置）まで延びる穴を設けたことを特徴とする P I N 構造のラテラル型半導体受光素子を提供する。

【0009】

【発明の実施の形態】以下、本発明の実施形態について説明する。図 1 は本発明の一実施形態に相当するフォトダイオードを示す断面図である。図 2 は、この実施形態のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。図 1 は図 2 の A-A 線断面図に相当する。

【0010】このフォトダイオードは、P I N 構造がシリコン基板（半導体基板）1 の基板面に対して垂直に形成されたラテラル型フォトダイオード（半導体受光素子）であり、受光領域（i 層 15 の p 層 5 と n 層 7 とで挟まれた領域）2 に、受光面 3 から i 層 15 の所定深さまで、シリコン基板 1 面に垂直に延びる穴 4 が設けてある。

【0011】p 層 5 および n 層 7 の上面には、p 電極 6 および n 電極 8 がそれぞれ形成されている。シリコン基板 1 の下面には p 電極 11 が形成されている。また、シリコン基板 1 の上面の両電極 6、8 および穴 4 の位置を除いた部分に、シリコン酸化膜等からなる素子保護層 9 が所定の厚さで形成されている。このフォトダイオードは、例えば以下の方法で作製できる。

【0012】先ず、p 型のシリコン基板 1 の表層部に n ウエル（不純物濃度の極めて薄い領域）10 を設ける。次に、n ウエル 10 の所定間隔を開けた 2 つの領域の一方に p 型不純物を、他方に n 型不純物をそれぞれ添加して拡散させる。これにより、n ウエル 10 に p 層 5 及び n 層 7 が形成され、n ウエル 10 の p 層 5 と n 層 7 との

間の部分がi層15として残る。次に、p層5及びn層7の上に電極6、8を形成した後、素子保護層9を形成する。

【0013】次に、集束イオンビーム加工装置(FIB)を用い、シリコン基板1上面の両電極6、8で挟まれた部分にイオンビームを照射して、素子保護層9とi層15をエッチングすることにより、受光面3からi層15の所定深さ(p層5およびn層7の深さより浅い位置)まで、シリコン基板1の厚さ方向に延びる穴4を開ける。

【0014】ここで、穴4のp層5～n層7間方向の寸法は、穴4とp層5との間および穴4とn層7との間にそれぞれ所定厚さのi層15が存在する寸法に設定する。また、各電極対間の受光面3が大きい場合には、図2に示すように、受光面3内に複数の穴4を設けることが好ましい。この場合には、例えば、電極6、8の幅W1を1μm、電極6、8の間隔W2を2～4μm、穴4のピッチKを2～4μm、穴4の直径を1μmとする。

【0015】このフォトダイオードは、n層7の上面に接触するn電極8と基板1の下面のp電極11との間に、n層7側を正として電源を接続して逆バイアス電圧を付与し、p層5の上面に接触するp電極6を出力回路に接続することにより、受光面3からi層15に入射された光を電流に変換して検出することができる。また、このフォトダイオードでは、受光面3から穴4内に入射された光(一部を図1に2点鎖線で表示)は、穴4の底面や側面から受光領域2に直接入射するとともに、底面や側面で反射されることで、底面から側面に向かって受光領域2に入射されたり、側面から対向する側面に向かって受光領域2に入射されたりする。そのため、穴4が無い場合よりも受光領域2での受光効率が高くなる。

【0016】受光面積を大きくするために穴4を設けず単純に受光面3を大きくした場合には、i層のp層側で生じた電子がn層の電極に達するまでの移動時間が長くなるとともに、寄生容量が大きくなるため、応答速度が遅くなる。これに対して、このフォトダイオードでは、穴4を設けることで、穴4が無い場合よりも穴4の側面の分だけ受光面積が大きくなっている。そのため、このフォトダイオードでは、i層のp層側で生じた電子がn層の電極に達するまでの移動時間が、受光面3が同じ大

同じ大きさで穴4を設けない場合よりも小さくなる。これらのことから、このフォトダイオードによれば、応答速度を遅くすることなく、受光面積を大きくして受光効率を高くすることができる。

【0017】さらに、このフォトダイオードは、穴4を有することによって、i層15の穴4の周囲部分に掛かる電界強度が局所的に大きくなっている。これにより、i層15の穴4の周囲部分で光を吸収して発生した正孔と電子はi層15を高速で移動することができるため、穴4の無い場合と比較して応答速度が速くなる。したがって、このフォトダイオードによれば、穴4を設けることによって、受光領域2での受光効率が高くなって受光感度が向上するとともに、応答速度も高くなる。

【0018】なお、この実施形態では、PIN構造のラテラル型フォトダイオードについて説明しているが、本発明のPIN構造のラテラル型半導体受光素子はこれに限定されず、ベースとコレクタの部分がPIN構造になっているラテラル型フォトランジスタ等にも適用される。

20 【0019】

【発明の効果】以上説明したように、本発明のPIN構造のラテラル型半導体受光素子によれば、応答速度を低下させることなく受光感度を向上させることができる。

【図面の簡単な説明】

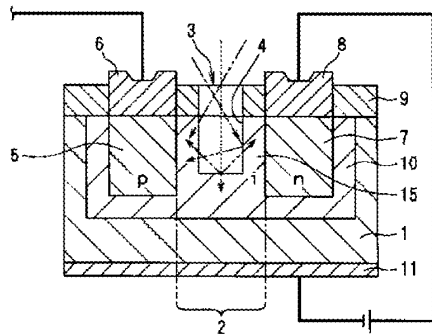
【図1】本発明の一実施形態に相当するフォトダイオードを示す断面図であって、図2のA-A線断面図に相当する図である。

【図2】図1のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。

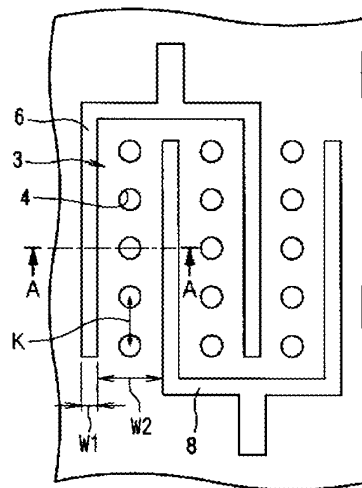
30 【符号の説明】

- 1 シリコン基板(半導体基板)
- 10 nウエル
- 11 p電極
- 15 i層
- 2 受光領域
- 3 受光面
- 4 穴
- 5 p層
- 6 p電極
- 7 n層
- 8 n電極
- 9 素子保護層

【図1】



【図2】



フロントページの続き

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Fターム(参考) 5F049 MA04 MB03 NA01 NA03 NA15
PA14 PA20 QA01 QA20 SZ13

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		
<small>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</small>			

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☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Shih-Yuan		WANG		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
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City	Palo Alto	State/Province	CA		
Postal Code	94306	Country	US		
Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
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Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Los Altos	State/Province	CA	Country of Residence	US
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City	Los Altos	State/Province	CA		
Postal Code	90422	Country	US		
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For further information see 37 CFR 1.33(a).

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

☐ An Address is being provided for the correspondence information of this application.			
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Email Address		<input type="button" value="Add Email"/>	<input type="button" value="Remove Email"/>

Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		
Attorney Docket Number	309-0015USCIPDIV	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	48	Suggested Figure for Publication (if any)	5B

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)	
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
	Division of	18385213	2023-10-30		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18385213	Continuation in part of	17974325	2022-10-26	11830954	2023-11-28
Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
18385213	Continuation in part of	18113474	2023-02-23		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113474	Division of	17707429	2022-03-29	11621360	2023-04-04
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17707429	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113474	Continuation in part of	17707429	2022-03-29	11621360	2023-04-04

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0015USCIPDIV	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17707429	Division of	17532832	2021-11-22	11309444	2022-04-19
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17532832	Continuation in part of	17182954	2021-02-03	11791432	2023-10-17
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Continuation in part of	PCTUS1667977	2016-12-21		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16042535	2018-07-23	10700225	2020-06-30
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16296985	2019-03-08	10468543	2019-10-16
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113474	Division of	177077429	2022-03-29	11621360	2023-04-04
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
177077429	Division of	17532831	2021-11-22	11309444	2022-04-19
Prior Application Status		Patented		Remove	
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17532831	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17
Prior Application Status		Patented		Remove	
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17182954	Division of	16528958	2019-08-01	11121271	2021-09-14

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0015USCIPDIV	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	14947718	2015-11-20	10622498	2020-03-25
Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958		Continuation in part of		PCTUS1667977	2016-12-21
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-20	10446700	2019-09-25
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16042535	2018-07-23	10700225	2020-06-30
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16296985	2019-03-08	10468543	2019-10-16
Prior Application Status		Abandoned		Remove	
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958		Continuation in part of		PCTUS1843289	2018-07-23
Prior Application Status		Abandoned		Remove	
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958		Continuation in part of		PCTUS1857963	2018-10-29
Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958		Claims benefit of provisional		62713455	2018-08-01
Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958		Claims benefit of provisional		62716310	2018-08-08

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		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62717750	2018-08-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62719689	2018-08-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62724449	2018-08-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62733476	2018-09-19
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/737062	2018-09-26
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/750016	2018-10-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/770656	2018-09-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/772498	2018-09-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/777157	2018-12-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/779693	2018-12-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/784342	2018-12-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/794330	2019-01-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/797141	2019-01-25

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/797263	2019-01-26
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/800371	2019-02-01
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/802171	2019-02-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/802718	2019-02-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/805850	2019-02-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/808949	2019-02-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/819604	2019-03-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/819669	2019-03-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/820695	2019-03-19

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		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/828976	2019-04-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/841798	2019-05-01
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/843206	2019-05-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/846554	2019-05-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/853280	2019-05-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/860115	2019-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/863231	2019-06-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/863852	2019-06-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/867186	2019-06-26

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		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/868911	2019-06-29		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/870533	2019-07-03		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/873891	2019-07-13		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/874418	2019-07-15		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
PCT/US18/57963	Continuation of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/797821	Continuation in part of	14/947718	2015-11-20	10622498	2020-03-25
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/797821	Continuation in part of	15/309922	2016-11-09	9818893	2017-10-25
Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
15/797821	Continuation in part of	PCT/US16/67977	2016-12-21		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
15/797821	Claims benefit of provisional	62/465734	2017-03-01		

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/474179	2017-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/484474	2017-04-12
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/487606	2017-04-20
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/488998	2017-04-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/500581	2017-05-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/505974	2017-05-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/509093	2017-05-20
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/510249	2017-05-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/514889	2017-06-04

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/521504	2017-06-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/522169	2017-06-20
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/527962	2017-06-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/530281	2017-07-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/533078	2017-07-16
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/533603	2017-07-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/542243	2017-08-07

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/547728	2017-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/542243	2017-08-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639472	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/628764	2018-02-09

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/643010	2018-03-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/640522	2018-03-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/599246	2017-12-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/645810	2018-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/666005	2018-05-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/607860	2017-12-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/631630	2018-02-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/677609	2018-05-29

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/634692	2018-02-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/652830	2018-04-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/591072	2017-09-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639356	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/615314	2018-01-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/623971	2018-01-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/637945	2018-03-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/651053	2018-03-30

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/682909	2018-06-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/659072	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/659067	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/669194	2018-05-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/675130	2018-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/547728	2017-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/651087	2018-03-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/646871	2018-03-22

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Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/662217	2018-04-24		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/639920	2018-03-07		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/633514	2018-02-21		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/296985	Continuation of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/042535	Continuation in part of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/535801	2017-07-21		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/540524	2017-08-02		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/542243	2017-08-07		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/547728	2017-08-18		

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/591072	2017-11-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/599246	2017-12-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/607860	2017-12-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/615314	2018-01-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/623971	2018-01-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/628764	2018-02-09

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		Application Number	
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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/631630	2018-02-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/633514	2018-02-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/634692	2018-02-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/637945	2018-03-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639356	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639472	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639920	2018-03-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/640522	2018-03-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/643010	2018-03-14

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		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/645810	2018-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/646871	2018-03-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/651053	2018-03-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/651087	2018-03-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/652830	2018-04-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/659067	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/659072	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/662217	2018-04-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/666005	2018-05-02

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/669194	2018-05-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/675130	2018-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/677609	2018-05-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/682909	2018-06-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/270577	2015-12-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/304907	2016-03-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/290391	2016-02-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/334934	2016-05-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/338263	2016-05-18

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/346850	2016-06-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/359349	2017-07-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/366188	2016-07-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/368109	2016-07-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/374828	2016-08-13
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/376869	2016-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/380364	2016-08-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/383391	2016-09-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/383479	2016-09-04

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Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/394222	2016-09-14		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/398607	2016-09-23		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/401126	2016-09-28		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/406999	2016-10-12		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/414671	2016-10-29		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/415339	2016-10-31		
Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
15/309922	a 371 of international	PCT/US15/61120	2015-11-17		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/309922	Continuation of	14/943898	2015-11-17	9530905	2016-12-27
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/309922	Continuation of	14/945003	2015-11-18	9525084	2016-12-20

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/213558	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/199607	2015-07-13
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/175855	2015-06-15

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/090879	2014-12-11

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/182602	2015-06-21

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/100025	2015-01-05

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/188876	2015-07-06

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/111582	2015-02-03

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/947718	Continuation of	PCT/US14/39208	2014-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/826446	2013-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/843021	2013-07-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/905109	2013-11-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/834873	2013-06-13
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/892821	a 371 of international	PCT/US14/39208	2014-05-22

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/826446	2013-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/843021	2013-07-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/905109	2013-11-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/834873	2013-06-13
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

<p>This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.</p> <p>☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.</p>
--

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h) (1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1			
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
<input type="button" value="Clear"/>			
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor: <input type="text"/>			
If the Applicant is an Organization check here. ☒			
Organization Name	W&W Sens Devices, Inc.		
Mailing Address Information For Applicant:			
Address 1		38 Third Street, Suite 307	
Address 2			
City	Los Altos	State/Province	CA
Country	US	Postal Code	94022
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is <u>not</u> checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).					
This Application Data Sheet must be signed by a patent practitioner if one or more of the applicants is a juristic entity (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, all joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of all joint inventor-applicants.					
See 37 CFR 1.4(d) for the manner of making signatures and certifications.					
Signature	/Ivan S. Kavrukov/		Date (YYYY-MM-DD)	2024-09-03	
First Name	Ivan S.	Last Name	Kavrukov	Registration Number	25,161
Additional Signature may be generated within this form by selecting the Add button.					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

NOTIFICATION OF TRANSMITTAL OF
THE INTERNATIONAL SEARCH REPORT AND
THE WRITTEN OPINION OF THE INTERNATIONAL
SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

To: IVAN S. KAVRUKOV COOPER & DUNHAM LLP 30 ROCKEFELLER PLAZA NEW YORK, NY 10112	Date of mailing <i>(day/month/year)</i> 17 DEC 2020
Applicant's or agent's file reference 5176/91538-PCT	FOR FURTHER ACTION See paragraphs 1 and 4 below
International application No. PCT/US 20/51733	International filing date <i>(day/month/year)</i> 21 September 2020 (21.09.2020)
Applicant W&WSENS DEVICES INC.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:
 The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46).
When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.
How? Directly to the International Bureau preferably through ePCT, or on paper to:
 The International Bureau of WIPO, 34, chemin des Colombettes, 1211 Geneva 20, Switzerland

For more detailed instructions, see the *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ With regard to any protest against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

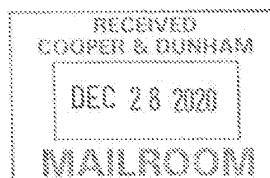
Shortly after the expiration of 18 months from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within 19 months from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until 30 months from the priority date (in some Offices even later); otherwise, the applicant must, within 20 months from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices. In respect of other designated Offices, the time limit of 30 months (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Within 22 months from the priority date, the applicant may request that a supplementary international search be carried out by a different International Searching Authority that offers this service (Rule 45bis.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1460, Alexandria, Virginia 22313-1460 Facsimile No. 571-273-8300	Authorized officer <p style="text-align: center; margin-top: 20px;">Lee Young</p> Telephone No. PCT Helpdesk: 571-272-4300
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Form PCT/ISA/220 (revised January 2020)



PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 5176/91538-PCT		FOR FURTHER ACTION see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 20/51733	International filing date (day/month/year) 21 September 2020 (21.09.2020)	(Earliest) Priority Date (day/month/year) 24 September 2019 (24.09.2019)
Applicant W&WSENS DEVICES INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

a. With regard to the language, the international search was carried out on the basis of:

- ☒ the international application in the language in which it was filed.
☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91 (Rule 43 *bis*(a)).

c. ☐ With regard to any nucleotide and/or amino acid sequence disclosed in the international application, see Box No. I.

2. ☐ Certain claims were found unsearchable (see Box No. II).

3. ☐ Unity of invention is lacking (see Box No. III).

4. With regard to the title,

- ☒ the text is approved as submitted by the applicant.
☐ the text has been established by this Authority to read as follows:

5. With regard to the abstract,

- ☒ the text is approved as submitted by the applicant.
☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the drawings,

- a. the figure of the drawings to be published with the abstract is Figure No. 59
☒ as suggested by the applicant.
☐ as selected by this Authority, because the applicant failed to suggest a figure.
☐ as selected by this Authority, because this figure better characterizes the invention.
- b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2019)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 20/51733

A. CLASSIFICATION OF SUBJECT MATTER

IPC - H01L 27/146, 31/101, 31/102 (2020.01)

CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y --- A	US 2018/0102442 A1 (W&WSENS, DEVICES INC.) 12 April 2018 (12.04.2018) entire document; especially Fig. 8; Fig. 45; para [0038], para [0203]-[0248], para [0333]-[0336], para [0489]	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41
Y --- A	US 2011/0156195 A1 (TIVARUS et al.) 30 June 2011 (30.06.2011) entire document; especially Fig. 13; para [0001], [0032], [0062]	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41
Y --- A	US 2012/0153127 A1 (HIRIGOYEN et al.) 21 June 2012 (21.06.2012) entire document; especially Fig. 4; para [0052], [0057]	3-5, 12, 17-19, 21, 33, 36, 38, 42
Y --- A	US 2018/0012918 A1 (ARTILUX CORPORATION) 11 January 2018 (11.01.2018) entire document; especially para [0059]	10
Y --- A	US 2019/0156317 A1 (BRILLNICS, INC) 30 May 2019 (30.05.2019) entire document; especially para [0010]-[0012]	17
Y --- A	US 2012/0012741 A1 (VASILYEV) 19 January 2012 (19.01.2012) entire document; especially Fig. 10-11; para [0084], [0089]	32
		3-4, 33
		3, 5, 12

☐ Further documents are listed in the continuation of Box C☐ See patent family annex.

* Special categories of cited documents.

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

15 November 2020

Date of mailing of the international search report

17 DEC 2020

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-8300

Authorized officer

Lee Young

Telephone No. PCT Helpdesk: 571-272-4300

Form PCT/ISA/210 (second sheet) (July 2019)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

To: IVAN S. KAVRUKOV
COOPER & DUNHAM LLP
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

Date of mailing
(day/month/year)

17 DEC 2020

Applicant's or agent's file reference
5176/91538-PCT

FOR FURTHER ACTION

See paragraph 2 below

International application No.
PCT/US 20/51733

International filing date (day/month/year)
21 September 2020 (21.09.2020)

Priority date (day/month/year)
24 September 2019 (24.09.2019)

International Patent Classification (IPC) or both national classification and IPC

IPC - H01L 27/146, 31/101, 31/102 (2020.01)

CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102

Applicant

W&WSENS DEVICES INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/229.

Name and mailing address of the ISA/IJS
Mail Stop PCT, Attn: ISA/US
Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-8300

Date of completion of this opinion

15 November 2020

Authorized officer

Lee Young

PCT Help Desk

Telephone No. 571-272-4300

Form PCT/ISA/237 (cover sheet) (revised January 2019)

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
 - ☒ the international application in the language in which it was filed.
 - ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b)).
3. ☐ With regard to **any nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:
 - a. ☐ forming part of the international application as filed:
 - ☐ in the form of an Annex C/ST.25 text file.
 - ☐ on paper or in the form of an image file.
 - b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
 - c. ☐ furnished subsequent to the international filing date for the purposes of international search only:
 - ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
 - ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).
4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
5. Additional comments:

Form PCT/ISA/237 (Box No. I) (revised January 2019)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US 20/51733

Box No. V	Reasoned statement under Rule 43bis.1(s)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement		
1. Statement			
Novelty (N)	Claims	1-42	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	3-5, 12, 17-19, 21, 33, 36, 38, 42	YES
	Claims	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41	NO
Industrial applicability (IA)	Claims	1-42	YES
	Claims	NONE	NO
2. Citations and explanations:			
<p>Claims 1, 2, 6-9, 11, 13-16, 20, 22-31, 34, 35, 37, and 39-41 lack an inventive step under PCT Article 33(3) as being obvious over US 2018/0102442 A1 to W&Wsens, Devices Inc. (hereinafter "Wsens") in view of US 2011/0156195 A1 to Tivarus et al. (hereinafter "Tivarus").</p> <p>Regarding claim 1, Wsens discloses a photosensor wafer of crystalline Si and a CMOS Logic Processor (CLP) wafer stacked on each other for electrical interaction and forming a structure (Fig. 8; para [0038]- an integrated combination of a microstructure-enhanced photodetector (MSPD) and an active electronic circuit; para [0203]- Silicon chip 500 can any combination of the following devices: MSPDs; MSAPDs; vertical cavity surface emitting lasers (VCSEL) that are either wafer bonded to the chip and/or have a precision cavity for dropping the VCSEL into as in a silicon platform; CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers; Fig. 45 shows cmos layer and MSPC layer stacked on each other; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration; para [0489]- the microstructure holes can be very complex, as for example in Berenschoot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon) comprising: an array of laterally spaced pixels formed in said photosensor wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics); wherein said pixels comprise photosensors each including one or more microstructure holes (4412) extending into said photosensor wafer (Fig. 45 shows holes 4412 extending into the said photo wafer (Si and/or GeSi layer); para [0333]- microstructure holes 4412; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further including plural N-doped and/or P-doped regions (4482, 4484) of the photosensor wafer configured to interact with light photons impinging on said pixels, including on said holes (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N...Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.); one or more active CMOS circuits formed in said CLP wafer (Fig. 45; para [0036], [0248], [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration...reinforcement of the MSPD/MSAPD structure and CMOS/BiCMOS IC electronics); and electrical interconnects between said pixels and said one or more active CMOS circuits, wherein said interconnects are configured to convey electrical signals between said pixels and said one or more active CMOS circuits (Fig. 21; para [0246]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power.); Wsens fails to disclose respective lenses over said pixels; light photons impinging on said pixels through said lenses; wherein said CLP wafer is at a side of said photosensor wafer that is opposite said lenses.</p> <p>Tivarus, drawn to a stacked CMOS sensor, discloses respective lenses (1304) over pixels (1204, 1206); light photons impinging on said pixels through said lenses; wherein CLP wafer (1306) is at a side of said photosensor wafer (1300) that is opposite said lenses (1304) (Fig. 13 shows the wafer 1306 is at a side of said photosensor wafer 1300 that is opposite the lenses 1304; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0032]- light 302 from a subject scene is input to an imaging stage 304. Imaging stage 304 can include conventional elements such as a lens; para [0082]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1215, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306;). It would have been obvious to a person having ordinary skill in the art to combine the lenses and the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0001]-[0006]).</p>			
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Form PCT/ISA/237 (Box No. V) (revised January 2019)

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
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Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made.

Claims 27 and 35 lack antecedent basis for terms "said lenses". For purposes of this search, claims 27 and 35 are interpreted as depending from claim 26.

Claim 42 depends on claim 3408 which is not exist. For purposes of this search, claim 42 is interpreted as depending on claim 40.

Form PCT/ISA/237 (Box No. VIII) (revised January 2019)

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Supplemental Box

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Box V.2 - Citations and Explanations:

Regarding claim 2, Weens in view of Tivarus disclose the structure of claim 1. Tivarus further discloses including respective color filters between said lenses and pixels configured to select respective wavelength ranges (Fig. 13 shows color filters 1302 between lenses 1304 and photodetectors 1202, 1204, 1208, 1208; para [0247]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300.).

Regarding claim 6, Weens in view of Tivarus disclose the structure of claim 1. Weens further discloses in which said at least some of said holes in the photosensor wafer are generally cylindrical (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 7, Weens in view of Tivarus disclose the structure of claim 1. Weens further discloses in which said at least some of said holes in the photosensor wafer are inverted pyramids (Fig. 24; para [0186]- scanning electron micrographs of holes in the shape of inverted pyramids; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 8, Weens in view of Tivarus disclose the structure of claim 1. Weens further discloses in which said at least some of said holes in the photosensor wafer are funnel shaped (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 9, Weens in view of Tivarus disclose the structure of claim 1. Weens further discloses in which said hole of each of at least some of said pixels comprises a cluster of nanoholes (9212) into said photosensor wafer (Fig. 82 shows a cluster of nanoholes 9212, para [0560]- The nano/micro structure holes 9212 can have lateral surface dimensions ranging from 30 nm to 5000 nm or more and spacing between the nano micro structure holes can range from 10 nm to 10000 nm or more. The holes can be shaped as a circle, oval, square, polygon, hourglass, fractal, amoeba, star or a combination of shapes).

Regarding claim 11, Weens in view of Tivarus disclose the structure of claim 1. Weens further discloses including light reflectors under said pixels (Fig. 9B; para [0208]- a via 930 can be etched to remove most or all of the substrate to the etch stop layer which can in addition be patterned with nano-micro structures 914 and/or can be coated with dielectric distributed Bragg reflectors.).

Regarding claim 13, Weens in view of Tivarus disclose the structure of claim 1. Weens further discloses in which at least some of said holes differ in shape from one another (Fig. 24 shows the different shape of holes; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 14, Weens in view of Tivarus disclose the structure of claim 1. Weens further discloses in which each of said pixels comprises laterally spaced doped regions (4294) (Fig. 41-42; para [0319]- after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P+-N to N+-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants; para [0330]).

Regarding claim 15, Weens in view of Tivarus disclose the structure of claim 1. Weens further discloses in which each of said pixels comprises vertically spaced doped regions (4260) (Fig. 41-42; para [0319]- A N+ connecting well 4260 formed by ion implantation and/or diffusion can connect the cathode on the surface to the N+ layer/region 4282 and in the case of an N substrate the cathode can be on the bottom of the substrate with or without additional connect wells.; para [0330]).

Regarding claim 16, Weens in view of Tivarus disclose the structure of claim 1. Weens further discloses in which said pixels include Ge regions in said photosensor wafer, configured to extend a response of said pixels to light in a 2 micrometers wavelength range (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped i Si and/or GeSi layer; para [0344]- Operating wavelength range for Si i layer can range from 750 nm to 1070 nm and for GeSi can range from 750 nm to 1350 nm and in some cases 900 nm to 1350 nm and in some cases 1100 nm to 1350 nm and in some cases 1250 nm to 1550 nm and in some cases 1250 nm to 1650 nm and in some cases to 2000 nm depending on the Ge fraction in the GeSi alloy.).

Regarding claim 20, Weens in view of Tivarus disclose the structure of claim 1. Weens further discloses including doped Si conformally lining at least some of said holes and hyperdoping over said doped Si lining (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped i Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P+-N to N+-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants (it is noted P+ or N+ doping is hyperdoping.)).

Regarding claim 22, Weens in view of Tivarus disclose the structure of claim 1, further including a first layer of electrically insulating material under said pixels (Fig.46 shows BOX layer under the pixel; para [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO2, which is an insulating material.)) and a second layer of an electrically insulating material over said active CMOS circuits (para [0442]- entire monolithically integrated MSPD/AMSPD with CMOS and/or BiCMOS electronics chip can be entirely and/or partially hermetically sealed with dielectrics such as silicon oxide, silicon nitride, aluminum oxide, aluminum nitride, polymers such as polyimide, and/or spin-on-glass.).

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Box V.2 - Citations and Explanations:

Regarding claim 23, Wsens in view of Tivarus disclose the structure of claim 22. Wsens further discloses wherein the first and second layers of electrically insulating material are selected from a group consisting of Si Oxide and Si Nitride (para Fig.46 shows BOX layer under the pixel; para [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO₂, which is an insulating material); [0442]- entire monolithically integrated MSPD/AMSPD with CMOS and/or BiCMOS electronics chip can be entirely and/or partially hermetically sealed with dielectrics such as silicon oxide, silicon nitride, aluminum oxide, aluminum nitride, polymers such as polyimide, and/or spin-on-glass.).

Regarding claim 24, Wsens in view of Tivarus disclose The structure of claim 22. Wsens further discloses wherein one or more additional layers of electrically insulating material are formed on said first and/or second layers of electrically insulating material (Fig. 2A shows a Bragg reflector layer on BOX layer; para [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO₂, which is an insulating material); para [0255]- Starting with a silicon substrate that can have a buried oxide (BOX) layer and/or buried hole layer (SOH silicon on hole), and/or with or without an etch stop layer; para [0256]- In addition a dielectric Bragg reflector; para [0319]).

Regarding claim 25, Wsens discloses a high-speed photodetector array (HSPA) wafer of crystalline Si and a CMOS Logic Processor (CLP) wafer stacked on each other for electrical interaction and forming a structure (Fig.8; para [0186]- FIGS. 1A-1H are top-view scanning electron micrographs of holes in the shape of inverted pyramids used in a microstructure high speed photodiode (MSPD) and/or a high speed microstructure avalanche photodiode (MSAPD); para [0209]- Arrays of MSPD/MSAPD can be monolithically integrated with CMOS/BiCMOS electronics; para [0336]- FIG. 46 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration; para [0489]- the microstructure holes can be very complex, as for example in Berenschoot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon) comprising:
an array of laterally spaced photodetectors formed in said HSPA wafer (Fig. 2G and 2I shows array of laterally spaced pixels (the structures comprise MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 2I is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics); wherein each of said photodetectors includes at least one microstructure hole (4412) extending into said HSPA wafer (Fig. 45 shows holes 4412 extending into the said photo wafer (1 Si and/or GeSi layer); para [0333]- microstructure holes 4412; para [0336]- FIG. 46 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further includes plural N-doped and/or P-doped regions (4482, 4484) of the HSPA wafer configured to interact with light photons impinging on said photodetector from a first side of the HSPA wafer (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N...Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.);
one or more active CMOS circuits formed in said CLP wafer (Fig.45; para [0038], [0336]- FIG. 46 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration...reinforcement of the MSPD/MSAPD structure and CMOS/BiCMOS IC electronics); and
electrical interconnects between said high speed photodetector array and said one or more active CMOS circuits, wherein said interconnects are configured to convey electrical signals between said HSPA and said one or more active CMOS circuits (Fig. 2I; para [0248]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power).
Wsens fails to disclose wherein said CLP wafer is at a side of said HSPA wafer that is opposite said first side.
Tivarus, drawn to a stacked CMOS sensor, discloses CLP wafer (1306) is at a side of a wafer (1300) that is opposite the first side (Fig. 13 shows the wafer 1306 is at a side of the wafer 1300 that is opposite the side with photodetectors; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306). It would have been obvious to a person having ordinary skill in the art to combine the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 26, Wsens in view of Tivarus disclose the structure of claim 25 and the HSPA wafer as discussed above. Tivarus further discloses including an array of lenses (1304) formed over the photodetectors (1204, 1206) on said first side of the wafer (1300) (Fig. 13; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). It would have been obvious to a person having ordinary skill in the art to combine the lenses disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 27, Wsens in view of Tivarus disclose the structure of claim 26. Wsens further discloses plural holes in pixels in said HSPA wafer (Fig. 45 shows plural holes in a single pixel structure; para [0333]- microstructure holes 4412); said photodetectors and said active CMOS circuits are configured to operate at 56 Gb/s or greater data rates that include 112 Gb/s (para [0218]- With thinner 1 layer, 50 Gb/s, 60 Gb/s, 80 Gb/s, 100 Gb/s can be achieved). Tivarus further discloses in which each of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses disclosed in Tivarus overlies the holes of Wsens since they overly the substrate of Tivarus and the substrate of Wsens has holes.

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Box V.2 - Citations and Explanations:

Regarding claim 28, Wsena in view of Tivarus disclose the structure of claim 25. Wsena further discloses in which: at least some of said holes in the HSPA wafer are generally cylindrical (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 29, Wsena in view of Tivarus disclose the structure of claim 25. Wsena further discloses in which at least some of said holes in the HSPA wafer are inverted pyramids (Fig. 24; para [0186]- scanning electron micrographs of holes in the shape of inverted pyramids; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 30, Wsena in view of Tivarus disclose the structure of claim 25. Wsena further discloses in which at least some of said holes in the HSPA wafer are funnel shaped (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 31, Wsena in view of Tivarus disclose the structure of claim 25. Wsena further discloses including an array of optical filters (2014, 2016, 2018) formed at said first side of the HSPA wafer over said photodetectors (Fig. 20; para [0246]- Bandpass filters can also be fabricated on the top surface where the microstructured holes for absorption enhancement are etched; para [0247]- Note that some or all of the MSPDs can also be MSPADs. The MSPDs form an array where each MSPD1, MSPD2, MSPD3, ... MSPDn has a bandpass filter with its own unique bandpass wavelength. Having a different bandpass wavelength for each of the MSPD in the array allows for the selection of specific wavelengths in a CWDM optical signal).

Regarding claim 34, Wsena in view of Tivarus disclose the structure of claim 25. Wsena further discloses in which said photodetectors include Ge regions in said HSPA wafer, configured to enhance a response of said photodetectors to light in a wavelength range that includes 1350 nm and / or in a wavelength range that includes 1550 nm (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped i Si and/or GeSi layer; para [0344]- Operating wavelength range for Si 1 layer can range from 750 nm to 1070 nm and for GeSi can range from 750 nm to 1350 nm and in some cases 900 nm to 1350 nm and in some cases 1100 nm to 1350 nm and in some cases 1250 nm to 1550 nm and in some cases 1250 nm to 1650 nm and in some cases to 2000 nm depending on the Ge fraction in the GeSi alloy).

Regarding claim 35, Wsena in view of Tivarus disclose the structure of claim 26. Wsena further discloses plurality of holes in pixels (Fig. 45 shows plurality of holes in a single pixel structure; para [0333]- microstructure holes 4412). Tivarus further discloses in which at least some of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses overlies the holes since they overlie the substrate and the substrate of Wsena has holes. Wsena further discloses said photodetector array and said CMOS active circuits are configured to operate at data rates of 56 Gb/s or higher (para [0218]- With thinner 1 layer, 50 Gb/s, 60 Gb/s, 80 Gb/s, 100 Gb/s can be achieved.).

Regarding claim 37, Wsena in view of Tivarus disclose the structure of claim 25. Wsena further discloses including doped Si conformally lining said holes and hyperdoping over said doped Si lining the holes (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped i Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants (It is noted P+ or N+ doping is hyperdoping.)).

Regarding claim 39, Wsena in view of Tivarus disclose the structure of claim 25. Wsena further discloses in which said CLP wafer includes clock recovery circuits and transimpedance amplifiers (para [0045]- The additional active electronic circuits can comprise one or more transimpedance amplifiers (TIAs); para [0273]- The CMOS/BiCMOS ASICs can include one or more of the following: TIAs; clock data recovery (CDR) circuitry; equalizers; and limiting amplifiers (LA)), and wherein said HSPA and CLP wafers are configured to operate at aggregated data rates of 400-1000 Gb/s or more (para [0268]- increase the aggregated data rates to greater than 40 Gb/s and in some cases greater than 100 Gb/s and in some cases greater than 1 Tb/s).

Regarding claim 40, Wsena discloses a monolithic wafer of crystalline Si having a first side and a second side (Fig. 38; para [0325]- and/or polycrystalline silicon layers; para [0482]- the microstructure holes can be very complex, as for example in Berenschoet et al. Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon), comprising: an array of laterally spaced photosensor or photodetector pixels formed at said first side of the wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSPAD arrays monolithically integrated with CMOS and/or BiCMOS electronics); wherein each of said pixels includes at least one hole (4412) formed into said first side of the wafer (Fig. 45 shows holes 4412 formed into the said photo wafer (i Si and/or GeSi layer); para [0333]- microstructure holes 4412; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further includes plural N-doped and/or P-doped regions (4482, 4484) of the wafer configured to interact with light photons impinging on said pixels, including on said holes (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4486 that can be implanted with ions such as Ar, Na, Xe, O, and/or N. Also shown are upper ion implanted region 4484; para [0343]- Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSPAD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSPAD.);

CMOS logic processors (para [0038], [0246]- FIG. 21 is a simple schematic diagram showing MSPD/MSPAD arrays monolithically integrated with CMOS and/or BiCMOS electronics); and (claim 40 continued)

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(claim 40 continued) electrical interconnects in said wafer configured to convey electrical signals between said pixels and said one or more active CMOS circuits (Fig. 21; para [0246]). The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BCMOS electronics with a transmission line 2142. The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power). Wsens fails to disclose respective optical lenses over said pixels configured to direct to said pixels and said holes light impinging on said first side of the wafer; CMOS logic processors formed at said second side of the wafer.

Tivarus, drawn to a stacked CMOS sensor, discloses respective optical lenses (1304) over the pixels (1302, 1304) configured to direct to said pixels light impinging on the first side of the wafer (upper side); CMOS logic processors (1306) formed at the second side of the wafer (lower side). (Fig. 13; para [0001])—more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0032]—light 302 from a subject scene is input to an imaging stage 304. Imaging stage 304 can include conventional elements such as a lens; para [0062]—Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]—Circuit wafer 1306; it would have been obvious to a person having ordinary skill in the art to combine the lenses and the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]–[0006]).

Regarding claim 41, Wsens in view of Tivarus disclose the monolithic wafer of claim 40. Wsens further discloses plurality of holes in pixels in the wafer (Fig. 45 shows plurality of holes in a single pixel structure; para [0333]—microstructure holes 4412). Tivarus further discloses in which at least some of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]). A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300. Therefore the lenses disclosed by Tivarus overlies the holes disclosed in Wsens since they overlie the substrate in Tivarus and the substrate of Wsens has holes.

Claim 10 lacks an inventive step under PCT Article 33(3) as being obvious over Wsens in view of Tivarus and further in view of US 2012/0153127 A1 to Hirigoyen et al. (hereinafter "Hirigoyen").

Regarding claim 10, Wsens in view of Tivarus disclose the structure of claim 1, but fails to disclose further including light blockers between adjacent pixels to reduce crosstalk. Hirigoyen, drawn to image sensor, discloses light blocker (40) between adjacent pixels (S1, S2) to reduce crosstalk (Fig. 4; para [0008], [0052])—Isolation region H... reduces optical crosstalk thanks to an optical waveguide formed by the differences in refractive indices between the substrate 10, the conductive material 30, and the optical isolator 40. para [0087]—Image sensor IS3 differs from image sensor IS2 in that the color filters F1, F2, F3 and the microlenses L1, L2, L3 are arranged on the backside of the substrate 10...the optical isolator 40 extends entirely through the trench 15). It would have been obvious to a person having ordinary skill in the art to combine the light blockers disclosed by Hirigoyen to the structure disclosed by Wsens to enhance the performance by reducing the crosstalk between pixels (See Hirigoyen, para [0052]).

Claim 32 lacks an inventive step under PCT Article 33(3) as being obvious over Wsens in view of Tivarus and further in view of US 2018/0012916 A1 to Artix Corporation (hereinafter "Artix").

Regarding claim 32, Wsens in view of Tivarus disclose the structure of claim 31. Wsens further discloses array of optical filters (para [0241])—each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array). Wsens in view of Tivarus fail to disclose said array of optical filters includes Near InfraRed (NIR) filters to select specific NIR wavelength ranges. Artix, drawn to image sensor array, discloses NIR filter to select specific NIR wavelength ranges (para [0058])—the optical signal 406 may be filtered by a wavelength filter not shown in this figure, such as an NIR filter in the filter layer). It would have been obvious to a person having ordinary skill to include some of the NIR filters disclosed by Artix to the array of optical filters to increase the performance of the filter by enabling selecting specific NIR wavelength ranges (See Artix, para [0059]).

Claims 3-6, 12, 17-19, 21, 33, 36, 38, and 42 meet the criteria set forth under PCT Article 33(2)-(3) because the prior art does not teach or fairly suggest the subject matter claimed.

The prior art for claim 3 is exemplified by Wsens, Tivarus, US 2019/0166317 A1 to Brillnics, Inc (hereinafter "Brillnics"), and US 2012/0012741 A1 (Vasylyev).

Regarding claim 3,

Wsens in view of Tivarus disclose the structure of claim 2. Wsens further discloses at least one Near InfraRed (NIR) pixel and an NIR optical filter over said NIR pixel to select specific NIR wavelength ranges (para [0122])—The wavelength range, depending on the percentage of Ge in Si, for 0% Ge can range from 840-960 nm, and with 10% Ge or less in GeSi alloy that is either relaxed or not relaxed, the wavelength can range from 840-960 nm for not relaxed GeSi layer and 840-960 nm for relax, for 20% or less Ge, the wavelength can be extended to 1000 nm and in some cases to 1250 nm for not relaxed GeSi layer and for 40% or less Ge, the wavelength can be extended to 1310 nm (it is noted the wavelength of 840-1310 nm is in the NIR wavelength range); para [0241])—each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array.) Wsens in view of Tivarus fail to disclose in which said pixels are configured in a Bayer array and each of at least several pixels in the Bayer array encompasses only a single hole in said photosensor wafer.

Brillnics, drawn to a CMOS sensor, discloses pixels are configured in a Bayer array (para [0068])—when the unit pixel groups are arranged in the Bayer array) that includes at least one Near InfraRed (NIR) pixel (para [0096])—The color pixels in the unit RGB pixel group 200 configured as described above not only have an inherent particular responsibility in a visible range (400 nm to 700 nm), but also have a high responsibility in a near-infrared (NIR) region (800 nm to 1,000 nm). However, Brillnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

--see next page

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US 20/51735

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

Box V.2 - Citations and Explanations:

Vasylyev, drawn to a light detector, discloses one lenses with one hole (Fig. 10-11; para [0088]- FIG. 10 shows a cone-shape cavity forming light input port 14; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14). However, Vasylyev fails to remedy the deficiencies of Wsens, Tivarus and Brilnics.

None of the prior art discloses each of at least several pixels in the Bayer array encompasses only a single hole in said photosensor wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 3, therefore claim 3 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claim 4 and 33 is exemplified by Wsens, Tivarus and Brilnics.

Regarding claim 4, Wsens in view of Tivarus disclose the structure of claim 2, but fail to disclose in which said pixels include one or more Bayer arrays at least one of which comprises a Near InfraRed (NIR) pixel, and wherein the at least one NIR pixel in at least one of said one or more Bayer arrays is larger than other pixels therein.

Brilnics, drawn to a CMOS sensor, discloses pixels include one or more Bayer arrays at least one of which comprises a Near InfraRed (NIR) pixel (para [0068]-when the unit pixel groups are arranged in the Bayer array; para [0095]- the photodiode PD22 serving as the second green (Gr) photoelectric conversion part also operate as infrared (NIR) photoelectric conversion parts.). However, Brilnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses wherein the at least one NIR pixel in at least one of said one or more Bayer arrays is larger than other pixels therein. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 4, therefore claim 4 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 33, Wsens in view of Tivarus disclose the structure of claim 32, but fail to disclose wherein said array of photodetectors includes some that are larger than others, and said larger photodetectors are under said NIR filters.

Brilnics, drawn to a CMOS sensor, discloses NIR photodetector are larger (para [0012]-Further, there has been known an infrared (IR, NIR) sensor in which the four pixels in a unit pixel group are replaced with one NIR dedicated pixel having a larger pixel size.). However, Brilnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses wherein said array of photodetectors includes some that are larger than others, and said larger photodetectors are under said NIR filters. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 33, therefore claim 33 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claim 5 and 12 is exemplified by Wsens, Tivarus and Vasylyev

Regarding claim 5, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which each of said at least some of said pixels has only a single one of said holes.

Vasylyev, drawn to a light detector, discloses one lenses with one hole (Fig. 10-11; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14.). However, Vasylyev fails to remedy the deficiencies of Wsens.

None of the prior art discloses in which each of said at least some of said pixels has only a single one of said holes. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 5, therefore claim 5 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 12, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which at least some of said pixels have only a single hole each and said single hole is an off-center hole.

Vasylyev, drawn to a light detector, discloses photodetector have only a single hole each (Fig. 10-11; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14). However, Vasylyev fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses said single hole is an off-center hole. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 12, therefore claim 12 meets the criteria set out in PCT Article 33(2)-(3).

-see next page

Form PCT/ISA/237 (Supplemental Box) (revised January 2019)

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US 20/51733

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

Box V.2 - Citations and Explanations:

The prior art for claim 17 is exemplified by Wsens, Tivarus and Hingoyen.

Regarding claim 17, Wsens in view of Tivarus disclose the structure of claim 1, but fails to disclose in which said pixels have slanted sidewalls configured to reduce crosstalk between adjacent pixels and improve optical confinement.

Hingoyen, drawn to image sensor, discloses sidewalls (40) configured to reduce crosstalk between adjacent pixels and improve optical confinement (Fig. 4; para [0052]- isolation region 11... reduces optical crosstalk thanks to an optical waveguide formed by the differences in refractive indices between the substrate 10, the conductive material 30, and the optical isolator 40. para [0057]- Image sensor IS3 differs from image sensor IS2 in that the color filters F1, F2, F3 and the microlenses L1, L2, L3 are arranged on the backside of the substrate 10...the optical isolator 40 extends entirely through the trench 15). However, Hingoyen otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses said pixels have slanted sidewalls configured to reduce crosstalk between adjacent pixels and improve optical confinement. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 17, therefore claim 17 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claims 18-19, 21, 36, 38 and 42 is exemplified by Wsens and Tivarus.

Regarding claim 18, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said holes are conformally lined with doped Si (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose at least some adjacent holes are doped to opposite polarities.

None of the prior art discloses at least some adjacent holes are doped to opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 18, therefore claim 18 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 19, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses graphene (para [0195]- the basic steps consist of etching holes in a device wafer that can include epitaxial layers that can include doped P and/or N and/or I layers, SOI, additional dielectric coatings, metallic layers/fillers, graphene). Wsens in view of Tivarus fail to disclose at least some of said holes are conformally lined with graphene.

None of the prior art discloses at least some of said holes are conformally lined with graphene. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 19, therefore claim 19 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 21, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which said pixels are in an array in which centrally located pixels are smaller in size than other pixels.

None of the prior art discloses said pixels are in an array in which centrally located pixels are smaller in size than other pixels. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 21, therefore claim 21 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 36, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which said holes are conformally lined with doped Si (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose adjacent holes are doped to opposite polarities.

None of the prior art discloses adjacent holes are doped to opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 36, therefore claim 36 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 38, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses graphene (para [0195]- the basic steps consist of etching holes in a device wafer that can include epitaxial layers that can include doped P and/or N and/or I layers, SOI, additional dielectric coatings, metallic layers/fillers, graphene). Wsens in view of Tivarus fail to disclose said holes are conformally lined with graphene.

None of the prior art discloses said holes are conformally lined with graphene. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 38, therefore claim 38 meets the criteria set out in PCT Article 33(2)-(3).

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WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US 2005/1733

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

Box V.2 - Citations and Explanations.

Regarding claim 42, Weens in view of Tivarus disclose the monolithic wafer of claim 40. Weens further discloses in which said holes are lined with doped regions of said wafer (Fig. 42; para [3319]). The microstructure holes 4212 can be etched first partially into the low doped and/or undoped 1 Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P (or N) type dopants). Weens in view of Tivarus fail to disclose adjacent holes are lined with doped regions of opposite polarities.

None of the prior art discloses adjacent holes are lined with doped regions of opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 42, therefore claim 42 meets the criteria set out in PCT Article 33(2)-(3).

Claims 1-42 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

SEARCH HISTORY

Application Number	PCT/US 20/51733
Search Conducted By	JQ
Search Approved By	ALK

CPC/IPC Classifications Searched	CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102 IPC (8)- H01L 27/146, 31/101, 31/102 (2020.01)
Date Conducted	09 November 2020 (09.11.2020)

Documentation Searched	CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102 IPC (8)- H01L 27/146, 31/101, 31/102 (2020.01)
Search Terms Used	Photosensor/photodetect*/photodiode/hspa Wafer/substrate Crystal/crystalline Si/silicon Cmos/clp Stack~/layer~ Pixel Array/grid Lens/lenses/microlenses Hole/opening/aperture Micro/microstructure/um N/P/dope~ Lines/traces/interconnects
Date Conducted	09 November 2020 (09.11.2020)

Electronic Database Searched	PatBase
Files Searched	Full-text: AU BE BR CA CH CN DE DK EP ES FI FR GB IN JP KR SE TH TW US WO Bibliographic: Europe AT BA BE BG CH CS CY CZ DD DK EE ES FI GE GR HR HU IE IS IT LT LU LV MC MD MT NL NO PL PT RO RS SE SI SK SM TR UA YU Asia EA GC HK ID IL IN KZ MN MY PH RU SG SU TH TJ TW UZ VN North America CA CR CU DO GT HN MX NI PA SV TT South America AR BR CL CO EC PE UY Australasia AU NZ Africa AP DZ EG KE MA MW OA ZA ZM ZW
Date Conducted	09 November 2020 (09.11.2020)
Search Logic: Classification Search: 1) IC=(H01L27/146 or H01L31/101 or H01L 31/102) (45716)	

- 2) CPC=(H01L27/14609 or H01L27/14612 or H01L27/14643 or H01L31/101 or H01L31/102) (9304)
- 3) 1 or 2 (46498)
- 4) 3 and FT=(Photosensor? or photodetect* or photodiode? or hspa) (13742)
- 5) 4 and FT=(wafer or substrate) (11476)
- 6) 5 and FT=((crystal or crystalline) w3 (Si or silicon)) (1286)
- 7) 6 and FT=(cmos or clip) (747)
- 8) 7 and FT=(stack~ or layer~) (733)
- 9) 8 and FT=(pixel?) (561)
- 10) 9 and FT=(array or grid) (423)
- 11) 10 and FT=(lens or lenses or microlenses) (281)
- 12) 11 and FT=(hole? or opening? or aperture?) (181)
- 13) 12 and FT=(micro or microstructure or um) (146)
- 14) 13 and FT=(N or P or doped or doping) (144)
- 15) 14 and FT=(lines or traces or interconnects) (102)
- 16) 15 and FT=(color w3 filter?) (57)
- 17) 16 and FT=("Near InfraRed" or NIR) (26)
- 18) 16 and FT=(cmos w3 circuit?) (19)
- 19) 18 not 17 (13)
- 20) 3 and FT=(cmos or clip) (20106)
- 21) 20 and FT=((Photosensor? or photodetect* or photodiode? or hspa) w3 (wafer or substrate)) (762)
- 22) 21 and FT=((array or grid) w3 pixel?) (211)
- 23) 22 and FT=(lens or lenses or microlenses) (158)
- 24) 23 and FT=(hole? or opening? or aperture?) (101)
- 25) 24 and FT=(micro or microstructure or um) (79)
- 26) 25 and FT=(lines or traces or interconnects) (70)
- 27) 26 and FT=(color w3 filter?) (49)
- 28) 27 not (17 or 18) (39)
- 29) 26 and FT=("Near InfraRed" or NIR) (16)
- 30) 29 not (17 or 18 or 27) (3)

Search limited only by search terms and not by classifications:

- 31) FT=((Photosensor? or photodetect* or photodiode? or hspa) w3 (wafer or substrate)) (3738)
- 32) 31 and FT=(cmos or clip) (1143)
- 33) 32 and FT=((array or grid) w3 pixel?) (272)
- 34) 33 and FT=(lens or lenses or microlenses) (205)
- 35) 34 and FT=(hole? or opening? or aperture?) (126)
- 36) 35 and FT=(micro or microstructure or um) (98)
- 37) 36 and FT=(lines or traces or interconnects) (83)
- 38) 37 and FT=(color w3 filter?) (53)
- 39) 38 not (17 or 18 or 27 or 29) (4)
- 40) 37 and FT=("Near InfraRed" or NIR) (20)
- 41) 40 not (17 or 18 or 27 or 29 or 38) (3)
- 42) FT=(cmos w3 circuit?) (17544)
- 43) 42 and FT=((Photosensor? or photodetect* or photodiode? or hspa) w3 (wafer or substrate)) (110)
- 44) 43 and FT=((array or grid) w3 pixel?) (39)
- 45) 44 not (17 or 18 or 27 or 29 or 38 or 40) (29)
- 46) 42 and FT=(Photosensor? or photodetect* or photodiode? or hspa) (1555)
- 47) 46 and FT=((crystal or crystalline) w3 (Si or silicon)) (443)
- 48) 47 and FT=((array or grid) w3 pixel?) (64)
- 49) 48 not (17 or 18 or 27 or 29 or 38 or 40 or 44) (42)

F/B search:

50) PN=(us2018102442 or us2017250211) (2)

51) CTB 50 or CTF 50 (269)

52) 51 not (17 or 18 or 27 or 29 or 38 or 40 or 44 or 48) (265)

53) 52 and FT=(cmos w3 circuit?) (13)

Electronic Database Searched	Google
Files Searched	Google Patents
Date Conducted	09 November 2020 (09.11.2020)
Search Logic:	
photosensor cmos logic processor About 12,000 results	
photosensor cmos logic processor wafer About 3,810 results	
photosensor cmos logic processor wafer array pixels About 2,760 results	
photosensor cmos logic processor wafer array pixels lenses About 2,090 results	
photosensor cmos logic processor wafer array pixels lenses n-doped About 802 results	
photosensor cmos logic processor wafer array pixels lenses p-doped About 1,850 results	
photosensor cmos circuits wafer array pixels lenses About 4,400 results	
photosensor cmos circuits wafer array pixels lenses NIR About 1,270 results	

Electronic Database Searched	Google
Files Searched	Google Scholar
Date Conducted	09 November 2020 (09.11.2020)
Search Logic:	
photosensor cmos logic processor About 20,000 results	
photosensor cmos logic processor wafer About 5,410 results	

photosensor cmos logic processor wafer array pixels
About 3,250 results

photosensor cmos logic processor wafer array pixels lenses
About 1,980 results

photosensor cmos logic processor wafer array pixels lenses n-doped
About 157 results

photosensor cmos logic processor wafer array pixels lenses p-doped
About 145 results

photosensor cmos circuits wafer array pixels lenses
About 6,740 results

photosensor cmos circuits wafer array pixels lenses NIR
About 1,120 results

Supplemental SAO searching:

Electronic Database Searched		PatBase
Files Searched		Full-text: AU BE BR CA CH CN DE DK EP ES FI FR GB IN JP KR SE TH TW US WO Bibliographic: (Europe) AT BA BE BG CH CS CY CZ DD DK EE ES FI GE GR HR HU IE IS IT LT LU LV MC MD MT NL NO PL PT RO RS SE SI SK SM TR UA YU (Asia) EA GC HK ID IL IN KZ MN MY PH RU SG SU TH TJ TW UZ VN (North America) CA CR CU DO GT HN MX NI PA SV TT (South America) AR BR CL CO EC PE UY (Australasia) AU NZ (Africa) AP DZ EG KE MA MW OA ZA ZM ZW
Date Conducted		20 November 2020 (20.11.2020)
Search Logic:		
Search 1:	(photosens* or photodetect*) (Results 567476)	
Search 2:	1 and (wafer or substrate or chip) (Results 212373)	
Search 3:	2 and (si or silicon) (Results 111160)	
Search 4:	3 and (CMOS) (Results 15125)	
Search 5:	4 and (pixel%) (Results 9352)	
Search 6:	5 and (dope or doped or doping) (Results 4083)	
Search 7:	6 and (lens or lenses or microlenses) (Results 2208)	
Search 8:	7 and ((connect* or interconnect*) near pixel%) (Results 813)	
Search 9:	8 and (holes OR microholes) (Results 481)	
Search 10:	8 and (holes OR microholes or nanohole%) (Results 481)	
Search 11:	10 and ((holes OR microholes or nanohole%) near (lens or lenses or microlenses)) (Results 3)	
Search 12:	10 and ((holes OR microholes or nanohole%) near (pixel%)) (Results 40)	
Search 13:	10 and Bayer (Results 103)	
Search 14:	13 and (IR or NIR or infrared or (infra%red) or (infra_red)) (Results 86)	
Search 15:	10 and (((holes OR microholes or nanohole%) near (pixel%)) near (one or single)) (Results 8)	
Search 16:	10 and (((wall% or sidewall%) near pixel% near (angle~ or slant~)) (Results 2)	

Search 17: 10 and ((hole% or microhole%) near dope~) (Results 18)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

NOTIFICATION OF TRANSMITTAL OF
THE INTERNATIONAL SEARCH REPORT AND
THE WRITTEN OPINION OF THE INTERNATIONAL
SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

To: IVAN S. KAVRUKOV WISSING MILLER LLP 434 WEST 33RD STREET, 7TH FLOOR NEW YORK, NY 10001		Date of mailing (day/month/year) DEC 06 2021
Applicant's or agent's file reference 309-0013PCT	FOR FURTHER ACTION See paragraphs 1 and 4 below	
International application No. PCT/US 21/50717	International filing date (day/month/year) 16 September 2021 (16.09.2021)	
Applicant W&SENS DEVICES, INC.		

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:
 The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

How? Directly to the International Bureau preferably through ePCT, or on paper to:
 The International Bureau of WIPO, 34, chemin des Colombettes, 1211 Geneva 20, Switzerland

For more detailed instructions, see the *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:**

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

Shortly after the expiration of **18 months from the priority date, the international application will be published** by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months from the priority date**, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months from the priority date** (in some Offices even later); otherwise, the applicant must, **within 20 months from the priority date**, perform the prescribed acts for **entry into the national phase** before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Within **22 months from the priority date**, the applicant may request that a **supplementary international search** be carried out by a different International Searching Authority that offers this service (Rule 45bis.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Kari Rodriguez Telephone No. PCT Helpdesk: 571-272-4300
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Form PCT/ISA/220 (revised January 2020)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 309-0013PCT		FOR FURTHER ACTION see Form PCT/ISA/220 as well as, where applicable, item 5 below.	
International application No. PCT/US 21/50717	International filing date (<i>day/month/year</i>) 16 September 2021 (16.09.2021)	(Earliest) Priority Date (<i>day/month/year</i>) 21 September 2020 (21.09.2020)	
Applicant W&WSENS DEVICES, INC.			

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

a. With regard to the language, the international search was carried out on the basis of:

- ☒ the international application in the language in which it was filed.
☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).

c. ☐ With regard to any nucleotide and/or amino acid sequence disclosed in the international application, see Box No. I.

2. ☐ Certain claims were found unsearchable (see Box No. II).

3. ☐ Unity of invention is lacking (see Box No. III).

4. With regard to the title,

- ☒ the text is approved as submitted by the applicant.
☐ the text has been established by this Authority to read as follows:

5. With regard to the abstract,

- ☒ the text is approved as submitted by the applicant.
☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the drawings,

- a. the figure of the drawings to be published with the abstract is Figure No. 25
☒ as suggested by the applicant.
☐ as selected by this Authority, because the applicant failed to suggest a figure.
☐ as selected by this Authority, because this figure better characterizes the invention.
- b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 21/50717

A. CLASSIFICATION OF SUBJECT MATTER IPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762 (2021.01) CPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762; H04N 5/36965; H01G 9/2045		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) See Search History document		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched See Search History document		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) See Search History document		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2018/0102442 A1 (W&WSENS, DEVICES INC.) 12 April 2018 (12.04.2018) entire document, especially: para [0031], [0223], [0241], [0263], [0456], [0549]	1-22
A	US 2016/0240579 A1 (OMNIVISION TECHNOLOGIES INC.) 18 August 2016 (18.08.2016) entire document, especially: para [0002], [0020], [0023], [0024], [0034], [0038]	1-22
A	US 2017/0141153 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 18 May 2017 (18.05.2017) entire document, especially: [0015]-[0019], [0023], [0024], [0055]	1-22
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 08 November 2021		Date of mailing of the international search report DEC 06 2021
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300		Authorized officer Kari Rodriguez Telephone No. PCT Helpdesk: 571-272-4300

Form PCT/ISA/210 (second sheet) (July 2019)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: IVAN S. KAVRUKOV
WISSING MILLER LLP
434 WEST 33RD STREET, 7TH FLOOR
NEW YORK, NY 10001

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing
(day/month/year)

DEC 06 2021

Applicant's or agent's file reference

309-0013PCT

FOR FURTHER ACTION

See paragraph 2 below

International application No.

PCT/US 21/50717

International filing date (day/month/year)

16 September 2021 (16.09.2021)

Priority date (day/month/year)

21 September 2020 (21.09.2020)

International Patent Classification (IPC) or both national classification and IPC

IPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762 (2021.01)

CPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762; H04N 5/36965;
H01G 9/2045

Applicant W&WSENS DEVICES, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US
Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450
Facsimile No. 571-273-8300

Date of completion of this opinion

08 November 2021

Authorized officer

Kari Rodriguez

PCT Help Desk

Telephone No. 571-272-4300

Form PCT/ISA/237 (cover sheet) (revised January 2019)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US 21/50717

Box No. 1 Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
 - ☒ the international application in the language in which it was filed.
 - ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(b)).
3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:
 - a. ☐ forming part of the international application as filed:
 - ☐ in the form of an Annex C/ST.25 text file.
 - ☐ on paper or in the form of an image file.
 - b. ☐ furnished together with the international application under PCT Rule 13ter.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
 - c. ☐ furnished subsequent to the international filing date for the purposes of international search only:
 - ☐ in the form of an Annex C/ST.25 text file (Rule 13ter.1(a)).
 - ☐ on paper or in the form of an image file (Rule 13ter.1(b) and Administrative Instructions, Section 713).
4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
5. Additional comments:

Form PCT/ISA/237 (Box No. 1) (revised January 2019)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US 21/50717

Box No. V	Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement		
1. Statement			
Novelty (N)	Claims	1-22	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-22	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-22	YES
	Claims	NONE	NO
2. Citations and explanations:			
<p>Claims 1-22 meet the criteria set out in PCT Article 33(2)-(3) because the prior art does not teach or fairly suggest the subject matter claimed.</p> <p>The prior art for claim 1-22 is exemplified by US 2018/0102442 A1 to W&WSens, Devices Inc. (hereinafter 'W&WSens'), US 2016/0240579 A1 to Omnivision Technologies Inc. (hereinafter 'Omnivision'), and US 2017/0141153 A1 to Taiwan Semiconductor Manufacturing Co. Ltd. (hereinafter 'Taiwan').</p> <p>Regarding Claim 1, W&WSens discloses a microstructure enhanced absorption photosensitive device (para [0031]- This patent specification relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.) comprising: a CMOS ASIC wafer (120) (para [0223]- FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments. The chip can include multiple MSPD (and/or MSAPD) with single and/or multiple CMOS/BiCMOS electronic application specific integrated circuits.) the CMOS ASIC wafer is configured to process signals (para [0203]- CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers); a semiconductor material (102) in which an array is formed (para [0241]- MSPD/MSAPD arrays can be fabricated over the holes either in the oxide and/or in the silicon such that each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array.); wherein a region of undoped or low-doped Si (FIG. 24; element "I Si"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) between said doped Si regions (see arrangement of elements of "P Si and/or GeSi and/or Ge", "I Si" and "N Si and/or Bragg reflector layers of Si/GeSi"), and a single microhole (2540) (FIG. 24, 2412; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.); wherein a region of undoped or low-doped Ge or an alloy (FIG. 24; element "I Si and/or GeSi and/or Ge"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) thereof between said doped regions of Ge or an alloy thereof (see arrangement of elements of "P Si and/or GeSi and/or Ge", "I Si and/or GeSi and/or Ge" and "N Si and/or GeSi and/or Ge"); deep trench (FIG. 89, element 8970; para [0549]- In some cases, instead of a highly doped connecting well, a deep trench with oxide 8970 on its sidewalls and the center can have conducting silicide 8972 and/or metal as shown in FIG. 89); and connecting electrodes (para [0456]- In some cases a metal connecting electrode can be formed from the surface to the P+ substrate via a trench (not shown) and in some cases a TSV (not shown) can be formed to the bottom anode metal). W&WSens fails to disclose a CMOS image sensor wafer (CIS) stacked to each other, the CMOS ASIC wafer is configured to receive the signals that the CIS wafer produces, wherein the CIS wafer comprises: an array of both Si pixels and Ge pixels; each Si pixel comprises an upper and a lower region of Si doped to opposite polarities and the microhole extending into the Si pixel; each Ge pixel comprises an upper and a lower region of Ge or an alloy thereof doped to opposite polarities and a single microhole extending into the Ge pixel; wherein the deep trench is a trench isolation between adjacent Si pixels and Ge pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the Si and Ge pixels; and pixel electrodes coupled to said Si and Ge pixels, wherein connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.</p> <p>Omnivision discloses a microstructure enhanced absorption photosensitive device (para [0002]-This invention is related to image sensors; para [0020]- each of the plurality of visible light pixels includes a photosensitive element, such as for example a photodiode, to receive a portion of light, and pixel support circuitry to generate a signal representative of an intensity of the received portion of light.) comprising: a CMOS ASIC wafer (para [0034]- Digital counter 480 may be implemented using CMOS circuitry disposed on the ASIC die fabricated using a standard CMOS process of the stacked die system) and a CMOS image sensor wafer (CIS) (FIG. 2, image sensor 200) stacked to each other (para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme) such that signals that the CIS wafer produces (para [0023]- In one example, each of the plurality of visible light pixels 211 includes a photosensitive element such as a photodiode to receive a portion of light, as well as pixel support circuitry to generate a signal representative of an intensity of the received portion of light.), wherein the CIS wafer comprises: a semiconductor material (FIG. 5, semiconductor layer 510) in which an array is formed of Si pixels (para [0020]- For instance, in one example, an imaging system includes an image pixel array having a plurality of visible light pixels, and a plurality of silicon photon avalanche diode (SPAD) pixels). (claim 1 continued) --see supplemental box</p>			

Form PCT/ISA/237 (Box No. V) (revised January 2019)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US 21/50717

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

---Box V.2 - Citations and Explanations---

(claim 1 continued)

Omnivision fails to disclose the CMOS ASIC wafer is configured to receive and process signals, and wherein an array is formed of both Si pixels and Ge pixels; wherein each Si pixel comprises an upper and a lower region of Si doped to opposite polarities and a region of undoped or low-doped Si between said doped Si regions, and a single microhole extending into the Si pixel; wherein each Ge pixel comprises an upper and a lower region of Ge or an alloy thereof doped to opposite polarities and a region of undoped or low-doped Ge or an alloy thereof between said doped regions of Ge or an alloy thereof, and a single microhole extending into the Ge pixel; deep trench insulation between adjacent Si pixels and Ge pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the Si and Ge pixels; and pixel electrodes coupled to said Si and Ge pixels, connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Taiwan discloses a microstructure enhanced absorption photosensitive device (para [0017]- The present application is directed to a CMOS image sensor with elemental silicon and silicon germanium for long-wavelength pixel sensors: By arranging the photodetector in the silicon germanium layer, the photodetector advantageously has good sensitivity to and absorption of long-wavelength radiation, such as, for example, infrared radiation) comprising: a CMOS image sensor wafer (CIS) (FIG.1, 100; para [0018]- With reference to FIG. 1, a cross-sectional view 100 of some embodiments of a CMOS image sensor with a semiconductor stack 102 of silicon and silicon germanium is provided.), wherein the CIS wafer comprises:

a semiconductor material in which an array is formed of both Si pixels and Ge pixels (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer; para [0016]- Another solution is to use silicon germanium in place of elemental silicon for the semiconductor layer); wherein each Si pixel comprises an upper (FIG.2A, upper silicon layer 104; para [0023]- an upper silicon layer 104 a of the pair is arranged over and directly abuts the silicon germanium layer 106 a.) and a lower region of Si (FIG.2A, lower silicon layer 204; para [0023]- Further, in some embodiments, a lower silicon layer 204 of the pair is arranged over and directly abuts the semiconductor substrate 202) doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204); wherein each Ge pixel comprises a region of Ge or an alloy thereof doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204 and a silicon germanium layer 106 a arranged between the silicon layers 104 a, 204);

deep trench insulation (FIG. 1, deep trench isolation 112; para [0024]- The isolation region 112 is, for example, a shallow trench isolation (STI) region, a deep trench isolation (DTI) region, or an implant isolation region.) between adjacent Si pixels and Ge pixels (para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region; para [0016]- Another solution is to use silicon germanium in place of elemental silicon for the semiconductor layer.) in said array (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) and an electrically and optically isolating material in said deep trench insulation (para [0061]- In some embodiments, the process for forming the isolation region 112 comprises filling the trench with a dielectric material, such as silicon dioxide.) in the Si and Ge pixels (para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region; para [0019]- The pixel sensor 110 comprises a photodetector 114 at least partially buried in the silicon germanium layer 106, and one or more pixel transistors arranged on the upper surface 108 of the silicon layer 104.); and pixel electrodes coupled to said Si and Ge pixels (Claim 21- wherein the transistor further comprises a gate electrode, a gate dielectric layer, and an additional source/drain region, wherein the gate dielectric layer spaces the gate electrode over the surface of the silicon layer; para [0017]- A photodetector is at least partially buried in the silicon germanium layer and a transistor is arranged on a surface of the elemental silicon layer with a source/drain region electrically coupled to the photodetector);

Taiwan fails to disclose a CMOS ASIC wafer and a CMOS image sensor wafer (CIS) stacked to each other such that the CMOS ASIC wafer is configured to receive and process signals that the CIS wafer produces, wherein a region of Si to opposite polarities and a region of undoped or low-doped Si between said doped Si regions, and a single microhole extending into the Si pixel, wherein an upper and lower region of Ge or an alloy thereof to opposite polarities and a region of undoped or low-doped Ge or an alloy thereof between said doped regions of Ge or an alloy thereof, and a single microhole extending into the Ge pixel; an electrically and optically isolating material in said microholes; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

None of the prior art discloses, the CMOS ASIC wafer is configured to receive signals; a region of Si to opposite polarities and the microhole extending into the Si pixel; an upper and a lower region of Ge or an alloy thereof to opposite polarities and a single microhole extending into the Ge pixel; an electrically and optically isolating material in said microholes; wherein connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular elements as required by claim 1, therefore claim 1 meets the criteria set out in PCT Article 33(2)-(3).

Claims 2-13 depend from claim 1, and therefore, meet the criteria set out in PCT Article 33(2)-(3) as well.

--see next page

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US 21/50717

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

---Supplemental Box - Box V.2 - Citations and Explanations---

Regarding Claim 14,

W&WSens discloses a method (para [0031]- This patent specification relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics; para [0061]- According to some embodiments, a method of making a microstructure-enhanced photodetector (MSPD) configured to convert an optical input that at least some of the time has a cross-section that is essentially continuous spatially to an electrical output) comprising:

a CMOS ASIC wafer (120) (para [0223]- FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments. The chip can include multiple MSPD (and/or MSAPD) with single and/or multiple CMOS/BiCMOS electronic application specific integrated circuits.) such that the CMOS ASIC wafer is configured to process signals (para [0203]- CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers);

forming a semiconductor material (102) by fabricating an array of pixels (2530 and/or 2532) therein (para [0241]- MSPD/MSAPD arrays can be fabricated over the holes either in the oxide and/or in the silicon such that each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array.);

forming a region of undoped or low-doped semiconductor material (FIG. 24; element "I Si and/or GeSi and/or Ge"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) between said doped regions (see arrangement of elements of "P Si and/or GeSi and/or Ge", "I Si and/or GeSi and/or Ge" and "N Si and/or GeSi and/or Ge"), and a single microhole (2540) (FIG. 24, 2412; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.);

forming deep trench (FIG. 89, element 8970; para [0549]- In some cases, instead of a highly doped connecting well, a deep trench with oxide 8970 on its sidewalls and the center can have conducting silicide 8972 and/or metal as shown in FIG. 89);

and forming connecting electrodes (para [0456]- In some cases a metal connecting electrode can be formed from the surface to the P+ substrate via a trench (not shown) and in some cases a TSV (not shown) can be formed to the bottom anode metal).

W&WSens fails to disclose stacking and bonding to each other a CMOS image sensor wafer (CIS) (110), and the CMOS ASIC wafer is configured to receive the signals that the CIS wafer produces; forming at each pixel an upper and a lower region of semiconductor material doped to opposite polarities (2534, 2536), wherein the microhole (2540) extending into the pixel; wherein the deep trench is a trench isolation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the pixels; and forming pixel electrodes (154) coupled to said pixels, wherein connecting electrodes (152) coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Omnivision discloses a method (para [0002]-This invention is related to image sensors; para [0027]- In the example, the sensor die and ASIC die are stacked and coupled together during fabrication in a stacked chip scheme) comprising:

stacking and bonding (para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme; para [0038]- FIG. 5 includes a first device die 506, a second device die 508 and a bonding interface 507 at which first device die 506 is bonded to second device die 508.) to each other a CMOS ASIC wafer (para [0034]- Digital counter 480 may be implemented using CMOS circuitry disposed on the ASIC die fabricated using a standard CMOS process of the stacked die system) and a CMOS image sensor wafer (CIS) (FIG. 2, image sensor 200; para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme) such signals that the CIS wafer produces (para [0023]- In one example, each of the plurality of visible light pixels 211 includes a photosensitive element such as a photodiode to receive a portion of light, as well as pixel support circuitry to generate a signal representative of an intensity of the received portion of light.);

forming the CIS wafer in a semiconductor material (FIG. 5, semiconductor layer 510) by fabricating an array of pixels therein (para [0020]- For instance, in one example, an imaging system includes an image pixel array having a plurality of visible light pixels, and a plurality of silicon photon avalanche diode (SPAD) pixels; para [0038]- The illustrated example shows a plurality of visible light pixels, 502A, 502B, 502C and 502D, as well as a plurality of SPAD pixels 503A and 503B).

Omnivision fails to disclose the CMOS ASIC wafer is configured to receive and process signals; forming at each pixel an upper and a lower region of semiconductor material doped to opposite polarities and a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; wherein the deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the pixels; forming deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the pixels; and forming pixel electrodes coupled to said pixels, connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Taiwan discloses a method (para [0056]- With reference to FIGS. 6-12, a series of cross-sectional views of some embodiments of a method for manufacturing a CMOS image sensor with silicon and silicon germanium is provided.) comprising:

a CMOS image sensor wafer (CIS) (FIG. 1, 100; para [0018]- With reference to FIG. 1, a cross-sectional view 100 of some embodiments of a CMOS image sensor with a semiconductor stack 102 of silicon and silicon germanium is provided.);

forming the CIS wafer in a semiconductor material by fabricating an array of pixels therein (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer);

forming at each pixel an upper (FIG. 2A, upper silicon layer 104; para [0023]- an upper silicon layer 104 a of the pair is arranged over and directly abuts the silicon germanium layer 106 a.) and a lower region of semiconductor material (FIG. 2A, lower silicon layer 204; para [0023]- Further, in some embodiments, a lower silicon layer 204 of the pair is arranged over and directly abuts the semiconductor substrate 202) doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204) to opposite polarities and a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; (claim 14 continued)

---see next page

Form PCT/ISA/237 (Supplemental Box) (revised January 2019)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US 21/50717

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

---Supplemental Box - Box V.2 - Citations and Explanations---

(claim 14 continued) forming deep trench insulation (FIG. 1, deep trench isolation 112; para [0024]- The isolation region 112 is, for example, a shallow trench isolation (STI) region, a deep trench isolation (DTI) region, or an implant isolation region.) between adjacent pixels (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) in said array (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) and an electrically and optically isolating material in said deep trench insulation in the pixels (para [0061]- In some embodiments, the process for forming the isolation region 112 comprises filling the trench with a dielectric material, such as silicon dioxide.; para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region); and forming pixel electrodes coupled to said pixels (Claim 21- wherein the transistor further comprises a gate electrode, a gate dielectric layer, and an additional source/drain region, wherein the gate dielectric layer spaces the gate electrode over the surface of the silicon layer).

Taiwan fails to disclose stacking and bonding to each other a CMOS ASIC wafer and a CMOS image sensor wafer (CIS) such that the CMOS ASIC wafer is configured to receive and process signals that the CIS wafer produces; forming a region to opposite polarities and a region of undoped or low-doped semiconductor material between said doped region; optically isolating material in said microholes; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

None of the prior art discloses, the CMOS ASIC wafer is configured to receive signals; a region to opposite polarities and the microhole extending into the pixel; optically isolating material in said microholes in the pixels; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular steps as required by claim 14, therefore claim 14 meets the criteria set out in PCT Article 33(2)-(3).

Claim 15 depends from claim 14, and therefore, meet the criteria set out in PCT Article 33(2)-(3) as well.

Regarding Claim 16,

W&WSens discloses a microstructure enhanced absorption photosensitive device (para [0031]- This patent specification relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.) comprising: a CMOS ASIC wafer (para [0223]- FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments. The chip can include multiple MSPD (and/or MSAPD) with single and/or multiple CMOS/BiCMOS electronic application specific integrated circuits.) the CMOS ASIC wafer is configured to process signals (para [0203]- CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers);

a layer in which an array of pixels is formed (para [0241]- MSPD/MSAPD arrays can be fabricated over the holes either in the oxide and/or in the silicon such that each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array);

wherein a region of undoped or low-doped semiconductor material (FIG. 24; element "I Si and/or GeSi and/or Ge"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) between said doped regions (see arrangement of elements of "P Si and/or GeSi and/or Ge", "I Si and/or GeSi and/or Ge" and "N Si and/or GeSi and/or Ge"), and a single microhole (2540) (FIG. 24, 2412; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.);

deep trench (FIG. 89, element 8970; para [0549]- In some cases, instead of a highly doped connecting well, a deep trench with oxide 8970 on its sidewalls and the center can have conducting silicide 8972 and/or metal as shown in FIG. 89);

and connecting electrodes (para [0456]- In some cases a metal connecting electrode can be formed from the surface to the P+ substrate via a trench (not shown) and in some cases a TSV (not shown) can be formed to the bottom anode metal).

W&WSens fails to disclose a CMOS image sensor wafer (CIS) (110) stacked to each other, the CMOS ASIC wafer is configured to receive the signals that the CIS wafer produces, wherein each pixel comprises an upper and a lower region of semiconductor material doped to opposite polarities (2534, 2536), and the microhole extending into the pixel; wherein the deep trench is a trench isolation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes; and pixel electrodes (154) coupled to said pixels, wherein connecting electrodes (152) coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Omnivision discloses a microstructure enhanced absorption photosensitive device (para [0002]-This invention is related to image sensors; para [0020]- each of the plurality of visible light pixels includes a photosensitive element, such as for example a photodiode, to receive a portion of light, and pixel support circuitry to generate a signal representative of an intensity of the received portion of light.) comprising: a CMOS ASIC wafer (para [0034]- Digital counter 480 may be implemented using CMOS circuitry disposed on the ASIC die fabricated using a standard CMOS process of the stacked die system) and a CMOS image sensor wafer (CIS) (FIG. 2, image sensor 200) stacked to each other (para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme) such that signals that the CIS wafer produces (para [0023]- In one example, each of the plurality of visible light pixels 211 includes a photosensitive element such as a photodiode to receive a portion of light, as well as pixel support circuitry to generate a signal representative of an intensity of the received portion of light.), wherein the CIS wafer comprises:

a layer (FIG. 5, semiconductor layer 510) in which an array of pixels is formed (para [0020]- For instance, in one example, an imaging system includes an image pixel array having a plurality of visible light pixels, and a plurality of silicon photon avalanche diode (SPAD) pixels; para [0038]- The illustrated example shows a plurality of visible light pixels, 502A, 502B, 502C and 502D, as well as a plurality of SPAD pixels 503A and 503B); (claim 16 continued)

--see next page

Form PCT/ISA/237 (Supplemental Box) (revised January 2019)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US 21/50717

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

---Supplemental Box - Box V.2 - Citations and Explanations---

(claim 16 continued) Omnivision fails to disclose the CMOS ASIC wafer is configured to receive and process signals; wherein each pixel comprises an upper and a lower region of semiconductor material doped to opposite polarities, a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; wherein the deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes; deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes; and pixel electrodes coupled to said pixels, connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Taiwan discloses a microstructure enhanced absorption photosensitive device (para [0017]- The present application is directed to a CMOS image sensor with elemental silicon and silicon germanium for long-wavelength pixel sensors; By arranging the photodetector in the silicon germanium layer, the photodetector advantageously has good sensitivity to and absorption of long-wavelength radiation, such as, for example, infrared radiation) comprising: a CMOS image sensor wafer (CIS) (FIG. 1, 100; para [0018]- With reference to FIG. 1, a cross-sectional view 100 of some embodiments of a CMOS image sensor with a semiconductor stack 102 of silicon and silicon germanium is provided.), wherein the CIS wafer comprises:

a layer in which an array of pixels is formed (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer); wherein each pixel comprises an upper (FIG. 2A, upper silicon layer 104; para [0023]- an upper silicon layer 104 a of the pair is arranged over and directly abuts the silicon germanium layer 106 a.) and a lower region of semiconductor material (FIG. 2A, lower silicon layer 204; para [0023]- Further, in some embodiments, a lower silicon layer 204 of the pair is arranged over and directly abuts the semiconductor substrate 202) doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204);

deep trench insulation (FIG. 1, deep trench isolation 112; para [0024]- The isolation region 112 is, for example, a shallow trench isolation (STI) region, a deep trench isolation (DTI) region, or an implant isolation region.) between adjacent pixels (para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region) in said array (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) and an electrically and optically isolating material in said deep trench insulation (para [0061]- In some embodiments, the process for forming the isolation region 112 comprises filling the trench with a dielectric material, such as silicon dioxide);

and pixel electrodes coupled to said pixels (Claim 21- wherein the transistor further comprises a gate electrode, a gate dielectric layer, and an additional source/drain region, wherein the gate dielectric layer spaces the gate electrode over the surface of the silicon layer);

Taiwan fails to disclose a CMOS ASIC wafer and a CMOS image sensor wafer (CIS) stacked to each other such that the CMOS ASIC wafer is configured to receive and process signals that the CIS wafer produces, wherein a region of semiconductor material to opposite polarities and a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; an electrically and optically isolating material in said microholes; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

None of the prior art discloses, the CMOS ASIC wafer is configured to receive signals; a region of semiconductor material to opposite polarities and the microhole extending into the pixel; an electrically and optically isolating material in said microholes; wherein connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular elements as required by claim 16, therefore claim 16 meets the criteria set out in PCT Article 33(2)-(3).

Claims 17-22 depend from claim 16, and therefore, meet the criteria set out in PCT Article 33(2)-(3) as well.

Claims 1-22 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used by industry.



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ELECTRONIC PAYMENT RECEIPT

APPLICATION #
18/822,880

RECEIPT DATE / TIME
09/03/2024 02:21:44 PM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	67016011	AUTHORIZED BY	Ivan Kavrukov
CUSTOMER #	139982	FILING DATE	-
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	SHIH-PING Wang

Payment Information

PAYMENT METHOD CARD / 2892	PAYMENT TRANSACTION ID E202493E23339898	PAYMENT AUTHORIZED BY Mary Ellen Finnegan
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PRE-AUTHORIZED ACCOUNT 600125	PRE-AUTHORIZED CATEGORY 37 CFR 1.21 (Miscellaneous fees and charges)
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FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
2111	UTILITY PATENT APPL. SEARCH FEE	280.00	1	280.00
4011	BASIC FILING FEE- UTILITY	64.00	1	64.00
2311	EXAMINATION OF ORIGINAL PATENT APPLICATION	320.00	1	320.00
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Doc code: IDS

PTO/SB/08a (02-18)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 11/30/2020. OMB 0651-0031

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	Filing Date		
	First Named Inventor	Shih-Yuan WANG	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	309-0015USCIPDIV	

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	11309444		2022-04-19	Wang et al.	
	2	8558336		2013-10-15	Su	
	3	10411053		2019-09-10	Yokogawa	
	4	10522582		2019-12-31	Maruyama et al.	
	5	9000492		2015-04-07	Suzuki et al.	
	6	6879014		2005-04-12	Wagner	
	7	7396696		2008-07-08	Kim	
	8	7525170		2009-04-28	Hsu	

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	First Named Inventor	Shih-Yuan WANG		
	Art Unit			
	Examiner Name			
	Attorney Docket Number	309-0015USCIPDIV		

	9	8129710		2012-03-06	Cho	
	10	8357960		2013-01-22	Dutta	
	11	8946675		2015-02-03	Yu	
	12	9184202		2015-11-10	Dutta	
	13	11211419		2021-12-28	Wu	
	14	11728457		2023-08-15	Sung	

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	1	20100320444		2010-12-23	Dutta	
	2	20110309331		2011-12-22	Yu et al.	
	3	20180182806		2018-06-28	Jin et al.	

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	First Named Inventor	Shih-Yuan WANG	
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	4	20110156195		2011-06-30	Tivarus et al.	
	5	20120153127		2012-06-21	Hirigoyen et al.	
	6	20180012918		2018-01-11	Na et al.	
	7	20190166317		2019-05-30	Tanaka et al.	
	8	20120012741		2012-01-19	Vasylyev	
	9	20180102442		2018-04-12	Wang	
	10	20160240579		2016-08-18	Sun et al.	
	11	20170141153		2017-05-18	Lee et al.	
	12	20180102442		2018-04-12	Wang et al.	
	13	20200006407		2020-01-02	Yokogawa	
	14	20200006416		2020-01-02	Baba et al.	

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	15	20050145779		2005-07-07	Mochizuki et al.	
	16	20120153416		2012-06-21	Tanaka et al.	

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	1	20080101301	KR		2008-11-21	Dongbu Hitek Co. Ltd.		☐
	2	2002314116	JP		2002-10-25	Seiko Epson Corp.		☐
	3	0103255	WO		2001-01-11	Scott		☐
	4	2019018846	WO		2019-01-24	W&W Sens Devices Inc.		☐
	5	09040854	EP		1999-09-08	IBM United Kingdom Limited		☐
	6	2007013065	JP		2007-01-18	Matsushita Electric Works Ltd.		☐
	7	103956403	CN		2017-02-15	Suzhou Beipeng Photoelectric Technology Co. Ltd.		☐

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	Attorney Docket Number	309-0015USCIPDIV	

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	1	Copy of International Search Report and Written Opinion for PCT/US2020/051733 mailed December 17, 2020.	☐
	2	Copy of Written Opinion of International Search Report for PCT/US2020/051733 dated December 17, 2020.	☐
	3	BEAUSOLEIL, Nanoelectronic and Nanophotonic Interconnect, The emerging integrated circuit interconnection bottleneck may be overcome if tiny, efficient photon-transport waveguides and small transceivers for photon-electron information exchange can be developed, 18 pages, January 29, 2007; revised September 25, 2007.	☐
	4	Copy of International Search Report and Written Opinion for PCT/US2021/050717 mailed December 6, 2021.	☐
	5	B. F. LEVIN et al., 1 Gb/s Si High Quantum Efficiency Monolithically Integrable, Applied Physics Letters, AIP Publishing LLC, Vol. 66, No. 22, May 29, 1995, Pages 2984-2986.	☐
	6	GAO YANG et al., Photon-trapping Microstructures Enable High-speed High-efficiency Silicon Photodiodes, Nature Photonics, Vol. 11, No. 5, April 3, 2017, Pages 301-308.	☐
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	Filing Date		
	First Named Inventor	Shih-Yuan WANG	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	309-0015USCIPDIV	

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☐ See attached certification statement.			
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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.			
Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-09-03
Name/Print	Ivan S. Kavrukov	Registration Number	25,161
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Application Number	TBD
Filing Date	TBD
First Named Inventor	Shih-Yuan WANG
Title	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	309-0015USCIPDIV

SIGNATURE of Applicant or Patent Practitioner			
Signature	/Ivan S. Kavrukov/	Date (Optional)	
Name	Ivan S. Kavrukov	Registration Number	25,161
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W&WSens Devices, Inc.



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



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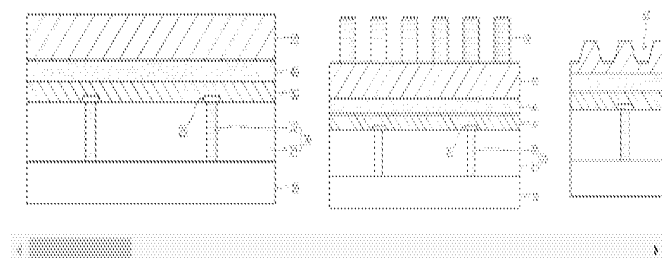


Image sensor and method for manufacturing thereof

Abstract

An image sensor and a manufacturing method thereof are provided to improve condensing rate and simplify its process while adopting a vertical photodiode of which resolution and sensitivity are improved. A CMOS(Complementary Metal Oxide Silicon) circuit is formed at a semiconductor circuit, and a metallic wiring layer which includes a metal wire and an inter insulation film is formed at a semiconductor substrate. A first conductivity type conductive layer is formed at the metallic wiring layer, and an intrinsic layer is formed at the first conductivity type conductive layer. A second conductivity type conductive layer(51) is formed at the intrinsic layer is formed at the intrinsic layer. At one or more than one layer of those three layers, the first conductivity conductive layer, the intrinsic layer and the second conductivity conductive layer, a concavo-convex part is formed.

Images (14)



Classifications

H01L27/14607 Geometry of the photosensitive area

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Claims (10)

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A semiconductor substrate on which a CMOS circuit is formed; A metal wiring layer including a metal wiring and an interlayer insulating film formed on the semiconductor substrate; A first conductivity type conductive layer formed on the metal wiring layer; An intrinsic layer formed on the first conductivity type conductive layer; And A second conductivity type conductive layer formed on the intrinsic layer, At least one of the first conductive type conductive layer, the intrinsic layer and the second conductive type conductive layer is an image sensor, characterized in that at least one uneven portion is formed on the upper surface. The method of claim 1, At least one trench is formed in any one of the first conductive conductive layer, the intrinsic layer and the second conductive conductive layer formed on the metal wiring. The method of claim 1, And an upper electrode and a color filter array formed on the second conductive conductive layer. The method of claim 1, And an adhesive layer formed between the upper electrode and the

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Other languages: Korean

Inventor: 심원만

Worldwide applications

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Application KR1020070047886A events [③](#)

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color filter array. The method of claim 4, wherein The adhesive layer is an image sensor, characterized in that formed of a thermal resin. Forming a metal wiring layer including a metal wiring and an interlayer insulating film on the semiconductor substrate on which the CMOS circuit is formed; Forming a first conductivity type conductive layer on the metallization layer; Forming an intrinsic layer on the first conductivity type conductive layer; And Forming a second conductivity type conductive layer on the intrinsic layer. At least one uneven portion is formed on an upper surface of any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer. The method of claim 6, Forming the uneven portion on the upper surface of any one of the first conductive conductive layer, the intrinsic layer and the second conductive conductive layer formed on the metal wiring, Forming at least one mask pattern on any one of the first conductivity type conductive layer and the intrinsic layer; And forming at least one trench on an upper surface of any one of the first conductive type conductive layer, the intrinsic layer, and the second conductive type conductive layer by using the mask pattern as an etching mask. The method of claim 7, wherein The trench is a method of manufacturing an image sensor, characterized in that formed by a dry etching method or a wet etching method. The method of claim 6, Forming an upper electrode on the second conductive conductive layer; And And forming a color filter array on the upper electrode. The method of claim 1, Forming an adhesive layer formed of a thermal resin on the upper electrode.

Description

translated from Korean

Image sensor and method for manufacturing thereof

1 to 5A are diagrams illustrating a manufacturing process of the image sensor of the first embodiment.

6 to 9 are diagrams illustrating a manufacturing process of the image sensor of the second embodiment.

10 to 13 are diagrams illustrating a manufacturing process of the image sensor of the third embodiment.

The embodiment discloses an image sensor and a method of manufacturing the same.

An image sensor is a semiconductor device that converts an optical image into an electrical signal, and is classified into a charge coupled device (CCD) image sensor and a complementary metal oxide silicon (CMOS) image sensor (CIS). do.

CCD image sensor has complex driving method, high power consumption, multi-stage photo process, and manufacturing process has complicated disadvantage. Therefore, as a next generation image sensor to overcome the disadvantage of the charge coupling device, CMOS image sensor is attracting attention.

The CMOS image sensor implements an image by sequentially detecting an electrical signal of each unit pixel by a switching method by forming a photodiode and a MOS transistor in the unit pixel.

This CMOS image sensor is simpler to drive than the CCD image sensor, which is widely used as a conventional image sensor, and can realize various scanning methods, and can integrate signal processing onto a single chip, thereby miniaturizing the product. The use of compatible CMOS technology reduces manufacturing costs and lowers power consumption.

The CMOS image sensor according to the related art may be divided into a photo diode region (not shown) that receives a light signal and converts the light signal into an electrical signal, and a transistor region (not shown) that processes the electrical signal.

However, the CMOS image sensor according to the related art has a structure in which a photodiode and a transistor are horizontally disposed on a semiconductor substrate.

Of course, although the disadvantages of the CCD image sensor have been solved by the horizontal CMOS image sensor according to the prior art, there are still problems in the horizontal CMOS image sensor according to the prior art.

That is, according to the horizontal CMOS image sensor according to the prior art, the photodiode and the transistor are formed adjacent to each other horizontally on the substrate. Accordingly, there is a need for an additional area for forming a photodiode, thereby reducing the fill factor area and limiting the possibility of resolution.

In addition, according to the horizontal CMOS image sensor according to the prior art there is a problem that it is very difficult to achieve the optimization for the process of manufacturing the photodiode and transistor at the same time. That is, in a fast transistor process, a shallow junction is required for low sheet resistance, but such a shallow junction may not be suitable for a photodiode.

In addition, according to the horizontal CMOS image sensor according to the prior art, the size of the unit pixel is increased or decreased to maintain the sensor sensitivity of the image sensor as additional on-chip functions are added to the image sensor. Should be.

However, when the pixel size is increased, the resolution of the image sensor is reduced, and the area of the photodiode decreases in the sensor sensitivity of the image sensor.

The embodiment provides an image sensor and a method of manufacturing the same that can provide new integration of transistor circuits and photodiodes.

The present invention also provides an image sensor and a method of manufacturing the same, in which resolution and sensor sensitivity can be improved together.

In addition, to provide an image sensor and a method of manufacturing the same that can achieve a light condensation rate and simplify the process while employing a vertical photodiode.

An image sensor according to an embodiment includes a semiconductor substrate on which a CMOS circuit is formed; A metal wiring layer including a metal wiring and an interlayer insulating film formed on the semiconductor substrate; A first conductivity type conductive layer formed on the metal wiring layer; An intrinsic layer formed on the first conductivity type conductive layer; And a second conductivity type conductive layer formed on the intrinsic layer, wherein any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer has at least one uneven portion formed thereon. It includes.

In addition, the manufacturing method of the image sensor according to the embodiment comprises the steps of: forming a metal wiring layer including a metal wiring and an interlayer insulating film on the semiconductor substrate on which the CMOS circuit is formed; Forming a first conductivity type conductive layer on the metallization layer; Forming an intrinsic layer on the first conductivity type conductive layer; And forming a second conductivity type conductive layer on the intrinsic layer, and forming an uneven portion on an upper surface of any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer. Steps.

Hereinafter, an image sensor and a method of manufacturing the same according to an embodiment will be described in detail with reference to the accompanying drawings.

In the description of the embodiments, where described as being formed "on / over" of each layer, the on / over may be directly or through another layer (indirectly) includes everything formed.

In the drawings, the thickness or size of each layer is exaggerated, omitted, or schematically illustrated for convenience and clarity of description. In addition, the size of each component does not necessarily reflect the actual size.

In addition, the same code / symbol was used about the same part in description of each Example.

<First Embodiment>

5A is a cross-sectional view of the image sensor according to the first embodiment.

5A, the image sensor of the embodiment includes a semiconductor substrate 10 on which a CMOS circuit is formed; A metal wiring layer 20 including a metal wiring 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 30 formed on the metal wiring layer 20; An intrinsic layer 40 formed on the first conductivity type conductive layer 30; And a second conductivity type conductive layer 51 having an uneven portion 53 formed on an upper surface of the intrinsic layer 40.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 51.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A plurality of trenches 52 may be formed in the second conductive layer 51 so that the upper surface of the second conductive layer 51 may have an uneven portion 53 having a plurality of uneven shapes. .

Alternatively, as illustrated in FIG. 5B, one uneven portion 53b may be formed in the second conductive layer 51b connected to the metal wire 22 to form one pixel.

As shown in FIGS. 5A and 5B, the photodiode formed on the metal wire 25 connected to the CMOS circuit (not shown) is formed to have at least one uneven portion.

Therefore, since the photodiode having at least one uneven portion is formed in one pixel including the CMOS circuit and the photodiode, the area of the photodiode can be increased to increase the light sensing efficiency.

An image sensor according to an embodiment may provide vertical integration of a transistor circuit and a photodiode.

In addition, the fill factor can be approached to 100% by vertical integration of the transistor circuit and the photodiode.

In addition, the vertical integration can provide higher sensitivity at the same pixel size than the prior art.

In addition, each unit pixel can implement a more complex circuit without reducing the sensitivity.

In addition, the surface of the photodiode formed in the unit pixel is formed in a dome shape, so that the surface area per unit pixel is increased, so that the light receiving region of the photodiode is enlarged, thereby increasing the light efficiency.

In addition, the surface of the photodiode formed in the unit pixel is formed in the shape of a dome such as a micro lens to maximize the light collecting rate.

In addition, since the photodiode is formed in a shape similar to a lens, a separate microlens forming process may not be performed, thereby simplifying the process.

A method of manufacturing the image sensor of the first embodiment will be described with reference to FIGS. 1 to 5A.

Referring to FIG. 1, a metal wiring layer 20 including a metal wiring 22 and an interlayer insulating film 21 is formed on a semiconductor substrate 10 on which a CMOS circuit (not shown) is formed.

Although not illustrated, an isolation layer (not shown) defining an active region and a field region is formed in the semiconductor substrate 10, and the photoelectric charges received by the photodiodes connected to a photodiode described later to form a unit pixel are used as electrical signals. A CMOS circuit (not shown) may be formed of a transistor structure for changing the circuit into a transistor.

Although not shown, the metal wiring layer 20 may be formed of a plurality of layers to connect the power line or the signal line to the CMOS circuit.

The metal wiring layer 20 is formed of a plurality of metal wirings 22 formed through the interlayer insulating film 21 and the interlayer insulating film 21 on the semiconductor substrate 10.

For example, the interlayer insulating film 21 may be formed of an oxide film, and the metal wire 22 may be formed of various conductive materials including metal, alloy, or silicide, that is, aluminum, copper, cobalt, or tungsten. .

The lower electrode 25 may be formed on the metal wiring layer 20 to be electrically connected to the metal wiring 22. For example, the lower electrode 25 may be formed of metals such as Cr, Ti, TiW, and Ta. Of course, the lower electrode 25 may not be formed.

A metal pixel 22 connected to the CMOS circuit of the semiconductor substrate 10 may be formed on the interlayer insulating layer 21, and then a photodiode may be formed on the metal wiring layer 20 to form a unit pixel.

The photodiode is formed on the metal wiring layer 20 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used.

The pin diode is formed of a structure in which an n-type amorphous silicon layer, an intrinsic amorphous silicon layer, and a p-type amorphous silicon layer are bonded to each other. The performance of the photodiode is determined by the efficiency of converting it into electrical form by receiving external light and the total charge capacitance. The existing photodiode is depleted when heterojunction of PN, NP, NPN, PNP, etc. Although the charge is generated and stored in the region, the pin diode is a photodiode having a structure in which an intrinsic amorphous silicon layer, which is a pure semiconductor, is bonded between a p-type silicon layer and an n-type silicon layer. All of the intrinsic amorphous silicon layers formed therebetween become depletion regions, which is advantageous for generation and storage of charges.

As described above, in the exemplary embodiment, a pin diode is used as the photodiode, and the pin diode may have a structure of P-I-N or N-I-P. Particularly, in the embodiment, a pin structure having a PIN structure is used as an example, and the n-type amorphous silicon layer includes a first conductivity type conductive layer 30 and the intrinsic amorphous silicon layer. In this case, the intrinsic layer 40 and the p-type amorphous silicon layer are referred to as a second conductivity type conductive layer 50.

A method of forming the photodiode using the pin diode will be described below.

A first conductivity type conductive layer 30 is formed on the metal wiring layer 20. The first conductivity type conductive layer 30 may serve as the N layer of the P-I-N diode employed in the present embodiment. That is, the first conductivity type conductive layer 30 may be an N type conductivity type conductive layer, but is not limited thereto.

The first conductivity type conductive layer 30 may be formed using n-doped amorphous silicon doped with N-type impurities, but is not limited thereto.

That is, the first conductivity type conductive layer 30 is a-Si:H, a-SiGe:H, a-SiC, a-SiN: H or the like by adding germanium, carbon, nitrogen or oxygen to amorphous silicon. SiO: H or the like.

In addition, the first conductivity type conductive layer 30 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the first conductive layer 30 may be formed of amorphous silicon by PECVD by mixing PH_3 , P_2H_6 and the like with silane gas (SiH_4).

Next, an intrinsic layer 40 is formed on the first conductivity type conductive layer 30. The intrinsic layer 40 may serve as an I layer employed in the embodiment.

The intrinsic layer 40 may be formed using intrinsic amorphous silicon. The intrinsic layer 40 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the intrinsic layer 40 may be formed of amorphous silicon by PECVD using silane gas (SiH_4).

In addition, the intrinsic layer 40 is preferably formed to a thickness of about 10 to 1,000 times the thickness of the first conductive type conductive layer 30. This is because the thicker the intrinsic layer 40 is, the more the depletion region of the photodiode increases, which is advantageous for storing and generating a large amount of photocharges.

Next, a second conductivity type conductive layer 50 is formed on the intrinsic layer 40.

The second conductivity type conductive layer 50 may serve as a P layer of the P-I-N diode employed in the embodiment. That is, the second conductivity type conductive layer 50 may be a P type conductivity type conductive layer, but is not limited thereto.

For example, the second conductivity type conductive layer 50 may be formed using P-doped amorphous silicon, but is not limited thereto.

The second conductivity type conductive layer 50 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the second conductivity type conductive layer 50 may be formed of amorphous silicon by PECVD by mixing a gas such as BH_3 or B_2H_6 with silane gas (SiH_4).

As described above, since the circuit region formed on the semiconductor substrate 10 and the photodiode are vertically formed, the fill factor of the photodiode may approach 100%.

Referring to FIG. 2, a mask pattern 100 is formed on the second conductive conductive layer 50.

The mask pattern 100 is to form the second conductive conductive layer 50 in the form of irregularities. The mask pattern 100 is formed by applying and patterning a photoresist film.

At least one mask pattern 100 may be formed on the second conductive conductive layer 50 so that the upper surface of the second conductive conductive layer 50 has a step difference.

Referring to FIG. 3, the trench 52 is formed by etching the second conductive conductive layer 50 using the mask pattern 100 as an etch mask. Then, the concave-convex portion 53 of the concave-convex shape is formed on the upper surface of the second conductivity type conductive layer 51 by the trench 52.

The second conductive conductive layer 51 may be etched by a dry or wet etching process. In particular, the etching of the second conductivity type conductive layer 51 proceeds so that the intrinsic layer 40 under the second conductivity type conductive layer 51 is not exposed.

As described above, since the uneven portion 53 is formed on the upper surface of the second conductive conductive layer 51, the surface area of the second conductive conductive layer 51 is increased, and thus the light receiving area of the photodiode is increased. This can be extended to improve the light detection rate of the image sensor.

In addition, at least one convex dome-shaped lens is formed in one pixel by the concave-convex portion 53 of the second conductivity type conductive layer 51 to increase the light efficiency of the photodiode.

Referring to FIG. 4, the upper electrode 60 is formed on the second conductive type conductive layer 51 on which the uneven portion 52 is formed.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cadmium tin oxide (CTO).

By the shape of the uneven portion 53, the upper electrode 60 may also be formed in the uneven shape having a step.

Referring to FIG. 5A, an adhesive layer 70 and a color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

In the image sensor formed as described above, photodiodes having a plurality of dome shapes may be formed in one pixel, thereby improving light condensation.

Alternatively, as illustrated in FIG. 5B, one uneven portion 53b may be formed in the second conductive conductive layer 51b formed on the metal wiring 22.

As a result, the light receiving area is extended by the uneven shape of the photodiode, thereby increasing the photosensitive index.

Second Embodiment

9 is a sectional view of an image sensor according to a second embodiment.

The image sensor of the embodiment with reference to FIG. 9 includes: a semiconductor substrate 10 on which a CMOS circuit is formed; A metal wiring layer 20 including a plurality of metal wirings 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 31 having at least one uneven portion 33 formed on an upper surface of the metal wiring layer 20; An intrinsic layer 40 formed on the first conductivity type conductive layer 31; And a second conductivity type conductive layer 50 formed on the intrinsic layer 40.

At least one trench 32 may be formed in the first conductive conductive layer 31 so that one or more uneven portions 33 may be formed on an upper surface of the first conductive conductive layer 31.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive layer 50.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A manufacturing process of the image sensor of the second embodiment will be described with reference to FIGS. 6 to 9.

Referring to FIG. 6, a metal wiring layer 20 and a lower electrode 25 are formed on the semiconductor substrate 10.

Since the semiconductor substrate 10, the metallization layer 20, and the lower electrode 25 are the same as in the above-described first embodiment, description thereof will be omitted.

After forming the metal wiring 22 connected to the CMOS circuit of the semiconductor substrate 10 on the interlayer insulating film 21, a photodiode is formed on the metal wiring layer 20.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used. Since the photodiode used in the second embodiment is the same as the first embodiment, a detailed description thereof will be omitted and only the process sequence will be described.

A method of forming the photodiode using the pin diode will be described below.

After forming the first conductive layer 30 on the metal wiring layer 20, at least one mask pattern 100 is formed on the first conductive layer 30.

The mask pattern 100 is for forming the first conductivity type conductive layer 30 in the form of irregularities. The mask pattern 100 is formed by coating and patterning a photoresist film. At least one mask pattern 100 may be formed on the first conductivity type conductive layer 30 so that the upper surface of the first conductivity type conductive layer 30 has a step difference.

Referring to FIG. 7, the trench 32 is formed by etching the first conductive layer 30 using the mask pattern 100 as an etch mask. Then, the concave-convex portion 33 having the concave-convex shape is formed on the upper surface of the first conductivity type conductive layer 31 by the trench 32.

The first conductive layer 31 may be etched by a dry or wet etching process. In particular, the etching of the first conductivity type conductive layer 31 proceeds so that the metal wiring layer 20 positioned under the first conductivity type conductive layer 31 is not exposed.

Referring to FIG. 8, an intrinsic layer 40 and a second conductive layer 50 are sequentially formed on the first conductive layer 30.

Then, the intrinsic layer 40 formed along the upper surface of the first conductivity type conductive layer 31 has a stepped upper surface by the uneven portion 33 of the first conductivity type conductive layer 31. The second conductive layer 50 has a stepped upper surface by the intrinsic layer 40.

Therefore, the surface of the photodiode including the first conductive layer 31, the intrinsic layer 40, and the second conductive layer 50 is formed in an uneven shape to improve the light sensing rate due to the increase of the surface area. It becomes possible.

In addition, since the photodiode has a shape such as a convex lens, it is possible to improve the light collecting rate.

In addition, the photodiode may have at least one uneven portion per pixel to increase the light detection rate of the photodiode.

Referring to FIG. 9, an upper electrode 60 is formed on the second conductive layer 50.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cadmium tin oxide (CTO).

The adhesive layer 70 and the color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

Third Embodiment

13 is a sectional view of an image sensor according to a third embodiment.

The image sensor of the embodiment with reference to FIG. 13 includes a semiconductor substrate 10 having a CMOS circuit formed thereon; A metal wiring layer 20 including a plurality of metal wirings 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 30 formed on the metal wiring layer 20; An intrinsic layer 41 having at least one uneven portion 43 formed on an upper surface of the first conductive conductive layer 30; And a second conductivity type conductive layer 50 formed on the intrinsic layer 41.

At least one trench 42 may be formed in the intrinsic layer 41, and at least one uneven portion 43 may be formed on an upper surface of the intrinsic layer 41.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 50.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A manufacturing process of the image sensor of the second embodiment will be described with reference to FIGS. 10 to 13.

Referring to FIG. 10, a metal wiring layer 20 and a lower electrode 25 are formed on the semiconductor substrate 10.

Since the semiconductor substrate 10, the metallization layer 20, and the lower electrode 25 are the same as those of the first embodiment described above, description thereof will be omitted.

After forming the metal wiring 22 connected to the CMOS circuit of the semiconductor substrate 10 on the interlayer insulating film 21, a photodiode is formed on the metal wiring layer 20.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used. Since the photodiode used in the second embodiment is the same as the first embodiment, a detailed description thereof will be omitted and only the process sequence will be described.

A method of forming the photodiode using the pin diode will be described below.

The first conductivity type conductive layer 30 and the intrinsic layer 40 are sequentially formed on the metal wiring layer 20.

The mask pattern 100 is formed on the intrinsic layer 40.

The mask pattern 100 is for forming the intrinsic layer 40 in the form of irregularities. The mask pattern 100 is formed by applying and patterning a photoresist film. At least one mask pattern 100 may be formed on the intrinsic layer 40 so that the upper surface of the intrinsic layer 41 has a step.

Referring to FIG. 11, the trench 42 is formed by etching the intrinsic layer 40 using the mask pattern 100 as an etch mask. Then, the uneven portions 43 having the uneven shape are formed on the upper surface of the intrinsic layer 41 by the trench 42.

The intrinsic layer 41 may be etched by a dry or wet etching process. In particular, the etching of the intrinsic layer 41 proceeds so that the first conductivity type conductive layer 30 positioned below the intrinsic layer 41 is not exposed.

Referring to FIG. 12, a second conductivity type conductive layer 50 is formed on the intrinsic layer 41.

Then, in the second conductivity type conductive layer 50 formed along the upper surface of the intrinsic layer 41, the upper surface is stepped by the uneven portion 43 of the intrinsic layer 41.

Therefore, the surface of the photodiode including the first conductivity type conductive layer 30, the intrinsic layer 41, and the second conductivity type conductive layer 50 is formed in an uneven shape to improve the light sensing rate due to the increase of the surface area. It becomes possible.

In addition, since the photodiode has a shape such as a convex lens, it is possible to improve the light collecting rate.

Referring to FIG. 9, an upper electrode 60 is formed on the second conductivity type conductive layer 50.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cadmium tin oxide (CTO).

The adhesive layer 70 and the color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

The embodiments described above are not limited to the above-described embodiments and drawings, and it is to be understood that various changes, modifications, and changes can be made without departing from the technical spirit of the present embodiments. It will be obvious to those who have it.

According to the image sensor and the manufacturing method thereof according to the embodiment, it is possible to provide vertical integration of the transistor circuit and the photodiode.

In addition, the fill factor can be approached to 100% by vertical integration of the transistor circuit and the photodiode.

In addition, the vertical integration can provide higher sensitivity at the same pixel size than the prior art.

In addition, each unit pixel can implement a more complex circuit without reducing the sensitivity.

In addition, by adopting a vertical photodiode, insulation between unit pixels is secured, thereby preventing crosstalk between pixels and the like, thereby improving reliability of the image sensor.

In addition, in implementing the unit pixel of the photodiode, the light sensing ratio may be improved by increasing the surface area of the photodiode in the unit pixel.

Cited By (2)

In addition, the photodiode corresponding to the unit pixel may have a lens shape such as a convex lens, thereby improving the light condensing ratio.

Publication number	Priority date	Publication date	Assignee	Title
CN109728127A *	2017-10-30	2019-05-07	上海萝冀技术有限公司	Photodiode and forming method thereof, imaging sensor, fingerprint imaging mould group
US20210242354A1 *	2015-11-17	2021-08-05	W&Wsens Devices, Inc.	Microstructure enhanced absorption photosensitive devices
Family To Family Citations				

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Similar Documents

Publication	Publication Date	Title
KR100851756B1	2008-08-11	Image sensor and method for manufacturing thereof
KR100894391B1	2009-04-20	Image Sensor and Method for Manufacturing Thereof
KR100935771B1	2010-01-06	Image Sensor and Method for Manufacturing Thereof
KR100872719B1	2008-12-05	Image Sensor and Method for Manufacturing thereof
KR100913019B1	2009-08-20	Image Sensor and Method for Manufacturing Thereof
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KR100881276B1	2009-02-05	Image sensor and method for manufacturing thereof
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KR100872990B1	2008-12-08	Image Sensor and Method for Fabrication of the Same
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KR20080101301A	2008-11-21	Image sensor and method for manufacturing thereof
KR100924412B1	2009-10-29	Image Sensor and Method for Manufacturing Thereof
KR100935768B1	2010-01-06	Method for Manufacturing of Image Sensor
KR20090044117A	2009-05-07	Image sensor and method for manufacturing thereof

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
KR1020070047886A	2007-05-17	2007-05-17	Image sensor and method for manufacturing thereof

Applications Claiming Priority (1)

Application	Filing date	Title
KR1020070047886A	2007-05-17	image sensor and method for manufacturing thereof

Legal Events

Date	Code	Title	Description
2007-05-17	A201	Request for examination	
2008-04-15	E902	Notification of reason for refusal	
2008-10-20	E601	Decision to refuse application	

Concepts

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 manufacturing process		title,claims,abstract,description	20	0.000
 metal		claims,abstract,description	53	0.000
 metal		claims,abstract,description	53	0.000
 semiconductor		claims,abstract,description	28	0.000
 substrate		claims,abstract,description	26	0.000
 layer		claims,description	228	0.000
 adhesive		claims,description	21	0.000
 adhesive		claims,description	21	0.000
 interlayer		claims,description	14	0.000

▣ resin	claims,description	8	0.000
▣ resin	claims,description	8	0.000
▣ etching	claims,description	7	0.000
▣ dry etching	claims,description	4	0.000
▣ metallisation	claims,description	4	0.000
▣ wet etching	claims,description	4	0.000
▣ method	abstract,description	16	0.000
▣ sensitivity	abstract,description	8	0.000
▣ silicon	abstract,description	4	0.000
▣ silicon	abstract,description	4	0.000
▣ complement	abstract,description	2	0.000
▣ insulation	abstract,description	2	0.000
▣ metal oxide	abstract,description	2	0.000
▣ metal oxides	abstract,description	2	0.000
Show all concepts from the description section			

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(74) 대리인

허용록

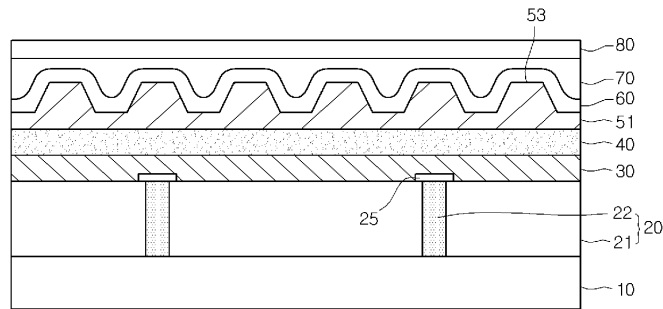
전체 청구항 수 : 총 10 항

(54) 이미지 센서 및 그의 제조방법

(57) 요약

실시예는 이미지 센서에 관한 것으로, 씨모스 회로가 형성된 반도체 기판; 상기 반도체 기판 상에 형성된 금속배선 및 중간절연막을 포함하는 금속배선층; 상기 금속배선층 상에 형성된 제1 도전형 전도층; 상기 제1 도전형 전도층 상에 형성된 진성층; 및 상기 진성층 상에 상부 표면에 적어도 하나 이상의 요철부가 형성된 제2 도전형 전도층을 포함한다.

도 5a - 도5a



특허청구의 범위

청구항 1

씨모스 회로가 형성된 반도체 기판;

상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층;

상기 금속배선층 상에 형성된 제1 도전형 전도층;

상기 제1 도전형 전도층 상에 형성된 진성층; 및

상기 진성층 상에 형성된 제2 도전형 전도층을 포함하며,

상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층은 그 상부 표면에 적어도 하나 이상의 요철부가 형성된 것을 특징으로 하는 이미지 센서.

청구항 2

제1항에 있어서,

상기 금속배선 상에 형성된 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층에는 적어도 하나 이상의 트랜치가 형성된 것을 포함하는 이미지 센서.

청구항 3

제1항에 있어서,

상기 제2 도전형 전도층 상부에는 상부전극 및 컬러필터 어레이가 형성된 것을 포함하는 이미지 센서.

청구항 4

제1항에 있어서,

상기 상부전극과 컬러필터 어레이 사이에는 접착층이 형성된 것을 포함하는 이미지 센서.

청구항 5

제4항에 있어서,

상기 접착층은 열 수지로 형성된 것을 특징으로 하는 이미지 센서.

청구항 6

씨모스 회로가 형성된 반도체 기판 상에 금속배선 및 층간절연막을 포함하는 금속배선층을 형성하는 단계;

상기 금속배선층 상에 제1 도전형 전도층을 형성하는 단계;

상기 제1 도전형 전도층 상에 진성층을 형성하는 단계; 및

상기 진성층 상에 제2 도전형 전도층을 형성하는 단계를 포함하며,

상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부 표면에는 적어도 하나 이상의 요철부가 형성되는 단계를 포함하는 이미지 센서의 제조방법.

청구항 7

제6항에 있어서,

상기 금속배선 상에 형성된 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부표면에 요철부를 형성하는 단계는,

상기 제1 도전형 전도층, 진성층 중 어느 하나의 층 상에 적어도 하나 이상의 마스크 패턴을 형성하는 단계;

상기 마스크 패턴을 식각 마스크로 하여 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의

층 상부 표면에 적어도 하나 이상의 트렌치를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 8

제7항에 있어서,

상기 트렌치는 건식식각 또는 습식식각 방법으로 형성된 것을 특징으로 하는 이미지 센서의 제조방법.

청구항 9

제6항에 있어서,

상기 제2 도전층 전도층 상에 상부전극을 형성하는 단계; 및

상기 상부전극 상에 컬러필터 어레이를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 10

제1항에 있어서,

상기 상부전극 상에 열 수지로 형성된 접착층을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

명세서

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

- <4> 실시예는 이미지 센서 및 그의 제조방법을 개시한다.
- <5> 이미지 센서는 광학적 영상(Optical Image)을 전기 신호로 변환시키는 반도체 소자로서, 크게 전하결합소자(charge coupled device:CCD) 이미지 센서와 씨모스(Complementary Metal Oxide Silicon:CMOS) 이미지 센서(CIS)로 구분된다.
- <6> CCD 이미지 센서는 구동방식이 복잡하고, 전력소비가 클 뿐만 아니라, 다단계의 포토공정이 요구되므로 제조공정이 복잡한 단점을 갖고 있으므로, 최근에는 상기 전하결합소자의 단점을 극복하기 위한 차세대 이미지 센서로서 씨모스 이미지 센서가 주목을 받고 있다.
- <7> 씨모스 이미지 센서는 단위 화소 내에 포토다이오드와 모스트랜지스터를 형성시킴으로써 스위칭 방식으로 각 단위 화소의 전기적 신호를 순차적으로 검출하여 영상을 구현한다.
- <8> 이러한 씨모스 이미지 센서는 종래 이미지 센서로 널리 사용되고 있는 CCD 이미지 센서에 비하여 구동방식이 간단하고 다양한 스캐닝 방식의 구현이 가능하며, 신호처리를 단일칩에 집적할 수 있어 제품의 소형화가 가능할 뿐만 아니라, 호환성의 씨모스 기술을 사용하므로 제조단가를 낮출 수 있고, 전력 소모 또한 낮다는 장점을 지니고 있다.
- <9> 종래기술에 의한 씨모스 이미지 센서는 빛 신호를 받아서 전기신호로 바꾸어 주는 포토다이오드(Photo diode) 영역(미도시)과 이 전기 신호를 처리하는 트랜지스터 영역(미도시)으로 구분할 수 있다.
- <10> 그런데 종래기술에 따른 씨모스 이미지 센서는 포토다이오드와 트랜지스터가 반도체 기판에 수평으로 배치되는 구조이다.
- <11> 물론, 종래기술에 의한 수평형 씨모스 이미지 센서에 의해 CCD 이미지 센서의 단점이 해결되기는 하였으나, 종래기술에 의한 수평형 씨모스 이미지 센서에는 여전히 문제점들이 있다.
- <12> 즉, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 포토다이오드와 트랜지스터가 기판 상에 상호 수평으로 인접하여 형성된다. 이에 따라, 포토다이오드 형성을 위한 추가적인 영역이 요구되며, 이에 의해 필 팩터(fill factor) 영역을 감소시키고 레졸루션(Resolution)의 가능성을 제한하는 문제가 있다.
- <13> 또한, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 포토다이오드와 트랜지스터를 동시에 제조하는 공

정에 대한 최적화를 달성하는 점이 매우 어려운 문제가 있다. 즉, 신속한 트랜지스터 공정에서는 작은 면저항 (low sheet resistance)을 위해 쉘로우 정션(shallow junction)이 요구되나, 포토다이오드에는 이러한 쉘로우 정션(shallow junction)이 적절하지 않을 수 있다.

- <14> 또한, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 추가적인 온칩(on-chip) 기능들이 이미지 센서에 부가되면서 단위화소의 크기가 이미지 센서의 센서티버티(sensitivity)를 유지하기 위해 증가되거나 또는 감소되어야 한다.
- <15> 그런데, 픽셀사이즈가 증가되면 이미지 센서의 레졸루션(Resolution)이 감소하게 되며, 또한 포토다이오드의 면적이 이미지 센서의 센서티버티(sensitivity)가 감소하는 문제가 발생한다.

발명이 이루고자 하는 기술적 과제

- <16> 실시예는 트랜지스터 회로와 포토다이오드의 새로운 집적을 제공할 수 있는 이미지 센서 및 그의 제조방법을 제공한다.
- <17> 또한, 레졸루션(Resolution)과 센서티버티(sensitivity)가 함께 개선될 수 있는 이미지 센서 및 그의 제조방법을 제공한다.
- <18> 또한, 수직형의 포토다이오드를 채용하면서 집광률 향상과 동시에 공정 단순화를 이룰 수 있는 이미지 센서 및 그의 제조방법을 제공하고자 한다.

발명의 구성 및 작용

- <19> 실시예에 따른 이미지 센서는, 씨모스 회로가 형성된 반도체 기판; 상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층; 상기 금속배선층 상에 형성된 제1 도전형 전도층; 상기 제1 도전형 전도층 상에 형성된 진성층; 및 상기 진성층 상에 형성된 제2 도전형 전도층을 포함하고, 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층은 그 상부 표면에 적어도 하나 이상의 요철부가 형성된 것을 포함한다.
- <20> 또한, 실시예에 따른 이미지 센서의 제조방법은, 씨모스 회로가 형성된 반도체 기판 상에 금속배선 및 층간절연막을 포함하는 금속배선층을 형성하는 단계; 상기 금속배선층 상에 제1 도전형 전도층을 형성하는 단계; 상기 제1 도전형 전도층 상에 진성층을 형성하는 단계; 및 상기 진성층 상에 제2 도전형 전도층을 형성하는 단계를 포함하며, 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부 표면에 요철부를 형성하는 단계를 포함한다.
- <21> 이하, 실시예에 따른 이미지 센서 및 그의 제조방법을 첨부된 도면을 참조하여 상세히 설명한다.
- <22> 실시예의 설명에 있어서, 각 층의 "상/위(on/over)"에 형성되는 것으로 기재되는 경우에 있어, 상/위(on/over)는 직접(directly)와 또는 다른 층을 개재하여(indirectly) 형성되는 것을 모두 포함한다.
- <23> 도면에서 각층의 두께나 크기는 설명의 편의 및 명확성을 위하여 과장되거나 생략되거나 또는 개략적으로 도시되었다. 또한 각 구성요소의 크기는 실제크기를 전적으로 반영하는 것은 아니다.
- <24> 또한, 각 실시예의 설명에 있어서 동일한 부분에 대하여 동일한 부호를 사용하였다.
- <25> <제1 실시예>
- <26> 도 5a는 제1 실시예에 따른 이미지 센서의 단면도이다.
- <27> 도 5a를 참조하여, 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 형성된 제1 도전형 전도층(30); 상기 제1 도전형 전도층(30) 상에 형성된 진성층(40); 및 상기 진성층(40) 상에 상부표면에 요철부(53)가 형성된 제2 도전형 전도층(51)을 포함한다.
- <28> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.
- <29> 상기 제2 도전형 전도층(51) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.
- <30> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다.

- <31> 상기 제2 도전형 전도층(51)에는 복수개의 트렌치(52)가 형성되어 상기 제2 도전형 전도층(51)의 상부표면은 복수개의 요철형상을 갖는 요철부(53)가 형성될 수 있다.
- <32> 또는, 도 5b에 도시된 바와 같이 상기 금속배선(22)과 연결되어 하나의 픽셀을 이루는 상기 제2 도전형 전도층(51b)에는 하나의 요철부(53b)가 형성될 수 있다.
- <33> 도 5a 및 도 5b에 도시된 바와 같이, 씨모스 회로(미도시)와 연결되는 금속배선(25) 상에 형성된 포토다이오드가 적어도 하나 이상의 요철부를 가지도록 형성된다.
- <34> 따라서, 씨모스 회로와 포토다이오드로 이루어지는 하나의 픽셀에 적어도 하나 이상의 요철부를 갖는 포토다이오드가 형성되므로써 상기 포토다이오드의 면적이 증가되어 광감지 효율을 증가시킬 수 있다.
- <35> 실시예에 따른 이미지 센서는 트랜지스터 회로와 포토다이오드의 수직형 집적을 제공할 수 있다.
- <36> 또한, 트랜지스터 회로와 포토다이오드의 수직형 집적에 의해 필 팩터(fill factor)를 100%에 근접시킬 수 있다.
- <37> 또한, 수직형 집적에 의해 종래기술보다 같은 픽셀 사이즈에서 높은 센서티비티(sensitivity)를 제공할 수 있다.
- <38> 또한, 각 단위 픽셀은 센서티비티(sensitivity)의 감소없이 보다 복잡한 회로를 구현할 수 있다.
- <39> 또한, 단위 픽셀 내에 형성된 포토다이오드의 표면이 돔 형태로 형성되어 단위 픽셀 당 표면적이 증가하여 포토다이오드의 수광영역이 확대되어 광효율을 증가시킬 수 있다.
- <40> 또한, 단위 픽셀 내에 형성된 포토다이오드의 표면이 마이크로렌즈와 같은 돔형태로 형성되어 집광율을 극대화시킬 수 있다.
- <41> 또한, 상기 포토다이오드의 형태가 렌즈와 유사한 형태로 형성되어 별도의 마이크로렌즈 형성공정을 진행하지 않아도 되므로 공정을 단순화시킬 수 있다.
- <42> 도 1 내지 도 5a를 참조하여 제1 실시예의 이미지 센서의 제조방법을 설명한다.
- <43> 도 1을 참조하여, 씨모스 회로(미도시)가 형성된 반도체 기판(10) 상에는 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20)이 형성되어 있다.
- <44> 도시하지는 않았지만, 상기 반도체 기판(10)에는 액티브 영역 및 필드 영역을 정의하는 소자분리막(미도시)이 형성되어 있으며, 단위 픽셀을 형성하기 위해 후술되는 포토다이오드에 연결되어 수광된 광전하를 전기신호로 변화시키기 위한 트랜지스터 구조물로 이루어진 씨모스 회로(미도시)가 형성되어 있을 수 있다.
- <45> 도시하지는 않았지만, 상기 금속배선층(20)은 전원라인 또는 신호라인과 씨모스 회로를 접속시키기 위해 복수의 층으로 형성될 수 있다.
- <46> 상기 금속배선층(20)은 반도체 기판(10) 상에 층간절연막(21)과 상기 층간절연막(21)을 관통하여 형성되는 복수의 금속배선(22)으로 형성되어 있다.
- <47> 예를 들어, 상기 층간절연막(21)은 산화막으로 형성될 수 있으며, 상기 금속배선(22)은 금속, 합금 또는 실리사이드를 포함한 다양한 전도성 물질, 즉 알루미늄, 구리, 코발트 또는 텅스텐 등으로 형성할 수 있다.
- <48> 상기 금속배선층(20) 상에 상기 금속배선(22)과 전기적으로 연결되는 하부전극(25)을 형성할 수도 있다. 예를 들어, 상기 하부전극(25)은 Cr, Ti, TiW 및 Ta과 같은 금속으로 형성할 수 있다. 물론 상기 하부전극(25)은 형성되지 않을 수 있다.
- <49> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성하여 단위픽셀을 형성할 수 있다.
- <50> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다.
- <51> 상기 핀 다이오드는 n형 비정질 실리콘층(n-type amorphous silicon), 진성 비정질 실리콘층(intrinsic amorphous silicon), p형 비정질 실리콘층(p-type amorphous silicon)이 접합된 구조로 형성되는 것이다. 포토다이오드의 성능은 외부의 빛을 받아 전기적 형태로 전환하는 효율과 총 보관 가능 전하량(charge capacitanc

e)에 따라 결정되는 것으로 기존의 포토다이오드는 P-N, N-P, N-P-N, P-N-P 등의 이종접합시 생성되는 공핍영역(Depletion region)에 전하를 생성 및 보관하였으나, 상기 핀 다이오드는 p형 실리콘층과 n형 실리콘층 사이에 순수한 반도체인 진성 비정질 실리콘층이 접합된 구조의 광 다이오드로서, 상기 p형과 n형 사이에 형성되는 진성 비정질 실리콘층이 모두 공핍영역이 되어 전하의 생성 및 보관에 유리하게 된다.

- <52> 이와 같이 실시예에서는 포토다이오드로서 핀 다이오드를 사용하며 핀 다이오드의 구조는 P-I-N 또는 N-I-P의 구조로 형성될 수 있다. 특히, 실시예에서는 P-I-N 구조의 핀 다이오드가 사용되는 것을 예로 하며, 상기 n형 비정질 실리콘층(n-type amorphous silicon)은 제1 도전형 전도층(30), 상기 진성 비정질 실리콘층(intrinsic amorphous silicon)은 진성층(40), 상기 p형 비정질 실리콘층(p-type amorphous silicon)은 제2 도전형 전도층(50)이라 칭하도록 한다.
- <53> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.
- <54> 상기 금속배선층(20) 상에 제1 도전형 전도층(30)을 형성한다. 상기 제1 도전형 전도층(30)은 본 실시예에서 채용하는 P-I-N 다이오드의 N층의 역할을 할 수 있다. 즉, 상기 제1 도전형 전도층(30)은 N타입 도전형 전도층일 수 있으나 이에 한정되는 것은 아니다.
- <55> 상기 제1 도전형 전도층(30)은 N형 불순물이 도핑된 비정질 실리콘(n-doped amorphous silicon)을 이용하여 형성될 수 있으나, 이에 한정되는 것은 아니다.
- <56> 즉, 상기 제1 도전형 전도층(30)은 비정질 실리콘에 게르마늄, 탄소, 질소 또는 산소 등을 첨가하여 a-Si:H, a-SiGe:H, a-SiC, a-SiN:H a-SiO:H 등으로 형성될 수도 있다.
- <57> 또한, 상기 제1 도전형 전도층(30)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 제1 도전형 전도층(30)은 실란가스(SiH_4)에 PH_3 , P_2H_6 등을 혼합하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.
- <58> 그 다음, 상기 제1 도전형 전도층(30) 상으로 진성층(intrinsic layer)(40)을 형성한다. 상기 진성층(40)은 실시예에서 채용하는 I층의 역할을 할 수 있다.
- <59> 상기 진성층(40)은 비정질 실리콘(intrinsic amorphous silicon)을 이용하여 형성될 수 있다. 상기 진성층(40)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 진성층(40)은 실란가스(SiH_4) 등을 이용하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.
- <60> 또한, 상기 진성층(40)은 상기 제1 도전형 전도층(30)의 두께 보다 약 10~1,000배 정도의 두꺼운 두께로 형성하는 것이 바람직하다. 이는 상기 진성층(40)의 두께가 두꺼울수록 포토다이오드의 공핍영역이 늘어나 많은 양의 광전하를 보관 및 생성하기에 유리하기 때문이다.
- <61> 그 다음, 상기 진성층(40) 상으로 제2 도전형 전도층(50)을 형성한다.
- <62> 상기 제2 도전형 전도층(50)은 실시예에서 채용하는 P-I-N 다이오드의 P층의 역할을 할 수 있다. 즉, 상기 제2 도전형 전도층(50)은 P 타입 도전형 전도층일 수 있으나 이에 한정되는 것은 아니다.
- <63> 예를 들어, 상기 제2 도전형 전도층(50)은 P 도핑된 비정질 실리콘(p-doped amorphous silicon)을 이용하여 형성될 수 있으나, 이에 한정되는 것은 아니다.
- <64> 상기 제2 도전형 전도층(50)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 제2 도전형 전도층(50)은 실란가스(SiH_4)에 BH_3 또는 B_2H_6 등의 가스를 혼합하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.
- <65> 상기과 같이 반도체 기판(10)에 형성된 회로영역과 포토다이오드가 수직형으로 형성됨으로써 포토다이오드의 필 팩터(fill factor)를 100%에 근접시킬 수 있다.
- <66> 도 2를 참조하여, 상기 제2 도전형 전도층(50) 상부로 마스크 패턴(100)을 형성한다.
- <67> 상기 마스크 패턴(100)은 상기 제2 도전형 전도층(50)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다.
- <68> 상기 마스크 패턴(100)은 상기 제2 도전형 전도층(50) 상에 적어도 하나 이상 형성되어 상기 제2 도전형 전도층(50)의 상부 표면이 단차를 가지도록 형성할 수 있다.

- <69> 도 3을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 제2 도전형 전도층(50)을 식각하여 트렌치(52)를 형성한다. 그러면 상기 트렌치(52)에 의해 상기 제2 도전형 전도층(51)의 상부 표면은 요철형태의 요철부(53)가 형성된다.
- <70> 상기 제2 도전형 전도층(51)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 제2 도전형 전도층(51)의 식각은 상기 제2 도전형 전도층(51) 하부에 위치한 진성층(40)이 노출되지 않도록 진행한다.
- <71> 상기와 같이, 상기 제2 도전형 전도층(51)의 상부 표면에 요철부(53)가 형성됨으로써 상기 제2 도전형 전도층(51)의 표면적은 증가하게 되고, 이로 인해 포토다이오드의 수광영역이 확장되어 이미지 센서의 광감지율을 향상시킬 수 있다.
- <72> 또한, 상기 제2 도전형 전도층(51)의 요철부(53)에 의하여 하나의 픽셀 내에 볼록한 돔 형태의 렌즈가 적어도 하나 이상 형성되어 포토다이오드의 광 효율을 증가시킬 수 있다.
- <73> 도 4를 참조하여, 상기 요철부(52)가 형성된 제2 도전형 전도층(51)의 상부로 상부전극(60)을 형성한다.
- <74> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.
- <75> 상기 요철부(53)의 형태에 의하여 상기 상부전극(60)도 단차를 가지는 요철형태로 형성될 수 있다.
- <76> 도 5a를 참조하여, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.
- <77> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.
- <78> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.
- <79> 상기와 같이 형성된 이미지 센서는 하나의 픽셀 내에 복수의 돔형태를 갖는 포토다이오드가 형성되어 집광율을 향상시킬 수 있다.
- <80> 또는 도 5b에 도시된 바와 같이, 상기 금속배선(22) 상에 형성된 제2 도전형 전도층(51b)에 하나의 요철부(53b)가 형성될 수 있다.
- <81> 그러면 상기 포토다이오드의 요철형태에 의하여 수광면적이 확장되어 감광지율을 높일 수 있다.
- <82> <제2 실시예>
- <83> 도 9는 제2 실시예에 따른 이미지 센서의 단면도이다.
- <84> 도 9를 참조하여 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 복수의 금속배선(22) 및 중간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 상부표면에 적어도 하나 이상의 요철부(33)가 형성된 제1 도전형 전도층(31); 상기 제1 도전형 전도층(31) 상에 형성된 진성층(40); 및 상기 진성층(40) 상에 형성된 제2 도전형 전도층(50)을 포함한다.
- <85> 상기 제1 도전형 전도층(31)에는 적어도 하나 이상의 트렌치(32)가 형성되어 상기 제1 도전형 전도층(31)의 상부표면은 하나 이상의 요철부(33)가 형성될 수 있다.
- <86> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.
- <87> 상기 제2 도전형 전도층(50) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.
- <88> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다
- <89> 도 6 내지 도 9를 참조하여 제2 실시예의 이미지 센서의 제조공정을 설명한다.
- <90> 도 6을 참조하여, 반도체 기판(10) 상에는 금속배선층(20) 및 하부전극(25)이 형성되어 있다.
- <91> 상기 반도체 기판(10), 금속배선층(20) 및 하부전극(25)은 상술된 제1 실시예와 동일하므로 이에 대한 설명은 생략하기로 한다.
- <92> 상기 중간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성한다.

- <93> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다. 제2 실시예에서 사용되는 포토다이오드는 제1 실시예와 동일하므로 이에 대한 구체적인 설명은 생략하고 공정순서에 대해서만 설명하도록 한다.
- <94> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.
- <95> 상기 금속배선층(20) 상에 제1 도전형 전도층(30)을 형성한 후, 상기 제1 도전형 전도층(30) 상부로 적어도 하나 이상의 마스크 패턴(100)을 형성한다.
- <96> 상기 마스크 패턴(100)은 상기 제1 도전형 전도층(30)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다. 상기 마스크 패턴(100)은 상기 제1 도전형 전도층(30) 상에 적어도 하나 이상 형성되어 상기 제1 도전형 전도층(30)의 상부 표면이 단차를 가지도록 형성할 수 있다.
- <97> 도 7을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 제1 도전형 전도층(30)을 식각하여 트렌치(32)를 형성한다. 그러면 상기 트렌치(32)에 의해 상기 제1 도전형 전도층(31)의 상부 표면에는 요철형태의 요철부(33)가 형성된다.
- <98> 상기 제1 도전형 전도층(31)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 제1 도전형 전도층(31)의 식각은 상기 제1 도전형 전도층(31) 하부에 위치한 금속배선층(20)이 노출되지 않도록 진행한다.
- <99> 도 8을 참조하여, 상기 제1 도전형 전도층(30) 상으로 진성층(intrinsic layer)(40) 및 제2 도전형 전도층(50)을 순차적으로 형성한다.
- <100> 그러면, 상기 제1 도전형 전도층(31)의 상부 표면을 따라 형성되는 상기 진성층(40)은 상기 제1 도전형 전도층(31)의 요철부(33)에 의해 상부 표면이 단차를 가지게 되고, 상기 제2 도전형 전도층(50)은 상기 진성층(40)에 의해 상부 표면이 단차를 가지게 된다.
- <101> 따라서, 상기 제1 도전형 전도층(31), 진성층(40) 및 제2 도전형 전도층(50)으로 이루어지는 포토다이오드의 표면은 요철형태로 형성되어 표면적 증가로 인하여 광감지율을 향상시킬 수 있게 된다.
- <102> 또한, 상기 포토다이오드의 형태가 볼록렌즈와 같은 형태를 가지게 되므로 집광율을 향상시킬 수 있게 된다.
- <103> 또한, 상기 포토다이오드는 하나의 픽셀당 적어도 하나 이상의 요철부가 형성되어 포토다이오드의 광감지율을 높일 수 있다.
- <104> 도 9를 참조하여, 상기 제2 도전형 전도층(50)의 상부로 상부전극(60)을 형성한다.
- <105> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.
- <106> 그리고, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.
- <107> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.
- <108> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.
- <109> <제3 실시예>
- <110> 도 13은 제3 실시예에 따른 이미지 센서의 단면도이다.
- <111> 도 13을 참조하여 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 복수의 금속배선(22) 및 중간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 형성된 제1 도전형 전도층(30); 상기 제1 도전형 전도층(30) 상에 상부표면에 적어도 하나 이상의 요철부(43)가 형성된 진성층(41); 및 상기 진성층(41) 상에 형성된 제2 도전형 전도층(50)을 포함한다.
- <112> 상기 진성층(41)에는 적어도 하나 이상의 트렌치(42)가 형성되어 상기 진성층(41)의 상부표면은 적어도 하나 이상의 요철부(43)가 형성될 수 있다.
- <113> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.
- <114> 상기 제2 도전형 전도층(50) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.

- <115> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다
- <116> 도 10 내지 도 13을 참조하여 제2 실시예의 이미지 센서의 제조공정을 설명한다.
- <117> 도 10을 참조하여, 반도체 기판(10) 상에는 금속배선층(20) 및 하부전극(25)이 형성되어 있다.
- <118> 상기 반도체 기판(10), 금속배선층(20) 및 하부전극(25)은 상술된 제1 실시예와 동일하므로 이에 대한 설명은 생략하기로 한다.
- <119> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성한다.
- <120> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다. 제2 실시예에서 사용되는 포토다이오드는 제1 실시예와 동일하므로 이에 대한 구체적인 설명은 생략하고 공정순서에 대해서만 설명하도록 한다.
- <121> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.
- <122> 상기 금속배선층(20) 상에 제1 도전형 전도층(30) 및 진성층(40)을 순차적으로 형성한다.
- <123> 상기 진성층(40) 상으로 상부로 마스크 패턴(100)을 형성한다.
- <124> 상기 마스크 패턴(100)은 상기 진성층(40)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다. 상기 마스크 패턴(100)은 상기 진성층(40) 상에 적어도 하나 이상 형성되어 상기 진성층(41)의 상부 표면이 단차를 가지도록 형성할 수 있다.
- <125> 도 11을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 진성층(40)을 식각하여 트렌치(42)를 형성한다. 그러면 상기 트렌치(42)에 의해 상기 진성층(41)의 상부 표면에는 요철형태의 요철부(43)가 형성된다.
- <126> 상기 진성층(41)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 진성층(41)의 식각은 상기 진성층(41) 하부에 위치한 제1 도전형 전도층(30)이 노출되지 않도록 진행한다.
- <127> 도 12를 참조하여, 상기 진성층(41) 상으로 제2 도전형 전도층(50)을 형성한다.
- <128> 그러면, 상기 진성층(41)의 상부 표면을 따라 형성되는 상기 제2 도전형 전도층(50)은 상기 진성층(41)의 요철부(43)에 의해 상부 표면이 단차를 가지게 된다.
- <129> 따라서, 상기 제1 도전형 전도층(30), 진성층(41) 및 제2 도전형 전도층(50)으로 이루어지는 포토다이오드의 표면은 요철형태로 형성되어 표면적 증가로 인하여 광감지율을 향상시킬 수 있게 된다.
- <130> 또한, 상기 포토다이오드의 형태가 볼록렌즈와 같은 형태를 가지게 되므로 집광율을 향상시킬 수 있게 된다.
- <131> 도 9를 참조하여, 상기 제2 도전형 전도층(50)의 상부로 상부전극(60)을 형성한다.
- <132> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.
- <133> 그리고, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.
- <134> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.
- <135> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.
- <136> 이상에서 설명한 실시예는 전술한 실시예 및 도면에 한정되는 것이 아니고, 본 실시예의 기술적 사상을 벗어나지 않는 범위 내에서 여러 가지 치환, 변형 및 변경할 수 있다는 것은 본 실시예가 속하는 기술 분야에서 통상의 지식을 가진자에게 있어 명백할 것이다.

발명의 효과

- <137> 실시예에 따른 이미지 센서 및 그의 제조방법에 의하면 트랜지스터 회로와 포토다이오드의 수직형 집적을 제공할 수 있다.

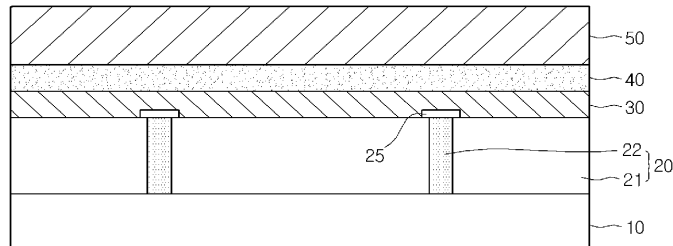
- <138> 또한, 트랜지스터 회로와 포토다이오드의 수직형 집적에 의해 필 팩터(fill factor)를 100%에 근접시킬 수 있다.
- <139> 또한, 수직형 집적에 의해 종래기술보다 같은 픽셀 사이즈에서 높은 센서티비티(sensitivity)를 제공할 수 있다.
- <140> 또한, 각 단위 픽셀은 센서티비티(sensitivity)의 감소없이 보다 복잡한 회로를 구현할 수 있다.
- <141> 또한, 수직형 포토다이오드를 채용하면서 단위 픽셀 간의 절연성을 확보함으로써 픽셀간의 크로스토크 등을 방지하여 이미지 센서의 신뢰성을 향상시킬 수 있다.
- <142> 또한, 포토다이오드의 단위픽셀을 구현함에 있어 단위 픽셀 내의 포토다이오드의 표면적을 증가시켜 광감지율을 향상시킬 수 있다.
- <143> 또한, 상기 단위픽셀에 해당하는 포토다이오드가 볼록렌즈와 같은 렌즈형태를 가지게 되어 집광율을 향상시킬 수 있다.

도면의 간단한 설명

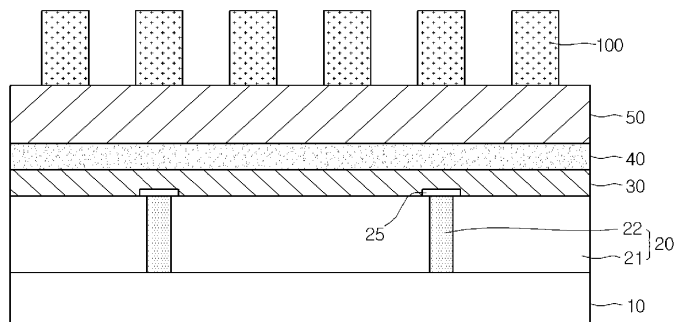
- <1> 도 1 내지 도 5a는 제1 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.
- <2> 도 6 내지 도 9는 제2 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.
- <3> 도 10 내지 도 13은 제3 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.

도면

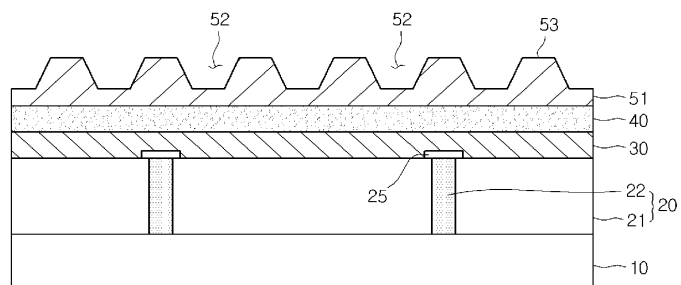
도면1



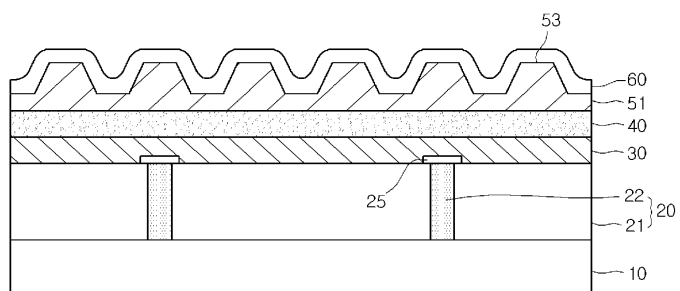
도면2



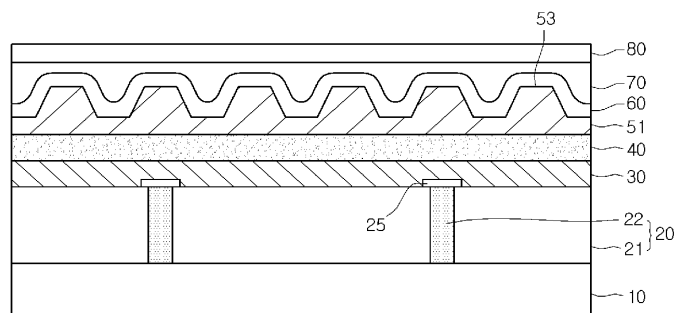
도면3



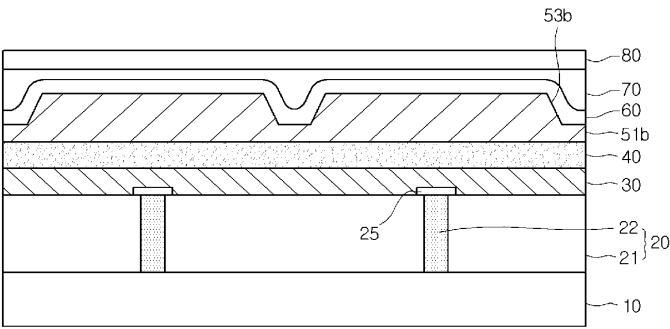
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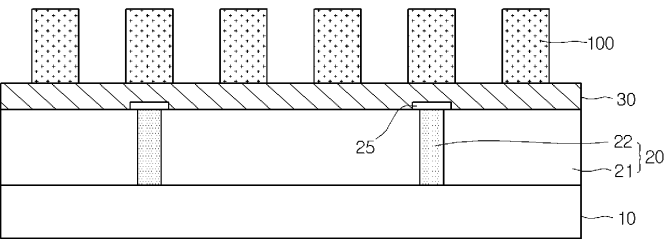
도면5a



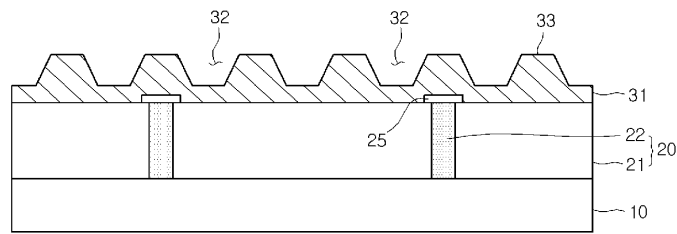
도면5b



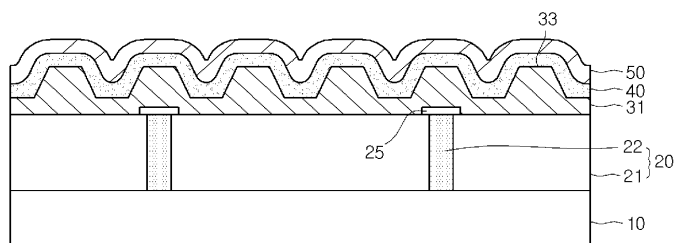
도면6



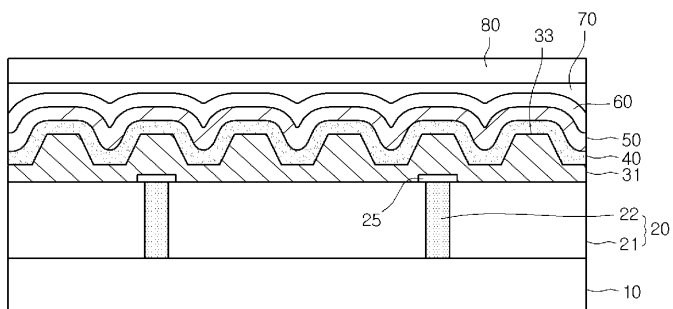
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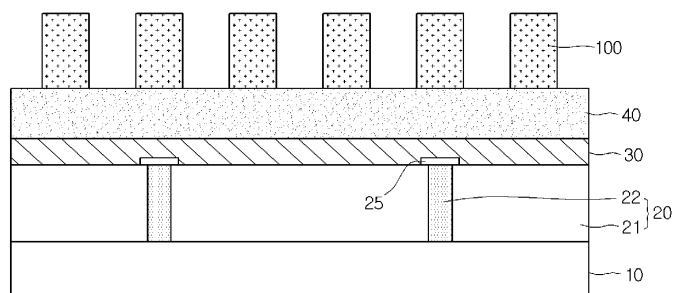
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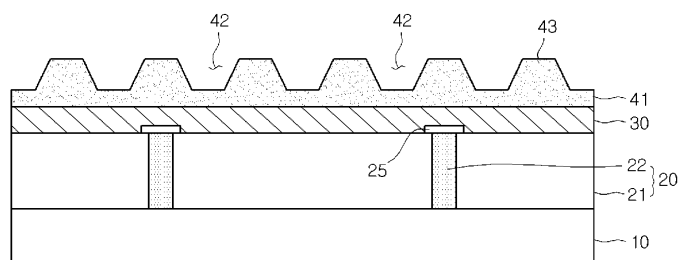
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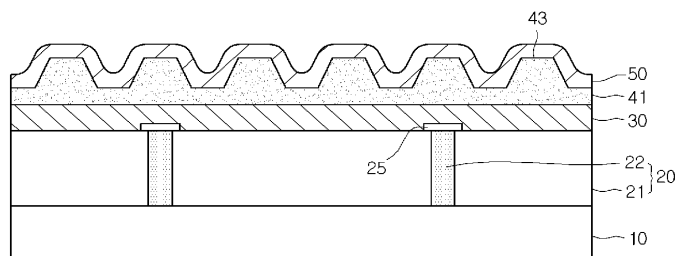
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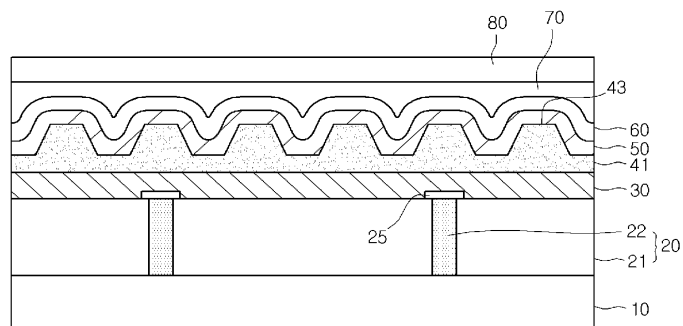
도면11



도면12



도면13



Attorney Docket No.: 309-0015USCIPDIV
Confirmation No.: TBD

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shih-Yuan WANG	Examiner: N/A
Application No.: TBD	Art Unit: N/A
Filed: TBD	CERTIFICATE OF TRANSMISSION
Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 /Mary Ellen Finnegan/ Date: September 3, 2024 Name: Mary Ellen Finnegan

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Alexandria, VA 22313-1450

SIR:

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

A copy of the non-U.S. patent document is enclosed herewith, in compliance with 37 CFR 1.98.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

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APPLICATION #
18/822,880

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ATTORNEY DOCKET #
309-0015USCIPDIV

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	67016011	FILING DATE	-
CUSTOMER #	139982	FIRST NAMED INVENTOR	SHIH-PING Wang
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 27

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_ADS-- Final.pdf	37	Application Data Sheet	9377 KB
Warning: This is not a USPTO supplied ADS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.			
309-0015USCIPDIV_Transmittal OfPowerOfAttorney- Signed.pdf	2	Power of Attorney	649 KB
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309-0015USCIP_Declaration_Shi h-YuanWANG-signed.pdf	2	Oath or Declaration filed	176 KB

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KR20080101301A.pdf	26	Foreign Reference	782 KB
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CN103956403B.pdf	17	Foreign Reference	4311 KB
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309-0015USCIPDIV_Specification---Final.pdf	87	Auxiliary PDF of Application	449 KB

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DOCUMENT	MESSAGE DIGEST(SHA-512)
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

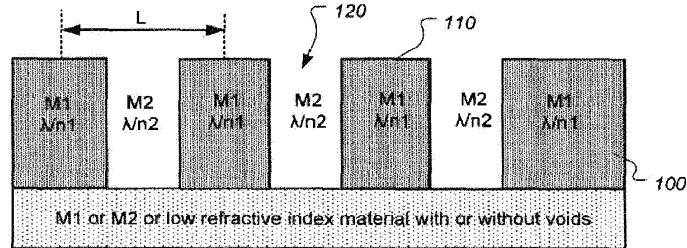


FIG. 1

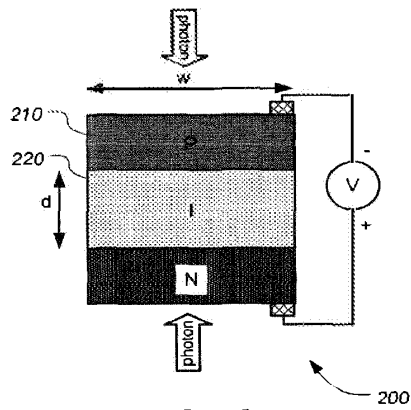


FIG. 2
(prior art)

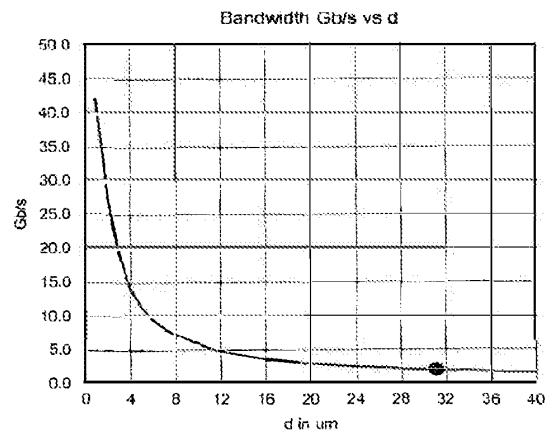


FIG. 3A
(prior art)

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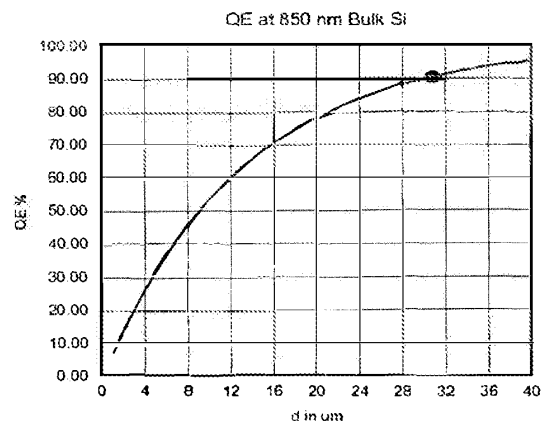
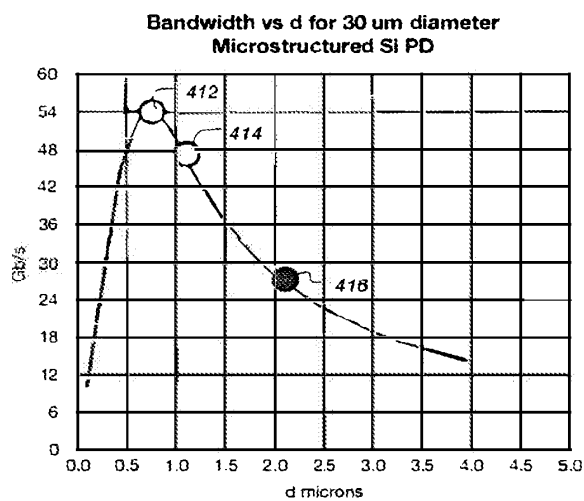
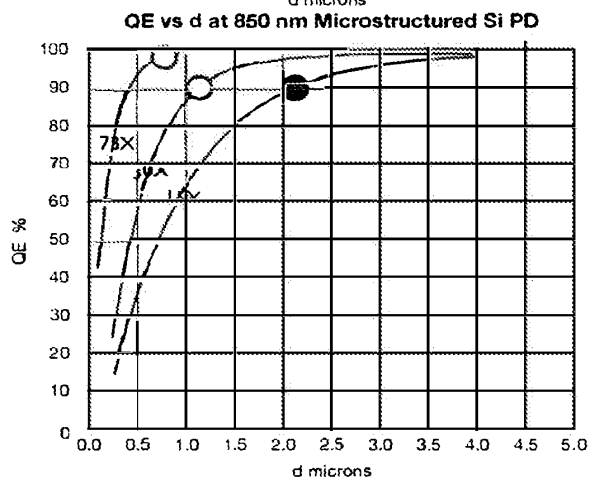
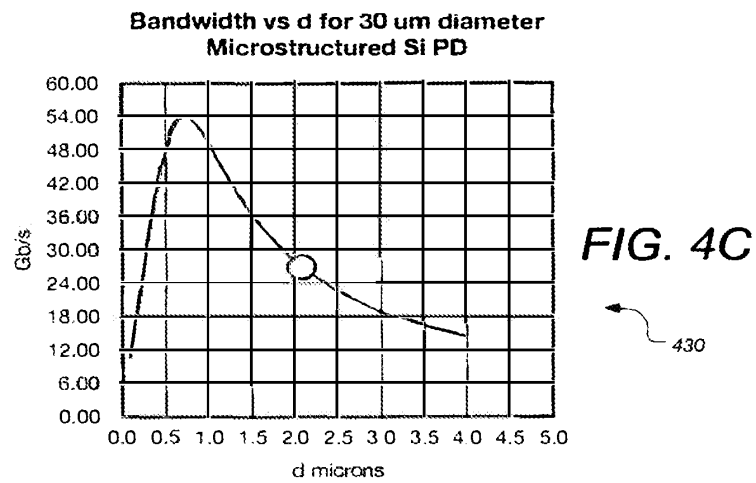
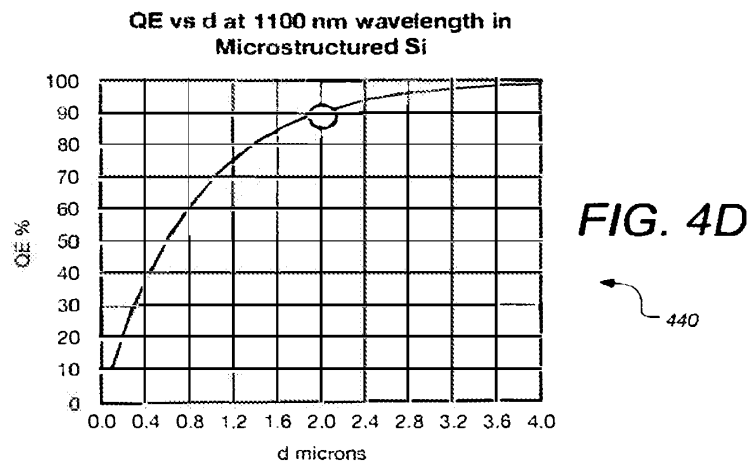


FIG. 3B
(prior art)

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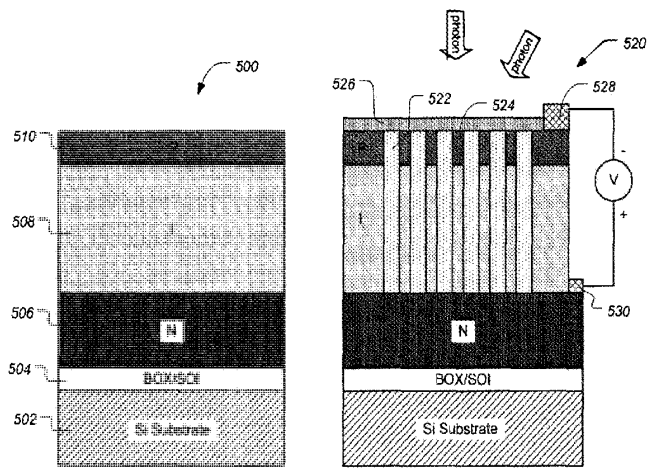


FIG. 5A

FIG. 5B

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309-00151-SCIP

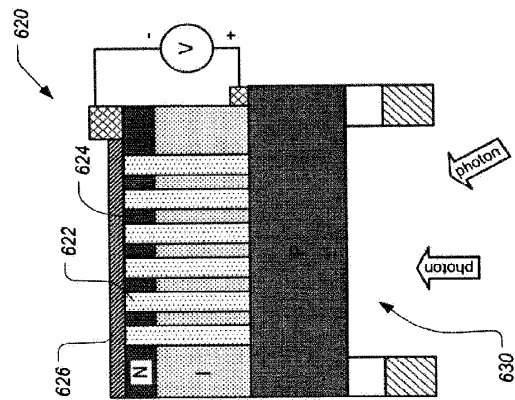


FIG. 6B

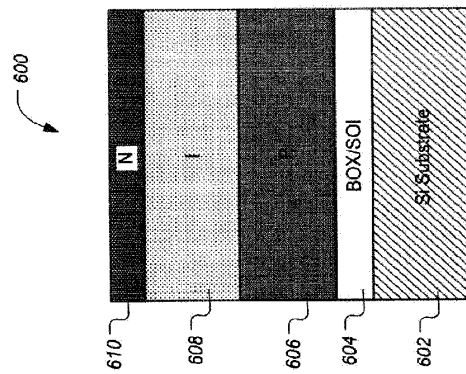


FIG. 6A

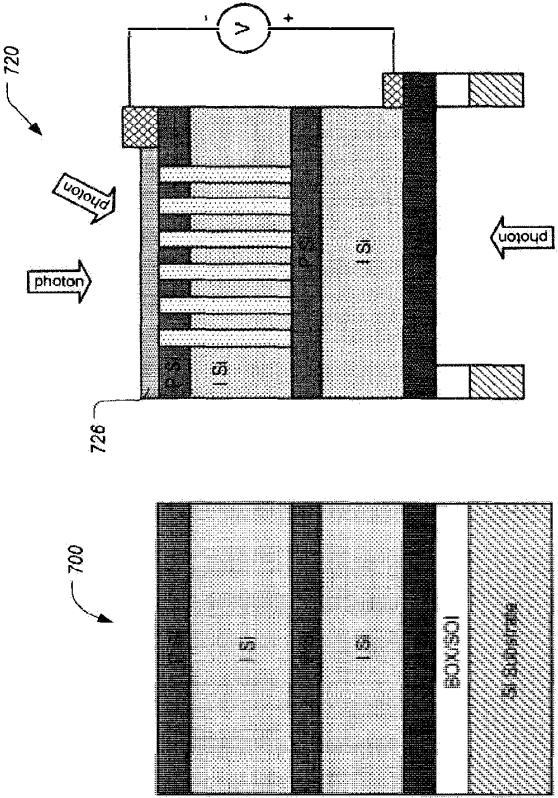


FIG. 7B

FIG. 7A

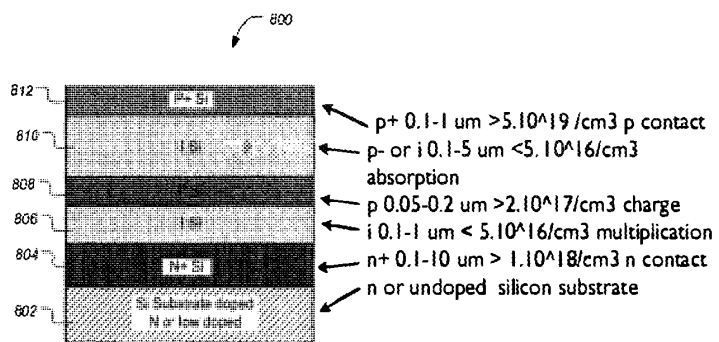
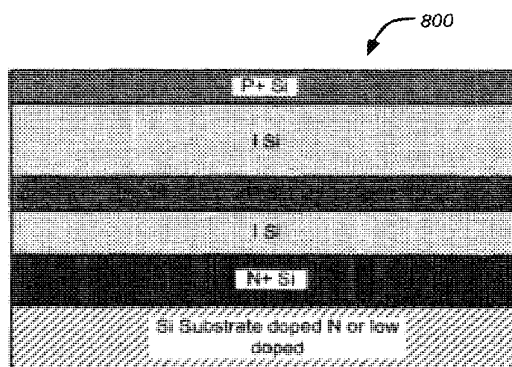
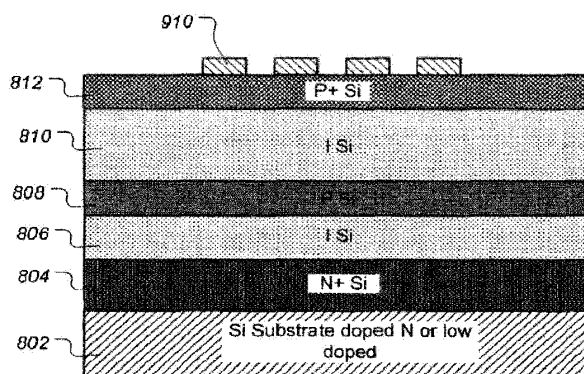
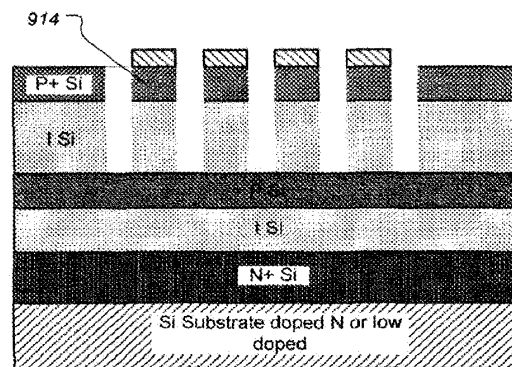
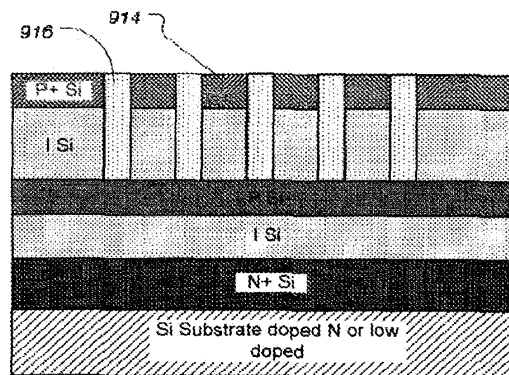


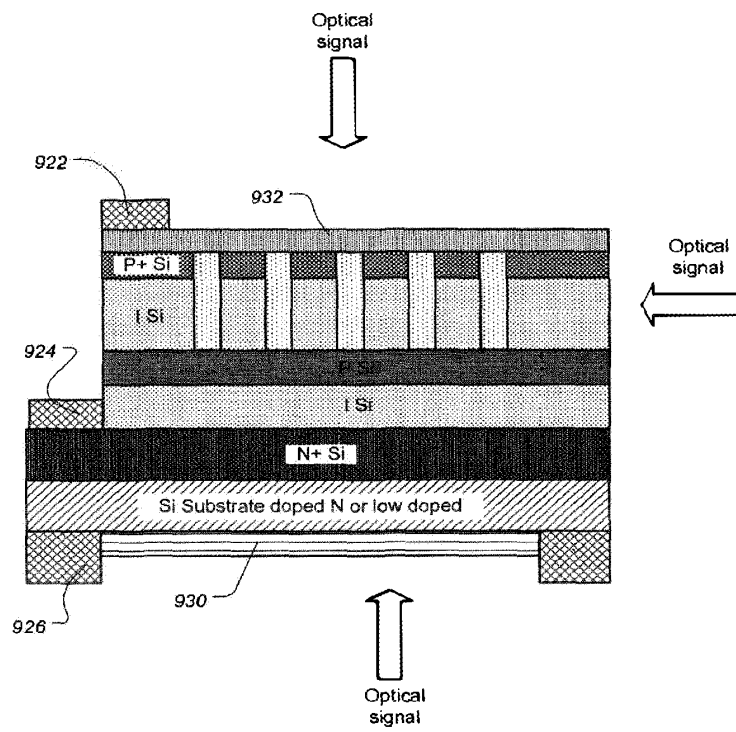
FIG. 8

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309,307,515(C)/P

**FIG. 9A****FIG. 9B**

**FIG. 9C****FIG. 9D**

**FIG. 9E**

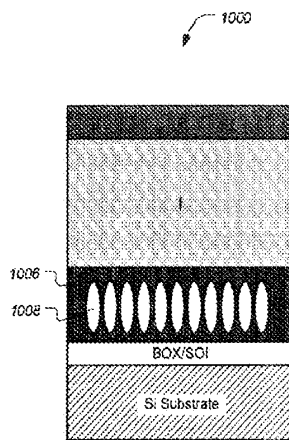


FIG. 10A

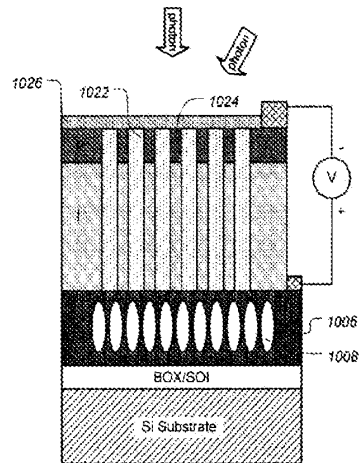


FIG. 10B

1245

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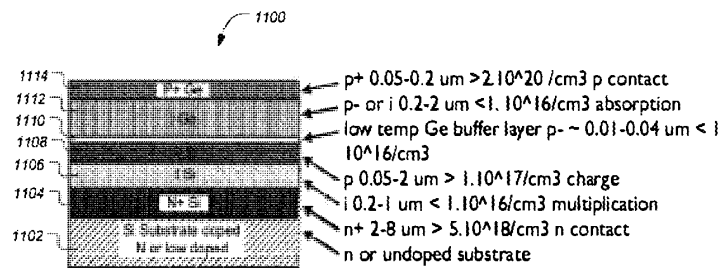


FIG. 11A

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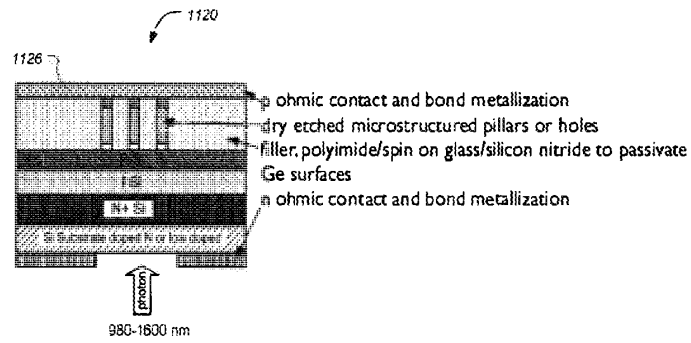


FIG. 11B

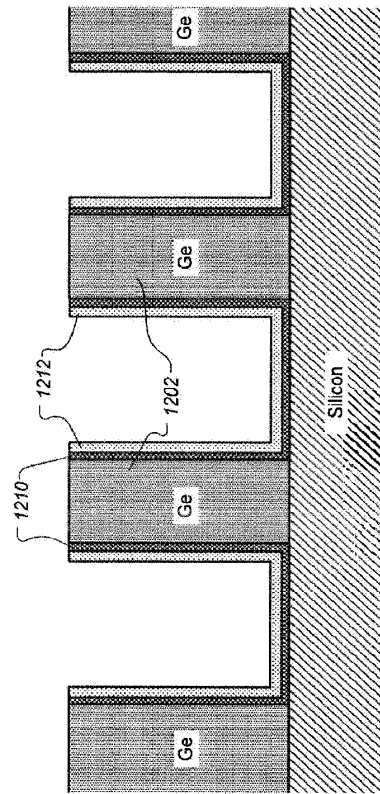


FIG. 12

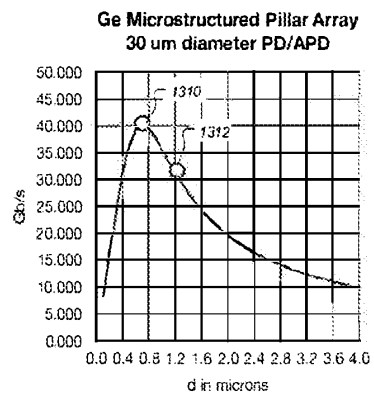


FIG. 13A

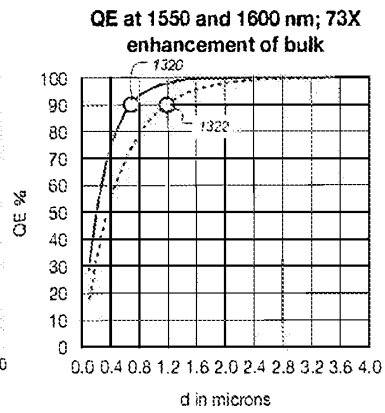


FIG. 13B

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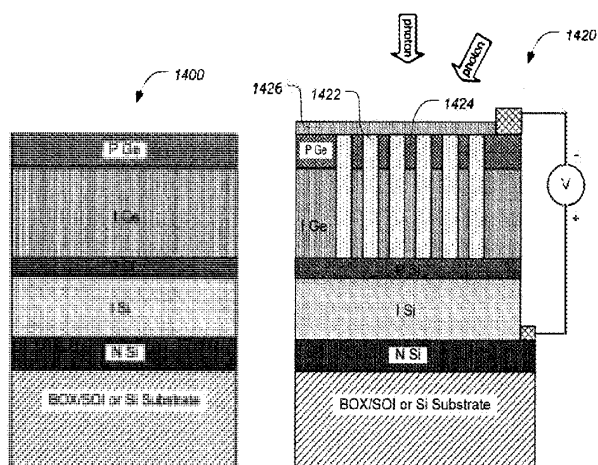


FIG. 14A

FIG. 14B

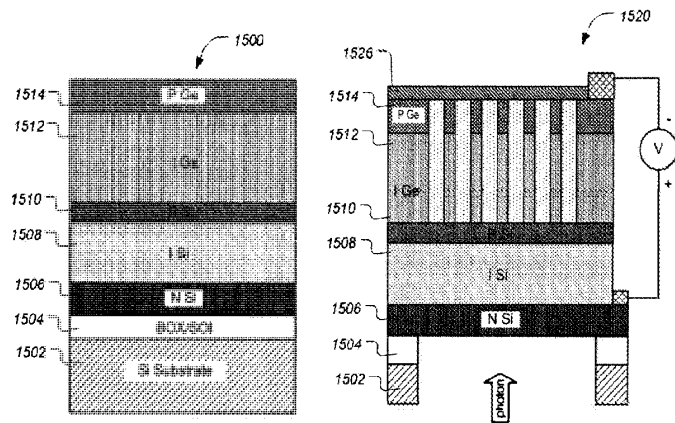


FIG. 15A

FIG. 15B

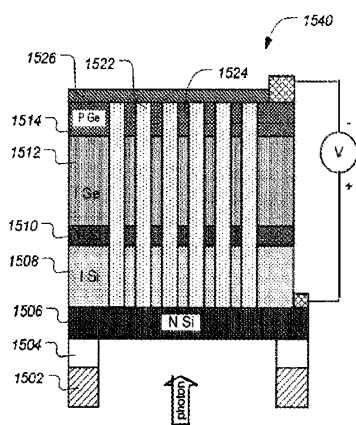


FIG. 15C

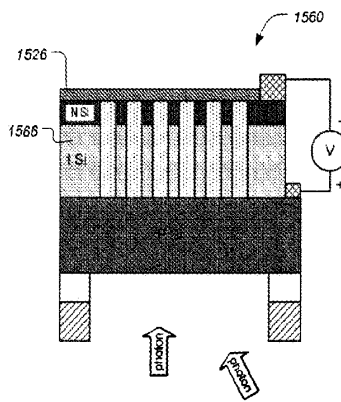


FIG. 15D

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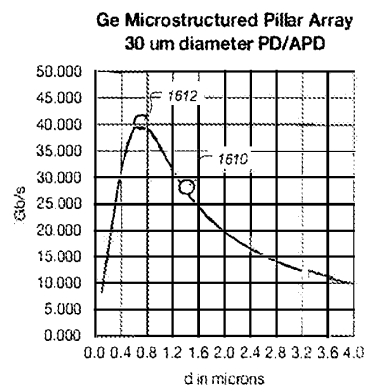


FIG. 16A

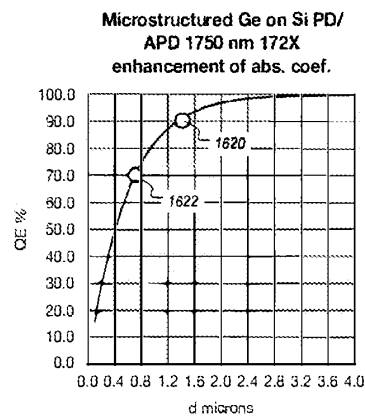


FIG. 16B

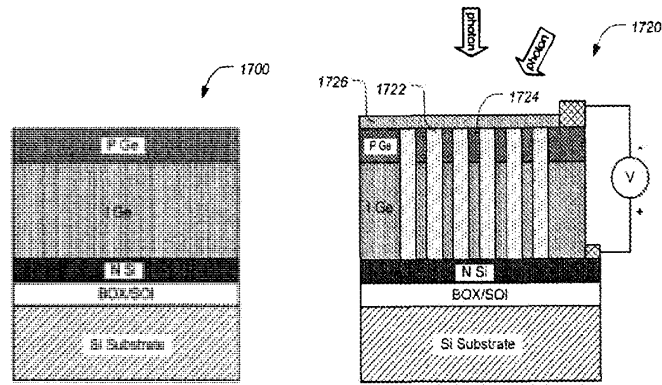


FIG. 17A

FIG. 17B

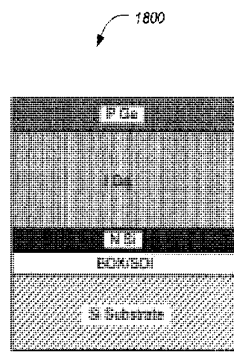


FIG. 18A

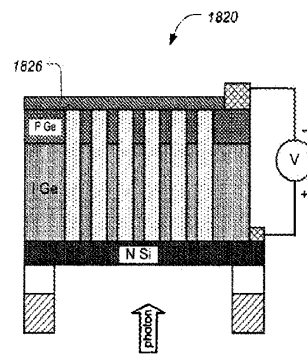
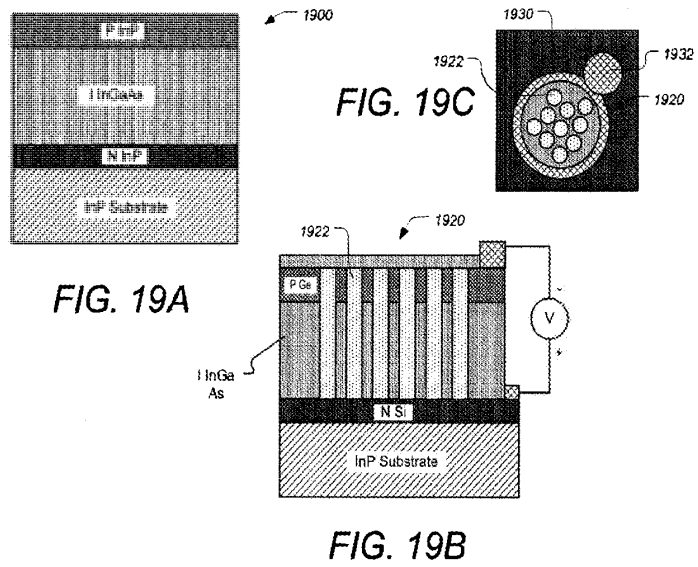


FIG. 18B



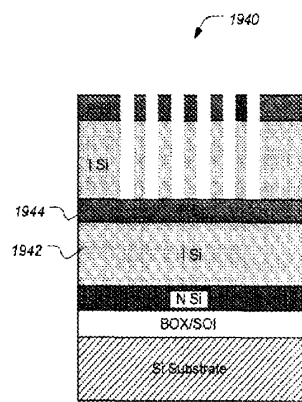


FIG. 19D

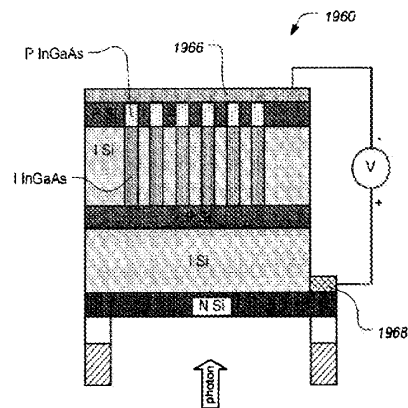
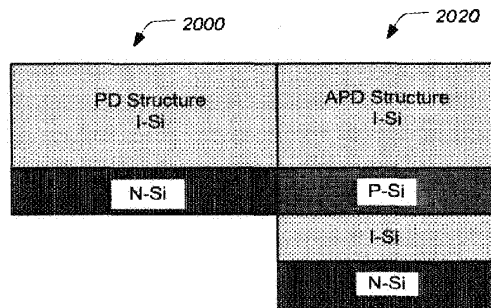
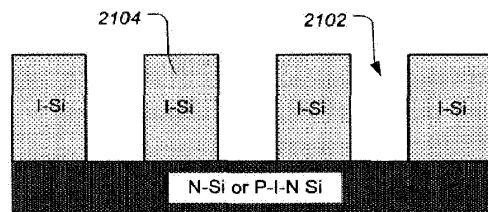
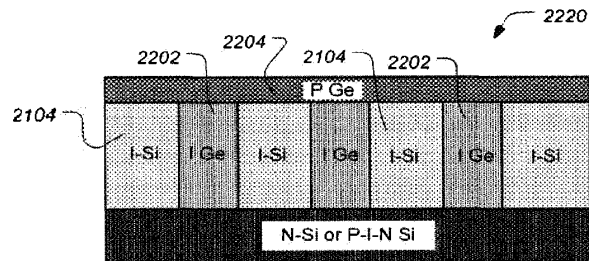
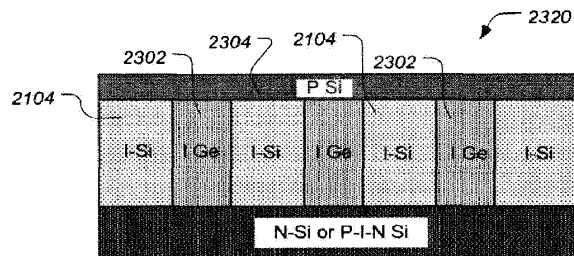


FIG. 19E

**FIG. 20****FIG. 21**

**FIG. 22****FIG. 23**

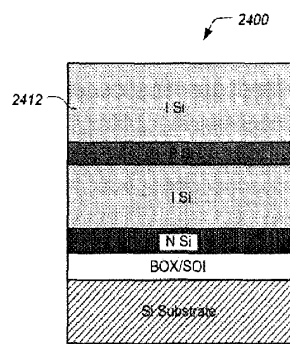


FIG. 24A

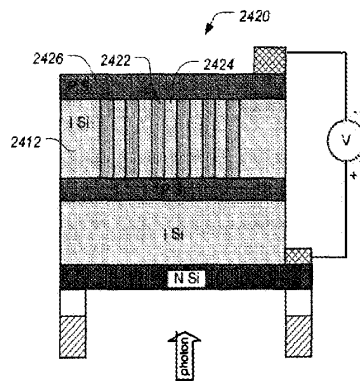


FIG. 24B

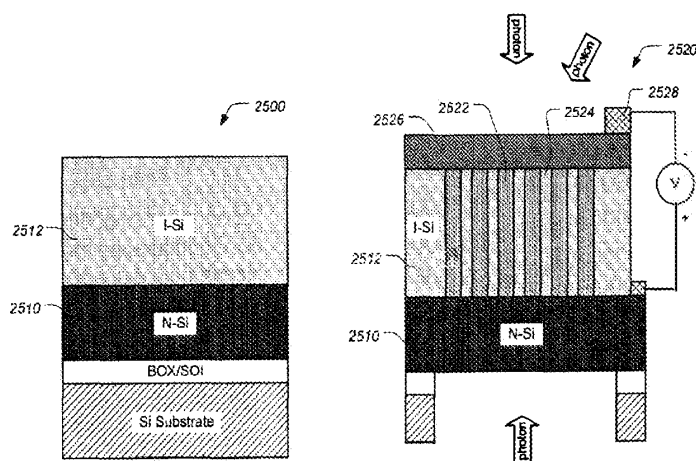
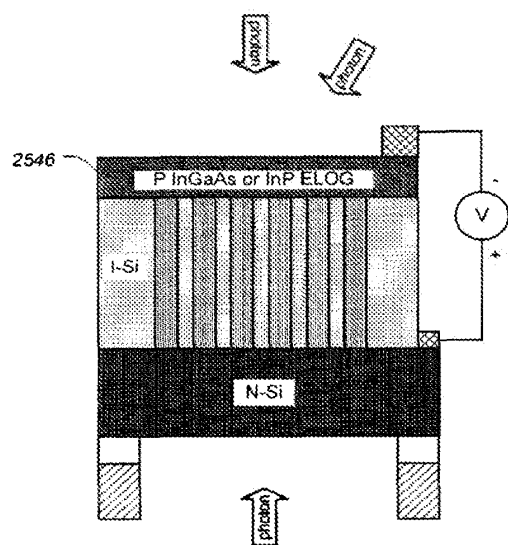


FIG. 25A

FIG. 25B

**FIG. 25C**

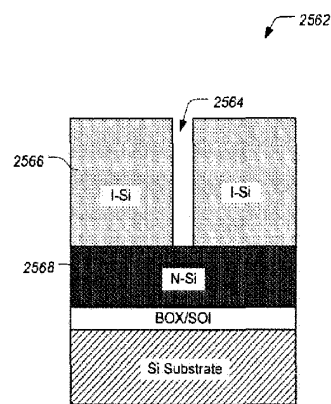


FIG. 25D

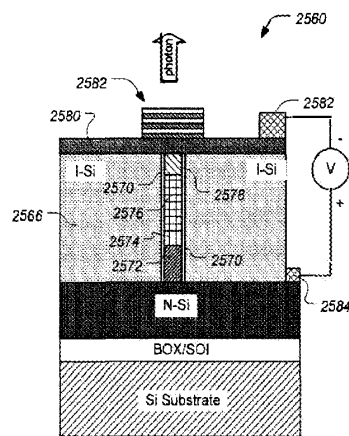
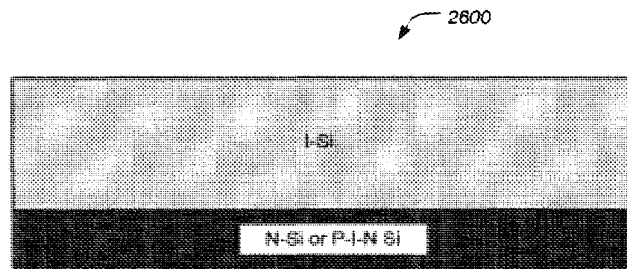
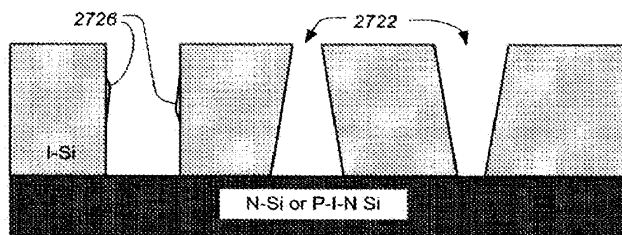
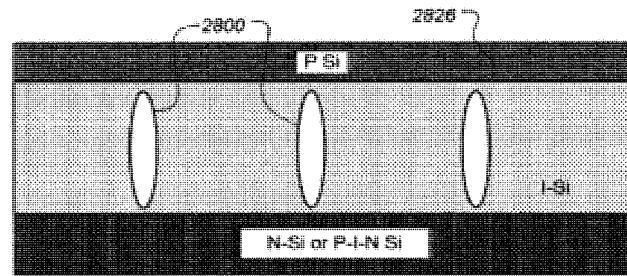
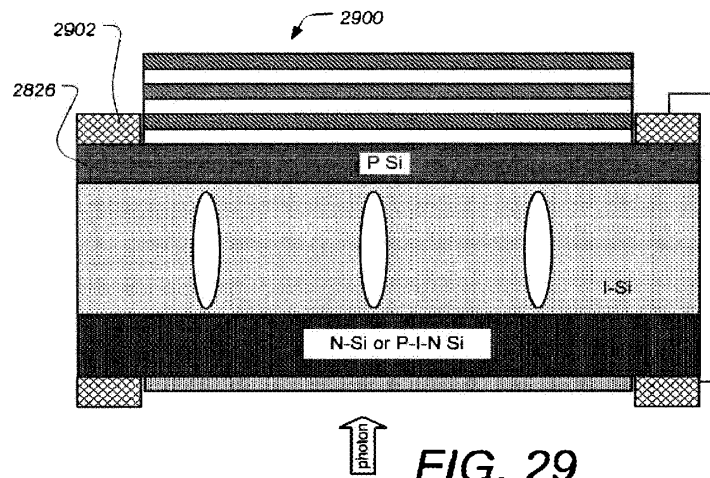


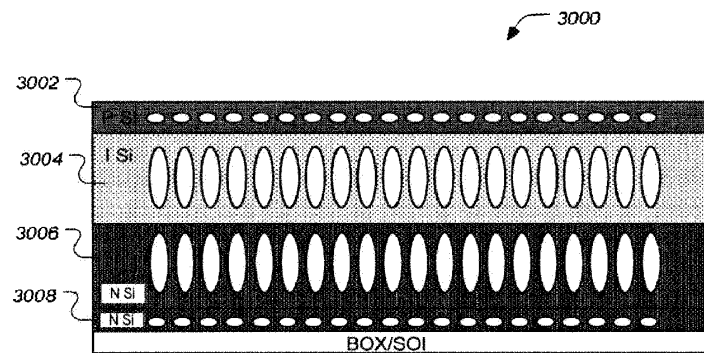
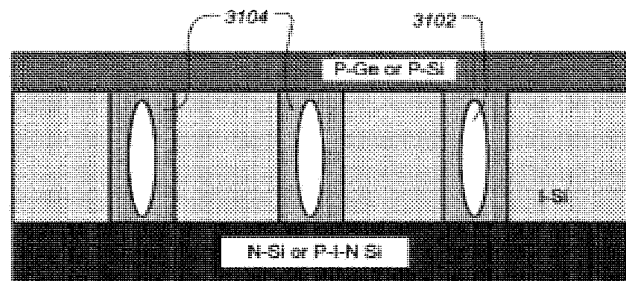
FIG. 25E

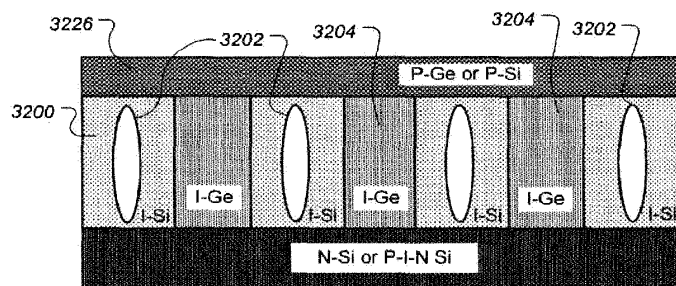
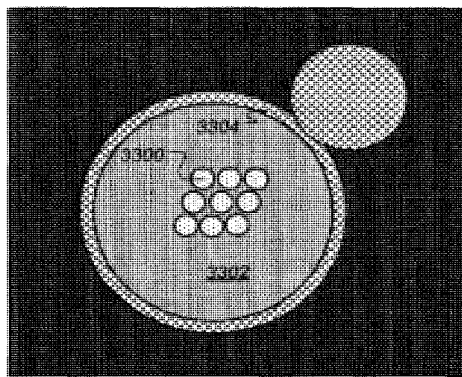
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**FIG. 26****FIG. 27**

**FIG. 28****FIG. 29**

**FIG. 30****FIG. 31**

**FIG. 32****FIG. 33**

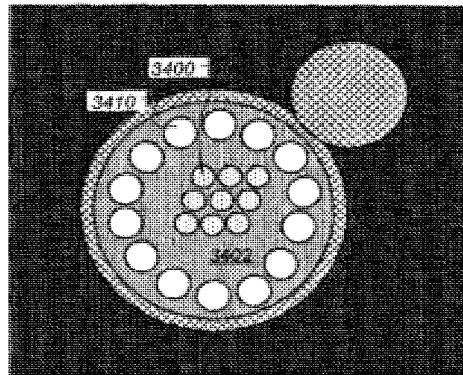


FIG. 34

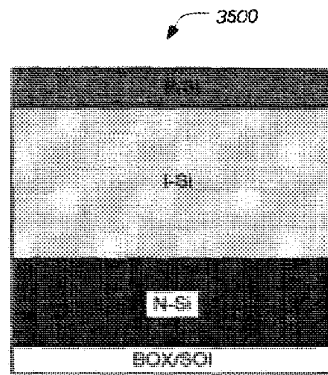


FIG. 35
(prior art)

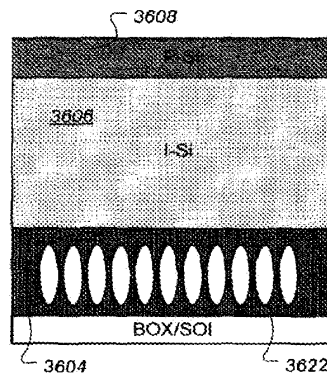
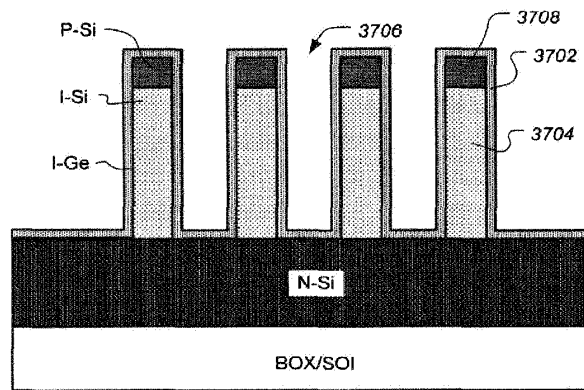
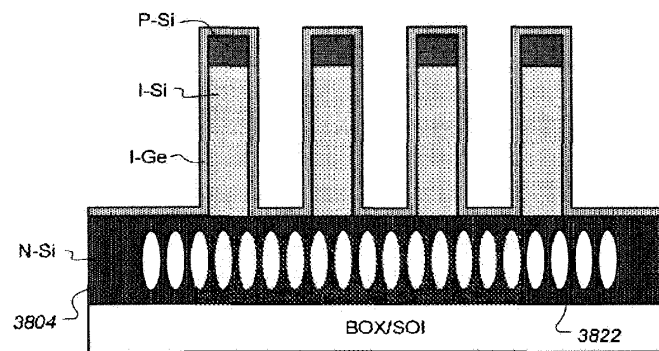


FIG. 36

**FIG. 37****FIG. 38**

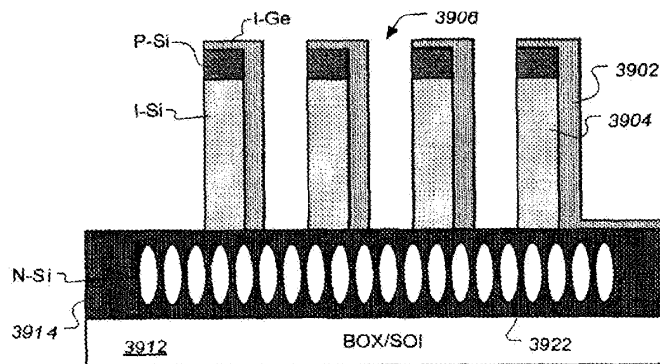


FIG. 39

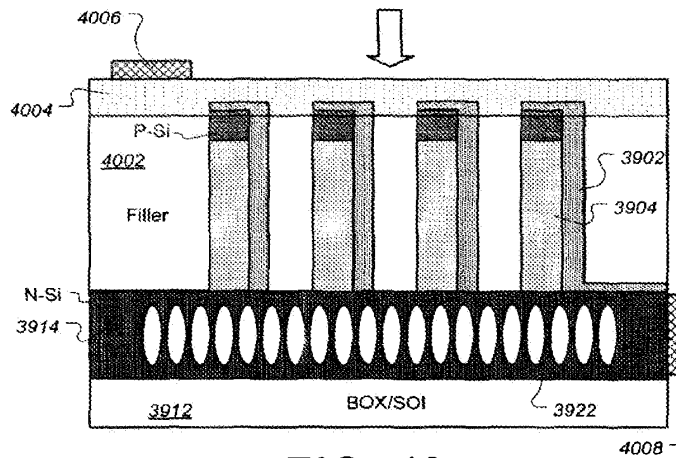


FIG. 40

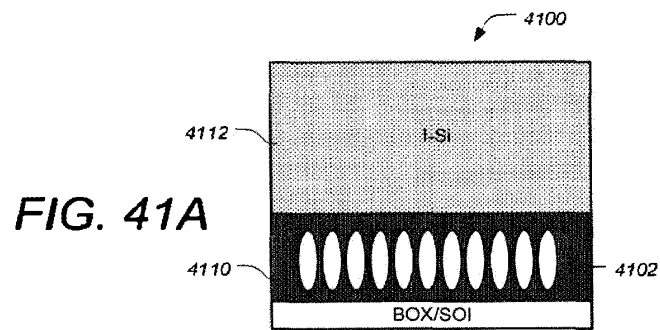
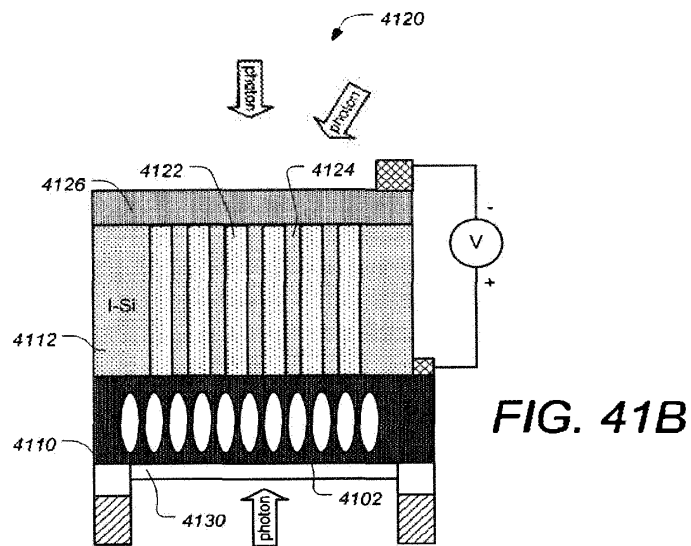


FIG. 42A

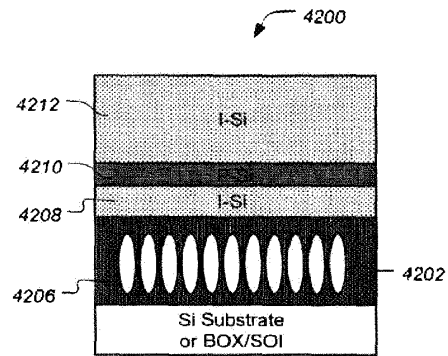
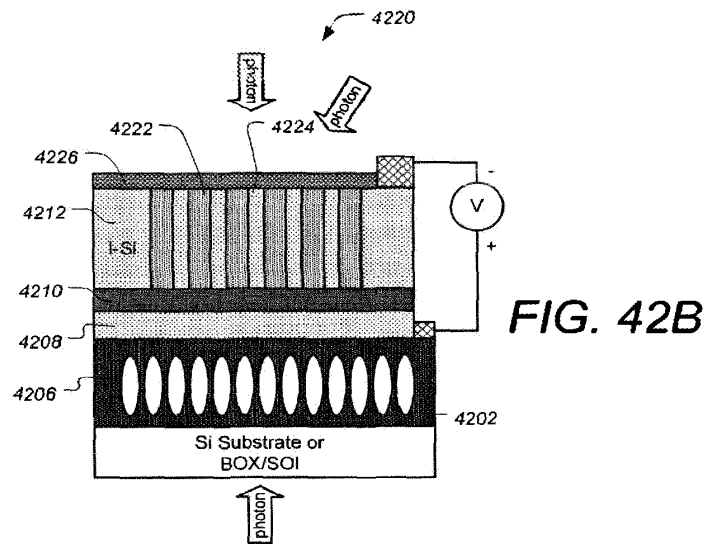


FIG. 42C

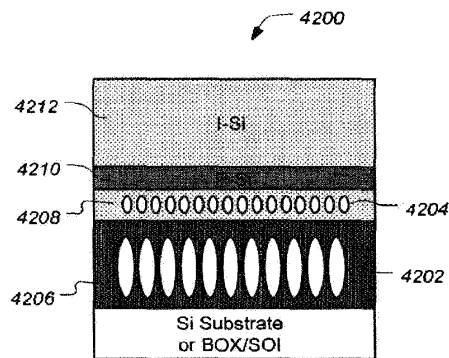
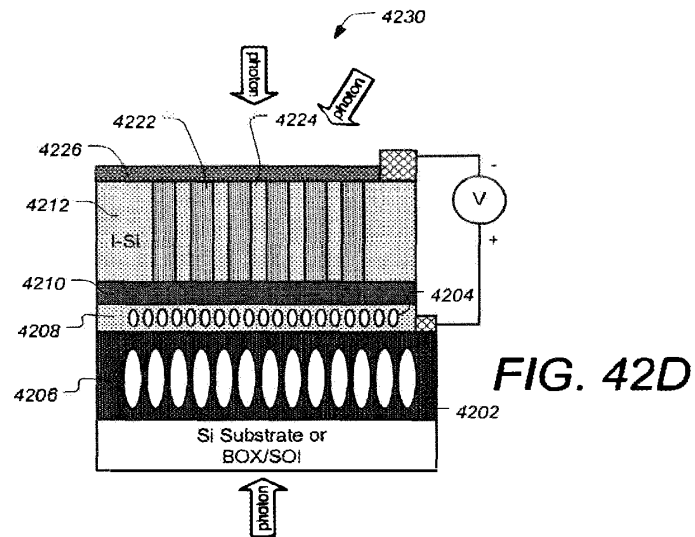
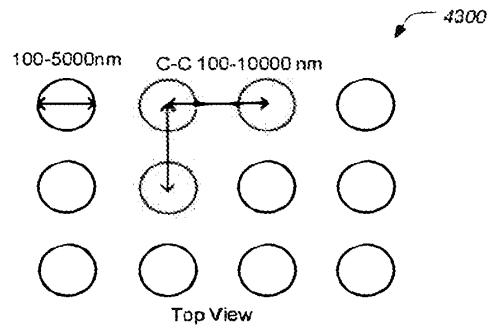
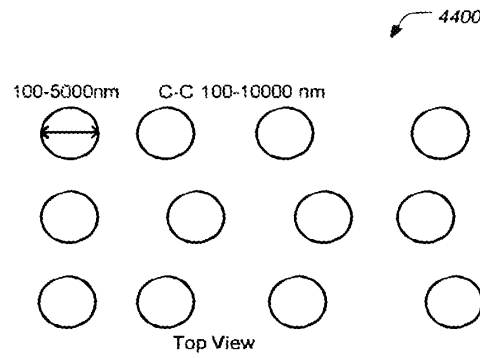
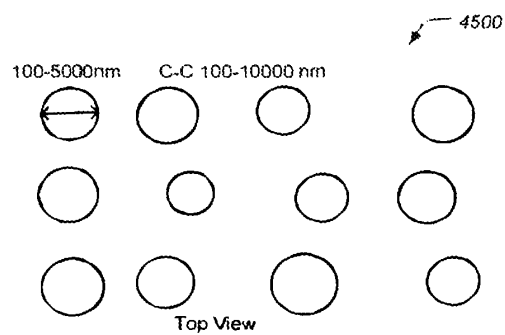
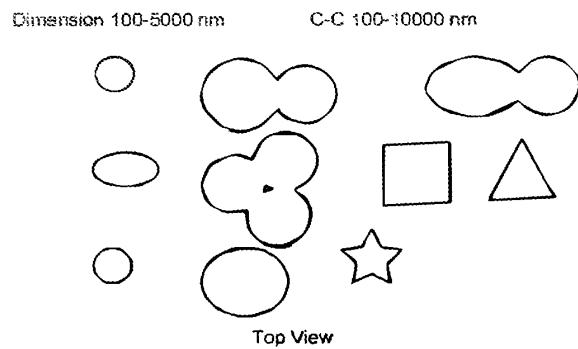
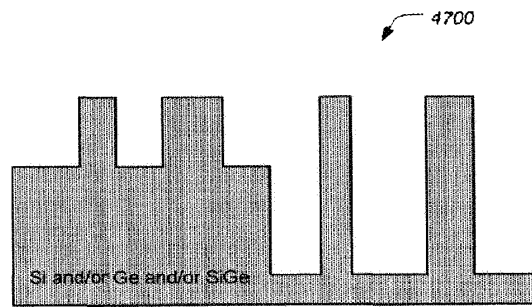
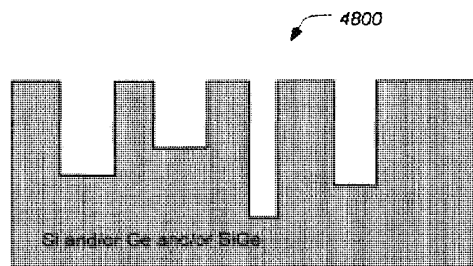
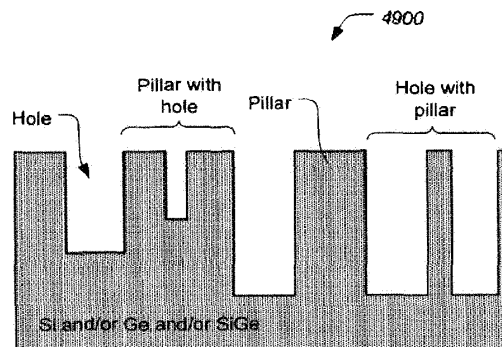
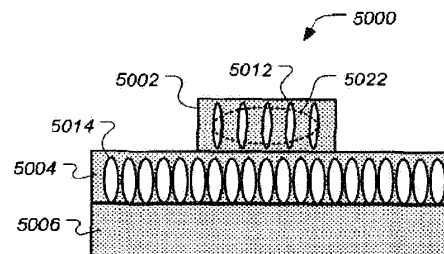


FIG. 42D

**FIG. 43****FIG. 44**

**FIG. 45****FIG. 46**

**FIG. 47****FIG. 48**

**FIG. 49****FIG. 50**

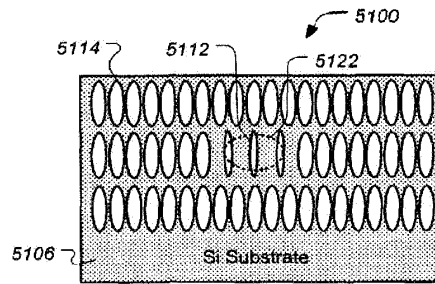


FIG. 51

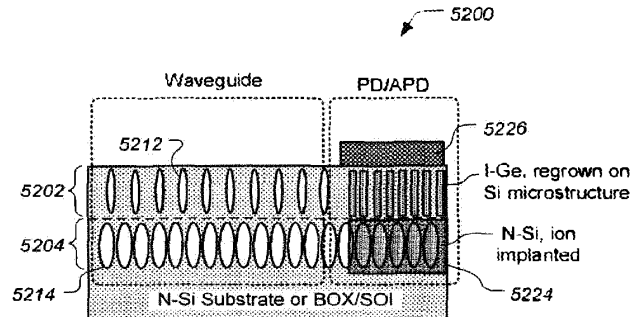
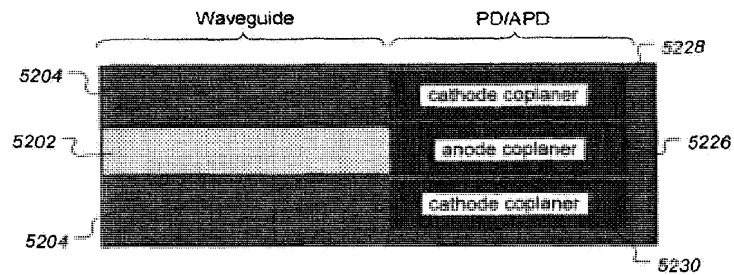
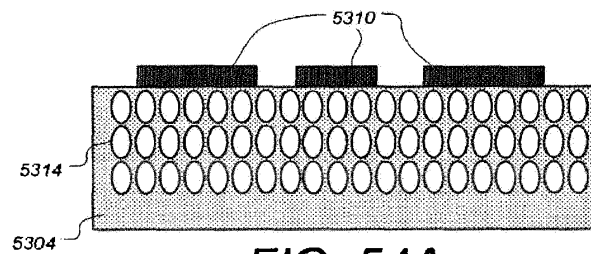
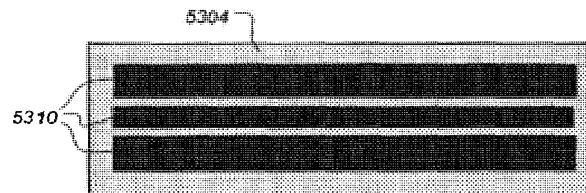
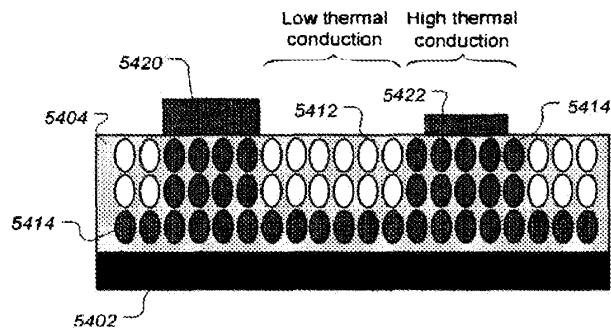
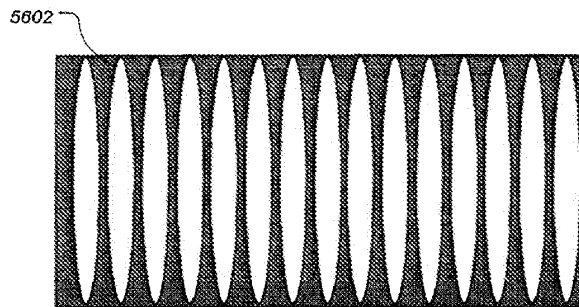


FIG. 52

**FIG. 53****FIG. 54A****FIG. 54B**

*FIG. 55**FIG. 56*

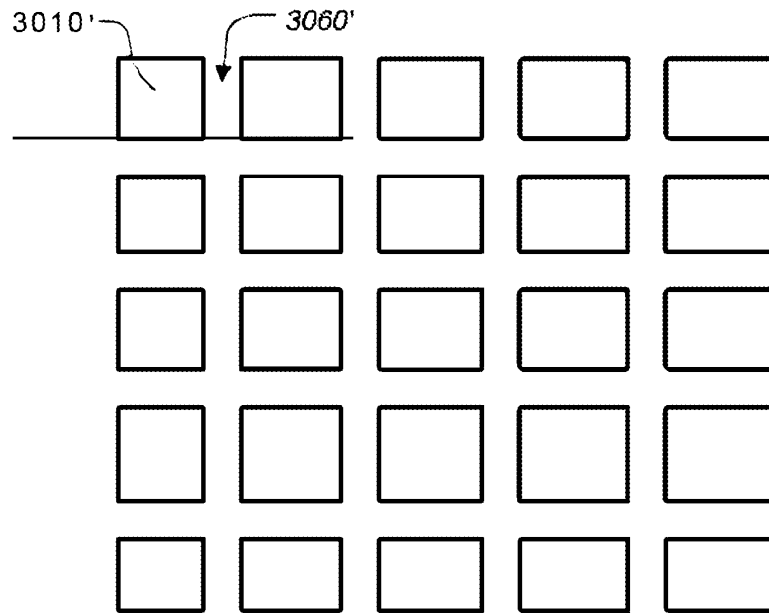


FIG. 57A

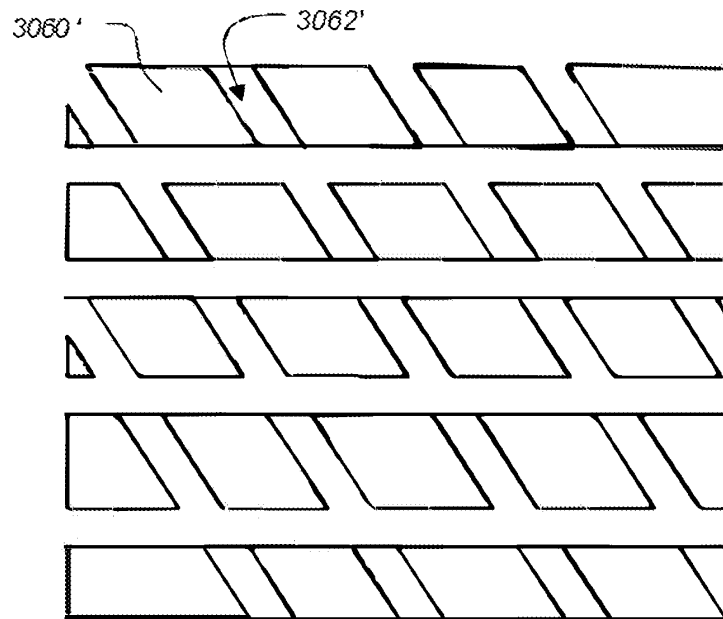


FIG. 57B

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IPPH ST36 XML through DFP

SUBJECT OF THE INVENTION

The Radix Rumiciss photodetector of photodetector preparation method and preparation

[0001] Technical field

[0002] The present invention relates to the Radix Rumiciss photodetector of a kind of photodetector preparation method and preparation, belong to semiconductor optoelectronic Sub- technical field.

[0003] Background technology

[0004] Photodetector is visited in biomedicine, data storage medium, flame monitoring, ultraviolet dosage measurement, high-energy ray It is used widely in the fields such as survey, medical treatment, safety check, industrial flaw detection. When incident illumination energy is more than photodetector material forbidden band width When spending, electronics will be made to transit to conduction band from valence band, produce electron hole pair, the electron hole pair of generation is collected by electrode, It is the formation of photoelectric current output. Quantum efficiency is to weigh one of most important performance indications of photodetector, mainly by Photon incident efficiency, internal quantum efficiency and carrier collection efficiency determine. Because the refractivity of quasiconductor and air is big, quite Light reflected by interface and be collected it is impossible to enter in device, lead to device efficiency to reduce. Generally according to incident illumination and reflected light Interference cancellation principle, design and prepare anti-reflection film so that the vertical incidence light incident efficiency of single wavelength reaches more than 95%. But the problem that this design brings is, when incident wavelength offset design wavelength, or angle of incidence offset from perpendicular, visit Survey efficiency drastically to decline.

[0005] According to Theory of Electromagnetic Field, taking for electric field perpendicular to the TE ripple of the plane of incidence as a example, can according to the seriality of interface With the Fresnel reflection coefficient deriving TE ripple it is :

[0006] Wherein, θ_0 For angle of incidence, θ_1 For the angle of emergence, θ_0 With θ_1 Meet :

[0007] Wherein n_0 For the refractive index of incident medium, n_1 Refractive index for emergent medium. Incident illumination with 650nm (TE ripple) From Air incidence, to silicon materials

surface, as shown in Figure 1 it can be deduced that TE wave reflection rate increases with the increase of angle of incidence, is said The sub- incident efficiency in Mingguang City is relevant with angle, the photon incident efficiency highest in vertical normal incidence direction. What generally people adopted is anti-reflection Film, according to anti-reflection film thickness be $\lambda/4$ when to wavelength the light transmission highest for λ , the two of one layer of 100nm of silicon materials superficial growth Silicon oxide is used for the incident illumination of anti-reflection 600nm, by equivalent to the silicon dioxide of 100nm and silicon materials become an interface, its admittance is Y, defining its eigenmatrix j_s :

- [0008] Wherein, n_1 And n_2 It is respectively the refractive index of silicon dioxide and silicon,
- [0009] For the phase thickness of silicon dioxide, d_1 For the actual (real) thickness of silicon dioxide, $Y=C/B$, after therefore adding anti-reflection film Reflection coefficient j_s :
- [0010] Wherein, n_0 Refractive index for air.
- [0011] Result of calculation as shown in fig. 2, it can be seen that increasing to 60° with angle of incidence from 0° , to 600nm wavelength, absorbance It is reduced to 75% from 91%, transmittance peak wavelength, also with the centre wavelength of the increase off-design of angle, is reduced to from 600nm 470nm, absorbance constantly declines.
- [0012] At present, all Radix Rumiciss photodetection is had strongly at aspects such as space optical communication, weak light detection, return laser beam detections Demand, such as diffuse-reflectance detection in space optical communication, return laser beam are dissipated due to the echo that laser beam divergence leads in detecting Penetrate etc. it is characterised in that the ranges of incidence angles of incident illumination is big, intensity is faint, and therefore these applications are required to photodetector in energy While the incident illumination of reception wider angle scope, there is high sensitivity and quantum efficiency.
- [0013] Just because of current anti-reflection film design requirement incident illumination vertical incidence, in actual detection system, need extra Detector Rotable Control System, due to being limited by Rotable Control System speed, scan efficiency is too low, therefore it is further proposed that Form focal plane arrays (FPA) with the Focused Optical system of photodetector cooperation and by increasing detector, realize to all directions The detection of signal, but extra system not only increases the volume of whole photodetector module, more increases and realizes difficulty.
- [0014] Content of the invention

- [0015] Present invention aim at solution above-mentioned technical problem, provide a kind of photodetector structure of Radix Rumiciss and preparation side Method.
- [0016] The technical solution used in the present invention is :
- [0017] A kind of preparation method of photodetector, comprises the steps :
- [0018] Lithography step, makes the figure of structure photosurface again by lithography in the upper surface of photodetection structure,
- [0019] Remove surface damage layer step, described photodetection structure is placed in 60-100 DEG C, in the KOH solution of 20wt%, goes Surface damage layer except about 10 μm being located at again in structure photosurface;
- [0020] Structure step again, described photodetection structure is placed in 60-100 DEG C, the isopropanol mixing of KOH and 8vol% of 3wt% In solution, form Radix Rumiciss structure in structure photosurface again.
- [0021] Preferably, also include the step protecting the region outside photosurface using photoresist in described lithography step;Described again The step removing the photoresist of protection is also included after structure step.
- [0022] Preferably, also comprise the steps, under 800-1200 DEG C of wet oxygen environment after described removal photoresist step Front grows the SiO_2 of 50nm, photoetching simultaneously erodes region outside structure photosurface again, forms passivation layer.
- [0023] Preferably, described Radix Rumiciss structure be described in structure photosurface again out-of-flatness surface, in order to make oblique incident ray contact institute The part of the reflected light producing after stating again structure photosurface enters in described photodetection structure as oblique incident ray again.
- [0024] Preferably, the out-of-flatness surface of the described photosurface of structure again is the continuous section of rule.
- [0025] Preferably, the continuous section of the described photosurface of structure again is taper, trapezoidal, rectangle, spherical, bulb-shaped recess shape, its figure Shape dutycycle 50% to 100%.

- [0026] Present invention further teaches a kind of Radix Rumiciss photodetector, including for producing photoelectric photodetection structure, The upper surface of described photodetection structure is provided with structure photosurface again, and the upper surface of the described photosurface of structure again is used for out-of-flatness surface So that the part of the reflected light producing after structure photosurface again described in oblique incident ray contact enter to as oblique incident ray again described In photodetection structure.
- [0027] Preferably, the upper surface of the described photosurface of structure again is additionally provided with passivation layer, described passivation layer cover all described in again Structure photosurface, the material of described passivation layer is SiO_2 、 SiN_x 、 MgF_2 、ITO.
- [0028] Preferably, the described photosurface of structure again can be applicable to by silicon, polysilicon, GaAs, GaN, InP, SiC, ZnO, SOI, tellurium In the photodetection structure of cadmium mercury preparation.
- [0029] Preferably, described photodetection structure is the avalanche photodetector of linear model and Geiger mode angular position digitizer, or is PIN light Electric explorer, or be MSM photoelectric detector.
- [0030] The beneficial effects of the present invention is : Provide a kind of preparation method of Radix Rumiciss photodetector, high efficient and reliable, pass through In photodetector surfaces structure again, break the restriction of Fresnel reflection coefficient angle of incidence, reduce the sensitivity to incident wavelength, no Extra system need to be added, only Radix Rumiciss are realized by single photodetector and detect.
- [0031] Brief description
- [0032] Below in conjunction with the accompanying drawings and embodiment the invention will be further described :
- [0033] Fig. 1 : , from air incidence to silicon materials surface, reflectance is with the change curve of angle of incidence for TE ripple.
- [0034] Fig. 2 : SiO_2 containing 100nm The transmission of the incident illumination to 0° , 30° and 60° angle of incidence for the silicon materials substrate of anti-reflection film is bent Line chart.
- [0035] Fig. 3 : The structural representation of the Radix Rumiciss photodetector of the present invention.

- [0036] Fig. 4 : Input path schematic diagram on the photosurface of structure again of the present invention for the oblique incident ray.
- [0037] Fig. 5 to Fig. 9 : The cross-sectional schematic of the photosurface of structure again of the present invention.
- [0038] Figure 10 : The corresponding profile of each step of the preparation method of Radix Rumiciss photodetector of the present invention.
- [0039] Specific embodiment
- [0040] Present invention is disclosed a kind of Radix Rumiciss photodetector, its structure is as shown in figure 3, include successively from top to bottom : Passivation Layer 101, again structure photosurface 102 and photodetection structure 103. Described photodetection structure 103 is used for producing photoelectric effect, and this is Prior art, will not be described here. In conjunction with shown in Fig. 4, the upper surface of the described photosurface of structure again 102 is out-of-flatness surface in order to make The part of the reflected light producing after structure photosurface 102 again described in oblique incident ray contact enters to described light as oblique incident ray again In electrical resistivity survey geodesic structure 103, described passivation layer 101 envelope completely described in structure photosurface 102 again.
- [0041] Specifically, when incident illumination incides the photosurface of structure again 102 of photodetection structure 103 according to certain angle, due to At incidence point, actual incident angle changes, and reduces actual incident angle for inclined plane, therefore, it is possible to improve tilt into Penetrate the absorbance of light. Meanwhile, the light of reflection reflects in multiple interfaces, increases the probability being transmitted into quasiconductor, thus Increase absorbance, break the restriction of Fresnel reflection coefficient angle of incidence, reduce the sensitivity to incident wavelength, realize Radix Rumiciss and visit Survey.
- [0042] The photosurface of structure again 102 in the present invention, can be carved by chemical attack, laser grooving, reactive ion etching, machinery The methods such as groove, epitaxial growth are formed, deeper 0.1 μm to 50 μm of structure structure. The surface topography of the described photosurface of structure again is rule Continuous section, can be taper as disclosed in Fig. 5 to Fig. 9, trapezoidal, rectangle, spherical, bulb-shaped recess etc., its figure dutycycle 50% To 100%.
- [0043] The photodetection structure 103 of the present invention can by structure photosurface 102 again increase passivation layer 101 repair because The surface damage that structure introduces again, reduces surface recombination, reduces dark current. And, because described passivation layer

101 has certain thickness Degree, between 1nm to 10 μm , therefore it can be used as a kind of presence of anti-reflection film. This passivation layer 101 material can be SiO_2 , SiN_x , MgF_2 , ITO etc.. Certainly, if being in the consideration of cost, this passivation layer 101 can also be saved, that is, Radix Rumiciss photodetector is only include photodetection structure and the structure photosurface again being provided thereon, at least part of surface of the described photosurface of structure again is out-of-flatness Surface, in order to make oblique incident ray contact described in the part of reflected light that produces after structure photosurface 102 again as oblique incident ray Enter in described photodetection structure 103.

- [0044] The photosurface of structure again 102 of the present invention is applied to by silicon, polysilicon, GaAs, GaN, InP, SiC, ZnO, SOI, tellurium cadmium The photodetector of the various material such as hydrargyrum preparation.
- [0045] The photosurface of structure again 102 of the present invention is applied to the avalanche photodetector of linear model and Geiger mode angular position digitizer, is also suitable In PIN photoelectric detector, MSM photoelectric detector etc..
- [0046] The preparation method of the Radix Rumiciss photodetector of the present invention once is described below.
- [0047] As shown in Figure 10, photodetection structure 103 adopts the PIN photoelectric detector that the silicon materials of N-shaped doping manufacture, its Structure photosurface 102 forms as a example taper by the method by chemical attack again, and preparation process and method are as follows :
- [0048] Step (a) , make the figure of structure photosurface 102 again by lithography in the upper surface of photodetection structure 103, using photoresist Region outside 104 protection photosurfaces 102;
- [0049] Step (b) , the photodetection structure 103 protected using photoresist 104 is placed in 60-100 DEG C, the KOH of 20wt% is molten A period of time is processed in liquid (About 40 seconds) , remove the surface damage layer of about 10 μm being located at again in structure photosurface 102;
- [0050] Step (c) , the photodetection structure 103 protected using photoresist 104 is placed in 60-100 DEG C, the KOH of 3wt% and A period of time is processed in the isopropyl alcohol mixture of 8vol % (About 30 minutes) , form inverted pyramid in structure photosurface 102 again Radix Rumiciss structure;

[0051] Step (d) , remove the photoresist 104 of protection, front growth 50nm under 800-1200 DEG C of the wet oxygen environment SiO_2 , photoetching simultaneously erodes region outside structure photosurface 102 again, forms passivation layer 101, that is, obtain the preferred embodiment of the present invention Radix Rumiciss photodetector.

[0052] All technical sides that the present invention still has numerous embodiments, all employing equivalents or equivalent transformation and formed Case, is within the scope of the present invention.

1. 1. a kind of preparation method of photodetector it is characterised in that : Comprise the steps, Lithography step, makes the figure of structure photosurface (102) by lithography in the upper surface of photodetection structure (103) again, removes surface Damage layer step, described photodetection structure (103) is placed in 60-100 DEG C, in the KOH solution of 20wt%, remove and be located at structure again The surface damage layer of about 10 μm in photosurface (102) ; Structure step again, described photodetection structure (103) is placed in 60-100 DEG C, and the isopropanol of KOH and 8vol% of 3wt% mixes Close in solution, form Radix Rumiciss structure in structure photosurface (102) again, described Radix Rumiciss structure is the described photosurface of structure again (102) The continuous section of rule, in order to make oblique incident ray contact described in structure photosurface (102) produces afterwards again reflected light again as oblique Penetrate light to enter in described photodetection structure (103).
2. 2. photodetector according to claim 1 preparation method it is characterised in that : Also include in described lithography step The step protecting again structure photosurface (102) region outward using photoresist (104) ; Also include removing after the described step of structure again protecting The step of the photoresist (104) of shield.
3. 3. photodetector according to claim 2 preparation method it is characterised in that : Described removal photoresist step it Also comprise the steps afterwards, under 800-1200 DEG C of wet oxygen environment, front grows the SiO_2 of 50nm, photoetching simultaneously erodes structure again Photosurface (102) region outward, forms passivation layer (101).
4. 4. the preparation method according to the arbitrary described photodetector of claim 1-3 it is characterised in that : Described structure photosurface again (102) continuous section is taper, trapezoidal, rectangle, spherical, bulb-shaped recess shape, its figure dutycycle 50% to 100%.
5. 5. a kind of Radix Rumiciss photodetector of preparation method according to claim 1 preparation it is characterised in that : Including for Produce photoelectric photodetection structure (103), the upper surface of described photodetection structure (103) is provided with structure photosurface again (102), the upper surface of the described photosurface of structure again (102) be out-of-flatness surface in order to make oblique incident ray contact described in structure light again The reflected

light that quick face (102) produces afterwards enters in described photodetection structure (103) as oblique incident ray again.

6. 6. Radix Rumiciss photodetector according to claim 5 it is characterised in that : The upper table of the described photosurface of structure again (102) Face is additionally provided with passivation layer (101), described passivation layer (101) cover all described in structure photosurface (102) again, described passivation layer (101) material is SiO_2 、 SiN_x 、 MgF_2 Or ITO.
7. 7. Radix Rumiciss photodetector according to claim 6 it is characterised in that : The described photosurface of structure again (102) can be applied In the photodetection structure (103) prepared by silicon, polysilicon, GaAs, GaN, InP, S iC, ZnO, SOI or mercury cadmium telluride.
8. 8. Radix Rumiciss photodetector according to claim 7 it is characterised in that : Described photodetection structure (103) is line Sexual norm and the avalanche photodetector of Geiger mode angular position digitizer, or be PIN photoelectric detector, or be MSM photoelectric detector.



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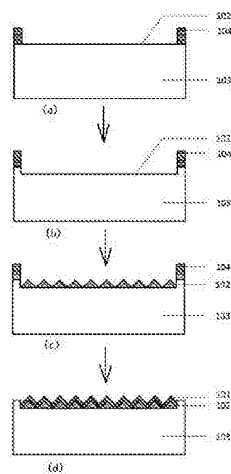
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(54)发明名称

光电探测器制备方法及制备的广角光电探测器

(57)摘要

本发明公开了一种光电探测器的制备方法，包括如下步骤：在光电探测结构的上表面光刻出再构光敏面的图形，去除位于再构光敏面内的表面损伤层，在再构光敏面内形成广角结构。本发明的有益效果在于：提供了一种广角光电探测器的制备方法，高效可靠，通过在光电探测器表面再构，打破菲涅尔反射系数入射角的限制，降低对入射波长的敏感度，不需加入额外的系统，仅通过单个光电探测器实现广角探测。



1. 一种光电探测器的制备方法, 其特征在于: 包括如下步骤,

光刻步骤, 在光电探测结构(103)的上表面光刻出再构光敏面(102)的图形, 去除表面损伤层步骤, 将所述光电探测结构(103)置于60-100℃, 20wt%的KOH溶液中, 去除位于再构光敏面(102)内的大约10μm的表面损伤层;

再构步骤, 将所述光电探测结构(103)置于60-100℃, 3wt%的KOH及8vol%的异丙醇混合溶液中, 在再构光敏面(102)内形成广角结构, 所述广角结构为所述再构光敏面(102)的规则连续截面, 用以使斜入射光接触所述再构光敏面(102)后产生的反射光再次作为斜入射光进入至所述光电探测结构(103)内。

2. 根据权利要求1所述的光电探测器的制备方法, 其特征在于: 所述光刻步骤中还包括使用光刻胶(104)保护再构光敏面(102)外的区域的步骤; 所述再构步骤之后还包括去除保护用的光刻胶(104)的步骤。

3. 根据权利要求2所述的光电探测器的制备方法, 其特征在于: 所述去除光刻胶步骤之后还包括如下步骤, 在800-1200℃的湿氧环境下正面生长50nm的SiO₂, 光刻并腐蚀掉再构光敏面(102)外的区域, 形成钝化层(101)。

4. 根据权利要求1-3任一所述的光电探测器的制备方法, 其特征在于: 所述再构光敏面(102)的连续截面为锥形、梯形、矩形、球形、球形凹陷形, 其图形占空比50%到100%。

5. 一种根据权利要求1所述的制备方法制备的广角光电探测器, 其特征在于: 包括用于产生光电效应的光电探测结构(103), 所述光电探测结构(103)的上表面上设有再构光敏面(102), 所述再构光敏面(102)的上表面为不平整表面用以使斜入射光接触所述再构光敏面(102)后产生的反射光再次作为斜入射光进入至所述光电探测结构(103)内。

6. 根据权利要求5所述的广角光电探测器, 其特征在于: 所述再构光敏面(102)的上表面还设有钝化层(101), 所述钝化层(101)完全覆盖住所述再构光敏面(102), 所述钝化层(101)的材料为SiO₂、SiNx、MgF₂或ITO。

7. 根据权利要求6所述的广角光电探测器, 其特征在于: 所述再构光敏面(102)可应用于由硅、多晶硅、GaAs、GaN、InP、SiC、ZnO、SOI或碲镉汞制备的光电探测结构(103)上。

8. 根据权利要求7所述的广角光电探测器, 其特征在于: 所述光电探测结构(103)为线性模式和盖革模式的雪崩光电探测器, 或为PIN光电探测器, 或为MSM光电探测器。

光电探测器制备方法及制备的广角光电探测器

技术领域

[0001] 本发明涉及一种光电探测器制备方法及制备的广角光电探测器,属于半导体光电子技术领域。

背景技术

[0002] 光电探测器在生物医学、数据存储媒介、火焰监测、紫外线剂量测量、高能射线探测、医疗、安检、工业探伤等领域得到广泛应用。当入射光能量大于光电探测器材料禁带宽度时,就会使得电子从价带跃迁至导带,产生电子空穴对,产生的电子空穴对被电极收集,就形成了光电流输出。量子效率是衡量光电探测器的一个最重要的性能指标之一,主要由光子入射效率、内量子效率和载流子收集效率决定。由于半导体和空气的折射率差大,相当的光被界面反射,无法进入到器件中被收集,导致器件效率降低。通常根据入射光和反射光的干涉相消原理,设计并制备增透膜,使得单一波长的垂直入射光入射效率达到95%以上。然而这种设计带来的一个问题是,当入射波长偏移设计波长,或者入射角偏离垂直方向,探测效率急剧下降。

[0003] 根据电磁场理论,以对于电场垂直于入射面的TE波为例,根据界面处的连续性可以推导出TE波的非涅尔反射系数为:

$$[0004] \quad r_{TM} = \frac{\sin(\theta_1 - \theta_0)}{\sin(\theta_1 + \theta_0)}$$

[0005] 其中, θ_0 为入射角, θ_1 为出射角, θ_0 与 θ_1 满足:

$$[0006] \quad n_1 \sin \theta_1 = n_0 \sin \theta_0$$

[0007] 其中 n_0 为入射介质的折射率, n_1 为出射介质的折射率。以650nm的入射光(TE波)从空气入射至硅材料表面为例,如图1所示,可以得出TE波反射率随入射角的增加而增加,说明光子入射效率与角度有关,垂直正入射方向的光子入射效率最高。通常人们采用的增透膜,根据增透膜厚度为 $\lambda/4$ 时对波长为 λ 的光透射率最高,在硅材料表面生长一层100nm的二氧化硅用于增透600nm的入射光,将100nm的二氧化硅和硅材料等效成一个界面,其导纳为Y,定义其特征矩阵为:

$$[0008] \quad \begin{bmatrix} B \\ C \end{bmatrix} = \begin{bmatrix} \cos \delta_1 & \frac{i}{n_1} \sin \delta_1 \\ i n_1 \sin \delta_1 & \cos \delta_1 \end{bmatrix} \begin{bmatrix} 1 \\ n_2 \end{bmatrix}$$

[0009] 其中, n_1 和 n_2 分别为二氧化硅和硅的折射率,

$$[0010] \quad \delta_1 = \frac{2\pi}{\lambda} n_1 d_1 \cos \theta_1$$

[0011] 为二氧化硅的相位厚度, d_1 为二氧化硅的实际厚度, $Y=C/B$,因此加入增透膜后的反射系数为:

$$[0012] \quad r = \frac{n_0 - Y}{n_0 + Y}$$

[0013] 其中, n_0 为空气的折射率。

[0014] 计算结果如图2所示,可以看出,随着入射角从 0° 增加到 60° ,对600nm波长,透射率从91%降低到75%,透射率峰值波长也随着角度的增加偏离设计的中心波长,从600nm降低至470nm,透射率不断下降。

[0015] 目前,在空间光通信、弱光探测、激光回波探测等方面均对广角光电探测有着强烈的需求,例如空间光通信中的漫反射探测、激光回波探测中由于激光发散角导致的回波散射等,其特征在于入射光的入射角范围大,强度微弱,因此这些应用均要求光电探测器在能接收较宽角度范围的入射光的同时,具有高的灵敏度及量子效率。

[0016] 正是由于目前增透膜设计要求入射光垂直入射,在实际探测系统中,需要额外的探测器旋转控制系统,由于受到旋转控制系统速度的限制,扫描效率太低,因此进一步提出了与光电探测器配合的聚焦光学系统及通过增加探测器组成焦平面阵列,实现对各个方向信号的探测,但是额外的系统不仅提高了整个光电探测器模块的体积,更加大了实现难度。

发明内容

[0017] 本发明目的在于解决上述技术问题,提供一种广角的光电探测器结构及制备方法。

[0018] 本发明采用的技术方案是:

[0019] 一种光电探测器的制备方法,包括如下步骤:

[0020] 光刻步骤,在光电探测结构的上表面光刻出再构光敏面的图形,

[0021] 去除表面损伤层步骤,将所述光电探测结构置于 $60-100^\circ\text{C}$,20wt%的KOH溶液中,去除位于再构光敏面内的大约 $10\mu\text{m}$ 的表面损伤层;

[0022] 再构步骤,将所述光电探测结构置于 $60-100^\circ\text{C}$,3wt%的KOH及8vol%的异丙醇混合溶液中,在再构光敏面内形成广角结构。

[0023] 优选的,所述光刻步骤中还包括使用光刻胶保护光敏面外的区域的步骤;所述再构步骤之后还包括去除保护用的光刻胶的步骤。

[0024] 优选的,所述去除光刻胶步骤之后还包括如下步骤,在 $800-1200^\circ\text{C}$ 的湿氧环境下正面生长50nm的 SiO_2 ,光刻并腐蚀掉再构光敏面外的区域,形成钝化层。

[0025] 优选的,所述广角结构为所述再构光敏面的不平整表面,用以使斜入射光接触所述再构光敏面后产生的反射光的部分再次作为斜入射光进入至所述光电探测结构内。

[0026] 优选的,所述再构光敏面的不平整表面为规则的连续截面。

[0027] 优选的,所述再构光敏面的连续截面为锥形、梯形、矩形、球形、球形凹陷形,其图形占空比50%到100%。

[0028] 本发明还揭示了一种广角光电探测器,包括用于产生光电效应的光电探测结构,所述光电探测结构的上表面上设有再构光敏面,所述再构光敏面的上表面为不平整表面用以使斜入射光接触所述再构光敏面后产生的反射光的部分再次作为斜入射光进入至所述光电探测结构内。

[0029] 优选的,所述再构光敏面的上表面还设有钝化层,所述钝化层完全覆盖住所述再构光敏面,所述钝化层的材料为 SiO_2 、 SiN_x 、 MgF_2 、ITO。

[0030] 优选的,所述再构光敏面可应用于由硅、多晶硅、GaAs、GaN、InP、SiC、ZnO、SbI、碲

镉汞制备的光电探测结构上。

[0031] 优选的,所述光电探测结构为线性模式和盖革模式的雪崩光电探测器,或为PIN光电探测器,或为MSM光电探测器。

[0032] 本发明的有益效果在于:提供了一种广角光电探测器的制备方法,高效可靠,通过在光电探测器表面再构,打破菲涅尔反射系数入射角的限制,降低对入射波长的敏感度,不需加入额外的系统,仅通过单个光电探测器实现广角探测。

附图说明

[0033] 下面结合附图及实施例对本发明作进一步描述:

[0034] 图1:TE波从空气入射至硅材料表面,反射率随入射角的变化曲线图。

[0035] 图2:含100nm SiO₂增透膜的硅材料衬底对0°、30°及60°入射角的入射光的透射曲线图。

[0036] 图3:本发明的广角光电探测器的结构示意图。

[0037] 图4:斜入射光在本发明的再构光敏面上的入射光路示意图。

[0038] 图5至图9:本发明的再构光敏面的剖视示意图。

[0039] 图10:本发明的广角光电探测器的制备方法的各个步骤对应的剖面图。

具体实施方式

[0040] 本发明揭示了一种广角光电探测器,其结构如图3所示,自上而下依次包括:钝化层101、再构光敏面102和光电探测结构103。所述光电探测结构103用于产生光电效应,此为现有技术,在此不再赘述。结合图4所示,所述再构光敏面102的上表面为不平整表面用以使斜入射光接触所述再构光敏面102后产生的反射光的部分再次作为斜入射光进入至所述光电探测结构103内,所述钝化层101完全包覆住所述再构光敏面102。

[0041] 具体的,当入射光按照一定角度入射到光电探测结构103的再构光敏面102,由于入射点处实际入射角度发生变化,对于倾斜面降低了实际入射角度,因此能够提高倾斜入射光的透射率。与此同时,反射的光在多个界面中反射,增加透射进入半导体的几率,从而增加透射率,打破菲涅尔反射系数入射角的限制,降低对入射波长的敏感度,实现广角探测。

[0042] 本发明中的再构光敏面102,可以由化学腐蚀、激光刻槽、反应离子刻蚀、机械刻槽、外延生长等方法形成,再构结构深0.1μm到50μm。所述再构光敏面的表面形貌为规则的连续截面,可以为如图5至图9揭示的锥形、梯形、矩形、球形、球形凹陷等,其图形占空比50%到100%。

[0043] 本发明的光电探测结构103可以通过在再构光敏面102上增加钝化层101来修复因再构引入的表面损伤,降低表面复合,降低暗电流。并且,由于所述钝化层101具有一定的厚度,在1nm到10μm之间,因此其可以作为一种增透膜的存在。该钝化层101材料可以为SiO₂、SiN_x、MgF₂、ITO等。当然,如果处于成本的考虑,也可省去该钝化层101,即广角光电探测器仅仅包括光电探测结构和设于其上的再构光敏面,所述再构光敏面的至少部分表面为不平整表面,用以使斜入射光接触所述再构光敏面102后产生的反射光的部分再次作为斜入射光进入至所述光电探测结构103内。

[0044] 本发明的再构光敏面102适用于由硅、多晶硅、GaAs、GaN、InP、SiC、ZnO、SOI、碲镉汞等各种材料制备的光电探测器。

[0045] 本发明的再构光敏面102适用于线性模式和盖革模式的雪崩光电探测器,也适用于PIN光电探测器、MSM光电探测器等。

[0046] 下面描述一下本发明的广角光电探测器的制备方法。

[0047] 如附图10所示,光电探测结构103采用n型掺杂的硅材料制造的PIN光电探测器,其再构光敏面102以通过化学腐蚀的方法形成锥形为例,制备过程和方法如下:

[0048] 步骤(a)、在光电探测结构103的上表面光刻出再构光敏面102的图形,使用光刻胶104保护光敏面102外的区域;

[0049] 步骤(b)、将使用光刻胶104保护的光电探测结构103置于60-100℃,20wt%的KOH溶液中处理一段时间(大约40秒),去除位于再构光敏面102内的大约10μm的表面损伤层;

[0050] 步骤(c)、将使用光刻胶104保护的光电探测结构103置于60-100℃,3wt%的KOH及8vol%的异丙醇混合溶液中处理一段时间(大约30分钟),在再构光敏面102内形成倒金字塔的广角结构;

[0051] 步骤(d)、去除保护用的光刻胶104,在800-1200℃的湿氧环境下正面生长50nm的SiO₂,光刻并腐蚀掉再构光敏面102外的区域,形成钝化层101,即得到本发明优选实施例的广角光电探测器。

[0052] 本发明尚有多种实施方式,凡采用等同变换或者等效变换而形成的所有技术方案,均落在本发明的保护范围之内。

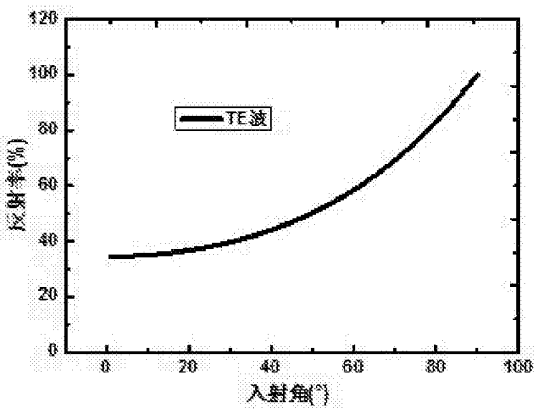


图1

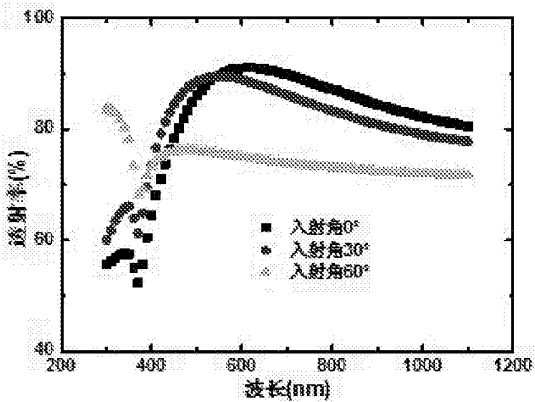


图2

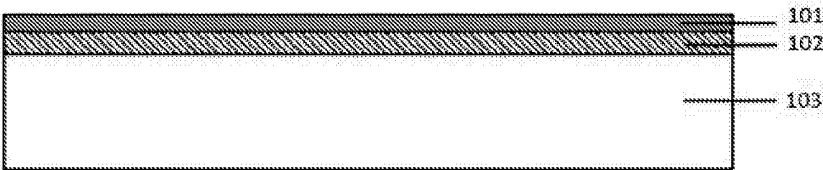


图3

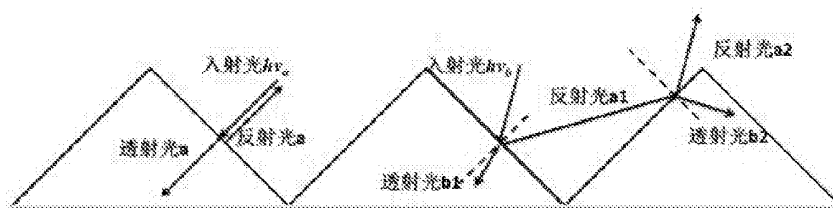


图4



图5



图6

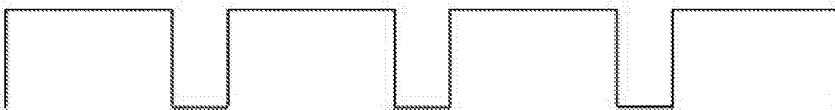


图7



图8



图9

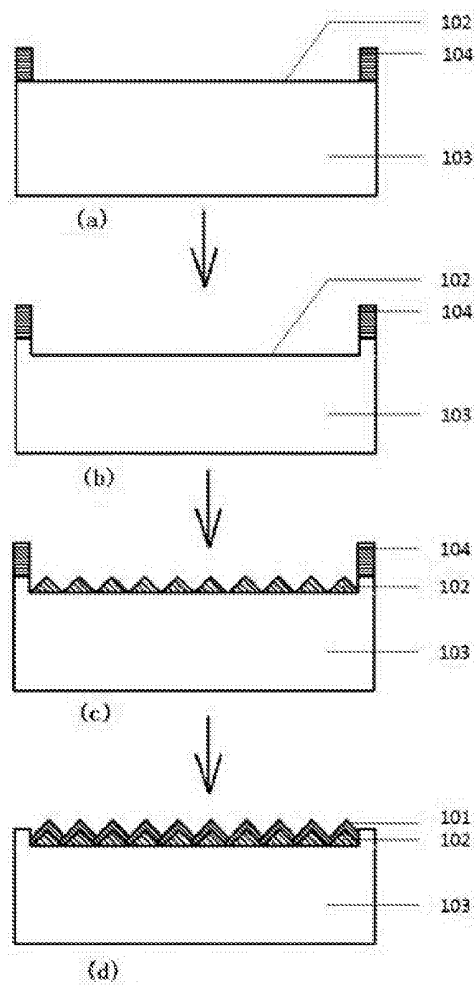


图10

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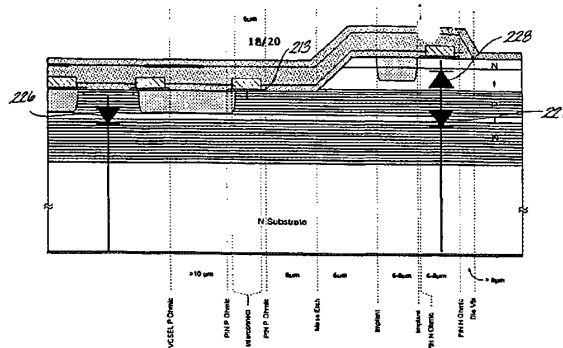
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(54) Title: A CLOSELY-SPACED VCSEL AND PHOTODETECTOR FOR APPLICATIONS REQUIRING THEIR INDEPENDENT OPERATION



(57) Abstract: A monolithically integrated VCSEL and photodetector, and a method of manufacturing the same, are disclosed for applications where the VCSEL and photodetector require separate operation such as duplex serial data communications applications. A first embodiment integrates a VCSEL with an MSM photodetector on a semi-insulating substrate. A second embodiment builds layers of a p-i-n photodiode on top of layers forming a VCSEL using a standard VCSEL process. The p-i-n layers are etched away in areas where VCSELs are to be formed and left where photodetectors are to be formed. The VCSELs underlying the photodetectors are inoperable, and serve to recirculate photons which are not initially absorbed back into the photodetector. The transmit and receive pairs are packaged into a single package for interface to multifiber ferrules. The distance between the devices is precisely defined photolithographically, thereby making alignment easier. In a further alternate embodiment, an FET is coupled to the p-i-n photodiode to form an integrated detector preamplifier along with the VCSEL transmitter all on the same optical reference plane.

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1 **A CLOSELY-SPACED VCSEL AND PHOTODETECTOR**
 FOR APPLICATIONS REQUIRING THEIR INDEPENDENT OPERATION

5 FIELD OF THE INVENTION

 The present invention relates to vertical cavity surface emitting lasers (VCSELs) and photodetectors, and more particularly to the application of such optoelectronic devices where they must operate independently but where it is also desirable to have a transmitter and a receiver closely-spaced.

10

 BACKGROUND OF THE INVENTION

 There are a number of data communications applications that make use of optoelectronic sending and receiving devices (i.e. light emitters and photodetectors). For fiber optic data communication applications requiring less than 200 MBits/sec, light emitting diodes (LEDs) are the light emitters of choice because they are relatively inexpensive to manufacture. For applications requiring higher speeds, lasers are typically used as the light emitters.

15

20 Until recently, most high speed data communications applications employed edge emitting lasers in a serial (single channel) format. With the advent of VCSELs, many such applications are now implemented using VCSEL arrays that can be interfaced to ferrules carrying multiple fibers to transmit several bits of data in parallel. At the receiving end, an array of photodetectors is coupled to the multiple fibers. The ability to manufacture VCSELs in arrays (an advantage of LEDs), combined with their high speed of operation (an advantage of lasers), makes VCSELs desirable in such applications.

25

30

 For high-speed serial duplex data communications applications, however, separately packaged light emitters (usually edge emitting lasers) and photodetectors are still employed. For long-haul applications (typically having distances greater than 1 kilometer), wavelength division multiplexing is often employed to transmit and receive data for a duplex channel over the same fiber. Because the primary cost of a long-haul duplex serial data channel resides in the

35

1 fiber and its installation, complex beam-splitting techniques
can be justified at the ends of the channel to separate the
transmit and receive data streams from the single fiber.

For short-haul or "premises" applications, however, the
5 cost of fiber and fiber installation is relatively less
important than the cost of the many transmit and receive
functions. Thus, it is the cost of the data transmit and
receive components, and particularly the optoelectronic
10 devices and their packaging, that drives cost considerations
for short-haul applications. Typical short-haul
implementations of a high-speed serial fiber optics data
communications channel operating in full duplex still employ
two multimode fibers, each one to connect an individually
packaged transmitting light emitter to an individually
15 packaged receiving photodetector. This is because the cost of
complex beam-splitting components often cannot be justified.

FIGS. 1(a) and 1(b) illustrate the components comprising
a typical implementation of a transmit or receive link for a
short-haul high-speed duplex data communications application.
20 FIG. 1(a) illustrates a fiber assembly 12. A round ferrule 26
houses an optical fiber 28, which is located precisely in the
center of ferrule 26. A typical diameter for ferrule 26 is
approximately 2.5 mm. Ferrule 26 comes with a latching
mechanism 30, which is used to clamp and secure the ferrule to
25 a barrel 32 of an optical sub-assembly 10, which is depicted
in Fig. 1(b). Barrel 32 houses optoelectronic device 14
typically in a TO can package 16 centrally located in the
barrel as shown. Optoelectronic device 14 is typically
located at an appropriate point within can 16 by a standoff 2.
30 Driver or amplifier circuitry is coupled to optoelectronic
device 14 through leads 22. A window 18 is provided in the
top of the can package to allow transmitted light out or
received light in, depending upon whether the optoelectronic
device is a light emitter or a photodetector. The TO package
35 is aligned with fiber 28 and epoxied using epoxy 24 to fix the
position of the optoelectronic device with respect to the
ferrule 26 and hence fiber 28. Optical elements such as lens
20 are typically provided to focus the light for optimal

1 optical efficiency, particularly where the light emitter is an
edge emitting laser. Barrel 32 is designed to mate with
latching mechanism 30 of fiber assembly 12.

Both fiber assembly 12 and barrel 10 are precision
5 manufactured for precise mating. Active alignment of TO
package 16 and optoelectronic device is ordinarily performed
in the x, y and z axes. First, the optoelectronic device is
precisely aligned within the package 16. Second, the package
16 is precisely aligned within barrel 10. Finally, optical
10 element 20 is precisely aligned with respect to its distance
from the optoelectronic device 14 to achieve proper optical
operation. Because a separate package is required for both
the transmit side and the receive side of the duplex data
channel, a total of twelve active alignments are typically
15 performed for each channel and each channel includes the cost
of eight precision-manufactured coupling parts.

FIGS. 1(c) and 1(d) provide schematic illustrations of
the fiber assembly 12 and optoelectronics subassembly 10 of
FIGS. 1(a) and 1(b), respectively.

20 FIG. 2 illustrates a typical duplex serial data
communications module 40, which has mounted to it an optical
subassembly 52 containing a light emitting device 13 disposed
in a TO can package 9 having a window 17, which is to be mated
with an optical fiber assembly 46 and which is dedicated to
25 data transmission. Module 40 also has an optical subassembly
50 mounted to it containing a photodetector 15 disposed in TO
can package 11 and which is to be mated with optical fiber
assembly 48 and dedicated to receiving data from a remote
module not shown. Because of the differing optical
30 requirements of the transmit and receive devices, the modules
must often be mounted in a staggered fashion as shown.
Moreover, the transmit devices are located at an optically
appropriate point in their can packages by standoffs 4 and 6
respectively.

35 Because of the cost of the precision components and the
large number of alignments required for implementing duplex
serial modules 40, it is highly desirable to integrate the
transmit and receive optoelectronic devices (i.e. light

1 emitter and photodetector) into one package. Integration of
the two devices into a single package is not, however, easily
achieved. The prior art implementations as illustrated in
FIGS. 1a-d and 2 cannot be readily adapted to multifiber
5 ferrules currently available for unidirectional data
transmission using VCSEL arrays. These multifiber ferrules
have fiber spacings which are typically about 250 microns and
can be less. The diameter of the TO can package 14 commonly
used in present implementations is itself 5600 microns in
10 diameter. Thus, the standard ferrule and barrel would have to
grow substantially in diameter to accommodate two fibers
having the spacing dictated by the TO cans housing the
optoelectronic devices.

Even if a substantially larger barrel could be created to
15 integrate the light emitter and photodetector as commonly
packaged to receive both a transmit and a receive fiber, it is
not clear that the resulting package could provide the
necessary separation of incoming and scattered outgoing light
beams to prevent crosstalk between the transmit and receive
20 signals (at least not without complex optics and possibly some
form of isolation). Although solutions have been disclosed to
stack a light emitter (typically an LED) on top of a
photodetector to transmit and receive wavelength division
multiplexed signals (the light emitter is transparent to the
received wavelength), beam-splitting must still be employed at
25 the opposite end.

Closely spaced VCSELs and photodetectors can suffer
leakage effects which can degrade the sensitivity of and
induce excess noise into the operation of the photodetector.
30 Also, current leakage from the VCSEL to the photodetector can
unacceptably alter the operating characteristics of the
photodetector over time.

Conventional photodetectors output low amplitude current
signals that are highly susceptible to noise and crosstalk
35 with the VCSEL. Therefore, conventional photodetectors
require highly sensitive interface electronics, typically
Gallium Arsenide (GaAs) for high speed, low noise integration
with the photodetector. The use of GaAs receiver electronics,

1 however, greatly adds to the cost of high speed data
communications.

5 Thus, there is room in the art for an improvement in the
area of optoelectronic device fabrication which facilitates
the integration of one or more pairs of transmit and receive
devices, without current leakage between them, for interfacing
with a single ferrule carrying one or more pairs of fibers
having spacings of 250 microns or less, to substantially
reduce the cost and complexity of implementing high-speed
10 serial duplex data communications channels including the cost
of receiver interface electronics.

SUMMARY OF THE INVENTION

15 It is therefore an objective of the present invention to
provide a VCSEL device sufficiently close to a photodetector
device to permit the use of commercially available multifiber
ferrules having fibers spaced on the order of 750 microns to
250 microns or less. Ferrules having fiber spacing of 750
microns are referred to as having a small form factor (SMFF).

20 An exemplary embodiment of the present invention provides
closely-spaced but independently operable optoelectronic
devices by monolithically integrating the two devices on the
same substrate. The invention also provides a process by
which multiple pairs of VCSELs and photodetectors can be
25 arrayed on the same substrate. The invention further provides
a process by which the closely-spaced but independently
operable optoelectronic devices can be packaged using known
lead-frame or ceramic packaging technologies. The invention
may be used to integrate any requisite optics with either the
30 semiconductor manufacturing technology or the packaging
technology.

35 The invention simplifies significantly the alignment of
the fibers to the closely-spaced optoelectronic devices by
taking advantage of the photolithographic nature of monolithic
semiconductor processing to precisely define the separation
between the optoelectronic devices.

 The invention also provides closely-spaced but
independently operable VCSEL and photodetector pairs capable

1 of near-field operation requiring no optics and which permit
butt coupling between a package containing the optoelectronic
devices and a flat faced multifiber ferrule.

5 In a first preferred embodiment of the invention, one or
more VCSELs are formed using a known process for manufacturing
such devices. The one or more VCSELs comprise an n-type GaAs
substrate and a first mirror formed on the substrate, which is
a well-known distributed Bragg reflector (DBR), and a first
10 spacer or cladding layer which is formed on top of mirror.
This first mirror is also preferably doped n-type. An active
region is then formed on top of the first cladding layer, the
active region comprising at least one quantum well layer or
bulk layer. A second spacer or cladding layer is formed on
the active region, with a second DBR being formed on the
15 second spacer layer and doped to have p-type conductivity.

On top of the VCSEL layers is grown an etch-stop layer of
AlGaAs having about 90% or greater Al content. An extended p-
type layer of AlGaAs having more typical alloy proportions is
then grown on top of the etch-stop layer. On top of this p-
20 type layer is grown an intrinsic layer (i) which is undoped
GaAs. On top of the intrinsic layer is grown an n-type region
of AlGaAs. An etching process is then performed to etch away
the extended p, i, and n layers where the one or more VCSELs
are to be formed. The etching process uses the etch-stop
25 layer to mark the end of the etching process so that the VCSEL
area has exposed the top surface of an appropriately designed
mirror. A proton implant region is created which separates
the one or more VCSELs and the photodetectors formed by the
unetched p, i, and n layers. Anode contacts are formed over
30 the non-implanted p regions to form apertures for the VCSELs.
A VCSEL cathode contact is formed on the substrate. Anode
contacts are also formed on the p region of the p-i-n
photodiode and a cathode contact is made to the n region of
the p-i-n photodiode.

35 Thus, in this preferred embodiment, a VCSEL circuit can
be isolated from a p-i-n photodiode using a proton implant
isolation region which is commonly used to isolate VCSELs
formed in arrays. The anode contacts to the p region of the

1 p-i-n photodiode may be coupled to ground so that the VCSEL
structure which lies underneath the p-i-n photodiode is never
turned on and other bipolar parasitic effects are avoided.
The width of the proton implant isolation region is typically
5 between 50 and 100 microns. Thus, the VCSEL and the p-i-n
photodiode can be separated by an accurately known distance,
significantly less than 25 microns if desired. Moreover, the
difference in thickness between the VCSEL and the p-i-n
photodiode is small, thereby permitting near-field coupling of
10 the optoelectronic devices to fibers.

One significant advantage of the first embodiment of the
invention is that it requires very few additional steps to an
otherwise typical VCSEL manufacturing process. A second
advantage is that, when an anti-reflection coating of silicon
15 nitride is applied to the photo-receiving n region of the
photodiode, in conjunction with the p-type mirror which
underlies the p-i-n photodiode, a high degree of efficiency is
achieved. The silicon nitride anti-reflection coating
increases transmission of incoming light into the surface of
20 the p-i-n photodiode. Additionally, any light which is not
absorbed by the intrinsic layer of the photodiode on its way
through will be reflected from the underlying p-type mirror
back into the intrinsic layer and will then have a second
opportunity to be absorbed.

25 Another embodiment of the invention employs a VCSEL with
an MSM photodiode. The VCSEL is manufactured on a semi-
insulating substrate. Because the MSM photodetector employs
the semi-insulating layer as its common cathode, the two
optoelectronic devices are virtually isolated from one another
30 electronically as a result. A photolithographically defined
minimum spacing of 250 microns or less can also be achieved
using the second preferred embodiment of the invention. An
anti-reflection coating is also preferably employed over the
MSM photodetector to increase efficiency. To further enhance
35 electrical isolation between the two devices, an isolation
region can also be formed, preferably by implantation.
Another advantage of using an MSM photodiode is that the two

1 anode terminals can be used to drive a differential amplifier,
thereby permitting common-mode rejection of noise.

Each embodiment can be integrated with optically
transmissive materials that can be formed into lenses on the
5 surface of the semiconductor. Either embodiment can also be
implemented within standard precision manufactured barrels to
be aligned with circular ferrules containing multiple fibers.
Finally, either embodiment can be encapsulated using known
lead-frame or ceramic packaging technology to permit near-
10 field flat coupling between a flat package having an optically
transmissive surface and a commercially available flat
rectangular ferrule containing multiple fibers.

A further embodiment of the present invention provides a
low cost method of repeatably manufacturing a closely-spaced
15 or small form factor (SMFF) package for optical transceivers.
The system includes a highly insulative, proton implantation
region that isolates the photodetector and eliminates current
leakage (i.e. crosstalk) between the VCSEL and photodetector.
In an alternate embodiment of the present invention, the
20 photodetector is integrated with a FET to form a high speed
integrated detector preamplifier on a single chip.

In one aspect, the present inventions provides a method
of manufacturing monolithic VCSEL and photodetector pairs by
forming VCSEL layers directly on a semiconductor wafer
25 substrate by forming first mirror layers, forming a first
cladding layer on the first mirror layers, forming an active
region on the first cladding layer, forming a second cladding
layer on the active region, forming second mirror layers on
the second cladding layer, forming photodiodes distributed
30 across the wafer, and defining active and inactive VCSELs by
forming isolation regions around the second mirror layers of
the active VCSELs.

In another aspect, the present inventions provides method
of manufacturing monolithic VCSEL and photodetector pairs by
35 forming VCSEL layers directly on a semiconductor wafer
substrate by forming first mirror layers, forming a first
cladding layer on the first mirror layers, forming an active
region on the first cladding layer, forming a second cladding

1 layer on the active region, forming second mirror layers on
the second cladding layer, forming photodiodes distributed
across the wafer, and defining active and inactive VCSELs by
forming proton implant isolation regions around the second
5 mirror layers of the active VCSELs.

In a still further aspect, the present invention provides
a method of manufacturing monolithic VCSEL and photodetector
pairs by forming VCSEL layers directly on a semiconductor
wafer substrate by forming first mirror layers, forming a
10 first cladding layer on the first mirror layers, forming an
active region on the first cladding layer, forming a second
cladding layer on the active region, forming second mirror
layers on the second cladding layer, forming photodiodes
distributed across the wafer, and defining active and inactive
15 VCSELs by forming proton implant isolation regions 50-100
microns wide around the second mirror layers and extending
vertically through the second mirror layers to the second
cladding layer.

In still another aspect, the present invention provides
20 a method of manufacturing monolithic VCSEL and photodetector
pairs by forming VCSEL layers directly on a semiconductor
wafer substrate by forming first mirror layers, forming a
first cladding layer on the first mirror layers, forming an
action region on the first cladding layer, forming a second
25 cladding layer on the active region, forming second mirror
layers on the second cladding layer, forming photodiodes
distributed across the wafer, and forming VCSEL anode contacts
overlapping a topmost second mirror layer and the isolation
region of the active VCSELs.

30 In still another aspect, the present invention provides
a method of manufacturing monolithic VCSEL and photodetector
pairs by forming VCSEL layers directly on a semiconductor
wafer substrate, then forming photodiodes distributed across
the wafer directly on the semiconductor wafer substrate at
35 discrete locations.

In still another aspect, the present invention provides
a method of manufacturing monolithic VCSEL and photodetector
pairs by forming VCSEL layers directly on a semiconductor

1 wafer substrate by forming first mirror layers, forming a
first cladding layer on the first mirror layers, forming an
active region on the first cladding layer, forming a second
cladding layer on the active region, forming second mirror
5 layers on the second cladding layer, defining active regions
and inactive regions by forming isolation regions in the VCSEL
layers, and then forming photodiodes distributed across the
wafer on the second mirror layers of inactive VCSELs.

In still another aspect, the present invention provides
10 a method of manufacturing monolithic VCSEL and photodetector
pairs by forming VCSEL layers directly on a semiconductor
wafer substrate by forming first mirror layers, forming an
active region on the first cladding layer, forming a second
cladding layer on the active region, forming second mirror
15 layers on the second cladding layer, forming photodiodes
distributed across the wafer by forming distributed p-type
layers on a topmost second mirror layer, forming an intrinsic
layer on the distributed p-type layers, forming an n-type
layer on the intrinsic layers, forming a photodiode cathode
20 contact on each of the n-type layers, and forming distributed
photodiode anode contacts on the topmost second mirror layer.

In another aspect, the present invention provides a
method of manufacturing an integrated VCSEL and photodetector
pair by forming layers of VCSEL on a semiconductor substrate,
25 forming layers of a photodiode on a top-most layer of a first
portion of the VCSEL layers, isolating a second portion of the
VCSEL layers from the photodiode layers by implanting an
isolation region between the first and second portions of the
VCSEL layers, forming a VCSEL cathode contact connected to the
30 semiconductor substrate, forming a VCSEL anode contact
connected to the top-most VCSEL layer in the second portion,
forming a photodiode cathode contact on a topmost layer of the
photodiode layers, and forming a photodiode anode contact on
the top-most VCSEL layer of the first portion of the VCSEL
35 layers.

The present invention provides a method of manufacturing
an integrated VCSEL and photodetector pairs by forming VCSEL
layers directly on a semiconductor wafer substrate, then

1 forming photodiodes distributed across the VCSEL layers at
discrete locations, forming active and inactive regions of the
VCSEL by forming isolation regions in the VCSEL layers, and
isolating the VCSEL from the photodiodes by forming proton
5 implant isolation regions around the photodiodes.

The present invention further provides a method of
manufacturing an integrated VCSEL and photodetector pairs by
forming VCSEL layers directly on a semiconductor wafer
substrate; then forming photodiodes on the VCSEL at discrete
10 locations, forming a photodiode n-type contact (cathode) on
the upper most photodiode layer; and forming a photodiode p-
type contact (anode) on the upper most VCSEL layer, forming a
VCSEL p-type contact (anode) on the topmost VCSEL layer;
forming a VCSEL n-type contact (cathode) coupled to the
15 semiconductor substrate; forming active and inactive regions
of the VCSEL by creating isolation regions in the VCSEL
layers; then isolating the VCSEL layers from the photodiodes
by forming proton implant isolation regions around the
photodiodes.

20 In another aspect, the present invention provides a
method of manufacturing monolithic VCSEL and photodetector
pairs by forming VCSEL layers directly on a semiconductor
wafer substrate, then forming an etch stop layer on the VCSEL
layers, then forming photodiodes distributed across the wafer
25 directly on the etch stop layer at discrete locations.

In still another aspect, the present invention provides
a method of manufacturing monolithic VCSEL and photodetector
pairs by forming VCSEL layers directly on a semiconductor
wafer substrate by; forming first mirror on the substrate,
30 forming a cladding layer on the first mirror, forming an
active region on the first cladding layer, forming a second
cladding layer on the active region, forming a second mirror
on the second cladding layer, forming an etch stop layer on
the second mirror, forming photodiodes distributed across the
35 wafer at discrete locations by forming distributed p-type
layers on a top most second mirror layer, forming an intrinsic
layer on the distributed p-type layers, forming an n-type
layer on the intrinsic layers, forming a photodiode n-type

1 contact on each of the n-type layers, and forming distributed
photodiode p-type contacts on the topmost second mirror.

In still another aspect, the present invention provides
a method of manufacturing monolithic VCSEL and photodetector
5 pairs by: forming VCSEL layers directly on a semiconductor
wafer substrate; then forming an etch stop layer directly on
the VCSEL; then forming photodiode layers distributed across
said etch stop layer at discrete locations then forming a
photodiode n-type contact (cathode) on said upper most
10 photodiode layer; and forming a photodiode p-type contact
(anode) on said upper most VCSEL layer; then forming a VCSEL
p-type contact (anode) on said topmost VCSEL layer; forming a
VCSEL n-type contact (cathode) coupled to said semiconductor
substrate; defining active and inactive regions of the VCSEL
15 by forming isolation regions in the VCSEL layers; then
isolating said VCSEL layers from said photodiodes layers by
forming proton implant isolation regions around said
photodetector.

In still another aspect, the present invention provides
20 a method of manufacturing monolithic VCSEL and photodetector
pairs by: forming VCSEL layers directly on a semiconductor
wafer substrate; then forming photodiode layers distributed
across the VCSEL layers at discrete locations; forming a
photodiode n-type contact (cathode) on said upper most
25 photodiode layer; and forming a photodiode p-type contact
(anode) on said upper most VCSEL layer; forming a VCSEL p-type
contact (anode) on said topmost VCSEL layer; forming a VCSEL
n-type contact (cathode) coupled to said semiconductor
substrate; defining active and inactive regions of the VCSEL
30 by forming isolation regions in the VCSEL layers; then
isolating said VCSEL layers from said photodiodes layers by
forming proton implant isolation regions around said
photodiodes, forming interconnect metal pads on said
photodiode anode and cathode and VCSEL anode; forming a
35 dielectric matching layer on said VCSEL layers; forming vias
in the dielectric matching layer for the interconnect metal
pads; forming an anti-reflective coating on said
photodetector.

1 In still another aspect, the present invention provides
a method of manufacturing a monolithic VCSEL and integrated
photodetector preamplifier by: forming VCSEL layers directly
on a semiconductor wafer substrate; then forming an etch stop
5 layer on the uppermost VCSEL layer; forming photodiodes
distributed across said wafer directly on said VCSEL layers at
discrete locations; then forming one or more transistors
coupled to the photodiode.

 In still another aspect, the present invention provides
10 a method of manufacturing an integrated photodetector
preamplifier by forming photodiodes directly on a
semiconductor wafer substrate, and then forming one or more
transistors coupled to the photodiodes.

15 BRIEF DESCRIPTION OF THE DRAWINGS

 The foregoing objectives and the features of the
preferred embodiments of the present invention will be better
understood by those skilled in the art with reference to the
following detailed description in conjunction with the
20 accompanying drawings, wherein:

 FIG. 1(a) (prior art) illustrates a fiber assembly of a
typical implementation of a high-speed data transmission link
using a single optoelectronic device for each half of a duplex
channel;

25 FIG. 1(b) (prior art) illustrates an optical assembly of
a typical implementation of a high-speed data transmission
link using a single optoelectronic device for each half of a
duplex channel;

 FIG. 1(c) (prior art) illustrates a schematic view of the
30 fiber assembly of Fig. 1(a) and the optical assembly of Fig
1(b);

 FIG. 1(d) (prior art) illustrates the high-speed duplex
data communications module using known precision manufactured
parts to implement the transmit and receive links of a high-
35 speed duplex data communications channel of Fig. 2;

 FIG. 2 (prior art) illustrates a high-speed duplex data
communications module using known precision manufactured parts

1 to implement the transmit and receive links of a high-speed duplex data communications channel;

FIG. 3 illustrates a cross-section of an integrated VCSEL and an MSM photodetector in accordance with the present invention;

FIG. 4 illustrates a monolithic plan view of a preferred embodiment of the invention;

FIG. 5a illustrates a cross-section of a VCSEL and a p-i-n photodiode in accordance with the present invention;

10 FIG. 5(b) illustrates the orientation of the VCSEL laser diode and p-i-n photodiode as illustrated by the cross-section in FIG. 5(a);

FIG. 6(a) (prior art) illustrates a commercially available dual fiber version of a round fiber ferrule;

15 FIG. 6(b) (prior art) illustrates a commercially available rectangular multifiber ferrule;

FIG. 7(a) illustrates how the present invention can be packaged using conventional lead-frame technology to facilitate interface to a rectangular multifiber ferrule.

20 FIG. 7(b) illustrates how optical lenses can be integrated with the present invention;

FIG. 7(c) illustrates how the present invention can be implemented using butt coupling technology;

25 FIG. 8 illustrates how a transmit and receive pair made in accordance with the present invention can be packaged to interface with a round multifiber ferrule such as the one illustrated in Fig. 6(a);

30 FIG. 9 is a cross-sectional view of a conventional VCSEL structure deposited upon a semiconductor substrate having a p-i-n photodiode formed on the VCSEL in accordance with an exemplary embodiment of the present invention;

FIG. 10(a) is a cross-section of a conventional VCSEL structure deposited upon a semiconductor substrate with a p-i-n photodiode formed on the VCSEL having an integrated n-ohmic ring formed on the photodiode in accordance with an exemplary embodiment of the present invention;

FIG. 10(b) is a top view demonstrating the integration of a p-i-n photodiode mesa on a VCSEL with an n-ohmic ring

1 formed on the photodiode in accordance with an exemplary
embodiment of the present invention;

FIG. 11(a) is a cross-section of a VCSEL with an
integrated p-i-n photodiode mesa, with an n-ohmic ring formed
5 on the photodiode in accordance with an exemplary embodiment
of the present invention;

FIG. 11(b) is a top view demonstrating the integration of
the p-i-n photodiode mesa on a VCSEL, with an n-ohmic ring
formed on the photodiode mesa in accordance with an exemplary
10 embodiment of the present invention;

FIG. 12(a) is a cross-section of a VCSEL and associated
p-ohmics, integrated with a p-i-n photodiode mesa, having a
n-ohmic ring formed on the mesa and a p-ohmic ring formed on
the photodiode mesa, in accordance with an exemplary
15 embodiment of the present invention;

FIG. 12(b) is a top view demonstrating the integration of
the p-i-n photodiode mesa on a VCSEL, with n-ohmic and p-
ohmic rings in accordance with an exemplary embodiment of the
present invention;

20 FIG. 13(a) is a cross-section demonstrating the
integration of proton implant isolation regions in accordance
with an exemplary embodiment of the present invention;

FIG. 13(b) is a top view demonstrating the integration of
the p-i-n photodiode mesa on a VCSEL, with proton implant
isolation regions in accordance with an exemplary embodiment
25 of the present invention;

FIG. 14(a) is a cross-sectional view demonstrating the
integration of Ohm vias into the dielectric layer for the
photodiode and VCSEL in accordance with an exemplary
30 embodiment of the present invention;

FIG. 14(b) is a top view demonstrating the integration
Ohm vias into the dielectric layer for the photodiode and
VCSEL in accordance with an exemplary embodiment of the
present invention;

35 FIG. 15(a) is a cross-section demonstrating the
integration of interconnect metal pads for the VCSEL and
photodiode ohmic contacts in accordance with an exemplary
embodiment of the present invention;

1 FIG. 15(b) is a top view demonstrating the integration
of interconnect metal pads for the VCSEL and photodiode ohmic
contacts in accordance with an exemplary embodiment of the
present invention;

5 FIG. 16(a) is a cross-section demonstrating the
integration of a VCSEL dielectric matching layer with
photodiode via in accordance with an exemplary embodiment of
the present invention;

10 FIG. 16(b) is a top view demonstrating the integration
of a VCSEL dielectric matching layer with photodiode via in
accordance with an exemplary embodiment of the present
invention;

15 FIG. 17(a) is a cross-section demonstrating the
integration of a one quarter wavelength anti-reflective
coating on the photodiode in accordance with an exemplary
embodiment of the present invention;

20 FIG. 17(b) is a top view demonstrating the integration of
a one quarter wavelength anti-reflective coating on the
photodiode in accordance with an exemplary embodiment of the
present invention;

FIG. 18(a) is a cross-section demonstrating the mask
layout to produce the present invention in accordance with an
exemplary embodiment of the present invention;

25 FIG. 18(b) is a top view demonstrating the mask layout to
produce the present invention in accordance with an exemplary
embodiment of the present invention;

30 FIG. 19 is a perspective view demonstrating the
integration of an FET with a p-i-n photodetector to form an
integrated photodetector and preamplifier in accordance with
an exemplary embodiment of the present invention; and

FIG. 20 is a top view of a transmit / receive / amplifier
circuit integrated onto one wafer which utilizes low cost wire
bond / lead frame technology in accordance with an exemplary
embodiment of the present invention.

35

DETAILED DESCRIPTION OF THE INVENTION

The present invention generally pertains to a monolithic
semiconductor device having a VCSEL integrated with a

1 photodetector on the same substrate, the VCSEL and
photodetector to be operated independently as a transmit and
receive device respectively. The VCSEL and photodetector are
physically situated in close enough proximity to permit
5 packaging of one or more pairs of the VCSEL and photodetector
such that they may be coupled to multifiber ferrules having
fiber spacings on the order of 250 microns or less. The
present invention also includes a method of manufacturing the
independently operated VCSEL and photodetector, as well as the
10 packaging and coupling of one or more pairs of the integrated
VCSEL and photodetector and their coupling to multifiber
ferrules.

A first preferred embodiment of the invention is now
discussed in detail in conjunction with FIGS. 3 and 4. As
15 shown in FIG. 3, a VCSEL and a metal-semiconductor-metal (MSM)
photodetector are integrated on the same semi-insulating GaAs
substrate. The conductance of the semi-insulating substrate
is typically between about 10^{-12} and 10^{-5} ohm-cm. The VCSEL is
built on top of the substrate beginning with an n- layer 68,
20 upon which an n+ layer 70 is grown which forms the cathode of
the VCSEL.

A first mirror 78 is formed on layer 70, which is
preferably an epitaxially formed distributed Bragg reflector
(DBR) which comprises a plurality of alternating semiconductor
25 layers having high and low indices of refraction, with each
layer having a thickness of $\lambda/4n$, where λ is the wavelength of
the optical radiation emitted from the laser and n is the
index of refraction of the layer. The semiconductor layers
are doped to achieve n-type conductivity. A quantum well (QW)
30 active region 74 is formed between a first spacer 73 and a
second spacer 75, with first spacer 73 formed on the top layer
of the first mirror. Active region 74 has at least one QW
layer.

A second mirror 76 is formed on second spacer 75 and is
35 preferably an epitaxially grown DBR which is comprised of a
plurality of alternating semiconductor layers having high and
low indices of refraction, with each layer having a thickness
of $\lambda/4n$, where λ is the wavelength of the optical radiation

1 emitted from the laser and n is the index of refraction of the
layer. The second mirror 76 is doped to achieve a p-type
conductivity. An isolation implant 80 is formed around the
second mirror 76, and preferably extends to a depth just
5 inside spacer 75. A mesa region is then etched around the
outside of the VCSEL 89 to a depth which exposes the cathode
layer 70. A cathode contact 72 is then formed on the exposed
surface of cathode layer 70, and an anode contact 82 is formed
which overlaps the surface of isolation implant region 80 and
10 the topmost layer of second mirror 76, and which further
defines an aperture 88 which comprises a portion of the
surface of the top-most layer of second mirror 76. Radiation
84 is emitted through aperture 88.

The MSM photodetector 62 is formed on the surface of the
15 semi-insulating substrate 60 as two non-electrically coupled
metal patterns 62 and 64, each having fingers which are
interdigitated with one another. When one or both of the
patterns is biased to some voltage, carriers generated by
received light are swept to the anodes of the two diodes by
20 the applied electric field. Because the MSM operates without
conducting any current through the substrate 60, there is
virtually no electrical crosstalk or leakage between the VCSEL
89 and the MSM photodetector 62. Thus, the VCSEL 89 can emit
radiation 84 from aperture 88 based on digital data to be
25 transmitted while MSM photodetector 62 can receive radiation
86 in which is encoded digital data received from a remote
data source. To achieve even better isolation, an isolation
region 80 can be formed preferably by proton implant between
VCSEL 89 and MSM photodetector 62.

30 FIG. 4 illustrates a plan view of the device which is
shown as a cross-section in FIG. 3. For clarity,
corresponding structures will be indicated by identical index
numbers. The cathode layer 70 and its metal cathode contact
72 of the VCSEL are extended to the boundary of substrate 60
35 which is furthest away from MSM photodetector 86. Bond wire
71 can then be used to connect cathode contact 72 to a bond
pad of, for example, a lead frame. The VCSEL anode contact 82
is brought to the same substrate boundary by bond wire 77,

1 metal extender 79 and bond wire 69. Metal patterns 66 and 64,
which form the anode and anode terminals of MSM photodetector
62, are also bonded to the leads of whatever form of packaging
is used. One of the metal patterns is typically coupled to a
5 bias voltage while the other is coupled to ground or a
different bias voltage. An anti-reflection coating can be
employed on the MSM to increase optical efficiency.

A second preferred embodiment is disclosed in FIG. 5a.
For convenience and clarity, like structures will be denoted
10 by the same index numbers as in previous figures. This
particular embodiment is preferred because it can be
implemented using more standard VCSEL manufacturing processes.
A first mirror 78 is formed on a standard semiconductor GaAs
substrate 79. The first mirror is preferably a semiconductor
15 DBR comprising twenty to thirty periods of AlAs/AlGaAs layers.
Each of the layers has a thickness of $\lambda/(4n)$ and is doped to
have n-type conductivity. A first spacer or cladding layer 73
is then formed on first mirror 78, which is either undoped or
very lightly doped. An active region 74 is then formed on the
20 first spacer 73 which comprises at least one GaAs QW layer.
A second mirror 76 is then formed on top of a second undoped
or very lightly doped spacer or cladding layer 75. The second
mirror 76 again preferably consists of alternating layers of
AlAs/AlGaAs layers, each being $\lambda/(4n)$ thick. Second mirror 76
25 is doped to have p-type conductivity. On top of second mirror
76 is formed a thin etch-stop layer 93, which has a
significantly higher ratio of Al to Ga, about 9 to 1 or
greater. On top of the etch-stop layer 93, an extended p-type
layer 100 of AlGaAs is formed. On top of p-type layer 100 is
30 formed an intrinsic layer (i) 102 of undoped GaAs. Finally, an
n-type layer 104 is formed on top of intrinsic layer 102.

The structure is then etched in those areas where a VCSEL
is to be formed, and not etched where a p-i-n photodiode is to
be formed. The etch strips away the n-type layer 104 and
35 intrinsic layer 102 and continues into p-type layer 100 until
the etch-stop layer 93 is detected. The etching process is
terminated so that the etch-stop layer is etched away and an
appropriately thick top layer of second mirror 76 is exposed.

1 Those of skill in the art will recognize that there are other
well-known techniques by which the endpoint of an etching
process may be detected to end the etching process at the
appropriate time and which are intended to be within the scope
5 of the present invention.

A proton isolation implant is performed to create
isolation region 80 between VCSEL 92 and p-i-n photodiode 90.
The implant region 80 typically achieves a depth which extends
just inside spacer layer 75 and has a width preferably between
10 about 50 and 100 microns. A circular metal contact 82 is then
formed on the top of mirror 76 and which overlaps slightly
implant region 80. Contact 82 provides access to the anode of
VCSEL 92. A contact 81 is then formed on the back side of
substrate 79 and serves as the cathode terminal of VCSEL 92.
15 Contacts 94 are preferably formed on both sides of p-i-n
photodiode 90 which provide electrical access to the anode of
p-i-n photodiode 90 as well as to the anode of the VCSEL 91
which underlies p-i-n photodiode 90. Finally, contact 96 is
formed on n-type layer 104 to form the cathode of p-i-n in
20 photodiode 90. An anti-reflection coating preferably having
a thickness of about one quarter wavelength is applied to
photo-receiving surface 101.

A simplified schematic of the structure of FIG. 5a is
shown in FIG. 5b. VCSEL 92 is operated with forward bias
25 between anode terminal 82 and cathode terminal 98 to produce
radiation 84 having a wavelength of λ . In an exemplary
embodiment p-i-n photodiode 90 is operated with reverse bias
between cathode contact 96 and anode contacts 94. Moreover,
anode contacts 94 are shorted to substrate contact 98 to
30 ensure that VCSEL 91 will not become forward biased and emit
light. Thus, VCSEL 92 can be operated to emit light encoded
with data to be transmitted to a remote receiver employing a
similar structure, and p-i-n photodiode 90 can operate to
receive radiation 86 which is encoded with data received from
35 the same remote terminal.

Those of skill in the art will recognize that one of the
many advantages of the second preferred embodiment of FIG. 5a
is that a typical process used to create arrays of VCSELs,

1 including the isolation implant commonly used to separate the
individual VCSELs of the array, can be used to create arrays
of VCSEL/p-i-n photodiode pairs. The additional steps
5 required to build the p-i-n photodiode on top of the VCSEL
process are negligible in cost. Moreover, the difference in
the thickness of the two devices is also negligible for
purposes of facilitating near-field coupling of the devices to
fibers to eliminate the need for optics. Additionally, due to
10 the underlying second mirror of inoperable VCSEL 91, any light
not absorbed by the intrinsic layer 102 of p-i-n photodiode 90
will be reflected back into intrinsic layer 102, thus having
a second chance to be absorbed. Finally, the thicker the
intrinsic layer, the lower the capacitance of the p-i-n diode
(the faster its operation) and the better its optical
15 efficiency.

FIG. 6(a) illustrates how the commonly used single fiber
round ferrule can be implemented using two or more fibers.
Such fibers are now currently available from Siecor as
prototypes. The cylindrical ferrule 110 has the same
20 dimensions (i.e., 2.5 mm) as those ferrules commonly used with
only one fiber. Thus, one fiber 112 can be used for
transmitting data as coupled to a VCSEL while fiber 114 can be
used to receive data from a remote transmitter as coupled to
a photodetector.

25 FIG. 6(b) illustrates a commonly available rectangular
ferrule which can have eight or more fibers 122, and which has
guides 120 for receiving alignment pins. Rectangular ferrule
116 typically has a polished face 118 for coupling to an array
of transmitting VCSELs. This rectangular ferrule 116 can be
30 easily adapted to devices made in accordance with the present
invention, such that each pair of fibers 122 can be aligned
with a pair of integrated VCSEL/photodetectors.

FIG. 7(a) illustrates how a single VCSEL/photodetector
pair could be packaged using standard lead-frame technology to
35 be interfaced to a rectangular multifiber ferrule such as the
one illustrated in Fig. 6(b). Integrated transmit/receive
chip 130 can be epoxied to lead frame 128 and then bonded to
bond pads 141 via bond wires 143. If optics are required,

1 lenses 138 and 136 can be formed over VCSEL 89, 92 and
photodetector 62,90 respectively, either using materials which
are formed over chip 130 during the manufacturing of chip 130
or such optics can be integrated within the surface of the
5 plastic encapsulation formed by the package. Lead frame 128
can also have guide pins 140 to be used in conjunction with a
rectangular ferrule such as the one shown in FIG. 6(b). FIG.
7(b) shows a side view of FIG. 7a to illustrate the use of
optics over photodetector 62, 90 and VCSEL 89, 92.

10 FIG. 7(c) illustrates how lead frame 128 can be butt
coupled to a rectangular ferrule 150 containing two fibers 124
and 126. If distance 160 is fairly precisely known, and
distance 147 between fibers 124 and 126 is fairly precise, a
fairly accurate alignment can be achieved between fibers 124
15 and 126 and VCSEL 89, 92 and photodetector 62, 90 because the
distance between VCSEL 89, 92 and photodetector 62, 90 are
fairly precise based on the photo-optical alignment process
used in manufacturing the integrated semiconductor 130. Thus,
a fairly accurate positioning of the chip 130 with respect to
20 the lead frame 128 during packaging will provide a reasonably
accurate passive alignment. Of course, fine alignment can be
achieved using well-known active alignment techniques. A
further advantage of the coupling technique shown in FIG. 8 is
that no optics must be interposed between package 146 and
25 ferrule 150 if the coupling distance 152 is close enough. Of
course, a flat transmissive surface 148 can be easily achieved
on package 146.

Fig. 8 illustrates a lead-frame package which can be used
to interface with a round multifiber ferrule such as the two-
30 fiber ferrule of Fig. 6(a). Barrel 127 is designed to
precisely mate with the round ferrule of Fig. 6(b)

An alternate embodiment of the present invention relates
to a monolithic semiconductor device having a VCSEL integrated
with a photodetector and preamplifier on the same substrate,
35 the VCSEL and photodetector to be operated independently as a
transmit and receive device respectively. The present
invention also includes a method of manufacturing the

1 independently operated VCSEL and photodetector with an
integrated FET preamplifier.

This alternate embodiment of the present invention is
implemented using standard VCSEL manufacturing techniques.
5 The conventional VCSEL portion 200 of this alternative
embodiment of the present invention as shown in FIG. 9
includes a substrate 201, a first or lower mirror 202, an
optical cavity 203, and a second or upper mirror 204. The
substrate 201 is made of gallium arsenide (GaAs) or any other
10 suitable material. The first and second mirrors 202, 204 are
comprised of multilayered distributed Bragg reflectors, (DBRs)
as is conventional in the art.

In this alternate embodiment, aluminum gallium arsenide
(AlGaAs) and aluminum arsenide (AlAs), with varying
15 concentrations of aluminum and gallium are used to fabricate
the upper and lower mirrors 202, 204. The optical thickness
of each mirror layer is typically designed to be a quarter
wavelength of the emitted light of the laser where the optical
thickness is given by the product of the physical thickness
20 and the index of refraction.

The conventional optical cavity 203 includes an active
region surrounded by first and second cladding regions. The
first and second cladding regions are made of AlGaAs in the
exemplary embodiment. In the active region 203, at least one
25 quantum well made of GaAs is disposed on adjacent barrier
layers made of $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$. As is generally understood in the
art, the number of and materials forming the quantum wells and
surrounding barrier layers can be varied depending on the
design.

30 In this alternate embodiment, the first or lower mirror
202 is doped to n-type conductivity while the second or upper
mirror 204 is doped to have p-type conductivity. The p-type
second mirror 204 is capped by a layer of GaAs 205 which is
approximately 100 Angstroms thick.

35 A thin etch stop layer 206, consisting of approximately
100-200 Angstroms of AlAs is deposited on the p-type mirror
cap 205. On top of the etch stop layer 206 an additional
intrinsic i-type layer 207 is deposited, consisting of an

1 absorbing GaAs material. The p-doping extends through the AlAs
etch stop layer 206 into the i-type region 207 to avoid
heterostructural barriers and band problems. Finally an n-
type layer 208 of $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ is formed on top of the
5 intrinsic layer 207 with a thin GaAs cap.

This alternate embodiment minimizes photodetector pulse
deformation due to minority carrier drift within the p-i-n
photodiode 211 structure. The GaAs i-type layer 207 absorbs
light at 850 nanometer whereas the n-type layer 208 is non
10 absorbent at this wavelength. Therefore photon absorption is
confined to the i-type layer 207 wherein the photons are
removed by the reverse electric fields. If photocarrier
absorption occurs in the n-type region 208 or the p-type
region 204 on either side of the i-type region 207, minority
15 photons are absorbed, and minority carriers are generated.
There is no electric field within the background doped n-type
region 208 or p-type region 204 to remove these minority
carriers. These minority carriers must then drift and diffuse
through normal diffusion processes eventually being swept into
20 the i-type region 207. These diffusion processes may deform
the shape of the photodetector output pulse by creating a long
time tail to the trailing edge of the pulse.

As shown in the cross-sectional view of FIG. 10(a)
circular n-ohmic 209 is formed to make contact with the
25 photodiode n-type region 208 while the surface is planar. FIG.
10 (b) is a top view of the ring contact 209 deposited on the
n-type region 208. The structure is then masked and etched
in those areas where the transmit VCSEL 210 is to be formed,
FIG. 11(a), and not etched where the photodetector 211 is to
30 be formed. There are well known techniques by which the
endpoint of an etching process may be detected to end the
etching process at the appropriate time. A disadvantage of
these etch techniques is the non uniformity of etch rates over
the surface of the wafer. Etch rate variation is created by
35 fluid motion, surface effects, light effects and various other
phenomenon. This variation in etch rate results in
imperfections in the surface finish of the VCSEL and added
complexity in the manufacturing control process.

1 In response to the drawbacks of the prior art, this
alternate embodiment of the present invention incorporates an
AlAs etch stop layer 206 to facilitate selective etching of
the upper n-type region 208 and i-type region 207. The n-type
5 region 208 and i-type region 207 are etched using a known
combination of citric acid with a high percentage of peroxide.
When the etch solution reaches the etch stop layer 206 the
peroxide interacts with the AlAs to form an oxide surface.
The citric acid solution is not sufficiently strong to remove
10 the aluminum oxides so that the oxide surface in effect
inhibits or stops the etch. This selective etch technique
removes the time critical aspect of conventional etch
techniques and greatly simplifies the manufacturing process.
From a timing standpoint, the device can now be over etched
15 assuring the uniform removal of the upper n-type region 208
and i-type region 207 over the entire surface of the VCSEL
210.

Next, the etch stop layer 206 is removed using an
alternate etch solution which will not etch the GaAs cap 205
20 on the upper p-type mirrors 204. Preferably, a solution of
hydrochloric acid, with 10 percent water is used to remove
the etch stop layer. As is shown in FIG. 11(a), a
photodetector mesa 211, with a slight undercut in the AlAs
etch stop layer 206, is closely coupled to a surrounding VCSEL
25 210. The present invention achieves the required device
uniformity without implementation of rigorous process controls
required by other known techniques. FIG. 11(b) is a top view
of the photodetector mesa 211 with integrated n-type contact
209.

30 Referring to FIG. 12(a) in this alternate embodiment of
the present invention, a metal contact 212 is formed on the
bottom of the substrate 201 and serves as the cathode 212
terminal of the VCSEL 210. The contact metalization forming
the n-ohmic contact 212 on the bottom of the substrate 201 may
35 be, for example, eutectic gold germanium deposited by electron
beam evaporation or sputtering. Additionally, p-ohmic
contacts 213, 214, and 215 are then formed on the top of the
second or upper mirror 204. As shown in the top view of FIG.

1 12(b) a circular metal contact 213 is formed on the outside of
the photodetector 211, while at the same time circular
contacts 214, 215 are formed on the upper most surface 205 of
the VCSEL 210. The top contact metalization forming p-ohmic
5 contacts 213, 214, and 215 may be, for example, gold with 2%
beryllium added or a layered structure of
titanium/platinum/gold, preferably deposited by electron beam
evaporation.

In this alternate embodiment of the present invention a
10 proton implant forms an isolation region 216 between the VCSEL
210 and the photodetector 211 (FIG 13(a)). The standard
proton implantation process that is used for current
constriction within the conventional VCSEL 217, 218, may be
used to create a highly insulative ring 216 (top view FIG.
15 13(b)) around the photodetector 211 thereby isolating the
VCSEL 210 structure from the photodetector 211. In the top
view of FIG. 13(b) it can be seen that a guard band 216 of
highly insulative material is formed between the n-type
contact 209 and the p-ohmic contact 213 of the photodetector
20 211.

This alternate embodiment has several advantages over
prior art isolation mechanisms. For example, the operating
time constants of a p-i-n photodetector 211 are inversely
proportional to the capacitance of the device. The capacitance
25 of the device is directly proportional to the surface area of
the device. As is shown in the top view of FIG. 13(b) the
highly insulative proton implant region 216 decreases the
active surface area of the device, thereby reducing the
capacitance of the device and increasing the maximum operating
30 speed of the photodetector 211.

The photodetector proton implant region 216 also
increases the sensitivity of the photodetector 211 by
eliminating leakage paths through which current could
otherwise flow between the VCSEL 210 and the photodetector
35 211. Typical photodetectors must receive very low optical
power levels so that most photodetectors are low current
devices. Therefore, a relatively small amplitude leakage
current can severely degrade the sensitivity of the

1 photodetector 211 by introducing excess noise into the
receiver system as well as unacceptably changing the
performance of the p-i-n photodetector 211 over time. The
proton implant region 216 effectively stops electrical
5 conduction at the edge of the highly resistive proton implant
region 216 between the p-type contact 213 and n-type contact
209, thereby eliminating all leakage paths.

Current constriction within the conventional VCSEL 210
is provided by using proton implant regions 217 and 218 to
10 creating active and inactive regions of the VCSEL. The VCSEL
proton implant regions 217 and 218 convert the upper mirror
DBR 204 into areas of high resistivity around the active VCSEL
210 device. The VCSEL proton implant regions 217, 218
typically achieve depths which extend just inside the spacer
15 layer. In this alternate embodiment of the present invention,
the thicknesses of the photodetector 211 i-type region 207
and n-type region 208 are chosen so that the implant depth
that is appropriate for the VCSEL 210 is also appropriate for
the photodetector 211.

20 The forced commonality between the proton implant region
217, 218 of the VCSEL 210 and the proton implant region 216 of
the photodetector 211 allows for a more efficient
manufacturing process. The process sequence that was
appropriate for the VCSEL 210, with a modified mask layout is
25 also appropriate for the photodetector 211. Therefore, all
proton implantations 216, 217 and 218 can be performed in a
single process step with a single mask layout.

Referring to FIG. 13(a) the photodetector proton implant
region 216 completely transects the n-type region 207 and
30 penetrates into the i-type region 208. However, the proton
implant region 216 does not penetrate the p-type region 204
providing a conduction path to the p-type contact 213, to
maintain the required continuity between the n-type contact
209 and p-type contact 213 of the photodetector 211. In this
35 alternate embodiment of the present invention, the n-type
region 208 is approximately 3000 Angstroms thick, the
absorbing i-type region 207 is approximately 2.5 microns in
thickness and the area where the p-type region extends over

1 into the i-type region 207 is approximately 2000 Angstroms so
that the entire thickness of the photodetector mesa 211 is
approximately 3 microns.

5 A dielectric protective layer 219 (FIG 14(a)) is
deposited to protect the outermost surface 205 of the VCSEL
210 and the photodetector 211. Silicon nitride is preferably
used for the dielectric protective layer 219. Therefore, vias
must be etched into the dielectric protective layer 219 to
10 provide access to the p-type contacts 214 and 215 of the VCSEL
210, as well as the n-type contact 209 and p-type contact 213
of the photodetector 211.

A thicker inter-connect metal 220 and 221 is deposited on
the photodetector n-type contact 209 and p-type contact 213
respectively, as shown in the cross section of FIG. 15(a).
15 Also, a thicker inter-connect metal 222 and 223 is deposited
on the p-type contacts 214 and 215 of VCSEL 210. The inter-
connect metal deposits 220-223, provide a low resistance, good
electrical conductor contact for wire bonding, probing, etc.
The metal deposits used for the n-type and p-type contacts
20 209, 213-215, are generally very thin and relatively high
resistance and are designed for transitioning from metal to
semiconductors through ohmic contacts that have a non-barrier
between the work function of the two materials. Therefore,
the inter-connect metal is chosen to provide low contact
25 resistance for current flow. FIG. 15(b) shows a top view of
the interconnect metal 220 and 221 integrated with the
photodetector 211.

In an alternate embodiment of the present invention, a
dielectric phase shifting layer 224, is preferably disposed on
30 the conventional VCSEL structure 210 (FIG. 16(a)). The
dielectric phase shifting layers 224 increase the total
transmission out of the VCSEL 210 as is disclosed in U.S.
Patent Application "VERTICAL CAVITY SURFACE EMITTING
CONSISTENT SLOPE EFFICIENCIES", Application No. 09/237,580;
35 the contents of which are incorporated herein by reference.
In this alternate embodiment of the present invention,
deposition of the dielectric phase shifting layers 224 is
halted prior to the deposition of the last quarter optical

1 wavelength of the material. The dielectric phase shifting
layers 224 are then completely etched off the photodetector
211 as shown in FIG. 16(a). Next a quarter optical wavelength
of the dielectric material 225 is deposited over the VCSEL 210
5 to complete it's mirror as well as on the photodetector 211 to
create an anti-reflective coating(FIG 17(a)). The quarter
optical wavelength material is preferably silicon nitride as
is known in the art.

When the anti-reflective coating 225 of silicon nitride
10 is applied to the photodetector 211 n-type region, in
conjunction with the p-type region of the upper mirror 204,
which underlies the photodiode 211, a high degree of
efficiency is achieved. The anti-reflective coating 225
increases the transmission of incoming light into the p-i-n
15 photodiode structure 211. Additionally, any light that does
not get absorbed in the i-type region 207 is reflected off the
upper mirror 204 of the VCSEL 210 and is absorbed as it
propagates back through the i-type region 207 for the second
time. Because of this double pass mechanism the absorption
20 characteristics of the i-type region 207 is twice what it
otherwise would be, providing excellent quantum efficiencies,
and very high response at gigabit speeds.

In an alternate embodiment of the present invention, a
variable tuning layer is deposited on the outer surface of the
25 dielectric phase shifting layer 224. The variable tuning
layer facilitates predictable adjustment of the optical
efficiency of the laser during fabrication to achieve lasers
with substantially similar slopes on a wafer to wafer basis.
The manufacture and use of a variable tuning layer is
30 disclosed in U.S. Provisional Patent Application "ENCAPSULATED
LASER WITH CONTROLLED SLOPE EFFICIENCY", Application No.
60/125,916, filed on March 24, 1999, the contents of which are
hereby incorporated by reference. In this alternate
embodiment the initial VCSELs are tested by any conventional
35 technique, preferably on a representative sample, to determine
characteristics of the initial VCSELs, such as the slope
efficiency distribution.

1 The thickness of the variable thickness dielectric layer
required to tune the slope efficiency distribution to within
the target specification is calculated. This calculated
thickness is then used to interrupt the prior layer
5 deposition, etch the dielectric layers off the photodetector
and then deposit the remaining phase shifting layer thickness
and tuning layer. If the calculated thickness of the
dielectric tuning layers was $1/8$ of a wavelength, the phase
shifting layer deposition would be interrupted at $1/8$ of a
10 wavelength less complete, the dielectric would be etched off
the photodetector 211 and the remaining phase shifting layer
dielectric and tuning layer thickness would be deposited. The
combination of the two materials would then be a quarter
wavelength to complete the design of the anti-reflective
15 coating 225 for the photodetector 211.

FIG. 18(a) is a cross section of the present invention,
including the mask layout, with approximate dimensions, for
manufacturing this alternate embodiment of the present
invention. Also shown are the p-i-n laser 226, a parasitic
20 VCSEL 227 underneath the photodetector 211 and the p-i-n photo
diode 228. The p-type contact 213 of the p-i-n photodetector
211 may be coupled to ground so that the parasitic VCSEL 227
structure which lies underneath the p-i-n photodetector 211 is
never turned on and other bipolar parasitic effects are
25 avoided.

Referring to Fig. 19, in an alternate embodiment of the
present invention, an epitaxial n-i-p structure, 230, 231 and
232 respectively, along with highly insulative proton implant
regions 233 and 234, are used to integrate a FET onto the
30 photodetector 211 to create an integrated detector pre-
amplifier. FIG. 19 shows a perspective view of the integrated
detector pre-amplifier 229. Metal deposits are formed on the
outer most surface 235 of the photodetector 211 to form the
source 236, gate 237 and drain 238 on an n-type channel of a
35 typical transistor structure. In this alternate embodiment
the proton implant regions 233 and 234 intersect the back of
the source 236, gate 237 and drain 238 as well as the lower
surface of the source 237 and drain 238. In this way the

1 proton implant regions 233 and 234 form an isolated conductive region 239 or well, within a highly insulative field formed by the proton implantations 233 and 234.

5 The width of the conductive region is arbitrary and can be tailored to produce a predetermined transistor. To achieve gigabit data communication rates, the length of the gate 237, which is the critical transistor design parameter, can be on the order of one micron. The GaAs layer upon which the metal layers are deposited is a highly conductive material also with
10 very good frequency response. A one micron metal deposit is well within reasonable process control technology known in the art. The gate 237, is typically a layered structure of titanium, platinum and gold which can be deposited by any suitable method known in the art, such as by sputtering or
15 electron beam vaporization. The thicknesses of the metal deposit is typically 500A, 1000A, 3000A for the Ti, Pt, Au respectively as is well known in the GaAs transistor art.

The source 236 and the drain 238 are typically layered structures of Nickel with Gold on Gold Germanium, n- ohmics.
20 The nickel acts as a barrier to prohibit the gold from interfusing with the gold germanium and changing the eutectics of the gold germanium. In the preferred embodiment of the present invention a ratio of 88 percent gold to 12 percent germanium is used to form a eutectic which has a phase melting
25 point near 360°C to make a good ohmic contact.

This alternate embodiment of the present invention is less susceptible to receiver noise, crosstalk, etc. than conventional photodetector designs. The coupled FET and photodetector create an integrated detector pre-amp such that
30 the output signal of the photo detector is amplified by the FET and converted from a current signal to a voltage signal. Therefore, a relatively large voltage signal is being modulated rather than a low level current signal.

In conventional SMFF transceiver designs, the
35 photodetector is susceptible to crosstalk from the high drive currents of the VCSEL as well as receiver noise and other degradations to receiver sensitivity. In this alternate embodiment the photo detector is integrated on the same mesa

1 as the amplifying transistor circuitry so that the output
signals of the integrated detector pre-amp are no longer very
low current signals that are sensitive to noise, crosstalk and
the like but are more stable amplified voltage signals.

5 The signal to noise ratio of conventional optical
receiver is limited by the front end noise. Currently, front
end receivers which interface with conventional high speed
photodetectors, utilize GaAs technology because high speed,
highly sensitive, low noise performance is required to
10 accurately amplify the low level current output of the
conventional photodetector.

In this embodiment of the present invention, the low
noise circuitry is integrated with the photodetector on the
same wafer. In this embodiment the integrated amplifier is
15 realized with relatively simple transistor circuits. The
transistor circuits are readily implemented with techniques
known in the art without resorting to the highly integrated
processes required for GaAs integrated circuits. These
relatively simple transistor circuits are generally bond pad
20 limited. Coupling the photodetector to the transistors
eliminates capacitance and bond wire inductance which
otherwise limit system performance. The amplified output
signal of the integrated detector preamplifier, which is no
longer susceptible to noise and other degradations, allows the
25 front end receiver amplifier to be implemented with CMOS
integrated circuit technology that is comparably a much lower
cost than the more complex GaAs integrated circuit technology
required for conventional photodetectors.

In an alternate embodiment of the present invention the
30 integrated detector preamplifier is coupled with VCSEL
transmit technology to provide a closely spaced transmit 241,
receive 242, amplifier 243 circuit 240 on a single integrated
circuit chip as shown in the top view of FIG. 20.
Conventional transceiver designs require closely coupled high
35 speed integrated circuitry for reduced delay times. The high
speed integrated circuitry generally considerable power
dissipation and heat to the packaged system. The integrated
device with the wire bonds 244 coming off the VCSEL and

1 integrated receive amplifier can then be mounted onto lead
frames 245, which is a low cost packaging technology.

5 The transmit/receive amplifier circuit embodiment of the
present invention has the added benefit of being relatively
easy to manufacture. This alternate embodiment of the present
invention is implemented using standard VCSEL manufacturing
techniques and process sequences as previously described. The
AlAs etch stop layer would be deposited on a conventional
VCSEL. On top of the etch stop layer an additional intrinsic
10 i-type layer is deposited, consisting of an absorbing GaAs
material. The p-doping extends through the AlAs etch stop
layer into the i-type region to avoid heterostructural
barriers and band problems. Finally an n-type layer of
 $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ is formed on top of the intrinsic layer with a
15 thin GaAs cap.

Next the transistor, source 236, gate 237 and drain 238
and n-type contacts 209 for the photodetector 211 are
deposited preferably by electron beam evaporation. In this
alternate embodiment the source 236 and drain 238 contacts are
20 the same n-type contact that was used for the photodetector
209. Next selective etching to expose the VCSEL and form the
integrated photodetector preamplifier mesa is performed. The
p-type contacts 213, 214 and 215 may then be deposited,
preferably by electron beam evaporation, followed by a proton
25 implantation for the transistor 233 & 234, photodetector guard
ring 216 and VCSEL 217.

As previously described, dielectric layers are next
deposited. Dielectric material is deposited on the transistor
to decrease degradation and increase the operating life of the
device. Silicon nitride is the preferred dielectric material.
30 Next vias are etched into the dielectric layers to allow the
interconnect metal 220, 221, 222 and 223 to be deposited.
Finally an anti-reflective coating 225 is applied to the
photodetector 211.

35 It should be noted that a number of variations to the
inventions described above will be apparent to those skilled
in the art. For example, the p-i-n photodiode can be
deposited directly on a semiconductor substrate along with the

1 proton implant guard ring to create a high performance
photodetector. In this alternate embodiment the device
capacitance can be matched exactly with the mask design and
the reverse bias to achieve complete depletion of the i-type
5 region as is required for high speed performance. In
addition, the above photodetector can be integrated with the
FET to form a high speed integrated detector preamplifier.
The VCSEL could include a power monitoring photodetector,
wherein the monitoring photodetector may be below the VCSEL or
10 on the side or in another location within the package to
provide controlled monitoring and feedback.

Those of skill in the art will recognize that the exact
order in which the process steps take place, as well as the
particular material system used, are irrelevant to the
15 patentability of the present invention. For example, one
material system might include a GaAs substrate, GaAs quantum
wells, DBR layers of AlAs and AlGaAs, and an intrinsic layer
of GaAs. The p and n layers of the p-i-n would also be made of
AlGaAs. Other known material systems may be used to produce
20 different wavelengths of emitted radiation and the particular
dimensions of the integrated devices may be changed to suit
particular transmission modes or packaging requirements.
Moreover, although it is desirable that the
photolithographically defined spacings between the transmit
25 and receive pairs are preferably small, of course larger
spacings can be easily accommodated by the present invention.

30

35

1 CLAIMS

1. A method of manufacturing monolithic VCSEL and photodetector pairs, said method comprising the steps of:
forming VCSEL layers directly on a semiconductor wafer
5 substrate;
forming photodetectors distributed across said wafer directly on said VCSEL layers at discrete locations;
defining active and inactive regions of the VCSEL by forming isolation regions in the VCSEL layers; and
10 isolating said VCSEL layers from said photodetectors layers by forming proton implant isolation regions around said photodetectors.
2. The method of claim 1 further comprising the step of:
15 prohibiting operation of said inactive VCSELs by short circuiting said semiconductor wafer substrate to said photodiode anode contact to ensure that said active VCSELs will not become forward biased.
3. A method of manufacturing monolithic VCSEL and photodetector pairs, said method comprising the steps of:
forming VCSEL layers directly on a first side of a semiconductor wafer substrate;
forming photodiode layers distributed across said VCSEL
25 layers at discrete locations;
forming a photodiode n-type contact (cathode) on an uppermost photodiode layer;
forming a photodiode p-type contact (anode) on an uppermost VCSEL layer;
30 forming a VCSEL p-type contact (anode) on an uppermost VCSEL layer;
forming a VCSEL n-type contact (cathode) on a second side of said semiconductor substrate;
defining active and inactive regions of the VCSEL by
35 forming isolation regions in the VCSEL layers; and
isolating said VCSEL layers from said photodiodes layers by forming proton implant isolation regions around said photodiodes.

1 4. The method of claim 3 wherein the step of forming VCSEL
 layers directly on a semiconductor wafer substrate further
 comprises:

 forming first mirror layers on a semiconductor wafer;
5 forming a first cladding layer on said first mirror
 layer;
 forming an active region on said first cladding layer;
 forming a second cladding layer on said active region;
 and
10 forming second mirror layers on said second cladding
 layer.

 5. The method of claim 3 wherein the step of forming said
 photodiode layers directly on said VCSEL layers further
15 comprises:

 forming distributed p-type layers on said VCSEL layers;
 forming an intrinsic layer on said distributed p-type
 layers; and
 forming an n-type layer on said intrinsic layers.

20 6. The method of claim 3 wherein the step of forming
 photodiode layers directly on said VCSEL layers at discrete
 locations further comprises:

 forming said photodiode layers distributed across said
25 VCSEL layers; and
 selectively removing said photodiode layers from said
 VCSEL layers at discrete locations.

 7. The method of claim 3 further comprising the step of:
30 prohibiting operation of said inactive VCSELs by short
 circuiting said semiconductor wafer substrate to said
 photodiode anode contact to ensure that said active VCSELs
 will not become forward biased.

35 8. A method of manufacturing monolithic VCSEL and
 photodetector pairs, said method comprising the steps of:

 forming VCSEL layers directly on a first side of a
 semiconductor wafer substrate;

1 forming an etch stop layer directly on said VCSEL layers;
 forming photodiode layers distributed across said etch
stop layer at discrete locations;
 forming a photodiode n-type contact (cathode) on an
5 uppermost photodiode layer;
 forming a photodiode p-type contact (anode) on an
uppermost VCSEL layer;
 forming a VCSEL p-type contact (anode) on an uppermost
VCSEL layer;
10 forming a VCSEL n-type contact (cathode) on a second side
of said semiconductor substrate;
 defining active and inactive regions of the VCSEL by
forming isolation regions in the VCSEL layers; and
 isolating said VCSEL layers from said photodiodes layers
15 by forming proton implant isolation regions around said
photodetector.

9. The method of claim 8 wherein the step of forming VCSEL
layers directly on a semiconductor wafer substrate further
20 comprises:
 forming first mirror layers on a semiconductor wafer;
 forming a first cladding layer on said first mirror
layer;
 forming an active region on said first cladding layer;
25 forming a second cladding layer on said active region;
and
 forming second mirror layers on said second cladding
layer.

30 10. The method of claim 8 wherein the step of forming said
photodiode layers directly on said etch stop layer further
comprises:
 forming distributed p-type layers on said VCSEL layers;
 forming an intrinsic layer on said distributed p-type
35 layers; and
 forming an n-type layer on said intrinsic layers.

- 1 11. The method of claim 8 wherein the step of forming
photodiode layers directly on said etch stop layer at discrete
locations further comprises:
forming said photodiode layers distributed across said
5 etch stop layer;
selectively removing said photodiode layers from said
etch stop layer at discrete locations, and
selectively removing said etch stop layer from said
uppermost VCSEL layer where said photodiode layers have been
10 selectively removed.
12. The method of claim 11 wherein the etch stop layer is
aluminum arsenide.
- 15 13. The method of claim 12 wherein the step of selectively
removing said photodiode layers from said etch stop layer at
discrete locations comprises selectively etching said
photodiode layers using a solution of citric acid with a high
percentage of peroxide.
- 20 14. The method of claim 12 wherein the step of selectively
removing said etch stop layer comprises selectively etching
said etch stop layer using a solution of hydrochloric acid
with water.
- 25 15. The method of claim 6 further comprising the step of:
prohibiting operation of said inactive VCSELs by short
circuiting said semiconductor wafer substrate to said
photodiode anode contact to ensure that said active VCSELs
30 will not become forward biased.
16. A method of manufacturing monolithic VCSEL and
photodetector pairs, said method comprising the steps of:
forming VCSEL layers directly on a first side of a
35 semiconductor wafer substrate;
forming photodiode layers distributed across said VCSEL
layers at discrete locations;

- 1 forming a photodiode n-type contact (cathode) on an
uppermost photodiode layer;
 forming a photodiode p-type contact (anode) on an
uppermost VCSEL layer;
5 forming a VCSEL p-type contact (anode) on an uppermost
VCSEL layer;
 forming a VCSEL n-type contact (cathode) on a second side
of said semiconductor substrate;
 defining active and inactive regions of the VCSEL by
10 forming isolation regions in the VCSEL layers;
 isolating said VCSEL layers from said photodiodes layers
by forming proton implant isolation regions around said
photodiodes;
 forming interconnect metal pads on said photodiode anode
15 and cathode and VCSEL anode;
 forming a dielectric phase shifting layer on said VCSEL
layers;
 forming vias in the dielectric phase shifting layer for
the interconnect metal pads; and
20 forming an anti-reflective coating on said photodetector.
17. The method of claim 16 further comprising the step of:
 prohibiting operation of said inactive VCSELs by short
circuiting said semiconductor wafer substrate to said
25 photodiode anode contact to ensure that said active VCSELs
will not become forward biased.
18. A method of manufacturing a monolithic VCSEL and
integrated photodetector preamplifier, said method comprising
30 the steps of:
 forming VCSEL layers directly on a semiconductor wafer
substrate;
 forming photodiodes distributed across said wafer
directly on said VCSEL layers at discrete locations; and
35 forming one or more transistors coupled to the
photodiodes.

1 19. The method of claim 18 wherein the step of forming VCSEL
layers directly on a semiconductor wafer substrate comprises:
forming first mirror layers on a semiconductor wafer;
forming a first cladding layer on said first mirror
5 layer;
forming an active region on said first cladding layer;
forming a second cladding layer on said active region;
and
forming second mirror layers on said second cladding
10 layer.

20. The method of claim 18 wherein the step of forming said
photodiode layers directly on said VCSEL layers comprises:
forming distributed p-type layers on said VCSEL layers;
15 forming an intrinsic layer on said distributed p-type
layers; and
forming an n-type layer on said intrinsic layers.

21. The method of claim 19 wherein the step of forming
20 photodiode layers directly on said VCSEL layers at discrete
locations comprises:
forming said photodiode layers distributed across said
VCSEL layers; and
selectively removing said photodiode layers from said
25 VCSEL layers at discrete locations.

22. The method of claim 20 wherein the transistor is a FET.

23. The method of claim 22 wherein the step of forming a FET
30 comprises:
forming insulating regions on the surface of said
photodiode materials wherein said insulating regions form a
conductive well for the FET and isolate said photodiodes from
said VCSEL;
35 forming ohmic electrical contacts for a source and drain
which overlap said insulating regions and conductive well; and

- 1 forming a contact for the gate within the conductive well
formed by the isolation regions on the uppermost photodetector
layer.
- 5 24. A method of manufacturing a monolithic VCSEL and
integrated photodetector and preamplifier, said method
comprising the steps of:
 forming VCSEL layers directly on a semiconductor wafer
substrate;
- 10 forming an etch stop layer on an uppermost VCSEL layer;
 forming photodiodes distributed across said wafer directly
on said etch stop at discrete locations; and
 forming one or more transistors coupled to the photodiode.
- 15 25. The method of claim 24 wherein the step of forming VCSEL
layers directly on a semiconductor wafer substrate further
comprises:
 forming first mirror layers on a semiconductor wafer;
 forming a first cladding layer on said first mirror layer;
- 20 forming an active region on said first cladding layer;
 forming a second cladding layer on said active region; and
 forming second mirror layers on said second cladding
layer.
- 25 26. The method of claim 25 wherein the step of forming said
photodiode layers directly on said etch stop layer further
comprises:
 forming distributed p-type layers on said VCSEL layers;
 forming an intrinsic layer on said distributed p-type
- 30 layers; and
 forming an n-type layer on said intrinsic layers.
27. The method of claim 26 wherein the step of forming
photodiode layers directly on said etch stop layer at discrete
- 35 locations comprises:
 forming said photodiode layers distributed across said
etch stop layer;

1 selectively removing said photodiode layers from said etch
stop layer at discrete locations, and
 selectively removing said etch stop layer from said VCSEL
layer where said photodiode layers have been selectively
5 removed.

28. The method of claim 27 wherein the etch stop layer is
aluminum arsenide, with high content of aluminum.

10 29. The method of claim 28 wherein the step of selectively
removing said photodiode layers from said etch stop layer at
discrete locations comprises selectively etching said
photodiode layers using a solution of citric acid with a high
percentage of peroxide.

15 30. The method of claim 28 wherein the step of selectively
removing said etch stop layer comprises selectively etching
said etch stop layer using a solution of hydrochloric acid with
water.

20 31. The method of claim 26 wherein the transistor is a FET.

32. The method of claim 28 wherein the step of forming a FET
comprises:

25 forming insulating regions around said photodiodes wherein
said insulating regions form a conductive well for the FET and
isolate said photodiodes from said VCSEL;

 forming first a electrical contact for a source and a
second electrical contact for a drain on said insulating
30 regions; and

 forming a third electrical contact for a gate within the
conductive well formed by the insulating regions.

33. A method of manufacturing a semiconductor photodetector,
35 said method comprising the steps of:

 forming distributed photodiodes on a semiconductor
substrate by forming p-type layers directly on a semiconductor
substrate;

1 forming an intrinsic layer on said p-type layers;
 forming an n-type layer on said intrinsic layers; and
 forming a proton implant isolation region between the p-
type contact and the n-type contact (cathode) of the
5 photodiodes.

34. A method of manufacturing an integrated photodetector
preamplifier, said method comprising the steps of:
 forming photodiodes directly on a semiconductor wafer
10 substrate; and
 forming one or more transistors on said photodiodes.

35. The method of claim 34 wherein the step of forming said
photodiode layers directly on said semiconductor substrate
15 further comprises:
 forming distributed p-type layers on said VCSEL layers;
 forming an intrinsic layer on said distributed p-type
layers; and
 forming an n-type layer on said intrinsic layers.

20 36. The method of claim 35 wherein the transistor is an FET.

37. The method of claim 36 wherein the step of forming a FET
further comprises:
25 forming insulation regions around said photodiodes wherein
said insulation regions form a conductive well for the FET;
 forming a first electrical contact for a source and a
second electrical contact for a drain, wherein said first and
second electrical contacts overlap said insulation regions and
30 conductive well on an uppermost photodiode layer; and
 forming a third electrical contact for a gate within the
conductive well formed by the insulation regions on said
uppermost photodiode layer.

35 38. A monolithic optical transmitter and receiver pair
comprising:
 a substrate;
 an optical transmitter formed on said substrate;

1 an optical receiver formed laterally adjacent to said
optical transmitter; and
 an isolation region that electrically isolates said
optical transmitter from said optical receiver.

5 39. The monolithic optical transmitter and receiver pair of
claim 38 wherein the optical receiver comprises a photodiode.

 40. The monolithic optical transmitter and receiver pair of
10 claim 38 wherein the optical transmitter comprises a VCSEL with
a plurality of layers.

 41. The optical transmitter of claim 40 wherein the plurality
of VCSEL layers further comprises:

15 a first mirror layers on a semiconductor wafer;
 a first cladding layer on said first mirror layer;
 an active region on said first cladding layer;
 a second cladding layer on said active region; and
 a second mirror layers on said second cladding layer.

20 42. The optical receiver of claim 39 wherein the photodiode
further comprises:

 distributed p-type layers formed on said VCSEL layers;
 an intrinsic layer formed on said distributed p-type
25 layers; and
 an n-type layer formed on said intrinsic layers.

 43. A monolithic optical transmitter and receiver pair
comprising:

30 a substrate;
 a multi-layer VCSEL structure formed on said substrate;
 a photodiode formed on said VCSEL structure at discrete
locations;

 a first proton implant isolation region within said VCSEL
35 structure defining active and inactive regions of the VCSEL
structure; and

 a second proton implant isolation region formed around
said photodiode.

1

44. The monolithic optical transmitter and receiver pair of claim 43 wherein the VCSEL structure further comprises:

5

first mirror layers on a semiconductor wafer;
a first cladding layer on said first mirror layer;
an active region on said first cladding layer;
a second cladding layer on said active region; and
a second mirror layers on said second cladding layer.

10

45. The monolithic optical transmitter and receiver pair of claim 43 wherein the photodiode further comprises:

distributed p-type layers formed on said VCSEL layers;
an intrinsic layer formed on said distributed p-type layers; and

15

an n-type layer formed on said intrinsic layers.

46. A monolithic optical transmitter and receiver pair comprising:

20

a substrate;
a multi-layer VCSEL structure formed on said substrate;
an etch stop layer formed on the uppermost layer of said VCSEL;

a photodiode formed on said etch stop layer at discrete locations;

25

a first proton implant isolation region within said VCSEL structure defining active and inactive regions of the VCSEL structure; and

a second proton implant isolation region formed around said photodiode.

30

47. The monolithic optical transmitter and receiver pair of claim 46 wherein the VCSEL structure further comprises:

35

a first mirror formed on a semiconductor wafer;
a first cladding layer formed on said first mirror;
an active region formed on said first cladding layer;
a second cladding layer formed on said active region; and
a second mirror formed on said second cladding layer.

1 48. The monolithic optical transmitter and receiver pair of
claim 46 wherein the photodiode further comprises:
distributed p-type layers formed on said VCSEL layers;
an intrinsic layer formed on said distributed p-type
5 layers; and
an n-type layer formed on said intrinsic layers.

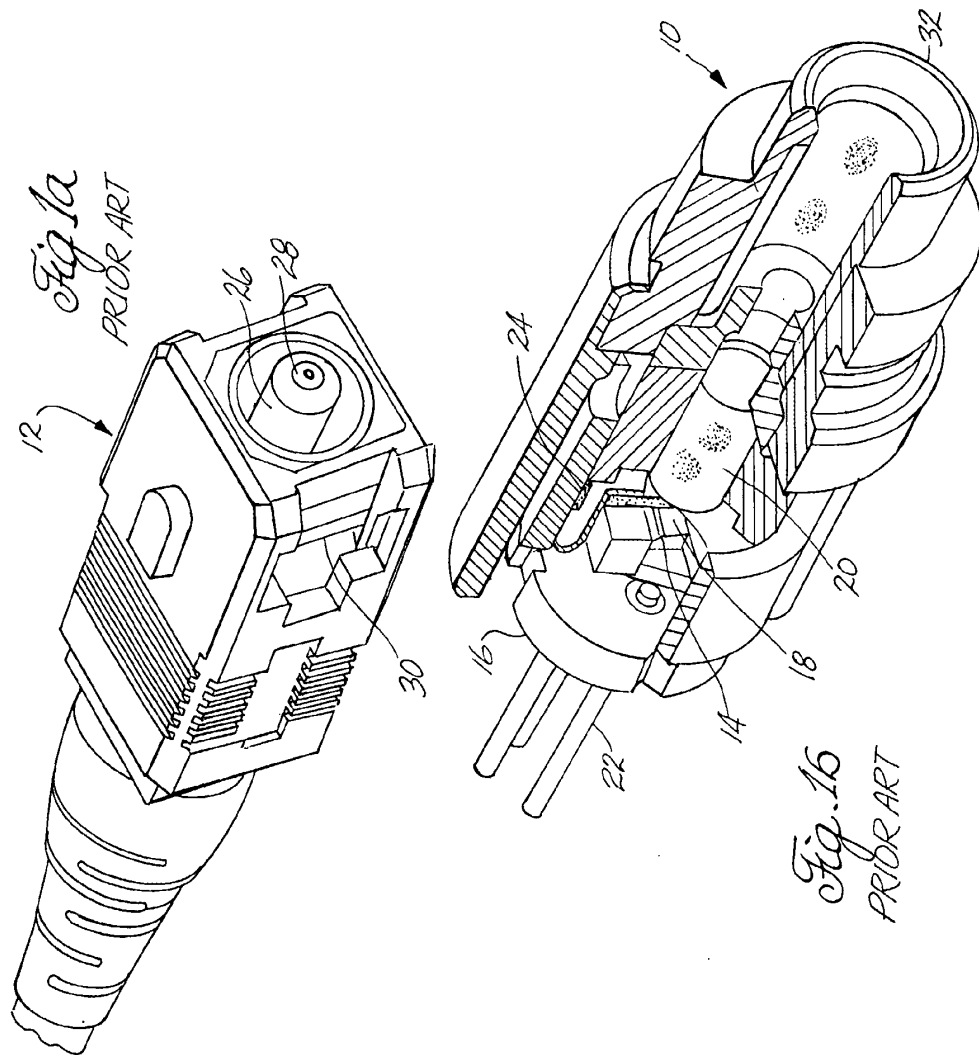
49. A monolithic optical transmitter and receiver pair
comprising:
10 a substrate;
a multi-layer VCSEL structure formed on a first side of
said substrate;
an etch stop layer formed on the uppermost layer of said
VCSEL;
15 a photodiode formed on said etch stop layer at discrete
locations;
a photodiode n-type contact (cathode) formed on said
photodiode;
a photodiode p-type contact (anode) formed on said VCSEL;
20 a VCSEL p-type contact (anode) formed on said VCSEL;
a VCSEL n-type contact (cathode) coupled to a second side
of said semiconductor substrate;
a first proton implant isolation region within said VCSEL
structure defining active and inactive regions of the VCSEL
25 structure;
a second proton implant isolation region around said
photodiode;
interconnect metal pads formed on said photodiode anode
and cathode and VCSEL anode;
30 a dielectric phase shifting layer formed on said VCSEL ;
and
an anti-reflective coating formed on said photodiode.

50. A monolithic optical transmitter and receiver pair
35 comprising:
a substrate;
a multi-layer VCSEL structure formed on said substrate;

- 1 one or more photodiodes formed on said VCSEL structure at
discrete locations; and
 one or more transistors coupled to the photodiodes.
- 5 51. The monolithic optical transmitter and receiver pair of
claim 50 wherein the VCSEL structure further comprises:
 a first mirror formed on a semiconductor wafer;
 a first cladding layer formed on said first mirror;
 an active region formed on said first cladding layer;
10 a second cladding layer formed on said active region; and
 a second mirror formed on said second cladding layer.
52. The monolithic optical transmitter and receiver pair of
claim 50 wherein the photodiode further comprises:
15 distributed p-type layers formed on said VCSEL layers;
 an intrinsic layer formed on said distributed p-type
layers; and
 an n-type layer formed on said intrinsic layers.
- 20 53. The monolithic optical transmitter and receiver pair of
claim 52 wherein the transistor is a FET.
54. The monolithic optical transmitter and receiver pair of
claim 53 wherein the FET further comprises:
25 insulation regions formed around said photodiodes wherein
said insulation regions form a conductive well for the FET and
isolate said photodiodes from said VCSEL;
 a first electrical contact forming a source and a second
electrical contact forming a drain, wherein said first and
30 second electrical contacts overlap said insulation regions and
said conductive well on an uppermost surface of said
photodiode; and
 a third electrical contact forming a gate on said
uppermost photodiode layer within the conductive well created
35 by the isolation regions on the uppermost photodiode layer.
55. An integrated photodetector and preamplifier comprising:
 a substrate;

- 1 photodiodes formed on said substrate; and
 one or more transistors coupled to the photodiodes.
56. The integrated photodetector and preamplifier of claim 55
5 wherein the photodiode further comprises:
 distributed p-type layers formed on said substrate;
 an intrinsic layer formed on said distributed p-type
 layers; and
 an n-type layer formed on said intrinsic layers.
- 10 57. The integrated photodetector and preamplifier of claim 56
 wherein the transistor is a FET.
58. The integrated photodetector and preamplifier of claim 57
15 wherein the FET further comprises:
 insulation regions formed around said photodiodes wherein
 said insulation regions form a conductive well for the FET;
 a first electrical contact forming a source and a second
 electrical contact forming a drain, wherein said first and
20 second electrical contacts overlap said insulation regions and
 said conductive well on said photodiode; and
 a third electrical contact forming a gate on said
 photodiode within the conductive well formed by the isolation
 regions on the uppermost photodiode layer.
- 25 59. The monolithic optical transmitter and receiver pair of
 claim 54 wherein the insulation regions formed around said
 photodiodes are proton implantation regions.
- 30 60. The integrated photodetector and preamplifier of claim 58
 wherein the insulation regions formed around said photodiodes
 are proton implantation regions.

35



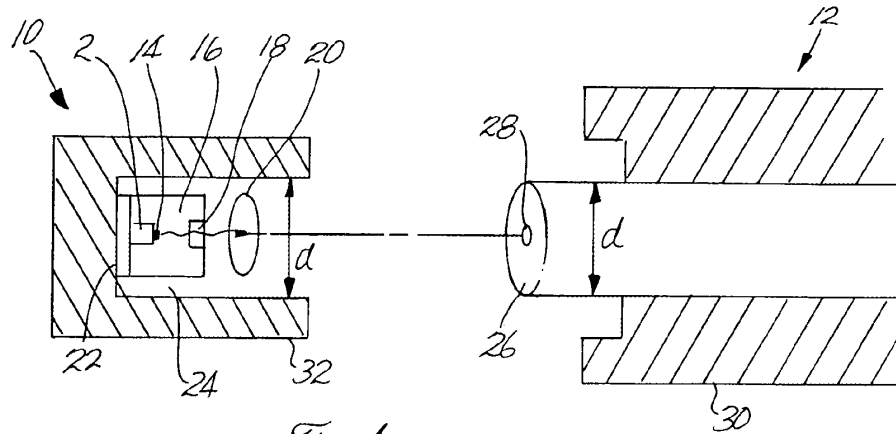


Fig. 1c
PRIOR ART

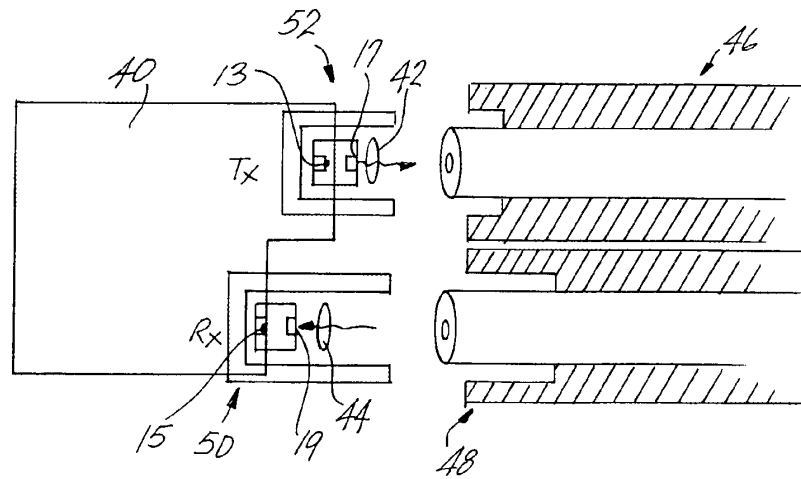


Fig. 1d
PRIOR ART

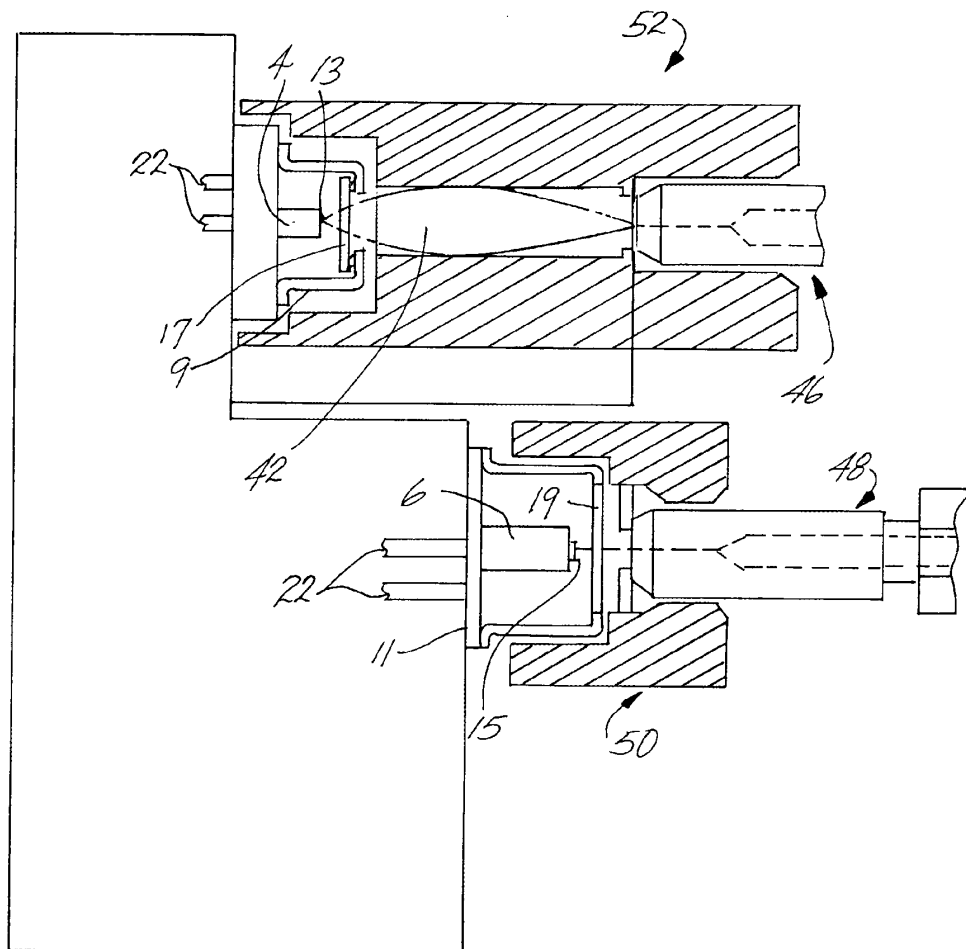
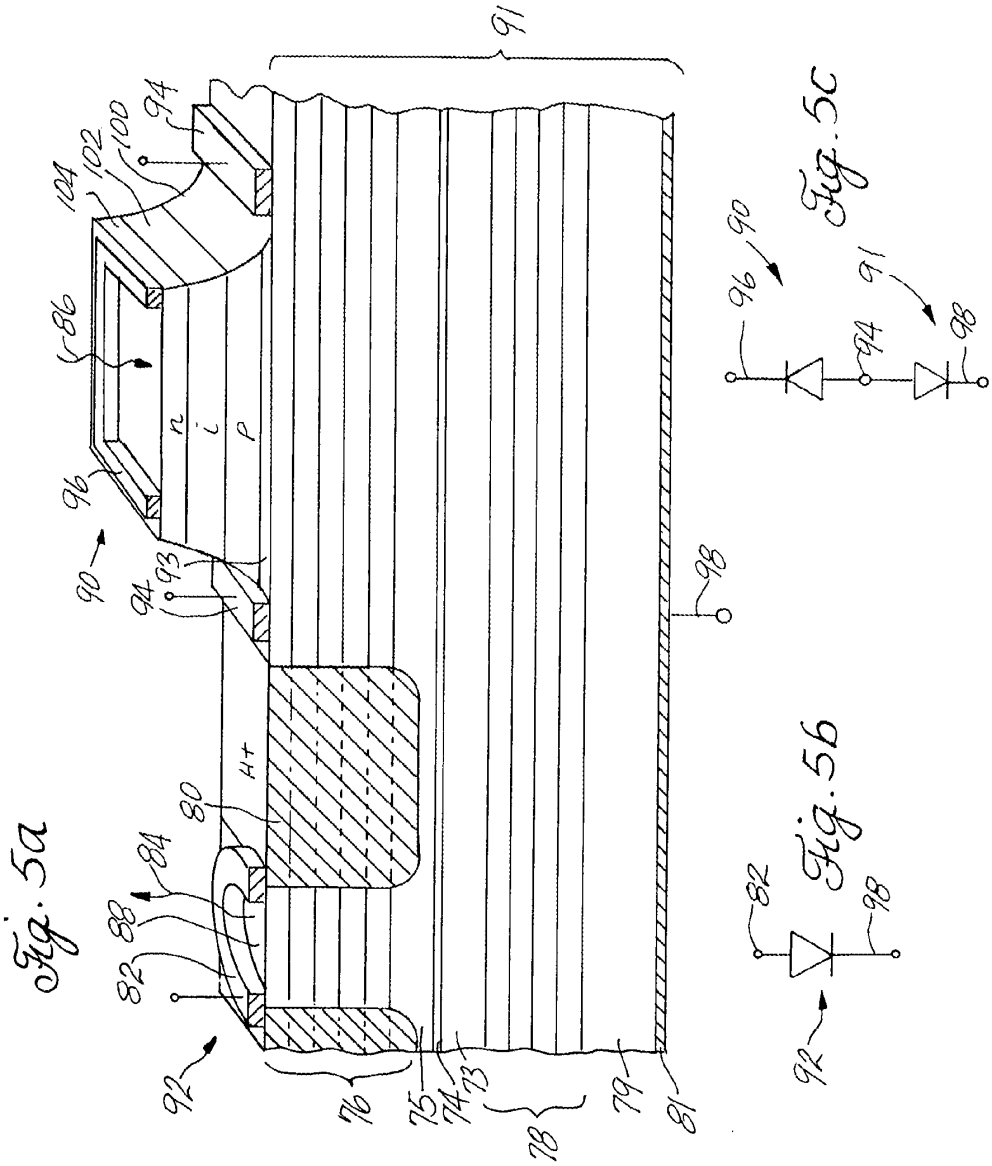


Fig. 2
PRIOR ART



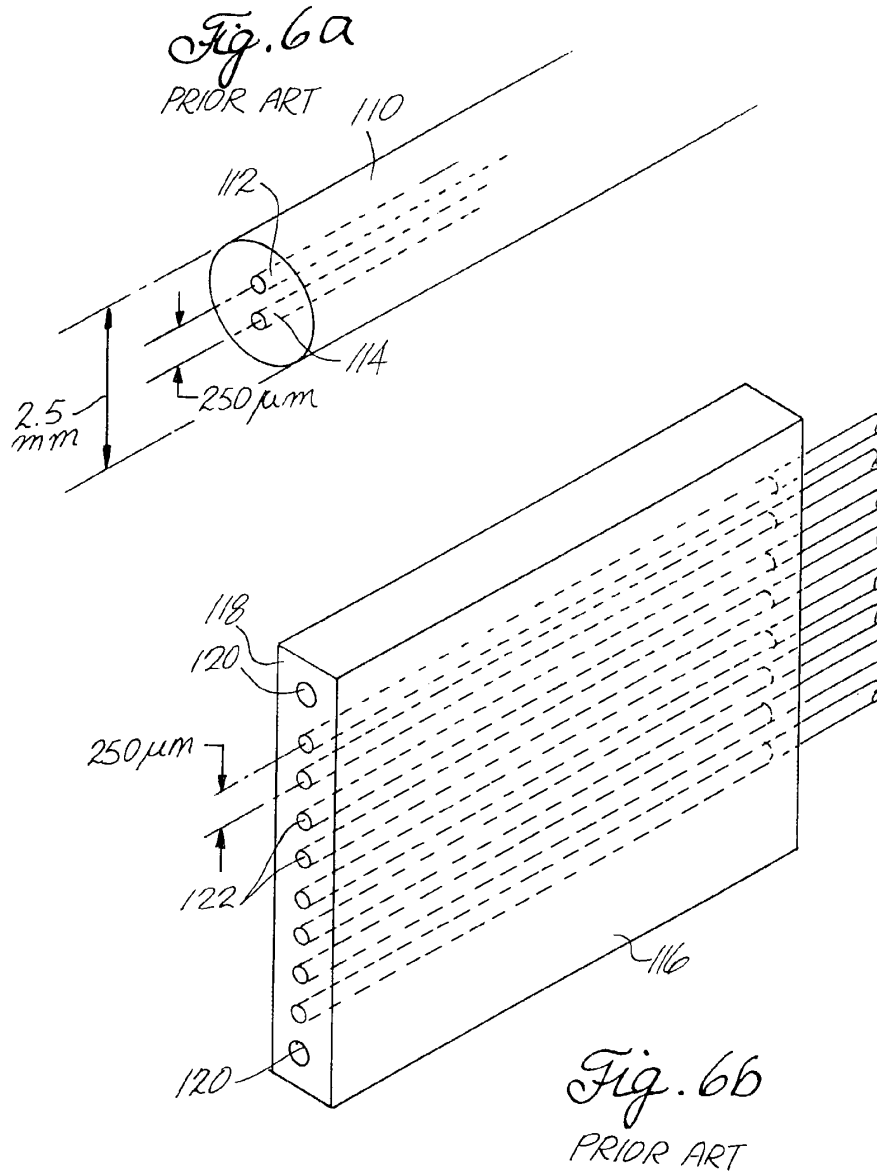


Fig. 7a

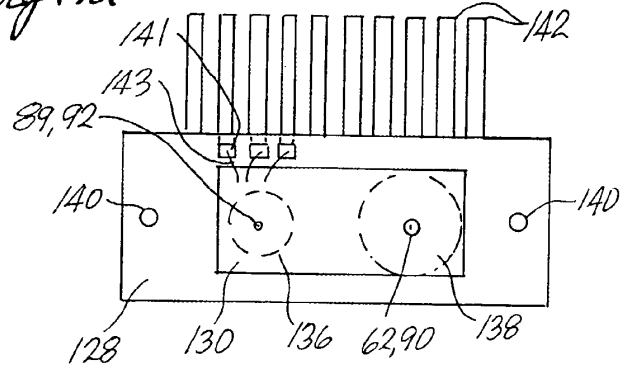


Fig. 7b

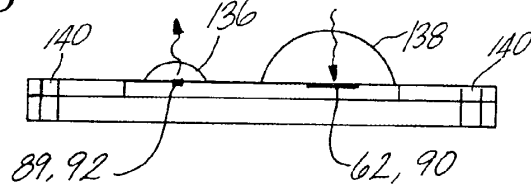
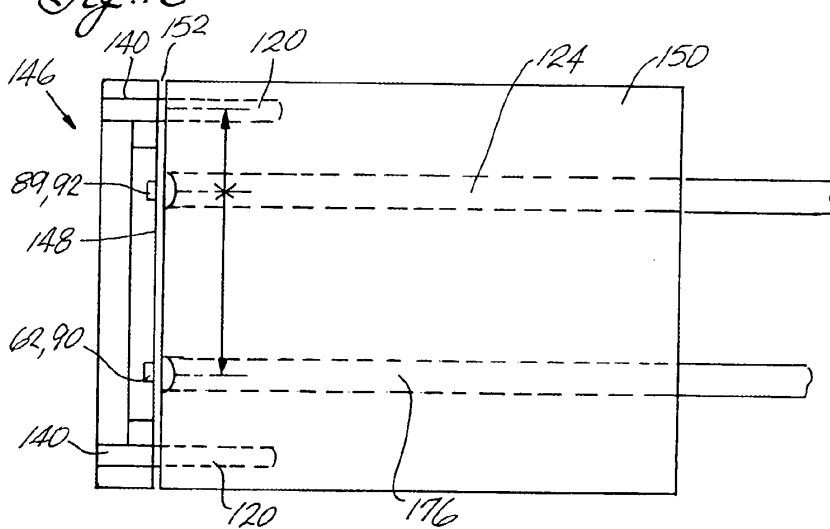
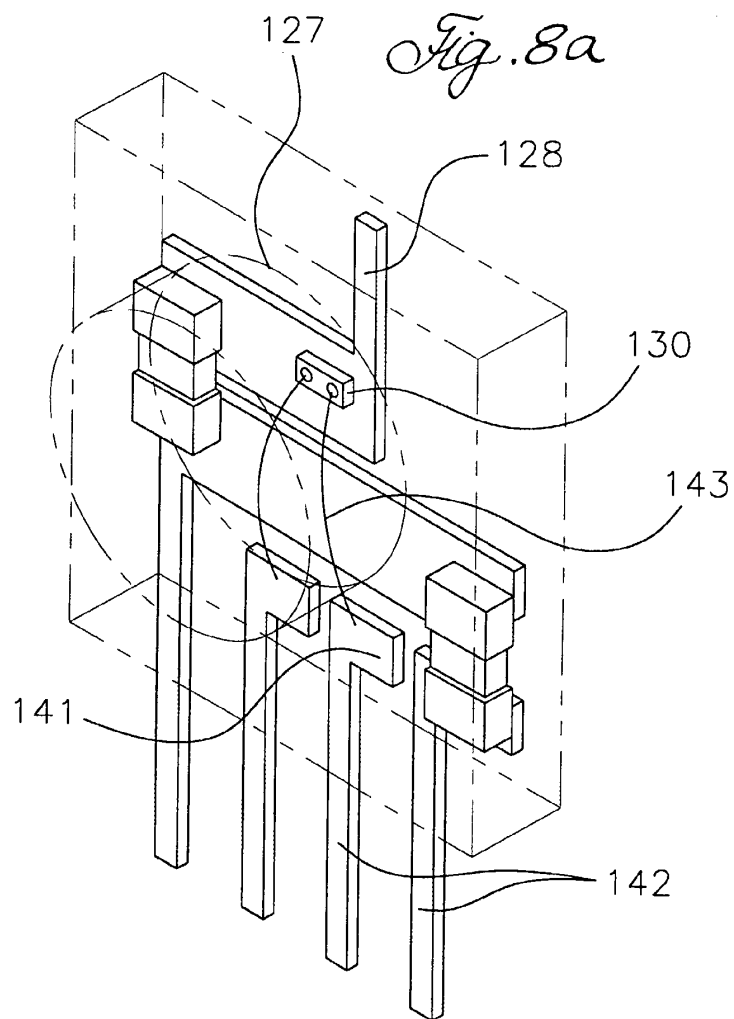
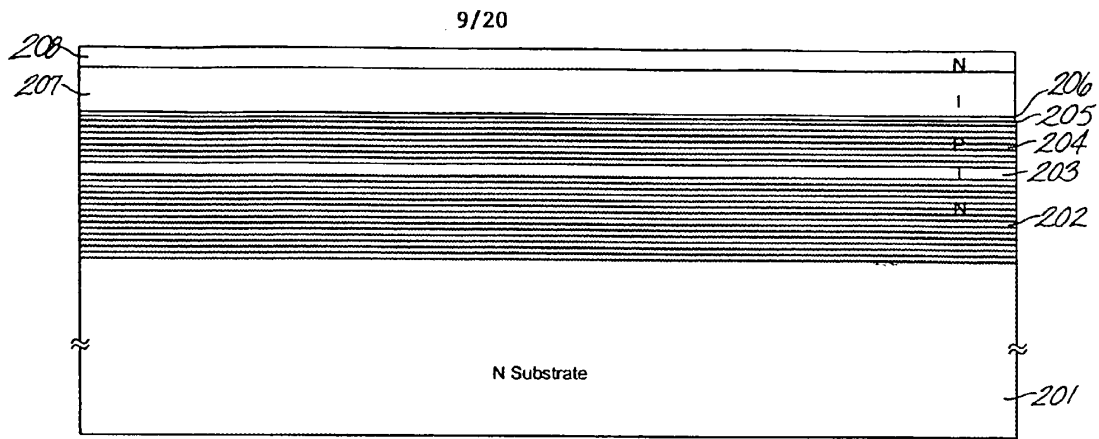
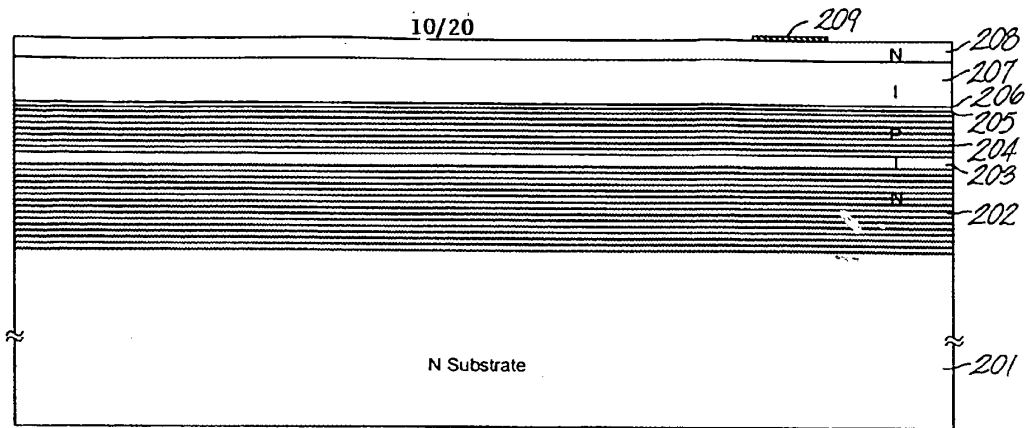
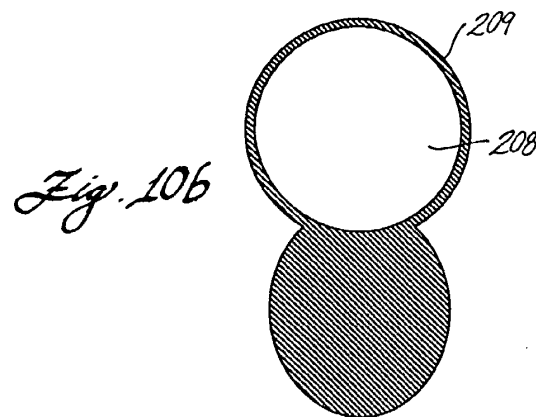


Fig. 7c









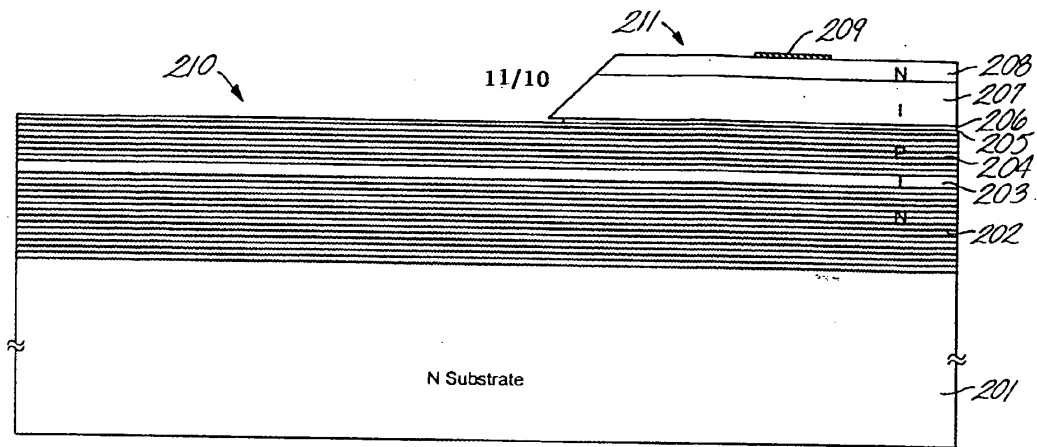


Fig. 11a

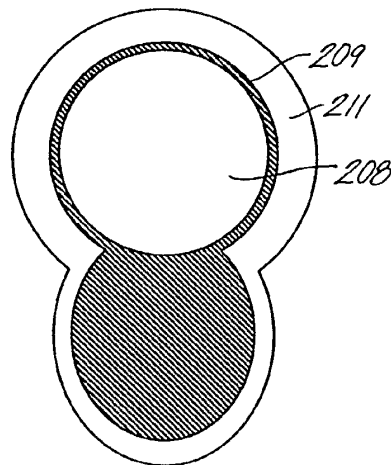


Fig. 11b

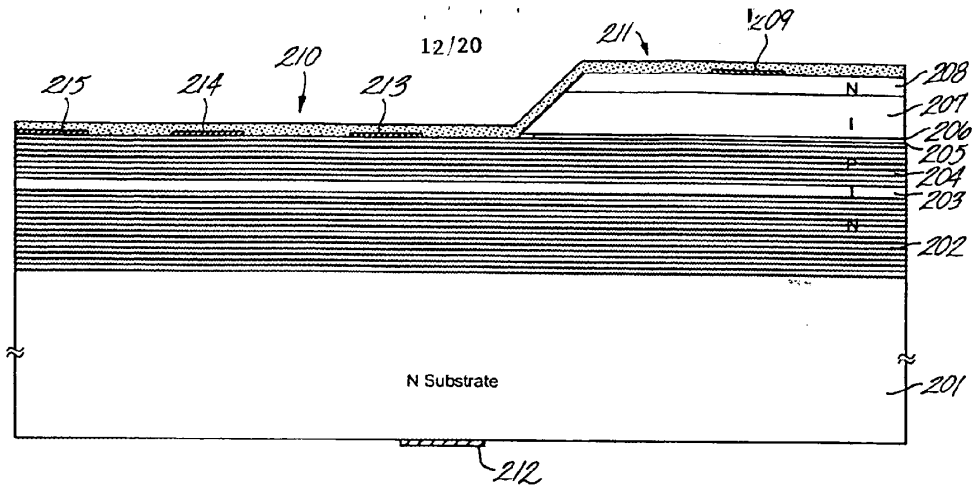


Fig. 12a

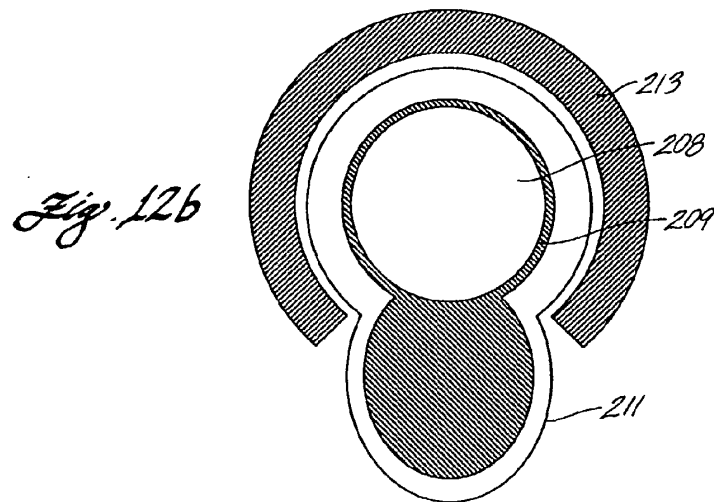


Fig. 12b

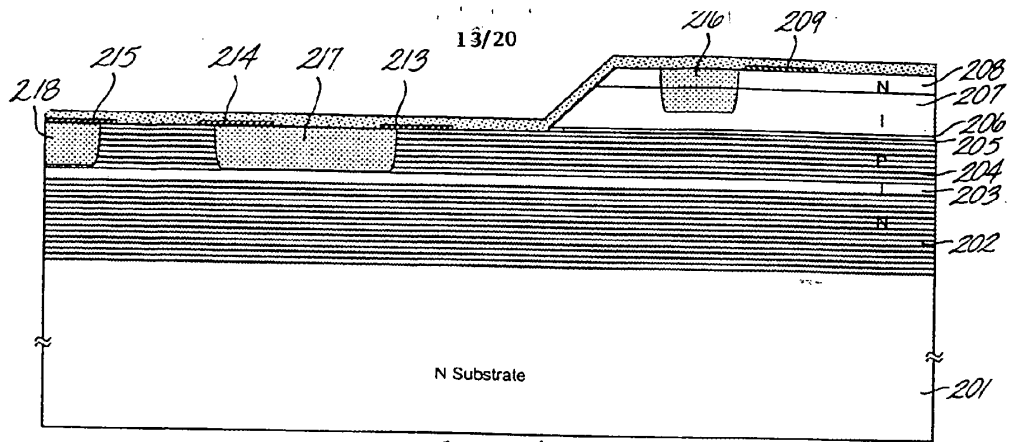
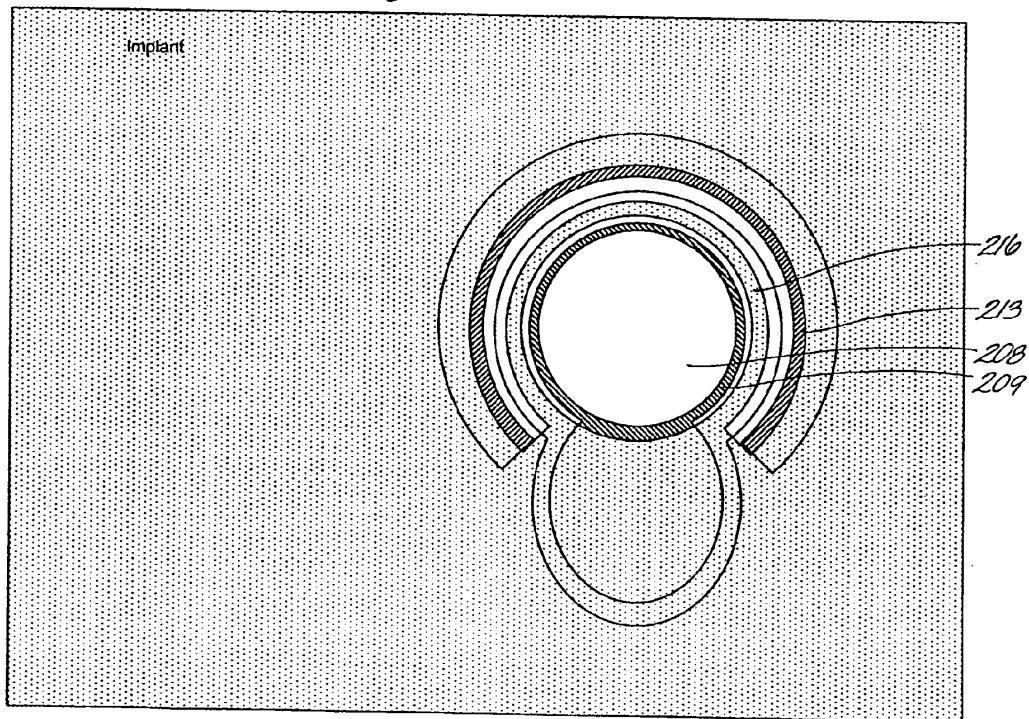


Fig. 13b



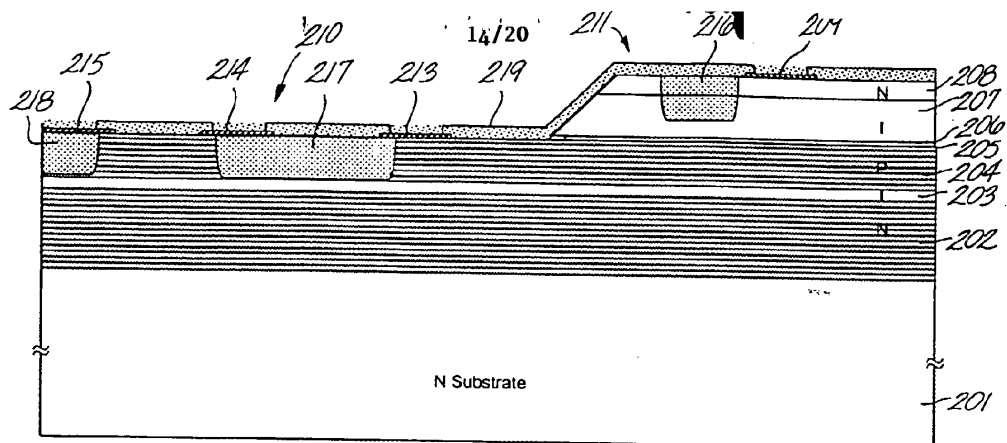
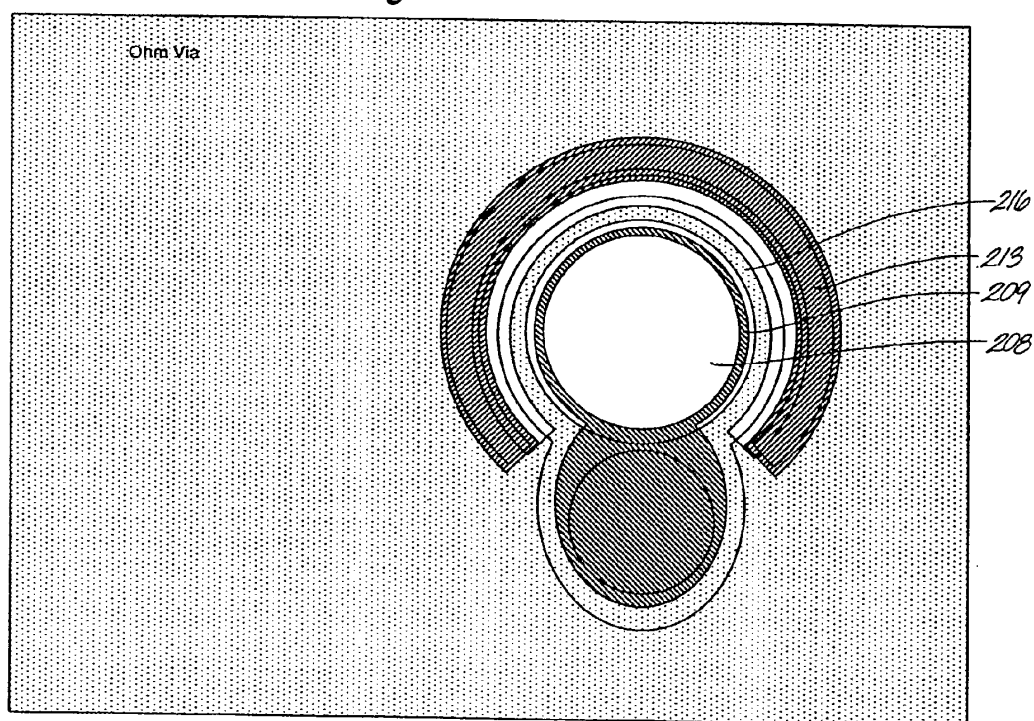


Fig. 14a

Fig. 146



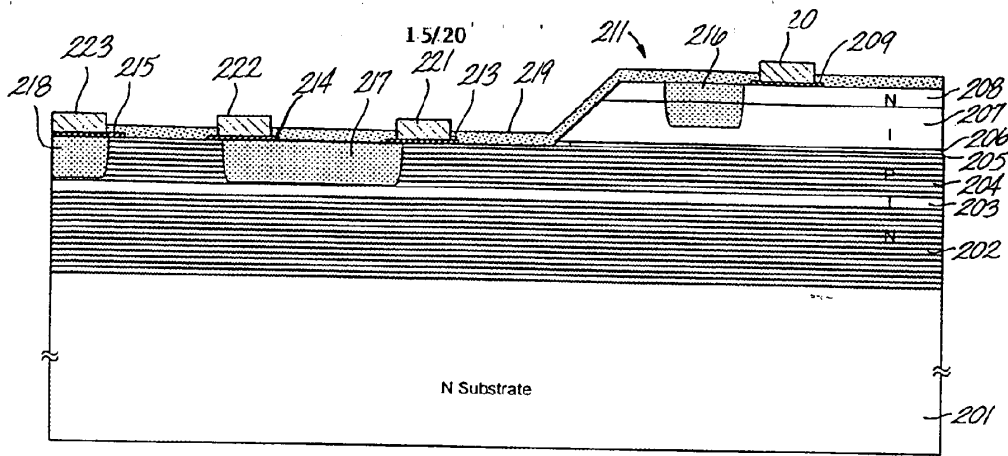
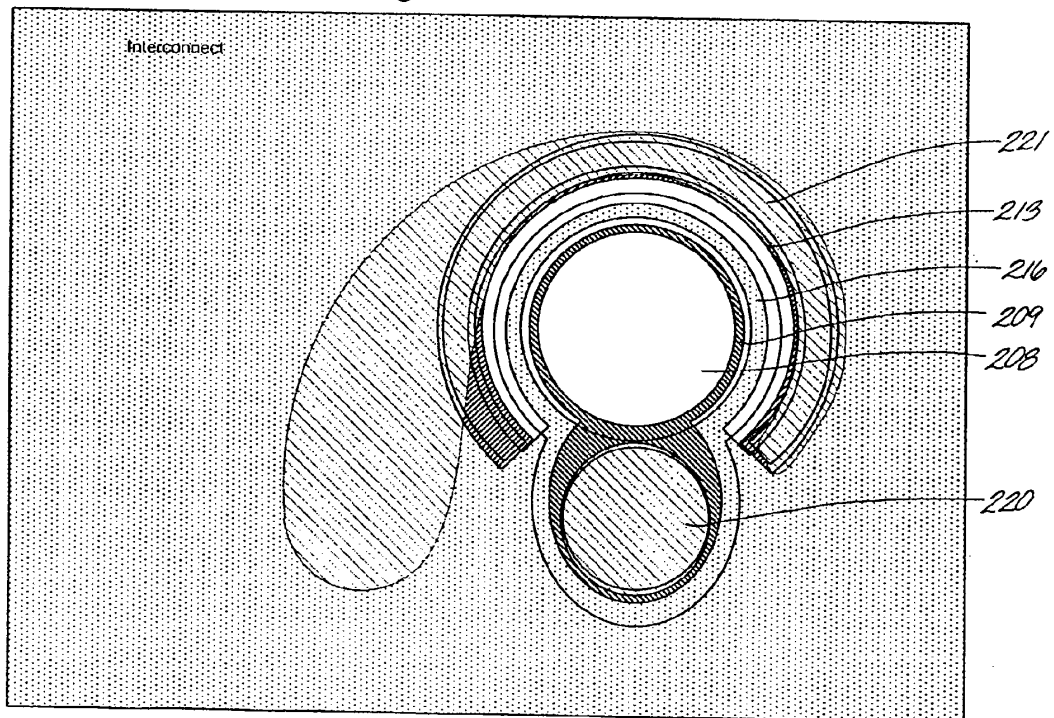
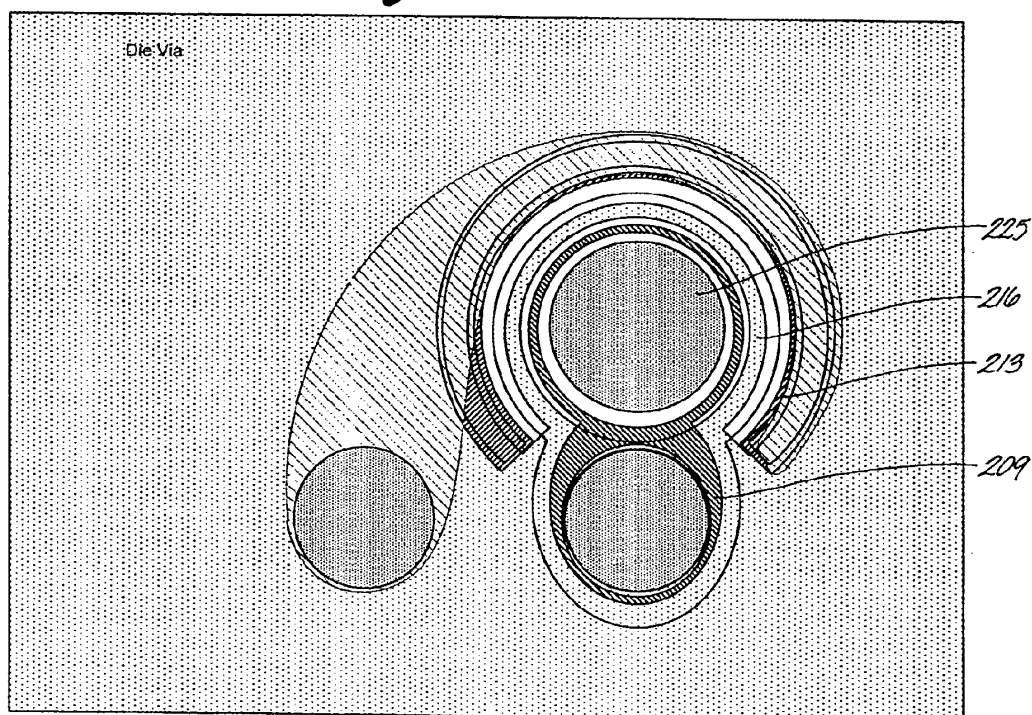
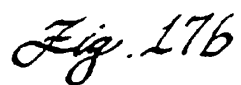
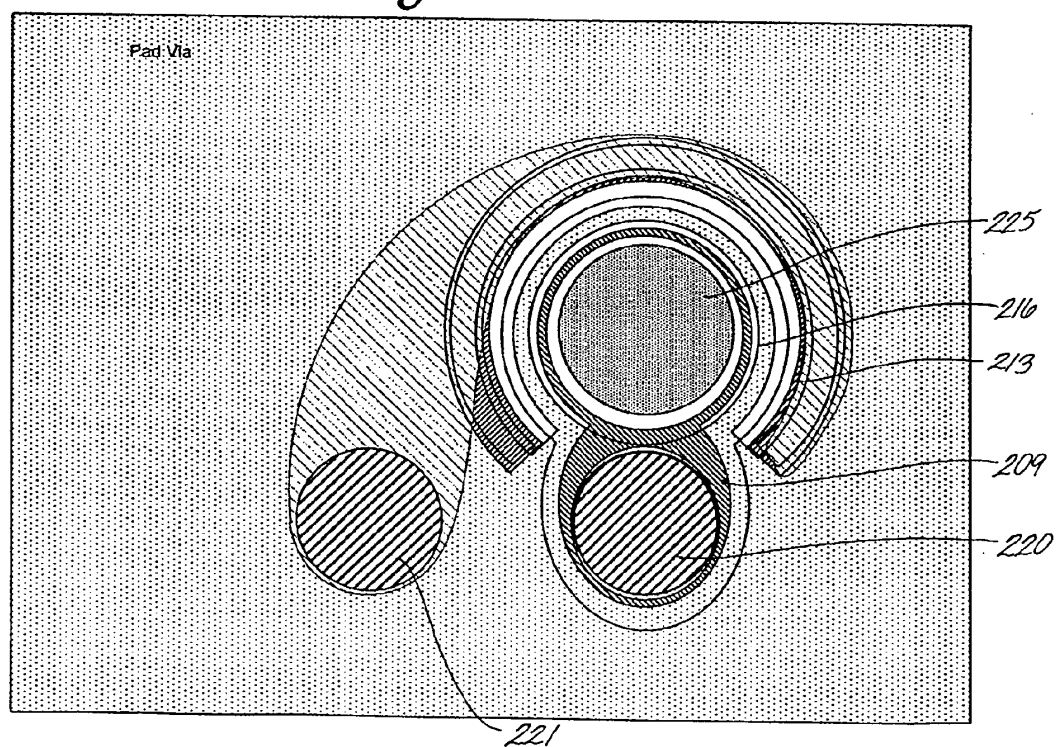


Fig. 15a

Fig. 15b







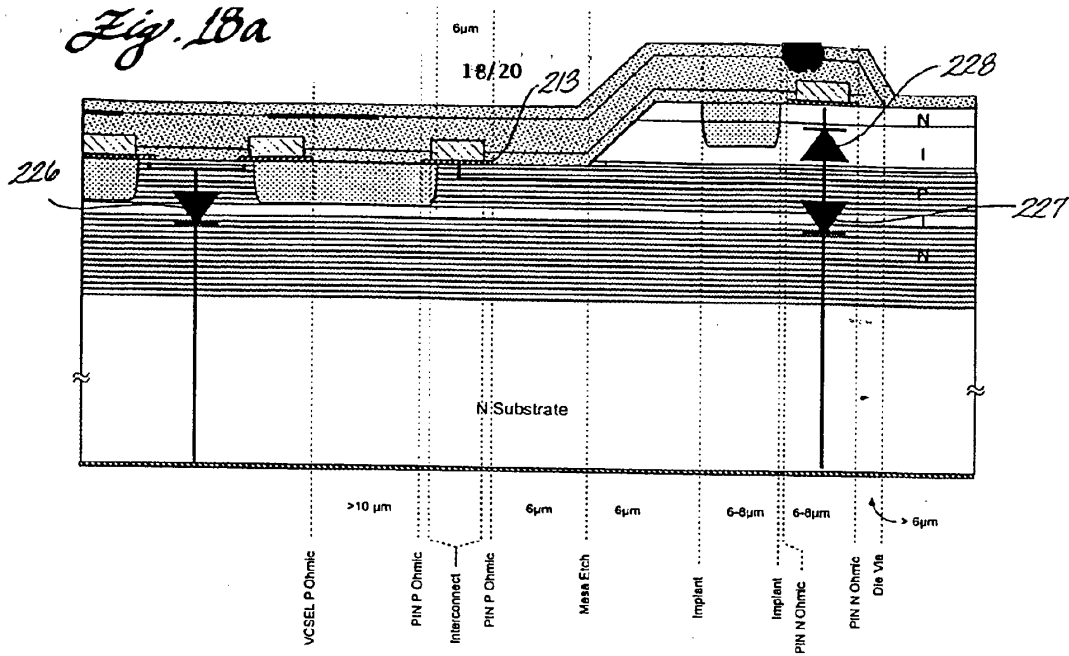
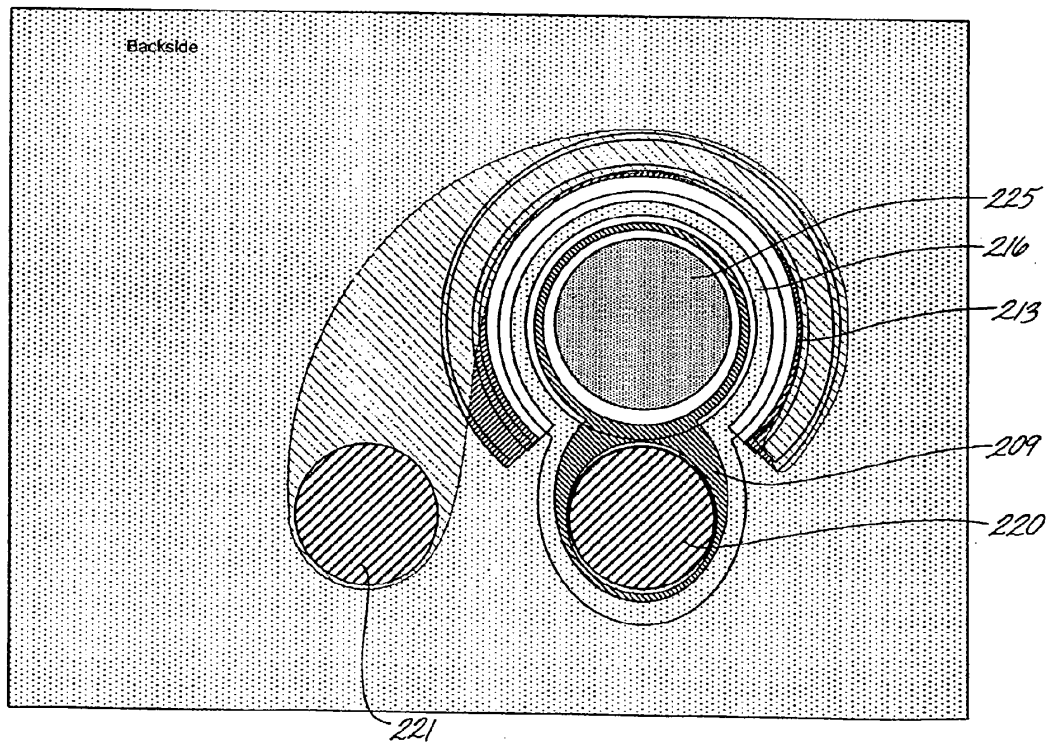


Fig. 18b



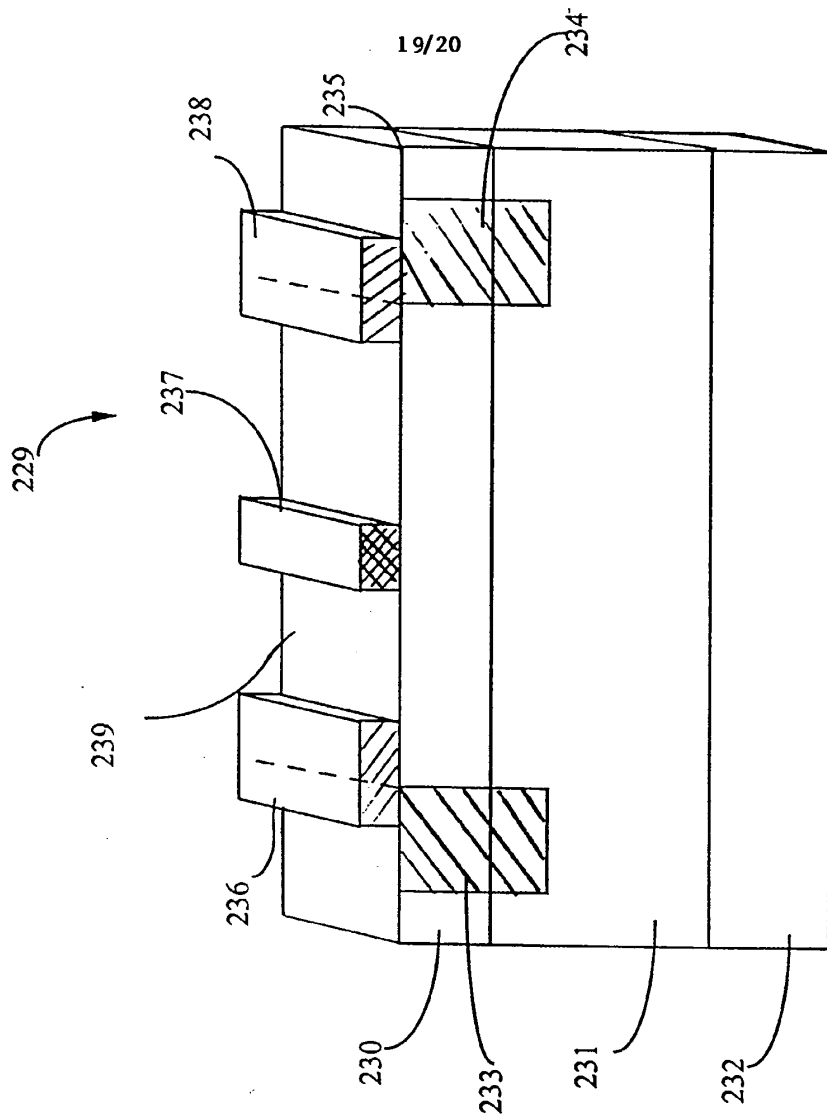


FIG. 19

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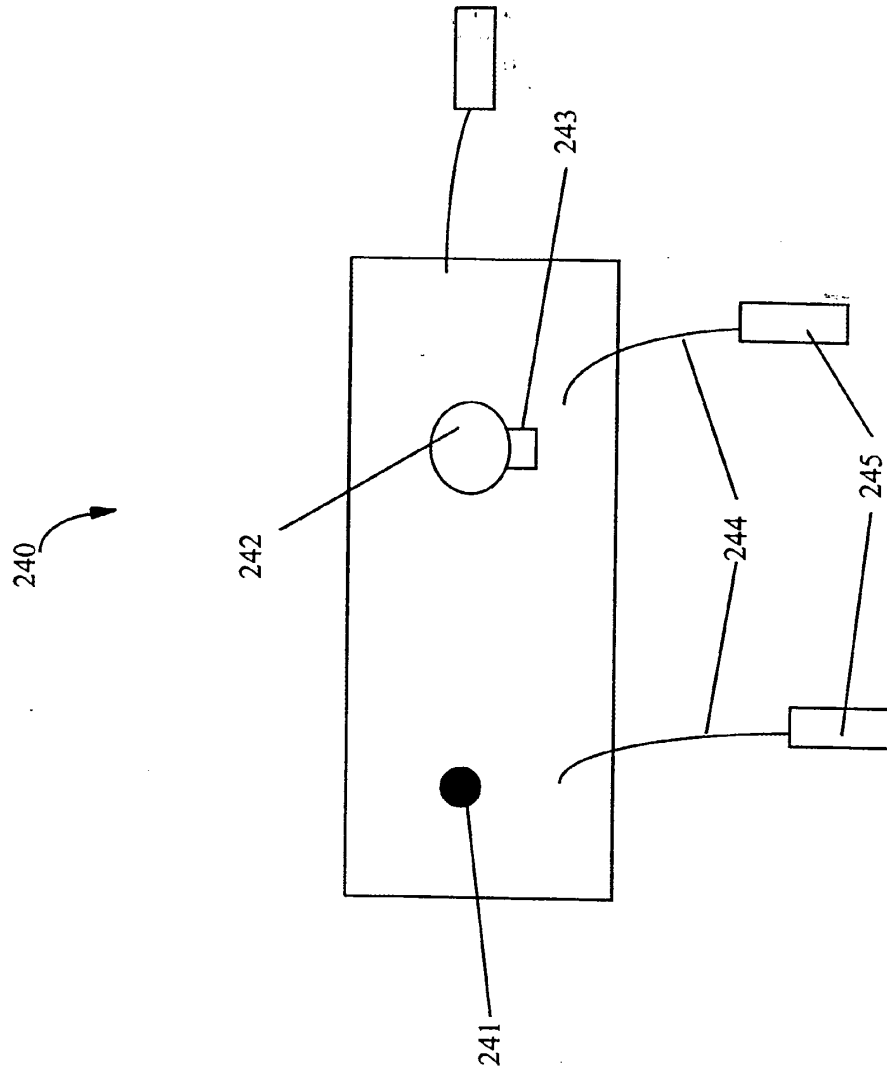


FIG. 20

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62/540,524	02 August 2017 (02.08.2017)	US	62/651,053	30 March 2018 (30.03.2018)	US
62/542,243	07 August 2017 (07.08.2017)	US	62/651,087	31 March 2018 (31.03.2018)	US
62/547,728	18 August 2017 (18.08.2017)	US	62/652,830	04 April 2018 (04.04.2018)	US
62/553,844	02 September 2017 (02.09.2017)	US	62/659,072	17 April 2018 (17.04.2018)	US
62/556,426	10 September 2017 (10.09.2017)	US	62/659,067	17 April 2018 (17.04.2018)	US
62/561,869	22 September 2017 (22.09.2017)	US			
62/591,072	27 November 2017 (27.11.2017)	US			

(54) Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

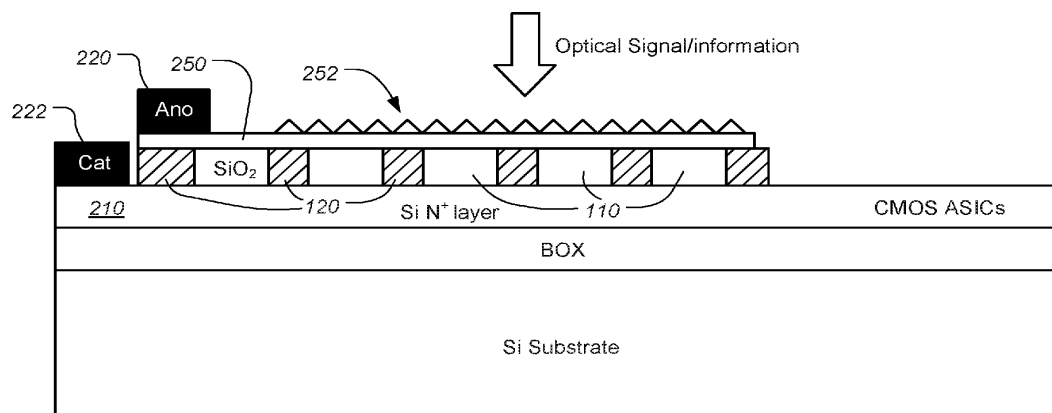


FIG. 2

(57) **Abstract:** Lateral and vertical micro structure enhanced photodetectors and avalanche photodetectors are monolithically integrated with CMOS/BiCMOS ASICs and can also be integrated with laser devices using fluidic assembly techniques. Photodetectors can be configured in a vertical PIN arrangement or lateral metal- semiconductor-metal arrangement where electrodes are in an inter-digitated pattern. Microstructures, such as holes and protrusions, can improve quantum efficiency in silicon, germanium and III-V materials and can also reduce avalanche voltages for avalanche photodiodes. Applications include optical communications within and between datacenters, telecommunications, LIDAR, and free space data communication.

[Continued on next page]

62/662,217	24 April 2018 (24.04.2018)	US
62/666,005	02 May 2018 (02.05.2018)	US
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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y -- A	US 2016/0307939 A1 (WANG, S et al.) 20 October 2016; entire document	1-6, 9-14, 17-19, 21-23, 25-30, 33, 35-47, 49 -- 7-8, 15-16, 24, 31-32, 48 -- 20, 34, 50
Y -- A	US 2016/0254407 A1 (WANG, S et al.) 01 September 2016; entire document	7-8, 15-16, 24, 31-32 -- 20, 34, 50
Y	US 2004/0222357 A1 (KING, D et al.) 11 November 2004; abstract; figure 1; paragraph [0016]	48
A	US 5,525,828 A (BASSOUS, E et al.) 11 June 1996; entire document	1-50
A	US 2002/0097962 A1 (YOSHIMURA, T et al.) 25 July 2002; entire document	1-50
A	US 2015/0340538 A1 (CORIANT ADVANCED TECHNOLOGY, LLC) 26 November 2015; entire document	1-50
A	US 7,605,406 B2 (IGUCHI, Y) 20 October 2009; entire document	1-50

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Date of the actual completion of the international search

14 January 2019 (14.01.2019)

Date of mailing of the international search report

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EP 0 940 854 B1

Description

[0001] This invention relates to semiconductors and more particularly to integrated optoelectronic receiver devices and circuits incorporating photodetectors and MODFETs formed with SiGe layers.

[0002] The advent of fiber-optic communications technology has increased the demand for high-speed optoelectronic devices and circuits that operate with data rates of greater than 1 Gbit/sec. In particular, a growing market exists for local area networks and short-haul optical connections that operate at wavelengths of $\lambda = 850$ nm. It would be desirable to fabricate these circuits monolithically due to the lower cost of production and performance advantages over discrete components. It would also be desirable to fabricate such circuits entirely in a silicon-based technology due to the reduced cost arising from their compatibility with existing Si-based technologies including CMOS logic circuits.

[0003] In the prior art, GaAs has been the previous choice for monolithically integrated optical receivers operating at $\lambda = 850$ nm. This is due to the favorable intrinsic material properties of GaAs; the absorption length for 850 nm-radiation in GaAs is $\alpha^{-1} = 1 \mu\text{m}$, and the electron mobility in GaAs is roughly $8500 \text{ cm}^2/\text{Vs}$ at room temperature. J. S. Wang et al., IEEE Phot. Tech. Lett. 5, 316 (1993) demonstrated the fabrication of high-speed integrated photoreceiver circuits composed of GaAs metal-semiconductor-metal (MSM) photodiodes and MESFETs with -3 dB bandwidths as high as 11 GHz at $\lambda = 850$ nm. Further improvement of GaAs-based receiver performance has been obtained using GaAs MSM photodetectors integrated with AlGaAs/GaAs modulation-doped field effect transistors (MODFETs). V. Hurm et al., Electron. Lett. 29, 9 (1993) demonstrated photoreceiver circuits of this type with -3 dB bandwidths as high as 14 GHz at $\lambda = 850$ nm.

[0004] In order to replace GaAs, an integrated Si-based technology must have comparable performance to GaAs and a relatively low-cost process. However, the intrinsic material properties of Si are much less favorable compared to GaAs. The absorption length in Si for 850 nm-radiation is $\alpha^{-1} = 20 \mu\text{m}$, which is over an order of magnitude longer than in GaAs. Therefore, for a Si photodetector to have high responsivity it must have a thick absorbing region making the detector very slow, and for high speed the absorbing region should be very thin resulting in an extremely poor responsivity. For instance, Y. S. He et al., Electron. Lett. 29, 9 (1993) demonstrated the operation of a lateral p-i-n photodiode integrated with a Si NMOS technology with a responsivity of 0.48 A/W at $\lambda = 870$ nm, but with a -3 dB bandwidth of only 900 MHz. Moreover, these results were only made possible by using ultra-high purity Si, and an extremely large bias voltage of 30 V. On the other hand, M. Y. Liu et al., Appl. Phys. Lett. 65, 887 (1994) demonstrated operation of a Si on insulator (SOI) MSM photodiode with an absorbing region thickness of only $0.1 \mu\text{m}$ that had a bandwidth

over 100 GHz, but a severely-degraded responsivity at $\lambda = 780$ nm of 0.0057 A/W. Improvements in the bandwidth/responsivity tradeoff of Si photodiodes are possible, for instance, in U.S. Pat. No. 5,589,704 which was issued on Dec. 31, 1996 to B. F. Levine, the responsivity of an MSM detector was shown to increase by a factor of close to 4 by roughening the surface of a Si epi-layer grown on an SOI wafer. However such a technique is limited to use with SOI substrates, and may not be suitable for practical applications due to the complexities of the roughening process. Si photodetectors are further hindered by the fact that the electron mobility in Si/SiO₂ inversion layers is several times lower than GaAs at room temperature, and the frequency performance and gain of Si NMOS devices is considerably poorer compared to GaAs MESFETs.

[0005] In U.S. Pat. No. 5,525,828 which was issued on Jun. 11, 1996 to E. Bassous et al., it was noted that the speed and/or responsivity of Si MSM photodetectors could be increased by adding a certain percentage of Ge to the absorbing layer. Increasing the percent Ge-composition of Si_{1-x}Ge_x alloy decreases the absorption length, and increases the electron and hole mobilities thereby leading to potentially faster devices.

[0006] It has also been shown that field-effect transistors fabricated on Si/Si_{1-x}Ge_x layer structures offer considerable advantages over bulk Si transistors. For n-channel MODFETs incorporating tensile-strained Si/Si_{1-x}Ge_x quantum wells, frequency performance is considerably better than Si MOSFETs for a given gate length device. Similar performance advantages can be obtained in p-channel MODFETs fabricated on compressive-strained Si_{1-y}Ge_y/Si_{1-x}Ge_x quantum wells. For instance, M. Arafa et al., IEEE Electron. Dev. Lett. 17, 586 (1996) obtained unity current-gain cutoff frequencies of 70 GHz for $0.1 \mu\text{m}$ gate length p-channel transistors fabricated on compressive-strained Si_{0.7}Ge_{0.3}/Si_{0.3}Ge_{0.7} heterostructures. In U.S. Pat. No. 5,659,187 which was issued on Aug. 19, 1997 to F. K. Legoues and B. S. Meyerson, it was shown that a low-defect density layer of relaxed Si_{1-x}Ge_x, with arbitrary Ge composition can be grown on a lattice-mismatched substrate using an intermediate graded-composition buffer layer where strain has been relieved in the buffer layer or below via activation of modified Frank Read sources which is a mechanism to generate new dislocations. This work demonstrated the practicality of producing devices and circuits using Si/SiGe heterostructures grown on a SiGe graded composition buffer layer on Si substrates. Finally, U.S. Pat. No. 5,534,713 which was issued on Jul. 9, 1996 to K. Ismail and F. Stern showed that complementary logic circuits could be fabricated using high-mobility electron and hole channels fabricated in strained Si/SiGe layers grown on relaxed SiGe buffer layers.

[0007] Despite the apparent advantages of SiGe technology over bulk Si for photodetectors, MODFETs, and CMOS logic circuits, the concept of combining these devices to form integrated photoreceiver circuits has not

been suggested, nor has a clear method for monolithically integrating these structures in such a way as to allow high-frequency operation and low cost Si manufacturing been suggested.

[0008] It is an object of the present invention to provide a simple means of monolithically integrating a photodetector with high speed and responsivity with a microwave transistor on a Si substrate in such a way as to allow high frequency performance better than Si and comparable to that achievable in GaAs.

[0009] It is a further object of this invention to provide a method for fabricating an optoelectronic integrated circuit using a process that is fully compatible with standard Si processing.

[0010] It is still a further object of this invention to provide a means for monolithically integrating a high-speed photoreceiver circuit with a practical CMOS logic manufacturing technology.

[0011] According to the present invention provides a semiconductor structure according to claim 1.

[0012] The semiconductor structure includes spaced apart drain and source regions extending to the quantum well layer and a Schottky gate contact to control charge in the conducting channel to form a MODFET. Portions of the quantum well layer, said undoped $\text{Si}_{1-y}\text{Ge}_y$ spacer layer and said doped $\text{Si}_{1-y}\text{Ge}_y$ supply layer are removed to expose said relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer wherein electrodes are formed on said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer to form a photodetector. The quantum well layer is under tensile strain and consists of Si. The electrodes include two or more interdigitated Schottky electrodes. y is in the range from 0.2 - 0.35.

[0013] Preferably, further included is a trench extending through said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer surface and surrounding said photodetector. The trench is filled with material including dielectric material. Further included is a layer of Si over said doped $\text{Si}_{1-y}\text{Ge}_y$ supply layer. Preferably, the doped $\text{Si}_{1-y}\text{Ge}_y$ supply layer is n-type. The positively-biased electrodes of said photodetector provide Schottky contacts with barrier height for holes that is greater than half the band gap of said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer, and negatively-biased electrodes of said photodetector provide Schottky contacts with barrier height for electrons that is greater than half the band gap of said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer. The negatively-biased electrodes of said photodetector provide Schottky contacts with barrier height for electrons that is greater than half the band gap of said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer, and positively-biased electrodes of said photodetector form Ohmic contact to an n-type doped region. Negatively-biased electrodes of said photodetector form Ohmic contacts to a p-type doped region and said positively-biased electrodes of said photodetector form an Ohmic contact to an n-type doped region.

[0014] Preferably, said substrate is heavily-doped greater than 10^{18} atoms/cm³ and said substrate is an SOI substrate comprising a thick Si layer, a SiO_2 layer, and a Si overlayer. The substrate is lightly-doped Si, and

the region of said substrate underneath said photodetector is heavily-doped greater than 10^{18} atoms/cm³.

[0015] Preferably, said photodetector absorbing region is bordered by deep trenches extending from said photodetector surface down to said Si substrate, and filled with a dielectric material, so as to prevent photo-generated carriers generated in said $\text{Si}_{1-y}\text{Ge}_y$ buffer layer from diffusing laterally past said deep trenches.

[0016] Preferably, further included are spaced apart drain and source regions extending to said quantum well layer, a gate dielectric layer above said supply layer between said drain and source and a gate electrode above said dielectric layer to form a MOSFET. Further included are first and second spaced apart doped regions, one above the other, with a portion of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer there between to form a photodetector and an Ohmic contact to said respective first and second doped regions for applying a potential there between and further included is a trench extending into said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer to provide a barrier to electrical charge. The first doped region includes a region of said quantum well layer, said undoped $\text{Si}_{1-y}\text{Ge}_y$ spacer layer and said doped $\text{Si}_{1-y}\text{Ge}_y$ supply layer. The second doped region includes a region of said substrate.

[0017] The invention further provides a method of forming semiconductor structure as claimed in claim 15.

[0018] Preferably, further included is the step of doping said substrate underneath said photodetector greater than 10^{18} atoms/cm³, the steps of forming spaced apart drain and source regions extending to said quantum well layer, forming a gate dielectric layer above said supply layer between said drain and source and forming a gate electrode above said dielectric layer to form a MOSFET, the steps of forming first and second spaced apart doped regions, one above the other with a portion of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer there between to form a photodetector and forming an Ohmic contact to said respective first and second doped regions for applying a potential therebetween, the step of forming a trench extending through said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer to provide a barrier to electrical charge, and wherein the step of forming said second doped region includes the step of doping said substrate.

[0019] These and other features, objects, and advantages of the present invention will become apparent upon consideration of the following detailed description of the invention when read in conjunction with the drawing in which:

Figs. 1A - 1E are cross-sectional diagrams of the fabrication sequence of one embodiment of the invention where a metal-semiconductor-metal (MSM) photodetector and an n-channel modulation-doped field effect transistor (MODFET) are integrated using an epitaxially-grown Si/SiGe heterostructure.

Fig. 2 is a circuit diagram of a simple photoreceiver circuit.

Fig. 3 is a cross-sectional diagram of a second embodiment of the invention, where an n-channel Si/SiGe MODFET is integrated with a SiGe MSM photodetector with planar, deep trench isolation.

Fig. 4A is a cross-sectional diagram of a not claimed semiconductor structure where the absorbing layer is composed of a symmetrically-strained superlattice, and Fig. 4B is an energy-band diagram of the absorbing layer in Fig. 4A.

Fig. 5 is a cross-sectional diagram of a not claimed semiconductor structure where an MSM photodetector and a p-channel MODFET are integrated using an epitaxially-grown Si/SiGe heterostructure.

Fig. 6A is a cross-sectional diagram of a further embodiment of the invention where the positively (negatively) biased electrode of the MSM photodetector is composed of a material with high Schottky barrier for holes (electrons). Fig. 6B is a cross-sectional diagram of a further embodiment of the invention where the negatively biased photodetector electrode is composed of a material with high Schottky barrier for electrons, and the positively biased electrode is composed of an n-type Ohmic contact. Fig. 6C is a cross-sectional diagram of a further embodiment of the invention where the positively (negatively) biased photodetector electrode is composed of an n-type (p-type) Ohmic contact.

Fig. 7A is a cross-sectional diagram of an further embodiment of the invention where the substrate is an SOI wafer. Fig. 7B is a cross-sectional diagram of a further embodiment of the invention where the substrate is a heavily-doped n- or p-type Si wafer. Fig. 7C shows a cross-sectional diagram of a further embodiment of the invention where the substrate has a heavily-doped implanted region located directly underneath the MSM photodetector.

Fig. 8A shows a cross-sectional view along the line 8A-8A of Fig. 8B. Fig. 8B shows a top view of a SiGe MSM photodetector. Fig. 8C is a graph of the normalized photoresponse versus frequency of the SiGe MSM photodetector shown in Figs. 8A and 8B.

Fig. 9 is a graph of current gain and of maximum available gain plotted versus frequency for an n-channel Si/SiGe MODFET.

Fig. 10 is a cross-sectional diagram of a not claimed example of a semiconductor structure where a vertical p-i-n photodetector and an n-channel MODFET are integrated using an epitaxially-grown Si/SiGe heterostructure.

Fig. 11 is a cross-sectional diagram of a further em-

bodiment of the invention where an MSM photodetector and an n-channel modulation-doped MOSFET are integrated using a standard self-aligned polygate, salicide process.

Fig. 12 is a cross-sectional diagram of a not claimed example of a semiconductor structure where an MSM photodetector and a strained Si n-MOSFET are integrated using a planar fabrication process.

Fig. 13 is a cross-sectional diagram of a not claimed example of a semiconductor structure where an MSM photodetector is integrated with both an n-channel and a p-channel MODFET using an epitaxially-grown Si/SiGe heterostructure.

[0020] Figs. 1A-1E show the fabrication sequence for one embodiment of the invention where an n-channel, Si/SiGe modulation-doped field effect transistor (MODFET) 15 is integrated with a SiGe metal-semiconductor-metal (MSM) photodetector. A typical layer structure is shown in Fig. 1A. The layers are epitaxially grown on a Si substrate 1 using a high-precision epitaxy technique such as molecular beam epitaxy, rapid thermal chemical vapor deposition, or ultra high vacuum chemical vapor deposition (UHV-CVD). Substrate 1 may also be SiGe, Ge, GaAs, SiC, SOS and SOI. Suitable adjustments will be required to accommodate a different substrate lattice constant compared to Si. The following description is directed to a Si substrate. For a description of how to grow epitaxial Si and $\text{Si}_{1-x}\text{Ge}_x$ layers by UHV-CVD, reference is made to U.S. Pat. No. 5,298,452 which was issued on Mar. 29, 1994 to B. S. Meyerson. For $\text{Si}_{1-x}\text{Ge}_x$ layers, GeH_4 is added to Si-containing gas such as SiH_4 or Si_2H_6 in the UHV-CVD reactor. Ge is incorporated into the crystal lattice in place of Si during formation of the layer in the amount or proportion of x. Layer 2 comprises a $\text{Si}_{1-x}\text{Ge}_x$ buffer layer that has a thickness in the range from 0.2 to 1.5 μm , with a preferred value of about 0.5 μm , and has a percent Ge composition that is increased from x = 0 (in a continuous or stepwise fashion) to a value in the range from x = 0.10 to 1.0 with a preferred value of x = 0.25. Layer 2 serves to relax the strain caused by the lattice mismatch between layer 2 of graded Ge composition $\text{Si}_{1-x}\text{Ge}_x$ and Si substrate 1. Ge has a lattice spacing of 1.04 times the lattice spacing of Si. Thus for a relaxed top surface of buffer layer 2 where x equals 0.25, the lattice spacing of the unit cell along each axis in the top surface is about 1.01 times the lattice spacing of the unit cell of Si along each axis. For a description of how to grow relaxed low defect top surfaces of $\text{Si}_{1-x}\text{Ge}_x$ layers, reference is made to U.S. Pat. No. 5,659,187 which was issued on Aug. 19, 1997 to F. K. Legoues and B. S. Meyerson. After the graded region of layer 2, a 0.25 to about 10 μm thick, undoped or not-intentionally doped layer 3 of $\text{Si}_{1-y}\text{Ge}_y$ is grown, where the Ge composition, typically y = 0.25, is in the range from y = 0.10 to 1.0. Layer 3 acts as the absorbing medium for radiant

energy as well as a relaxed, device quality pseudosubstrate for growth of subsequent layers. The background impurities in layer 3 should be low enough to allow penetration of the electric field from the surface electrodes into the entire layer.

[0021] In one embodiment, the subsequent layers are a Si quantum well layer 4, a $\text{Si}_{1-y}\text{Ge}_y$ undoped or not-intentionally doped offset layer 5, a doped $\text{Si}_{1-y}\text{Ge}_y$ supply layer 6 and optionally a Si layer 7. By an undoped layer, it is meant a not-intentionally doped layer which may have a background dopant concentration so low as to not substantially affect the function of the layer. The Ge composition of layers 5 and 6 are in the range of $y = 0.1$ to 1.0 and y is preferably the same as the composition of layer 3. A quantum well for electrons is formed in Si layer 4 due to the conduction band splitting arising from the tensile strain in Si layer 4. The isolation for MODFET 15 is achieved by forming an etched mesa region, thereby exposing the surface 8 of $\text{Si}_{1-y}\text{Ge}_y$ buffer layer 3 in the etched regions, as shown in Fig. 1B. Next, in Fig. 1C, n-type implanted regions 9 are formed to facilitate making low-resistance contacts to the Si quantum well layer 4. The source and drain metallization 10 can then be deposited as depicted in Fig. 1D, followed by the gate metallization 12 shown in Fig. 1E.

[0022] The MSM photodetector is created by depositing interdigitated Schottky electrodes 11 on the exposed surface 8 of buffer layer 3. To simplify the fabrication process, it is possible for MSM electrodes 11 to be defined in the same lithographic step as the Ohmic metallization 10, as depicted in Fig. 1D. MSM electrodes 11 are configured in such a way such that a bias applied between adjacent electrodes, as shown in Fig. 1E, creates an electric field that penetrates into the underlying absorbing layer 3. Light or radiant 14 energy incident from or passing through surface 8 creates free carriers, electrons 15 and holes 16, in layer 3 that travel to electrodes 11, creating a current signal that is proportional to the power of the incident light.

[0023] Fig. 2 depicts the manner in which the devices shown in Fig. 1 are connected to form a simple photoreceiver circuit 17. A bias voltage, V_{diode} , is applied to the positive MSM electrode, while the negative electrode is connected to the gate of depletion-mode transistor 18, and to a bias resistor 19, R_{bias} , which is connected to a negative supply voltage, $-V_{\text{ss}}$. The transistor source is connected to ground, while the drain is connected to a load resistor 20, R_{load} , which is connected to the supply voltage, V_{dd} . In this configuration, the photocurrent induced by the incident light creates a voltage across the bias resistor 19 which is input to the gate of the transistor 18, thereby modulating the transistor current, and creating an amplified signal at the output lead 21, V_{out} . Resistors 19 and 20 may be formed and interconnected on the chip with the photodetector 22 and transistor 18 which is well known in the art. Other optoelectronic circuits may be formed which for example use more transistors to optimize the circuit to the application.

[0024] Fig. 3 shows another embodiment of the invention that is the same as that shown in Fig. 1E, except that the MSM photodetector is surrounded by a deep isolation trench 23 that extends from the surface 8 of the relaxed buffer layer 3 down into the substrate 1. Isolation trench 23 serves to confine the carriers that are generated in $\text{Si}_{1-y}\text{Ge}_y$ buffer layer 3 from diffusing laterally outside the region directly beneath the detector geometry. The trench also serves to isolate slow carriers generated outside the high-field region directly beneath the detector geometry from being collected by the surface electrodes 11, thereby leading to improved high-frequency performance. Furthermore, deep isolation trench 23 can be planarized by filling with a dielectric material 24. The trench can readily be incorporated into the fabrication scheme shown in Figs. 1A-1E, by etching deep isolation trench 23 before the mesa isolation in Fig. 1B, then filling the trench with dielectric material 24, followed by a planarization step. The subsequent fabrication steps can then be performed as depicted in Fig. 1B-1E.

[0025] Fig. 4A shows a not claimed semiconductor structure that is the same as that shown in Fig. 1E, except that the relaxed buffer layer 38, over layer 2, is composed of a symmetrically strained superlattice instead of a constant-composition alloy $\text{Si}_{1-y}\text{Ge}_y$. The superlattice consists of alternating layers of $\text{Si}_{1-x}\text{Ge}_x$, 35, and $\text{Si}_{1-z}\text{Ge}_z$, 36, where $x < y < z$, and have Ge-compositions such that the average composition in buffer layer 38 is equal to y where y is in the range from 0.1 to 0.9 , with a preferred value of 0.25 . The tensile strain in $\text{Si}_{1-x}\text{Ge}_x$ layer 35, and the compressive strain in $\text{Si}_{1-z}\text{Ge}_z$ layer 36 enhances the absorption of radiation by reducing the effective band gap of buffer layer 38. To ensure that the photogenerated carriers are not trapped in the potential wells formed by strained layers 35 and 36, the Ge composition of buffer layer 38 can be graded in a continuous fashion, to produce a smooth, rather than abrupt, potential profile. This situation is shown schematically in Fig. 4B, where the conduction and valence band edges, shown by curves 41 and 42, of alternating strained layers 35 and 36 are plotted along with the conduction and valence band edges, shown by curves 43 and 44, of a constant composition layer. The average band gap of the symmetric superlattice E_{g2} , shown by arrow 45, is reduced compared to that of the constant composition layer, E_{g1} , shown by arrow 46, leading to greater photoabsorption in the symmetric superlattice. The operation of the MODFET 15 structure shown in Fig. 4A is not affected by the symmetric superlattice because no net strain is built up in layer 38. Therefore, after the growth of the superlattice 38, only a thin, constant-composition $\text{Si}_{1-y}\text{Ge}_y$ layer 37, needs to be deposited before growing the MODFET 15 layers 4-7. For layer 37, y is in the range from 0.1 to 0.9 , and is preferably equal to the average Ge-composition of layer 38.

[0026] Another not claimed semiconductor structure is shown in Fig. 5, where a SiGe MSM photodetector is integrated with a p-channel MODFET 47. This configuration consists of a graded buffer layer 2 followed by a

constant composition $\text{Si}_{1-y}\text{Ge}_y$ absorbing layer 3, similar to that of Figs. 1A-1E. These layers are followed by a layer structure for a p-channel MODFET 47, consisting of a $\text{Si}_{1-w}\text{Ge}_w$ doped layer 48, where $w < y$, an undoped $\text{Si}_{1-y}\text{Ge}_y$ layer 49, a compressive-strained $\text{Si}_{1-z}\text{Ge}_z$ quantum well layer 50, where $z > y$, an undoped $\text{Si}_{1-y}\text{Ge}_y$ layer 51, and optionally a thin Si layer 52. The Ge percentages for this embodiment can vary from $y = 0.1$ to 0.9 , $w = 0$ to 0.5 , and $z = 0.5$ to 1.0 . This example could be particularly useful because the high Ge-content buffer layer 3 produces very efficient optical absorption, yet is also ideal for producing very high hole mobilities in p-channel MODFETs due to the compressive strain in the $\text{Si}_{1-z}\text{Ge}_z$ quantum well layer 50, particularly for the case of a pure-Ge channel where the mobility is not degraded by alloy scattering. MODFET 47 can be fabricated similar to the n-type device process shown in Figs. 1A-1E, where a mesa etch is used to isolate MODFET 47 and expose the surface 8 of photodetector absorbing layer 3. Next, p-type implanted regions 53 are formed to create low-resistance contacts to the $\text{Si}_{1-z}\text{Ge}_z$ quantum well layer 50. The source and drain metallization 54 can then be deposited, followed by the gate metallization 56. The example in Fig. 5 could also be fabricated with a reduced number of fabrication steps by defining the MSM electrodes 55 in the same lithographic step as the gate metallization 56 for MODFET 47.

[0027] As the Ge content of the buffer layers is increased, the band gap shrinks, leading to larger dark currents for the photodiode. A method of reducing the dark current without a dramatic increase in process complexity is to use different materials for alternate electrodes of the photodetector. Fig. 6A shows one embodiment of the invention, where the positively-biased electrodes 60 of the MSM photodiode have a high Schottky barrier height for holes, and the negatively-biased electrodes 61 have a high Schottky barrier height for electrons. To simplify the fabrication process, it is possible for the positively-biased (negatively-biased) electrodes 60 (61) to be defined in the same lithographic step as the Ohmic (gate) metallization, 10 (12). Possible candidates for the positively-biased MSM electrodes and Ohmic contact material are Er, W, Ti, Ni and Co, while the negatively-biased MSM electrodes and gate material might be Pt or Ir.

[0028] Fig. 6B shows another embodiment of the invention where negatively biased photodiode electrode 61 is composed of a material with high Schottky barrier for electrons, such as Pt or Ir, and the positively biased electrode is composed of n-type doped region 63, and electrode 64 which makes an Ohmic contact to region 63. As in Fig. 6A, the fabrication process can be simplified by fabricating n-type doped region 63 and positively-biased electrode 64 at the same time as MODFET 15 source-drain implant 9, and Ohmic metallization 10, and negatively-biased electrode 61 at the same time as MODFET gate metallization 12.

[0029] Fig. 6C shows another embodiment of the in-

vention where the photodiode consists of a lateral p-i-n geometry, and where the positively-biased photodiode electrode is composed of n-type doped region 63, and electrode 64 which makes an Ohmic contact to region 63, and the negatively-biased photodiode electrode is composed of p-type doped region 65, and an electrode 66 which makes an Ohmic contact to region 65.

[0030] The photodetector performance can be optimized by varying the properties of the substrate. For instance, Fig. 7A shows a structure similar to Fig. 1E, where the substrate is an SOI wafer 70 and consists of a thick Si substrate 71, a SiO_2 layer 72, and a roughly 200 nm-thick Si layer 73. Without degrading MODFET 15 performance, SiO_2 layer 72 can improve the performance of the SiGe MSM photodetector by preventing slow carriers generated in Si substrate 71 below SiO_2 layer 72 from reaching the MSM surface electrodes 11, thereby increasing the detector speed. The amount of light reflected back into buffer layer 3 can be maximized by adjusting the thickness of SiO_2 layer 72 to equal odd integer multiples of $1/4n$, where 1 is the wavelength of the incident light, and n is the refractive index of SiO_2 .

[0031] Similarly, as shown in Fig. 7B, the substrate could consist of a heavily doped ($> 10^{18} \text{ cm}^{-3}$) Si wafer 74 that causes photogenerated carriers in the layer to recombine before they can reach surface electrodes 11. The heavily-doped substrate 74 also acts to prevent the electric field produced by MSM interdigitated electrodes 11 from penetrating into substrate 74, thereby increasing the electric field strength in undoped SiGe absorbing layer 3, and subsequently increasing the detector speed.

[0032] As shown in Fig. 7C, the substrate capacitance can be reduced compared to the embodiment shown in Fig. 7B by selectively doping substrate 1 only in region 75 underneath MSM interdigitated electrodes 11. Selectively-doped region 75 can easily be formed before the growth of the Si/SiGe epi-layers using ion implantation, and then later aligned to MSM interdigitated electrodes 11.

[0033] Fig. 8C, curve 77, is a graph of the frequency response of the SiGe MSM photodetector comprising a $\text{Si}_{0.75}\text{Ge}_{0.25}$ absorbing layer at a thickness of $2.8 \mu\text{m}$ depicted in the cross-sectional and top-view diagrams of Figs. 8A and 8B. In Fig. 8C, the ordinate represents normalized photoresponse (dB) and the abscissa represents frequency (Hz). This device had a dc responsivity of 0.1 A/W , and displayed a -3 dB (-6 dB) bandwidth of 0.95 GHz (2.7 GHz), at $\lambda = 850 \text{ nm}$, for a bias voltage of +5 V. To our knowledge, this is the highest bandwidth achieved to date for a crystalline SiGe MSM photodetector for an incident radiation of $\lambda = 850 \text{ nm}$.

[0034] Fig. 9 shows the frequency response of an n-channel MODFET fabricated very similar to MODFET 15 shown in Fig. 1E. In Fig. 9, curve 78 shows the current gain versus frequency of the n-channel MODFET and curve 79 shows the maximum available gain versus frequency. In Fig. 9, the left ordinate represents current gain (dB), and the right ordinate represents maximum avail-

able gain (dB), and the abscissa represents frequency. The device shows a unity-gain cutoff frequency of 31 GHz, for a gate length of 0.7 μm , performance which is far superior to bulk Si MOSFETs of the same gate length. These results shown by curve 77 in Figs. 8C and by curves 78 and 79 in Fig. 9 on the individual components of the integrated circuit indicate the viability of the present invention, particularly given the straightforward method of integration described herein.

[0035] The selectively-doped substrate configuration shown in Fig. 7C can also be modified to integrate a vertical p-i-n photodetector 80 with an n- or p-channel MODFET 15. One such example is shown in Fig. 10, where p-i-n photodetector 80 and an n-channel MODFET 15 are fabricated using an n-type modulation-doped heterostructure, as described in Fig. 1E. In this embodiment, the p-i-n photodetector 80 is created when an n-type implanted region 80 and top contact 81 are aligned to a heavily-doped p-type region 82 created before the growth of the Si/SiGe epi-layers 2 and 3. The bottom contact 83 is made by etching down to and into substrate 1 as shown in Fig. 10. The example in Fig. 10 has the advantage that the n-channel, modulation-doped regions 4-7 do not need to be etched away to make top contact 81 of the p-i-n detector 80, because this contact already needs to be doped n-type. This example can also be used with a buffer layer 38 consisting of a symmetric superlattice as described in Fig. 4. MODFET 15 shown in this example is an n-channel device. For integration with a p-channel MODFET, the doping and polarity of the p-i-n contacts 80-83 can be reversed. The p-i-n configuration has the advantage that the carriers are always generated in a high-field region, and the distance the photogenerated carriers have to travel is reduced because detector electrodes 81 and 83 are on both the top and bottom of absorbing region 3.

[0036] Fig. 11 shows how an MSM photodiode 85 and MODFET 86 can be integrated using a fabrication scheme similar to that of a standard Si MOSFET or CMOS process. In the preferred embodiment, the layer structure is the same as that used in Fig. 1A. The MODFET 86 can be fabricated by depositing a thin gate oxide layer 90 followed by an undoped poly-silicon layer that is patterned and etched to define the gate electrode 91. Next an ion implant is performed to define n-type source and drain regions 92 where poly-silicon gate electrode 91 is used as a self-aligned implant mask. Next, a mesa isolation etch is performed which exposes the surface 8 of the buffer layer 3 in the etched regions. Next an insulating layer 93, such as silicon nitride, is deposited and then etched to form sidewall spacer regions 94. Finally, a self-aligned silicide (salicide) process is performed, where metal is deposited, heated to form metal-silicide or metal-germanosilicide contacts 95 to n-type source and drain regions 92 and the unreacted metal selectively etched away. The main feature of this embodiment is that the MSM photodetector 85 can be fabricated at the same time as MODFET 86 source and drain contacts 95 using

the salicide process, by patterning windows in insulating layer 93 above SiGe buffer layer 3 to form metal-silicide or metal-germanosilicide photodetector electrodes 96 in openings of insulating layer 93.

[0037] Fig. 12 shows another not claimed example of a semiconductor structure where a SiGe MSM 97 and a strained-Si n-channel MOSFET 98 are integrated using a planar processing scheme. For this structure, the layer structure consists of the same graded $\text{Si}_{1-x}\text{Ge}_x$ layer 2 and constant composition, $\text{Si}_{1-y}\text{Ge}_y$ buffer layer 3 grown on Si substrate 1 as shown in Fig. 1E. On top of buffer layer 3 is grown a tensile-strained Si layer 100, as shown in Fig. 12. In the example, the MOSFET 98 is fabricated by depositing or growing a thin gate oxide layer 101, followed by an undoped poly-silicon layer, which is patterned and etched to define the gate electrode 102. Next an optional p-well implant 103, is performed for threshold voltage control, and an ion implant is performed to define n-type source and drain regions 104, where poly-silicon gate electrode 102 is used as a self-aligned implant mask. Next, trench isolation regions 105, are formed and filled with dielectric material 106, and a second insulating layer 107, such as silicon nitride, is deposited and etched to form sidewall spacer regions 108. Finally, a self-aligned silicide (salicide) process is performed, where metal is deposited, heated to form metal-silicide, or metal-germanosilicide contacts 109 on n-type source and drain regions 104, and the unreacted metal selectively etched away. The MSM photodetector 97 is fabricated using the same salicide process used to create the MOSFET 98 source and drain regions, by patterning windows in insulating layer 107 above SiGe buffer layer 3 to form metal-silicide or metal-germanosilicide photodetector electrodes 110 in the openings of insulating layer 107. This example has the advantage of utilizing a planar processing scheme, because Si layer 100 is not etched away. Because Si layer 100 is only ~ 10 nm thick, it has little effect on the photoabsorption, and can act as a stable surface material for formation of MSM electrodes 110.

[0038] Fig. 13 shows another not claimed example of a semiconductor structure where MSM photodetector 85 is integrated with both a p-channel and an n-channel Si/SiGe MOSFET, 139 and 140, using an epitaxial multi-layer structure. The layer structure consists of a Si substrate 1, a graded $\text{Si}_{1-x}\text{Ge}_x$ layer 2 and constant composition $\text{Si}_{1-y}\text{Ge}_y$ buffer layer 3 as described in Fig. 1A. In the example, on top of $\text{Si}_{1-y}\text{Ge}_y$ buffer layer 3 are grown an n-type doped $\text{Si}_{1-y}\text{Ge}_y$ supply layer 120, an undoped $\text{Si}_{1-y}\text{Ge}_y$ offset layer 121, a tensile-strained Si quantum well layer 122, which acts as the electron channel for the NMOS device, another undoped $\text{Si}_{1-y}\text{Ge}_y$ offset layer 123, a compressive-strained $\text{Si}_{1-z}\text{Ge}_z$ layer 124, where $z > y$, which acts as the hole channel for the PMOS device, an undoped $\text{Si}_{1-y}\text{Ge}_y$ offset layer 125, and an undoped Si layer 126. In this example, the Ge-percentages of layers 120, 121, 123 and 125 is in the range $y = 0.1$ to 0.9 , with a preferred value of $y = 0.25$. The Ge-percentage of layer 124 is in the range $z = 0.3$ to 1.0 , and preferably

has a value where $z-y$ is greater than 0.2. Next a thin gate oxide layer 127, is grown or deposited, followed by a p-type doped poly-silicon layer. The CMOS circuit can be fabricated by etching the poly-silicon to form the gates of the n- and p-type CMOS devices 128, which then act as implant masks for formation of p-type doped region 129, and n-type doped region 130. Doped regions 129 and 130 form contacts to the buried quantum well channel layers 124 and 122, respectively. Next, trench isolation regions 131, are formed and filled with dielectric material 132, for planarization. At this point, an etch is performed to expose the surface 8 of $\text{Si}_{1-y}\text{Ge}_y$ buffer layer 3, and a blanket insulating layer 134, such as silicon nitride, is deposited. windows for forming the photodiode electrodes are patterned and etched at the same time as nitride sidewall regions 135 are formed. Finally, a salicide step is performed, as described in Fig. 11, to create the MSM electrodes 136, as well as the source and drain contacts 137 and 138 of the PMOS and NMOS devices, respectively. The example shown in Fig. 13 is a versatile configuration where not only PMOS device 139 or NMOS device 140 can be combined with MSM photodetector 85 to act as part of a photoreceiver amplifier circuit, but PMOS device 139 and NMOS device 140 can be combined and used to form a CMOS logic circuit. Therefore, the embodiment in Fig. 13 can potentially be used to fabricate a high-speed photoreceiver circuit on the same chip as a high-speed, low-power CMOS technology, for future "system-on-a-chip" applications.

[0039] An integrated optoelectronic circuit and process for making is described incorporating a photodetector and a MODFET on a chip. The chip contains a single-crystal semiconductor substrate, a buffer layer of SiGe graded in composition, a relaxed SiGe layer, a quantum well layer, an undoped SiGe spacer layer and a doped SiGe supply layer. The photodetector may be a metal-semiconductor-metal (MSM) or a p-i-n device. The detector may be integrated with an n- or p-type MODFET, or both in a CMOS configuration, and the MODFET can incorporate a Schottky or insulating gate. The invention overcomes the problem of producing Si-manufacturing-compatible monolithic high-speed optoelectronic circuits for 850 nm operation by using epitaxially-grown Si/SiGe heterostructure layers.

Claims

1. A semiconductor structure comprising a single crystal semiconductor substrate (1), a $\text{Si}_{1-x}\text{Ge}_x$ buffer layer (2) graded from $x = 0$ to y where y is in the range from 0.1 to 1.0, a layer of relaxed $\text{Si}_{1-y}\text{Ge}_y$ (3) having a thickness in the range from 0.25 μm to 10 μm , a quantum well layer (4), an undoped $\text{Si}_{1-y}\text{Ge}_y$ spacer layer (5), and a doped Si_yGe_y supply layer (6), spaced apart drain and source regions (9) extending to the quantum well layer (4) so that said quantum well layer (4) is the conducting channel of

a field-effect transistor; wherein said undoped $\text{Si}_{1-y}\text{Ge}_y$ spacer layer (5) separates dopants in said doped $\text{Si}_{1-y}\text{Ge}_y$ supply layer (6) from said conducting channel; and wherein portions of said quantum well layer (4), said undoped $\text{Si}_{1-y}\text{Ge}_y$ spacer layer (5) and said doped $\text{Si}_{1-y}\text{Ge}_y$ supply layer (6) are removed to provide an expose portion of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ (3) layer to form a photodetector and wherein said exposed layer of relaxed $\text{Si}_{1-y}\text{Ge}_y$ (3) layer is the absorbing region of said photodetector.

2. The semiconductor structure of claim 1 further including a Schottky gate contact to control charge in said conducting channel to form a MODFET.
3. The semiconductor structure of claim 1 wherein electrodes (60, 61, 64, 65) are formed on said exposed portion of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer to form a photodetector.
4. The semiconductor structure of claim 1 wherein said quantum well layer is under tensile strain and consists of Si.
5. The semiconductor structure of claim 3 wherein said electrodes include two or more interdigitated Schottky electrodes.
6. The semiconductor structure of claim 3 further including a trench extending through said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer surface and surrounding said photodetector; optionally said trench is filled with a dielectric material.
7. The semiconductor structure of claim 3 wherein positively-biased electrodes of said photodetector comprise Er, W, Ti, Ni or Co, and provide Schottky contacts (60) with barrier height for holes that is greater than half the band gap of said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer, and negatively-biased electrodes (61) of said photodetector comprise Pt or Ir and provide Schottky contacts with barrier height for electrons that is greater than half the band gap of said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer.
8. The semiconductor structure of claim 5 wherein negatively-biased electrodes (61) of said photodetector comprise Pt or Ir and provide Schottky contacts with barrier height for electrons that is greater than half the band gap of said exposed relaxed $\text{Si}_{1-y}\text{Ge}_y$ layer, and positively-biased electrodes (64) of said photodetector comprise Er, W, Ti, Ni or Co, and form Ohmic contact to an n-type doped region (63).
9. The semiconductor structure of claim 5 wherein negatively-biased electrodes (66) of said photodetector form Ohmic contacts to a p-type doped region (65) and said positively-biased electrodes (64) of said

photodetector form an Ohmic contact to an n-type doped region (63).

10. The semiconductor structure of claim 1 wherein said substrate is heavily-doped greater than 10^{18} atoms/cm³, or wherein said substrate is an SOI substrate comprising a thick Si layer, a SiO₂ layer, and a Si overlayer.

11. The semiconductor structure of claim 3 wherein said substrate is lightly-doped Si, and the region of said substrate underneath said photodetector is heavily-doped greater than 10^{18} atoms/cm³.

12. The semiconductor structure of claim 3 wherein said photodetector absorbing region is bordered by deep trenches extending from said photodetector surface down to said Si substrate, and filled with a dielectric material, so as to prevent photogenerated carriers generated in said Si_{1-y}Ge_y buffer layer from diffusing laterally past said deep trenches.

13. The semiconductor structure of claim 1 further including spaced apart drain and source regions extending to said quantum well layer, a gate dielectric layer above said supply layer between said drain and source and a gate electrode above said dielectric layer to form a MOSFET.

14. The semiconductor structure of claim 1 further including first and second spaced apart doped regions, one above the other, with a portion of said relaxed Si_{1-y}Ge_y layer there between to form a photodetector and an Ohmic contact to said respective first and second doped regions for applying a potential there between, and optionally one of the following;

- a) further including a trench extending into said exposed relaxed Si_{1-y}Ge_y layer to provide a barrier to electrical charge;
- b) wherein said first doped region includes a region of said quantum well layer, said undoped Si_{1-y}Ge_y spacer layer and said doped Si_{1-y}Ge_y supply layer; or
- c) wherein said second doped region includes a region of said substrate.

15. A method for forming a semiconductor structure comprising the steps of:

selecting a single crystal semiconductor substrate (1),
forming a Si_{1-x}Ge_x buffer layer (2) graded from $x = 0$ to y in the range from 0.1 to 1.0,
forming a layer of relaxed Si_{1-y}Ge_y (3) having a thickness in the range from 0.25 μ m to 10 μ m,
forming a quantum well layer (4),
forming an undoped Si_{1-y}Ge_y spacer layer (5),

forming a doped Si_{1-y}Ge_y supply (6),
forming spaced apart drain and source regions extending to said quantum well layer (4) so that said quantum well layer (4) is the conducting channel of a field-effect transistor,
removing portions of said quantum well layer (4),
said undoped Si_{1-y}Ge_y spacer layer (5) and said doped Si_{1-y}Ge_y supply layer (6) to expose said relaxed Si_{1-y}Ge_y layer and forming electrodes (11) on said exposed relaxed Si_{1-y}Ge_y layer to form a photodetector, wherein said exposed layer of relaxed Si_{1-y}Ge_y (3) is the absorbing region of said photodetector.

Patentansprüche

1. Halbleiterstruktur, welche ein monokristallines Halbleitersubstrat (1), eine Si_{1-x}Ge_x-Pufferschicht (2), die einen Gradienten von $x = 0$ bis y aufweist, wobei y im Bereich von 0,1 bis 1,0 liegt, eine Schicht aus relaxiertem Si_{1-y}Ge_y (3) einer Dicke im Bereich von 0,25 μ m bis 10 μ m, eine Quantentopfschicht (4), eine undotierte Si_{1-y}Ge_y-Abstandsschicht (5) und eine dotierte Si_{1-y}Ge_y-Versorgungsschicht (6) umfasst, wobei sich Drain- und Source-Zonen (9), die einen Abstand voneinander aufweisen, bis zu der Quantentopfschicht (4) erstrecken, derart, dass es sich bei der Quantentopfschicht (4) um den leitenden Kanal eines Feldeffekttransistors handelt; wobei die undotierte Si_{1-y}Ge_y-Abstandsschicht (5) die Dotierstoffe in der dotierten Si_{1-y}Ge_y-Versorgungsschicht (6) von dem leitenden Kanal trennt; und wobei Abschnitte der Quantentopfschicht (4), der undotierten Si_{1-y}Ge_y-Abstandsschicht (5) und der dotierten Si_{1-y}Ge_y-Versorgungsschicht (6) entfernt sind, um einen frei liegenden Abschnitt der relaxierten Si_{1-y}Ge_y-Schicht (3) bereitzustellen, um einen Photodetektor zu bilden, und wobei es sich bei der frei liegenden Schicht der relaxierten Si_{1-y}Ge_y-Schicht (3) um die absorbierende Zone des Photodetektors handelt.
2. Halbleiterstruktur nach Anspruch 1, welche ferner einen Schottky-Gate-Kontakt umfasst, um die Ladung in dem leitenden Kanal zu regeln, um einen MODFET zu bilden.
3. Halbleiterstruktur nach Anspruch 1, wobei auf dem frei liegenden Abschnitt der relaxierten Si_{1-y}Ge_y-Schicht Elektroden (60, 61, 64, 65) ausgebildet sind, um einen Photodetektor zu bilden.
4. Halbleiterstruktur nach Anspruch 1, wobei die Quantentopfschicht unter Zugspannung steht und aus Si besteht.
5. Halbleiterstruktur nach Anspruch 3, wobei die Elek-

troden zwei oder mehr ineinander greifende Schottky-Elektroden umfassen.

6. Halbleiterstruktur nach Anspruch 3, welche ferner einen Graben umfasst, der sich durch die Fläche der frei liegenden relaxierten $\text{Si}_{1-y}\text{Ge}_y$ -Schicht hindurch erstreckt und den Photodetektor umgibt; gegebenenfalls ist der Graben mit einem dielektrischen Material gefüllt.
7. Halbleiterstruktur nach Anspruch 3, wobei Elektroden mit positiver Vorspannung des Photodetektors Er, W, Ti, Ni oder Co umfassen und Schottky-Kontakte (60) einer Barrierenhöhe für Defektelektronen bereitstellen, die größer ist als die Hälfte des Bandabstands der frei liegenden relaxierten $\text{Si}_{1-y}\text{Ge}_y$ -Schicht, und Elektroden (61) mit negativer Vorspannung des Photodetektors Pt oder Ir umfassen und Schottky-Kontakte einer Barrierenhöhe für Elektronen bereitstellen, die größer ist als die Hälfte des Bandabstands der frei liegenden relaxierten $\text{Si}_{1-y}\text{Ge}_y$ -Schicht.
8. Halbleiterstruktur nach Anspruch 5, wobei Elektroden (61) mit negativer Vorspannung des Photodetektors Pt oder Ir umfassen und Schottky-Kontakte einer Barrierenhöhe für Elektronen bereitstellen, die größer ist als die Hälfte des Bandabstands der frei liegenden relaxierten $\text{Si}_{1-y}\text{Ge}_y$ -Schicht, und Elektroden (64) mit positiver Vorspannung einen Ohmschen Kontakt zu einer n-leitend dotierten Zone (63) bilden.
9. Halbleiterstruktur nach Anspruch 5, wobei Elektroden (66) mit negativer Vorspannung des Photodetektors Ohmsche Kontakte zu einer p-leitend dotierten Zone (65) bilden und die Elektroden (64) mit positiver Vorspannung des Photodetektors einen Ohmschen Kontakt zu einer n-leitend dotierten Zone (63) bilden.
10. Halbleiterstruktur nach Anspruch 1, wobei das Substrat mit mehr als 10^{18} Atomen/ cm^3 stark dotiert ist oder wobei es sich bei dem Substrat um ein SOI-Substrat handelt, welches eine dicke Si-Schicht, eine SiO_2 -Schicht und eine Si-Deckschicht umfasst.
11. Halbleiterstruktur nach Anspruch 3, wobei es sich bei dem Substrat um leicht dotiertes Si handelt und die Zone des Substrats unterhalb des Photodetektors mit mehr als 10^{18} Atomen/ cm^3 stark dotiert ist.
12. Halbleiterstruktur nach Anspruch 3, wobei die absorbierende Photodetektorzone von tiefen Gräben begrenzt ist, welche sich von der Photodetektorfläche aus nach unten bis zu dem Si-Substrat erstrecken und mit einem dielektrischen Material gefüllt sind, um zu verhindern, dass Ladungsträger, die in der

$\text{Si}_{1-y}\text{Ge}_y$ -, Pufferschicht durch Photonen erzeugt werden, seitlich über die tiefen Gräben hinaus diffundieren.

13. Halbleiterstruktur nach Anspruch 1, welche ferner Drain- und Source-Zonen, die einen Abstand voneinander aufweisen und sich bis zu der Quantentopfschicht erstrecken, eine Gate-Dielektrikumschicht oberhalb der Versorgungsschicht zwischen der Drain- und der Source-Zone und eine Gate-Elektrode oberhalb der dielektrischen Schicht umfasst, um einen MOSFET zu bilden.
14. Halbleiterstruktur nach Anspruch 1, welche ferner, eine über der anderen, eine erste und zweite dotierte Zone umfasst, die einen Abstand voneinander aufweisen, wobei sich zwischen diesen ein Abschnitt der relaxierten $\text{Si}_{1-y}\text{Ge}_y$ -Schicht befindet, um einen Photodetektor und einen Ohmschen Kontakt zu der ersten bzw. zweiten dotierten Zone zu bilden, um zwischen diesen eine Potentialdifferenz anzulegen, und wobei wahlweise eine der folgenden Bedingungen erfüllt ist:
 - a) sie umfasst ferner einen Graben, welcher sich in die frei liegende relaxierte $\text{Si}_{1-y}\text{Ge}_y$ -Schicht erstreckt, um eine Barriere für eine elektrische Ladung zu schaffen;
 - b) wobei die erste dotierte Zone eine Zone der Quantentopfschicht, der undotierten $\text{Si}_{1-y}\text{Ge}_y$ -Abstandsschicht und der dotierten $\text{Si}_{1-y}\text{Ge}_y$ -Versorgungsschicht umfasst; oder
 - c) wobei die zweite dotierte Zone eine Zone des Substrates umfasst.
15. Verfahren zur Bildung einer Halbleiterstruktur, welches die folgenden Schritte umfasst:
 - Auswählen eines monokristallinen Halbleitersubstrats (1),
 - Bilden einer $\text{Si}_{1-x}\text{Ge}_x$ -Pufferschicht (2), welche einen Gradienten von $x = 0$ bis y im Bereich von 0,1 bis 1,0 aufweist,
 - Bilden einer Schicht aus relaxiertem $\text{Si}_{1-y}\text{Ge}_y$ (3), welche eine Dicke im Bereich von 0,25 μm bis 10 μm aufweist,
 - Bilden einer Quantentopfschicht (4),
 - Bilden einer undotierten $\text{Si}_{1-y}\text{Ge}_y$ -Abstandsschicht (5),
 - Bilden einer dotierten $\text{Si}_{1-y}\text{Ge}_y$ -Versorgungsschicht (6),
 - Bilden von Drain- und Source-Zonen, die einen Abstand voneinander aufweisen und sich bis zu der Quantentopfschicht (4) erstrecken, derart, dass es sich bei der Quantentopfschicht (4) um den leitenden Kanal eines Feldeffekttransistors handelt,
 - Entfernen von Abschnitten der Quantentopf-

schicht (4), der undotierten $\text{Si}_{1-y}\text{Ge}_y$ -Abstandsschicht (5) und der dotierten $\text{Si}_{1-y}\text{Ge}_y$ -Versorgungsschicht (6), um die relaxierte $\text{Si}_{1-y}\text{Ge}_y$ -Schicht frei zu legen, und bilden von Elektroden (11) auf der frei liegenden relaxierten $\text{Si}_{1-y}\text{Ge}_y$ -Schicht, um einen Photodetektor zu bilden, wobei es sich bei der frei liegenden Schicht aus relaxiertem $\text{Si}_{1-y}\text{Ge}_y$ (3) um die absorbierende Zone des Photodetektors handelt.

Revendications

1. Structure à semi-conducteur, comprenant un substrat (1) en semi-conducteur monocristallin, une couche tampon (2) en $\text{Si}_{1-x}\text{Ge}_x$, dans laquelle $x = 0$ à y , avec y dans la fourchette de 0,1 à 1,0, une couche (3) en $\text{Si}_{1-y}\text{Ge}_y$ relaxé, ayant une épaisseur dans la fourchette de 0,25 μm à 10 μm , une couche de puits quantique (4), une couche d'espacement (5) en $\text{Si}_{1-y}\text{Ge}_y$ non dopé, et une couche d'alimentation (6) en $\text{Si}_{1-y}\text{Ge}_y$ dopé, des régions de drain et de source (9) espacées, s'étendant vers la couche de puits quantique (4), de manière que ladite couche de puits quantique (4) soit le canal conducteur d'un transistor à effet de champ ; dans lequel ladite couche d'espacement (5) en $\text{Si}_{1-y}\text{Ge}_y$ non dopé sépare des dopants, situés dans ladite couche d'alimentation (6) en $\text{Si}_{1-y}\text{Ge}_y$ dopé, vis-à-vis dudit canal conducteur ; et dans lequel des parties de ladite couche de puits quantique (4), ladite couche d'espacement (5) en $\text{Si}_{1-y}\text{Ge}_y$ non dopé et ladite couche d'alimentation (6) en $\text{Si}_{1-y}\text{Ge}_y$ dopé sont éliminées pour fournir une partie exposée de ladite couche (3) en $\text{Si}_{1-y}\text{Ge}_y$ relaxé, de manière à former un photodétecteur et dans lequel ladite couche exposée de couche (3) en $\text{Si}_{1-y}\text{Ge}_y$ relaxé est la région absorbante dudit photodétecteur.
2. Structure à semi-conducteur selon la revendication 1, comprenant en outre un contact de grille de Schottky, pour commander la charge dans ledit canal conducteur, de manière à former un MODFET.
3. Structure à semi-conducteur selon la revendication 1, dans laquelle des électrodes (60, 61, 64, 65) sont formées sur ladite partie exposée de ladite couche en $\text{Si}_{1-y}\text{Ge}_y$ relaxé, de manière à former un photodétecteur.
4. Structure à semi-conducteur selon la revendication 1, dans laquelle ladite couche de puits quantique est placée sous une contrainte de traction et est composée de Si.
5. Structure à semi-conducteur selon la revendication 3, dans laquelle lesdites électrodes comprennent deux électrodes de Schottky interdigitées, ou plus.
6. Structure à semi-conducteur selon la revendication 3, comprenant en outre une tranchée, s'étendant à travers ladite surface de couche en $\text{Si}_{1-y}\text{Ge}_y$ relaxé exposée et entourant ledit photodétecteur ; ladite tranchée étant, en option, remplie d'un matériau diélectrique.
7. Structure à semi-conducteur selon la revendication 3, dans laquelle des électrodes, polarisées de manière positive, dudit photodétecteur sont composées de Er, W, Ti, Ni ou Co, et fournissent des contacts de Schottky (60) avec une hauteur de barrière pour des trous supérieure à la moitié de la largeur de bande interdite de ladite couche en $\text{Si}_{1-y}\text{Ge}_y$ relaxé exposée, et des électrodes (61), polarisées de manière négative, dudit photodétecteur sont composées de Pt ou Ir et fournissent des contacts de Schottky avec une hauteur de barrière pour des électrons supérieure à la moitié de la largeur de bande interdite de ladite couche en $\text{Si}_{1-y}\text{Ge}_y$ relaxé exposée.
8. Structure à semi-conducteur selon la revendication 5, dans laquelle des électrodes (61), polarisées de manière négative, dudit photodétecteur sont composées de Pt ou Ir et fournissent des contacts de Schottky avec une hauteur de barrière pour des électrons supérieure à la moitié de la largeur de bande interdite de ladite couche en $\text{Si}_{1-y}\text{Ge}_y$ relaxé exposée, et des électrodes (64), polarisées de manière positive, dudit photodétecteur sont composées de Er, W, Ti, Ni ou Co, et forment un contact ohmique avec une région (63) à dopage de type n.
9. Structure à semi-conducteur selon la revendication 5, dans laquelle des électrodes (66), polarisées de manière négative, dudit photodétecteur forment des contacts ohmiques avec une région (65) à dopage de type p, et lesdites électrodes (64), polarisées de manière positive, dudit photodétecteur forment un contact ohmique avec une région (63) à dopage de type n.
10. Structure à semi-conducteur selon la revendication 1, dans laquelle ledit substrat est fortement dopé, à plus de 10^{18} atomes/ cm^3 , ou dans lequel ledit substrat est un substrat SOI, comprenant une épaisse couche en Si, une couche en SiO_2 , et une surcouche en Si.
11. Structure à semi-conducteur selon la revendication 3, dans laquelle ledit substrat est en Si légèrement dopé, et la région dudit substrat située au-dessous dudit photodétecteur est fortement dopée, à plus de 10^{18} atomes/ cm^3 .
12. Structure à semi-conducteur selon la revendication 3, dans laquelle ladite région absorbante de photodétecteur est délimitée par des tranchées profondes,

s'étendant à partir de ladite surface de photodétecteur en descendant vers ledit substrat, et remplies d'un matériau diélectrique, de manière à empêcher que des porteurs photogénérés, générés dans ladite couche tampon en $\text{Si}_{1-y}\text{Ge}_y$, diffusent latéralement, au delà desdites tranchées profondes. 5

13. Structure à semi-conducteur selon la revendication 1, comprenant en outre des régions de drain et de source espacées, s'étendant vers ladite couche de puits quantique, une couche diélectrique de grille, située au-dessus de ladite couche d'alimentation, entre drain et source, et une électrode de grille, située au-dessus de ladite couche diélectrique, pour former un MOSFET. 10 15

14. Structure à semi-conducteur selon la revendication 1, comprenant en outre des première et deuxième région dopées, espacées, l'une au-dessus de l'autre, avec, entre elles, une partie de ladite couche en $\text{Si}_{1-y}\text{Ge}_y$ relaxé, pour former un photodétecteur et un contact ohmique avec lesdites première et deuxième régions dopées respectives, pour appliquer entre elles un potentiel et, en option, l'un des suivants : 20 25

- a) comprenant en outre une tranchée, s'étendant dans ladite couche en $\text{Si}_{1-y}\text{Ge}_y$ relaxé exposée, pour fournir une barrière à une charge électrique ; 30
b) dans laquelle ladite première région dopée comprend une région de ladite couche de puits quantique, ladite couche d'espacement en $\text{Si}_{1-y}\text{Ge}_y$ non dopé et ladite couche d'alimentation en $\text{Si}_{1-y}\text{Ge}_y$ dopé ; ou 35
c) dans laquelle ladite deuxième région dopée comprend une région dudit substrat. 40

15. Procédé pour former une structure à semi-conducteur, comprenant les étapes consistant à : 40

sélectionner un substrat (1) en semi-conducteur monocristallin,
former une couche tampon (2) en $\text{Si}_{1-x}\text{Ge}_x$, dans laquelle $x = 0$ à y , avec y dans la fourchette de 0,1 à 1,0, 45
former une couche (3) en $\text{Si}_{1-y}\text{Ge}_y$ relaxé, ayant une épaisseur dans la fourchette de 0,25 μm à 10 μm ,
former une couche de puits quantique (4), 50
former une couche d'espacement (5) en $\text{Si}_{1-y}\text{Ge}_y$ non dopé,
former une couche d'alimentation (6) en $\text{Si}_{1-y}\text{Ge}_y$ dopé,
former des régions de drain et de source espacées, s'étendant vers ladite couche de puits quantique (4), de manière que ladite couche de puits quantique (4) soit le canal conducteur d'un 55

transistor à effet de champ,
éliminer des parties de ladite couche de puits quantique (4), de ladite couche d'espacement (5) en $\text{Si}_{1-y}\text{Ge}_y$ non dopé et de ladite couche d'alimentation (6) en $\text{Si}_{1-y}\text{Ge}_y$ dopé, pour exposer ladite couche en $\text{Si}_{1-y}\text{Ge}_y$ relaxé, et former des électrodes (11) sur ladite couche en $\text{Si}_{1-y}\text{Ge}_y$ relaxé exposée, de manière à former un photodétecteur, dans lequel ladite couche (3) en $\text{Si}_{1-y}\text{Ge}_y$ relaxé exposée est la région absorbante dudit photodétecteur.

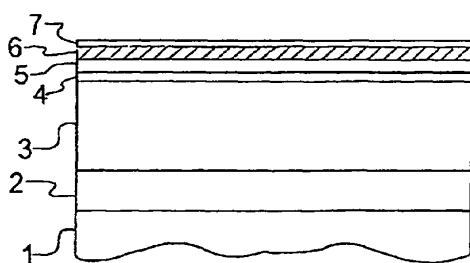


Fig. 1A

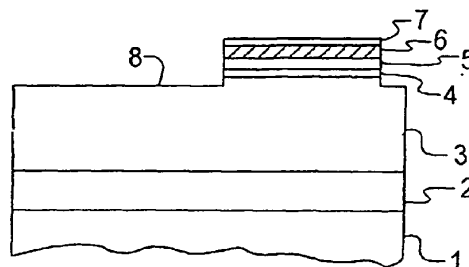


Fig. 1B

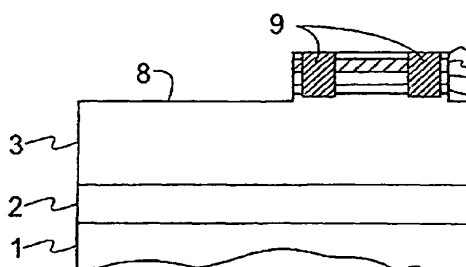


Fig. 1C

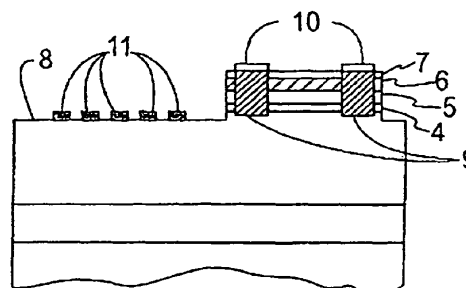


Fig. 1D

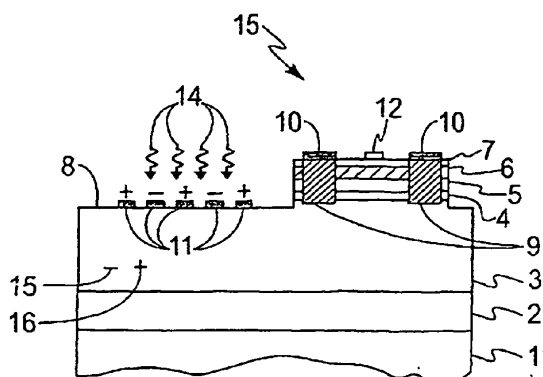


Fig. 1E

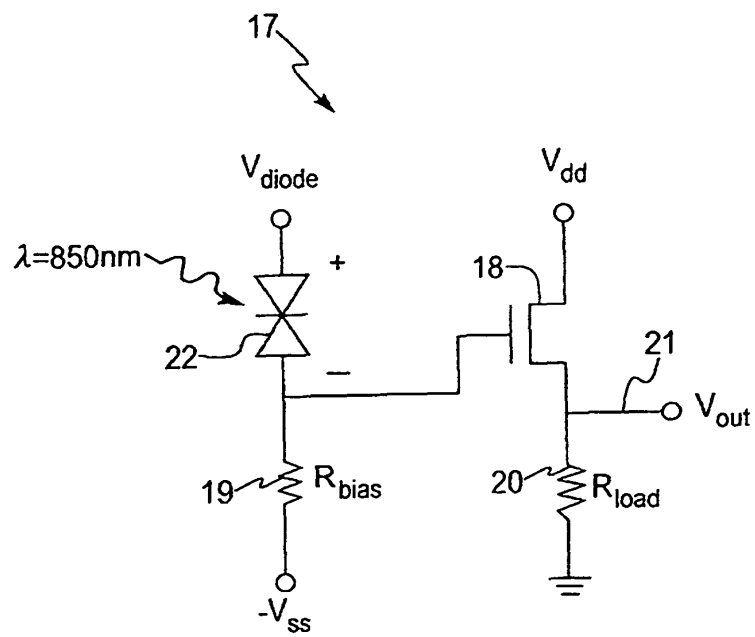


Fig. 2

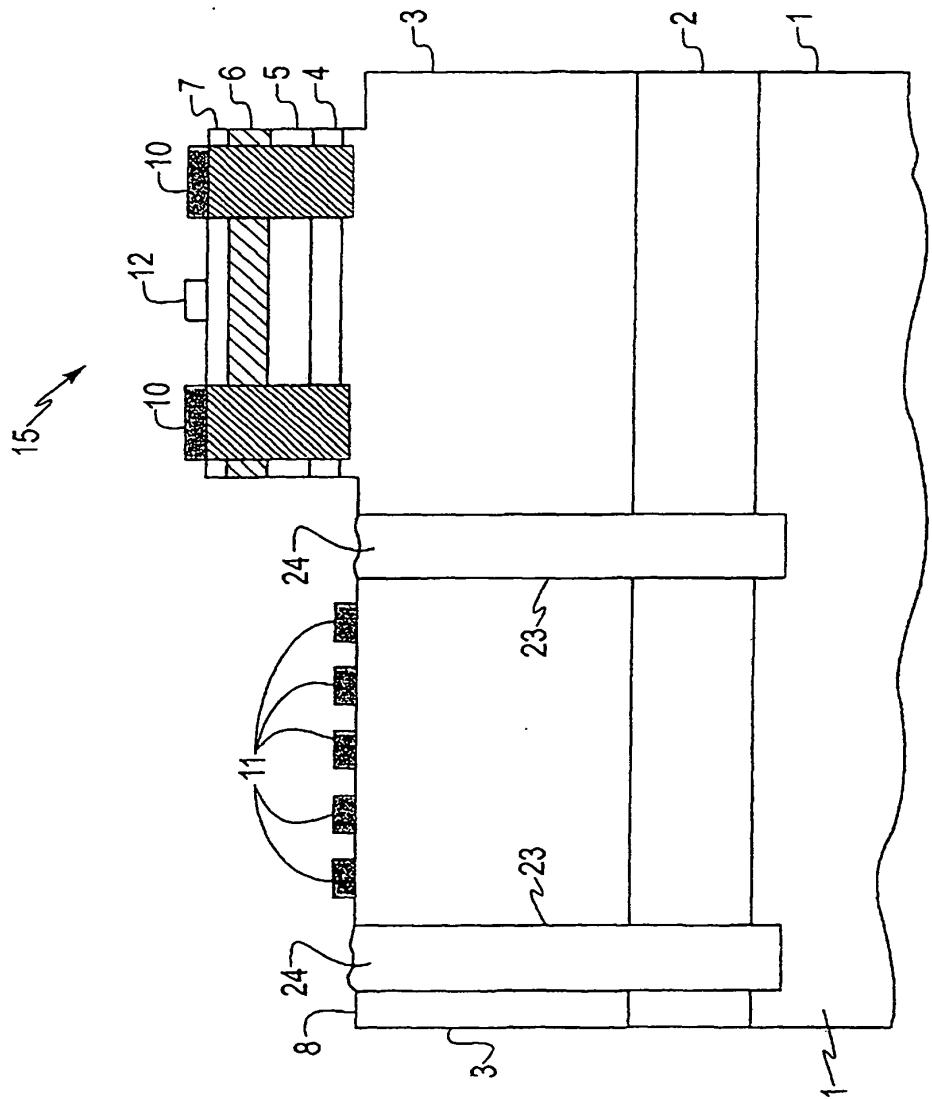


Fig. 3

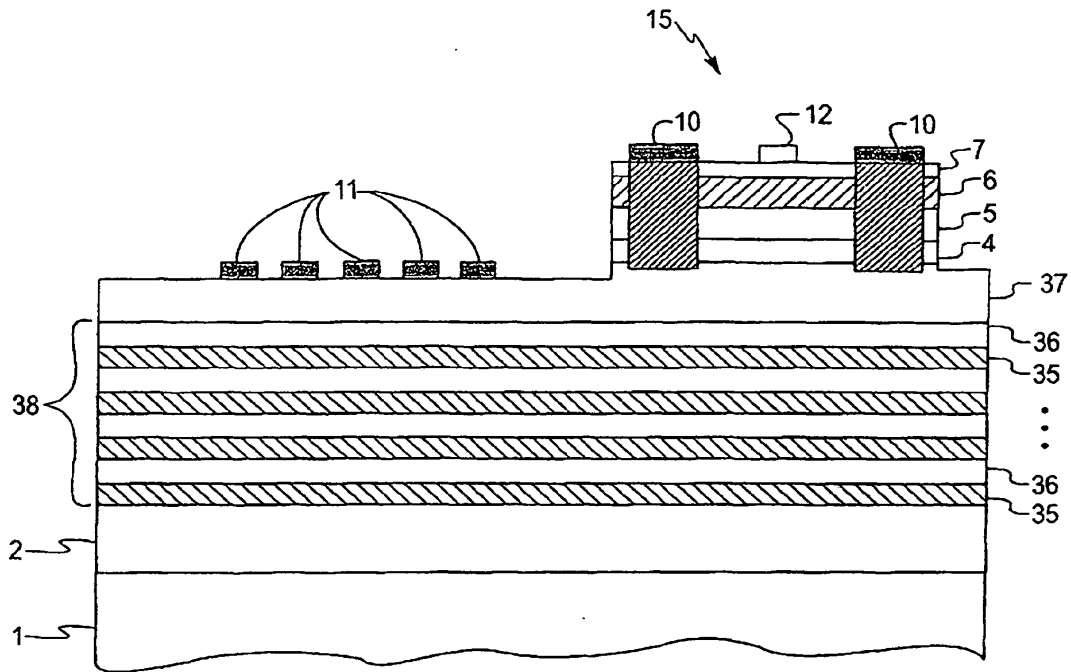


Fig. 4A

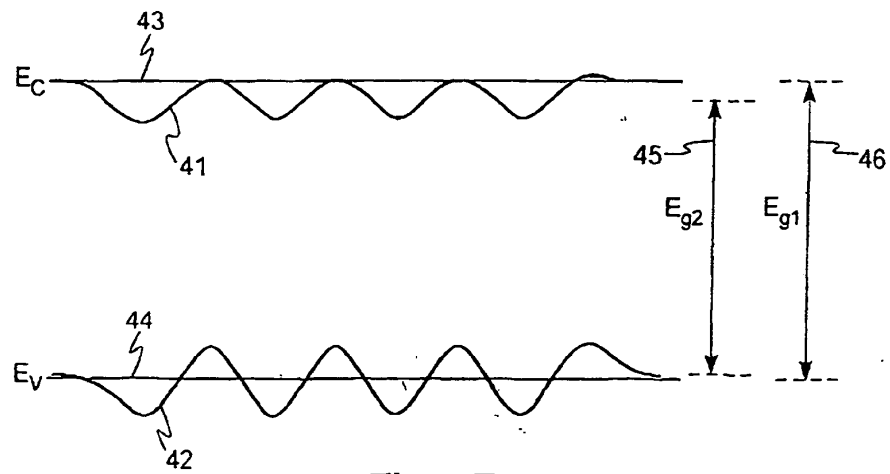


Fig. 4B

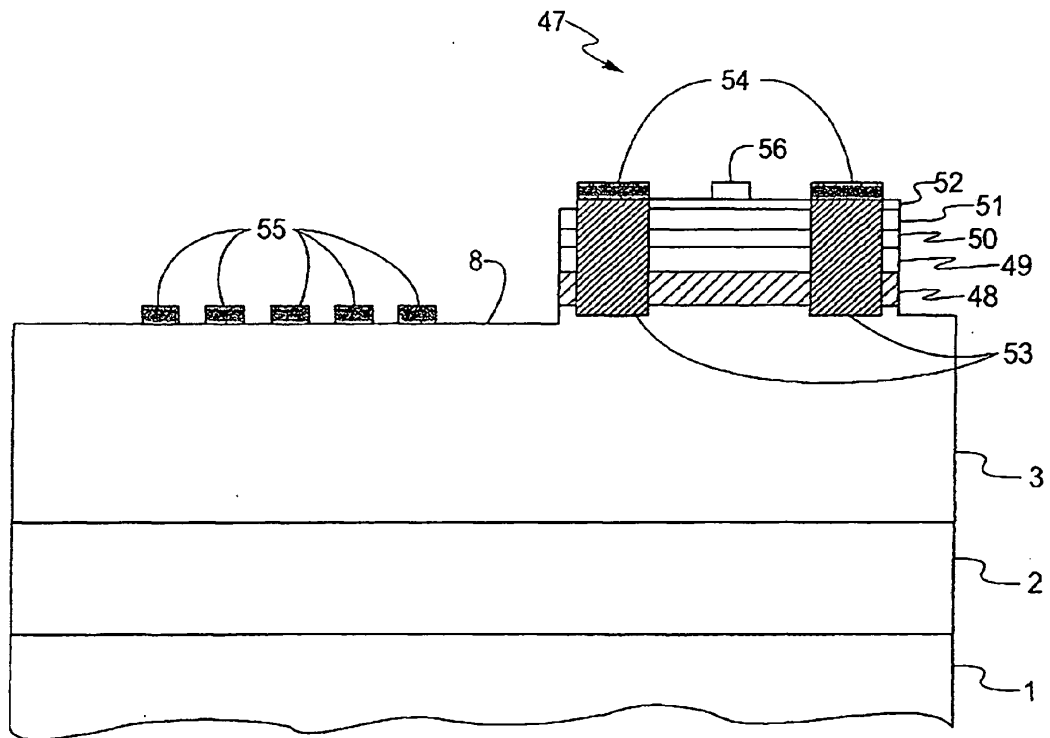


Fig. 5

Fig. 6A

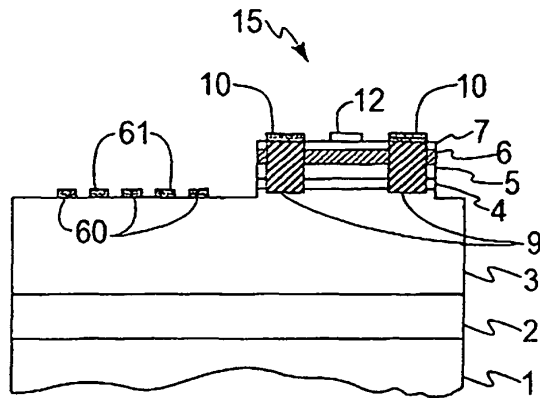


Fig. 6B

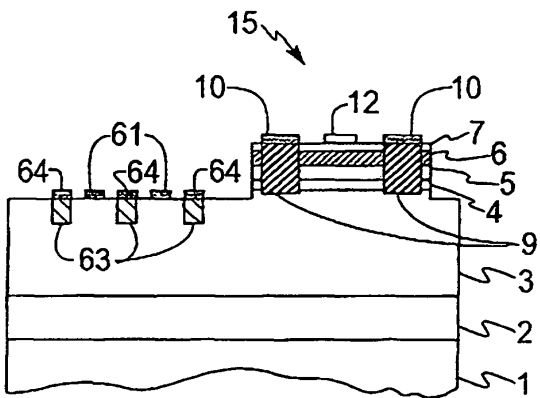
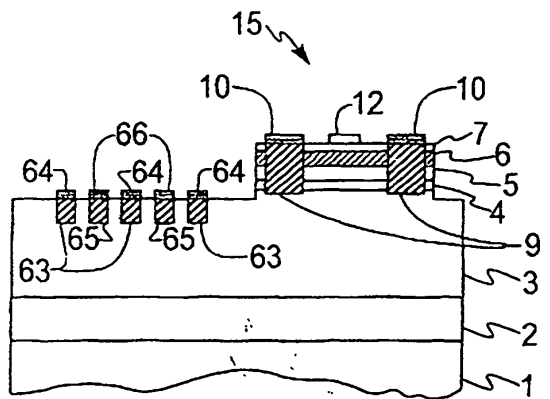


Fig. 6C



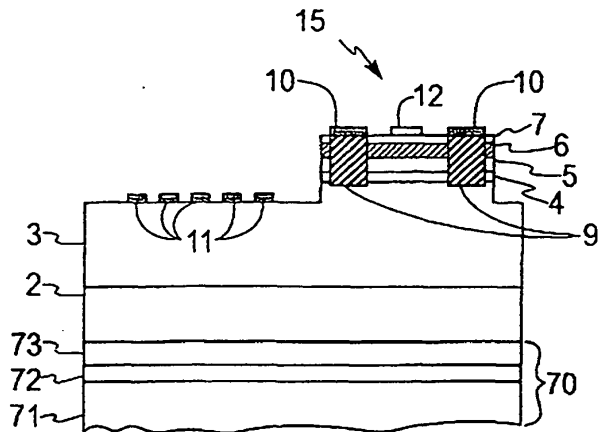


Fig. 7A

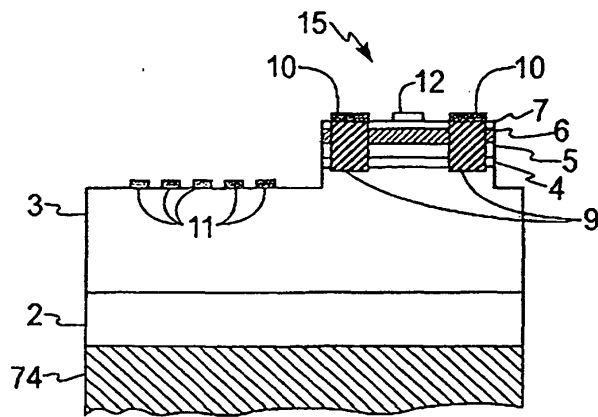


Fig. 7B

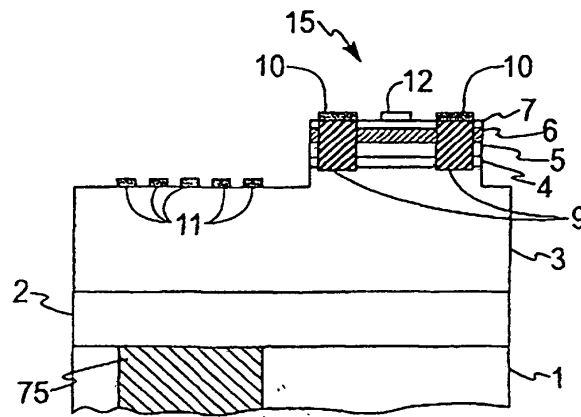


Fig. 7C

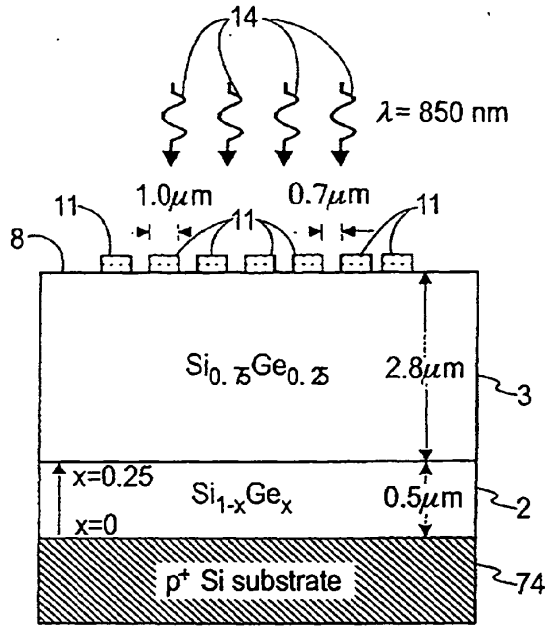


Fig. 8A

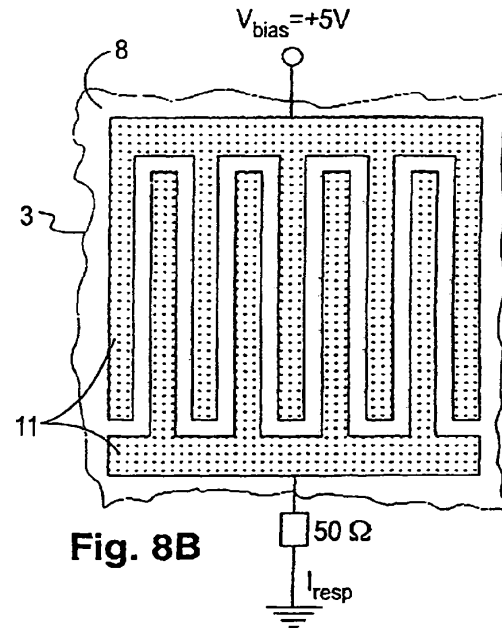


Fig. 8B

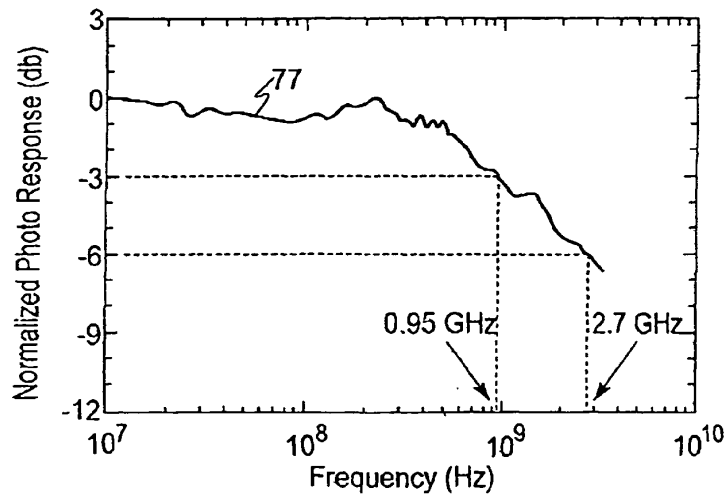


Fig. 8C

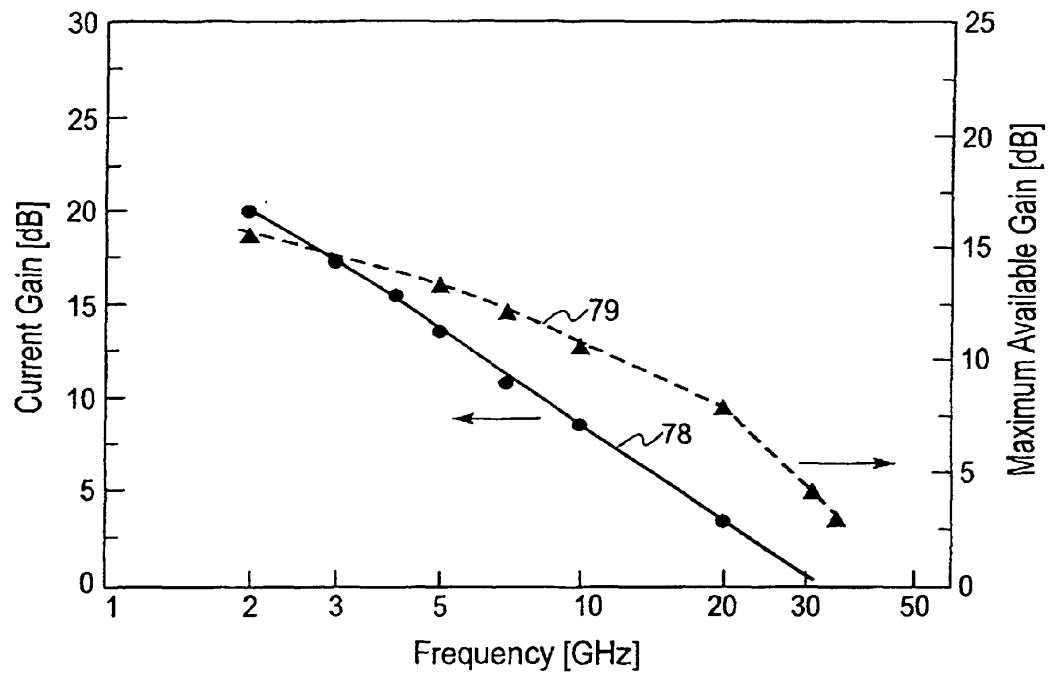


Fig. 9

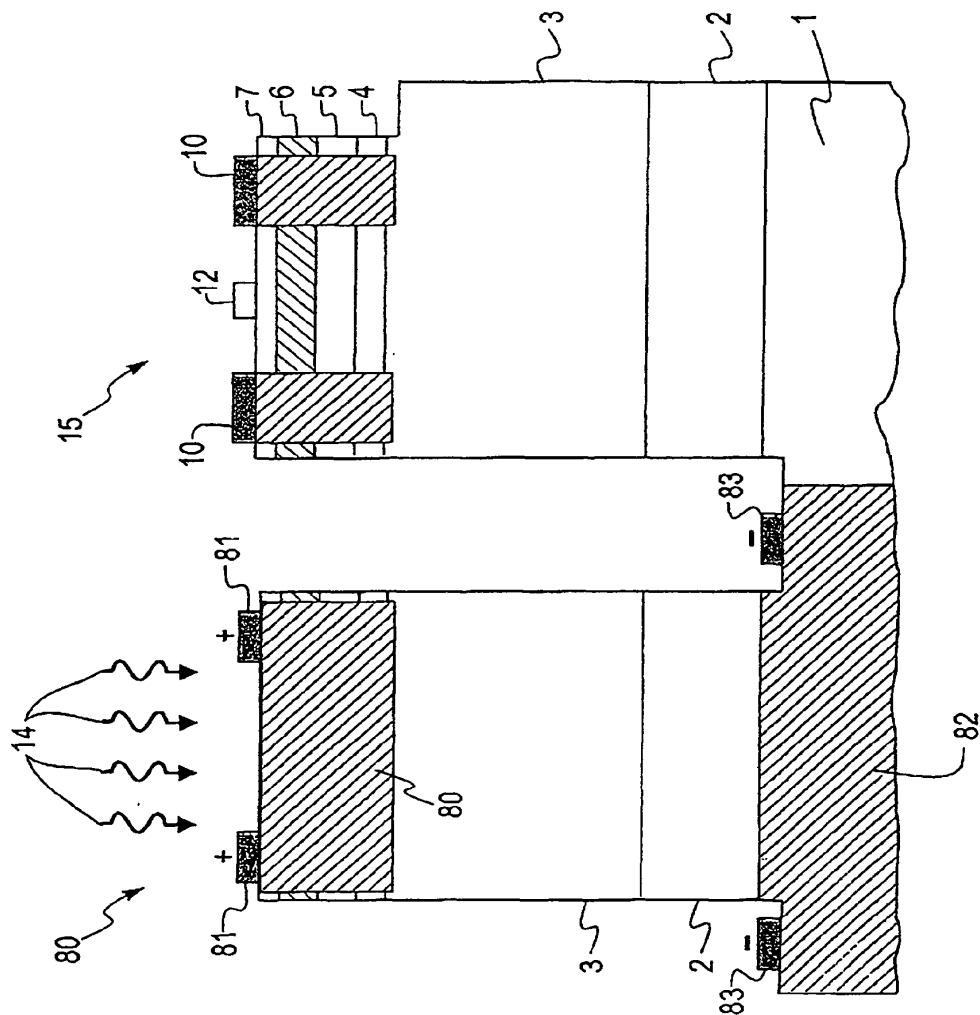


Fig. 10

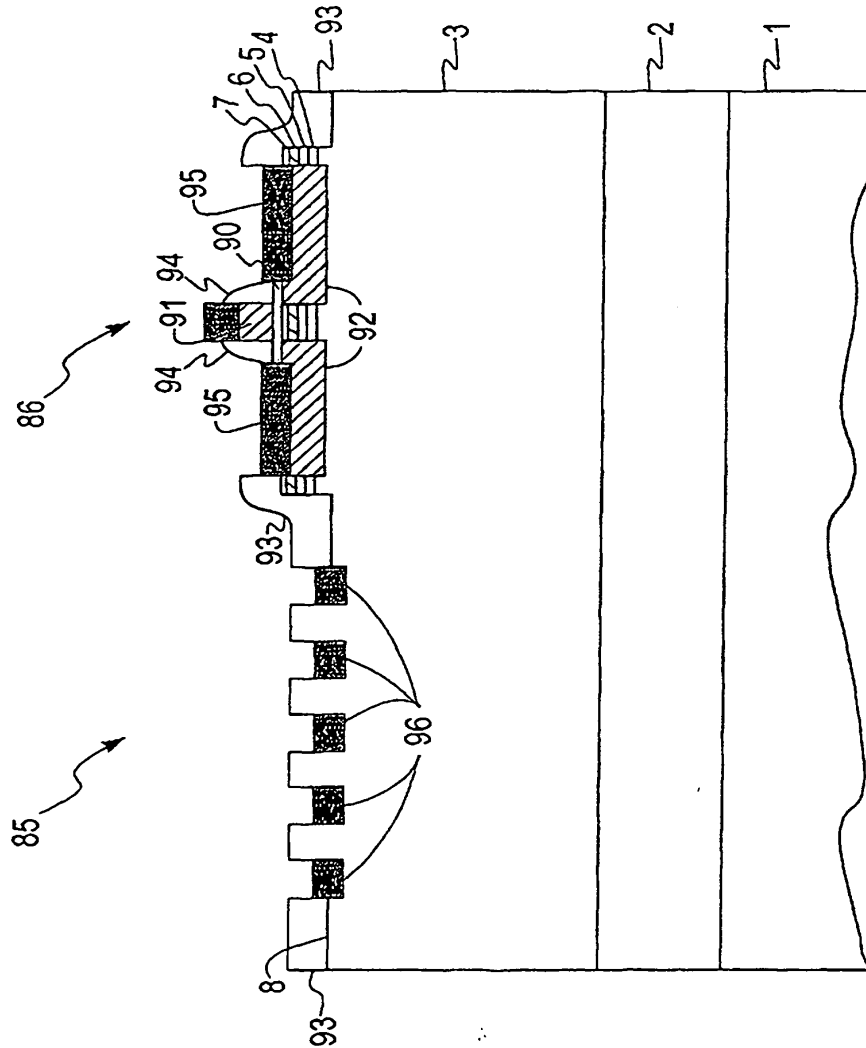


Fig. 11

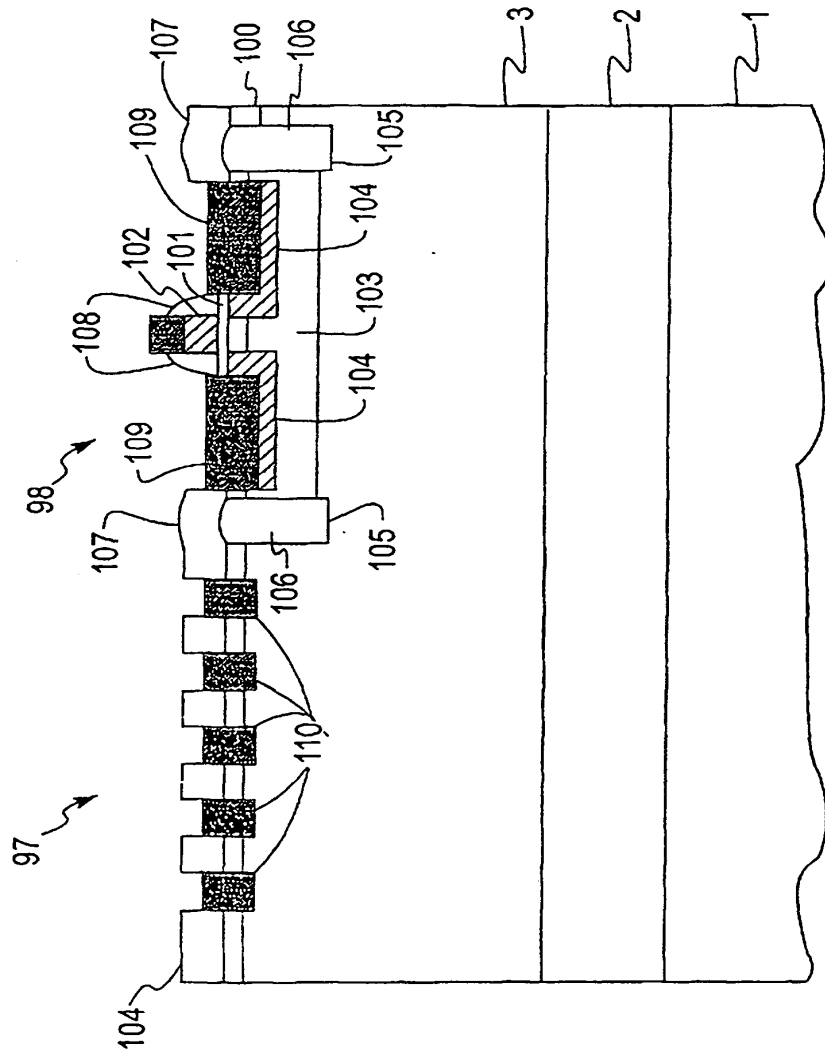


Fig. 12

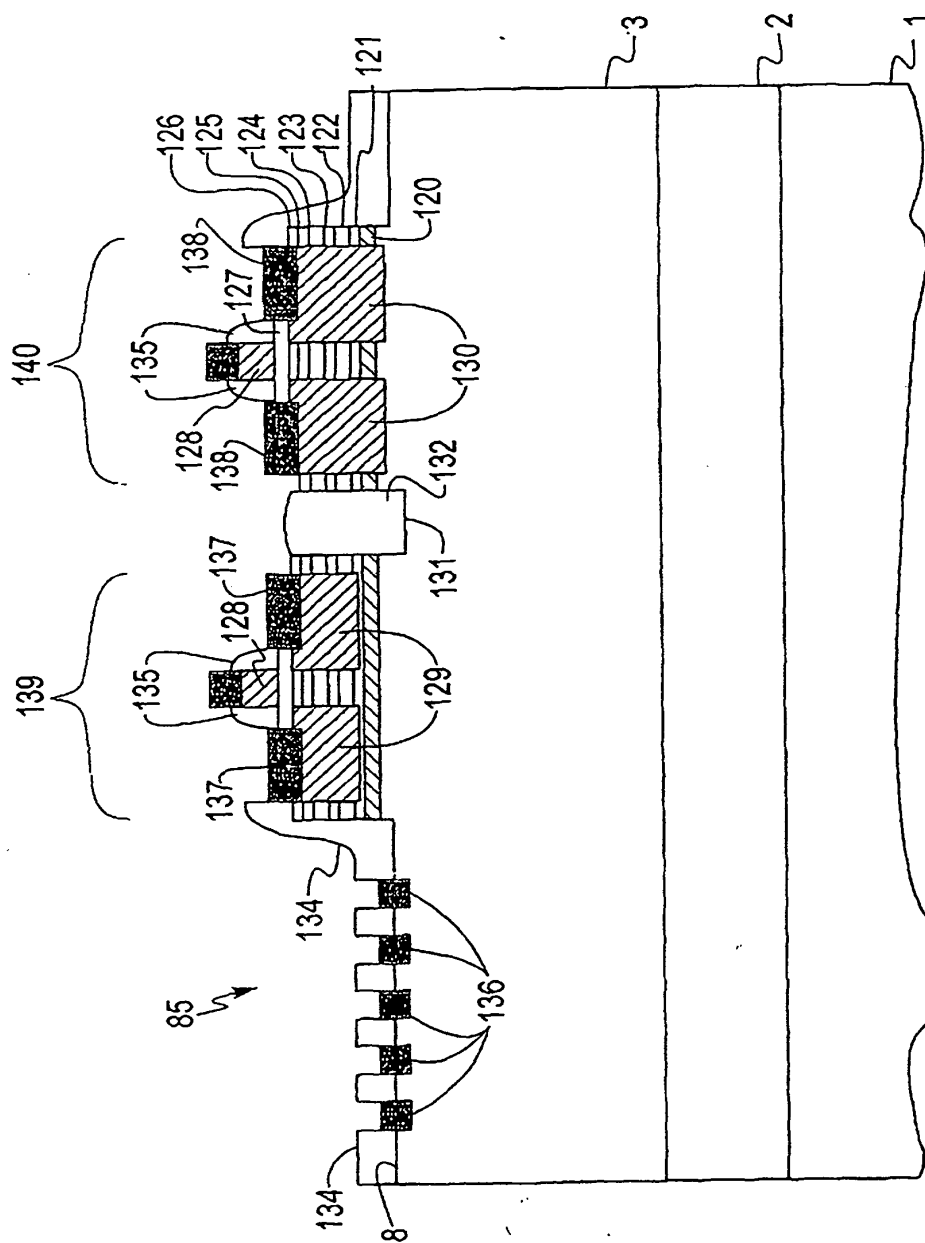


Fig. 13

REFERENCES CITED IN THE DESCRIPTION

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- US 5525828 A [0005]
- US 5659187 A [0006] [0020]
- US 5534713 A [0006]
- US 5298452 A [0020]

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- **V. Hurm et al.** *Electron. Lett.*, 1993, vol. 29, 9 [0003]
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- **M. Y. Liu et al.** *Appl. Phys. Lett.*, 1994, vol. 65, 887 [0004]
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MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

REFERENCE TO RELATED APPLICATIONS

- 5 **[0001]** This patent application is a continuation in-part of each of U.S. Application 18/113,474 and 17/974,325.
- [0002]** 18/113,474 is a division of 17/707,429, now Pat. 11,621,360.
- [0003]** 17/707,429 is a continuation in-part of 17/182,954, now Pat. 11,791,432.
- [0004]** 17/182,954 is a division of 16/528,958, now Pat. 11,121,271, which
- 10 claims priority to U.S. Provisional Patent.
- [0005]** 16/528,958 is a continuation in-part of 15/797,821, now Pat. 10,446,700
- [0006]** 16/528,958 claims priority to U.S. Provisional Pat. Applns. 62/713,455, 62/716,310, 62/717,750, 62/719,689, 62/724,449, 62/733,476, 62/737,062, 62/750,016, 62/770,656, 62/772,498, 62/777,157, 62/779,693, 62/784,342,
- 15 62/794,330, 62/797,141, 62/797,263, 62/800,371, 62/802,171, 62/802,718, 62/805,850, 62/808,949, 62/819,604, 62/819,669, 62/820,695, 62/828,976, 62/841,798, 62/843,206, 62/846,554, 62/853,280, 62/860,115, 62/863,231, 62/863,852, 62/867,186, 62/868,911, 62/870,533, 62/873,891, 62/874,418
- [0007]** 15/797,821 is a continuation in-part of 14/947,718, now Pat. 10,622,498.
- 20 **[0008]** 14/947,718 is a continuation of Int'l Pat. Appln. PCT/US14/39208.
- [0009]** PCT/US14/39208 claim priority to:
- [0010]** U.S. Prov. Ser. No. 61/826,446 filed May 22, 2013;
- [0011]** U.S. Prov. Ser. No. 61/834,873 filed June 13, 2013;
- [0012]** U.S. Prov. Ser. No. 61/843,021 filed July 4, 2013; and
- 25 **[0013]** U.S. Prov. Ser. No. 61/905,109 filed November 15, 2013.
- [0014]** 17/974,325 is a continuation in-part of said 17/182,954.
- [0015]** The chain of parents and siblings of this patent application includes U.S., International, and provisional patent applications that are in addition to those listed above but are identified in the ADS filed concurrently herewith.
- 30 **[0016]** This patent application incorporates by reference the subject matter of each of the patent applications listed above as well as of each of the additional U.S., International, and provisional patent applications listed in the concurrently filed ADS.

[0017] The above-referenced provisional patent applications are collectively referenced herein as “the commonly assigned incorporated applications.”

5

FIELD

[0018] The present invention generally relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.

10

BACKGROUND

[0019] Fiber-optic communication is widely used in applications such as telecommunications and communication within large data centers. Because of attenuation losses associated with using shorter optical wavelengths most fiber-optic communication uses optical wavelengths of 800 nm and longer. Commonly used transmission windows exist between 1260 nm and 1675 nm. A main component of optical receivers used in fiber-optic communication system is the photo detector, usually in the form of a photodiode (PD) or avalanche photodiode (APD).

[0020] High-quality low-noise APDs can be made from silicon. However, while silicon will absorb light in the visible and near infrared range, it becomes more transparent at longer optical wavelengths. Silicon PDs and APDs can be made for optical wavelengths of 800 nm and longer by increasing the thickness of the absorption “I” region of the device. FIG. 2 is a cross section of a conventional PIN photodiode 200, where “d” is the length of the absorption “I” region 220. FIGs. 3A and 3B show bandwidth and quantum efficiency a conventional silicon photodiode with a 30-micron diameter at 850 nm optical wavelength. As can be seen, in order to obtain a quantum efficiency of 90% the thickness “d” of the “I” region is over 30 microns. This leads to a maximum bandwidth of less than 2.5 Gb/s, which is too low for many current and future telecom and data center applications.

[0021] To avoid the inherent problem that silicon PDs and APDs have with longer wavelengths and higher bandwidths, other materials are used. Germanium (Ge) detects infrared out to a wavelength of 1700 nm, but has relatively high multiplication noise. InGaAs can detect out to longer than 1600 nm, and has less

multiplication noise than Ge but still has far greater noise than silicon. InGaAs is known to be used as the absorption region of a heterostructure diode, most typically involving InP as a substrate and as a multiplication layer. This material system is compatible with an absorption window of roughly 900 to 1700 nm.

5 However both InGaAs and Ge devices are relatively expensive and have relatively high multiplication noise when compared with silicon.

[0022] The subject matter claimed herein is not limited to embodiments that solve any specific disadvantages or that operate only in environments such as those described above. Rather, this background is only provided to illustrate one
10 exemplary technology area where some embodiments described herein may be practiced.

SUMMARY

[0023] According to some embodiments, a photodetector with microstructure-
15 enhanced photoabsorption is described. The photodetector (e.g. photodiode or avalanche photodiode) includes: a cathode region; an anode region; reverse biasing circuitry configured to apply a voltage between the cathode and anode regions such that the cathode region is driven to a more positive voltage than the anode region; and a microstructure-enhanced photon absorbing semiconductor
20 region configured to absorb photons from a source signal. The absorbing region includes a plurality of microstructures that are dimensioned and positioned to increase absorption of photons at a range of wavelengths that includes a wavelength of the source signal. According to some embodiments the microstructures have at least one dimension that is equal to or shorter than a
25 longest signal wavelength. According to some embodiments the microstructures are pillars, holes and/or voids. The microstructures can be arranged into a periodically-spaced array, a non-periodically-spaced array, a randomly-spaced array or a multiperiodically-spaced array. According to some embodiments the microstructures have a major longitudinal axis that is normal to the upper surface of
30 the underlying substrate material. According to some other embodiments, the microstructures have major longitudinal axes that are not parallel to one another. According to some embodiments, the microstructures are oriented so as to reduce sensitivity to any single direction of the source signal.

[0024] According to some embodiments, the microstructures increase absorption at least in part by forming an absorbing mode high contrast grating that makes use of resonance effects, scattering effects, near field effects, sub-wavelength effects, and/or interference effects.

5 **[0025]** According to some embodiments, the absorbing region and the microstructures are formed of silicon. According to some embodiments, a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 5 gigabits per second, at wavelengths of 850 nanometers with a quantum efficiency of at least 60%. According to some embodiments, a silicon
10 photodiode is provided that can detect source signals at a data bandwidth of greater than 10 gigabits per second, at signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%. According to some embodiments a silicon avalanche photodiode is provided that can detect source signals at a data bandwidth of greater than 5 gigabits per second, at wavelengths of 850
15 nanometers, while having a gain of greater than 2. According to some embodiments a silicon APD has a multiplication region with microstructures that extend into the P multiplication layer, N multiplication layer and/or charge layer. According to some embodiments a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 1 gigabit per second, at
20 wavelengths of 980 nanometers with a quantum efficiency of at least 40%. According to some embodiments a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 0.5 gigabits per second, at wavelengths of 1000 nanometers with a quantum efficiency of at least 30%. According to some embodiments, the microstructures effectively reduce
25 capacitance of the photodetector when compared to a microstructure-free device having a similar photon absorbing length.

[0026] According to some embodiments, the absorbing semiconductor region and the microstructures are formed of silicon and germanium. According to some embodiments, the microstructures are formed by etching away portions of silicon
30 and using a selective area growth process to grow germanium in the etched away portions. According to some embodiments, the absorbing semiconductor region and the microstructures are formed of germanium. According to some embodiments, the photo detector is configured to receive the source signal from

the substrate-side. The anode region can include a germanium P layer formed by an epitaxial lateral overgrowth process. The device can be configured such that the source signal to passes through the absorbing region a first time, reflects from a surface and thereafter passes through the absorbing region a second time. The
5 device can also be configured to receive the source signal the top-side and the anode region can be made of a silicon P layer. According to some embodiments, a avalanche photodiode is provided that detects source signals at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 1750 nanometers or shorter, and having a gain of greater than 2. According to some
10 embodiments, the absorbing semiconductor region and the microstructures are formed of III-V family material(s) such as InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, AlGaAs, AlGaN, GaP, InSb or InAs.

[0027] According to some embodiments, the microstructures include voids buried within the absorbing semiconductor region. According to some
15 embodiments, voids are buried in a layer of material so as to effectively lower the refractive index at the signal wavelength(s) and as well as lower the capacitance of the layer of material.

[0028] According to some embodiments, a photovoltaic device is described that includes a semiconductor material having a plurality of voids buried therein. The
20 semiconductor material being configured to convert solar radiation into direct current electricity. According to some embodiments, the voids are microstructured voids and are configured to enhance absorption of the semiconductor material thereby increasing conversion efficiency of the device. According to some embodiments, the voids are sized and/or spaced apart by less than 3 microns, and
25 are configured to alter an effective refractive index of the semiconductor material near a surface, for example to reduce reflection of incident sunlight from the device and/or increase internal reflections within the semiconductor material.

[0029] According to some embodiments a glass material is described in which the glass has a plurality of buried voids dimensioned between 0.01 microns to
30 1000 microns. In some examples the glass forms a part of a photovoltaic device. According to some embodiments, the buried voids are filled with a material gel, polymer and gas. The buried voids can provide flexibility of the glass material,

and/or increased resistance of the glass material to physical damage and/or damage propagation.

[0030] According to some embodiments, a microwave transmission line structure is described that includes: a semiconductor substrate material having a plurality of high-density dielectric-filled voids configured to reduce a dielectric constant of the semiconductor substrate material; and a plurality of metallic microwave transmission lines, least one of which is positioned above the semiconductor substrate material. According to some embodiments, the dielectric-filled voids are filled a material such as: nitrogen, argon, vacuum, air, helium, polymer, metal oxides, silicon dioxide, silicon nitride, calcium fluoride, or zinc oxide. According to some embodiments, the voids are further configured to reduce dispersion and reduce loss associated with the microwave transmission lines at least in part by reducing current loop flow and/or eddy currents.

[0031] According to some embodiments, an optical waveguide structure is described that includes: an optical mode region; and a supporting semiconductor material adjacent to the optical mode region. The supporting material includes a plurality of microstructured voids that are configured to alter an effective index of refraction of the supporting material based on the size, shape, density, etc. of the microstructured voids.

[0032] According to some embodiments, a heat exchanger system is described that includes: a heat generating device; a heat sink configured to dissipate heat to a surrounding medium; and an intermediate material mounted between the heat generating device and the heat sink. The intermediate material includes a plurality of buried voids configured to effect thermal conductivity of the intermediate material. According to some embodiments, some of the buried voids are filled with thermally conductive material and others are filled with a thermally isolating material. The two types of voids being positioned to conduct heat from the heat generating device to the heat sink and to reduce thermal cross talk with other heat sensitive devices mounted on the intermediate material.

30

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] To further clarify the above and other advantages and features of the subject matter of this patent specification, specific examples of embodiments

thereof are illustrated in the appended drawings. It should be appreciated that these drawings depict only illustrative embodiments and are therefore not to be considered limiting of the scope of this patent specification or the appended claims. The subject matter hereof will be described and explained with additional specificity

5 and detail through the use of the accompanying drawings in which:

[0034] FIG. 1 is schematic side cross section of three dimensional micro structures that enhance bulk absorption coefficient in photo sensitive devices, according to some embodiments;

[0035] FIG. 2 is a cross section diagram showing aspects of a typical structure
10 of a conventional PIN photodiode;

[0036] FIGs. 3A and 3B are plots showing bandwidth and quantum efficiency (QE), respectively, of a bulk conventional silicon photodiode versus "d" in microns;

[0037] FIGs. 4A-4D are graphs showing the enhancement of bulk absorption coefficient vs bandwidth and QE for a microstructured Si photodetector, according
15 to some embodiments;

[0038] FIGs. 5A and 5B are cross sections showing aspects of a top illuminated microstructured PIN silicon photodiode, according to some embodiments;

[0039] FIGs. 6A and 6B are cross sections showing aspects of a bottom
20 illuminated microstructured NIP silicon photodiode, according to some embodiments;

[0040] FIGs. 7A and 7B are cross sections showing aspects of a microstructured avalanche photodiode, according to some embodiments;

[0041] FIG. 8 is a cross section showing a silicon epitaxial structure for a high-
25 speed high-efficiency microstructured APD, according to some embodiments;

[0042] FIGs. 9A-9E are a series of cross sections showing some basic microstructure processing steps, for a high-speed APD, according to some embodiments;

[0043] FIGs. 10A-10B are cross sections showing aspects of a top illuminated
30 microstructured photo diodes, avalanche photo diodes and/or photovoltaics (PV) with microstructured voids in N-Si, according to some embodiments;

[0044] FIGs. 11A and 11B are cross sections showing aspects of an heteroepitaxial APD structure of Ge on Si, according to some embodiments;

[0045] FIG. 12 is a cross section illustrating aspects of a passivation method for Ge surfaces on microstructures, according to some embodiments;

[0046] FIGs. 13A and 13B are graphs showing the effects of microstructure enhancement of Ge bulk absorption coefficient for photodiodes and/or avalanche
5 photodiodes based on Ge on Si, according to some embodiments;

[0047] FIGs. 14A-14B are cross sections showing aspects of a top-illuminated Ge on Si avalanche photodiode having microstructured pillars/holes, according to some embodiments;

[0048] FIGs. 15A-15D are cross sections illustrating aspects of bottom-
10 illuminated Ge on Si avalanche photodiodes having microstructured pillars/holes, according to some embodiments;

[0049] FIGs. 16A and 16B are graphs comparing single pass and double pass photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments;

15 **[0050]** FIGs. 17A-17B are cross sections showing aspects of a top-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 700 to 1800 nm, according to some embodiments;

[0051] FIGs. 18A-18B are cross sections showing aspects of a bottom-
20 illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 1200 to 1800 nm, according to some embodiments;

[0052] FIGs. 19A-19C are diagrams illustrating how microstructures can reduce capacitance of a photodiode such that a larger area photo diode can be fabricated
25 with the same bandwidth and QE, according to some embodiments;

[0053] FIGs. 19D-19E are cross sections showing aspects of fabricating an APD device having a III-V absorbing layer grown on a P-I-N silicon multiplication layer, according to some embodiments;

[0054] FIG. 20 shows bulk layers without a final P-Si layer for devices having
30 microstructured Ge buried or embedded in an Si microstructure, according to some embodiments;

[0055] FIG. 21 is a cross section showing etching of microstructured pillars and/or holes for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments;

[0056] FIG. 22 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after the Ge "I" layer is grown in the etched region and planarized, according to some embodiments;

[0057] FIG. 23 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after I-Ge regrowth and planarization, and a cap layer of P-Si, according to some embodiments;

[0058] FIGs. 24A - 24B are cross sections showing aspects of a microstructured APD with buried/embedded I-Ge absorbing microstructures in I-Si microstructures, according to some embodiments;

[0059] FIGs. 25A - 25C are cross sections showing aspects of a photodiode having buried/embedded Ge microstructures in a Si microstructured pillar and/or hole array, according to some embodiments;

[0060] FIGs. 25D - 25E are cross sections showing aspects of a forward biased device such as a vertical cavity surface emitting laser (VCSEL), according to some embodiments;

[0061] FIG. 26 is a cross section showing starting epitaxial layers in which microstructured voids are fabricated, according to some embodiments;

[0062] FIG. 27 is a cross section showing microstructured holes/pillars etched into the I-Si layer, according to some embodiments;

[0063] FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping P⁺ anode layer 2826, according to some embodiments;

[0064] FIG. 29 is a cross section showing Bragg reflectors formed on the P-Si surface to provide a highly reflective mirror, according to some embodiments;

[0065] FIG. 30 shows an example of a PIN PD/PV structure with microstructured voids to enhance absorption, reduce bulk refractive index, reduce capacitance and increase mechanical flexibility of large sheets of PV on semiconductor material, according to some embodiments;

[0066] Fig. 31 is a cross section showing regrown I-Ge with a buried/embedded voids, according to some embodiments;

[0067] Fig. 32 is a cross section showing a device having buried microstructured voids in I-Si with regrown I-Ge and capped by an epitaxial layer, according to some embodiments;

[0068] FIG. 33 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some embodiments;

[0069] FIG. 34 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some other embodiments;

[0070] Fig. 35 shows the basic epitaxial structure for a conventional Si PV/PD diode on N Si substrate;

[0071] FIG. 36 shows microstructured voids incorporated into an N-Si layer, according to some embodiments;

[0072] FIG. 37 is a cross section showing etched Si microstructured pillars/holes with regrown Ge covering the Si, according to some embodiments;

[0073] FIG. 38 is a cross section showing microstructured Si pillars/holes with Ge regrowth on an N-Si layer having embedded microstructured voids, according to some embodiments;

[0074] FIG. 39 is a cross section showing partial coverage I-Ge on microstructured Si pillars/holes, according to some embodiments;

[0075] FIG. 40 is a cross section showing the basic components for the a microstructured Si-Ge pillar hole array PD/PV and/or APD, according to some embodiments;

[0076] FIGs. 41A-41B are cross sections showing aspects of a microstructured pillar/hole array device above a N-Si layer having buried microstructured voids, according to some embodiments;

[0077] FIGs. 42A-42D are cross sections showing aspects of an APD with microstructured pillar/hole arrays above an N-Si layer having buried microstructured voids, according to some embodiments;

[0078] FIGs. 43-46 are top views illustrating various dimensions, spacings and shapes for microstructured elements, according to some embodiments;

[0079] FIGs. 47-48 are cross sections showing microstructured pillar and hole arrays having varying lengths and depths, according to some embodiments;

[0080] FIG. 49 shows a microstructured surface having a combination of both pillars and holes, according to some embodiments;

[0081] FIG. 50 is a cross section of an optical ridge waveguide, according to some embodiments;

[0082] FIG. 51 is a cross section of a buried optical waveguide in silicon using voids, according to some embodiments;

5 **[0083]** FIGs. 52 and 53 are a cross section and top view, respectively, of a ridge waveguide integrated with a microstructured PD/APD, according to some embodiments;

[0084] FIGs. 54A and 54B show a microwave transmission line on Si with voids, according to some embodiments;

10 **[0085]** FIG. 55 is a cross section of voids for thermal conduction and thermal isolation of heat producing ICs and light emitters, according to some embodiments; and

[0086] FIG. 56 is a cross section showing a distribution of voids to increase lateral path length for increasing lateral electrical resistivity and decrease lateral

15 thermal conduction, according to some embodiments;

[0087] FIGs. 57A and 57B are simplified partial schematic top views of a semiconductor surface having holes configured as trenches, according to some embodiments.

20

DETAILED DESCRIPTION

[0088] A detailed description of examples of preferred embodiments is provided below. While several embodiments are described, it should be understood that the new subject matter described in this patent specification is not
25 limited to any one embodiment or combination of embodiments described herein, but instead encompasses numerous alternatives, modifications, and equivalents. In addition, while numerous specific details are set forth in the following description in order to provide a thorough understanding, some embodiments can be practiced without some or all of these details. Moreover, for the purpose of clarity, certain
30 technical material that is known in the related art has not been described in detail in order to avoid unnecessarily obscuring the new subject matter described herein. It should be clear that individual features of one or several of the specific embodiments described herein can be used in combination with features or other

described embodiments. Further, like reference numbers and designations in the various drawings indicate like elements.

[0089] According to some embodiments, microstructures are used to enhance the bulk absorption constant (also referred to as absorption coefficient) to achieve high quantum efficiency (QE) while maintaining an absorption length suitable for high data rate applications. As used herein, "QE" refers to internal quantum efficiency (IQE). IQE is equal to external quantum efficiency (EQE) in cases where reflection and transmission are negligible.

[0090] According to some embodiments, microstructures are used to improve bulk absorption constant at wavelengths in the proximity of the semiconductor material's band gap. This allows for extending the operating optical wavelengths and/or operating spectrum of the photosensor. The enhanced bulk absorption constant (or coefficient) is called the effective absorption constant (or coefficient). The term "effective" is used since absorption constant or coefficient is an inherent material property. However, with resonance effects, plasmonic effects, field enhancement effects, scattering effects, near field and sub wavelength effects, the effective absorption constant or coefficient can be greater than the bulk or material absorption constant or coefficient. As used herein, the following terms are used interchangeably: enhanced absorption constant, enhanced absorption coefficient; enhanced effective absorption constant; enhanced effective absorption coefficient; enhanced absorption; enhanced effective absorption; and effective absorption constant; and effective absorption coefficient.

[0091] According to some embodiments, enhanced absorption can also have drastic effects on path length. In one bulk absorption example, the path length for the photons to be absorbed to 1/e of its original amplitude is, for example 100 micrometers (μm), whereas under enhanced absorption according to some embodiments, the path length is 1 micrometer for the optical amplitude to decay to 1/e of its original amplitude. Equivalently, if path length is kept constant to one micrometer then the enhanced absorption coefficient is 100 times greater than the bulk absorption coefficient.

[0092] This is seen by the relationship $A = A_0 e^{-\alpha L}$ where A is the decaying amplitude of the incident photon flux A_0 and α is the absorption coefficient and L the path length for absorption to take place. So, rather than have L be 100 times

longer, an effective α can be defined such that it is 100 times greater than a non enhanced absorption coefficient such as the bulk absorption coefficient. The resonance/scattering/near field effects of microstructures for example gives the equivalence of the path length that is 100 times longer where the

5 resonant/scattering/near field microstructure is just one micron long. To put it another way, in a very simplistic view, the photons in the resonant structures make 50 round trips before reaching the $1/e$ value of its original amplitude, so the equivalent linear length is 100 times the length of the resonant structure. For simplicity, resonance/scattering/near field effects will collectively be referred to
10 herein as "resonant" which can include, resonant, scattering, near field, plasmonic, nonlinear and linear optical effects.

[0093] As used herein the terms "microstructures" and "microstructured" refer to: pillars, voids, holes and mesas, of various shapes and sizes having at least one dimension in the micrometer scale, submicrometer scale, and/or sub-wavelength
15 scale.

[0094] According to some embodiments, properties of the microstructures can also be explained as the absorption mode of high contrast grating (HCG) being used to enhance the effective absorption constant/coefficient or enhanced absorption. Conventionally, HCG uses material that is transparent at the optical
20 wavelength of interest. In contrast, according to some embodiments, at least one of the microstructures is absorbing or weakly absorbing at the optical wavelength of interest. According to some embodiments a low-Q absorbing mode HCG enhances absorption (e.g. Q values in the range of 2-200).

[0095] According to some embodiments, a low index material is used such as
25 buried oxide (BOX), silicon on insulator (SOI), silicon on sapphire (SOS), low-density semiconductors such as amorphous semiconductor, nanowire semiconductors, voids and holes to lower the effective refractive index. Refractive index is an inherent property of a material. However, according to some embodiments, when structures such as voids, air gaps, and/or holes (which can be
30 filled with low index material, and/or regrowth) have dimensions on the order of the optical wavelength, the optical electromagnetic field will see an average refractive index consisting of the material refractive index and the structures (which can be filled by a low refractive index material). This average is referred to herein as the

effective refractive index. According to some embodiments, a low index or effective low index material need not be used in the microstructures.

[0096] According to some embodiments, the techniques for enhancing effective absorption can be applied to various materials including: silicon, germanium, III-V material such as InP, GaAs, GaN, InGaAs, and any combination of the III-V material family. As used herein, the term "material family" of a III-V material is defined as any material that is lattice matched or approximately lattice matched (within a few percent) to GaAs, InP, GaN, InSb semiconductors. For example, the InP material family can include InGaAs, InGaAsP, InAlAs. According to some embodiments, in the case of microstructures, regrowth such as selective area growth (SAG) of Ge, InGaAs, or other III-V material in silicon microstructures can be carried out without the detrimental effects of lattice mismatch since the dimension of the footprint of the lattice mismatched material on silicon is small (approximately a few micrometers to sub-micrometers). This allows Ge and other III-V materials to be integrated with silicon without the use of a conventional buffer layer (such as amorphous Ge in the case of Ge on Si growth). The heterogeneous integration of materials can be homo or hetero structures, combination of crystalline and microcrystalline and amorphous semiconductor, conductor such as carbon, graphene, insulator, dielectrics, solid, gaseous, liquid such as glass or polymer that can be semiconducting.

[0097] Due to the microstructures, the capacitance can also be represented by an effective capacitance which is a parallel capacitance of (1) the dielectric constant of one semiconductor, and (2) the dielectric constant of another material, which can be a semiconductor, dielectric, gas, vacuum, partial vacuum, liquid such as glass or polymer (polyimide, mylar, or other organic compound). The effective capacitance of the device is the combination of the capacitance of the parallel capacitors, which can be two or more. An advantage of the use of microstructure according to some embodiments, is that the effective capacitance can be significantly lower than the capacitance of a homogeneous material such as a semiconductor. The lower capacitance allows a device to have a larger area while still maintaining suitably high data rate bandwidth, and/or increase the data rate bandwidth by reducing the thickness of the device to reduce the transit time.

[0098] According to some embodiments, the photosensor can be a photodiode (PD), avalanche photodiode (APD), photovoltaic (PV) or solar cell, or any optoelectronic device that converts photons to electrons. According to some embodiments, emitters such as lasers and light emitting diodes that convert
5 electrons/holes to photons can also be implemented using microstructures.

[0099] According to some embodiments, the enhanced absorption allows the APD/PD to: (1) extend the sensitivity of the APD/PD to photons with energies (or wavelength) closer to the material band gap with QE greater than 60% and data
10 Gb/s), due to shorter absorption length therefore shorter transit time; (3) increase quantum efficiency with enhanced absorption; (4) be manufactured of silicon which has superior APD properties with low excess noise; (5) be compatible with Si Photonics and CMOS processes. According to some embodiments, the PD/APD can be integrated with ASIC (application specific integrated circuits) such as signal
15 processing, signal amplification, memory, cpu, electrical transmitter, optical waveguides, integrated optics, and other ICs for specific applications. This is advantageous for mass production using CMOS foundries.

[00100] According to some embodiments, microstructures such as voids are used to reduce effective refractive index to create resonant structures to enhance
20 the absorption. In microstructures where selective area growth are used to integrate Ge or III-V material with silicon, voids can be made in the silicon microstructure such that the absorbing region is a resonant structure to enhance the effective absorption coefficient by 2 to over 100 times.

[00101] According to some embodiments, silicon is used for avalanche gain.
25 Silicon has the lowest excess noise for an avalanche photodiode. By integrating Ge and/or III-V material with silicon, the absorption takes place in Ge and/or III-V material and the electronic gain occurs in silicon. Depending on the optical wavelengths, for example shorter than 1100 nm, silicon may be used for both absorption and electronic gain with the use of microstructures.

30 **[00102]** According to some embodiments, microstructures such as buried voids can reduce lateral electrical and thermal conductivity. In situations where directional conductivity of electrical or thermal (phonons) is preferred, voids can be used to confine the flow of electrical current and/or heat.

[00103] According to some embodiments, the absorption of photons in semiconductors is enhanced with the use of microstructures. The microstructures can have effects such as resonance, field enhancement, near field and sub wavelength effects, scattering, plasmonics, photonic crystal, absorption mode in
5 high contrast grating at the near field regime, which are both linear and non linear effects that can effectively increase the effective absorption length resulting in a greater absorption of the photons for a given length.

[00104] According to some embodiments, microstructures used for absorption enhancement for silicon photodiodes and silicon avalanche photodiodes can result
10 in silicon PD and APD with bandwidths in excess of 10 Gb/s (or equivalently 6.75 GHz approximately depending of the digital coding format) at photons with wavelengths of 850 nm approximately (which is the current datacom preferred wavelength) with quantum efficiencies of approximately 90% or more.

[00105] Silicon optical detectors are very robust due to the maturity of the
15 material and processing techniques, the surfaces can be easily passivated to eliminate dangling bonds that can cause surface states and carrier recombination centers, they have excellent carrier lifetimes due to low defects and high material purity, and for APD applications, the noise is low due to the small ionization ratio between holes and electrons (k factor, silicon have the lowest k factor than any III-
20 V material) and such detectors are CMOS compatible for integration with electronics for signal processing and with Si photonics.

[00106] According to some embodiments, other material such as germanium, III-V, a-Si (amorphous silicon) may also be used singly or together with other materials such that a multiple bandgap in parallel can be fabricated with enhanced
25 absorption.

[00107] According to some embodiments, microstructures and voids are used to reduce the effective refractive index and capacitance to achieve the absorption mode high contrast grating effect and to reduce the effective capacitance of the device for lower RC time constants.

30 **[00108]** In addition, according to some embodiments, microstructures buried in the semiconductor can reduce lateral electrical and thermal conduction. Microwave transmission lines are possible for example where high-density voids are buried in Si to reduce the dielectric constant and also eddy currents in the semiconductor

resulting in low loss and dispersion. Voids can also be used for thermal isolation and to improve thermal conductivity by filling the voids with thermal conductors. This is useful in thermal management of components on a silicon substrate.

[00109] The enhancement using nanowires (Garnett et al, Light trapping in
5 silicon nanowire solar cells, Nano Letters, 2010, 10, 1082-1087; Kelzenberg et al, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, Nature Materials, vol. 9, March 2010, 239-244) and nanoholes (Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Proceeding of SPIE, Vol. 7772, 77721G-1, 2010) have
10 been reported. Nanowire is known to be used for light trapping in photovoltaic applications where the photogenerated carriers diffuse to the anode or cathode of a P-N junction with zero external bias operating at DC (direct current).

[00110] According to some embodiments, the photogenerated carriers are swept out with an external reverse bias in the absorbing "i" region of a P-I-N diode (PD) or
15 P-I-P-I-N diode (APD) for high modulation bandwidth (greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain, with gain greater than 3 dB.

[00111] The cause or causes of the enhancement of the absorption coefficient are believed to include one or more of the following: an increase in optical field
20 concentration, resonance effects, constructive and destructive optical interferences (amplitude and phase) effects, scattering, and high contrast grating (HCG) effects. See, e.g. Chang-Hasnain et al, High contrast gratings for integrated optoelectronics, Advances in Optics and Photonics 4, 379-440 (2012), hereinafter "Chang-Hasnain." The HCG effects are at the near-wavelength regime (See,
25 Chang-Hasnain) where the optical wavelength in the material of the grating and the optical wavelength in the surrounding material of the grating is the range of the period of the grating.

[00112] FIG. 1 is schematic side cross section of three dimensional micro structures that enhance bulk absorption coefficient in photo sensitive devices,
30 according to some embodiments. Microstructured pillars 110 and/or holes 120 are etched into the "I" Si layer 100. The optical wavelength in material M_1 is λ/n_1 where n_1 is the refractive index of M_1 and the optical wavelength in material M_2 is given by λ/n_2 where n_2 is the refractive index of material M_2 . The center to center distance L

of the structures 110 can be between λ/n_1 and λ/n_2 or approximately 100-2000 nm, which is referred to as the near-wavelength regime. The diffraction regime is where L (one cycle) is greater than the wavelength, while the subwavelength regime is where L is less than the wavelength. The cross section of FIG. 1 shows the 3D (dimension) microstructured pillar/hole array, which enhances the bulk film absorption coefficient by factors of 1.5 to over 100. The period of the 3D pillar/hole microstructured array can be seen as a 3D high contrast grating, whose period of the grating Λ can lie between λ/n_1 where n_1 is the optical refractive index of material M_1 and λ/n_2 where n_2 is the optical refractive index of material M_2 . If $n_1 > n_2$ then $\lambda/n_1 < \Lambda < \lambda/n_2$ where λ is the optical wavelength of the light to be absorbed by the microstructured pillar/hole array typically in the "I" region of a P-I-N PD or for APD, the absorbing "I" region P-I-P-I-N where the second "I" region is the multiplication region, or the wavelength of the optical signal to be detected by the PD and APD. At this near-wavelength regime of the 3D HCG microstructured pillar/hole array, the resonance Q (quality factor, or proportional to the ratio of the energy stored in the resonator/energy losses per cycle; where it is the optical cycle, the optical frequency impinging on the resonator or in the resonator) can be as high as 10^7 (see, Chang-Hasnain) if the HCG has minimal absorption loss as is known. In addition, in most cases the ratio of the index of the HCG to the surrounding material index need only be approximately 1.1 to observe the effects of the HCG.

[00113] The HCG effect that may explain the high enhancement of the absorption coefficient of the bulk material is that a single or multiple HCG layer (or a single microstructured pillar/hole array layer) due to its resonance effects and/or due to a varying of the microstructured pillar/hole period spacing, the optical signal resonating in the HCG/microstructured pillar-hole array can be directed to propagate in the plane of the HCG/microstructured pillar-hole array rather than normal to the surface. Together with resonance and in-plane propagation this can greatly increase the absorption path length in the HCG/microstructured pillar-hole array. According to some embodiments, the absorbing HCG mode is operated with a reverse voltage bias for PD/APD and a built-in bias (zero applied bias) in photovoltaic devices.

[00114] Using the phenomenon of near-wavelength and also deep-wavelength where the HCG period is much less than the optical wavelength, and the diffraction

regime where the HCG period is greater than the optical wavelength (See, Chang-Hasnain) the microstructured pillar-hole-void array can have enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100.

[00115] According to some embodiments, the HCG effect is also used in the
5 absorbing mode or lossy mode or low Q of 1-10000 (compared with known HCG that are in the non-absorbing mode or non-lossy mode to achieve high Q of greater than 1,000,000 and high reflectivity), in both buried/embedded (not fully buried) Ge microstructures in Si and buried/embedded void microstr Fig. 49: "Pillar with hole structures in either Ge or Si to improve the quantum efficiency (QE) and operating
10 wavelength range of Si (400-1100 nm) and Ge (400 to 1800 nm) and Ge on Si photodiodes and avalanche photodiodes operated in a reverse bias mode of the pn, pin, pinip junctions (p and n can be switched for certain device configurations) that can be homo or heterojunction, crystalline or amorphous or any combinations thereof. In addition, the substrate can be on SOI or BOX or voids to reduce the
15 index of refraction or effective index of refraction and the dielectric constant or effective dielectric constant (a dielectric with many voids can be represented as an effective dielectric constant, or equivalently effective capacitance).

[00116] Known silicon photodetectors have been limited to wavelength ranges of 200 to 1000 nm due to indirect bandgap of 1.1 eV. In particular, near the band gap
20 wavelengths of 800-1000 nm, the frequency response of the silicon photodetector to a modulated optical signal at Gb/s rate is limited to 1.5 Gb/s approximately or less due to the weak absorption constant of Si at those wavelengths which are approximately 760 cm^{-1} at 850 nm and 67 cm^{-1} and 63 cm^{-1} at 980 and 1000 nm respectively, resulting in long absorption lengths of material, 30 microns or more,
25 which results in low frequency response for the PD/APD. The wavelengths 850 nm is of interest since this is the standard wavelength for short distance (few meters to a few kilometers) multimode fiber optical datacommunication.

[00117] The amount of incident photons absorbed is approximately given by $\eta = 1 - e^{-\alpha L}$ where η (also the quantum efficiency if reflection off the surface of the PD
30 is negligible) is the amount absorbed and " α " is α the absorption constant and "L" is the length length of the absorber. Using this equation and the absorption constant of Si at 850 nm, 90% of the incident photons are absorbed at a depth of approximately 30 μm . Known high speed photodetectors typically have an

absorption region of approximately $2\text{ }\mu\text{m}$ in length. The reason for this is that transit time and RC time of the photodiode need to be considered to have a bandwidth of 20 GHz (or approximately 30 Gb/s) or more and still have an external quantum efficiency of 80-90% or better.

- 5 **[00118]** Efficiency and bandwidth (transit and RC time): At a field strength of $6 \times 10^4\text{ V/cm}$ the electron drift velocity is $1 \times 10^7\text{ cm/s}$ at a temperature of 300 K. The 3 dB bandwidth of the photodetector due to transit time is given by:
 $f(3\text{dB}) = 0.45/t(\text{transit})$ where $t(\text{transit})$ is the transit time for the carriers to cross the depleted high field region. FIG. 2 is a cross section diagram showing aspects of a
10 typical structure of a PIN photodiode structure. Assuming negligible photocarriers generated in the P region 210 of the PIN 200 and mostly generated in the "i" region 220, the transit time is determined by the electron drift velocity and "d" (the high field "i" region). The PIN 200 is reversed biased (e.g. between -4 and -25 V). The "i" region 220 is fully depleted in this case. The RC time of the PIN structure 200 is
15 determined by the capacitance, which is the ratio of the area ($\pi w^2/4$) of the PIN 220 to d.

- [00119]** According to conventional techniques, a $30\text{ }\mu\text{m}$ thick absorption layer ("i") to achieve 90% absorption for Si at 850 nm wavelength will give a transit time limited 3dB bandwidth of 1.5 GHz (approximately 2.2 Gb/s) which is too low for
20 many current applications. Many current applications are in the 10-20 Gb/s range and in the near future 40 Gb/s. A d of $2\text{ }\mu\text{m}$ or less is desirable for current high-speed photodiodes in optical datacom applications to give over 30 Gb/s bandwidth.

- [00120]** RC time is another time to consider in photodiodes (applies to both APD and PD). The 3 dB bandwidth due to RC time is given by $f(\text{RC}) = 1/(2\pi\text{RC})$; where
25 C is the capacitance of the photodiode and R is the load resistance which is typically 50 ohms (and occasionally 25 ohms). Capacitance in the case of a conventional PIN structure photodiode with the "i" region fully depleted by the reverse bias, is just a parallel plate capacitance given by $\epsilon A/d$ where ϵ is the dielectric constant of the material (multiplied by vacuum permittivity of 8.854×10^{-14}
30 farads/cm) which is 11.9 for Si, A is the area of the capacitor ($\pi(w/2)^2$), and d is the depleted "i" (i and l are used herein interchangeably). The $f(\text{RC})$ becomes larger as d increases since the capacitance is decreasing with increasing d and a fixed area, where the diode diameter for example is $30\text{ }\mu\text{m}$ (diameters of high frequency

PD/APD range from 5 to 60 μm). Diameter of diode for calculating the RC time is the total capacitive area of the diode that includes the photosensitive area and any metallization that may contribute to the overall capacitance.

[00121] The overall frequency bandwidth of the photodiode is a sum of the squares of the transit time and the RC time. This is given by the equation:

$$f = 1 / (2\pi(RC)^2 + (\tau/2.4)^2)^{1/2}.$$

[00122] FIGs. 3A and 3B are plots showing bandwidth and QE, respectively, of a bulk conventional Silicon photodiode versus “d” in microns. From plots 310 and 312 in FIGs. 3A and 3B, for the combined $f(3\text{dB})$ of the transit time and RC time and the quantum efficiency η (assuming negligible reflection losses) we see that for bulk silicon to reach 10 Gb/s, the quantum efficiency (QE) is less than 40%, for a 30 μm diameter PD, which is too low for most datacom applications.

[00123] According to some embodiments, to overcome the relatively weak absorption of semiconductors with radiation energies near the bandgap and indirect bandgap semiconductors, for example Si at 850-1100 nm, a microstructured array is used that is etched into silicon that is grown by conventional methods epitaxially such as chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE). Note that according to some embodiments, non semiconductors can be used: such as polymers, glass, ceramics, hybrid material such as transition metal oxides, hydrides, chlorides, sulfides embedded with semiconductor, metal, carbon nanoparticles and or atoms, which may or may not have a bandgap. The microstructured array of silicon consists of pillars of Si and/or holes in Si. See, Garnett and Yang, *Light Trapping in Silicon Nanowire Solar Cells*, *Nano Lett.* 2010, 10, 1082–1087 (hereinafter “Garnett et al.”) that experimentally demonstrates that an ordered array of silicon nanowires increased the optical path length of the incident optical radiation by 73 times greater than that of bulk silicon.

[00124] According to some embodiments, as described earlier, the concept of effective absorption coefficient is introduced. The effective absorption coefficient of the ordered array of Si nanowires is 73X that of bulk silicon; bulk α for Si is 760 /cm and nanowire Si α is 5.548×10^4 /cm at 850 nm which is higher than direct bandgap III-V material.

[00125] It should be noted that the microstructures can also be epitaxially grown using methods such as VLS (vapor liquid solid epitaxial grown) nanowires or microwires (some nanowires have the largest dimension, such as the diameter, in the micron range, so that it can be called a microwire) with or without catalysts, or
5 using a dielectric mask for selective area growth (SAG) epitaxy.

[00126] The nanowire array described in Garnett et al. has a diameter of the nanowire of approximately 390 nm using an array of beads of 530 nm as a dry etch mask. Roughly 1/2 of the Si material is etched away; the effective capacitance for the nanowire array is less than that of the bulk. The effective capacitance can be
10 estimated as two parallel capacitors, one with Si and another with polyimide (filler) whose dielectric constants are 11.9 and 3.4 respectively. The area of each capacitor will be 1/2 that of a 30 μm diameter parallel plate.

[00127] With the effective capacitance lower, the overall 3dB bandwidth for a 30 μm diameter device is significantly higher. FIGs. 4A-4D are graphs showing the
15 enhancement of bulk absorption coefficient vs bandwidth and QE for a microstructured Si photodetector, according to some embodiments. FIGs. 4A and 4B shows the bandwidth (plot 410) and quantum efficiency (plot 420) of a microstructured Si photodiode (PD) or avalanche photodiode (APD) at 850 nm wavelength photons impinging on the PD/APD either single or double pass. With
20 an effective absorption coefficient (EAC) of 73X (412), 30X (414) or 15X (416) over bulk absorption coefficient (BAC), the bandwidth and QE are 54 Gb/s, 98%; 49 Gb/s 90%, 28 Gb/s 90% respectively for a 30 micrometer diameter PD/APD for example. At 1100nm, shown in plots 430 and 440 of FIGs. 4C and 4D, with enhancement, for example, of 172X QE of 90% and bandwidths of 26 Gb/s can be
25 attained using Si microstructured PD/APD. Both PD and APD operate at a reverse bias of -2 to -50 volts range. APDs in general will have less bandwidth than PDs for the same geometry due to the added multiplication layer of the APD. In addition, APDs have a gain-bandwidth product. For simplicity, APD and PD are shown to be approximately the same.

30 **[00128]** According to some embodiments, a combination of low capacitance due to the gaps between the microstructured pillars and the enhanced absorption allows the silicon photodiode and avalanche photodiode to operate at bandwidths greater than 10 Gb/s with high quantum efficiencies (> 90%) at 850 nm

wavelength. This has not been demonstrated by conventional silicon PD/APD at these wavelengths. 850 nm is chosen as the nominal wavelength, but according to some embodiments, wavelengths can have values from 700 to 1100 nm.

- 5 [00129] According to some embodiments, the weak absorption in the bulk can be taken advantage of for photodetector applications since this will allow light at 850 nm and longer to pass through Si substrate and epitaxial layers toward the microstructured silicon with minimal optical loss and minimal photocurrent outside of the high field region, which can diffuse to the i-region and can cause the photodetector to have a degradation in frequency response.
- 10 [00130] According to some embodiments, the techniques described herein are applied to other semiconductors, polymers, organic films, glass, dielectrics, hybrid material such as glass, dielectrics, polymers embedded with nanoparticles of metal, semiconductors. According to some embodiments, one or more of the following are used: Ge, III-V material family such as InP, GaAs, GaN, InGaN; II-VI
- 15 material family such as ZnSe, and also heterostructure material such as III-V grown on Si, Ge grown on Si. For example, for Ge on Si, microstructures are fabricated on the Ge to increase absorption which allows a shorter length of Ge to be used resulting in higher speed due to lower effective capacitance and shorter transit time for the carriers.
- 20 [00131] FIGs. 5A and 5B are cross sections showing aspects of a top illuminated microstructured PIN silicon photodiode, according to some embodiments. FIG. 5A shows the starting basic material structure 500. In FIG. 5B, silicon epitaxial structure is shown for a high-speed high efficiency microstructured photodiode 520. The photodiode 520 in FIG. 5B is designed for top
- 25 illumination. According to some embodiments, BOX/SOI layer 504 may not be used. FIGs. 6A-B, *infra* show an example for bottom illumination. Note that with minor modifications the n and p doping can be switched and the direction of illumination may also be affected. According to some embodiments, the illumination can be either perpendicular to the surface of the PD/APD or at an
- 30 angle off perpendicular to the surface. According to some embodiments, in integrated structures where the optical signal is guided in an optical waveguide, the microstructured absorption region can also be illuminated edge wise, directly into the microstructures or evanescently coupled to the microstructured i region.

[00132] FIG. 5B shows a microstructured pillar and or hole PD 520 in silicon with the starting material 500 consisting of a P-I-N Si layer grown on an Si substrate 502 that can be N doped or low doped in which case an extra N⁺ layer is first grown on the substrate to minimize series resistance. The dimensions and doping of the layers can range as follows; N⁺ cathode contact layer 506 (or a thin layer on top of 506, between 506 and 508) with N doping of greater than $5 \cdot 10^{17}/\text{cm}^3$, and thickness ranging approximately from 0.1 to 10 micrometers or more; N layer 506 with N doping greater than $5 \cdot 10^{17}/\text{cm}^3$, and thickness ranging approximately from 0.1 to 10 micrometers or more; I high field absorption region 508 with background doping of less than $5 \times 10^{16}/\text{cm}^3$ and thickness ranging approximately from 0.1 to 5 micrometers depending on applications; and P⁺ anode layer 510 with P doping greater than $5 \cdot 10^{18}/\text{cm}^3$ and thickness ranging approximately from 0.1 to 5 micrometers or more. The PD (and APD) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area) is nominally 30 micrometers (10-80 micrometers in diameter are possible ranges) in diameter for 20 Gb/s or more bandwidth operation. According to some embodiments, the area can be larger for lower bandwidth or smaller for higher bandwidth operation. The Si microstructures of arrays of holes 522 and/or pillars 524 shown in FIG. 5B, which can be random, patterned or pseudo-random, are for enhancing the bulk absorption coefficient of Si to detect photons with wavelengths from 300-1100 nm. In the case of datacom applications, according to some embodiments, the optical signal wavelengths range from 750-1100 nm. A transparent conducting oxide and P-ohmic layer 526 is also provided.

[00133] The PD 520 is operated in a reverse bias mode, with negative voltage on the anode (P⁺ layer 510 via P-ohmic and bond contact metal 528) and positive voltage on the cathode (N⁺ layer 506 with N-ohmic bond contact metal 530) ranging from -1 to -20 volts. According to some embodiments, the PD structure 520 shown in Fig. 5B (and PD structure 620 in FIG. 6B, *infra*) can also be used for photovoltaic (PV) operation without any external bias.

[00134] As shown in FIG. 5B, the optical signal can impinge normal to the surface or at an angle off normal. In certain cases, optical signal coming in at an angle off normal can have a higher QE and can also be at a certain rotation about the axis normal to the surface. This is to avoid the bald spot effect where some

photons travelling normal to the surface can “see” bald spots whereas for photons illuminating at an angle off normal to the surface, the bald spots are hidden by other microstructures. This is not the case in near field optics where the spacing of the microstructures are of the order of the optical wavelength or subwavelength,

5 the bald spots are not a significant issue.

[00135] FIGs. 6A and 6B are cross sections showing aspects of a bottom illuminated microstructured NIP silicon photodiode, according to some embodiments. The optical signal impinges on the photodiode 620 from the substrate side or bottom. The substrate 602 can be thinned to 10 microns or less
10 by etching for example a via and stopping at the P layer or the photodiode can be fabricated on a BOX (buried oxide) or silicon on insulator (SOI) silicon wafer and the etch via can stop at the BOX layer 604 which can also be selectively etched to the silicon layer 606, the via 630 is as wide or wider as the photosensitive area of the photodiode 620. An antireflection layer (not shown) is applied to the silicon
15 remaining layer 606 or the BOX layer 604 (the BOX layer 604 can be designed as a part of the antireflection layer for example) to minimize reflection (the BOX layer 604 can also be selectively etched off such that antireflection layer can be applied to the silicon P layer 606 to minimize multiple reflections). The back illuminated photodiode 620 has the advantage that a reflector 626 can be applied on the N
20 layer 610 to reflect any light not absorbed on the first pass, in effect doubling the length of the “I” layer 608. The QE can be increased due to the extra length. In addition the reflector 626 on the N layer 610 can be smooth or textured to scatter (non-specular or diffused reflection) the light (optical signal) to optimize absorption by the microstructures (arrays of pillars 624 or holes 622). Since the length of the
25 “I” region is effectively doubled, the transit time can effectively be reduced since only half of “I” is needed.

[00136] Bottom illuminated PDs such as PD 620 in FIG. 6B are also sometimes referred to back/substrate illuminated PDs, and top illuminated PDs such as PD 520 in FIG. 5B are also sometimes referred to front/surface illuminated PDs.

30 **[00137]** According to some embodiments, the basic structure of a microstructured Si photodiode such as shown in FIGs. 5A, 5B, 6A and 6B, is fabricated from a bulk thin film epitaxially grown silicon with a P-I-N structure on a

silicon wafer which can be doped N type or not intentionally doped or low doped N type Si substrate with (100) orientation or other orientation such as (111).

[00138] According to some embodiments, the basic layer structures (such as layers 502, 504, 506, 508 and 510 of structure 500 of FIG. 5A, and layers 602, 604, 606, 608 and 610 in structure 600 of FIG. 6A) are all grown epitaxially using one or more of the following methods: chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), plasma enhanced chemical vapor deposition (PECVD), molecular beam epitaxy (MBE), atomic layer deposition (ALD), pulsed laser deposition (PLD) on Si substrate of either P or N or low doped or undoped) or BOX/SOI substrates.

[00139] Processing details have been left out for simplicity. According to some embodiments the following basic steps are carried out: first (for pillars, not necessary for holes), depositing the p ohmic contact metal layer using e-beam, thermal or sputtering deposition; second, photolithographically (or imprint lithography) defining the microstructure pattern either pillars or holes and forming the etch mask for either dry or wet etching; third, etching of microstructure patterns on the P and I layers partially or fully and can extend into the N layer; fourth, passivating the sidewalls of the microstructure patterns (pillars or holes) with thermal oxide to minimize surface recombination of the photogenerated carriers via surface states due to dangling bonds and other surface imperfections (other passivation techniques may also be applied such as ALD (atomic layer deposition) of Si oxides and Si nitrides); fifth, planarization (filler step) using either spin on glass, polyimide, or plasma enhanced chemical vapor deposition (PECVD) of dielectrics such as Si oxides and Si nitrides; sixth, etch back to expose the P layer or P ohmic metal layer (polyimide or spin-on glass may partially fill the holes or space between the pillars/microstructures); and seventh, ohmic and/or bond contacts formed on the P and N layers. In the case of top illuminated photodetectors, where the optical signal enters on the epitaxial surface where the microstructure patterns are fabricated, a transparent conducting oxide is deposited to connect all the P ohmic metal layers (for pillars). In the case where the microstructures are holes or voids the transparent conducting oxide layer is not used, according to some embodiments. A voltage bias is applied between the P layer (anode) and the N layer (cathode) of -1 to -20 V, and the photodiode is

operated in a reverse bias mode to deplete as much as possible the "I" layer, preferably the entire I layer.

[00140] FIGs. 7A and 7B are cross sections showing aspects of a microstructured avalanche photodiode, according to some embodiments. As in the Si microstructured photodiodes shown in FIGs. 5A, 5B, 6A and 6B, the epitaxial layers 700 for the APD 720 are grown first followed by microstructure processing. The microstructured avalanche photodiode 720 can be illuminated (e.g. with 300-1100 nm) from the top with transparent metal oxide P ohmic contact 726, or the P ohmic contact 726 can be a mirror to reflect the photons illuminating from the bottom (e.g. with 950-1100 nm) to have a double pass absorption. The double pass absorption greatly improves the RC time and the Transit time of the APD for a higher frequency response.

[00141] FIG. 8 is a cross section showing a silicon epitaxial structure for a high-speed high-efficiency microstructured APD, according to some embodiments. Layers 800 are shown prior to microstructure processing. With minor modifications, the n and p doping can be switched and the direction of illumination may also be affected. Starting with a N silicon substrate 802 (or low doped or silicon on sapphire or a BOX /SOI wafer depending on the application and packaging considerations), an N⁺ layer 804 (N ohmic contact layer) is formed with doping concentration of greater than 10^{18} cm^{-3} (typically phosphorous) with layer thickness ranging approximately from 0.1 to 10 μm . A non-intentionally doped layer "i" 806 or a P⁻ (very low doping level P layer) has a doping concentration less than $5 \times 10^{16} \text{ cm}^{-3}$ (this is the multiplication or electronic gain layer of the APD) with thickness ranging approximately from 0.1 to 2.0 μm depending on gain and bandwidth of the APD. A P charge layer 808 is grown with an approximate thickness 0.05-0.2 μm and doping concentration of greater than $2 \times 10^{17} \text{ cm}^{-3}$. An absorption layer 810 is grown (P⁻ or "i") ("I" and "i" are used interchangeably herein) with doping less than $5 \times 10^{16} \text{ cm}^{-3}$ with thickness ranging approximately from 0.1 to 5 μm . Finally a P⁺ contact layer 812 is grown with doping greater than $5 \times 10^{19} \text{ cm}^{-3}$ with layer thickness ranging approximately from 0.1 to 1.0 μm . According to some embodiments, all layers 800 are grown epitaxially using CVD or MOCVD reactors. Doping and thickness are approximate and are adjusted depending on applications.

[00142] For best noise performance of the Si APD, photogenerated electrons should dominate in the multiplication process; i.e. holes diffuse/drift toward p (anode) and electrons diffuse/drift toward the n (cathode) with reverse bias. The Si layers 800 are grown epitaxially using chemical vapor deposition, plasma

5 enhanced chemical vapor deposition, molecular beam epitaxy, atomic layer deposition (can be a combination of these methods to generate the optimal layer structure in doping and interface quality) on doped or undoped substrates. The total length for the electrons to transit range from approximately 0.25 to 7.2 microns. This can be, for example, 0.5 μm for absorption, 0.1 μm for charge, 0.5
10 μm for multiplication, with a total of 1.1 μm for the APD layer structure 800 shown. According to some embodiments, for higher QE, the absorption region can be lengthened to one μm for a total transit length of 1.6 μm for example. Other layer thickness and doping concentrations can be adjusted to optimize device characteristics for different wavelength, integration with CMOS, application
15 requirements, operating conditions such as bias voltage, gain and noise.

[00143] Also, the APD can be illuminated with modulated optical signal from the bottom, where using BOX or SOI, the bulk of the substrate can be removed to minimize optical losses and thus can use the double pass of the photons in the enhanced absorbing microstructured layer.

20 **[00144]** FIGs. 9A-9E are a series of cross sections showing some basic microstructure processing steps, for a high-speed APD, according to some embodiments. FIG. 9A shows the high speed APD epi structure 800 as described with respect to FIG. 8. In FIG. 9B, as in the PD process, a P-ohmic metallization or dielectric mask 910 can be deposited first on the P layer 812 for the
25 microstructured pillars. In the case of holes and/or voids this step may not be carried out. Dry etch mask 910 is deposited on the surface using photolithography, metal/dielectric deposition techniques and wet/dry etching. In FIG. 9C, according to some embodiments, reactive ion etching (RIE) or deep reactive ion etching (DRIE), wet etching using chemicals and oxidation of the Si are used to generate
30 the microstructured pillars 914. Native silicon oxide for surface passivation can be provided by thermal oxidation (which is preferred in some cases), electrochemical anodization, and/or plasma enhanced chemical vapor deposition. According to some embodiments, the thermal oxidation of the pillars 914 can also be used to

fine tune the diameter of the pillar since the oxide is created from the Si material. Thermal oxidation also smooths the surface which is favorable for electrical properties. In FIG. 9D a filler 916 is used to fill or partially fill the space between the Si pillars 914 to support subsequent contact layers to be deposited. The filler
5 916 can be spin on glass, polyimide, dielectric such as silicon nitride, or silicon oxide, that can be deposited for example using plasma enhanced chemical vapor deposition. Once the contacts are made the fillers can be left in place or removed by dissolving the filler with an etchant or solvent. Removing the filler has an advantage of further reducing the capacitance of the device since air has a
10 dielectric constant of 1. The reduction of the capacitance allows the device to operate at higher bandwidth due to reduction of the RC time. In FIG. 9E, the anode and cathode ohmic contact metallizations 922, 924 and 926 are made. Depending on the direction of illumination, transparent conducting oxide TCO 932 (such as indium tin oxide ITO) can be used. In the case of top illumination, a dry
15 etch can be used to expose the pillars if they are buried in the filler. The TCO 932 can then be used to contact the P⁺ silicon pillars at the tip or the P ohmic metallization 922. Ohmic contact metallization is then applied to the cathode (N⁺) layer either on the surface (924) or bottom (926) depending on integration topology.

20 **[00145]** In the case of the optical signal coming from the substrate side (the bottom), the wafer is thinned. If the thinning is carried out by etching it can include a buried silicon dioxide layer such as silicon on insulator, SOI/BOX, such that the oxide layer can act as an etch stop layer. The wafer can be thinned first by chemical mechanical polishing to 100 μm followed by a via etch to the oxide layer
25 which can be selectively etched off, such that the optical signal only need to traverse a few micrometers of Si bulk material. Anti-reflection coating 930 is applied to the Si surface to minimize reflection loss. Ohmic metallization is applied to the N⁺ layer followed by bond metal 924. On the microstructured pillars, ohmic metallization is applied to the P⁺ tips (if its not applied already in the preliminary
30 steps), followed by bond metal 922. According to some embodiments, an advantage of the optical signal entering from the substrate surface (i.e. the bottom) is that the light will bounce and travel twice within the pillar structures, thus

increasing the quantum efficiency. According to some other embodiments, the pillars can be made shorter to improve the transit time.

[00146] According to some embodiments, the optical signal can also enter from the edge as shown FIG. 52, *infra*, either in a guided mode or in free space. In the edge application, TCO 932 and solid anode ohmic contacts may not be used and wafer thinning may not be carried out. Cathode ohmic contacts can instead complete the structure. According to some embodiments, in edge approach, the pillars are arranged such that their density is not uniform to optimize the capture of the optical radiation. It can be arranged in a V pattern for example to reduce optical reflection.

[00147] Not shown in FIGS. 9A-9D are mesa etching steps used to define the diameter of the APD 920. According to some embodiments, other methods such as ion implantation may also be used. Note that the microstructures themselves provide good confinement of current in the vertical direction and not in the lateral direction. Other known processing steps that are not shown for sake of simplicity include: thermal oxidation passivation of exposed surfaces; adding guard rings; thinning of the wafer; adding anti-reflection coatings; annealing of ohmic contacts; and creating via holes for removal of filler.

[00148] Taking advantage of low absorption constant of bulk Si. High speed photodiodes made with III-V material often are constructed such that the photocarriers are generated only in the i layer of a PiN structure to minimize the photogenerated carriers outside of the high field region that can cause degradation to the frequency response of the device. This can be done easily in III-V material since there are many ternary and quaternary material such as InGaAsP, InGaAs, InAs, that are lattice matched to InP and the bandgap of these alloys can be changed by altering the composition such that the P⁺ anode 812 and P charge 808 layers are mostly transparent and the i layer is absorbing. However it is not easy for silicon since there are no materials that are lattice matched to silicon. Germanium can be grown on silicon but with the addition of a buffer layer to accommodate for the lattice mismatch.

[00149] According to some embodiments, a method to overcome this issue in silicon is to take advantage of the low absorption constant of silicon at radiation near the bandgap of silicon. According to some embodiments, the wafer can be

thinned to the insulator of an SOI structure and the 850 nm optical signal will only traverse 1-2 μm of bulk silicon losing approximately 10% or less of the incident radiation. The rest of the radiation continues to the microstructured pillar silicon where the absorption is stronger possibly due to resonance effects. According to

5 some embodiments, the shape of the pillars can be circular, oval, rectangle, chevron, hexagon, double-circle, crescent, star, or any shape to optimize absorption and collection efficiency. The pillar diameter range from 50-1200 nm (smallest dimension can be 50 and largest dimension 1200 nm) and can be spaced uniformly or non-uniformly, periodic or aperiodic, chirped, or a pattern either locally
10 or globally to optimize APD/PD performance and applications. The spacing of the pillars can be 20-2000 nm. The microstructured pillars can be 100 to 10000 nm in length that is optimized for bandwidth and efficiency for a particular wavelength near the silicon bandgap for example 850, 880, 980, 1000 nm.

[00150] According to some embodiments, multiple dimensions (both structure
15 and spacing) of the microstructures within a single PD/APD can broaden the resonance bandwidth of the microstructures such that the enhanced absorption coefficient is over a broader optical spectrum.

[00151] The substrate becomes less absorbing as the wavelength approaches 1100 nm (1.1 eV Si indirect bandgap).

20 **[00152]** According to some embodiments, the microstructured pillars/holes/voids can have orientations that are not perpendicular to the surface of the silicon substrate. Other orientations off perpendicular or with multiple orientations or even random or pseudo-random are possible to optimize the QE with respect to the directivity of the optical signal. In multiple and/or random or pseudo random
25 orientations of the microstructures, the device become less sensitive to the direction of light illumination which is beneficial in PV applications. In certain applications, antenna like high directivity of the PD/APD may be desirable to avoid cross talk for example from other optical signal sources or to further improve its QE.

30 **[00153]** According to some embodiments, microstructured hole arrays, instead of pillar arrays, are used as light traps in silicon. Microstructure hole arrays have similar properties as microstructured pillars. See e.g. Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications,

Next Generation (Nano) Photonic and Cell Technologies for Solar Energy Conversion, edited by Loucas Tsakalakos, Proc. of SPIE Vol. 7772, 77721G (2010). According to some embodiments, instead of etching microstructured pillar arrays as described herein, microstructured hole arrays are etched using RIE/DRIE

5 and similar processing for the pillars, including thermal oxidation for surface passivation, deep ion implantation for electrical isolation, confinement of optical fields and reduction of capacitance. In the case of the hole arrays, it is possible that the filler need not extend the entire length of the hole. For example, if the surface tension of the filler is high, only partial filling of the holes with filler will be possible
10 and provide support for subsequent layers of TCO, metal, oxide, silicide, alloys to name a few that may be necessary to complete the device structure. According to some embodiments, in the case of microstructured holes, fillers are not used in the PD/APD/PV devices since the surface is contiguous rather than consisting of islands as in the case of microstructured pillars.

15 **[00154]** According to some embodiments, the microstructured holes can have diameters of 50-3000 nm and can be a square, hexagon, oval, rectangle, chevron, double-hole, with the smallest dimension at 50 nm to the largest dimension of 3000 nm approximately. The spacing between holes (adjacent edges) can be regular or irregular or a pattern at 20-2000 nm. The depth (or length) of the hole can be 100
20 to 10000 nm and can be uniform depth or non-uniform depth. Dimensions are chosen for optimal absorption, quantum efficiency, bandwidth and radiation collection efficiency for a particular wavelength and application.

[00155] As discussed earlier, to optimize High Contrast Grating in the Absorption regime of this invention, it may be desirable to have the microstructured
25 enhanced absorption structures on materials of a lower refractive index such as BOX or SOI where the silicon dioxide refractive index is lower than that of Si, Ge or III-V/II-VI material. According to some embodiments, the effective refractive index can be made lower than the refractive index of the microstructures with the inclusion of voids in the substrate. FIGs. 10A-10B are cross sections showing
30 aspects of a top illuminated microstructured photo diodes, avalanche photo diodes and/or photovoltaics (PV) with microstructured voids in N-Si, according to some embodiments. Voids can be included in the substrate or as a microstructure for enhancing absorption coefficient as will be discussed *infra*. Refractive index in the

optical spectrum of Si, Ge, III-V material typically range from 3-3.6, by using silicon dioxide such as SOI and voids that are 50% of the material in volume, the refractive index or effective refractive index can be reduced to approximately 0.5 that of the bulk semiconductors. By adjusting the ratio of the volume of the voids to the material (Si for example) the effective refractive index can also be adjusted from a few percent to more than 90% that of the bulk material. The voids can be filled with other material such that it is not just air, gas or vacuum, but a dielectric such as glass, polymer, dielectric, oxide, or amorphous semiconductor that can be optically and/or electrically passive and or active with optical and/or electrical gain for example.

[00156] FIG. 10A shows the layers 1000 including N-Si layer 1006 which contains microstructured voids 1008 that effectively reduce the refractive index of the N-Si layer 1006 as described. FIG. 10B shows a top illuminated PD/APD/PV 1020 that includes microstructured pillars 1024 and/or holes 1022, as well as transparent conducting oxide layer 1026. Microstructured voids 1008 can be random or patterned. The microstructured voids 1008 can be used reflect photons back to the absorbing "I" region if the voids 1008 are patterned to have HCG effects at wavelengths where loss is low such as 950-1100 nm. According to some embodiments, BOX or SOI substrates can also be used together with voids or without voids or without BOX/SOI.

[00157] According to some embodiments, the microstructuring techniques described herein are also applied to heteroepitaxial material (III-V on Si, Ge on Si, or II-VI on Si). Ge (bandgap 0.66 eV at 300K) having much smaller bandgap than Si, can be used for detecting optical signals at 850 and 1300 nm. Using the techniques described herein, Ge devices can also be made to detect optical signal with wavelength at 1550-1600 nm which can then replace III-V material based photodetectors. According to some embodiments, microstructures are grown such as nano/microwires or etched from bulk material with or without lithographic masking.

[00158] Ge thin film can be grown epitaxially on Si. See, e.g. Kang et al, Epitaxially-grown Ge/Si avalanche photodiodes for 1.3 μ m light detection, 23 June 2008 / Vol. 16, No. 13 / OPTICS EXPRESS 9365 (hereinafter "Kang et al."), where an APD was fabricated for 1310 nm wavelength operation for a 30 μ m diameter

device. The QE of the device with a 1 μm Ge absorption length is only 56% whereas by using microstructured pillars/holes/voids according to embodiments described herein, QE of approximately 90% or greater can be achieved at 1300-1600 nm wavelength with bandwidths of approximately 30 Gb/s or greater for a 30
5 micrometer diameter PD/APD. Such devices can find useful applications in datacenters, local area networks, and in metro and long distance optical data/telecommunications. According to some embodiments, integration on silicon is used which results in significant cost reduction in manufacturing and packaging. In comparison, in Kang et al. a 30 μm diameter APD was only able to reach
10 approximately 15 Gb/s bandwidth at 1310 nm and cannot extend the wavelength due to low absorption of the bulk material without sacrificing a significant reduction in bandwidth.

[00159] FIGs. 11A and 11B are cross sections showing aspects of an heteroepitaxial APD structure of Ge on Si, according to some embodiments.

15 Layers 1100 and APD device 1120 show a possible heteroepitaxial APD structure of Ge on Si (as opposed to descriptions, *supra*, of homoepitaxial APD/PD structure where only silicon is used with different doping concentrations). Similar processing methods as in the homoepitaxial Si APD are used to fabricate microstructured pillar/hole arrays. According to some embodiments, the absorption constant of
20 bulk Ge is enhanced by greater than 70X, for example 73-172X. According to some embodiments, APDs and PDs with bandwidths in excess of 30 Gb/s can be achieved in devices with an active diameter of 30 μm or less at wavelengths to 1750 nm and QE of approximately 90% or greater. This is a significant improvement over existing Ge on Si APD with illumination normal or off normal to
25 the surface of the substrates.

[00160] According to some embodiments, the microstructured pillar and hole (and variations thereof) arrays can be fabricated in Si, Ge, Ge on Si, SiGe on Si, SiGe on Ge; it can be any combination of Si, Ge and SiGe.

[00161] At longer wavelengths 1200-1800 nm, Ge (germanium) photodiodes are
30 often used since Ge has a bandgap of 0.66 eV (whereas Si has a bandgap of 1.1 eV). However, for high bandwidth applications (greater or equal to 20 Gb/s) Ge photodiodes are only good to 1350 nm due to the fact that for transit times to be approximately 30 picosec (electron saturated drift velocity is 6×10^6 cm/s at 1×10^4

V/cm in order to have a bandwidth of approximately 20 Gb/s ($f(3\text{dB})=0.44/\tau$ where τ is the transit time through the "I" region) the length of the absorption region or the "I" region is limited to approximately 2 microns. At this length, the QE at 1550 and 1600 nm is less than 10%, which is not generally acceptable for optical receivers for datacom and telecom applications. In a waveguide configuration, the length of the absorption region can be 50-100 microns and still achieve 20 Gb/s or higher with QE equal or greater than 90%. The waveguide Ge on Si photodiode structure have been reported by other research groups however such waveguide photodiodes have excess optical losses due to waveguide losses and coupling loss (coupling of optical signal to the optical waveguide) which can be as high as 3 dB or half of the optical signal is lost. The "free-space" coupling (where the optical signal is directed to the PD/APD using elements such as lens, diffraction elements, light pipes, optical waveguides to name a few) of optical signal to the microstructured photodiode and avalanche photodiode have much less optical losses, typically a few percent or less. One of the reason is the large area of the microstructured PD/APD which is 30 microns in diameter as compared to waveguide photodiodes its dimensions are a few microns, typically 1-2 microns. Not only is coupling loss high in waveguide PD/APD, it often uses active alignment which requires that the waveguide PD/APD is turned on to monitor the coupling of the optical signal into the waveguide PD/APD. This active alignment is slow and time consuming which adds cost to the packaging of the waveguide PD/APD in any optical receiver module. In contrast, the large area microstructured PD/APD, according to some embodiments, uses only passive alignment where it is aligned without turning on the microstructured PD/APD. Such alignment is much faster and easier which reduces the cost of a microstructured PD/APD in any optical receiver module. It should be noted that with the effective capacitance of the microstructured PD/APD significantly lower than bulk PD/APD by 10 to 80% or more, the area of the microstructured PD/APD can be correspondingly larger by 10 to 80% or more.

[00162] In FIG. 11B, a microstructured Ge on Si pillars/holes APD structure 1120 with bottom illumination is shown. Epitaxial layers for an APD Ge on Si are used where the optical absorption to generate electron-hole pairs takes place in Ge and the gain/multiplication of the electrical charged carriers takes place in Si. The

epitaxially grown layers are similar to Ge on Si bulk (thin film) APD with the following layer compositions ranges (shown in FIG. 11A). N is undoped, or low doped (20 ohms-cm) Si substrate 1102, which can also be SOI or BOX, to allow removal of the Si substrate for bottom illumination and/or to reduce the refractive index. If SOI or BOX substrates are used, the N ohmic contact and bond metal will be on the N⁺-Si surface adjacent to the multiplication I region. N⁺ contact layer 1104 which can be 2-8 microns, $N^+ > 5 \cdot 10^{18} \text{ cm}^{-3}$. I multiplication layer (or gain layer) 1106 which can be undoped (not intentionally doped), 0.2-1.0 microns thick and $I < 1 \cdot 10^{16} \text{ cm}^{-3}$. P charge layer 1108 having a thickness of 0.05-0.2 microns and $P \sim 1\text{-}6 \cdot 10^{17} \text{ cm}^{-3}$. P⁻ low temp Ge buffer layer 1110 having a thickness of $\sim 0.01\text{-}0.04$ microns and $P^- \sim < 1 \cdot 10^{16} \text{ cm}^{-3}$. I or P⁻ absorption layer 1112 having a thickness of 0.2- 2.0 microns, and I (or P⁻) $< 1 \cdot 10^{16} \text{ cm}^{-3}$. Finally, P⁺ contact layer 1114 has a thickness of 0.05- 0.2 microns, and $P^+ > 2 \cdot 10^{20} \text{ cm}^{-3}$, approximately.

[00163] Starting with a wafer with all the layers 1100 grown for APD operation, the processing details are left out for simplicity. The basic steps involve first, depositing the p ohmic contact metal layer 1126 using e-beam, thermal or sputtering deposition. The microstructure pattern of either pillars or holes is photolithographically, using positive or negative or image reversal photoresist methods depending on pillars or holes, defined to form the etch mask for either dry or wet etching. According to some embodiments imprint lithography can be used. The microstructure patterns are etched on the P⁺ and I (or P⁻) and P Ge layers 1114, 1112 and 1110, respectively, partially or fully to the P Si layer 1108 (e.g. using fluorine, chlorine, bromine based gases such as SF₆, CF₄, BCl₂, Cl₂, for selective dry etching using RIE and DRIE). The selectivity of the etch between Ge and Si can be as high as 70, so as to etch Ge 70 times faster than Si by adjusting gases mixtures, pressure, temperature and bias, and power. The sidewalls of the microstructure patterns (pillars or holes) are passivated with dielectric or SiGe and gradually reducing the Ge content such that Si remains on the surface (using for example atomic layer deposition ALD) and subsequently using thermal oxidation to minimize surface recombination of the photogenerated carriers via surface states due to dangling bonds and other surface imperfections. According to some embodiments, other passivation techniques may also be applied such as ALD of Si oxides and Si nitrides. Planarization is performed using either spin on glass,

polyimide, or PECVD deposition of dielectrics such as Si oxides and Si nitrides. An etch back is performed to expose the P layer. For microstructured holes and pillars, it may not be necessary to planarize completely, by using polyimide or spin-on glass to partially fill the holes and spaces between pillars. Ohmic and/or bond

5 contacts are formed on the P and N layers. For top illuminated photodetectors, where the optical signal enters on the epitaxial surface where the microstructure patterns are fabricated, a transparent conducting oxide 1126 (the transparent conducting oxide may not be used in the case of microstructured holes) is deposited to connect all the P ohmic metal layers (for pillars). A voltage bias is

10 applied between the P⁺ Ge layer 1114 (anode) and the N⁺ Si layer 1104 (cathode) of -2 to -45 V. The APD 1120 is operated in a reverse bias mode to deplete as much as possible both of the "I" layers. Many detailed processing steps are left out such as annealing, surface preparations, deposition of ohmic contacts, bond metal, RIE, DRIE, wet etching, masks for etching, mask removal, antireflection coatings,

15 mirrors such as Bragg reflectors on the microstructured layers, to name a few. Ohmic contact metallization to P and N semiconductors and bond metallizations are well known in the art and details are not mentioned here. Also, holes are used in electron-hole pairs as charged electrical carriers and holes as in a physical void such as the microstructured holes. From context it should be understood if "hole"

20 refers to a charged electrical particle or a physical void.

[00164] According to some embodiments, Ge surfaces of the microstructured pillars or holes and any Ge surfaces exposed to an electric field, where electric current can flow and/or where electric charges are formed are passivated to reduce current leakage, minimize surface states that can be a potential sink or

25 recombination centers for carriers, especially photogenerated carriers of electrons and holes (as in Si, thermal oxide or rapid thermal oxidation, to create SiO₂ and SiO_x used to passivate any silicon surfaces that can cause excessive leakage current or recombination centers for photogenerated carriers, or a carrier sink) and GeO_xN_y which is a native Ge oxynitride that is formed in two stages, where the Ge

30 microstructured pillars and/or holes are first exposed to oxygen and then to ammonia ambient in a rapid thermal annealer to form the Ge oxynitride passivation layer. These passivation methods are well known in the art.

[00165] FIG. 12 is a cross section illustrating aspects of a passivation method for Ge surfaces on microstructures, according to some embodiments. Shown are microstructured Ge pillars 1202 (or holes) for a PD and/or APD. On the Ge surfaces is conformally epitaxially grown SiGe layer 1210. Gradually, the Ge content is reduced within layer 1210 until only Si is exposed on the surface. Thermal oxidation of Si is then used to passivate the exposed Si surfaces, forming SiO₂ layer 1212, to minimize leakage current and surface states that can be a potential sink for carriers, especially photogenerated carriers (electrons and holes) that can degrade QE.

[00166] FIGs. 13A and 13B are graphs showing the effects of microstructure enhancement of Ge bulk absorption coefficient for photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments. According to some embodiments, a 73x enhancement of bulk absorption coefficient is gained in PD/APD devices having microstructured pillars/holes at 1550 and 1600 nm. FIG. 13A shows the bandwidth versus “d” or the length of the “I” layer for 1550 nm (point 1310) and for 1600 nm (point 1312). Note that APDs have both a Ge “I” layer and an Si “I” layer; whereas for PDs have just a Ge “I” layer. FIG. 13B shows QE versus “d” or “I” layer length for 1550 nm (point 1320) and 1600 nm (point 1322). It can be seen that for a 30 micron diameter active region PD/APD bandwidths of 40 and 31 Gb/s can be attained at 1550 nm and 1600 nm optical wavelength respectively with 90% QE. This result was not achievable with bulk Ge photodiodes and avalanche photodiodes of conventional design.

[00167] The separation of using Ge microstructures to absorb the light generating e-h (electron-hole) pairs and using Si for the avalanche multiplication of the carriers, preferably electrons, results in an APD with very low noise due to the fact that the ionization ratio (defined as hole ionization rate/electron ionization rate) for electrons injected into the multiplication region (gain region which is a function of applied reversed bias voltage) is lower than in III-V material family. This result in a low excess noise factor leads advantageously to a high signal to noise ratio (S/N).

[00168] FIGs. 14A-14B are cross sections showing aspects of a top-illuminated Ge on Si avalanche photodiode having microstructured pillars/holes, according to some embodiments. FIG. 14A shows the bulk layers 1400. In FIG. 14B, top

illuminated microstructured Ge on Si APD 1420 is shown with a semitransparent conductive oxide 1426 connecting the P-ohmics on the Ge microstructured pillars 1424 (holes 1422) as described *supra*. Both top and bottom illuminated microstructured Ge on Si share similar epitaxial structures. The processing steps

5 for top and bottom illuminated microstructured APDs are similar. The main differences are that the transparent conductive oxide for top illuminated APD (or PD) is replaced with an opaque ohmic/bond metallization that can act as a mirror to reflect the optical signal back toward the absorption I layer. According to some embodiments, the mirror can also consist of Bragg reflectors either wafer bond to

10 the microstructure or epitaxially or vacuum deposited such as dielectric or conductive metal dielectrics to enhance the reflectivity to greater than 90% of the optical signal. In addition, bottom illuminated PD/APD may require a window or via where most of the Si substrate is removed to reduce optical losses depending on the wavelength of the optical signal.

15 **[00169]** FIGs. 15A-15C are cross sections illustrating aspects of bottom-illuminated Ge on Si avalanche photodiodes having microstructured pillars/holes, according to some embodiments. FIG. 15A shows the bulk layers 1500 prior to forming the microstructures (pillars and/or holes). FIG. 15B shows a Ge on Si microstructured APD 1520 with the optical signal illuminating from the bottom

20 (substrate side) for wavelengths from 1200-1800 nm. Note that Si is basically transparent at these wavelengths. According to some embodiments, to further reduce optical losses, the Si wafer can be thinned just at the area of illumination, for example through a via of 50-500 microns in diameter and thinned to the N⁺ layer of the Si; or the Si substrate 1502 can include a BOX or SOI layer 1502. The Si

25 substrate 1502 can then be thinned selectively to the BOX or insulator layer 1502 which can be etched away selectively. According to some embodiments, an anti reflection layer (not shown) can be added to minimize reflection. The advantage of this arrangement is that the optical signal will have a double bounce, reflecting off the metallization 1526 on the Ge P⁺ layer 1514 and traversing the Ge "I" absorber

30 region 1512 once again. For example, as shown in FIGs. 13A and 13B, keeping the same absorption length, Ge "I" length, the QE for both 1550 and 1600 nm would be approximately 90% or higher for a Si substrate side (bottom) illumination by the optical signal assuming negligible reflection loss. According to some

embodiments, the Ge "I" absorption length can be further shortened to increase the bandwidth and still maintain acceptable QE.

[00170] For Ge epitaxially grown on Si, it is known that the bulk absorption coefficient is greater than that of Ge bulk by itself (not grown on Si); at 1750 nm the
5 Ge on Si absorption coefficient is approximately 100 cm^{-1} . According to some embodiments, this can be enhanced by the microstructured pillars and/or holes by 172 times. The resulting enhanced Ge on Si microstructured pillar and/or holes absorption coefficient can be about $1.72 \cdot 10^4 \text{ cm}^{-1}$.

[00171] FIG. 15C shows an APD 1540 in which the microstructure extends all
10 the way to the N cathode layer 1506 to further reduce capacitance and refractive index. In this case, the absorbing i layer 1512 is microstructured as is the charge layer 1510 and the i multiplication layer 1508. According to some embodiments, the microstructures can also be formed partially into the charge and multiplication layers 1510 and 1508. Additionally, according to some embodiments, the
15 microstructures in the absorbing layer 1512 and the multiplication layer 1508 need not be the same. In FIG. 15D, photons may generate electron hole pairs in the multiplication region which may contribute to added gain but also may contribute to excess noise. According to some embodiments, the absorption and multiplication region using the microstructure APD is combined in one region without the use of
20 the charge layer. This is possible due to enhanced absorption: the length of absorption and multiplication can be of the order of one micron or less allowing reasonable avalanche voltage.

[00172] FIG. 15D shows a microstructured APD 1560 where the absorption and multiplication region are a single region 1566, pillars or holes, according to some
25 embodiments. This is enabled by the microstructure enhancing the absorption coefficient so that less than one micron of the absorbing microstructure length is needed to achieve QE of approximately 90% or more and avalanche multiplication can also occur in this length of material. For example, if $0.5 \mu\text{m}$ of microstructured Si shown in Fig.15D is the thickness of layer 1566, a back illuminated APD 1560
30 allows a double bounce of the optical signal reflecting off the N ohmic contact and bond metallization resulting in an effective length of one micron of absorption length. The Si APD 1560 can operate at $0.5 \mu\text{m}$ multiplication length resulting in gain of 3 dB or more with a reverse bias ranging from -5 to -50 volts. According to

some embodiments, the structure shown in FIG. 15D can be applied to other material systems such as Ge, Ge on Si, III-V, and III-V on Si or not on Si.

[00173] FIGs. 16A and 16B are graphs comparing single pass and double pass photodiodes and/or avalanche photodiodes based on Ge on Si, according to some
5 embodiments. Points 1610 and 1620 show the bandwidth and QE values for single pass with d of approximately 1.4 microns and points 1612 and 1622 show the bandwidth and QE values for a thinner d of approximately 0.7 microns single pass. For double pass the device will have points 1612 for bandwidth and point 1622 for QE. At 1750 nm optical signal wavelength, using absorption coefficient
10 data of 100/cm for Ge on Si and with, for example, 172 times (172X) enhancement factor due to the microstructured Ge on Si photodiode/avalanche photodiode structures, a bandwidth of 27 Gb/s and a QE of approximately as high as 90% can be attained with an "I" (also "d") length of approximately 1.4 microns for a single pass (top illuminated - where the optical signal illuminates the top Ge
15 microstructured side). As mentioned earlier, for photodiodes the "I" or "d" is the absorption length, whereas for avalanche photodiodes the "I" is the combined absorption length and the multiplication length. For example, for an APD to achieve 27 Gb/s the total "I" length needs to be limited to 1.4 microns. A double pass arrangement can be used such that for example the absorption length is 0.9
20 microns and the multiplication is 0.5 microns, making the absorption length effectively 1.8 microns to achieve QE above 90%. However, if we instead have the optical signal illuminate from the bottom Si substrate side, the Si substrate and Si layers are basically transparent and have minimal optical losses (approximately 1-3 dB/cm) at optical radiation energies that are below the bandgap of Si (1.1 eV or
25 1127 nm wavelength at 300K) for example for radiation from 1200-1800 nm wavelengths. The advantage of illuminating from the Si substrate side (bottom) is that the optical signal can have a double pass at the Ge "I" absorbing region if the metallization on the P^+ contact layer is reflective which it should be since it is metallic composing of Au, Al, Ag, Cr, Zn, Ti, Ta, Ge, or a combination of these
30 metals and semiconductors. Bragg reflectors consisting of material with alternating refractive indices from oxides, nitrides, chlorides, semiconductors, either wafer bonded to the microstructures or deposited on the microstructures can also be incorporated. Reflectivity can be greater than 90%. With double pass, as shown in

FIGs. 16A and 16B, a bandwidth of 40 Gb/s can be attained with a QE approximately as high as 90% or more.

- [00174]** FIGs. 17A-17B are cross sections showing aspects of a top-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 700 to 1800 nm, according to some embodiments. FIG. 17A shows the bulk layers 1700. In FIG. 17B, Ge on Si microstructured pillars 1724 and/or holes 1722 are in a configuration for photodiode 1720. This is essentially a P-I-N structure where the "P" and "I" are Ge with microstructured pillars 1724 and/or holes 1722 to enhance the bulk absorption coefficient of Ge grown on Si. The increase in the absorption coefficient of Ge grown on Si (Ge on Si) could be due to the stress build in the Ge epitaxial layer due to lattice mismatch with the Si host substrate that it is grown on. Optical signal as in the case for Ge on Si APD can be illuminated from either the microstructured side (as in FIG. 17B) or the substrate side (as in FIG. 18B).
- [00175]** FIGs. 18A-18B are cross sections showing aspects of a bottom-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 1200 to 1800 nm, according to some embodiments. FIG. 18A shows the bulk layers 1800. FIG. 18B shows photodiode 1820 configured for signal illumination from the Si substrate side (bottom illumination) with photo energies that are less than the Si bandgap of 1.1 eV at 300K. The corresponding wavelength range is 1200 to 1800 nm. Ohmic contact 1826 can also act as a mirror such that the light makes a double pass of the Ge absorbing microstructures where the metal contact layer on the P Ge can reflect the optical signal back toward the Ge "I" absorbing layer.
- [00176]** It should be noted that in all the discussions of the P-I-N structures, according to some embodiments the P and N are interchanged such as with an N-I-P structure formed on a P substrate or on a low doped P substrate or undoped substrate. According to some embodiments, the N and P for the APD structures are also interchanged and the substrate can be P, low doped P or undoped. However, in an Si multiplication layer, to achieve the lowest noise and the best S/N, electrons are injected into the multiplication region as dominantly as possible since the ionization rate of electrons is higher than the ionization rate of holes in Si; the ionization ratio for Si can range from 0.06 to 0.002 where as compared to Ge

and InGaAs it is 0.9 and 0.45 respectively. This is why in many of the embodiments described herein the enhanced absorption is in Ge microstructures and the gain or multiplication which is dependent on the field strength and therefore on the applied reverse bias voltage which for the described devices can
5 range from -10 to -60 V, is in Si.

[00177] According to some embodiments, the microstructured pillars and or holes for Si and Ge on Si photodiodes (PD) and avalanche photodiodes (APD) are used to replace relatively expensive III-V photodiodes. The Si microstructured pillars and holes PD/APD can operate from 500 to 1100 nm at bandwidths of 20
10 Gb/s or higher and QE of 90% or higher. In particular, the datacom wavelengths of 730-980 nm. The microstructured pillars and or holes on Ge epitaxially grown on Si PD and APD can operate from 500-1800 nm with bandwidths of 20 Gb/s or more and QE of 90% or more. In particular, the telecom wavelengths of 1250-1600 nm and possibly to 1750 nm. The techniques described herein thus extends the
15 wavelengths, bandwidth and QE of conventional Si and Ge on Si free space coupled photodiodes and avalanche photodiodes.

[00178] According to some embodiments, the microstructured pillars can also be fabricated using VLS (vapor-liquid-solid epitaxy) growth of Ge nanowires on an Si substrate. Others have demonstrated the growth of vertical Ge nanowires on Si
20 (111) orientation for example, with Au nanoparticles as catalysts for the VLS epitaxial growth using chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD). Crystal orientations other than (111), or with materials with multiple orientations such as in polycrystalline may be used. Materials such as Si, Ge, III-V, glass, quartz, metal, to name a few can also be used as substrates.
25 According to some embodiments, a thin Ge buffer layer of approximately 2nm on Si (111) substrate is formed together with Au nanoparticles as catalysts for VLS growth in a CVD reactor. The Au catalyst can be deposited using a lithography mask to expose photoresist that is coated on the Si substrate. The Au is evaporated onto the Si substrate with patterned photoresist. Using standard
30 processing methods such as lift-off, the Au pattern is left behind on the Si substrate which is then the catalyst for Ge VLS growth on Si substrates. According to some embodiments, it can also be grown using selective area growth where a dielectric

mask is deposited on the Si substrate with a pattern of voids that allow Ge to grow in the void using CVD.

[00179] The microstructure of pillars and holes on the surface of a bulk photodiode not only enhance the absorption coefficient by factors ranging from 10-
5 200 over the absorption coefficient of bulk material (material without any microstructured features and grown on lattice matched substrates so that stress due to lattice mismatch is minimal) but also significantly reduce the capacitance of devices such as PDs and APDs. The reduction in capacitance allows the PD or APD to have a shorter absorption length, which in turns result in a faster transit
10 time for the photogenerated carriers to be swept out of the high field region. The absorption region typically is depleted as much as possible by the reverse bias voltage that is applied externally with an electric field strength approaching 10,000 V/cm or higher. If the microstructured pillars or holes can result in removing half or more of the semiconductor material, which for silicon has a dielectric constant of
15 11.9 and germanium have a dielectric constant of 16, replacing the removed material with either air (dielectric constant of 1) or polyimide (dielectric constant of 3.5) or other dielectrics with low dielectric constants, then the overall capacitance can be estimated to be the sum of the capacitance due to the total area occupied by the semiconductor and the capacitance due to the area occupied by air or
20 polyimide. $C(\text{total}) = C(\text{semiconductor}) + C(\text{air or polyimide})$ where $C = \epsilon A/d$ where ϵ is the dielectric constant times the free space permittivity (8.854×10^{-14} farads/cm), A is the area occupied by the semiconductor or air/polyimide and d is the length of the "l" region which can be the absorbing region or the absorbing and multiplication region as in the case for APD. From the equation for $C(\text{total})$, the more
25 semiconductor material which has a high dielectric constant removed and replaced by low dielectric material such as air/polyimide/ SiOx/spin on glass the lower the overall capacitance and the faster the RC time. This reduction of capacitance for PD and APD invention can be extended to other PD and APD such as those of III-V material, microstructures can be fabricated on its surfaces and extend into and
30 pass the optical signal absorbing regions to remove half or more of the semiconductor material to reduce its capacitance and can effectively make a larger area PD/APD and have the same bandwidth as before etching microstructures on the device. The larger area allows for easier coupling of the optical signal to the

photodetector. A simple formula for the increase in radius for example by replacing semiconductor material with low dielectric material is: $r = (\epsilon_1 / ((\epsilon_1 - \epsilon_2)x + \epsilon_2))^{1/2} r_0$ where x is the fraction of semiconductor area left, ϵ_1 is the dielectric constant of the semiconductor, ϵ_2 is the low dielectric material such as air or polyimide or spin on glass, and r_0 is the radius of the active area of the PD/APD before etching microstructured pillars and or holes. As an example, for a 20 micron diameter Ge photodiode with $\epsilon_1=16$ and for simplicity $\epsilon_2=1$ (air) and $x=.5$ (half of the semiconductor material is removed in the microstructured pillar or holes), the increase in the new radius with the same capacitance as the non-microstructured Ge PD is 13 microns or a diameter of 26 microns which is significantly larger than 20 microns and can significantly reduce the cost of coupling the optical signal into the microstructured large area photodetector. This reduces the cost of passive packaging of the optical receiver module and increase the yield.

[00180] FIGs. 19A, 19B and 19C are diagrams illustrating how microstructures can reduce capacitance of a photodiode such that a larger area photo diode can be fabricated with the same bandwidth and QE, according to some embodiments. FIG. 19A shows the bulk layers 1900 in an InP-InGaAs-InP structure. In FIG. 19B, the InP-InGaAs-InP layers with microstructured holes 1922 effectively reduce the capacitance of the photodiode 1920 to allow a larger area photodiode to be fabricated with the same bandwidth and QE. FIG. 19C is a top view showing PD 1920. The microstructured holes 1922 can be 100-1000 nm in diameter with depth of 0.1 to 3 microns. Also visible in FIG. 19C is contact ring 1930 and bond pad 1932. According to some embodiments, a complementary microstructured pillars can also be fabricated. According to some embodiments, the sidewalls of InP and InGaAs can be passivated with SiO_x, SiN_x (silicon oxide and silicon nitride via ALD or PECVD), polyimide or spin-on-glass that can be spun on using standard processing methods. The absorption coefficient of the bulk material can be enhanced by up to two orders of magnitude or more.

[00181] According to some embodiments, III-V material such as InP, InGaAs, InGaAsP, InAs, InSb, GaSb, InGaSb on Si, Ge on Si, is epitaxially grown in a sub micrometer selective area growth (SAG) or vapor liquid solid (VLS) (See, e.g. Sarkar et al, Heteroepitaxial growth dynamics of InP nanowires on silicon, Journal of Nanophotonics, Vol. 2, 021775 (12 February 2008); Roest, et al, Position-

controlled epitaxial III–V nanowires on silicon, Nanotechnology 17 (2006) S271–S275) heteroepitaxy using metal organic vapor epitaxy with or without catalyst which can consists of Au, Cu, Al, Ti, W, Fe, Cr to name a few. Also for vertical oriented microwires grown on silicon, wafers with surface orientation (111) are

5 selected. It is not necessary that the microwires be normal to the surface, it can be off normal and even have a mixture of orientations.

[00182] In VLS growth, the silicon wafer that has the layer structure for APD or PD just prior to heteroepitaxial growth is photolithographically (or e-beam or nanoimprint lithographically) patterned with aperture ranging from 10-5000 nm, and
10 spaced between 10-3000 nm. An Au deposition (e-beam, or thermal evaporation) follows with thickness of 0.1-10 nm, followed by a lift-off, VLS epitaxial growth in a MOCVD reactor.

[00183] For SAG growth (See, e.g. Chu et al, Wurtzite InP nanowire arrays grown by selective area MOCVD, Phys. Status Solidi C 7, No. 10, 2494 – 2497
15 (2010)), a 50 nm SiN_x is PECVD (or sputtered or ALD) deposited on a (111) oriented Si wafer with the necessary APD or PD epitaxial layers grown on it ready for heteroepitaxial growth. Using lithography (photo, e-beam or nanoimprint) apertures are defined with dimensions ranging from 10-5000 nm and spaced between 10-10000 nm followed by dry etching (RIE) to open a via to the silicon
20 surface. The wafer is then ready for SAG of Ge, III-V microwires in a MOCVD reactor.

[00184] Detailed processes such as surface treatments, surface preparations, annealing, plasma etching, are not described for simplicity. These processes can be found in the literature.

25 **[00185]** FIGs. 19D and 19E are cross sections showing aspects of fabricating an APD device having a III-V absorbing layer grown on a P-I-N silicon multiplication layer, according to some embodiments. In FIG. 19D, a Si APD structure 1940 is etched as shown for v epitaxial growth of the III-V material. In FIG. 19E a III-V absorbing layer is grown on P-I-N silicon multiplication layer for APD device 1960.

30 As in the III-V on Si for a PD device, the III-V nanowires or microwires can be grown on Si using VLS process with or without catalyst. Since the footprint of the nano/microwires on Si is of the order of a micron, defects due to stress from lattice mismatch are not a significant issue and high quality III-V nano/microwires can be

grown on Si. According to some embodiments, SAG is used for fabricating III-V microstructures on Si electronic gain layers.

- [00186]** From FIGs. 19D and 19E it can be seen that the InGaAs on Si APD 1960 starts with a Si APD structure 1940 where microstructures of holes or pillars are etched to the charge layer 1944 or just before the charge layer 1944. According to some embodiments, the microstructure holes and/or pillars can be etched into the multiplication layer 1942. Then using a process, for example SAG, with or without silicon oxide on the Si microstructure's sidewalls, I-InGaAs is grown, ending with P-InGaAs at the surface. Surface growth can use a process such as epitaxial lateral overgrowth (ELOG) to form a continuous P-InGaAs film of high quality. P ohmic alloy and bond metal 1966 are formed and annealed on the P-InGaAs. The back side processing consist of thinning the Si wafer using for example a BOX layer for selective etch stop and removing the BOX layer. Anti reflection can be coated on the backside silicon to reduce reflection. N ohmic 1968 is fabricated on the N Si layer. The optical signal is illuminated from the bottom. A reverse bias of -5 to -50 volts is applied to the cathode and anode. As mentioned earlier, the small footprint of the InGaAs on Si microstructure of the order of 10 square microns allows for high quality InGaAs material to be grown where lattice mismatch causing crystal defects are not significant.
- [00187]** According to some embodiments, the integration of Ge, III-V with Si PDs, PVs (See, FIG. 25C, *infra.*) and APDs allow the absorption spectrum of Ge and III-V material on a mature Si electronic platform. It allows integration of III-V with Si CMOS ICs for example for photodetector, optical light source such as light emitting diodes (LED) and laser diodes (LD) and III-V electronics such as transistors.

- [00188]** Multiple absorbing material and voids as microstructures. According to some embodiments, the microstructured pillars and/or holes are regrown with Ge such that both Si and Ge are microstructured to enhance the bulk absorption coefficient. According to some embodiments, voids can also be buried or embedded to generate a buried/embedded microstructure such that the surface is more planar. The microstructured voids can also enhance the absorption coefficient, by being patterned so as to enhance reflection and also to reduce the effective refractive index of a material (e.g. Si), reduce the weight of the device,

and increase mechanical flexibility. The microstructured voids can be random, pseudo-random or patterned typically with dimension and spacing that are approximately the order of a wavelength or subwavelength. According to some embodiments, instead of combining Ge with Si, others combinations can be used
5 for example III-V with Si or other semiconductor material, polymers, or other non semiconductor absorbers, which can significantly broaden the absorption spectrum over that of a single absorber.

[00189] The enhancement using nanowires (See, e.g. Garnett et al, Light trapping in silicon nanowire solar cells, Nano Letters, 2010, 10, 1082-1087;

10 Kelzenberg et al, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, Nature Materials, vol. 9, March 2010, 239-244) and nanoholes (See, e.g. Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Proceeding of SPIE, Vol. 7772, 77721G-1, 2010) have been reported by various groups. The known use of
15 nanowire for light trapping are for photovoltaic applications where the photogenerated carriers diffuse to the anode or cathode of a P-N junction with zero external bias, operating at DC (direct current). According to many of the embodiments described herein, the photogenerated carriers are swept out with an external reverse bias in the absorbing "i" region of a P-I-N diode (PD) or P-I-P-I-N
20 diode (APD) for high modulation bandwidth (e.g. greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain (e.g. gain greater than 3 dB). In addition, according to some embodiments, multiple absorbing materials can be used to broaden the absorption spectrum. The multiple absorbing materials are connected in parallel as current sources whereas in known
25 technology the absorbing materials are connected in series. In addition, the use of voids as microstructures to enhance the absorption of the material according to many embodiments described herein allows the surface to be more planar and simplify processing since fillers may be avoided. Also, the more planar surface allows the epitaxial growth of semiconductor Bragg reflectors to enhance reflection
30 for double or multiple pass absorption in the I absorption layer of the PD/APD. According to some embodiments, Dielectric Bragg reflectors can also be used in a more planar surface since the surface can be highly N or P doped and the ohmic contact can be made on the periphery such as a ring ohmic contact and the

dielectric Bragg reflectors deposited on the photosensitive area such as shown in FIG. 29, *infra*. Chemical mechanical polishing (CMP) can be used to smooth the surface of the epitaxial layer with buried voids.

[00190] Further aspects of fabricating devices having microstructured Ge that is buried or embedded in Si microstructure will now be described. FIG. 20 shows bulk layers without a final P-Si layer for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments. The final P-Si layer, according to some embodiment will be the last layer grown in the epitaxial structure where the first layer grown is the layer adjacent to the substrate, followed by the second layer that is adjacent to the first layer, and so forth to the last layer grown. Shown in FIG. 20 is P-I-N PD structure 2000 and a P-I-P-I-N APD structure 2020 both without the final P-Si layer. In many of the embodiments described herein, N can refer to N (mid N type doping of $5 \cdot 10^{16} \text{ cm}^{-3}$ to $8 \cdot 10^{17} \text{ cm}^{-3}$, low N doping less than $1 \cdot 10^{17} \text{ cm}^{-3}$, and high N doping greater than $5 \cdot 10^{17} \text{ cm}^{-3}$, with the same for P doping. I (or i) doping is commonly defined as intrinsic, or not intentionally doped or low doping background doping of less than $5 \cdot 10^{16} \text{ cm}^{-3}$. The "I" region is configured such that the field of a P-I-N junction is developed across the "I" region usually with an external reverse bias. In PD and APD applications, the absorbing material is in the "I" region so that the photogenerated carriers can be quickly sweep to anode (P) and cathode (N) layers. For APDs, the carriers (electrons in most cases shown here, since this gives the lowest noise APD) are swept to the second "I" region for multiplication (current gain) before transiting to the cathode layer). In the Figures herein, P-I-N, P-I-P-I-N structures are shown and the top P layer(s) that are in contact to external circuits are referred to as the anode and the N layer(s) that are in contact to external circuits are referred to as the cathode; the layers can be interchanged from P to N and N to P with P or low dope substrates to also fabricate PD's and APD's.

[00191] FIG. 21 is a cross section showing etching of microstructured pillars and/or holes for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments. The microstructure pillars 2104 and/or holes 2102 are etched into the I-Si layer, partially or entirely or to/into the N (PD structure) or P (APD structure) Si layer. The etching process can be one of the following: wet chemical etching, dry etching using reactive ion etching (RIE), a

deep reactive ion etching (DRIE), ion milling, and/or focused ion beam milling. The etching can be isotropic or anisotropic or a combination of isotropic and anisotropic. As shown in FIGs. 22 and 23, *infra*, Ge is then regrown in the etched region (i.e. the area around the pillars and on the sidewalls of the pillars in the case of pillars, or area in the holes, sidewalls of the holes in the case of holes) isotropically, anisotropically, or by selective area growth (SAG) where a dielectric layer such as SiO_x, SiN_x, cover area where regrowth of Ge is not desired which in some embodiments can include the sidewalls. During etching if a dielectric mask material such as SiO_x, SiN_x, SiC_x is used and left in place during epitaxial growth, the epitaxy layers may not grow on the dielectric mask in a crystalline film and may be amorphous in nature or may not grow on the dielectric layer other than some dendrites. Note that the isotropic or anisotropic growth rate often depends on the crystal plane it is growing on and any etched structures may expose multiple crystal planes resulting in different growth rates at those planes that can lead to anisotropic growth in the etched regions with 3D microstructures.

[00192] Growth of Ge on Si is well documented in the literature where a thin buffer Ge layer is first epitaxially grown at a lower temperature followed by a higher temperature Ge epitaxial growth using chemical vapor deposition (CVD), molecular beam epitaxy (MBE), atomic layer deposition (ALD), low pressure -CVD, and or a combination of growth techniques, for example the thin Ge buffer layer can be grown by MBE and the high quality thicker Ge film grown by CVD. The thin Ge buffer layer is to allow lattice mismatch stress to be accommodated between Si and Ge, (see, e.g. Feng et al, High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide, APPLIED PHYSICS LETTERS 95, 261105 ,2009).

[00193] The Ge regrowth may have voids or non-planarities and, where useful, the surface can be planarized using polishing such as chemical mechanical polishing (CMP) or etching. FIG. 22 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after the Ge "I" layer is grown in the etched region and planarized, according to some embodiments. Note that according to some embodiments, planarization is not needed and is omitted. After the Ge "I" layer 2202 is grown and planarized, a P⁺ Ge capping layer 2204 is grown to complete the P-I-N structure of a PD or P-I-P-I-

N structure of an APD. Optical signal or photons with wavelengths ranging from 400 to 1800 nm can illuminate the PD/APD 2220 from the anode (top) side (P⁺ side) 2202 and optical signal or photons with wavelength ranges 950-1800 from the substrate side (bottom) since Si is mostly non-absorbing at these wavelengths.

5 According to some embodiments, it is advantageous to configure the device 2220 for illumination from the substrate side since this will allow a double bounce of the optical signal or photons within the absorbing Ge microstructures embedded in Si. Shown in these figures are only the basic epitaxial layer structures. Structures and layers not shown for simplicity include: anti-reflection coatings, passivations, ohmic
10 metals, bond metallization, any metal interconnect to CMOS, via's for electrical connectivity, arrays of PD/APD for multichannel optical interconnects, to name a few. Optical signal/photons can illuminate either normal to the surface or at any angle off normal, including rotation angles for optimal PD/APD performances; optimizing QE and bandwidth of the PD/APD.

15 **[00194]** FIG. 23 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after I-Ge regrowth and planarization, and a cap layer of P-Si, according to some embodiments. In the case of FIG. 23, the buried Ge microstructures 2302 are capped with a P⁺ Si layer 2304. The Si P⁺ cap layer (anode) 2304 has low optical loss at optical wavelengths of 950-1800 nm
20 and therefore generates minimal photocarriers that are not in the high field "I" region of the PD/APD 2320 and contribute minimal diffusion photocurrent which can lead to a degradation of the frequency response of the PD/APD 2320 and the QE of the PD/APD.

[00195] Some dimension doping ranges for the buried or embedded Ge and
25 capping layers shown in FIGs. 20-23 will now be provided in greater detail, according to some embodiments. The dimension of the microstructured Ge (e.g. 2202 and/or 2302) can range in depth from 0.1 to 5 micrometers, have a lateral dimension range from 10-5000 nm, and a spacing between adjacent microstructure structures (the structures can be identical or non-identical) in contact (overlapping)
30 to 5000 nm. The "I" doping for both Ge (2202 and/or 2302) and Si (2104) is less than or equal to $5 \cdot 10^{16}/\text{cm}^3$. "I" is often called intrinsic or not intentionally doped and can have either a p or n background doping, the doping level is low enough that a reverse bias voltage of -2 to -45 volts can fully deplete the "I" region of

mobile holes or electrons (carriers). The capping layer, Si (2304) or Ge(2204) thickness can range from 0.1 to 5 μm with doping level greater than or equal to $6 \cdot 10^{17}/\text{cm}^3$. These parameters can be adjusted to other values, but the goals are to increase or optimize the QE and bandwidth of the PD/APD for a given application.

- 5 Series resistance, photogenerated diffusion current, ohmic contacts, capacitance, transit time, depletion of the "I" absorption region all contribute to the performance of the PD/APD. In addition for double/multiple bounce within the "I" region for optical signal illuminating from the bottom substrate side, a reflective metal or dielectric stack such as a Bragg reflector/mirror consisting of alternating dielectric
- 10 layers of different refractive indices or HCG can be used to reflect the optical signal back into the microstructured absorbing region at the top anode side. With the Si cap layer as in FIG. 23, the optical signal can illuminate the Si P⁺ cap layer (anode) 2304 and, since Si has minimal losses at 1100-1800 nm (below bandgap radiation), it can also have double bounce of the optical signal within the
- 15 microstructured buried/embedded Ge 2302 by providing a reflector such as a Bragg reflector epitaxially grown at the Si N⁺ layer or at the Si substrate to reflect the light back into the absorption region.

- [00196] According to some embodiments, all the discussions of microstructured layers herein, light can additionally impinge from top and bottom surfaces, as well
- 20 as on the sides of the microstructures, either directly or from scattering, near field effects, interferences, or resonance, which can vastly improve the QE of the microstructured photosensors since photogenerated carriers are generated directly in the high field absorbing "I" ("I") layer(s).

- [00197] According to some embodiments, dopant choices for Si and Ge (group 4
- 25 elements) include the following: (1) for donors (n-type) from group 5 elements - antimony, phosphorus, and arsenic; and (2) for acceptors (p-type) from group 3 elements - boron, aluminum, and gallium.

- [00198] It is also noted that in the structure shown in FIG. 23, the I-Ge microstructures 2302 buried in Si 2104 are completely surrounded by Si which has
- 30 a lower refractive index than Ge. At 1000-2000 nm wavelength range, the refractive index of Si is approximately 3.49 and for Ge is 4.1. The index ratio of Ge/Si is 1.17 so according to Chang-Hasnain reference, HCG effects will exist. The resonance and field concentration in the absorbing Ge microstructures can further enhance

the absorption coefficient from that of the bulk absorption coefficient value anywhere from greater than 1X to several orders of magnitude. The index difference also causes light to be confined and concentrated in the high index material, in this example, Ge; further improving QE.

5 **[00199]** The silicon (Si) microstructure can detect photons with wavelength ranging from 300-1100 nm and the germanium (Ge) microstructure can detect photons with wavelengths ranging from 300-1800 nm. According to some embodiments, for high bandwidth and high QE, the shorter wavelengths, 300-600 nm, may generate photocarriers outside the "I" region resulting in a diffusion
10 current that can result in non-optimal bandwidth and or QE. Where bandwidth is not an issue, the degradations may not be very significant.

[00200] FIGs. 24A and 24B are cross sections showing aspects of a microstructured APD with buried/embedded I-Ge absorbing microstructures in I-Si microstructures, according to some embodiments. FIG. 24A shows the bulk layers
15 2400. In FIG. 24B, the etched pillars 2424 and/or holes 2422 are filled with I-Ge (intrinsic-Ge, non-intentionally doped or undoped or low doped Ge) and finished with a capping layer 2426 of P⁺ Ge or Si to complete the anode of the APD 2420. The microstructured Ge 2422 is buried/embedded in Si 2412. Optical signal of wavelength 950-1800 nm (or photons from 300-1800nm where the shorter
20 wavelengths, 300-900 nm, may not have as high a bandwidth) can illuminate the APD 2420 from either top or bottom at various angles to the normal and/or normal to the surface. According to some embodiments, the starting layers prior to the I-Ge regrowth into the etched regions can also include the P⁺ Si layer 2426, such as shown in FIG. 7 with layer 726, *supra*. In the case shown in FIG. 24B, the starting
25 layer was removed to minimize P dopant diffusion during I-Ge regrowth. The buried or embedded Ge microstructure in Si microstructure allows the APD (or PD) 2420 to operate in two regimes. A first regime is at wavelengths where Si is low loss and Ge is absorbing or high loss (950-1800 nm). In this Si low loss regime, the Ge microstructures 2422 with a Si P⁺ anode cap layer 2426 is completely
30 buried in Si which has a lower refractive index than Ge. The Ge microstructure arrays can have HCG low Q with Q ranging from 1 to 3000 approximately (or other resonant, scattering, near field, linear and non-linear optical effects) or high enhancement of the absorption coefficient. A second regime is where both Si and

Ge are absorbing, 300-945 nm, and both Si microstructures 2424 and Ge microstructures 2422 work in parallel (parallel current generators) absorbing the photons with enhancement of the absorption coefficients of both Si and Ge. This is particularly advantageous for examples in photovoltaic applications.

- 5 **[00201]** FIGS. 25A - 25C are cross sections showing aspects of a photodiode having buried/embedded Ge microstructures in a Si microstructured pillar and/or hole array, according to some embodiments. Starting with a Si PD epitaxial layer structure 2500 with or without the P layer 2526, microstructures of holes 2522 and/or pillars 2524 are etched into the Si P layer 2526 and I layer 2512 and can
10 extend into the N layer 2510. Regrowth of Ge 2522 (or III-V material such as InGaAs, InAs, InSb, GaN, InGaN to name a few) using a process such as SAG with or without silicon oxide on the sidewalls of the Si microstructure 2524 or using a process such as VLS with or without catalysts, the I-Ge layer 2522 is grown
15 illuminated devices) at the surface where a process such as ELOG can be used to form a continuous P-Ge film. P ohmic alloy, annealed, followed by bond metallization completes the contact 2528 for the anode. The back side processing as discussed earlier is deposited on the silicon surface to reduce reflection. See, e.g. FIGs. 19A-19C, *supra*, where the silicon is thinned and etched to the BOX
20 layer selectively. The BOX layer is etched selectively and an anti reflection N ohmic alloy is formed on the N-Si layer, annealed and followed by bond metallization, which completes the cathode contact. Reverse bias of -2 to -10 volts is applied between the anode and cathode for high bandwidth PD applications. In PV applications, 0 bias is applied.
- 25 **[00202]** According to some embodiments, the dimensions and doping are similar to the Si microstructured PD shown in FIGs. 5A-5B, *supra*, with the I-Ge doping level less than $5 \cdot 10^{16} \text{ cm}^{-3}$, and dimensions ranging in thickness of 0.1 to 5 micrometers, and lateral dimension of the microstructure ranging from 10 to 5000 nm with adjacent structures that can touch/overlap to 5000 nm separation. Optical
30 signal/photons can either illuminate from the anode top side or cathode bottom side with wavelength range of 300-1800 nm and normal to the surface or at an angle to normal which can also include rotation. For bottom side illumination, the Si is thinned down to a few micrometers thickness for illumination at wavelength

ranges of 300-900 nm. Only the basic layers are shown for simplicity. For example, the following structures are not shown: isolation mesa or diffusion or ion implantation, passivation, anti-reflection, ohmic metal, guard rings (e.g. for an APD). Both Si microstructures and Ge microstructures can detect the optical
5 signal/photons in parallel for wavelengths where both are absorbing, 300-1100 nm, and only the Ge microstructure at wavelength ranges 900-1800 nm. The cap layer 2526 and 2546 in FIGs. 25B and 25C respectively can be either P⁺ Si or P⁺ Ge. For broad modulation bandwidth (sometimes just referred to as bandwidth) of greater than 10 Gb/s (gigabits per second), P⁺ Si cap layer is preferred for wavelengths
10 ranges from 950 to 1800 nm, since at these wavelengths Si has low optical losses (also referred to as low loss). According to some embodiments, the structure shown in FIGs. 25B and 25C can also be used for photovoltaic applications where no external bias is purposely applied in the reverse direction.

[00203] According to some embodiments, for all the structures shown, the P and
15 N can be interchanged to form for example N-I-P structures for the PD and PV (photovoltaic) and N-I-N-I-P structures for the APD.

[00204] The regrowth of Ge microstructures in Si also have applications in photovoltaic devices where the device is operated without external reverse bias. The P-I-N PD structure for example with Ge microstructures embedded or buried in
20 Si microstructures effectively have two bandgaps, Si bandgap and Ge bandgap that is exposed to the solar radiation. The combination of two bandgaps widens the absorption spectrum of the photovoltaic device and therefore can collect a broader spectrum of the solar energy. The two bandgaps can have a higher QE and or short circuit current over that of single bandgap photovoltaic devices or multiple
25 devices connected in series. The microstructures also have enhanced absorption that can further improve the QE and or short circuit current of the photovoltaic device. The solar spectrum at AM 0 and AM 1.0, with a photovoltaic device with a spectrum width of 300-1800 nm, at least approximately 90% of the solar spectrum is captured. In addition, in the PV device with Ge and Si microstructures are
30 adjacent laterally to each other (i.e. in parallel) rather than being vertically adjacent (i.e. in series) as in prior art PVs. This allows the Si and Ge to be exposed to solar photons equally and are parallel current generators that are additive; $I_{Si} + I_{Ge} = I_{total}$

where I_s is the photocurrent generated by the Si microstructures and I_{Ge} is the photocurrent generated by the Ge microstructure and I_{total} is the total photocurrent.

[00205] Although according to some embodiments the use of Si and Ge are described, according to some other embodiments, other materials are used.

5 According to some embodiments, Si is used with an InP microstructure embedded or buried. According to some embodiments, more than two materials are used such as Si, Ge, InGaAs, InP, GaAs, GaN, InGaN, InSb, to name a few. The microstructures, in addition to pillars and holes, can be embedded and or buried to use the effects of HCG to enhance the absorption coefficient over that of bulk
10 absorption coefficient to further improve QE and minimize the use of material in order to reduce cost of manufacturing.

[00206] FIG. 25C is a cross section showing grown Ge, InP, InGaAs to name a few, within silicon microstructures. SAG can be used where the sidewalls of the microstructures are oxidized or coated with a conformal dielectric and where the
15 oxide/dielectric is removed at the bottom of the microstructure surface where it is approximately parallel to the silicon substrate where it can provide crystalline information for the growth of Ge, InP, InGaAs microstructures. The area where the Ge, InP, InGaAs will epitaxially grow with or without catalysts using various growth methods such as VLS, MOCVD, CVD to name a few, is approximately 100 square
20 microns or less; more typically around 0.3-3 square microns. Because of the small area, crystalline defects due to lattice mismatch are not significant. The sidewalls with the silicon dioxide that can be thermally grown or deposited using ALD, provide an electrical insulation between the Si and the Ge, InP, InGaAs SAG grown layer. It should be noted that SAG growth can continue until the Ge or InP or
25 InGaAs (to name a few) can merge above the silicon microstructure and with lateral over growth (LOG) epitaxial process, the microstructures of Ge or InP or InGaAs can form a continuous epitaxial thin film layer that can be doped P type for the anode layer.

[00207] FIGs. 25D and 25E are cross sections showing aspects of a forward
30 biased device such as a vertical cavity surface emitting laser (VCSEL), according to some embodiments. VCSEL 2562 can also be fabricated using similar processing as described *supra* for the PDs, PVs and/or APDs. Starting with a Si PIN structure 2562, Si microstructure hole(s) 2564 are etched through I-Si layer

2566 to the N-Si layer 2568. According to some embodiments, the etching of hole 2564 can extend into the N-Si layer 2568. An SAG process is followed with or without silicon oxide on the Si microstructure sidewalls (oxide 2570 is shown).

First, a GaAs/AlGaAs distributed Bragg reflector 2572 (DBR) all N type is grown,
5 follow by N-GaAs 2574, The active layer 2576 is undoped InGaAs/GaAs multiple quantum well (MQW) of 1-5 wells, followed by P-GaAs 2578 to the surface and using ELOG which can form a continuous film at the surface of the I-Si 2566. Dielectric DBR 2582 on the P-GaAs 2580 completes the optical cavity. P ohmic alloy with anneal and bond metal 2584 on P-GaAs 2580 completes the anode
10 contact and N ohmic alloy with anneal and bond metal 2582 on N-Si 2568 completes the cathode contact. Forward bias of 1 to 20 volts to the anode and cathode will result 1200-1300 nm light to be emitted from the VCSEL 2560.

[00208] The design and growth of VCSELs at 1200-1300 nm and other wavelengths are known. See, e.g. "High-performance 1200-nm InGaAs and 1300-
15 nm InGaAsN quantum-well lasers by metalorganic chemical vapor deposition", Tansu et al; Selected Topics in Quantum Electronics, IEEE Journal of (Volume: 9, Issue: 5), 2003.

[00209] According to some embodiments, longer wavelength are selected when embedding InGaAs, InGaAsN and other III-V material, because at wavelengths
20 greater than 1000 nm silicon is mostly transparent and does not introduce excess additional optical losses. Accordingly, Si is a good heat sink for the VCSEL 2560. According to some embodiments, the GaAs/AlGaAs DBR 2572 is replaced with a silicon/air or a dielectric DBR on the bottom by thinning the Si wafer and etching to the BOX layer, removing the BOX layer and depositing a dielectric DBR. Design of
25 DBR, dielectric and semiconductors are well known. The silicon/air DBR will require further processing, using sacrificial layers such as Ge that can later be selectively etched away via etch trenches.

[00210] According to some embodiments, an LED is fabricated by applying minor variations, including removing the DBRs and adding multiple Si
30 microstructures. The LED can use MQW or just a simple heterojunction of P-GaAs/I-InGaAs/N-GaAs for example. Other semiconductors can also be used such as InGaAsN, InGaAsP, GaAsN, to name a few. The substrate can be another material such as sapphire, SOI, insulator on Si (IOS), ceramic, glass, quartz, GaN,

crystalline or non-crystalline. Additionally, other material for blue/UV LEDs such as GaN, AlGaIn, GaInN, AlN, can be grown using epitaxial reactors and methods of fabrication described above.

[00211] According to some embodiments, voids are formed, that are buried or
5 embedded in Si or Ge on Si or Ge. As used herein “buried” refers to cases when
the void is beneath the surface, and “embedded” refers to cases when the void can
intersect or be slightly above the surface. As described *supra*, during regrowth of
Ge on a microstructured Si with pillar and/or hole arrays, voids can develop due to
the fact that growth rate during epitaxial growth often depends on the crystal
10 orientation of the surface. Since etching microstructured pillars and/or holes in Si
can expose different surface orientation of the side walls, asymmetric growth rate
of Ge on these different Si surface orientation can result in void formation.
According to some embodiments, the void formation is exploited to generate a
buried and/or embedded microstructured void arrays that can behave as HCG and
15 or light trapping structures that concentrate the optical field and/or resonance
through interference of the optical field (amplitude and phase), scattering, near
field, linear and non-linear optical effects to enhance the bulk film absorption
coefficient by one to several orders of magnitude. In addition, the voids can be
used to reduce the effective refractive index of a material (e.g. Si with voids) since
20 the optical field sees an average or effective refractive index. At dimensions on the
order of a wavelength or less, the refractive index of voids and Si, for example, can
be approximated with an effective refractive index which is the average of the
volume occupied by Si and the volume occupied by the void. For example, if Si
occupies 1/2 the volume and voids occupy 1/2 volume, the Si index is 3.49 and the
void is 1.0 (for air), then the average effective index is approximately 2.25.

[00212] The voids also reduce capacitance of the device if the voids are
generated in the “I” region, as discussed *supra*; where the space between
microstructured pillars or the microstructured holes can reduce the capacitance of
the P-I-N PD diode or the P-I-P-I-N APD diode. The voids according to some
30 embodiments are either buried (buried holes) or embedded (space between pillars)
and the total capacitance is approximately the capacitance of the total area
occupied by the voids plus the capacitance of the total area occupied by the
semiconductor. In the case where the voids do not occupy the full thickness of the

"I" layer (i.e. only occupy part of the thickness), then the effective dielectric constant can be estimated by taking into account a volume that contains both the void and the semiconductor extending through the thickness of the "I" layer, the volume of the void and the volume of the semiconductor in a given volume; for example if the voids occupy 1/2 of a given volume of the thickness of the "I" layer and the semiconductor material occupies 1/2, and if the semiconductor material is Si with dielectric constant of 11.9, then the average effective dielectric constant is approximately 6.5, where the void is assumed to be air with dielectric constant of 1 for that given volume. The total area occupied by this effective dielectric constant, consisting of both voids and semiconductor material, is used in the capacitance calculation plus the area occupied only by semiconductor in the "I" region to give the total capacitance of the P-I-N or P-I-P-I-N diode. Reduction of capacitance leads to a reduction in RC time constant for the diode which improves the bandwidth of the PD and APD.

[00213] Although buried voids in semiconductor material are known, such voids are conventionally regarded as detrimental and as such are to be avoided. According to some embodiments, such voids are intentionally created and form useful features in the semiconductor material.

[00214] FIG. 26 is a cross section showing starting epitaxial layers in which microstructured voids are fabricated, according to some embodiments. To generate voids in PD, PV and APD structures start with a structure 2600. The starting material can be a Si PD or APD structure with or without the Si P⁺ anode layer. Details of the layers are not shown for simplicity.

[00215] FIG. 27 is a cross section showing microstructured holes/pillars etched into the I-Si layer, according to some embodiments. The microstructured holes (or space around pillars) are etched into the Si "I" layer and can extend pass the "I" layer or can be partially into the "I" layer. Wet and/or dry etching can be used or a combination of wet chemical and dry etching (RIE, DRIE for example) where the wet etching can be used to remove damage due to dry etching or wet etching in combination with dry etching and oxidation to form a certain shape or surface smoothness. As shown in FIG. 27, the etch can be isotropic or anisotropic, the sidewall can have negative or positive slope (slope defined with respect to the plane of the substrate). For anisotropic etching both negative and positive slope

can exist at the same time for an etched feature such as a pillar or hole.

Anisotropic epitaxial growth can result in void formation, with the shape of the void being determined by many factors including: side wall slope, crystal orientations of the side wall, growth conditions, pressure, temperature, flow rate, growth technique
5 (CVD, MBE, ALD or a combination of growth methods), surface preparation, and surface oxidation. According to some embodiments, surface oxide, partial oxide or other dielectric 2726 can be intentionally deposited on the side walls, which can also influence the regrowth of Si or Ge (or any other semiconductor such as InP, GaAs, InGaAs, GaN, InGaN, to name a few) and can be used to form voids.

10 **[00216]** FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping P⁺ anode layer 2826, according to some embodiments. The buried voids 2800 can be uniformly spaced, or with chirped spacing, or any complex patterns with a combination of periodic and aperiodic spacing or it can be random or pseudo-random. The buried voids 2800 can have a
15 length ranging approximately from 0.1 to 10 micrometers and lateral dimension ranging from 10-5000 nm. The voids can also be overlapping one another. Although FIG. 28 shows buried voids in Si, according to some embodiments buried voids can be formed in Ge. For example, in a Ge epitaxial layer on Si, or any other semiconductors, such as InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, and other
20 semiconductors in the III-V material family. The voids can be non-uniform in size and shape within the void and adjacent voids. The voids may also have non-uniform spacing and/or orientation. However, with proper process control uniformity in size and shape, patterning, random and pseudo-random placements of the voids can be attained. For simplicity the voids are shown to be uniform.

25 **[00217]** FIG. 29 is a cross section showing Bragg reflectors formed on the P-Si surface to provide a highly reflective mirror, according to some embodiments. With a more planar surface, high reflectivity Bragg reflectors 2900 may be deposited or grown using dielectrics or semiconductors on the P silicon layer 2826 surface. The ohmic contact and the bond metallization 2902 can be on the
30 peripheral in a ring configuration as shown in FIG. 29. Optical signal illuminating from the bottom will have a double/multiple pass through the absorbing I region thereby improving QE and the bandwidth of the PD/APD. In PV where bandwidth is not an issue, then the QE will be improved. According to some embodiments,

Bragg reflectors 2900 can be configured for wavelength selectivity so as to reflect the optical signal back into the absorbing I region.

[00218] According to some embodiments, voids are not only in the I region but are also formed in the P and/or N region of a PIN PD or PV, in the P charge region, 5 in the I multiplication region and/or the P anode and N cathode region of an APD. According to some embodiments, voids can also be formed in the substrate. The density, shape and material (voids can be filled with different material from vacuum, gas, helium to dielectrics with or without doping with rare earth elements for optical gain for example, carbon/graphene/diamond, copper, ceramics for 10 thermal conductivity for example) of the voids in each layer can be different or the same, or different/same within the same layer.

[00219] According to some embodiments, voids are also used to make the material more mechanically flexible and bend and or conform to different surface contours. For example, in PV applications where large sheets of the device are 15 fabricated, the sheets can conform to contours in for example the roof, or the sheets of semiconductor PV can be rolled for compactness in storage prior to deployment. According to some embodiments, voids sized between 0.01 microns and 1000 microns are introduced into semiconductor and/or glass material for use with photo voltaics for purposes of increasing flexibility and/or resistance to 20 physical damage and/or damage propagation.

[00220] High-density voids in semiconductors are also resistant to crack propagation since the crack will terminate at a boundary, in this case the boundary of the void. This is advantageous for large devices such as solar cells where if an object such as hail or stone strikes the solar cell, only the point of contact will be 25 damaged and perhaps a small adjacent area (5-50% of the diameter of impact for example) where the damages are localized to area of impact and cracks will not propagate across the entire cell. A device may survive such small damage events with minimal degraded performance without taking the entire solar panel down.

[00221] According to some embodiments, the voids are also formed in other 30 materials also such as glass, ceramics, polymers, metal, plastics, to name a few, to avoid crack propagation in case of foreign object impacts since cracks will terminate at a boundary, in this case the boundary at the void.

[00222] FIG. 30 shows an example of a PIN PD/PV structure 3000 with microstructured voids to enhance absorption, reduce bulk refractive index, reduce capacitance and increase mechanical flexibility of large sheets of PV on semiconductor material, according to some embodiments. The Si substrate is removed leaving only the BOX/SOI layers together with the PIN epitaxially grown layers. Ohmic contacts, bond metallizations, antireflection coatings, passivations, are not shown for simplicity. In addition to PV, the techniques are also applicable to PD, APD, light emitters such as light emitting diodes and diode lasers, and to electronic integrated circuits such as CMOS and ASIC (application specific integrated circuits) where voids can not only make the material more flexible and lighter but also as mentioned earlier more resistant to cracking. The voids, according to some embodiments can be filled with a gel that can repair impact damage and seal exposed cracked edges to prevent further deterioration due to moisture for example to the semiconducting surfaces. The gel can be spin on glass for example. According to some embodiments, the voids can be filled with material to enhance thermal conductivity for example, reduction of optical or microwave losses by removing the silicon and replacing with material that is not lossy such as Ar, He, Xe, N₂, Ne gas, or vacuum for example. The voids can have different sizes and shapes and densities and can be random, pseudo random, aperiodic, periodic, chirped, single or multiple patterns. The voids can also be in a single layer or in multiple layers of the device. Fig. 30, for example, shows the voids in P-Si layer 3002, I-Si layer 3004, and N-Si layers 3006 and 3008. According to some embodiments the index of refraction near the uppermost surface can be altered to more effectively index "match" with surrounding air so as to reduce reflections of incident light. For example, in PV applications near surface voids can be used to index match such that less incident sunlight is reflected from the PV surface. According to some embodiments, the index of refraction at lower surfaces can be altered so as to increase internal reflections that may, for examples, increase the number of passes light makes through an absorbing region.

[00223] According to some embodiments, random voids can also be generated by dry etching/electrochemical etching the surface of the semiconductor without any mask. Generating semiconductor nanowires followed by epitaxial regrowth on these random nanowires will result in buried voids. As discussed in Frajtag et al,

Growing thin films that contain embedded voids, 23 June 2011, SPIE Newsroom; DOI: 10.1117/2.1201105.003750, this method can be used in GaN light emitting diodes to minimize defect formation due to lattice mismatch of the GaN epitaxial layer with the substrate which can be sapphire, Si, SOI, IOS to name a few. The random formation of semiconductor nanowires by dry etching of the surface of the semiconductor (which can be Si, Ge, III-V material family such as InP, GaAs, InGaAs, InGaAsP, GaN, InGaN, InSb, to name a few) without any mask and subsequently regrowing on the nanowires epitaxially using CVD for example, to form random buried voids can also be used to reduce the effective refractive index of the semiconductor and reduce the effective capacitance of the P-I-N, P-I-P-I-N diodes if the voids are formed in the "I" absorption layer and/or P, N layers, and/or charge, multiplication layers of the PD, APD, in any combination to optimize the performance of the device in bandwidth, QE, and energy consumption.

[00224] Fig. 31 is a cross section showing regrown I-Ge with a buried/embedded voids, according to some embodiments. The regrowth of Ge 3104 epitaxially on Si microstructured pillars and/or holes results in voids 3102 in the Ge layer that can be intrinsic or non-intentionally doped or low doped using the method shown in FIGs. 27-28, *supra*. In addition, selective masking with dielectric such as SiO_x, SiN_x for example can be used to generate nanowires only in the selected areas such as the Ge regrowth, for example, and with additional regrowth of Ge, random voids can be buried only in the selected Ge areas. The random voids can be combined with patterned voids to optimize a device performance in terms of bandwidths, quantum efficiencies and power consumption. The microstructures shown in FIG. 31 combine the Ge microstructure and void microstructure to enhance to bulk absorption coefficient and reduce the effective capacitance of the diode.

[00225] Fig. 32 is a cross section showing a device having buried microstructured voids in I-Si with regrown I-Ge and capped by an epitaxial layer, according to some embodiments. As can be seen in FIG. 32, the buried/embedded microstructure voids 3202 can be in I-Si layer 3200 while the Ge microstructure 3104 is also buried/embedded in Si layer 3200 using a few additional processing steps. First the voids 3202 are buried/embedded as in FIG. 28 with or without the P-Si anode layer 3226. Microstructures are then again

etched into the I-Si layer 3200 with the voids and then Ge 3104 is regrown resulting in a microstructure with voids 3202 in the Si layer 3200 and a Ge microstructure 3104 to enhance the bulk absorption coefficient and reduce the capacitance of the diode. Not shown is that the microstructured voids can also be buried/embedded entirely in Ge for Ge on Si layers, such that in Fig. 28, if the I-Si layer 3200 is replaced with I-Ge followed by a P⁺ Ge capping anode layer 3226.

[00226] The buried/embedded microstructure voids is an inverse HCG structure with absorption, or a lossy HCG structure, and can have resonance, constructive and destructive optical interference effects of both phase and amplitude that can result in the enhancement of the bulk absorption coefficient. The period of the microstructure pillar, hole, void, buried/embedded Ge arrays can fall in the near-wavelength regime of the HCG effect or it can fall in the subwavelength regime where the grating period is much less than a wavelength and the diffraction regime where the period is greater than a wavelength. The HCG characteristics of the microstructure array and the input optical signal can be coupled to in-plane optical modes. The microstructured arrays can also behave as a lens to mode match the incoming optical signal. Good coupling efficiency also improves the overall QE of the PD/APD. According to some embodiments, a lossy HCG is provided where the absorbing region is a part of or included in the HCG structure (other effects such as scattering, near field, plasmonic, resonance, linear and non-linear optical effects to name a few, can also play a significant role in absorption enhancements), and where Si can be the HCG for photon energies that are below the Si bandgap and the Ge microstructures are buried or embedded within the Si that is absorbing to the photons with wavelength ranging from 950-1800 nm (where Si has relatively low optical losses).

[00227] According to some embodiments, the microstructures of holes, pillars, and voids can be arranged in any pattern or no pattern in the active area, including any parts of the P-I-N structure of a PD or P-I-P-I-N structure of an APD; the active area includes the absorbing "I" region and the P and N regions. According to some embodiments, to simplify manufacturing and to improve yield, the microstructures can extend outside the active areas of a PD/APD if it does not interfere with the PD/APD operations and performance. FIG. 33 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some

embodiments. The microstructure array 3300 consists of pillars, holes, and/or voids, and buried/embedded Ge in Si or Si in Ge or any combination of multiple semiconductors, can be distributed over the entire active area 3302 of the photodiode or avalanche photodiode or just partially for example in the center

5 where the optical intensity is the highest. The active area can be defined as any area that contributes to the generation of electrical signal upon illumination with optical signal, or in the case of a PV, the generation of electricity upon illumination with photons. In FIG. 33, the active area 3302 is commonly the area within the metal ohmic contact/bond metal ring 3304. The distribution of the array 3300 can
10 be non uniform, non periodic, non uniform is size of the microstructure, or in shape.

[00228] FIG. 34 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some other embodiments. In FIG. 34, the QE is optimized at the center of the active area where the optical intensity is the highest and away from the center, more semiconductor material is
15 removed in the microstructure pattern to reduce the capacitance of the active area in order to decrease the RC (resistance, capacitance) time constant to achieve higher bandwidth for the PD/APD and or to increase the active area to allow passive alignment of the optical signal to the PD/APD thereby reducing the cost of packaging and assembly. Microstructured pillars/holes/buried voids 3400 near the
20 center of the PD/APD optimize QE while the microstructured pillars/holes/buried voids 3410 at the periphery of active area 3402 minimize capacitance while still maintaining good QE.

[00229] Buried voids in the N (or P if P and N are switched) part of the P-I-N or P-I-P-I-N diode structure can reduce the effective refractive index of the

25 semiconductor in the N layer. This is useful in increasing the refractive index contrast for HCG structures (to include other possible optical effects that may be significant in absorption enhancements such as scattering, plasmonic, near field, linear and non-linear optical effects to name a few), for example in Si the refractive index is approximately 3.5 (for wavelengths 950-1800 nm) and if half of the volume
30 of the material is air, then the effective refractive index ($1/2$ air and $1/2$ Si) would be approximately 1.8 for the air-Si composite material. Any semiconductor microstructures of pillars or holes fabricated on top of this composite air-Si material will have a index contrast of, for example Si pillars on the composite air-Si layer,

approximately 2. The high index contrast would enhance the performance of the HCG. According to some embodiments, this is used to enhance the lossy HCG performance (where loss can be as high or higher than - 1 dB/cm) and enhance the absorption coefficient with its resonance, light concentration and in-plane light coupling effects to name a few. There is an advantage in having the voids in the N and or N⁺ layers since it will have a minimal effect on the electrical properties and characteristics of the diode since once electrons are swept into the N and or N⁺ layer, they are majority carriers.

[00230] The microstructured voids in the N and or N⁺ layer can be patterned, non-patterned or random or pseudo-random, and can be defined using lithography, masking and etching or just etching followed by a regrowth of Si, or Ge or any other material. The voids can range in length approximately from 0.01 to 10 micrometers and lateral dimensions can range approximately from 10-5000 nm with spacing between adjacent voids ranging approximately from overlapping to 5000 nm.

[00231] Fig. 35 shows the basic epitaxial structure 3500 for a conventional Si PV/PD diode on N Si substrate. FIG. 36 shows the structure of FIG. 35 with microstructured voids incorporated into the N-Si layer, according to some embodiments. The doping and thickness of the layers are dependent of the applications. For high bandwidth PD applications the "I" Si thickness ranges from 0.1 to 3 micrometers whereas for PV applications the "I" Si thickness ranges from 1 to 20 micrometers with doping range of intrinsic or not intentionally doped, background doping of $< 5 \cdot 10^{16} \text{ cm}^{-3}$. Device size to define the area of the capacitance for high bandwidth PD (for circular apertures) ranges from 5 to 100 micrometer diameter whereas for PV, the lateral dimension can range from 0.1 to > 50 cm (centimeters) limited only by the size of the wafer or substrate. The doping ranges and layer thicknesses for non "I" layers are similar for PV, PD and APD; P or P⁺ layer thickness ranges 0.1 to 3 micrometers P doping $> 5 \cdot 10^{18} \text{ cm}^{-3}$, N or N⁺ layer(s) thickness ranges of 0.1 to 10 micrometers N doping $> 1 \cdot 10^{17} \text{ cm}^{-3}$. The Si substrate can be N doped, low N doped or undoped.

[00232] After growing the N/N⁺ layer(s) on the Si substrate, microstructures of pillars and or holes and or nanowires are etched into the N/N⁺ layer(s) 3604 and followed by a N/N⁺ layer(s) regrowth resulting in buried voids 3622 as shown in Fig.

36. The regrowth surface may or may not need further planarization such as using chemical mechanical polishing (CMP). Some applications may have more optimal performance with a non-planar surface, for example PV that can couple sun light in multiple angles with minimal reflections (a rough surface reflect less light).

- 5 Subsequent "I" Si layer 3606 and P/P⁺ layer 3608 are grown on the N/N⁺ layer(s) 3604 with the buried voids 3622. In addition to reducing the effective refractive index, at wavelengths where Si has low loss (approximately -1 dB/cm or less), 950-1800 nm, the buried voids 3622 can be patterned into a reversed HCG and behave as a very reflective (close to 100% reflectivity) broad spectrum mirror for any
- 10 photons illuminating from the top (P side) and not absorbed in the "I" microstructured pillar/hole region on the first pass, the photons can be reflected back toward the absorbing "I" region. In addition, with the voids, the substrate may be more flexible and lightweight such that it can be more adaptable to contoured surfaces and/or for use where weight is an issue such as a solar panel, or for
- 15 mobility.

[00233] FIG. 37 is a cross section showing etched Si microstructured pillars/holes with regrown Ge covering the Si, according to some embodiments. The starting structure is the same as layers 3500 in FIG. 35. The Si microstructure pillar and/or hole arrays are etched with a depth ranging from 0.1 to 10

20 micrometers and subsequently regrown with a I-Ge layer 3702 of thickness 0.01 to 4 micrometers including according to some embodiments a 1-10 nm low temperature buffer Ge layer to account for lattice mismatch between the Si and Ge. Note that the Ge buffer may not be included for pillar hole lateral dimensions of approximately 1000 nm or less since the lattice mismatch strain at that small area

25 may not be significant to cause extensive defects to form. The lateral dimensions of the microstructured pillars 3704 and holes 3706 range from 10 to 5000 nm and spacing of adjacent elements from overlapping to 5000 nm. The P/P⁺ Si layer 3708 is left on in FIG. 37 as it may be useful in making good P ohmic contact with the ohmic metals of Ti, W, Al silicide that are 1-50 nm thick to be semitransparent or

30 transparent transition metal silicide.

[00234] FIG. 38 is a cross section showing microstructured Si pillars/holes with Ge regrowth on an N-Si layer having embedded microstructured voids, according to some embodiments. The structure shown in FIG. 38 is similar in starting

material as shown in FIG. 36. The buried voids 3822 in the N/N⁺ layer 3804 act to reduce the effective refractive index of layer 3804. The voids spacing and lateral dimensions can be subwavelength ($< \lambda$) or even deep subwavelength ($<< \lambda$) to minimize optical scattering loss such as Rayleigh scattering which is proportional to λ^{-4} where λ is the wavelength. The wavelength of interest range from 300 to 1800 nm.

[00235] FIG. 39 is a cross section showing partial coverage I-Ge on microstructured Si pillars/holes, according to some embodiments. In the variation of the microstructure shown in FIG. 39, instead of regrowing I-Ge over the entire Si microstructured pillars and holes, it is only grown on part of the Si microstructures. Part of the Si microstructure is without I-Ge and the other part has regrown I-Ge. The partial regrowth of Ge can be accomplished by partially covering the Si microstructure with a dielectric such as SiO_x or SiN_x by directional deposition such as electron beam evaporation deposition, or directional laser ablation deposition or other directional methods such as ion milling to remove native oxide of Si selectively or ALD thin layer of oxides/nitrides and removing selectively and directionally with ion beam milling. Once the Si microstructure is partially coated with an oxide or nitride (or other dielectric such as CaF_x, TaO_x, TiO_x, to name a few) Ge epitaxial regrowth will predominantly occur where there is lattice information such as a Si surface. The I-Ge regrowth 3902 thickness can range from 0.1 to 4 micrometers or more. The Si microstructure of pillars 3904 or holes 3906 can have a depth of 0.1 to 10 micrometers and a lateral dimension of 10 to 5000 nm and spacing between adjacent microstructures of overlapping to 5000 nm. Both Si and Ge microstructures are exposed to photons with wavelengths ranging from 300-1800 nm from photons impinging from the anode surface and impinging on the sidewalls of the microstructure directly, scattered, near field, resonance, HCG effect, linear and non-linear optical effects, and with enhanced absorption coefficient. Both Si and Ge will generate photocurrent due to the incident photons. The Si current generator and Ge current generator are in parallel and the total photocurrent generated by this PD/PV is the sum of the Si and Ge photocurrent generators. The buried voids 3922 reduce the refractive index of the N/N⁺ layer 3914 and improve the index contrast of the microstructure and the substrate thus improving the performance of the lossy HCG for enhancing the absorption

coefficient. The voids 3922 in the Si 3914 can also behave as a good reflector to reflect photons back toward the "I" absorbing layer for a double pass (for photons illuminating from the top side). BOX or SOI 3912 can also be used in addition with the buried voids or without the buried voids, as the refractive index of SiO₂ is approximately 1.54, roughly half that of silicon at infrared and near infrared wavelengths.

[00236] FIG. 40 is a cross section showing the basic components for a microstructured Si-Ge pillar hole array PD/PV and/or APD, according to some embodiments. Note that the APD multiplication layers are not shown for simplicity.

Only the very basic parts of the device is shown. After processing steps shown in FIG. 39 are completed, surface passivation is carried out using thermal oxide or ALD or PECVD or CVD deposition of oxide or nitride to passivate or SiGe as a passivation layer on Ge. A filler 4002 is spun on or deposited such as spin-on-glass, or SiO_x, SiN_x by PECVD or CVD. Using RIE to etch back to expose either the Ge or P/P⁺ Si (during i-Ge epitaxial growth, the P dopant in the P/P⁺ Si may diffuse into the Ge layer to also result in a P/P⁺ Ge layer). Ge and or Si P- ohmic material may be Al, W, AuGe, Au, Au/Ti and Al, TiN, Pt, transition metal-silicide respectively; ohmic contacts to P and N semiconductors are well known in the literature and art and these are only a few examples of possible ohmic contacts. A transparent conducting oxide (TCO) 4004 such as indium tin oxide (ITO) may be used to further reduce the series resistance of the anode. For microstructured holes, since the P/P⁺ layers are contiguous, TCO 4004 may not be used and only a perimeter (ring for circular apertured PD/APD/PV) border ohmic contact and metallization 4006 may be used instead to reduce series resistance of the ohmic contact, such as Al, Au/Ti. Cu, to name a few. Anti-reflection layers are not shown for simplicity. N ohmic material can be used on the substrate or on the N/N⁺ layer together with metallization. Al, Pt, transition metal silicide, followed with Al or Au deposition (e-beam, sputter, thermal evaporation) on the ohmic contacts reduce series resistance. Ohmic contacts normally use an annealing process that is well known in the art. Bond and/or connecting metallization 4006 is deposited (using standard processing methods) to complete the PD/APD/PV device. Sunlight/optical signal is illuminated from the top (anode) of the device normal to the surface or at any angle off normal and may be rotated to optimize the QE. At wavelengths where

Si is low loss (950-1800 nm or more) the buried voids can both reduce the effective refractive index of Si and act as a reflector to reflect photons that are not absorbed back toward the absorbing region. The surface of the N/N⁺ layer 3914 can be non-planar to help diffuse the reflected photons to optimize its absorption in the

5 microstructured Si and Ge array. A contact pad 4008 can be provided, for example, on the side of layer 3914 as shown. Although many of the embodiments show the microstructures of Si and Ge, Si, Ge are normal to the surface (vertically aligned) and straight, according to some other embodiments if the N/N⁺ surface is non-planar, subsequent layers may also be non-planar. Etching (wet chemical or
10 dry RIE, DRIE) may result in microstructures that are off normal and not straight (with bends) which may further improve the absorption of photons. Due to the non-planar topology of the surface, the microstructures may have various orientations depending on the orientation of the crystal within the same device. The different orientations of the microstructures are advantageous to capturing photons that may
15 be illuminating the surface of the device at different angles, for example for PV as the sun changes position in the sky and for PD/APD for applications where multiple optical signal may illuminate the PD/APD from different angles/directions.

[00237] Microstructured Si pillar and/or hole arrays/pattern/random PD shown in FIG. 5, *supra*, can also have buried voids in the N/N⁺ layers as shown in FIG. 10 to
20 both reduce the refractive index of Si so that the microstructures of Si pillars/holes are more optimized as lossy HCG by increasing the refractive index contrast and also as a HCG reflector in Si for wavelengths where Si has low loss, 950-1100 nm for this application as a wide bandwidth (> 5 Gb/s) PD or as a PV.

[00238] The Si substrate in all the embodiments described herein can be either
25 Si with doping, not intentionally doped, low doping, or buried oxide (BOX) or silicon on insulator (SOI) where the silicon layers again can be doped, heavily doped, lightly doped or not intentionally doped. The BOX and SOI layers allow the removal of the all or almost all of the Si substrate to reduce optical losses, increase mechanical flexibility and also the refractive index of SiO₂ in BOX and SOI have
30 refractive index of approximately 1.54 in the infrared and near infrared wavelengths which is roughly half of silicon refractive index. The low index of SiO₂ also improves the performance of HCG, or the silicon dioxide layer can be removed for bottom illuminated PD/APD/PV.

[00239] FIGs. 41A-41B are cross sections showing aspects of a microstructured pillar/hole array device above a N-Si layer having buried microstructured voids, according to some embodiments. The bulk layers 4100 shown in FIG. 41A include I-Si layer 4112 and N-Si layer 4110. Microstructured voids 4102 are formed in the N-Si layer 4110 using techniques such as described herein *supra*. The structures in FIGs. 41A and 41B are a version of the PDs/PVs shown in FIGs. 25A-B but with buried voids 4102 in the N/N⁺ layer 4110 to improve the refractive index contrast for lossy HCG (microstructures of Si and Ge) and to provide a reflector low loss HCG for photons. Pillars 4124 and/or holes 4122 arrays are formed in I-Si layer 4112. I-Ge is regrown in the etch region 4122 resulting in a buried/embedded Ge "I" layer with microstructure voids 4102 in the N Si layer 4110 to reduce the effective refractive index of Si and/or to reflect photons entering from the anode surface at wavelength where Si is low loss (950-1800 nm). Cap layer 4126 can be P-GE or P-Si regrowth. In the case of bottom illumination, an anti-reflection coating 4130 may be provided.

[00240] FIGs. 42A-42D are cross sections showing aspects of an APD with microstructured pillar/hole arrays above an N-Si layer having buried microstructured voids, according to some embodiments. The APDs shown in FIGs. 42A-42D are versions of the APD shown in FIGs. 24A and 24B, *supra*, except that buried voids 4202 are included in the N/N⁺ layer 4210 to improve the refractive index contrast for lossy HCG (microstructures of Si and Ge) and to provide a reflector low loss HCG for photons. According to some embodiments, BOX/SOI Si wafers can also be used with or without buried voids to improve refractive index contrast for optimal HCG lossy operation. Only the basic structures are shown for simplicity. Electrical isolation, passivations, ohmic metallization, anneal, anti reflections, bond/interconnect metallization, guard rings, to name a few are not shown. FIG. 42A shows the bulk layers 4200, which include N-Si layer 4206, I-Si layers 4208 and 4212 and P-Si layer 4210. Microstructured voids 4202 are formed in the N-Si layer 4206 using techniques such as described herein *supra*. As in the case of FIG. 41B, I-Ge is regrowth in the etched area 4222. The voids 4202 are to reduce the effective index of the N-Si since the optical field will be an average effective refractive index composing of air and Si. If the voids 4202 are patterned for HCG effect, photons can be reflected that are not absorbed in the first pass

through the "I" absorbing region 4212 for photons illuminating the APD 4220 from the top or anode surface. The APD can also be illuminated from the bottom or cathode side.

[00241] FIGs. 42C and 42D show another variation of an APD 4230 in which
5 voids 4204 are formed in the I-Si multiplication layer 4208 as well as in N⁺ layer 4206 to reduce the effective refractive index and capacitance of those layers. Note that the elongated nature of the microstructured voids will have a minimal effect on charged carrier transport in the semiconductor materials. According to some
10 embodiments, voids of various shapes and densities can be formed in the P anode, N cathode, P charge, and/or I multiplication layers of the APD in addition to the absorbing I layer. The addition of voids in the I multiplication layer 4208 and the I absorption layer 4212 can reduce the effective capacitance resulting in a short RC time constant for the device. The voids 4204 in the multiplication I Si layer 4208
15 also reduce the effective refractive index, which is helpful in enhancing the absorption coefficient in a HCG absorbing mode.

[00242] Epitaxial growth/regrowth/overgrowth/selective area growth/epitaxial lateral over growth of Si, Ge, SiGe, III-V such as InP, GaAs, GaN, InGaN, InGaAs, InGaAsP, InSb, heteroepitaxy, homoepitaxy, heterogeneous epitaxy to name a few, using chemical vapor deposition (CVD), metallic organic chemical vapor
20 deposition (MOCVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE), gas source molecular beam epitaxy (GSMBE) plasma enhanced chemical vapor deposition (PECVD), laser ablation deposition (LAD) to name a few, are well known in the art.

[00243] According to some embodiments, material other than Si and Ge on Si
25 are used. For example, the techniques described herein can be applied to all combinations of Si, Ge, III-V and II-VI material families and substrates.

[00244] FIGs. 43-46 are top views illustrating various dimensions, spacings and shapes for microstructured elements, according to some embodiments. FIG. 43 shows a microstructured pillar and/or hole array 4300 (also applicable to
30 embedded or buried voids) that is uniformly spaced with a fixed diameter ranging from 100-5000 nm and a spacing ranging from 100-10000 nm. The pillars and or holes can be formed in or using: Si, Ge, SiGe, or other materials such as III-V or II-VI material family. Examples includes: GaAs, InP, InGaAs, InGaAsN, InGaAsP,

InAs, GaN, InGaN, ZnTe, CdS, ZnSe, and HgTe. According to some embodiments, the microstructures can also be formed in or using absorbing polymers, glass, and/or ceramics.

[00245] FIG. 44 shows a microstructured pillar and/or hole array 4400 having a fixed diameter but with non-uniform spacing such as aperiodic or a mixture of periodic and aperiodic or random/pseudo random spacing or a mixture of random/pseudo random, periodic and aperiodic. According to some embodiments, the arrays can also be uniformly spaced periodic but with varying diameter. FIG. 45 shows a microstructured pillar and/or hole array 4500 having both variable diameters (ranging from 100 nm to 5000 nm) and variable spacing (ranging from 100 nm to 10000 nm). According to some embodiments, the variations can be random/pseudo random, or a pattern or a mixture of patterns or any combinations thereof. FIG. 46 shows a microstructured pillar and/or hole array 4600 having various shapes such as oval, circular, rectangle, doublets, triplets, and stars. In general, any shape that can be generated using a photolithographic mask, or e-beam direct write or that can be generated with a mold for imprint lithography, can be used. The pillar/hole arrays can also have a combination of different shapes and spacings, as well as variations in the depth of the microstructured holes or lengths of the microstructured pillars/mesas. The variations can be periodic, aperiodic, or random (or a mixture of periodic, aperiodic and random) within a single array.

[00246] According to some embodiments, for some applications an array dimension of Si or Ge or III-V microstructured pillars or holes of length 2 μm approximately (or depth of 2 μm approximately) with diameter of pillar/hole of 390 nm approximately and center to center spacing of 1060 nm approximately has been found to be suitable for enhancement of the absorption coefficient of greater than 50X.

[00247] According to some embodiments, the material can be Si, Ge, SiGe, Ge on Si, III-V, II-VI, III-V on Si, polymer, glass, ceramic and any combination thereof. Examples of III-VI and II-VI are InP, GaAs, AlGaAs, AlAs, AlInAs, InGaAs, InGaAsP, InAs, InGaAsN, InN, GaN, InSb, ZnSe, ZnTe, HgTe, and CdS. Also III-V, II-VI and group IV material such as Ge can be embedded in Si microstructures using SAG, VLS, ELOG growth methods in MOCVD, CVD, MBE, reactors.

[00248] FIGs. 47-48 are cross sections showing microstructured pillar and hole arrays having varying lengths and depths, according to some embodiments. FIG. 47 shows a microstructured pillar array 4700 having different lengths, diameters and spacing. According to some embodiments, the pillar diameters range from 10 nm to 5000 nm and the pillar heights range from 0.1 to 10 microns. FIG. 48 shows a microstructured hole array 4800 having different depths, diameters and spacings. According to some embodiments, the holes have diameters ranging from 10 nm to 5000 nm and depths ranging from 0.1 to 10 microns. The variation in lengths and etched depths can be accomplished by additional lithographic masking steps where regions are masked for longer etch or shorter etch to vary the length of the pillars and the depth of the holes. The lengths and depths can be gradually or sharply varied. A patterned grating effect can be used to further optimize the optical path lengths and increase the enhancement factor for absorption coefficient. Other uses include forming a light trap by using constructive and destructive optical interference, generating a fresnel lens, matching the mode of the optical signal, forming a filter in wavelength selectivity in wavelength division multiplexing for example, or as a wavelength selector for spectroscopy and sensor applications. It should be noted that by varying the dimensions and spacing of the microstructured pillars and holes in an array can also result in constructive and destructive optical interferences that can also increase the enhancement factor of the absorption coefficient, improve light trapping, create fresnel lens, mode matching of radiation patterns of the optical signal.

[00249] FIG. 49 shows shows a microstructured surface having a combination of both pillars and holes, according to some embodiments. Microstructure array 4900 includes pillars and holes co-existing on the same microstructured surface either globally or locally. Both pillars and holes can exist in a single array (such as shown in FIG. 49) for the microstructured photodetector, or holes and pillars can exist on separate arrays for different microstructured photodetectors. In addition, hole(s) can exist in a pillar and pillar(s) can exist within a hole and these also can be global or local. The pillars, holes, hole(s) in pillar and pillar(s) in holes can have any shape, for example a rectangular pillar within a round hole, can have any mixture thereof to optimize enhancement of the absorption coefficient, light trapping, constructive and destructive optical interference, scattering, near field effects,

linear and non-linear optical effects, subwavelengths effects, fresnel lens, wavelength selection, optical mode matching, diffraction, high contrast grating, blazed grating, high Q resonator, highly reflective mirrors using high contrast grating.

- 5 **[00250]** The microstructured pillar and hole (and variations thereof) arrays can be fabricated in Si, Ge, Ge on Si, SiGe on Si, SiGe on Ge. The array structure can be any combination of Si, Ge and SiGe. The array can be entirely Si or Ge or SiGe, or Ge on Si, or Si on Ge, or Ge on Si with SiGe on both. The structure can also include III-V and II-VI material systems together with Si, Ge and SiGe and any
- 10 combination of Si, Ge, and III-V, II-VI material systems. According to some embodiments, the array structure can also include polymer, glass, oxides, nitrides, sulfides and chlorides of transition metals, ceramics, quartz, SOI, IOS, organic conducting and non conducting polymers, carbon based material such as graphene to name a few.
- 15 **[00251]** The microstructures pillars, holes, voids, and any other shapes such as pyramids, microwires, nanowires, multiple materials, SAG microstructures, can have orientations that are not perpendicular to the surface of the substrate. They can have a single or multiple orientations that can be perpendicular and or off perpendicular to the surface. They can be random or pseudo random, single
- 20 pattern or multiple pattern orientations at any angle where angle can range from 0 to 90 degrees with respect to the normal to the silicon substrate, and they can be on sidewalls and on all three dimensions. With the microstructures at certain orientations, the photosensor can have a higher sensitivity to certain direction of illumination. Conversely, with multiple orientations and or random or pseudo
- 25 random orientations the photosensor can be mostly insensitive to direction of illumination.

- [00252]** Reducing the effective refractive index with buried voids in semiconductor has applications beyond PD/APD and PV devices. It also, for example, has applications in optical waveguides. FIG. 50 is a cross section of an
- 30 optical ridge waveguide, according to some embodiments. Waveguide 5000 uses the density of voids to alter the effective refractive index of Si. According to some embodiments materials other than Si are used, for example other semiconductors such as Ge, SiGe, any of the III-V semiconductor family, or other material such as

ceramics, glass, polymer. In Si photonic optical waveguide 5000, the ridge 5002 and slab 5004 are made of Si on a BOX (buried oxide) Si substrate 5006. Due to the high refractive index of Si. 3.49 at 1100-1800 nm wavelengths, the dimensional tolerance of the solid Si waveguide is very critical. Known Si photonic components

5 are difficult to manufacture and have low yield and are temperature sensitive. According to some embodiments, voids are buried in the Si layers. By varying the density of the voids, the refractive index of the composite Si-voids can be adjusted. In the schematic diagram of FIG. 50, a ridge waveguide 5000 has voids 5014 on slab 5004, as well as voids 5012 on ridge 5002. The density of voids 5012 in the

10 ridge 5002 is less than the density of voids 5014 in the slab 5004. The refractive index in the ridge 5002 is therefore higher than the refractive index in the slab 5004 resulting in a ridge optical waveguide. The optical mode of the waveguide 5000 is indicated by the dotted oval 5022. The lower refractive index helps in reducing the dimensional tolerance and the optical waveguide can have a larger dimension.

15 Thus, according to some embodiments, the refractive index can be varied by varying the void density making other components such as couplers easier to manufacture. The dimensions of the voids can be subwavelength ranging from 10nm to 1000nm depending on optical wavelengths.

[00253] According to some embodiments, voids are also buried in a silicon wafer

20 (including BOX/SOI silicon wafers) to adjust the effective refractive index of the Si wafer. The Si wafer with buried voids can then be the starting platform for silicon photonic circuits. It can also be the platform for large area PV cells that allow mechanical flexibility but still retain the high quality of silicon and its electrical characteristics. This can also be the platform for flexible displays and other

25 electronics that require mechanical flexibility and or light weight. According to some embodiments, burying or embedding voids is not limited to just Si, but can include Ge, GeSi, amorphous semiconductors, III-V, II-VI material families, polymers, glass, quartz, metal, alloys, ceramics and any other material that requires flexibility. In some embodiments, the voids can be filled with gas, liquid or solid for specific

30 applications. Gel such as spin on glass that does not require anneal for example can be used for impact/crack situations where the integrity of the device is compromised such as a crack due to impact, to seal surfaces such as semiconductors or any surfaces sensitive to environment such as moisture, water,

oxygen to name a few to prevent further deterioration. Voids are also excellent in preventing crack propagation.

[00254] FIG. 51 is a cross section of a buried optical waveguide in silicon using voids, according to some embodiments. A composite waveguide 5100 is formed in
5 Si substrate 5106 using Si-voids to selectively alter the effective refractive index in certain locations. The effective refractive index of Si can be adjusted precisely by adjusting the total volume of the voids in a given volume of Si. In the example shown in FIG. 51, the higher density voids 5114 surround a central region of lower density voids 5112. The optical mode of the waveguide 5100 is indicated by the
10 dotted oval 5122.

[00255] According to some embodiments, the dimension and spacing of the voids are optimized to reduce scattering losses and to provide ease of manufacturing. Also, the void dimensions and spacing can be adjusted for certain applications. For example, in HCG the dimensions and spacings are selected to
15 satisfy the near field regime where the dimensions and spacing lie approximately between the wavelength in the high refractive index material and the wavelength in the low refractive index material. In most cases, in the applications to reduce the effective refractive index, the void and the surrounding material dimensions and spacing are in the subwavelength regime where the microstructures containing the
20 voids are less or much less than the wavelength in either the high or low index material. For coupling applications, the diffraction regime may be the microstructure (voids and material) dimensions and spacing. It can also be a mixture of two or more regimes to optimize a device performance.

[00256] Array patterns can include microstructure ensembles whose distribution
25 of individual microstructures can be periodic, aperiodic, chirped, random, pseudo-random, uniform, or non-uniform in all three dimensions, orientations and spacings, (including overlapping). According to some embodiments, the patterns can include microstructures within microstructures. The terms “array” and “pattern” are used herein interchangeably.

30 **[00257]** The PD/APD are biased between the anode and cathode, to extract a broadband modulation signal greater than a gigabit per second (Gb/s) at a typical transmission line impedance is 25-50 ohms. According to some embodiments, the external bias is provided with a bias-tee connected to the transmission line to block

the RF signal from reaching the DC power supply and to block the DC from biasing the transmission line away from the PD/APD. The bias-tee basically consists of an inductor and capacitor, the inductor to block the RF and the capacitor to block the DC away from the PD/APD. External bias of -2 to -30 volts is applied depending on
5 the application, PD or APD and performance desired.

[00258] In PV mode, no external bias is applied and the PV is basically a current generator. All the electrical connections are for DC current from the PV which then connects to a converter that converts the DC current/voltage to AC current/voltage.

[00259] PV devices are in DC mode whereas PD/APD for data and tele
10 communication are all RF with modulation bandwidth ranging from 1 to 100 Gb/s. Transit time of carriers and capacitance are critical in PD and APD but not so much for PV.

[00260] The terms "modulation bandwidth" and "bandwidth" are interchangeable as used herein. Both terms refer to the modulation (e.g. of a laser or LED) where
15 an RF signal is impressed on the light. When this modulated light (also referred to as "optical signal") illuminates the PD/APD, the RF modulated signal is extracted and converted from light to electrical signal. For example, a bandwidth or modulation bandwidth of a PD/APD of 20 Gb/s means that an RF signal impressed on the laser light beam at a data rate at 20 Gb/s can be converted by the PD/APD
20 from optical to electrical with good signal integrity or signal replication. The laser/LED is the transmitter and the PD/APD is the receiver where the electrical signal can be further processed by an amplifier such as a transimpedance amplifier and the signal sent for further analysis and processing in application specific integrated circuits (ASIC) computers (CPU central processing unit), routers,
25 memories, to name a few.

[00261] According to some embodiments the applications for the microstructured pillars and or holes in Si and Ge and Si regrowth with Ge, Ge on Si, with and or without buried or embedded voids photodiodes and avalanche photodiodes, are in data and tele communications. According to some
30 embodiments, these applications include: fiber to home, local area network, data center optical interconnects board to board, on the board, rack to rack, and chip to chip, between data centers, metro area network, and optical communication for distances from less than a centimeter to over 10 kilometers or more. The

applications in consumer space also includes: game box, personal computers, tablets, mobile devices such as smart phones, animations studios, and anywhere that benefits from a bandwidth of more than one gigabit per second. Other applications of the microstructured PDs and APDs, according to some

5 embodiments, are in sensors where broadband communication is important, such as sensors for infrastructures, health, environment, oil exploration, where the sensors communicate with a remote receiver that is connected to data centers for data analysis.

[00262] Other applications of the microstructured PD and APD, according to
10 some embodiments, are in analytical instruments and optical tests and measurement instruments where high sensitivity and bandwidth are important.

[00263] According to some embodiments, the microstructured PV have applications in energy harvesting for power generation all the way from gigawatts to watts, to power cities and homes to powering sensors. Since the microstructured
15 PV is lightweight and high efficiency it can be used in mobile applications, space, solar transportation, recycling of photons in home, offices and factories. The PV can also be used on windows and can be semi-transparent.

[00264] The described microstructures in Si, Ge, Si regrowth with Ge, Ge on Si, pillars, holes, and voids can be any shape and form, and are not limited to the
20 schematics shown. According to some embodiments, the dimensions range from 10-10000 nm (nanometers). The microstructures can be within each other such as pillar(s) in hole(s), hole(s) in pillar(s) and void(s) can be in the pillar, and buried and or embedded in any layer of the semiconductor heterogeneous or homogeneous. The material used includes semiconductors such as Si, Ge, GeSi, Ge on Si, and
25 the III-V group material family of InP, GaN, InGaAsP, GaAs, and other semiconductors such as ZnO, CdTe, CuInGaSe (CIGS), amorphous Si, or any amorphous semiconductor and or microcrystalline and crystalline semiconductor. The material can be a combination of amorphous, microcrystalline, crystalline heterogeneous and or homogeneous. The material used is also not limited to
30 semiconductors, but also include polymers, electrically conducting, semiconducting, non conducting polymers, organic and or inorganic polymers, glass, conducting, semiconducting, non conducting glass. Nanoparticles of semiconductors and or metal can also be buried in the polymer and glass.

Semiconductors, polymer and glass can exist within the same microstructure, separately or in any combination.

[00265] According to some embodiments, in silicon photonic circuit applications, optical waveguides such as shown in FIG. 50, *supra*, can be integrated with optical
5 sources and optical detectors such as photodiodes, avalanche photodiodes and photoconductors. FIG. 52 is a cross section of a ridge waveguide integrated with a microstructured PD/APD, according to some embodiments. Device 5200 includes a ridge waveguide that is edge coupled to a microstructured Ge on Si photodiode or avalanche photodiode (with multiplication layers added). In the ridge wave guide
10 portion, as shown in FIG. 50, a ridge 5202 has lower density voids 5212 and slab 5204 has higher density voids 5214. Ion implantation is used to increase the N doping (region 5224) for the PD and a coplanar transmission line is fabricated on the photodiode to extract the electrical signal as shown in FIG. 53, *infra*. Anode contact 5226 is made of P-Ge, according to some embodiments. The cathode
15 contact is made to layer 5224 (cathode contact not shown for simplicity and clarity of drawing.)

[00266] FIG. 53 is a top view the integrated ridge waveguide and microstructured PD/APD shown in FIG. 52, according to some embodiments. The device 5200 is in a coplanar transmission line configuration. Ridge portion 5202 is
20 0.5 to 10 μm wide and 0.1 to 10 μm deep, according to some embodiments. Slab portion 5204 has higher density voids, as shown in FIG. 52, to vary the refractive index as a platform for silicon photonic circuits. Coplanar cathodes 5228 and 5230 are in contact with the N-Si ion implanted region 5224 shown in FIG. 52. According to some embodiments, the optical field can also be coupled evanescently by
25 placing the PD/APD above the optical waveguide such that the optical field overlaps the absorbing I microstructures.

[00267] FIGs. 54A and 54B show a microwave transmission line on Si with voids, according to some embodiments. High bit rate transmission lines on silicon suffers from a multitude of effects, from slow wave to dispersion to loss. However
30 by removing most of the silicon material with the addition of high-density voids according to some embodiments, the dispersion and loss can be alleviated and signal integrity restored. An advantage is that silicon can be the substrate for both microwave transmission line and for ICs without the use of intermediate ceramic

such as alumina for transmission line to connect various IC chips. FIG. 54A is a cross section showing high density voids 5314 buried in silicon 5304 which reduce the effective dielectric constant of the silicon, and disrupt lateral electrical conductivity which in turn can result in lower microwave loss and dispersion which are important as bit rate increases into the multi Gb/s range (e.g. 40-60 Gb/s). Coplanar microwave metallic transmission lines 5310 are provided as means to move the electrical signal to/from electronic devices (e.g. processors, storage devices, input-output devices, ASICs, CPUs, and memories) on the same substrate. FIG. 54B is a top view. Conventional techniques use multi chip carriers that need additional packaging. According to some embodiments, having many devices all on the same silicon substrate greatly reduces the cost since it can be all fabricated at once and requires no additional packaging for each chip. According to some embodiments, the voids 5314 are arranged in a fashion where the path length in silicon laterally is significantly increased in order to increase lateral resistivity. According to some embodiments, Ion implantation of protons and or oxygen can be used to further increase electrical resistivity. Although FIGs. 54A and 54B show a co-planar arrangement, according to some embodiments other microwave transmission line arrangements (e.g. microstrip, slotline, and stripline) are used with a semiconductor substrate having high-density buried voids. According to some embodiments, the positioning and/or other properties (e.g. size, shape, and filling material) of the high-density voids can be selected such that the slow wave effect can be manipulated or "tuned" in a way that is suitable for the application at hand.

[00268] FIG. 55 is a cross section of voids for thermal conduction and thermal isolation of heat producing ICs and light emitters, according to some embodiments. The buried voids in silicon 5404 can be filled with thermal conductors such as helium gas, metal such as copper, aluminum, tungsten, or ceramic such as boron nitride, or carbon, graphene, diamond like carbon, or heterogeneous material/ceramic doped with metal nanoparticles, carbon nanotubes. The voids 5414 underneath the heat producing elements such as ICs and CPUs 5422, and light emitters 5420 such as laser diodes and bipolar drivers, can be filled with enhanced thermal conductors to extract the heat from the hot components and direct it to a heat sink 5402. Voids 5412 between hot elements are kept at a low

thermal conducting state that are either in partial vacuum or filled with a gas such as nitrogen, argon, carbon dioxide, for example to prevent thermal cross talk between the hot components or to any other components where heat is not desirable. According to some embodiments, the voids are arranged in a fashion
5 such that the path length in silicon is vastly increased to maintain low thermal crosstalk. According to some embodiments, the techniques of FIG. 55 are used to keep PVs cool when exposed to the sun. According to some embodiments, thermoelectric devices can be integrated together with the voids to generate electricity from the excess heat.

10 **[00269]** FIG. 56 is a cross section showing a distribution of voids to increase lateral path length for increasing lateral electrical resistivity and decrease lateral thermal conduction, according to some embodiments. The buried voids 5602 configured for microwave transmission lines and/or for thermal management can be arranged in a randomly, pseudo randomly, or in a pattern in areas where lateral
15 electrical and thermal conductance is significantly reduced and vertical electrical and thermal conductance is significantly enhanced. There may be areas where lateral electrical and thermal conductance enhancement is desired, in which case the voids can overlap to form a conducting channel.

[00270] FIGS 57A-B are simplified partial schematic top views of a semiconductor
20 surface having holes configured as trenches, according to some embodiments. The semiconductor 3010' and 3008' can be: Si, Ge, GeSi and/or 111-V material such as InP, GaAs, GaN to name a few. In this case the microstructure "holes" are "connected" to form trenches 3060' and 3062'. The microstructure hole/trenches 3060' and 3062' are further configured to crisscross the surface of the
25 semiconductors 3010' and 3008', respectively. Although the trench-shaped holes in FIGS. 57A-B are shown in straight lines, they could alternatively be formed in curved lines or a combination of straight and curved lines. The width of each trench is approximately one wavelength, and in some cases can be less than a wavelength, and in some cases wide ranging from 600 nm to 1600 nm, and can run the length of
30 of the photosensitive area. The depth of the trench can range from 100 nm to 1000 nm or more, and in some cases 50 nm to 1000 nm or more, and in some cases 100 nm-600 nm.

[00271] This patent application refers to certain theories in explaining the nature and operation of devices, but it should be clear that such theories are based on current understanding and do not affect the actual operation of the disclosed devices even if future developments prove the theories incorrect. This patent
5 specification also refers to numerical ranges of parameters, and it should be understood that insubstantial departures from such ranges are still within the spirit of the disclosed advancements.

[00272] Although the foregoing has been described in some detail for purposes of clarity, it will be apparent that certain changes and modifications may be made
10 without departing from the principles thereof. It should be noted that there are many alternative ways of implementing both the processes and apparatuses described herein. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the body of work described herein is not to be limited to the details given herein, which may be modified within the scope and
15 equivalents of the appended claims.

CLAIMS

What it claimed is:

- 5 1. An integrated, single-chip structure of plural pillars of semiconductor material formed as respective photodetectors configured to generate electrical signals in response to illumination with light including light in the infrared and/or near infrared spectrum, said structure comprising:
- 10 deliberately formed holes into said pillars, filled at least partly with solid dielectric material;
- wherein:
- parts of at least two of the holes overlap such that at a surface of each of said pillars each of the at least two holes has a portion that overlaps with another of said at least two
- 15 holes and a portion that does not;
- said at least two holes that overlap thereby form a depression in said surface that comprises a portion of only one of said two or more holes and a portion at which two of said two or more holes overlap, and
- 20 said two or more holes have:
- depths in the range of 100-10000 nm from said surface, and
- widths in the range of 100-2000 or 100-5000 nm along said surface in at least one direction;
- 25 side-isolation comprising solid material at sides of said pillars; and
- a base dielectric region under the pillars that comprises solid dielectric material;
- wherein said pillars are configured to receive said light directly or through other materials; and
- 30 wherein the presence of said holes and side-isolation increases effective quantum efficiency (EQE) of the pillars to illumination with said light relative to an otherwise same pillars lacking said holes.

2. The integrated, single-chip structure of claim 1, wherein said at least two holes comprise at least three holes each of which has a portion that overlaps with another of said at least three holes and a portion that does not.
- 5
3. The integrated, single-chip structure of claim 1, in which said pillars comprise semiconductor material that is doped at one portion of the pillar but is less doped or is undoped at a portion of the pillar adjacent the doped portion.
- 10
4. The integrated, single-chip structure of claim 3, in which the pillars are elongated in an up-down direction and the more doped portion of each pillar is over the less doped or undoped portion thereof.
- 15
5. The integrated, single-chip structure of claim 1, further including electrical contacts to said pillars configured to provide an electrical field across said pillars.
- 20
6. The integrated, single-chip structure of claim 5, in which two or more of said pillars share one of said electrical contacts.
- 25
7. The integrated, single-chip structure of claim 1, further including active electronic circuits integrated with said pillars.
- 30
8. The integrated, single-chip structure of claim 7, in which said active electronic circuits comprises Si-based active circuits for signal processing of electrical signals generated by said pillars.
9. The integrated, single-chip structure of claim 1, in which said holes are configured as intersecting elongated trenches.
- 35
10. The integrated, single-chip structure of claim 9, in which said elongated trenches have widths no greater than a wavelength of said light at said surface.

11. The integrated, single-chip structure of claim 9, in which said elongated trenches run the length of photosensitive areas of said pillars.
12. The integrated, single-chip structure of claim 9, in which said elongated
5 trenches intersect at right angles.

ABSTRACT

Techniques for enhancing the absorption of photons in semiconductors with the use of microstructures are described. The microstructures, such as pillars and/or holes, effectively increase the effective absorption length resulting in a greater absorption
5 of the photons. Using microstructures for absorption enhancement for silicon photodiodes and silicon avalanche photodiodes can result in bandwidths in excess of 10 Gb/s at photons with wavelengths of 850 nm, and with quantum efficiencies of approximately 90% or more.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Shih-Yuan WANG et al.
Serial No.: Divisional Appln. of S.N. 18/385,213
Examiner: TBD
Group Art Unit TBD
Filing Date: TBD
For: MICROSTRUCTURE ENHANCED ABSORPTION
PHOTOSENSITIVE DEVICES

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

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PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Prior to examination and the issuance of the first Office Action, please amend the above-
identified application as follows:

Amendments to the Specification:

Please amend paragraph 0001 as follows:

[0001] This patent application is a division of U.S. Ser. No. 18/385,213, which in turn is a
continuation in-part of each of U.S. Application 18/113,474 and 17/974,325.

Amendments to the Claims:

Please rewrite the claims as follows. These amended claims replace all previously filed claims:

1. An integrated structure comprising:
 - an array of pillars comprising SI, Ge, and/or SiGe alloy semiconductor material,
 - wherein at least some of the pillars are configured as photodetectors that have respective light-receiving surfaces and respective sides;
 - wherein at least some of the photodetectors comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;
 - one or more holes that are deliberately formed at the light-receiving surface of each of at least some of the photodetectors, have elongated or other shapes at the light-receiving surfaces, extend into the photodetectors to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;
 - side-isolation comprising solid material between at least portions of the sides of at least some of the photodetectors;
 - a solid dielectric material forming a base dielectric region for the array;
 - electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;
 - wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes.
2. The integrated structure of claim 1, wherein the array of photodetectors is monolithically integrated with SI electronic devices.
3. The integrated circuit of claim 1, in which at least some of holes are elongated along the respective light-receiving surfaces.

4. The integrated structure of claim 3, wherein each of at least some of the photodetectors has a plurality of the elongated holes.
5. The integrated structure of claim 3, wherein each of at least some of the photodetectors has only one of the elongated holes.
6. The integrated structure of claim 3 in which the light-receiving surfaces have respective widths, and the elongated holes extend along less than the widths of the light-receiving surfaces of at least some of the photodetectors.
7. The integrated structure of claim 6 in which each of the elongated holes has at least one closed contour remote from respective side edges of the light-receiving surfaces of at least some of the photodetectors.
8. The integrated structure of claim 1, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors.
9. The integrated structure of claim 1, in which two or more of the photodetectors share one of the electrical contacts.
10. The integrated structure of claim 1, wherein the array of photodetectors is monolithically integrated with SI electronic devices for signal processing and transmission.
11. The integrated structure of claim 1, wherein the array of photodetectors is monolithically integrated with SI electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors.
12. The integrated structure of claim 1, in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the P-doped region before reaching any part of the N-doped region.

13. The integrated structure of claim 1, in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the N-doped region before reaching any part of the P-doped region.
14. An integrated structure comprising:
- an array of pillars comprising Si, Ge, and/or alloyed SiGe semiconductor material, wherein at least some of the pillars are configured as photodetectors that have respective sides and light-receiving surfaces with selected widths;
 - wherein at least some of the photodetectors comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;
 - one or more holes that are deliberately formed at the light-receiving surface of each of at least some of the photodetectors,
 - wherein each of the holes (i) has an elongated shape extending in length over less than the width of the light-receiving surface in which the hole is formed, (ii) has at least one closed contour at the light-receiving surface in which the hole is formed, (ii) extends into the photodetector in which the hole is formed to a depth of 100 to 10000 nm, and (iv) is filled at least partly with solid dielectric material;
 - side-isolation comprising solid material between at least portions of the sides of at least some of the photodetectors;
 - a solid dielectric material forming a base dielectric region for the array;
 - electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;
 - wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the holes; and

wherein the array of photodetectors is monolithically integrated with SI electronic devices for signal processing and transmission.

15. The integrated structure of claim 14, in which each of at least some of the photodetectors has only one of the elongated holes.

REMARKS

This patent application is a divisional of and incorporates by reference parent application Ser. Nos. 18/385,213 filed October 30, 2023, which is expected to issue as U.S. Patent No. 12,087,871 on September 10, 2024, according to Issue Notification dated 08/21/2024.

Applicant submits that through a chain of parents, the claims in this divisional application are entitled to the filing date of ultimate parent US application 14/947,718 filed November 20, 2015 (now U.S. Pat. 10,622,498) as continuation of PCT/US2014/39208 filed May 22, 2014 and provisionals to which it claims priority through the PCT application (including No. 61/834,873 filed June 13, 2013).

This patent application incorporates by reference and claims priority to each of the US, International, and Provisional applications in the chain of parents and siblings identified in the concurrently filed ADS.

Applicant invites the Examiner to telephone the undersigned if it appears that a call may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

WISSING MILLER LLP

Attorney for Applicants

By: /Ivan S. Kavrukov/

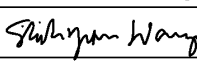
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
<p>As the below named inventor, I hereby declare that:</p> <p>This declaration is directed to: ☐ The attached application, or ☒ United States application or PCT international application number <u>18/385,213</u> filed on <u>October 30, 2023</u>.</p> <p>The above-identified application was made or authorized to be made by me.</p> <p>I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.</p> <p>I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p style="text-align: center;">WARNING:</p> <p>Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.</p>	
<p>LEGAL NAME OF INVENTOR</p> <p>Inventor: <u>Shih-Yuan Wang</u> Date (Optional) : _____</p> <p>Signature: <u></u></p>	
<p><small>Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.</small></p>	

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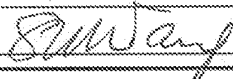
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES
<p>As the below named inventor, I hereby declare that:</p> <p>This declaration is directed to: ☐ The attached application, or</p> <p style="margin-left: 150px;">☒ United States application or PCT international application number <u>18/385,213</u></p> <p style="margin-left: 150px;">filed on <u>October 30, 2023</u></p> <p>The above-identified application was made or authorized to be made by me.</p> <p>I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.</p> <p>I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p style="text-align: center;">WARNING:</p> <p>Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.</p>	
<p>LEGAL NAME OF INVENTOR</p> <p>Inventor: <u>Shih-Ping Wang</u> Date (Optional): _____</p> <p>Signature: <u></u></p>	
<p><small>Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.</small></p>	

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Placeholder Sheet for Supplemental Content

Application Number: 18822880

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