US 20120153124A1

(19) **United States**

(12) **Patent Application Publication**

YU et al.

(10) **Pub. No.: US 2012/0153124 A1**

(43) **Pub. Date: Jun. 21, 2012**

(54) **VERTICALLY STRUCTURED PASSIVE PIXEL ARRAYS AND METHODS FOR FABRICATING THE SAME**

(75) Inventors: **Young-June YU**, Cranbury, NJ (US); **Peter Duane**, Waltham, MA (US); **Munib Wober**, Topsfield, MA (US)

(73) Assignee: **ZENA TECHNOLOGIES, INC.**, Cambridge, MA (US)

(21) Appl. No.: **12/974,499**

(22) Filed: **Dec. 21, 2010**

Publication Classification

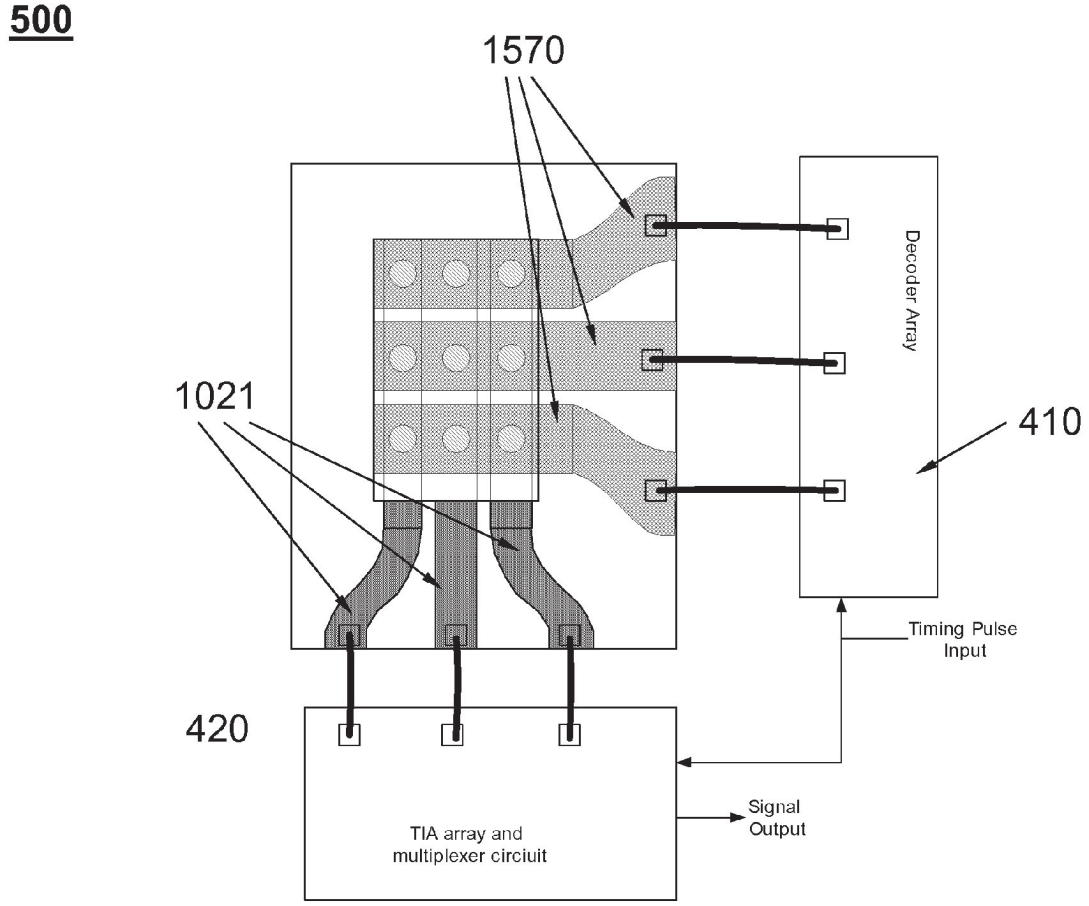
(51) **Int. Cl.**

H01L 27/146	(2006.01)
H01L 31/0352	(2006.01)
H01L 31/18	(2006.01)
B82Y 15/00	(2011.01)
B82Y 40/00	(2011.01)

(52) **U.S. Cl.** . **250/208.1**; 257/292; 438/73; 257/E31.032; 977/954

(57) **ABSTRACT**

An image sensor and methods of use the image sensor, methods of manufacturing the image sensor, and apparatuses comprising the image sensor are disclosed. The image sensor has pixels includes at least one nanopillar with a gate electrode surrounding the at least one nanopillar, wherein the at least one nanopillar is adapted to convert light impinging thereon to electrical signals and the gate electrode is operable to pinch off or allow current flow through the at least one nanopillar. The image sensor can have a plurality of pixels arranged in an individually addressable fashion. The at least one nanopillar has a cladding. A refractive index of the cladding being smaller than a refractive index of the nanopillar.



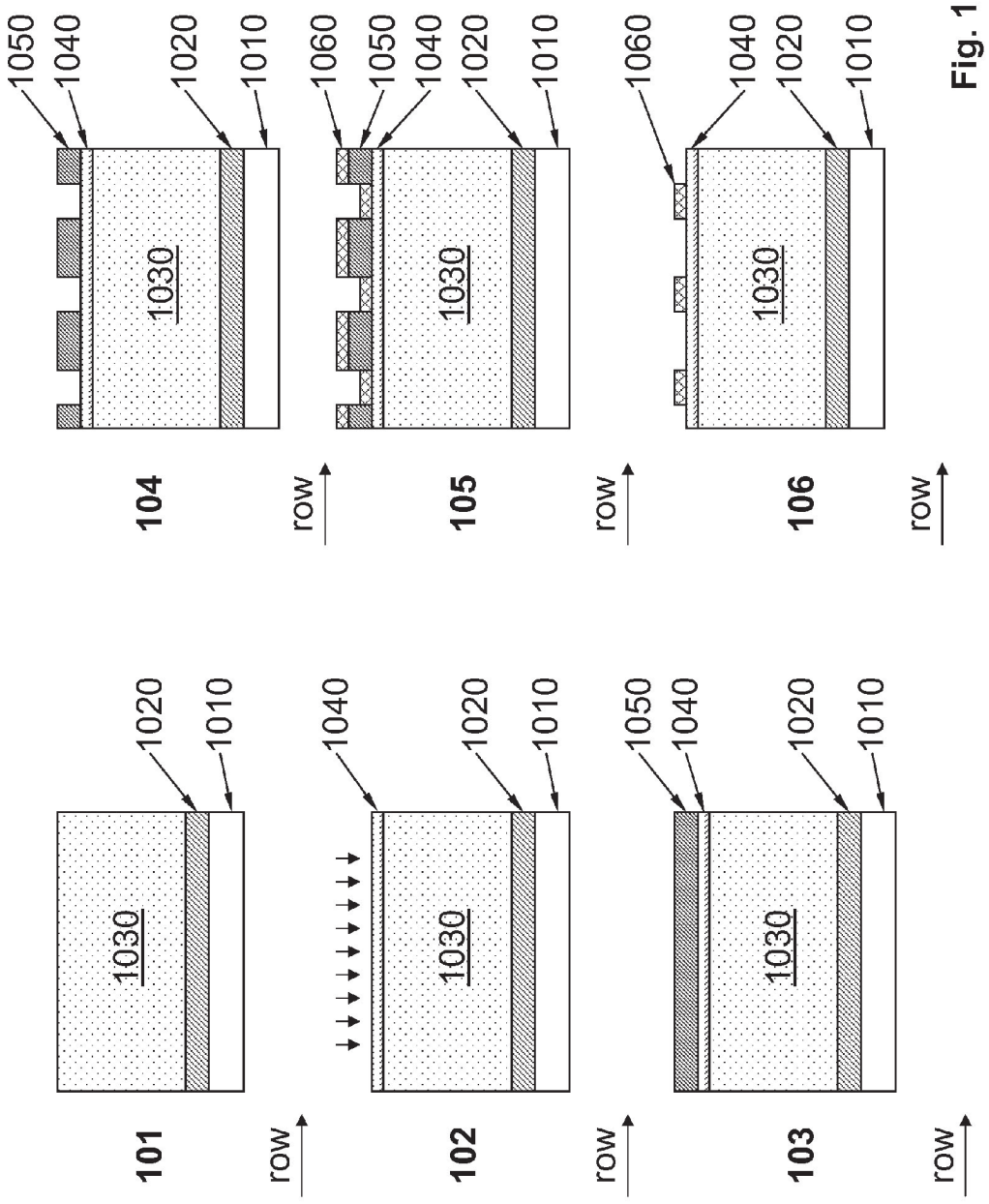

1050
1040
1020
1010
1030
104
row
1060
1050
1040
1020
1010
1030
105
row
1060
1040
1020
1010
1030
106
row
1020
1010
1030
101
row
1040
1020
1010
1030
102
row
1050
1040
1020
1010
1030
103
row

Fig. 1

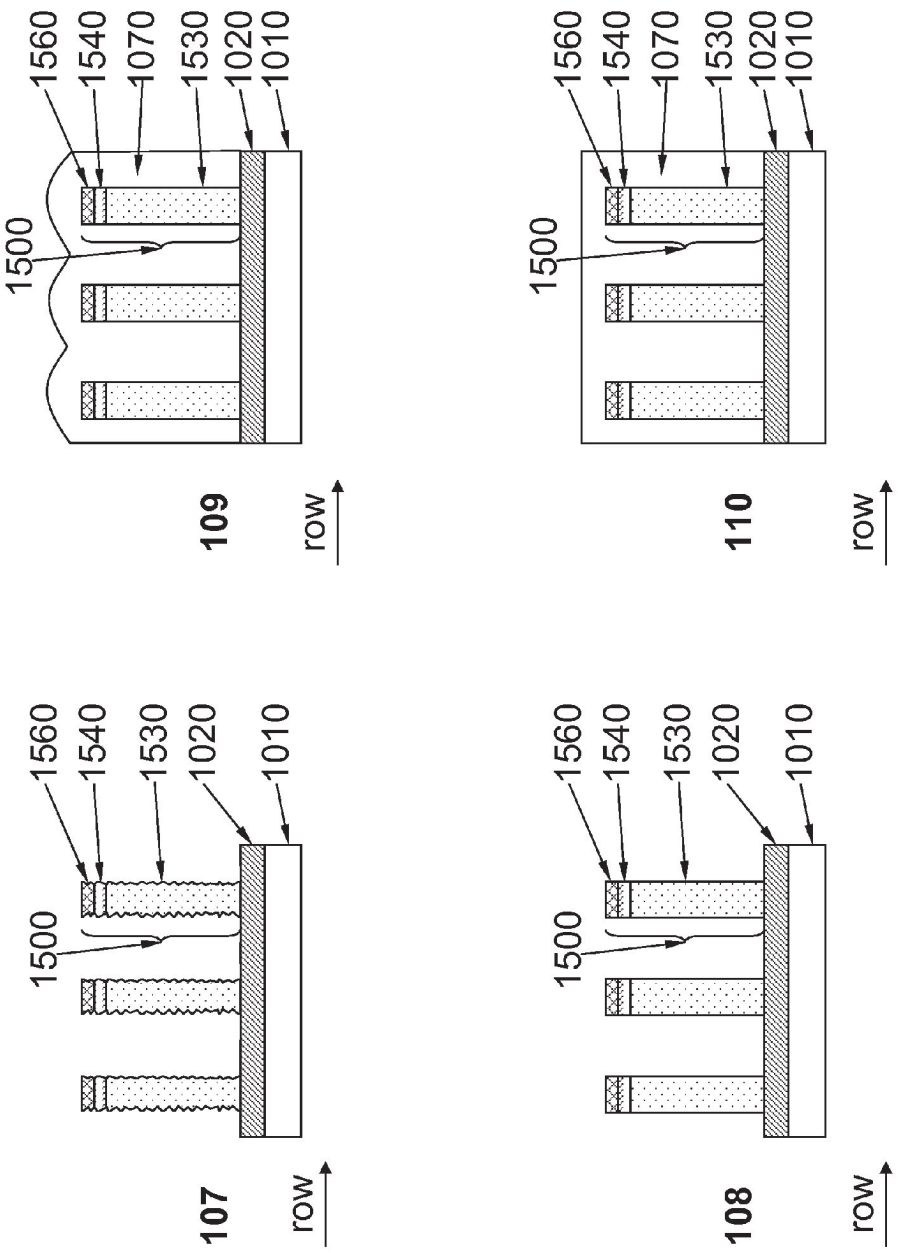

1560
1540
1070
1530
1020
1010
1500
109
row
1560
1540
1070
1530
1020
1010
1500
110
row
1560
1540
1530
1020
1010
1500
107
row
1560
1540
1530
1020
1010
1500
108
row

Fig. 1 (Cont.)

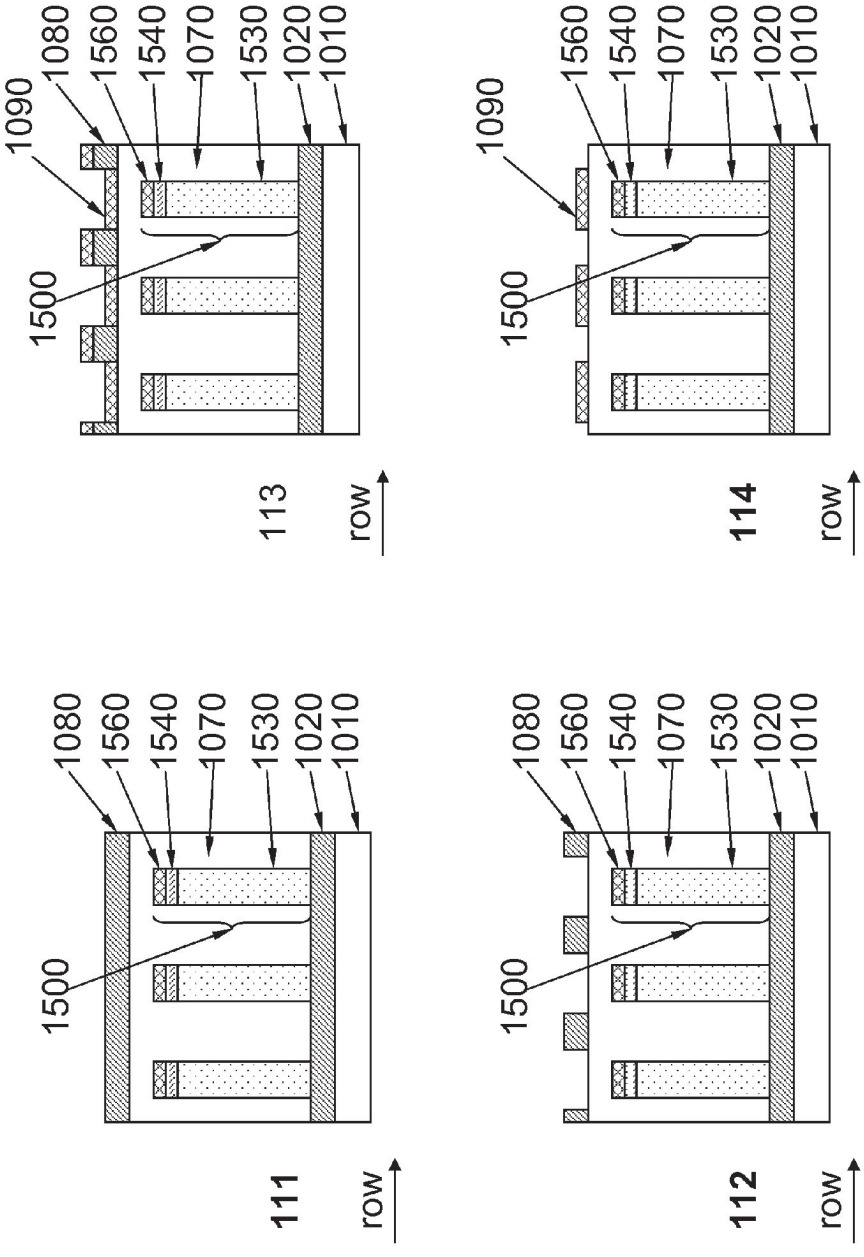

1090
1080
1560
1540
1070
1530
1020
1010
1500
113
row
1090
1560
1540
1070
1530
1020
1010
1500
114
row
1080
1560
1540
1070
1530
1020
1010
1500
111
row
1080
1560
1540
1070
1530
1020
1010
1500
112
row

Fig. 1 (Cont.)

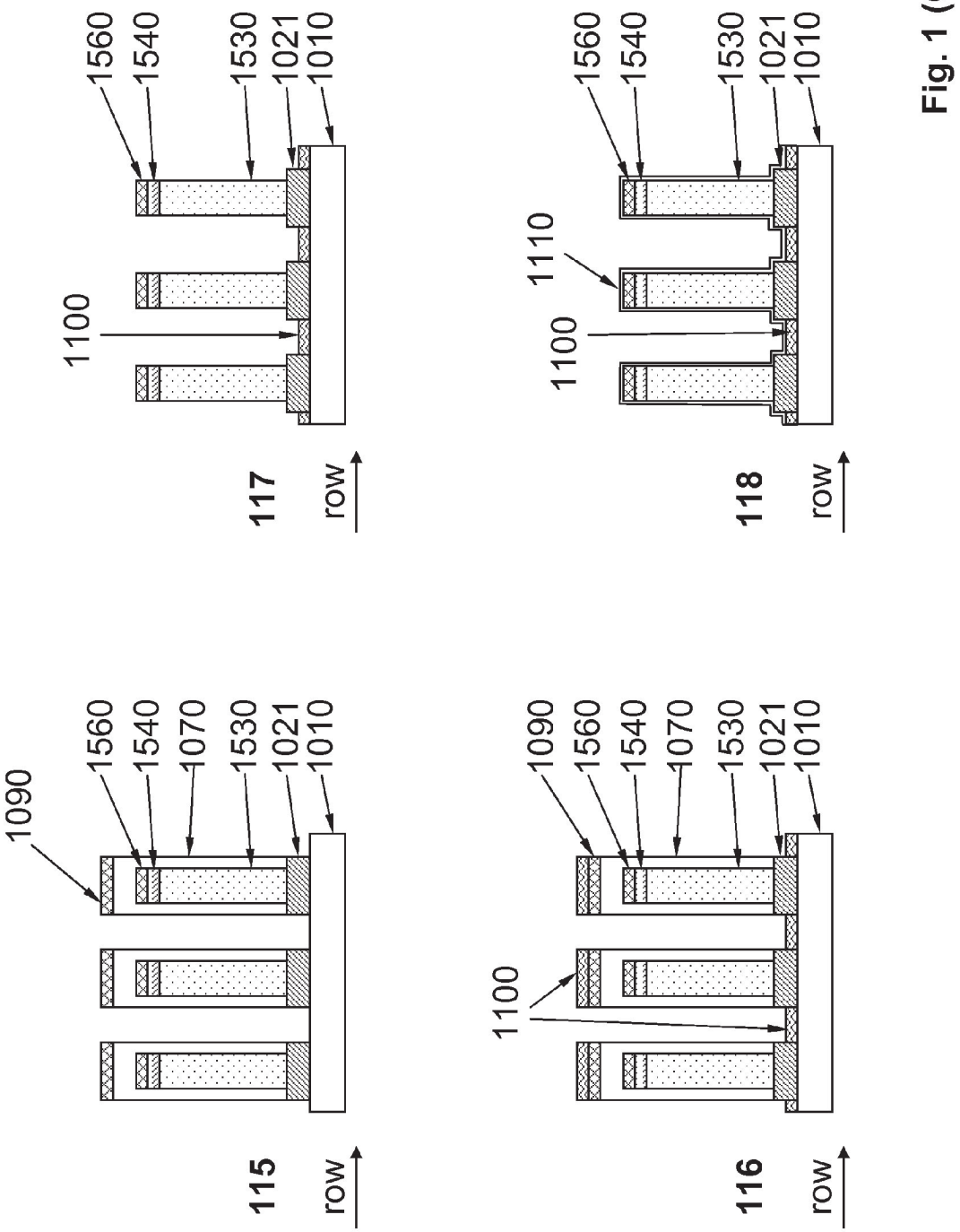

1560
1540
1530
1021
1010
1100
117
row
1560
1540
1530
1021
1010
1110
1100
118
row
1090
1560
1540
1070
1530
1021
1010
115
row
1090
1560
1540
1070
1530
1021
1010
1100
116
row

Fig. 1 (Cont.)

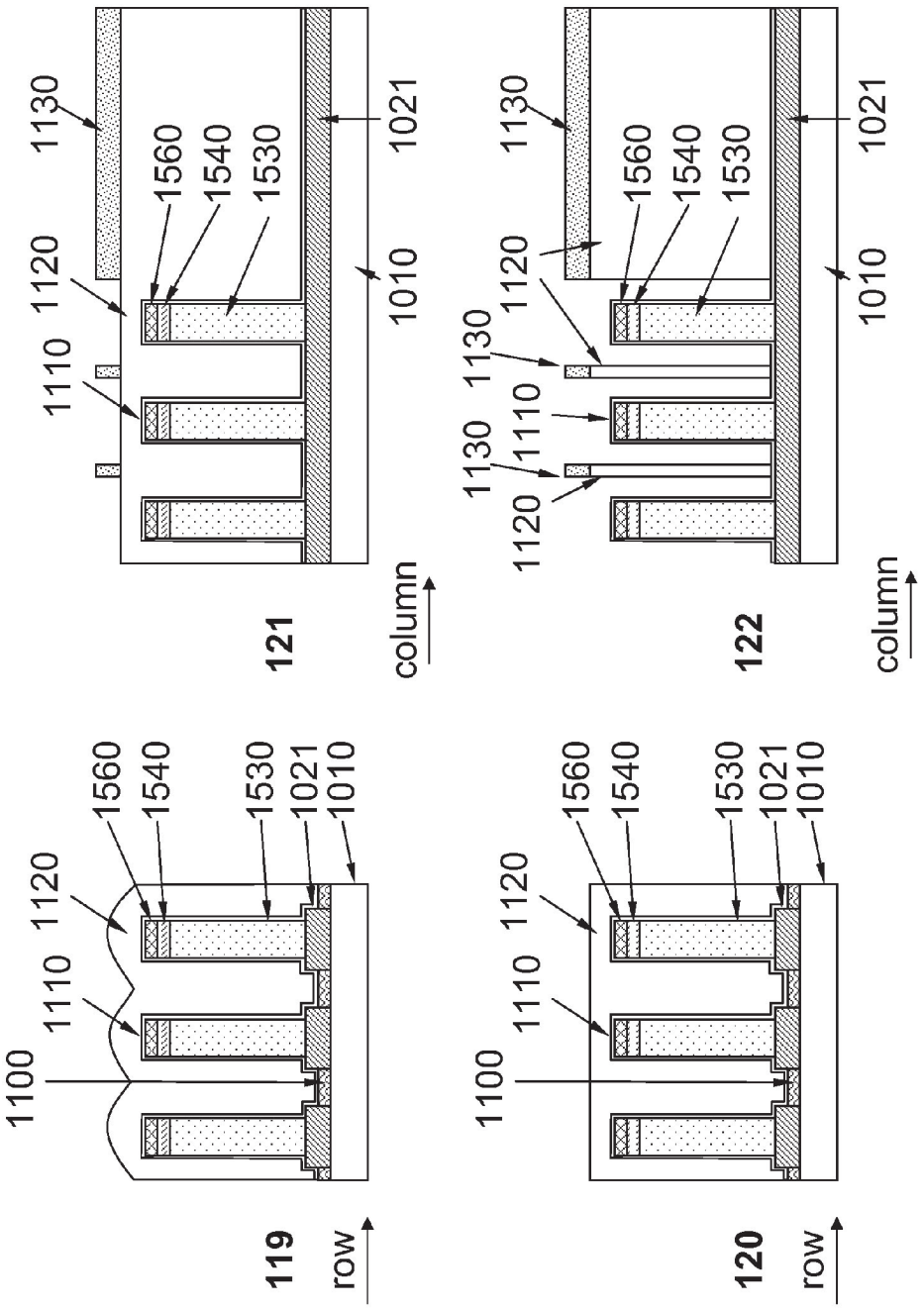
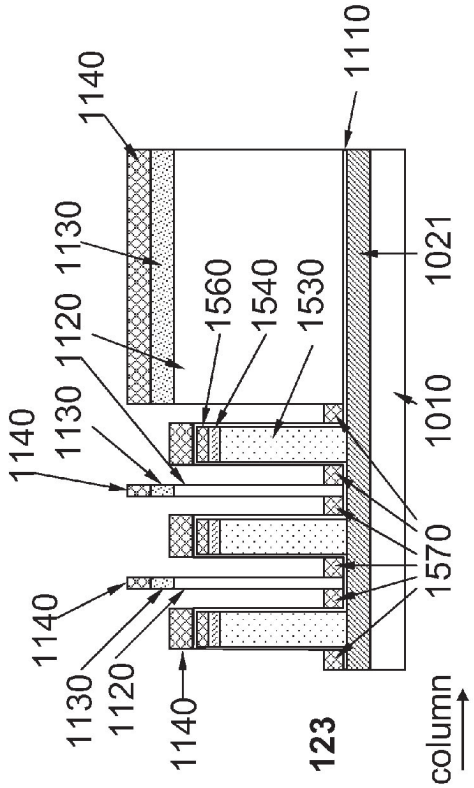

1130
1560
1540
1530
1021
1120
1010
1110
column
121
1130
1560
1540
1530
1021
1120
1010
1130
1110
1130
1120
column
122
1560
1540
1530
1021
1010
1120
1110
1100
row
119
1560
1540
1530
1021
1010
1120
1110
1100
row
120

Fig. 1 (Cont.)


1140
1130
1120
1140
1130
1120
1140
1560
1540
1530
1110
1021
1010
1570
123
column

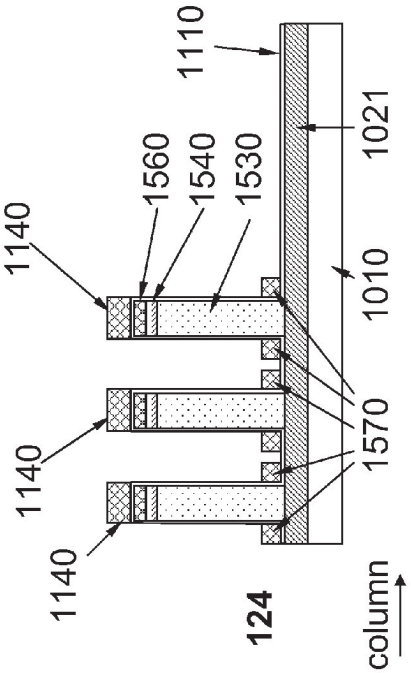
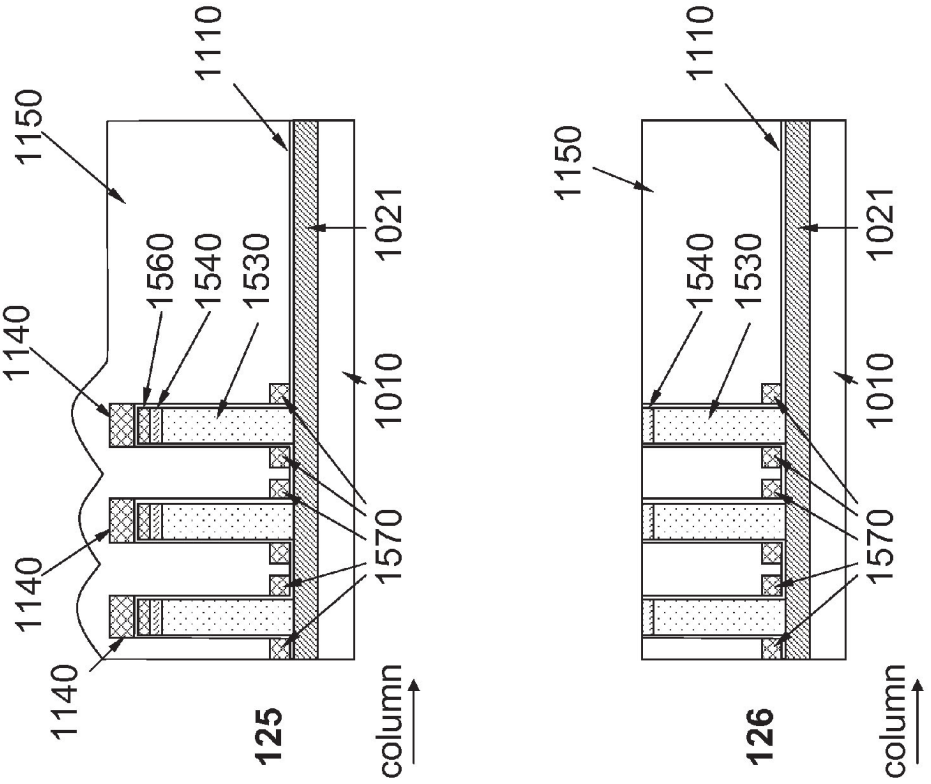

1140
1140
1140
1560
1540
1530
1110
1021
1010
1570
124
column

Fig. 1 (Cont.)

Fig. 1 (Cont.)


1110
1150
1560
1540
1530
1021
1140
1010
1570
1140
1140
125
column
1110
1150
1540
1530
1021
1010
1570
126
column

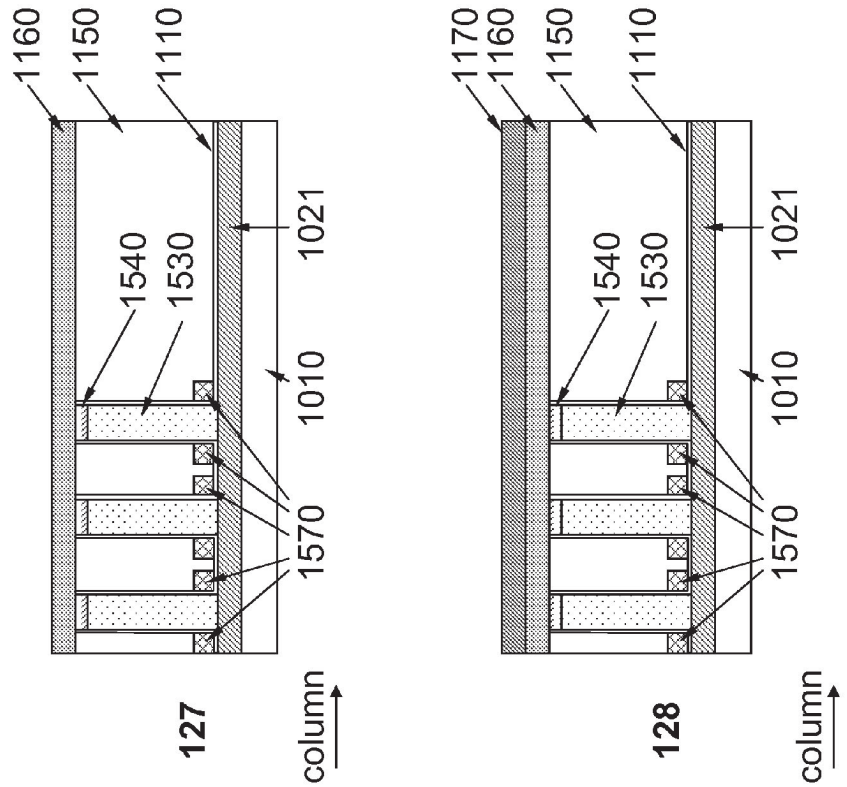

1160
1150
1110
1540
1530
1021
1010
1570
127
column
1170
1160
1150
1110
1540
1530
1021
1010
1570
128
column

Fig. 1 (Cont.)

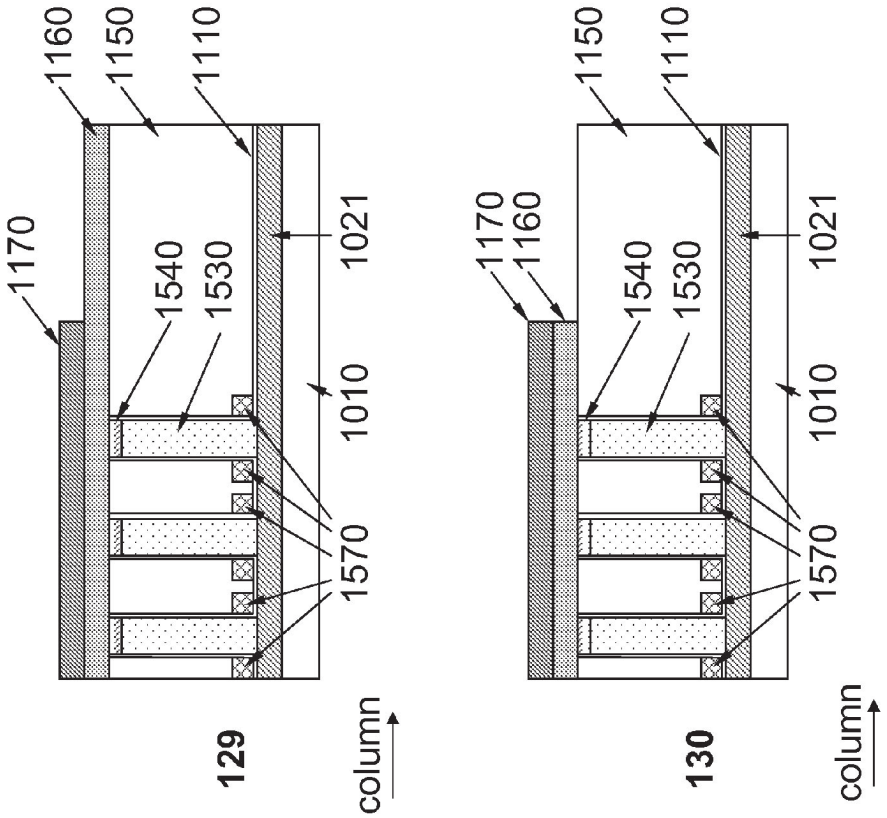
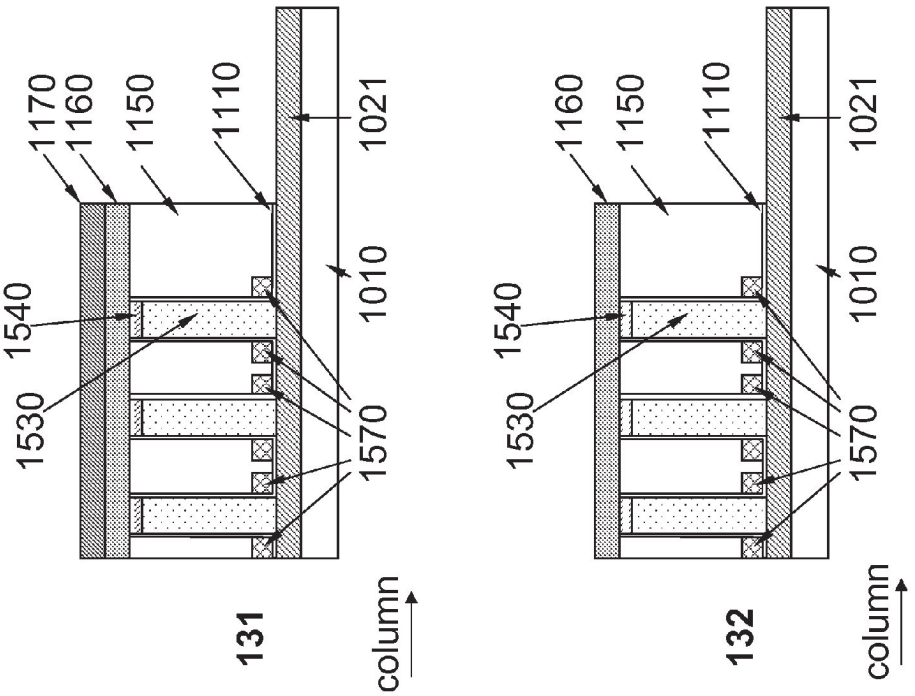

1160
1150
1110
1170
1540
1530
1021
1010
1570
129
column
1150
1110
1170
1160
1540
1530
1021
1010
1570
130
column

Fig. 1 (Cont.)

Fig. 1 (Cont.)


1170
1160
1150
1110
1021
1540
1010
1530
1570
131
column
1160
1150
1110
1021
1540
1010
1530
1570
132
column

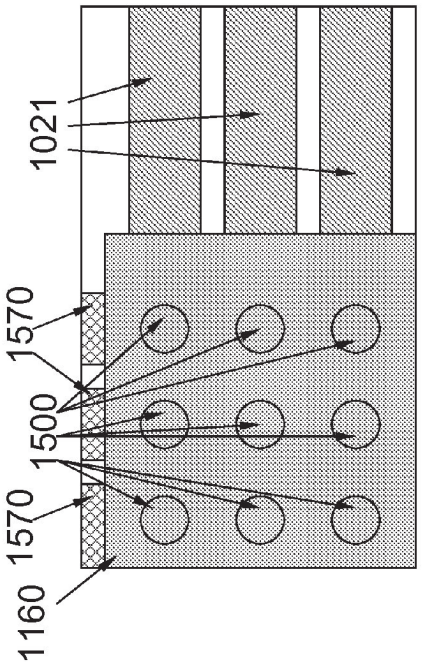


Fig. 2C

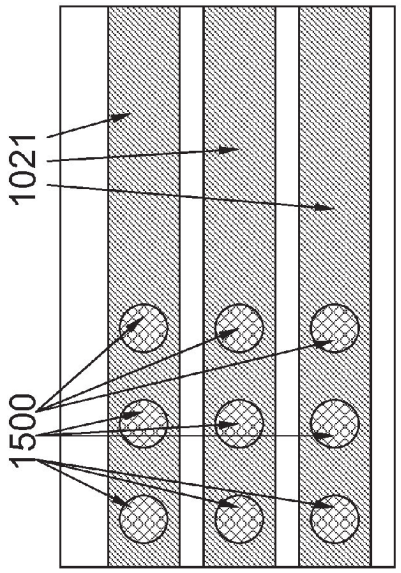


Fig. 2A

column

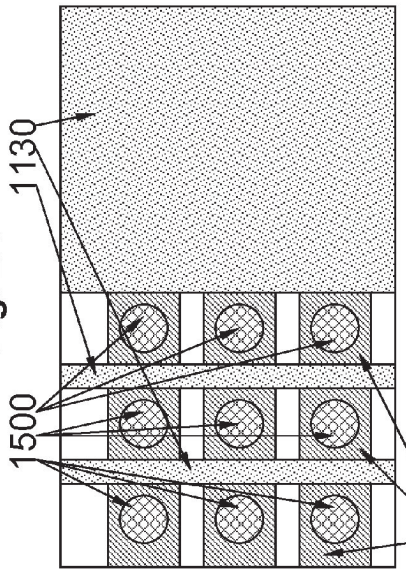


Fig. 2B

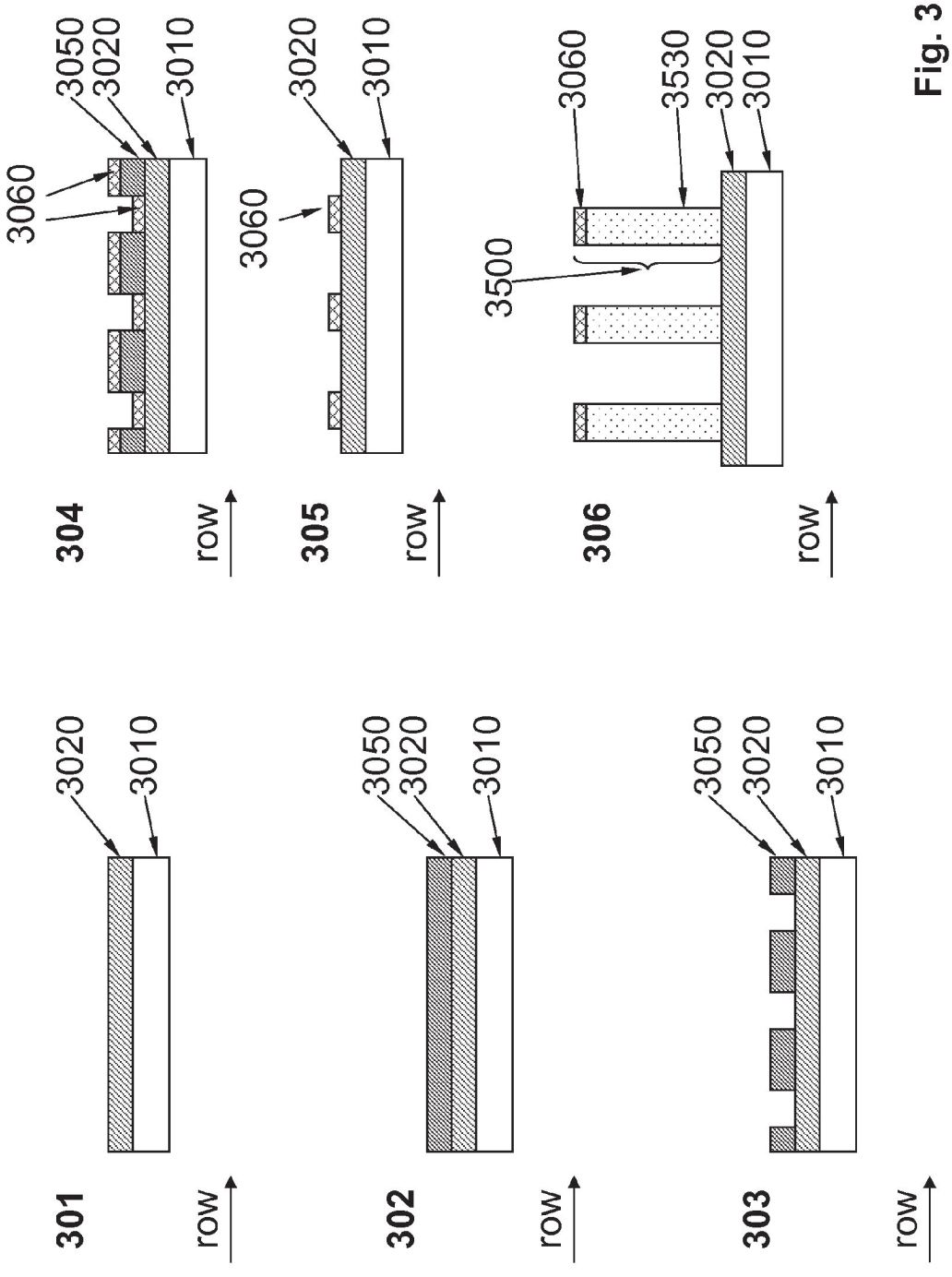
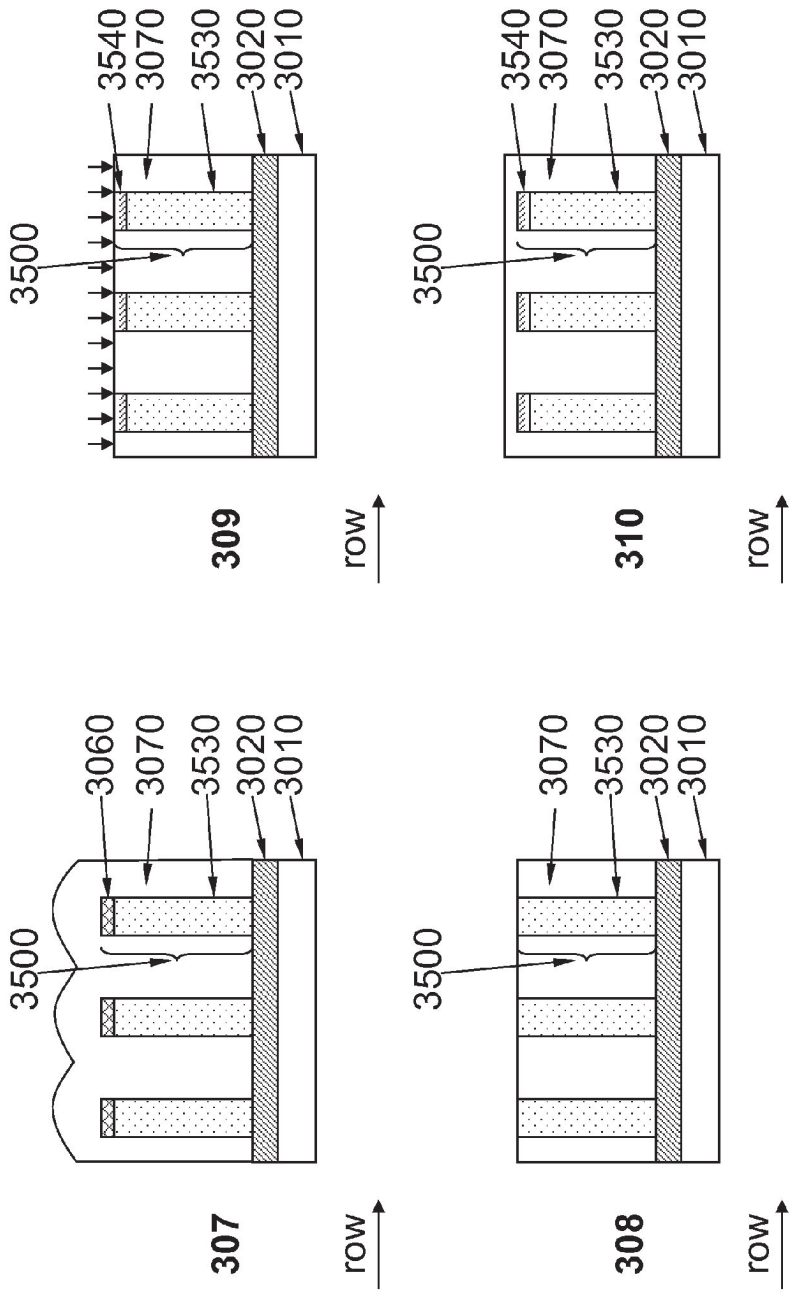

3020
3010
301
row
3050
3020
3010
302
row
3050
3020
3010
303
row
3060
3050
3020
3010
304
row
3060
3020
3010
305
row
3500
3060
3530
3020
3010
306
row

Fig. 3



Steps 311 – 332 are the same as steps 111-132 in Fig. 1.

Fig. 3 (cont.)

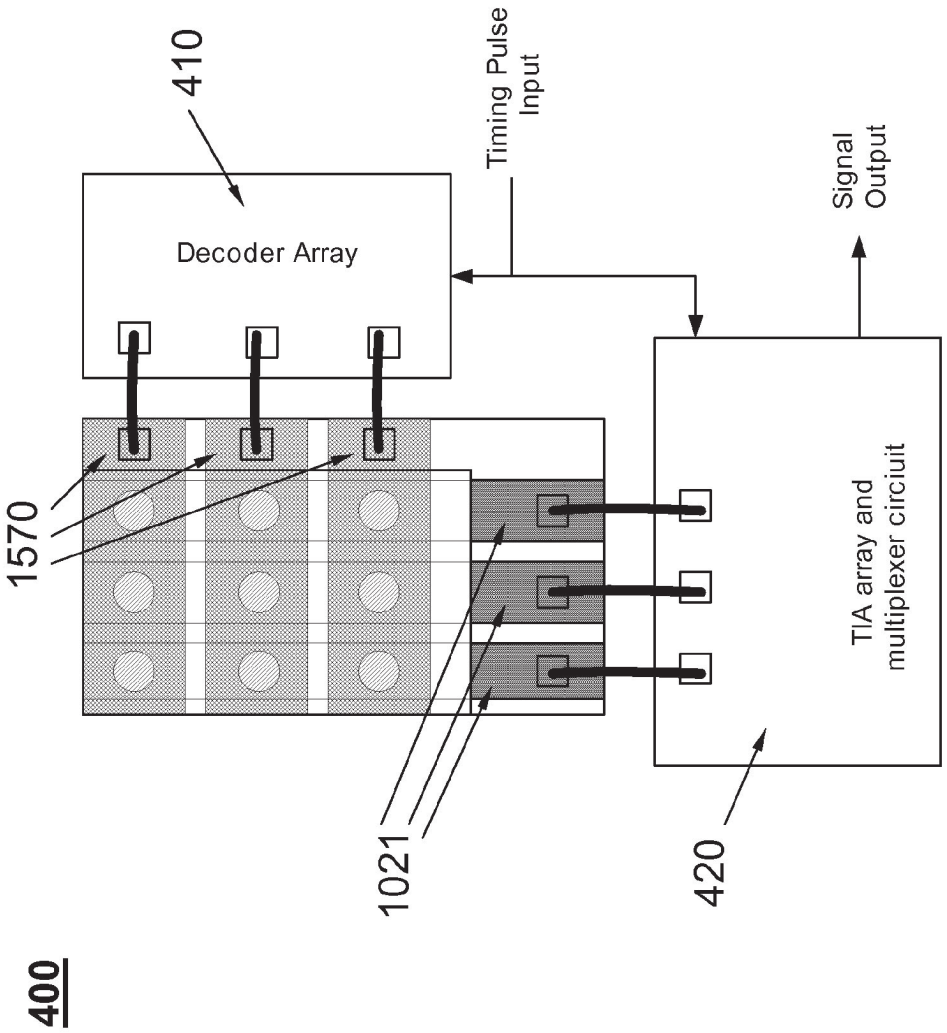

410
Timing Pulse Input
Signal Output
Decoder Array
1570
1021
420
TIA array and multiplexer circiuit
400

FIG. 4

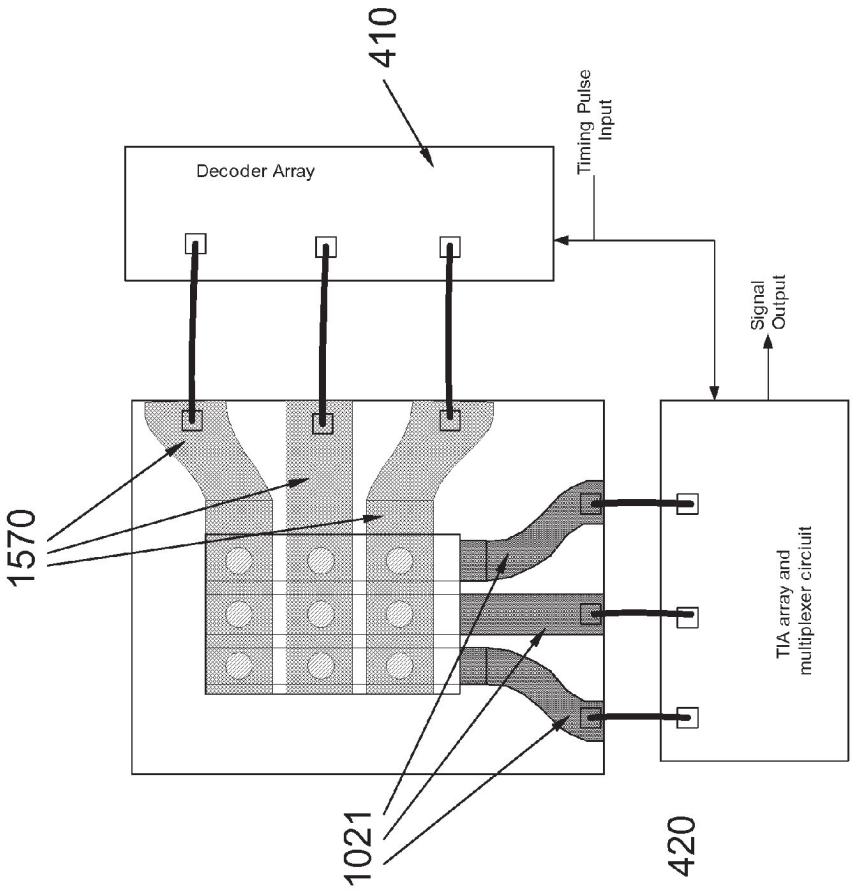

410
Decoder Array
Timing Pulse Input
Signal Output
1570
1021
420
TIA array and multiplexer circiuit
500

FIG. 5

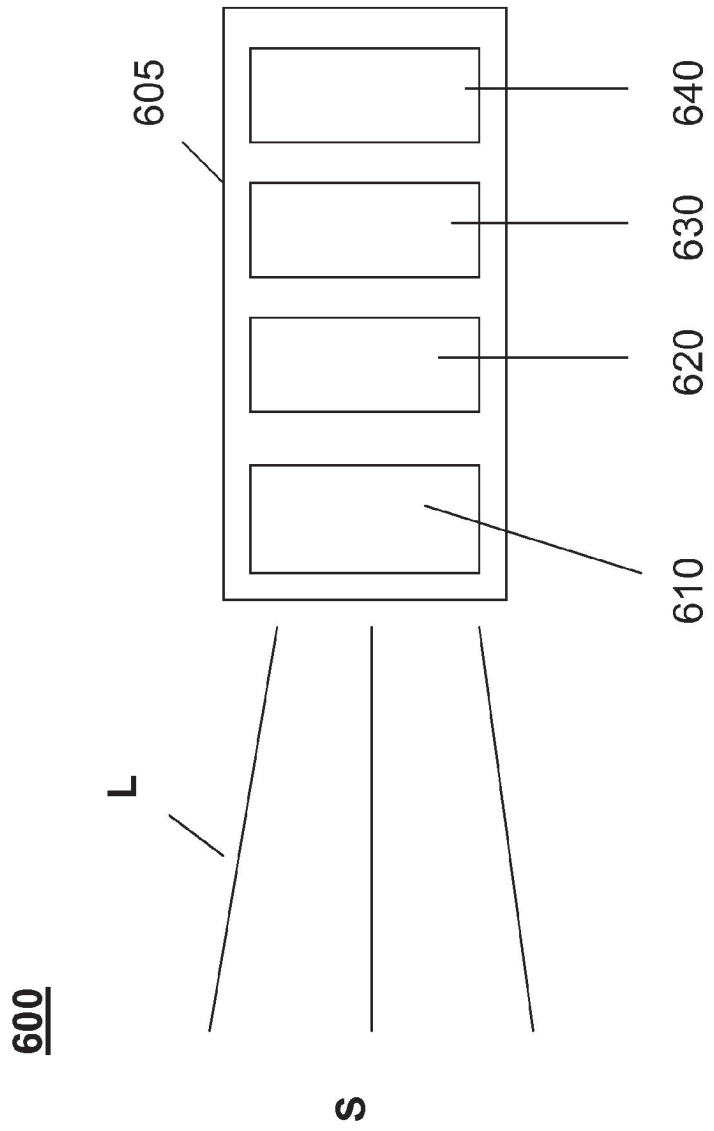


FIG. 6

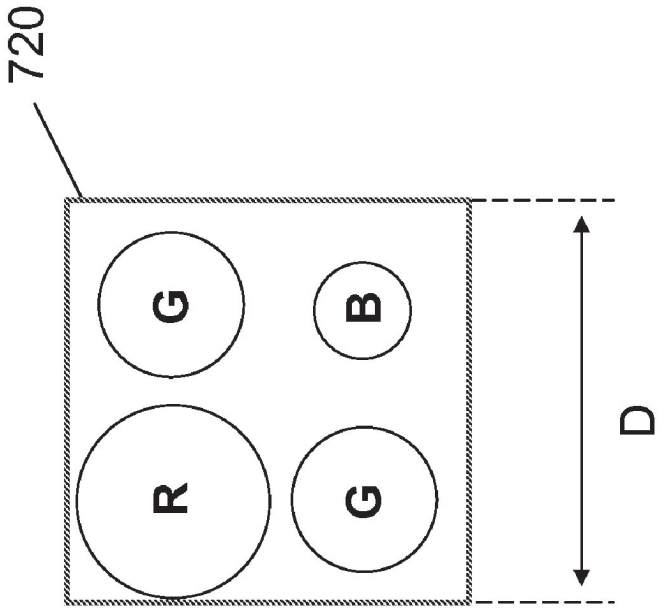


FIG. 7B

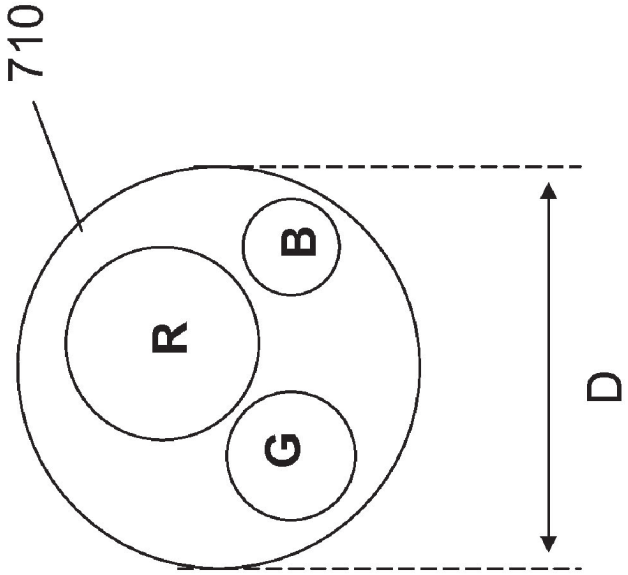


FIG. 7A

VERTICALLY STRUCTURED PASSIVE PIXEL ARRAYS AND METHODS FOR FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to U.S. patent application Ser. Nos. 12/204,686 (granted as U.S. Pat. No. 7,646,943), 12/648,942, 12/270,233, 12/472,264, 12/472,271, 12/478,598, 12/573,582, 12/575,221, 12/633,323, 12/633,318, 12/633,313, 12/633,305, 12/621,497, 12/633,297, 61/266,064, 61/357,429, 61/306,421, 61/306,421, 12/945,492, 12/910,664, 12/966,514, 12/966,535, 12/966,573 and 12/967,880, the disclosures of which are hereby incorporated by reference in their entirety.

BACKGROUND

[0002] An image sensor may be fabricated to have a large number (e.g. more than 1 million) of sensor elements (pixels) arranged in a defined pattern (e.g. a square grid). The pixels may be photodiodes, charge-coupled devices (CCD) or other photosensitive elements, that are adapted to convert electromagnetic radiation (e.g. visible light, infrared light) into electrical signals.

[0003] Recent advances in semiconductor technologies have enabled the fabrication of nanostructures, such as nanotubes, nanocavities, and nanowires. Among them, nanowires have drawn a lot of interest because of their usefulness as sensor elements in an image sensor. For instance, U.S. Patent Application Publication No. 2004/0075464 discloses a plurality of devices based on nanowires, herein incorporated by reference in its entirety. Discrete electronic devices such as transistors, photodiodes and photoconductors have been made successfully from nanostructures. It has been a challenge, however, to integrate and position such discrete electronic devices based on nanostructures in a functional apparatus, especially in a way that each of such devices can be individually controlled and addressed.

[0004] U.S. patent application Ser. Nos. 12/633,313 filed Dec. 8, 2009, and 12/575,221 filed Oct. 7, 2009, describe two methods for achieving this goal, which are herein incorporated by reference in their entirety. The first method includes forming a Cartesian (x-y) matrix wiring (e.g. aluminum) first and to then forming a nanowire array thereon. This method begins with a fabrication of a substrate which provides an x-y matrix wiring and components employing a conventional complementary metal-oxide-semiconductor (CMOS) fabrication process. Nanowires are then grown using a Vapor-Liquid-Solid (VLS) method in designated locations. However, the VLS growth generally requires temperatures that tend to damage the wiring and components on the substrate and tend to undesirably disturb pre-existing doping profile in the substrate.

[0005] The second method includes forming a nanowire array first by either a VLS growth or an etching method. Then, an x-y matrix of wiring is fabricated to electrically connect each nanowire in the nanowire array to external circuitry. This method requires nanoscale lithography on a non-planar surface.

[0006] Described hereinbelow are devices and methods of manufacturing the same, which include controlled integration of individually addressable nanostructures such as nanowires and nanopillars into a functional apparatus such as an image sensor, without the abovementioned problems.

SUMMARY

[0007] Described herein is an image sensor comprising a substrate; a plurality of pixels each of which has at least one nanopillar essentially extending vertically from the substrate, and a gate electrode surrounding the at least one nanopillar; wherein the at least one nanopillar is adapted to convert light impinging thereon to electrical signals and the gate electrode is operable to pinch off or allow current flow through the at least one nanopillar; wherein the at least one nanopillar has a cladding, a refractive index of the cladding being smaller than a refractive index of the nanopillar. The term "cladding" as used herein means a layer of substance surrounding the nanopillars. A refractive index of the cladding is preferably smaller than a refractive index of the nanopillars.

[0008] The image sensor can further comprise a plurality of readout lines, each of which electrically connected to one or more pixels; and a plurality of gate lines, each of which electrically connected to the gate electrode of one or more pixels, wherein no two pixels are connected to a same readout line and their gate electrodes are connected to a same gate line.

[0009] The image sensor can comprise first, second, third and fourth pixels, a first readout line electrically connected to the first and second pixels, a second readout line electrically connected to the third and fourth pixels, a first gate line electrically connected to the gate electrodes of the first and third pixels and a second gate line electrically connected to the gate electrodes of the second and fourth pixels.

[0010] The image sensor can comprise at least one pixel comprising at least first, second, and third nanopillars having a size effective to absorb and/or detect light of about 650 nm, 510 nm and 475 nm in wavelength, respectively.

[0011] The image sensor can comprise at least one pixel comprising at least first, second, third and fourth nanopillars having a size effective to absorb and/or detect light of red, green, green and blue light, respectively.

[0012] In an embodiment, the readout lines comprise a heavily doped semiconductor material; each of the nanopillars comprises a body of an intrinsic semiconductor material or lightly doped semiconductor material of the same conduction type as the heavily doped semiconductor material of the readout lines, and a junction layer of the opposite conduction type from the heavily doped semiconductor material of the readout lines; the body of each nanopillar is sandwiched between one of the readout lines and the junction layer of the nanopillar; the junction layers of all the nanopillars are electrically connected to a transparent conductive layer; and the nanopillars are epitaxial with the readout lines.

[0013] According to one embodiment, an apparatus can comprise the image sensor, a decoder connected to each gate line, and a trans-impedance amplifier and multiplexer circuit connected to each readout line.

[0014] According to one embodiment, an apparatus can comprise the image sensor, foreoptics and a readout circuit.

[0015] One method of manufacturing the image sensor includes steps of forming nanopillars by deep etching a silicon-on-insulator or silicon-on-glass type of substrate. Another method of manufacturing the image sensor includes steps of growing nanopillars by a VLS method.

[0016] Other features of one or more embodiments of this disclosure will seem apparent from the following detailed description, and accompanying drawings, and the appended claims.

[0017] According to an embodiment, an image sensor comprising, a substrate; a plurality of pixels each of which has at least one nanopillar essentially extending vertically from the substrate, and a gate electrode surrounding the at least one nanopillar; wherein the at least one nanopillar is adapted to convert light impinging thereon to electrical signals and the gate electrode is operable to pinch off or allow current flow through the at least one nanopillar. The term "image sensor" as used herein means a device that converts an optical image to an electric signal. An image sensor can be used in digital cameras and other imaging devices. Examples of image sensors include a charge-coupled device (CCD) or a complementary metal-oxide-semiconductor (CMOS) active pixel sensor. The term nanowires "extending essentially perpendicularly from the substrate" as used herein means that angles between the nanowires and the substrate are from 85° to 90°. The term "nanopillar" as used herein means a structure that has a size constrained to at most 1000 nm in two dimensions and unconstrained in the other dimension. The term "nanopillar" can also mean a structure that has a size constrained to at most 10 microns in two dimensions and unconstrained in the other dimension. The term "gate electrode" as used herein means an electrode operable to control electrical current flow by a voltage applied on the gate electrode.

[0018] According to an embodiment, each of the nanopillars has a vertical p-n junction or a vertical p-i-n junction. The term "p-i-n junction" as used herein means a structure of a lightly doped or intrinsic semiconductor region sandwiched between a p-type semiconductor region and an n-type semiconductor region. The p-type and n-type regions can be heavily doped for Ohmic contacts. The term "p-n junction" as used herein means a structure with a p-type semiconductor region and an n-type semiconductor region in contact with each other.

[0019] According to an embodiment, more than one pixels have a common electrode electrically connected thereto. The term "pixel" as used herein means the smallest addressable light-sensing element of an image sensor. Each pixel is individually addressable. Pixels in an image sensor can be arranged in a two-dimensional grid. Each pixel samples characteristics such as intensity and color of a small area of an image projected onto the image sensor. The color sampled by a pixel can be represented by three or four component intensities such as red, green, and blue, or cyan, magenta, yellow, and black, or cyan, magenta, yellow, and green. Many image sensors are, for various reasons, not capable of sensing different colors at the same location.

[0020] According to an embodiment, the common electrode is a transparent conductive material.

[0021] According to an embodiment, the nanopillars and the substrate comprise one or more semiconductor materials and/or metals.

[0022] According to an embodiment, diameters of the nanopillars are from 10 to 2000 nm, 50 to 150 nm, or 90 to 150 nm; and/or lengths of the nanopillars are from 10 to 10000 nm or 100 to 1000 nm; and/or cross-sectional shapes of the nanopillars are circles, squares or hexagons.

[0023] According to an embodiment, the nanopillars are sized to selectively absorb UV light (light of wavelengths from about 10 to about 400 nm), red light (light of wavelengths from about 620 to about 750 nm), green light (light of wavelengths from about 495 to about 570 nm), blue light (light of wavelengths from about 450 to about 475 nm), or IR light (light of wavelengths from about 0.78 to about 1000 microns).

[0024] According to an embodiment, the image sensor further comprises a plurality of readout lines, each of which electrically connected to one or more pixels; and a plurality of gate lines, each of which electrically connected to the gate electrode of one or more pixels, wherein no two pixels are connected to a same readout line and their gate electrodes are connected to a same gate line. The term "readout lines" as used herein means an electrode or a conductor line operable to transmit an electrical signal.

[0025] According to an embodiment, the image sensor comprises first, second, third and fourth pixels, a first readout line electrically connected to the first and second pixels, a second readout line electrically connected to the third and fourth pixels, a first gate line electrically connected to the gate electrodes of the first and third pixels and a second gate line electrically connected to the gate electrodes of the second and fourth pixels. The term "gate line" as used herein means an electrode or a conductor line operable to transmit an electrical signal to the gate electrodes.

[0026] According to an embodiment, the readout lines and the gate lines have one or more electronic devices connected thereto, the one or more electronic devices are selected from the group consisting of amplifiers, multiplexers, D/A or ND converters, computers, microprocessing units, and digital signal processors. The term "amplifier" as used herein means any device that changes, usually increases, the amplitude of a signal. The term "multiplexer" as used herein means a device that performs multiplexing; it selects one of many analog or digital input signals and forwards the selected input into a single line. An analog-to-digital converter (abbreviated ADC, ND or A to D) is a device that converts a continuous quantity to a discrete digital number. A digital-to-analog converter (DAC or D-to-A) is a device that converts a digital (usually binary) code to an analog signal (current, voltage, or electric charge).

[0027] According to an embodiment, the readout lines comprise a heavily doped semiconductor material; each of the nanopillars comprises a body of an intrinsic semiconductor material or lightly doped semiconductor material of the same conduction type as the heavily doped semiconductor material of the readout lines, and a junction layer of the opposite conduction type from the heavily doped semiconductor material of the readout lines; the body of each nanopillar is sandwiched between one of the readout lines and the junction layer of the nanopillar; the junction layers of all the nanopillars are electrically connected to a transparent conductive layer; and the nanopillars are epitaxial with the readout lines. An intrinsic semiconductor, also called an undoped semiconductor or i-type semiconductor, is a pure semiconductor without any significant dopant species present.

[0028] According to an embodiment, a method of using the image sensor comprises: (a) applying a bias voltage to the transparent conductive layer; (b) applying a first gate voltage to all the gate lines, the first gate voltage being effective to pinch off electrical current through the nanopillars; (c) exposing the image sensor to light; (d) connecting all the readout lines to ground to remove accumulated electrical charge thereon, then disconnecting all the readout lines from the ground; (e) applying a second gate voltage to one of the gate

lines, the second gate voltage being effective to allow electrical current through the nanopillars this one gate line surrounds; (f) taking a current reading on at least one of the readout lines; (g) applying the first gate voltage to this one gate line; (h) optionally repeating steps (d)-(g) on each gate line.

[0029] According to an embodiment, an apparatus comprises the image sensor, a decoder connected to each gate line, and a trans-impedance amplifier and multiplexer circuit connected to each readout line.

[0030] According to an embodiment, the trans-impedance amplifier and multiplexer circuit is functional to amplify an electrical current from each readout line and convert it into a voltage signal; the decoder and the trans-impedance amplifier and multiplexer circuit are synchronized by a common timing signal generated by a controller; and/or the decoder and the trans-impedance amplifier and multiplexer circuit are connected to the image sensor by wire-bonding, flip-chip bonding or bump bonding.

[0031] According to an embodiment, the readout lines are parallel or have a fan-out shape, and/or the gate lines are parallel or have a fan-out shape.

[0032] According to an embodiment, a method of using the image sensor to scan an object, comprises: converting reflected light from the object received by the pixels into analog electrical signals; amplifying the analog electrical signals; converting the amplified analog electrical signals to digital electrical signals using an analog-to-digital converter.

[0033] According to an embodiment, an apparatus comprises the image sensor, foreoptics, and a readout circuit, wherein the foreoptics are configured to receive light from a scene and focus or collimate the light onto the image sensor; and the readout circuit is connected to the image sensor and configured to receive output from the image sensor. The term "foreoptics" as used herein means optical components (e.g., lenses, mirrors) placed in an optical path before the image sensor.

[0034] According to an embodiment, the foreoptics comprise one or more of a lens, an optical filter, a polarizer, a diffuser, a collimator; and/or the readout circuit comprises one or more of ASICs, FPGAs, DSPs. An application-specific integrated circuit (ASIC) is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use. A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable". A digital signal processor (DSP) is a specialized microprocessor with an optimized architecture for the fast operational needs of digital signal processing.

[0035] According to an embodiment, the image sensor comprises at least one pixel comprising at least first, second, and third nanopillars having a size effective to absorb and/or detect light of about 650 nm, 510 nm and 475 nm in wavelength, respectively.

[0036] According to an embodiment, the image sensor comprises at least one pixel comprising at least first, second, third and fourth nanopillars having a size effective to absorb and/or detect light of red, green, green and blue light, respectively.

[0037] According to an embodiment, the image sensor further comprises a cladding surrounding at least one of the pixels or at least one of the nanopillars.

[0038] According to an embodiment, the cladding is hafnium oxide or silicon nitride.

[0039] According to an embodiment, the image sensor further comprises a micro lens on an upper end of the at least one nanopillar.

[0040] According to an embodiment, the at least one nanopillar has an absorptance of at least 50% across an entire wavelength range from 400 nm to 800 nm.

BRIEF DESCRIPTION OF THE DRAWINGS

[0041] FIG. **1** shows a method for fabricating the image sensor including steps of deep etching, according to an embodiment.

[0042] FIGS. **2**A-**2**C show top views the image sensor at different stages during the method of FIG. **1**.

[0043] FIG. **3** shows a method for fabricating the image sensor including a VLS growth step, according to another embodiment.

[0044] FIGS. **4** and **5** show an apparatus comprising the image sensor, according to an embodiment.

[0045] FIG. **6** shows another apparatus comprising the image sensor, according to an embodiment.

[0046] FIGS. **7**A and **7**B show schematics of a pixel of the image sensor, the pixel having more than one nanopillar sized to absorb and/or detect light of different wavelength or color, according to embodiments.

DETAILED DESCRIPTION

[0047] In the following detailed description, reference is made to the accompanying drawings, which form a part thereof. In the drawings, similar symbols typically identify similar components, unless the context dictates otherwise. The illustrative embodiments described in the detail description, drawings, and claims are not meant to be limiting. Other embodiments may be utilized, and other changes may be made, without departing from the spirit or scope of the subject matter presented here.

[0048] This disclosure is drawn to, among other things, methods of use, methods of fabrication, apparatuses, systems, and devices relating to an image sensor, each pixel of which has at least a nanopillar that can convert light impinging thereon to electrical signals (e.g. a nanopillar having a vertical p-n or p-i-n junction) and a gate electrode surrounding the nanopillar preferably near its lower end (i.e. the end connected to a substrate). The gate electrode may be located at another location of the nanopillar. The gate electrodes are functional to individually electrically connect the nanopillars to or disconnect the nanopillars from external readout circuitry. The pixels can be arranged in any suitable pattern such as a square grid, a hexagonal grid, and concentric rings. The pixels can be fabricated to absorb light in the ultraviolet (UV), visible (VIS) or infrared (IR) regions and to generate a detectable electrical signal in response thereto.

[0049] The nanopillars essentially extend vertically from the substrate, which can also be referred to as "standing-up".

[0050] The image sensor can be configured for various types of uses such as compact image sensors and spectrophotometers.

[0051] In one embodiment, the pixels are organized into a plurality of "rows". The pixels in each row are electrically connected in parallel to a readout line. Pixels in different rows are electrically connected to different readout lines. The pixels can be organized into a plurality of "columns" such that the gate electrodes of the pixels in each column are electrically connected in parallel to a gate line, the gate electrodes of

the pixels in different columns are electrically connected to different gate lines, and no two different pixels are connected to a same readout line and their gate electrodes are connected to a same gate line. The terms "row" and "column" do not require that pixels are physically aligned or arranged in any particular way, but rather are used to describe topological relationship between the pixels, readout lines and gate lines. An exemplary image sensor according to this embodiment comprises first, second, third, fourth pixels, each of which has a gate electrode, a first readout line electrically connected to the first and second pixels, a second readout line electrically connected to the third and fourth pixels, a first gate line electrically connected to the gate electrodes of the first and third pixels and a second gate line electrically connected to the gate electrodes of the second and fourth pixels.

[0052] In one embodiment, each pixel has at least one nanopillar, which comprises a p-n or p-i-n junction extending in the length direction of the nanopillar. The nanopillars in the pixels can be configured to absorb, confine and transmit light impinging thereon. For example, the nanopillars can function as waveguides to confine and direct light in a direction determined by its physical boundaries.

[0053] In one embodiment, more than one pixels can have a common electrode electrically connected thereto, for example, for providing a bias voltage. The common electrode can be a top layer made of a transparent conductive material, such as ITO (indium tin oxide) or aluminum doped ZnO (AZO).

[0054] In one embodiment, the readout lines and the gate lines can have suitable electronic devices connected thereto, such as, amplifiers, multiplexers, D/A or ND converters, computers, microprocessing units, digital signal processors, etc.

[0055] In one embodiment, the nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si, GaAs, InAs, Ge, ZnO, InN, GaInN, GaN, AlGaInN, BN, InP, InAsP, GaInP, InGaP:Si, InGaP:Zn, GaInAs, AlInP, GaAlInP, GaAlInAsP, GaInSb, InSb, Al, Al—Si, $TiSi_2$, TiN, W, $MoSi_2$, PtSi, $CoSi_2$, WSi_2, In, AuGa, AuSb, AuGe, PdGe, Ti/Pt/Au, Ti/Al/Ti/Au, Pd/Au, ITO (InSnO). The nanopillars and the substrate can be doped by suitable dopants such as GaP, Te, Se, S, Zn, Fe, Mg, Be, Cd, etc. It should be noted that the use nitrides such as Si_3N_4, GaN, InN and AlN can facilitate fabrication of image sensors that can detect light in wavelength regions not easily accessible by conventional techniques. Doping levels of the nanopillars and the substrate can be up to 10^{20} atoms/cm^3. Other suitable materials are possible.

[0056] Methods of fabrication of the image sensor can include shallow trench isolation (STI), also known as "Box Isolation Technique." STI is generally used on CMOS process technology nodes of 250 nanometers and smaller. Older CMOS technologies and non-MOS technologies commonly use isolation based on Local Oxidation of Silicon (LOCOS). STI is typically created early during the semiconductor device fabrication process, before transistors are formed. Steps of the STI process include, for instance, etching a pattern of trenches in the substrate, depositing one or more dielectric materials (such as silicon dioxide) to fill the trenches, and removing the excess dielectric using a technique such as chemical-mechanical planarization.

[0057] The nanopillars can be formed by a dry etching process, such as a deep etching process, or a Bosch process, in combination with a suitable lithography technique (e.g. photolithography, e-beam lithography, holographic lithography). The nanopillars can also be formed by a Vapor Liquid Solid (VLS) method. Diameters of the nanopillars can be from 10 to 2000 nm, preferably 50 to 150 nm, more preferably 90 to 150 nm. Lengths of the nanpillars can be from 10 nm to 10000 nm, preferably 1000 nm to 8000 nm, more preferably 4000 nm to 6000 nm. The nanopillars can have any suitable cross-sectional shape such as a circle, a square, a hexagon.

[0058] The nanopillars can be sized to selectively absorb a wavelength region of interest, for instance, as described in co-pending U.S. Patent Application Ser. No. 61/357,429 filed Jun. 22, 2010, herein incorporation by reference in its entirety. Absorptance can be adjusted by varying the nanopillar spacing (pitch), particularly to near unity.

[0059] The nanopillars can have a cladding material. The nanopillars can selectively absorb UV light, red light, green light, blue light, or IR light.

[0060] The image sensor can have large number of nanopillars, for instance, a million or more.

[0061] FIG. **1** shows steps of a method of manufacturing the image sensor, according to an embodiment, using dry etching. In each step, a schematic cross section of the image sensor being manufactured is shown. The cross section can be along either a "row" direction or a "column" direction as explained below.

[0062] In step **101**, a silicon-on-insulator (SOI)-type substrate or silicon-on-glass (SG)-type substrate is provided. The substrate has an oxide layer **1010**, a heavily doped layer (HDL) **1020** on the layer **1010** and an epi layer **1030** on the HDL layer **1020**. The HDL layer **1020** can be about 500 nm thick; epi layer **1030** can be about 3000 to 10000 nm thick. The substrate can have the following doping profiles: (i) the HDL layer **1020** is p+ (i.e. heavily doped to p type), the epi layer **1030** is p− (i.e. lightly doped to p type); (ii) the HDL layer **1020** p+, the epi layer **1030** is i (i.e. intrinsic); (iii) the HDL layer **1020** is n+ (i.e. heavily doped to n type), the epi layer **1030** is n− (i.e. light doped to n type); or (iv) the HDL layer **1020** is n-F, the epi layer **1030** is i.

[0063] In step **102**, a junction layer **1040** is formed on the epi layer **1030** by ion implantation. The junction layer **1040** is of the opposite conduction type as the HDL layer **1020**, i.e. if the HDL **1020** is p type, the junction layer **1040** is n type; if the HDL **1020** is n type, the junction layer **1040** is p type. The junction layer **1040** is made "shallow" (i.e. thin) by using very low implantation energy. For example, the thickness of the junction layer **1040** is from 10 to 200 nm. The junction layer **1040**, the epi layer **1030** and the HDL layer **1020** form a p-i-n, p-n, n-i-p, or n-p junction, depending on the doping profile.

[0064] In step **103**, a layer of resist **1050** is applied on the junction layer **1040**. The resist layer **1050** can be applied by spin coating. The resist layer **1050** can be a photo resist or an e-beam resist.

[0065] In step **104**, lithography is performed. The resist layer **1050** now has a pattern of openings in which the junction layer **1040** is exposed. The openings are preferably dots, squares or circles in shape. Shapes and locations of the openings correspond to the shapes and locations of the nanopillars of the image sensor being manufactured. The resolution of the lithography is limited by the wavelength of the radiation used. Photolithography tools using deep ultraviolet (DUV) light with wavelengths of approximately 248 and 193 nm, allows minimum feature sizes down to about 50 nm. E-beam lithography tools using electron energy of 1 keV to 50 keV allows minimum feature sizes down to a few nanometers.

[0066] In step **105**, a mask layer **1060** is deposited. The deposition can be done using a technique such as thermal evaporation, e-beam evaporation, sputtering, atomic layer deposition (ALD), plasma-enhanced chemical vapor deposition (PECVD). The mask layer **1060** can be a metal such as Cr or Al, or a dielectric such as SiO_2 or Si_3N_4. The thickness of the mask layer can be determined by desired etching depth in step **107** and etching selectivity.

[0067] In step **106**, remainder of the resist layer **1050** is lift off by a suitable solvent or ashed in a resist asher to remove any mask layer **1060** support thereon. A portion of the mask layer **1060** in the openings of the resist layer **1050** is retained. A portion of the junction layer **1040** is now exposed through the retained mask layer **1060**.

[0068] In step **107**, the exposed portion of the junction layer **1040** and the portion of the epi layer **1030** directly therebelow are deep etched until the HDL layer **1020** directly below the exposed portion of the junction layer **1040** is exposed, to form nanopillars **1500**. Each nanopillar **1500** now has a mask layer **1560** which is part of the mask layer **1060**, a junction layer **1540** which is part of the junction layer **1040** and an epi layer **1530** which is a part of the epi layer **1030**. Deep etching includes alternating deposition and etch steps and leads "scalloping" on sidewalls of the nanopillars **1500**, i.e. the sidewalls of the nanopillars **1500** are not smooth. The deep etching can use gases such as C_4F_8 and SF_6.

[0069] In step **108**, the sidewalls of the nanopillars **1500** are smoothed by dipping the image sensor in an etchant such as potassium hydroxide (KOH) followed by rinsing.

[0070] In step **109**, space between the nanopillars **1500** is filled by an oxide or a polymer **1070** such as silicon oxide or polyimide by a suitable technique such as chemical vapor deposition (CVD), drop casting, evaporation or spin coating.

[0071] In step **110**, an upper surface of the oxide or polymer **1070** is planarized by a suitable technique such as chemical mechanical polishing/planarization (CMP). The mask layer **1560** of the nanopillars **1500** should not be exposed.

[0072] In step **111**, another layer of resist **1080** is applied on the oxide or polymer **1070**. The resist layer **1080** can be applied by spin coating. The resist layer **1080** can be a photo resist or an e-beam resist.

[0073] In step **112**, lithography is performed. The resist layer **1080** now has a pattern of openings in which the oxide or polymer **1070** is exposed. The openings preferably are parallel slots extending across the entire width of the substrate. Each nanopillar **1500** entirely falls into the extent of one of the openings. All the nanopillars **1500** in the extent of the same opening will be later electrically connected to the same readout line. The shapes and locations of the openings correspond to the shapes and locations of the readout lines.

[0074] In step **113**, a mask layer **1090** is deposited. The deposition can be done using a technique such as thermal evaporation, e-beam evaporation, sputtering, atomic layer deposition (ALD), plasma-enhanced chemical vapor deposition (PECVD). The mask layer **1090** can be a metal such as Cr or Al, or a dielectric such as SiO_2 or Si_3N_4. The thickness of the mask layer can be determined by desired etching depth in step **115** and etching selectivity.

[0075] In step **114**, remainder of the resist layer **1080** is lift off by a suitable solvent or ashed in a resist asher to remove any mask layer **1090** support there on. A portion of the mask layer **1090** in the openings of the resist layer **1080** is retained. A portion of the oxide or polymer **1070** is now exposed between the retained mask layer **1090**.

[0076] In step **115**, the exposed portion of the oxide or polymer **1070** and the portion of the HDL layer **1020** directly therebelow are deep etched until the layer **1010** directly below the exposed portion of the oxide or polymer **1070** is exposed. The HDL layer **1020** is now segmented into readout lines **1021**. A cross section along the length of the readout lines **1021** is referred to as along the "column" direction.

[0077] In step **116**, a shield layer **1100** is deposited by a technique such as thermal evaporation or e-beam evaporation, to shield the exposed portion of the layer **1010**. The shield layer **110** can be Si_3N_4.

[0078] In step **117**, removing the oxide or polymer **1070** using a suitable method such as dissolving in a suitable etchant (e.g. HF, tetramethylammonium hydroxide) or dry etching. The nanopillars **1500** are now exposed.

[0079] In step **118**, a passivation layer **1110** is deposited by an isotropic deposition technique such as ALD to cover the entire exposed surfaces of the image sensor. This passivation layer **1110** will function as gate dielectric of the gate electrodes. The passivation layer **1110** can be SiO_2, Si_3N_4, ZrO_2, HfO_2, Al_2O_3, etc. Materials with high dielectric constants such as ZrO_2 and HfO_2 are preferred.

[0080] In step **119**, space between the nanopillars **1500** is filled by an oxide or a polymer **1120** such as silicon oxide or polyimide by a suitable technique such as chemical vapor deposition (CVD), drop casting, evaporation or spin coating.

[0081] In step **120**, an upper surface of the oxide or polymer **1120** is planarized by a suitable technique such as CMP. The passivation layer **1110** should not be exposed or damaged.

[0082] The image sensor in steps **121** through **132** is shown in a cross section along the "column" direction.

[0083] In step **121**, a patterned mask layer **1130** is deposited on the oxide or polymer **1120** using lithography and lift-off, similar to steps **111** to **114**. The patterned mask layer **1130** has openings in which the oxide or polymer **1120** is exposed. Each nanopillar **1500** entirely falls into the extent of one of the openings in the patterned mask layer **1130**. Shapes and locations of the openings correspond to shapes and locations of the gate lines and gate electrodes. Gate electrodes of all the nanopillars **1500** in the extent of the same opening will be later electrically connected to the same gate line. No two nanopillars are connected to a same readout line and their gate electrodes are connected to a same gate line. The gate electrodes can be part of the gate lines.

[0084] In step **122**, the exposed portion of the oxide or polymer **1120** is deep etched until the passivation layer **1110** directly therebelow is exposed.

[0085] In step **123**, a metal layer **1140** is deposited using a technique such as thermal evaporation or e-beam evaporation. The portion of the metal layer **1140** deposited around the lower end of the nanopillars **1500** forms the gate electrodes and gate lines **1570**. Each gate line **1570** is separated by the portion of the oxide or polymer **1120** directly below the patterned mask layer **1130**. The metal layer **1140** can be Cr, Al, Au, Ag, Pt, Pd, doped poly-silicon, etc. A cross section along the length of the gate lines **1570** is referred to as along the "row" direction.

[0086] In step **124**, removing the oxide or polymer **1120** using a suitable method such as dissolving in a suitable etchant (e.g. HF, tetramethylammonium hydroxide) or dry etching.

[0087] In step **125**, space between the nanopillars **1500** is filled by an oxide or a polymer **1150** such as silicon oxide or

polyimide by a suitable technique such as chemical vapor deposition (CVD), drop casting, evaporation or spin coating.

[0088] In step **126**, an upper surface of the oxide or polymer **1150** is planarized by a suitable technique such as CMP until the junction layer **1540** of the nanopillars **1500** is exposed.

[0089] In step **127**, a transparent conductive layer (TCL) **1160**, such as ITO or aluminum doped zinc oxide (AZO) is deposited by a suitable technique such sputtering. Annealing may be performed to facilitate forming Ohmic contact between the TCL layer **1160** and the junction layer **1540** of the nanopillars **1500**.

[0090] In step **128**, a layer of resist **1170** s applied on the TCL layer **1160**.

[0091] In step **129**, lithography is performed. The resist layer **1170** now has an opening over an edge portion of the substrate. No nanopillars **1500** fall into the extent of the opening; a portion of each readout line **1021** falls into the extent of the opening; and a portion of each gate line **1570** falls into the extent of the opening. A portion of the TCL layer **1160** is exposed in the opening.

[0092] In step **130**, the exposed portion of the TCL layer **1160** is removed by wet etch using a suitable etchant such as HCl. Now a portion of the oxide or polymer **1150** is exposed.

[0093] In step **131**, the exposed portion of the oxide or polymer **1150** and the portion of the passivation layer **1110** directly therebelow are removed by dry etch. Now each readout line **1021** and each gate line **1570** has an exposed portion, for connecting to external circuitry.

[0094] In step **132**, the resist layer **1170** is lift off by a suitable solvent or ashed in a resist asher.

[0095] Optionally, in one embodiment, micro lenses can be fabricated on upper ends of the nanopillars **1500** to enhance light collection. The micro lenses preferably have, convex upper surfaces, for instance, hemispherical or parabolic upper surfaces, and have a base corresponding to the pixel pitch. Other configurations are also possible.

[0096] An optional cladding material might also be deposited on the side surfaces of the nanopillars **1500**. The cladding material can be hafnium dioxide or silicon nitride.

[0097] FIG. **2**A shows a top view of the image sensor after step **120**. The nanopillars **1500** are organized in "columns", i.e. all the nanopillars **1500** in the same column are electrically connected to the same readout line **1021**.

[0098] FIG. **2**B shows a top view of the image sensor after step **122**.

[0099] FIG. **2**C shows a top view of the image sensor after step **132**. Each readout line **1021** and each gate line **1570** has an exposed portion for connection to external circuitry.

[0100] FIG. **3** shows steps of a method of manufacturing the image sensor, according to another embodiment, using the VLS method. In each step, a schematic cross section along the "row" direction or the "column" direction of the image sensor being manufactured is shown.

[0101] Details of the VLS method are described, for instance, in International Patent Application Publication No. WO2008/079076A1 and U.S. Patent Application Publication Nos. 200/80248304, 2008/0246123, 2008/0246020, and 2008/0237568, each of which is herein incorporation by reference in its entirety.

[0102] In step **301**, a silicon-on-insulator (SOI)-type substrate or silicon-on glass (SG)-type substrate is provided. The substrate has an oxide layer **3010** and a heavily doped layer (HDL) **3020** on the layer **3010**. The HDL layer **3020** can be about 500 nm thick. The HDL layer **3020** can be either p+ or n-F.

[0103] In step **302**, a layer of resist **3050** is applied on the HDL layer **3020**. The resist layer **3050** can be applied by spin coating. The resist layer **3050** can be a photo resist or an e-beam resist.

[0104] In step **303**, lithography is performed. The resist layer **3050** now has a pattern of openings in which the HDL layer **3020** is exposed. The openings are dots, squares or circles in shape, and correspond to the shapes and locations of the nanopillars of the image sensor being manufactured. The resolution of the lithography is limited by the wavelength of the radiation used. Photolithography tools using deep ultraviolet (DUV) light with wavelengths of approximately 248 and 193 nm, allows minimum feature sizes down to about 50 nm. E-beam lithography tools using electron energy of 1 keV to 50 keV allows minimum feature sizes down to a few nanometers.

[0105] In step **304**, a seed layer **3060** is deposited. The deposition can be done using a technique such as thermal evaporation, e-beam evaporation, sputtering, atomic layer deposition (ALD), plasma-enhanced chemical vapor deposition (PECVD). The seed layer **3060** can be a metal such as Au, Ag, Fe, Ni, Cr, Al or a combination thereof. The thickness of the seed layer **3060** can be from 1 nm to 10 nm.

[0106] In step **305**, remainder of the resist layer **3050** is lift off by a suitable solvent or ashed in a resist asher to remove any seed layer **3060** support there on. A portion of the seed layer **3060** in the openings of the resist layer **3050** is retained.

[0107] In step **306**, nanopillars **3500** are grown from the seed layer **3060** by the VLS method, wherein the seed layer **3060** functions as a catalyst. Preferably, the nanopillars **3500** are epitaxial with the underlying HDL layer **3020**. After the VLS growth, each nanopillar **3500** now has a body **3530** and the seed layer **3060** thereon. The body **3530** is either i or lightly doped to the same conduction type as the HDL layer **3020**, i.e. if the HDL layer **3020** is n type, the body **3530** should be n type; if the HDL layer **3020** is p type, the body **3530** should be p type. The length of the nanopillars **3500** can be determined by parameters of the VLS growth, such as length of time, temperature, gas flow rates, gas composition, etc.

[0108] In step **307**, space between the nanopillars **3500** is filled by an oxide **3070** such as silicon oxide by a suitable technique such as chemical vapor deposition (CVD) or a polymer **3070** such as polyimide by a suitable technique such as drop casting, evaporation, CVD or spin coating. The space between the nanopillars **3500** can alternatively be filled by other suitable dielectric materials.

[0109] In step **308**, an upper surface of the oxide or polymer **3070** is planarized by a suitable technique such as CMP, until the body **3530** of each nanopillar **3500** is exposed and the seed layer **3060** is entirely removed.

[0110] In step **309**, a junction layer **3540** is formed on a top surface of each nanopillar **3500** by ion implantation. The junction layer **3540** is of the opposite conduction type as the HDL layer **3020**, i.e. if the HDL **3020** is p type, the junction layer **3540** is n type; if the HDL **3020** is n type, the junction layer **3540** is p type. The junction layer **3540** is made "shallow" (i.e. thin) by using very low implantation energy. For example, the thickness of the junction layer **3540** is from 10 to 200 nm. The junction layer **3540**, the body **3530** and the

HDL layer **3020** form a p-i-n, p-n, n-i-p, or n-p junction, depending on the doping profile.

[0111] In step **310**, covering the junction layer **3540** by depositing more of the oxide or polymer **3070**.

[0112] Steps **311-332** are the same as steps **111-132** if FIG. **1**.

[0113] A method of using the image sensor comprises: (a) exposing the pixels to light; (b) reading electrical signals from a pixel by connecting at least one nanopillar in the pixel to external readout circuitry using the gate electrode surrounding the at least one nanopillar of the pixel. The electrical signals can be electric charge accumulated on the nanopillar, a change of electrical current through the nanopillar, or a change of electrical impedance of the nanopillar.

[0114] A method of using the image sensor made by the method shown in FIG. **1** or FIG. **3**, comprises: (a) applying a bias voltage to the TCL layer **1160**; (b) applying a first gate voltage to all gate lines **1570**, the first gate voltage being effective to pinch off electrical current through the nanopillars; (c) exposing the image sensor to light; (d) connecting all the readout lines **1021** to ground to remove accumulated electrical charge thereon, then disconnecting all the readout lines **1021** from the ground; (e) applying a second gate voltage to one of the gate lines **1570**, the second gate voltage being effective to allow electrical current through the nanopillars this gate line **1570** surrounds; (f) taking a current reading on at least one of the readout lines **1021**; (g) applying the first gate voltage to this gate line **1570**; (h) optionally repeating steps (d)-(g) on each gate line **1570**.

[0115] FIGS. **4** and **5** show an apparatus comprising the image sensor and a control circuit. The control circuit comprises a decoder **410** and a trans-impedance amplifier (TIA) and multiplexer circuit **420**. The image sensor and the control circuit can be formed as an integrated circuit or chip. To control or address the nanopillars, a gate voltage can be selectively applied to one of the gate lines **1570** at a time to allow electrical current through those nanopillars connected to that particular gate line **1570** and the readout lines **1021** can be used to read electrical current from each of those nanopillars. In this way, a row-by-row (i.e. gate line by gate line) addressing scheme may be executed. The TIA and multiplexer circuit **420** is connected to each readout line **1021** and can include a multiplexer to sequentially output electrical current one each readout line **1021** to a single terminal. The TIA and multiplexer circuit **420** can amplify the electrical current from each readout line **1021** and convert it into a voltage signal. The decoder array **410** is connected to each gate line **1570** and can include a multiplexer to sequentially apply gate voltages to each gate line **1570**. The TIA and multiplexer circuit **420** and the decoder array **410** can be synchronized by a common timing signal from a timing pulse input. A controller can be used to generate the timing signal. The control circuit can further comprise other functional components, such as, for example, an analog-to-digital converter, an exposure controller, and a bias voltage circuit, etc. An exemplary TIA can be OPA381; an exemplary multiplexer can be ADG732, and an exemplary decoder can be SN74154 (all from Texas Instruments Inc). It will be appreciated, of course, that other readout circuitry components may also be used.

[0116] The control circuit can be connected to the image sensor by any suitable interconnect techniques, such as wire-bonding, flip-chip bonding or bump bonding.

[0117] The readout lines **1021** and the gate lines **1570** can be parallel as shown in FIG. **4** or can have a "fan-out" shape as shown in FIG. **5**. As will be appreciated the fan out shaped electrodes provide greater room for connections to external circuitry.

[0118] The image sensor described herein can be used as various image sensors, including contact image sensors (CIS). Contact image sensors are capable of resolving features of a size approximately equal to the size of the pixel. The size of the pixel may be determined by the size of the nanopillar and the surrounding region in which the evanescent field propagates. CISs are a relatively recent technological innovation in the field of optical flatbed scanners that are rapidly replacing charge-coupled devices (CCDs) in low power and portable applications. As the name implies, CISs place the image sensor in near direct contact with an object to be scanned in contrast to using mirrors to bounce light to a stationary sensor, as is the case in conventional CCD scanners. A CIS typically consists of a linear array of detectors, covered by a focusing lens and flanked by red, green, and blue LEDs for illumination. Usage of LEDs allows the CIS to be relatively power efficient, with many scanners being powered through the minimal line voltage supplied, for instance, via a universal serial bus (USB) connection. CIS devices typically produce lower image quality compared to CCD devices; in particular, the depth of field is limited, which poses a problem for material that is not perfectly flat. However, a CIS contact sensor is typically modularized. All the necessary optical elements may be included in a compact module. Thus, a CIS module can help to simplify the inner structure of a scanner. Further, a CIS contact sensor is typically smaller and lighter than a CCD line sensor. With a CIS, the scanner can be portable with a height around 30 mm.

[0119] A CIS can include an elongate optical assembly comprising illumination, optical imaging, and detection systems. The illumination source illuminates a portion of the object (commonly referred to as a "scan region"), whereas the optical imaging system collects light reflected by the illuminated scan region and focuses a small area of the illuminated scan region (commonly referred to as a "scan line") onto the pixels of the CIS. The pixels convert light incident thereon into electrical signals. Image data representative of the entire object then may be obtained by sweeping the CIS across the entire object.

[0120] A method of scanning an object using a CIS essentially comprises three steps: first, the pixels of the CIS convert reflected light they receive from the object into analog electrical signals; second, the analog electrical signals are amplified; third, the amplified analog electrical signals are converted to digital electrical signals by an analog-to-digital (A/D) converter. The digital signals may then be further processed and/or stored as desired.

[0121] FIG. **6** shows a schematic of an apparatus **600** in accordance with an embodiment. The apparatus **600** comprises foreoptics **610**, the image sensor **620**, a readout circuit (ROC) **630**, and a processor **640**. A housing may enclose and protect one of more the foregoing components of the apparatus **600** from excessive or ambient light, the environment (e.g., moisture, dust, etc.), mechanical damage (e.g., vibration, shock), etc.

[0122] Light (L) from a scene (S) emanates toward the apparatus **600**. For clarity, only L from S impinging upon the apparatus **600** is depicted (although it will be appreciated that L from S propagates in all directions).

[0123] The foreoptics **610** may be configured to receive L from S and focus or collimate the received L onto the image

sensor **620**. For instance, foreoptics **610** may include one or more of: a lens, an optical filter, a polarizer, a diffuser, a collimator, etc.

[0124] The pixels in the image sensor **620** may include nanopillars of different sizes (e.g. from about 50 to 200 nm) for selective detection of light across a wavelength regions of interest.

[0125] The ROC **630** may be connected to the image sensor **620** and is configured to receive output therefrom.

[0126] The processor **640** is configured to receive output from the ROC **630**. The processor **640** may, in some instances, be configured to provide defect correction, linearity correction, data scaling, zooming/magnification, data compression, color discrimination, filtering, and/or other imaging processing, as desired.

[0127] In one embodiment, the processor **640** may include hardware, such as Application Specific Integrated Circuits (ASICs), Field Programmable Gate Arrays (FPGAs), digital signal processors (DSPs), or other integrated formats. However, those skilled in the art will recognize that the processor **640** may, in whole or in part, can be equivalently implemented in integrated circuits, as one or more computer programs having computer-executable instructions or code running on one or more computers (e.g., as one or more programs running on one or more computer systems), as one or more programs running on one or more processors (e.g., as one or more programs running on one or more microprocessors), as firmware, or as virtually any combination thereof, and that designing the circuitry and/or writing the code for the software and/or firmware would be well within the skill of one skilled in the art in light of this disclosure. In addition, those skilled in the art will appreciate that the mechanisms of the subject matter described herein are capable of being distributed as a program product in a variety of forms, and that an illustrative embodiment of the subject matter described herein applies regardless of the particular type of computer-readable medium used to actually carry out the distribution.

[0128] In some implementations, the apparatus **600** may also be configured as a spectrophotometer to measure intensity of reflection or absorption at one more wavelengths.

[0129] Depending on the construction of the image sensor **620**, light at different wavelengths may be detected nanopillars at different locations and with different sizes. A three- or four-nanopillar pixel may be fabricated. Of course, pixels having additional pillars are also possible.

[0130] FIGS. **7**A and **7**B show an exemplary three-nanopillar pixel and an exemplary four-nanopillar pixel according to embodiments. These pixels may be incorporated into the image sensor.

[0131] FIG. **7**A shows a pixel **710** including three nanopillars R, G, B, having different sizes configured to absorb and/or detect red, green, and blue light, respectively, according to an embodiment. For instance, the R, G, B nanopillars can have sizes effective to absorb and/or detect light of about 650 nm, 510 nm, and 475 nm in wavelength, respectively. The diameter of the pixel **710** may be 10 μm or less. The pixel **710** may be used in traditional shadow masked based display device.

[0132] FIG. **7**B shows a pixel **720** including four nanopillars R, G, B, G, having different sizes configured to absorb and/or detect red, green, and blue light, respectively, according to an embodiment. Two of the nanopillars, G, absorb and/or detect green light. The diameter of the pixel **720** may be 10 μm or less.

[0133] A cladding may, in some instance, surround at least one pixel of the image sensor to increase light absorption. The cladding of pixel **710** and **720** may be formed, for instance, from hafnium oxide or silicon nitride.

[0134] The foregoing detailed description has set forth various embodiments of the devices and/or processes by the use of diagrams, flowcharts, and/or examples. Insofar as such diagrams, flowcharts, and/or examples contain one or more functions and/or operations, it will be understood by those within the art that each function and/or operation within such diagrams, flowcharts, or examples can be implemented, individually and/or collectively, by a wide range of hardware, software, firmware, or virtually any combination thereof.

[0135] Those skilled in the art will recognize that it is common within the art to describe devices and/or processes in the fashion set forth herein, and thereafter use engineering practices to integrate such described devices and/or processes into data processing systems. That is, at least a portion of the devices and/or processes described herein can be integrated into a data processing system via a reasonable amount of experimentation.

[0136] The subject matter described herein sometimes illustrates different components contained within, or connected with, other components. It is to be understood that such depicted architectures are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In a conceptual sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermediate components.

[0137] With respect to the use of substantially any plural and/or singular terms herein, those having skill in the art can translate from the plural to the singular and/or from the singular to the plural as is appropriate to the context and/or application. The various singular/plural permutations may be expressly set forth herein for sake of clarity.

[0138] All references, including but not limited to patents, patent applications, and non-patent literature are hereby incorporated by reference herein in their entirety.

[0139] While various aspects and embodiments have been disclosed herein, other aspects and embodiments will be apparent to those skilled in the art. The various aspects and embodiments disclosed herein are for purposes of illustration and are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

What is claimed is:

1. An image sensor comprising:

a substrate;

a plurality of pixels each of which has at least one nanopillar essentially extending vertically from the substrate, and a gate electrode surrounding the at least one nanopillar;

wherein the at least one nanopillar is adapted to convert light impinging thereon to electrical signals and the gate electrode is operable to pinch off or allow current flow through the at least one nanopillar;

wherein the at least one nanopillar has a cladding, a refractive index of the cladding being smaller than a refractive index of the nanopillar.

2. The image sensor of claim 1, wherein each of the nanopillars has a vertical p-n junction or a vertical p-i-n junction.

3. The image sensor of claim 1, wherein more than one pixels have a common electrode electrically connected thereto.

4. The image sensor of claim 3, wherein the common electrode is a transparent conductive material.

5. The image sensor of claim 1, wherein the nanopillars and the substrate comprise one or more semiconductor materials and/or metals.

6. The image sensor of claim 1, wherein diameters of the nanopillars are from 10 to 2000 nm, 50 to 150 nm, or 90 to 150 nm; and/or lengths of the nanopillars are from 10 to 10000 nm or 100 to 1000 nm; and/or cross-sectional shapes of the nanopillars are circles, squares or hexagons.

7. The image sensor of claim 1, wherein the nanopillars are sized to selectively absorb UV light, red light, green light, blue light, or IR light.

8. The image sensor of claim 1, further comprising a plurality of readout lines, each of which electrically connected to one or more pixels; and a plurality of gate lines, each of which electrically connected to the gate electrode of one or more pixels, wherein no two pixels are connected to a same readout line and their gate electrodes are connected to a same gate line.

9. The image sensor of claim 8, comprising first, second, third and fourth pixels, a first readout line electrically connected to the first and second pixels, a second readout line electrically connected to the third and fourth pixels, a first gate line electrically connected to the gate electrodes of the first and third pixels and a second gate line electrically connected to the gate electrodes of the second and fourth pixels.

10. The image sensor of claim 8, wherein the readout lines and the gate lines have one or more electronic devices connected thereto, the one or more electronic devices are selected from the group consisting of amplifiers, multiplexers, D/A or A/D converters, computers, microprocessing units, and digital signal processors.

11. The image sensor of claim 8, wherein:

the readout lines comprise a heavily doped semiconductor material;

each of the nanopillars comprises a body of an intrinsic semiconductor material or lightly doped semiconductor material of the same conduction type as the heavily doped semiconductor material of the readout lines, and a junction layer of the opposite conduction type from the heavily doped semiconductor material of the readout lines;

the body of each nanopillar is sandwiched between one of the readout lines and the junction layer of the nanopillar;

the junction layers of all the nanopillars are electrically connected to a transparent conductive layer; and

the nanopillars are epitaxial with the readout lines.

12. A method of manufacturing an image sensor comprising:

providing a substrate having an oxide layer, a heavily doped layer on the oxide layer, and an epi layer on the heavily doped layer, the epi layer being intrinsic or lightly doped to a same conduction type as the heavily doped layer;

forming a junction layer on the epi layer, the junction layer being of an opposite conduction type as the heavily doped layer;

forming nanopillars from the junction layer and a portion of the epi layer, the nanopillars essentially extending vertically from the substrate;

forming readout lines from the heavily doped layer; and

forming gate lines.

13. The method of claim 12, wherein:

the heavily doped layer is p type or n type;

the heavily doped layer is about 500 nm thick;

the epi layer is about 3000 to 10000 nm thick;

the junction layer is about 10 to 200 nm thick;

the nanopillars are formed by deep etching;

the readout lines are formed by deep etching; and/or

the gate lines are formed by depositing a metal layer.

14. A method of manufacturing an image sensor comprising:

providing a substrate having an oxide layer, and a heavily doped layer on the oxide layer;

growing nanopillars essentially extending vertically from the substrate;

forming a junction layer on a top surface of each nanopillar, the junction layer being of an opposite conduction type as the heavily doped layer;

forming readout lines from the heavily doped layer; and

forming gate lines.

15. The method of claim 14, wherein:

the heavily doped layer is p type or n type;

the heavily doped layer is about 500 nm thick; and

the nanopillars are epitaxial with the heavily doped layer;

the nanopillars are grown by a VLS method;

the junction layer is formed by ion implantation;

the readout lines are formed by deep etching; and/or

the gate lines are formed by depositing a metal layer.

16. A method of using the image sensor of claim 1, comprises:

exposing the pixels to light;

reading an electrical signal from a pixel by connecting at least one nanopillar in the pixel, using the gate electrode surrounding the at least one nanopillar, to external readout circuitry.

17. The method of claim 16, wherein the electrical signal is an electric charge accumulated on the at least one nanopillar, a change of electrical current through the at least one nanopillar, or a change of electrical impedance of the at least one nanopillar.

18. A method of using the image sensor of claim 8, comprises:

(a) applying a bias voltage to the transparent conductive layer;

(b) applying a first gate voltage to all the gate lines, the first gate voltage being effective to pinch off electrical current through the nanopillars;

(c) exposing the image sensor to light;

(d) connecting all the readout lines to ground to remove accumulated electrical charge thereon, then disconnecting all the readout lines from the ground;

(e) applying a second gate voltage to one of the gate lines, the second gate voltage being effective to allow electrical current through the nanopillars this one gate line surrounds;

(f) taking a current reading on at least one of the readout lines;

(g) applying the first gate voltage to this one gate line;

(h) optionally repeating steps (d)-(g) on each gate line.

19. An apparatus comprising the image sensor of claim **8**, a decoder connected to each gate line, and a trans-impedance amplifier and multiplexer circuit connected to each readout line.

20. The apparatus of claim **19**, wherein the trans-impedance amplifier and multiplexer circuit is functional to amplify an electrical current from each readout line and convert it into a voltage signal; the decoder and the trans-impedance amplifier and multiplexer circuit are synchronized by a common timing signal generated by a controller; and/or the decoder and the trans-impedance amplifier and multiplexer circuit are connected to the image sensor by wire-bonding, flip-chip bonding or bump bonding.

21. The image sensor of claim **8**, wherein the readout lines are parallel or have a fan-out shape, and/or the gate lines are parallel or have a fan-out shape.

22. A method of using the image sensor of claim **1** to scan an object, comprises:

converting reflected light from the object received by the pixels into analog electrical signals;

amplifying the analog electrical signals;

converting the amplified analog electrical signals to digital electrical signals using an analog-to-ditigal converter.

23. An apparatus comprising the image sensor of claim **1**, further comprises foreoptics, and a readout circuit, wherein the foreoptics are configured to receive light from a scene and focus or collimate the light onto the image sensor; and the readout circuit is connected to the image sensor and configured to receive output from the image sensor.

24. The apparatus of claim **23**, wherein the foreoptics comprise one or more of a lens, an optical filter, a polarizer, a diffuser, a collimator; and/or the readout circuit comprises one or more of ASICs, FPGAs, DSPs.

25. The image sensor of claim **1**, comprising at least one pixel comprising at least first, second, and third nanopillars having a size effective to absorb and/or detect light of about 650 nm, 510 nm and 475 nm in wavelength, respectively.

26. The image sensor of claim **1**, comprising at least one pixel comprising at least first, second, third and fourth nanopillars having a size effective to absorb and/or detect light of red, green, green and blue light, respectively.

27. The image sensor of claim **1**, further comprising a cladding surrounding at least one of the pixels or at least one of the nanopillars.

28. The image sensor of claim **27**, wherein the cladding is hafnium oxide or silicon nitride.

29. The image sensor of claim **1**, further comprising a micro lens on an upper end of the at least one nanopillar.

30. The image sensor of claim **1**, wherein the at least one nanopillar has an absorptance of at least 50% across an entire wavelength range from 400 nm to 800 nm.

* * * * *