CMOS Image Sensors: Electronic Camera-On-A-Chip

Eric R. Fossum, *Senior Member, IEEE*

***Abstract*—CMOS active pixel sensors (APS) have performance competitive with charge-coupled device (CCD) technology, and offer advantages in on-chip functionality, system power reduction, cost, and miniaturization. This paper discusses the requirements for CMOS image sensors and their historical development. CMOS devices and circuits for pixels, analog signal chain, and on-chip analog-to-digital conversion are reviewed and discussed.**

I. Introduction

TODAY there are many kinds of electronic cameras with very different characteristics. Camcorders are the most well known electronic camera and capture images with television resolution at 30 frames per second. Digital "still" charge-coupled device (CCD) cameras capture higher resolution images (e.g., 1280×1024 pixels) at slower frame rates. These cameras, while presently expensive for consumer applications, are expected to rapidly drop in price. Monochrome low-resolution (e.g., 300 000 pixels) CCD cameras are very inexpensive. Spaceborne, high-resolution scientific CCD cameras occupy the opposite end of the spectrum.

New markets are emerging for digital electronic cameras, especially in computer peripherals for document capture and visual communications. If the cost of the camera can be made sufficiently low (e.g., $100 or less per camera) it is expected that most personal computers will have at least one camera peripheral. Even less expensive cameras will find automotive and entertainment applications. Wireless applications of cameras will require ultra-low-power operation. Very small cameras (e.g., less than 10 cm^3) will also permit new markets.

Despite the wide variety of applications, all digital electronic cameras have the same basic functions. These are 1) optical collection of photons, i.e., a lens; 2) wavelength discrimination of photons, i.e., filters; 3) detector for conversion of photons to electrons, e.g., a photodiode; 4) a method to readout the detectors, e.g., a CCD; 5) timing, control, and drive electronics for the sensor; 6) signal processing electronics for correlated double sampling, color processing, etc.; 7) analog-to-digital conversion; and 8) interface electronics. In a CCD-based system, these functions often consume several watts of power (e.g., 1–5 W) and are therefore a major drain on a camcorder battery. The volume and mass of the electronics and power supply constrains the level of miniaturization achievable with the system.

Over the past five years, there has been a growing interest in CMOS image sensors. The major reason for this interest is customer demand for miniaturized, low-power, and cost-effective imaging systems. CMOS-based image sensors offer the potential opportunity to integrate a significant amount of VLSI electronics on-chip and reduce component and packaging costs. It is now straightforward to envision a single-chip camera that has integrated timing and control electronics, sensor array, signal processing electronics, analog-to-digital converter (ADC) and full digital interface. Such a camera-on-a-chip will operate with standard logic supply voltages and consume power measured in the tens of milliwatts [1], [2]. This paper reviews CMOS image sensor technology and the roadmap to achieve a camera-on-a-chip imaging system.

II. Historical Background

Before CMOS active pixel sensors (APS's) and before CCD's, there were MOS image sensors. In the 1960's there were numerous groups working on solid-state image sensors with varying degrees of success using NMOS, PMOS, and bipolar processes. For example, in 1963, Morrison reported a structure (that is now referred to as a computational sensor) that allowed determination of a light spot's position using the photoconductivity effect [3]. The *scanistor* was reported in 1964 by IBM [4]. The scanistor used an array of n-p-n junctions addressed through a resistive network to produce an output pulse proportional to the local incident light intensity. In 1966, Westinghouse reported a 50×50 element monolithic array of phototransistors [5]. All of these sensors had an output signal proportional to the instantaneous local incident light intensity and did not perform any intentional integration of the optical signal. As a consequence, the sensitivity of these devices was low and they required gain within the pixel to enhance their performance.

In 1967, Weckler at Fairchild suggested operating p-n junctions in a photon flux integrating mode [6]. The photocurrent from the junction is integrated on a reverse-biased p-n junction capacitance. Readout of the integrated charge using a PMOS switch was suggested. The signal charge, appearing as a current pulse, could be converted to a voltage pulse using a series resistor. A 100×100 element array of photodiodes was reported in 1968 [7]. Weckler later called the device a *reticon* and formed Reticon to commercialize the sensor.

Also in 1967, RCA reported a thin-film transistor (TFT) solid-state image sensor using CdS/CdSe TFT's and photocon-

Manuscript received April 9, 1997; revised May 18, 1997. The review of this paper was arranged by Editor E. R. Fossum. An earlier version of this paper appeared in the 1995 International Electron Devices Meeting Digest of Technical Papers and the Proceedings of the 1997 International Symposium on VLSI Technology, Systems, and Applications, Taipei, Taiwan.

The author is with Photobit, La Crescenta, CA 91214 USA.

Publisher Item Identifier S 0018-9383(97)06925-6.

0018–9383/97$10.00 © 1997 IEEE

ductors [8] The 180×180 element array included self-scanning complementary logic circuitry for sequentially addressing pixels. A battery operated wireless camera was also reported to have been constructed to demonstrate the array.

Also active at that time was Plessey in the U.K. In a 1968 seminal paper, Noble described several configurations of self-scanned silicon image detector arrays [9]. Both surface photodiodes and buried photodiodes (to reduce dark current) were described. Noble also discussed a charge integration amplifier for readout, similar to that used later by others. In addition, the first use of a MOS source-follower transistor in the pixel for readout buffering was reported. An improved model and description of the operation of the sensor was reported by Chamberlain in 1969 [10]. The issue of fixed-pattern noise (FPN) was explored in a 1970 paper by Fry, Noble, and Rycroft [11].

Until recently, FPN has been considered the primary problem with MOS and CMOS image sensors. In 1970, when the CCD was first reported [12], its relative freedom from FPN was one of the major reasons for its adoption over the many other forms of solid-state image sensors. The smaller pixel size afforded by the simplicity of the CCD pixel also contributed to its embrace by industry.

Since the CCD's inception, the main focus of research and development has been CCD sensor performance. The camcorder market has driven impressive improvements in CCD technology. Criteria include quantum efficiency, optical fill factor (fraction of pixel used for detection), dark current, charge transfer efficiency, smear, readout rate, lag, readout noise, and full well, i.e., dynamic range. A desire to reduce cost and optics mass has driven a steady reduction in pixel size. HDTV and scientific applications have driven an increase in array size. Recently, emphasis has been placed on improved CCD functionality, such as electronic shutter, low power, and simplified supply voltages. There have been several reports of integrating CMOS with CCD's to increase CCD functionality [13]–[15], but with the exception of some line arrays, the effort has not been fruitful due to both cost and the difficulty of driving the large capacitive loads of the CCD.

While a large effort was applied to the development of the CCD in the 1970's and 1980's, MOS image sensors were only sporadically investigated and compared unfavorably to CCD's with respect to the above performance criteria [16]. In the late 1970's and early 1980's Hitachi and Matsushita continued the development of MOS image sensors [17], [18] for camcorder-type applications, including single-chip color imagers [19]. Temporal noise in MOS sensors started to lag behind the noise achieved in CCD's, and by 1985, Hitachi combined the MOS sensor with a CCD horizontal shift register [20]. In 1987, Hitachi introduced a simple on-chip technique to achieve variable exposure times and flicker suppression from indoor lighting [21]. However, perhaps due to residual temporal noise, especially important in low light conditions, Hitachi abandoned its MOS approach to sensors.

It is interesting to note that in the late 1980's, while CCD's predominated in visible imaging, two related fields started to turn away from the use of CCD's. The first was hybrid infrared focal-plane arrays that intially used CCD's as a readout multiplexer. Due to limitations of CCD's, particularly in low-temperature operation and charge handling, CMOS readout multiplexers were developed that allowed both increased functionality as well as performance compared to CCD multiplexers [22]. A second field was high-energy physics particle/photon vertex detectors. Many workers in this area also initially used CCD's for detection and readout of charge generated by particles and photons. However, the radiation sensitivity of CCD's and the increased functionality offered by CMOS (e.g., [23]) has led to subsequent abandonment of CCD technology for this application.

In the early 1990's though, two independently motivated efforts have led to a resurgence in CMOS image sensor development. The first effort was to create highly functional single-chip imaging systems where low cost, not performance, was the driving factor. This effort was spearheaded by separate researchers at the University of Edinburgh in Scotland (later becoming VVL) and Linkoping University in Sweden (later becoming IVP). The second independent effort grew from NASA's need for highly miniaturized, low-power, instrument imaging systems for next-generation deep-space exploration spacecraft. Such imaging systems are driven by performance, not cost. This latter effort was led by the U.S. Jet Propulsion Laboratory (JPL) with subsequent transfer of the technology to AT&T Bell Labs, Kodak, National Semiconductor and several other major U.S. companies, and the startup of Photobit. The convergence of the efforts has led to significant advances in CMOS image sensors and the development of the CMOS APS. It has performance competitive with CCD's with respect to read noise, dynamic range, and responsivity but with vastly increased functionality, substantially lower system power (10–50 mW), and the potential for lower system cost.

Contributing to the recent activity in CMOS image sensors is the steady, exponential improvement in CMOS technology. The rate of minimum feature size decrease has outpaced similar improvements in CCD technology (see Fig. 1). Furthermore, sensor pixel size is limited by both optical physics and optics cost, making moot the CCD's inherent pixel size advantage for most applications. Recent progress in on-chip signal processing (and off-chip DSP) has also reduced CMOS image sensor FPN to acceptable levels. In addition, the transition from analog imaging and display systems to digital cameras tethered to PC's permits digital FPN correction with negligible system impact.

There are three predominant approaches to pixel implementation in CMOS: 1) passive pixel; 2) photodiode-type active pixel, and 3) photogate-type active pixel. These are described below. There are also several ways to make p-n junction photodiodes in CMOS [24], but generally n^+ diodes on a p/p^+ epi substrate in an n-well process give the most satisfactory results.

III. Overall Architecture

The overall architecture of a CMOS image sensor is shown in Fig. 2. The image sensor consists of an array of pixels that are typically selected a row at a time by row select logic. This can be either a shift register or a decoder. The pixels are

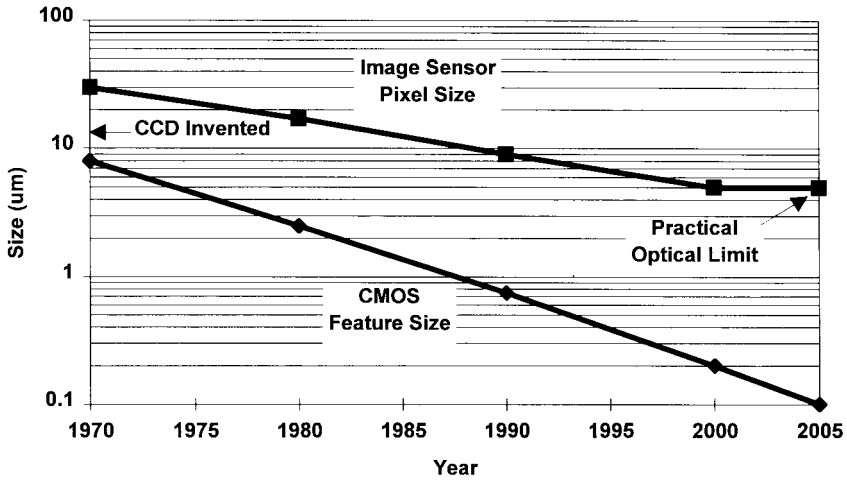


Fig. 1. The steadily increasing ratio between pixel size and minimum feature size permits the use of CMOS circuitry within each pixel.

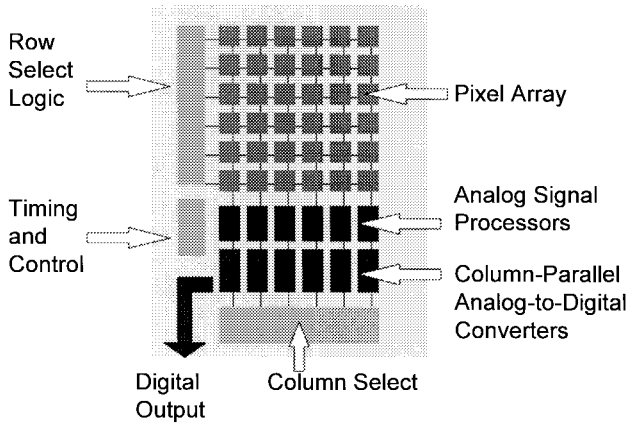


Fig. 2. CMOS APS integrates timing and control, ADC, and other circuitry on the same chip.

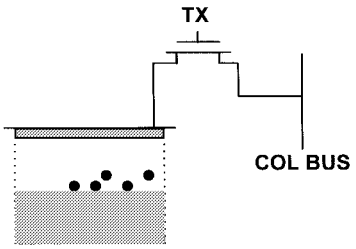


Fig. 3. Passive pixel schematic and potential well. When the transfer gate TX is pulsed, photogenerated charge integrated on the photodiode is shared on the bus capacitance.

read out to vertical column busses that connect the selected row of pixels to a bank of analog signal processors (ASP's). These ASP's perform functions such as charge integration, gain, sample and hold, correlated-double-sampling, and FPN suppression.

More advanced CMOS image sensors contain on-chip ADC's. In Fig. 2, the ADC's are shown as column-parallel ADCs; that is, each column of pixels has its own ADC. The digital output of the ADC's (or analog output of the ASP's) is selected for readout by column select logic that can be either a shift register or decoder. A timing and control logic block is also integrated on chip. This digital block is readily defined at a high level using tools such as VHDL and implemented on-chip using automated synthesis and place-and-route tools.

The CMOS image sensor architecture of Fig. 2 permits several modes of image readout. Progressive-scan readout of the entire array is the common readout mode. A *window* readout mode is readily implemented where only a smaller region of pixels is selected for readout. This increases access rates to windows of interest. A *skip* readout mode is also possible where every second (or third, etc.) pixel is readout. This mode allows for subsampling of the image to increase readout speed at the cost of resolution. Combination of skip and window modes allows electronic pan, tilt and zoom to be implemented.

IV. Pixel Circuits

Pixel circuits can be divided into *passive* pixels and *active* pixels. The active pixel sensor (APS) contains an active amplifier. There are three predominant approaches to pixel implementation in CMOS: photodiode-type passive pixel, photodiode-type active pixel, and photogate-type active pixel. These are described below.

A. Passive Pixel Approach

The photodiode-type passive pixel approach remains virtually unchanged since first suggested by Weckler in 1967 [6], [7]. The passive pixel concept is shown below in Fig. 3. It consists of a photodiode and a pass (access) transistor. When the access transistor is activated, the photodiode is connected to a vertical column bus. A charge integrating amplifier (CIA) readout circuit at the bottom of the column bus keeps the voltage on the column bus constant and reduces kTC noise [9]. When the photodiode is accessed, the voltage on the photodiode is reset to the column bus voltage, and the charge, proportional to the photosignal, is converted to a voltage by the CIA. The single-transistor photodiode passive pixel allows the highest design fill factor for a given pixel size or the smallest pixel size for a given design fill factor for a particular CMOS process. A second selection transistor has sometimes been

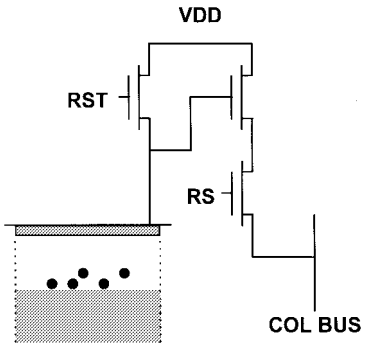


Fig. 4. A photodiode-type active pixel sensor (APS). The voltage on the photodiode is buffered by a source follower to the column bus, selected by RS-row select. The photodiode is reset by transistor RST.

added to permit true X-Y addressing. The quantum efficiency of the passive pixel (ratio of collected electrons to incident photons) can be quite high due to the large fill factor and absence of an overlying layer of polysilicon such as that found in many CCD's. This passive pixel is the basis for arrays produced by EG&G Reticon, Hitachi [17], Matsushita [18] and more recently, by Edinburgh University and VLSI Vision in Scotland [25], [26], Linkoping University and IVP in Sweden [27]–[29], and Toyohashi University [30].

Much larger pixels have been used for document imaging [31]. Page-sized image sensors $(7.7'' \times 9.6'')$ using amorphous silicon and constructed with a passive pixel architecture have been demonstrated with a dynamic range of 10^4–10^5.

The major problems with the passive pixel are its readout noise level and scalability. Readout noise with a passive pixel is typically of the order of 250 electrons r.m.s., compared to commercial CCD's that achieve less than 20 electrons r.m.s. of read noise. The passive pixel also does not scale well to larger array sizes and or faster pixel readout rates. This is because increased bus capacitance and faster readout speed both result in higher readout noise.

B. Active Pixel Approach

It was quickly recognized, almost as soon as the passive pixel was invented, that the insertion of a buffer/amplifier into the pixel could potentially improve the performance of the pixel. A sensor with an active amplifier within each pixel is referred to as an active pixel sensor or APS. Since each amplifier is only activated during readout, power dissipation is minimal and is generally less than a CCD. Non-CMOS APS devices have been developed that have excellent performance, such as the charge-modulation device (CMD) [32], but these devices [33]–[35] require a specialized fabrication process. In general, APS technology has many potential advantages over CCD's [36] but is susceptible to residual FPN and has less maturity than CCD's.

The CMOS APS trades pixel fill factor for improved performance compared to passive pixels using the in-pixel amplifier. Pixels are typically designed for a fill factor of 20–30%, similar to interline-transfer (ILT) CCD's. Loss in optical signal is more than compensated by reduction in read noise for a net increase in signal-to-noise (S/N) ratio and dynamic range. Microlenses are commonly employed with low fill factor ILT CCD's [37], [38] and can recover some of the lost optical signal. The simple, polyimide microlense refracts incident radiation from the circuitry region of the pixel to the detector region, but the loss in the microlense material and the inherent sensitivity of the CMOS APS to lateral carrier collection means that the effective improvement in sensitivity with a microlense may be two-fold.

C. Photodiode-Type APS

The photodiode-type (PD) APS was described by Noble in 1968 [9] and has been under investigation by Andoh at NHK in Japan since the late 1980's [39]–[41] in collaboration with Olympus, and later, Mitsubishi Electric. A similar device with an a-Si:H overlayer to improve effective fill factor was described by Huang and Ando in 1990 [42]. A diagram of the PD-APS is shown in Fig. 4.

The first high-performance PD-APS was demonstrated by JPL in 1995 in a 128×128 element array that had on-chip timing, control, correlated double sampling and fixed pattern noise (FPN) suppression circuitry [43]. The chip achieved 72 dB dynamic range with FPN less than 0.15% saturation. A 640×480 PD-APS with 5.6×5.6 μm pixels and on-chip color filter arrays and microlenses was described by Toshiba in 1997 [44], and a 800×1000 element PD-APS was reported by VLSI Vision also in 1997 [45].

More complicated pixels can be constructed to improve functionality and, to a lesser extent, performance. Hamamatsu reported on an improved sensor that used a transfer gate between the photodiode and the source follower gate [46]. The transfer gate keeps the photodiode at constant potential and increases output conversion gain by reducing capacitance but introduces lag. The Hamamatsu sensor also improved FPN using a feedback technique. More complication was added by the Technion to permit random access and electronic shuttering with a significant increase in pixel size [47]. Similar work was reported recently by Stanford [48]. A method for individual pixel reset for regional electronic shutter was presented by JPL [49]. Current-mode readout of CMOS APS has been investigated [50], and reported by Polaroid [51]. Gain and offset FPN remain a challenge in current mode.

Photodiode-type APS pixels have high quantum efficiency as there is no overlying polysilicon. The read noise is limited by the reset noise on the photodiode since correlated double sampling is not easily implementable without frame memory, and is thus typically 75–100 electrons r.m.s. The photodiode-type APS uses three transistors per pixel and has a typical pixel pitch of $15\times$ the minimum feature size (see Fig. 5). The photodiode APS is suitable for most mid to low-performance applications. The output signal remains constant for the same optical flux, to first order, since a decrease in detector area is compensated by an increase in conversion gain. Its S/N performance decreases for smaller pixel sizes since the reset voltage noise scales as $1/C^{1/2}$, where C is the photodiode capacitance. A tradeoff can be made in designed pixel fill-factor (photodiode area), dynamic range (full well) and conversion gain (μV/e$^-$). Lateral carrier collection permits



Fig. 5. Close-up of 11.9-μm pixel photodiode-type active pixels used in the 1024×1024 array shown in Fig. 11.

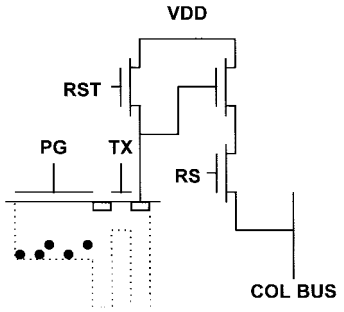


Fig. 6. Photogate-type APS pixel schematic and potential wells. Transfer of charge and correlated double sampling permits low-noise operation.

high responsivity even for small fill-factor [52] at the possible expense of pixel-to-pixel crosstalk.

D. Photogate-Type APS

The photogate APS was introduced by JPL in 1993 [53]–[55] for high-performance scientific imaging and low-light applications. The photogate APS combines CCD benefits and X-Y readout, and is shown schematically below in Fig. 6. Signal charge is integrated under a photogate. For readout, an output floating diffusion is reset and its resultant voltage measured by the source follower. The charge is then transferred to the output diffusion by pulsing the photogate. The new voltage is then sensed. The difference between the reset level and the signal level is the output of the sensor. This correlated double sampling suppresses reset noise, $1/f$ noise, and FPN due to threshold voltage variations.

The photogate and transfer gate ideally overlap using a double poly process. However, the insertion of a bridging diffusion between PG and TX has minimal effect on circuit

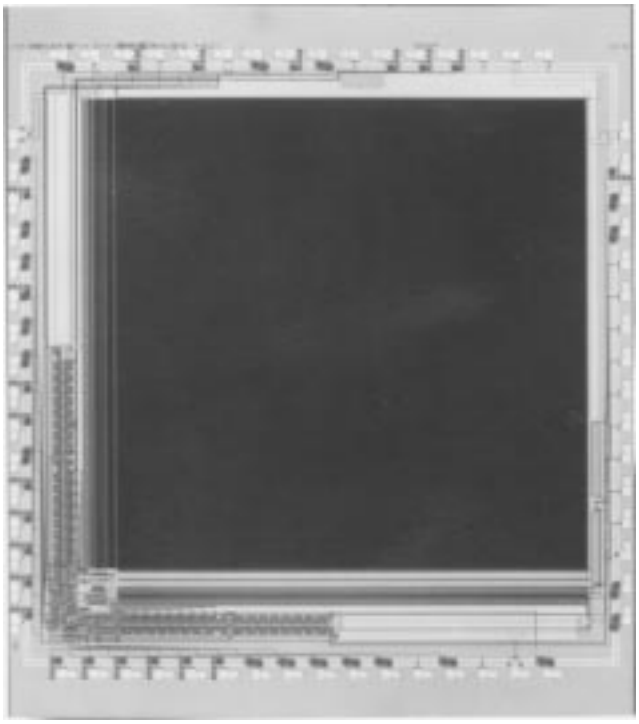


Fig. 7. A JPL 256×256 element PG-APS with on-chip timing and control circuits (left side) and analog signal chain including FPN suppression (bottom).

performance and permits the use of single poly processes [56]. (Approximately 100 e^- of lag has been attributed to the bridging diffusion [57]). A 256×256 element CMOS APS with 20.4 μm pixels implemented using a 1.2-μm n-well process with on-chip timing and control logic with 13 e^- r.m.s. read noise was reported by JPL [58]. This sensor required only 5 V and clock to produce analog video output (see Fig. 7). Variable integration time and window of interest readout is commanded asynchronously. Arrays as large as 1024×1024 with 10-μm pixel pitch in a 0.5-μm process have been developed by a JPL/AT&T collaboration [59] (Fig. 8).

The photogate-type APS uses five transistors per pixel and has a pitch typically equal to $20\times$ the minimum feature size. Thus, to achieve a 10-μm pixel pitch, a 0.5-μm process must be employed. A 0.25-μm process would permit a 5-μm pixel pitch. The floating diffusion capacitance is typically of the order of 10 fF yielding a conversion gain of 10–20 μV/e^-. Subsequent circuit noise is of the order of 150–250 μV r.m.s., resulting in a readout noise of 10–20 electrons r.m.s., with the lowest noise reported to date of 5 electrons r.m.s. [52]. The advantage in read noise for the photogate pixel is offset by a reduction in quantum efficiency, particularly in the blue, due to overlying polysilicon.

E. Logarithmic Pixels

In some cases, nonlinear output of the sensor is desired. Non-linear output permits an increase in intra-scene dynamic range as the photosignal is companded. Gamma-correction (basically a square-root transform) is one example of companding. A second example is logarithmic transformation, where the output signal from the pixel is proportional to the logarithm



Fig. 8. 1024×1024 element photogate CMOS APS with 10-μm pixel pitch fabricated using 0.5-μm design rules by AT&T/JPL.

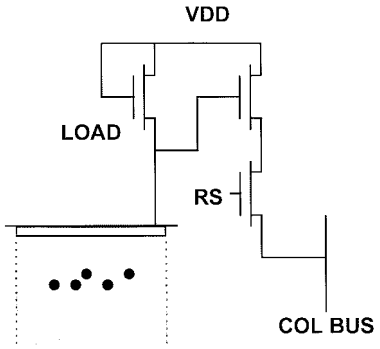


Fig. 9. Logarithmic pixel schematic circuit.



Fig. 10. Unprocessed image taken from a Photobit 256×256 element sensor with on-chip ADC operating at 30 frame/s. Note no blooming from light and lack of other artifacts.

of the photosignal [60]–[62]. An example of this type of pixel circuit [63] is shown in Fig. 9.

The photodiode voltage self-adjusts to a level such that the load transistor current is equal to the photocurrent collected by the photodiode. This results in a logarithmic transformation of the photosignal for typical light levels and wide intrascene dynamic range. The logarithmic pixel permits true random access in both space and time since it is a nonintegrating pixel. Drawbacks to this nonintegrating approach include slow response time for low light levels, and large FPN (e.g., 60 mV). Although able to cover over six orders of magnitude in incident light level, the sensor has a small signal-to-noise ratio (45 dB) due to temporal noise and small voltage swings.

A nonintegrating 512×512 element photodiode-type APS was reported by IMEC with a 6.6-μm pixel pitch [64]. This sensor operates in a nonintegrating current mode with logarithmic response. FPN was corrected by means of hot-carrier-induced threshold voltage shift. A 2048×2048 element logarithmic pixel sensor with 7.5-μm pixel pitch has also been reported [65].

F. Other Pixels

The pinned photodiode, developed for interline transfer CCD's, features high quantum efficiency (especially in the blue), low dark current, and low noise readout. The pinned photodiode has been combined with CMOS APS readout by JPL/Kodak to achieve high-performance pixel response [66].

A photogate CMOS APS with a floating-gate sense amplifier that allows multiple nondestructive, doubly sampled reads of the same signal was developed by JPL for use with oversampled column-parallel ADC's [67].

A floating gate sensor with a simple structure was reported by JPL/Olympus [68]. This sensor used a floating gate to collect and sense the photosignal and features a compact pixel layout with complete reset.

There has been significant work on retina-like CMOS sensors with nonlinear, adaptive response. While their utility for electronic image capture has not yet been demonstrated, their very large dynamic range and similarity to the response of the human eye offer intriguing possibilities for on-chip intelligent imaging [69], [70].

V. Analog Signal Processing

On-chip analog signal processing can be used to improve the performance and functionality of the CMOS image sensor. A charge integration amplifier is used for passive pixel sensors and sample and hold circuits typically employed for active pixel sensors. JPL has developed a delta-difference sampling (DDS) approach to suppress FPN peak-to-peak to 0.15% of saturation level [43]. Other examples of signal processing demonstrated in CMOS image sensors include smoothing using neuronMOSFET's [71], motion detection [72], [73], programmable amplification [74], multiresolution imaging [75], video compression [76], dynamic range en-

hancement [77], discrete cosine transform (DCT) [30], and intensity sorting [78]. Continued improvement in analog signal processing performance and functionality is expected. Other computational-type optical sensors have been demonstrated that use CMOS analog signal processing [79], [80].

VI. On-Chip Analog-to-Digital Converter (ADC)

To implement a camera-on-a-chip with a full digital interface requires an on-chip ADC. There are many considerations for on-chip ADC. The ADC must support video rate data that ranges from 0.92 Msamples/s for a 320×288 format sensor operating at 10 frame/s for videoconferencing, to 55.3 Msamples/s for a 1280×720 format sensor operating at 60 frames/s. The ADC must have at least 8b resolution with low integral nonlinearity (INL) and differential nonlinearity (DNL) so as not to introduce distortion or artifacts into the image (see Fig. 10). The ADC can dissipate only minimal power, typically under 100 mW, to avoid introduction of hot spots with excess dark current generation. The ADC cannot consume too much chip area or it will void the economic advantage of on-chip integration. The ADC cannot introduce noise into the analog imaging portion of the sensor through substrate coupling or other crosstalk mechanisms that would deteriorate image quality.

CMOS image sensors with on-chip single-slope ADC have been reported [29], [81] as has related work in on-chip ADC's for infrared focal-plane array readout [82], [83], [84]. There are many considerations for implementation of on-chip ADC [85], [86]. The ADC can be implemented as a single serial ADC (or several ADC's, e.g., one per color) that operate at near video rates [10 Msamples/s]. The ADC can also be implemented in-pixel [87]–[89] and operate at frame rates [e.g., 30 samples/s]. We have been pursuing column-parallel ADC's where each (or almost each) column in the pixel array has its own ADC (see Fig. 2) so that each ADC operates at the row rate [e.g., 15 ksamples/s]. In this architecture, single-slope ADC's work well for slow-scan applications (Fig. 11) but dissipate too much power for video-rates. Oversampled ADC's require significant chip area when implemented in column-parallel formats [67]. A successive approximation ADC has a good compromise of power, bit resolution, and chip area. On-chip ADC enables on-chip DSP for sensor control and compression preprocessing.

VII. Impact of CMOS Scaling Trends

The future prospects for CMOS image sensors are bright. There has been rapid progress in realizing cost-effective pixel sizes (see Fig. 12). The effect of predictable trends in CMOS technology, based on the industry standard technology roadmap, were examined by Fossum and Wong of JPL/IBM [90], [91]. To at least 0.25 μm minimum feature sizes, it appears that the standard CMOS process will permit the fabrication of high-performance CMOS image sensors.

The most obvious problem, but the easiest to correct, is the trend toward the use of silicides. Silicides are optically opaque and detrimental to image sensing. A silicide-blocking mask is already available in some processes. The switchover



Fig. 11. A JPL 1024×1024 photodiode-type CMOS APS with 1024 column-parallel single-slope ADC's for slow-scan scientific applications.

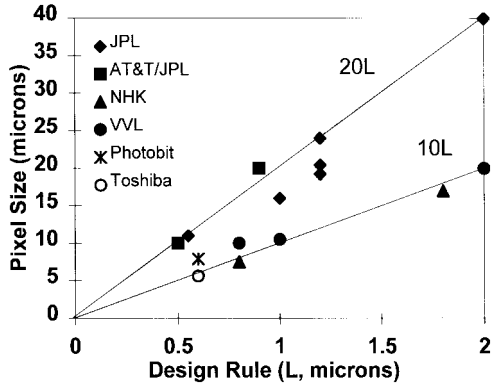


Fig. 12. Scaling trend in pixel size versus design rule. It is expected that pixel pitch must be between 5 μm and 10 μm to be competitive.

to silicon-on-insulator (SOI) technology will be problematic for the sensors due to the minimal absorption of photons in thin silicon films, but such a switchover is not expected to generally occur until beyond 0.25 μm minimum feature sizes. Active pixel sizes at the "practical lens limit" (e.g., 5 μm) will be readily achievable in 0.25 μm CMOS. Passive pixel sizes well below that size will also be achievable.

Below 0.25 μm, "off" transistor currents may be of concern. Dark current is expected to minimally increase from 0.5 μm processes to 0.25 μm processes. This will likely be compensated by a steady improvement in wafer and process quality control. Intrinsic FPN may increase due to threshold voltage mismatch, but FPN suppression circuitry will likely become more sophisticated as well. A switch from LOCOS to shallow trench isolation would likely improve sensor performance. Deep trench isolation would be useful to reduce crosstalk. Reduced power supply voltages will reduce analog circuitry "headroom", but is partially offset by concomitant reduction in threshold voltages. Increases in DRAM chip size will drive improvements in process control as well as stepper field size—useful for larger format image sensors.

Samsung Exhibit 1052, Page 7 of 10

It is inevitable that when CMOS image sensors capture a significant share of the electronic imaging market, process deviations from standard CMOS will be made to permit product differentiation and improved performance. This is already the case with analog CMOS for capacitors and isolation. Use of the pinned photodiode [66] will improve quantum efficiency and decrease dark current. Double poly will permit efficient implementation of capacitors.

VIII. Roadmap for Camera-on-a-Chip

All the component technologies to realize a CMOS electronic camera-on-a-chip have been developed. Single-chip cameras based on the lower performance passive pixel are already available. Higher performance single-chip cameras based on the CMOS APS technology are expected to emerge shortly. Improvement in on-chip ADC technology to take advantage of the high dynamic range is needed. Backend processes for color filter arrays and microlenses are nearly as complicated as the standard CMOS process and add significantly to cost. A single-chip color camera can be expected in the next year or two. Standards for digital cameras need to be developed to enable the wider development of the technology.

It can be anticipated that both CCD and CMOS-based imaging systems will converge to two-chip solutions. The CMOS imaging system is probably best partitioned into an image acquisition and compression preprocessing sensor, and a separate compression and color interpolation/filter DSP and frame buffer chip. CCD imaging systems will likely evolve to a CCD with a separate single CMOS IC for timing, control, drivers, signal processing, ADC and compression DSP. However, the low power and functionality advantages of the CMOS image sensor will permit continued market insertion of CMOS-based imaging technology.

IX. Conclusion

Highly miniaturized imaging systems based on CMOS image sensor technology are emerging as a competitor to CCD's for low-cost visual communications and multimedia applications. The CMOS active pixel sensor (APS) technology has demonstrated noise, quantum efficiency, and dynamic range performance comparable to CCD's with greatly increased functionality and much lower system power. CMOS image sensors with on-chip timing and control, and analog-to-digital conversion are enabling one-chip imaging systems with a full digital interface. Such a "camera-on-a-chip" may make image capture devices as ubiquitous in our daily lives as the microprocessor.

Acknowledgment

The author gratefully acknowledges the assistance of colleagues in North America, Asia, and Europe, too numerous to name individually, in the preparation of this manuscript. The assistance of J. Nakamura and J. Li in tracking down papers is greatly appreciated. The stories told to me of the early days of MOS imaging devices by G. Weckler, R. Dyck and S. Chamberlain were interesting and are also appreciated. The author appreciates the support of his former group at JPL, the present group at Photobit, and especially S. Kemeny in the preparation of this updated manuscript.

References

[1] E. R. Fossum, "CMOS image sensors: Electronic camera-on-a-chip," in *IEEE IEDM Tech. Dig.*, 1995, pp. 17–25.
[2] B. Ackland and A. Dickinson, "Camera-on-a-chip," in *1996 ISSCD Tech. Papers*, 1996, pp. 22–25.
[3] S. Morrison, "A new type of photosensitive junction device," *Solid-State Electron.*, vol. 5, pp. 485–494, 1963.
[4] J. Horton, R. Mazza, and H. Dym, "The scanistor—A solid-state image scanner," in *Proc. IEEE*, vol. 52, pp. 1513–1528, 1964.
[5] M. A. Schuster and G. Strull, "A monolithic mosaic of photon sensors for solid state imaging applications," *IEEE Trans. Electron Devices*, vol. ED-13, pp. 907–912, 1966.
[6] G. P. Weckler, "Operation of p-n junction photodetectors in a photon flux integration mode," *IEEE J. Solid-State Circuits*, vol. SC-2, pp. 65–73, 1967.
[7] R. Dyck and G. Weckler, "Integrated arrays of silicon photodetectors for image sensing," *IEEE Trans. Electron Devices*, vol. ED-15, pp. 196–201, Apr. 1968.
[8] P. K. Weimer, G. Sadasiv, J. Meyer, L. Meray-Horvath, and W. Pike, "A self-scanned solid-state image sensor," in *Proc. IEEE*, vol. 55, pp. 1591–1602, 1967.
[9] P. Noble, "Self-scanned silicon image detector arrays," *IEEE Trans. Electron Devices*, vol. ED-15, pp. 202–209, Apr. 1968.
[10] S. G. Chamberlain, "Photosensitivity and scanning of silicon image detector arrays," *IEEE J. Solid-State Circuits*, vol. SC-4, pp. 333–342, June 1969.
[11] P. Fry, P. Noble, and R. Rycroft, "Fixed pattern noise in photomatrices," *IEEE J. Solid-State Circuits*, vol. SC-5, pp. 250–254, May 1970.
[12] W. S. Boyle and G. E. Smith, "Charge-coupled semiconductor devices," *Bell Syst. Tech. J.*, vol. 49, pp. 587–593, 1970.
[13] R. Dawson, J. Preisig, J. Carnes, and J. Pridgen, "A CMOS/buried-n-channel CCD compatible process for analog signal processing applications," *RCA Rev.*, vol. 38, no. 3, pp. 406–435, 1977.
[14] D. Ong, "An all-implanted CCD/CMOS process," *IEEE Trans. Electron Devices*, vol. ED-28, pp. 6–12, Jan. 1981.
[15] C. Anagnostopoulos, C. Ludden, G. Brown, and K. Wong, "An integrated CMOS/CCD sensor for camera autofocus," in *Electronic Imaging '88: Int. Electron. Imag. Expo. and Conf.*, Waltham, MA, 1988, vol. 1, pp. 159–163.
[16] R. Melen, "The tradeoff in monolithic image sensors: MOS versus CCD," *Electron.*, vol. 46, pp. 106–111, May 1973.
[17] S. Ohba *et al.*, "MOS area sensor: Part II—Low noise MOS area sensor with anti-blooming photodiodes," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1682–1687, Aug. 1980.
[18] K. Senda, S. Terakawa, Y. Hiroshima, and T. Kunii, "Analysis of charge-priming transfer efficiency in CPD image sensors," *IEEE Trans. Electron Devices*, vol. ED-31, pp. 1324–1328, Sept. 1984.
[19] M. Aoki *et al.*, "A 2/3-inch format MOS single-chip color imager," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 745–750, Apr. 1982.
[20] H. Ando *et al.*, "Design consideration and performance of a new MOS imaging device," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 1484–1489, May 1985.
[21] T. Kinugasa *et al.*, "An electronic variable shutter system in video camera use," *IEEE Trans. Consumer Electron.*, vol. CE-33, pp. 249–255, 1987.
[22] See, for example, *Infrared Readout Electronics, Proc. SPIE*, vol. 1684, 1992.
[23] B. Dierckx, "XYW detector: A smart two-dimensional particle sensor," *Nucl. Instrum. Methods Phys. Res. A*, vol. 275, p. 527, 1989.
[24] P. Aubert, H. Oguey, and R. Vuillemier, "Monolithic optical position encoder with on-chip photodiodes," *IEEE J. Solid-State Circuits*, vol. 23, pp. 465–472, 1988.
[25] D. Renshaw, P. Denyer, G. Wang, and M. Lu, "ASIC image sensors," in *IEEE Int. Symp. Circuits and Syst.*, 1990, pp. 3038–3041.
[26] P. Denyer, D. Renshaw, G. Wang, and M. Lu, "CMOS image sensors for multimedia applications," in *Proc. IEEE Custom Int. Circuits Conf.*, 1993, pp. 11.5.1–11.5.4.
[27] K. Chen, M. Afghahi, P. Danielsson, and C. Svensson, "PASIC—A processor-A/D converter sensor integrated circuit," in *IEEE Int. Symp. Circuits and Syst.*, 1990, pp. 1705–1708.
[28] R. Forchheimer, P. Ingelhag, and C. Jansson, "MAPP2200: A second generation smart optical sensor," *Image Processing and Interchange, Proc. SPIE*, vol. 1659, pp. 2–11, 1992.

[29] C. Jansson, O. Ingelhag, C. Svensson, and R. Forchheimer, "An addressable 256×256 photodiode image sensor array with an 8-bit digital output," *Analog Integrated Circuits and Signal Processing*, vol. 4, pp. 37–49, 1993.
[30] S. Kawahito, M. Yoshida, M. Sasaki, K. Umehara, Y. Tadokara, K. Murata, S. Doushou, and A. Matsuzawa, "A compressed digital output CMOS image sensor with analog 2-D DCT processors and ADC quantizer," in *ISSCC Dig. Tech. Papers*, 1997, pp. 184–185.
[31] X. Wu, R. Street, R. Weisfield, D. Begelson, W. Jackson, D. Jared, S. Ready, and R. Apte, "Large format a-Si:H two-dimensional array as imaging devices," presented at *1995 IEEE Workshop CCD's and Advanced Image Sensors*, Dana Point, CA, Apr. 20–22, 1995.
[32] K. Matsumoto *et al*., "A new MOS phototransistor operating in a nondestructive readout mode," *Jpn. J. Appl. Phys.*, vol. 24, no. 5, pp. L323–L325, 1985.
[33] A. Yusa *et al*., "SIT image sensor: design considerations and characteristics," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 735–742, June 1986.
[34] N. Tanaka *et al*., "A 310 pixel bipolar imager (BASIS)," *IEEE Trans. Electron Devices*, vol. 37, pp. 964–971, Apr. 1990.
[35] J. Hynecek, "A new device architecture suitable for high-resolution and high-performance image sensors," *IEEE Trans. Electron Devices*, vol. 35, pp. 646–652, Mar. 1988.
[36] E. R. Fossum, "Active pixel sensors—Are CCD's dinosaurs?," *Charge-Coupled Devices and Optical Sensors III, Proc. SPIE*, vol. 1900, pp. 2–14, 1993.
[37] Y. Ishihara and K. Tanigaki, "A high sensitivity IL-CCD image sensor with monolithic resin lens array," in *IEEE IEDM Tech. Dig.*, 1983, pp. 497–500.
[38] Y. Sano, T. Nomura, H. Aoki, S. Terakawa, H. Kodama, T. Aoki, and Y. Hiroshima, "Submicron spaced lens array process technology for a high photosensitivity CCD image sensor," in *IEEE IEDM Tech. Dig.*, 1990, pp. 283–286.
[39] F. Andoh, K. Taketoshi, J. Yamazaki, M. Sugawara, Y. Fujita, K. Mitani, Y. Matuzawa, K. Miyata, and S. Araki, "A 250 000 pixel image sensor with FET amplification at each pixel for high-speed television cameras," in *ISSCC Dig. Tech. Papers*, 1990, pp. 212–213.
[40] H. Kawashima, F. Andoh, N. Murata, K. Tanaka, M. Yamawaki, and K. Taketoshi, "A 1/4 inch format 250 000 pixel amplifier MOS iamge sensor using CMOS process," in *IEEE IEDM Tech. Dig.*, 1993, pp. 575–578.
[41] M. Sugawara, H. Kawashima, F. Andoh, N. Murata, Y. Fujita, and M. Yamawaki, "An amplified MOS imager suited for image processing," in *ISSCC Dig. Tech. Papers*, 1994, pp. 228–229.
[42] Z.-S. Huang and T. Ando, "A novel amplified image sensor with a-Si:H photoconductor and MOS transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 1432–1438, June 1990.
[43] R. H. Nixon, S. E. Kemeny, C. O. Staller, and E. R. Fossum, "128×128 CMOS photodiode-type active pixel sensor with on-chip timing, control and signal chain electronics," *Charge-Coupled Devices and Solid-State Optical Sensors V, Proc. SPIE*, vol. 2415, pp. 117–123, 1995.
[44] E. Oba, K. Mabuchi, Y. Iida, N. Nakamura, and H. Miura, "A 1/4-inch 330 k square pixel progressive scan CMOS active pixel image sensor," *ISSCC Dig. Tech. Papers*, San Francisco CA, Feb. 1997, pp. 180–181.
[45] P. Denyer, J. E. Hurwitz, D. J. Baxter, and G. Townsend, "800 k-pixel CMOS sensor for consumer still cameras," *Solid-State Sensor Arrays: Development and Applications, Proc. SPIE*, vol. 3019, pp. 115–124, 1997.
[46] M. Kyomasu, "New MOS imager using photodiode as current source," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1116–1122, Aug. 1991.
[47] O. Yadid-Pecht, R. Ginosar, and Y. Diamand, "A random access photodiode array for intelligent image capture," *IEEE. Trans. Electron Devices*, vol. 38, pp. 1772–1780, Aug. 1991.
[48] C. Aw and B. Wooley, "A 128×128 pixel standard CMOS image sensor with electronic shutter," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1922–1930, Dec. 1996.
[49] O. Yadid-Pecht, B. Pain, C. Staller, C. Clark, and E. R. Fossum, "CMOS active pixel sensor star tracker with regional electronic shutter," *IEEE J. Solid-State Circuits*, vol. 32, pp. 285–288, Feb. 1997.
[50] B. Pain and E. R. Fossum, unpublished.
[51] R. D. McGrath, V. Clark, P. Duane, L. McIlrath, and W. Washkurak, "Current-mediated, current-reset 768×512 active pixel sensor array," *ISSCC Dig. Tech. Papers*, 1997, pp. 182–183.
[52] O. Yadid-Pecht, B. Pain, B. Mansoorian, and E. R. Fossum, "Optimization of active pixel sensor noise and responsivity for scientific applications," *Solid-State Sensor Arrays: Development and Applications, Proc. SPIE*, vol. 3019, pp. 125–136, 1997.
[53] S. Mendis, S. Kemeny, and E. R. Fossum, "A 128×128 CMOS active pixel image sensor for highly integrated imaging systems," in *IEEE IEDM Tech. Dig.*, 1993, pp. 583–586.
[54] ———, "CMOS active pixel image sensor," *IEEE Trans. Electron Devices*, vol. 41, pp. 452–453, Mar. 1994.
[55] S. K. Mendis, S. E. Kemeny, R. C. Gee, B. Pain, Q. Kim, and E. R. Fossum, "CMOS active pixel image sensors for highly integrated imaging systems," *IEEE J. Solid-State Circuits*, vol. 32, pp. 187–197, Feb. 1997.
[56] S. Mendis, S. E. Kemeny, R. Gee, B. Pain, and E. R. Fossum, "Progress in CMOS active pixel image sensors," *Charge-Coupled Devices and Solid State Optical Sensors IV, Proc. SPIE*, vol. 2172, pp. 19–29, 1994.
[57] E. R. Fossum, 1996, unpublished.
[58] R. H. Nixon, S. E. Kemeny, B. Pain, C. O. Staller, and E. R. Fossum, "256×256 CMOS active pixel sensor camera-on-a-chip," *IEEE J. Solid-State Circuits*, vol. 31, pp. 2046–2050, Dec. 1996.
[59] A. Dickinson, S. Mendis, B. Ackland, D. Inglis, K. Azadet, P. Jones, and E. R. Fossum, 1995, unpublished.
[60] S. G. Chamberlain and J. Lee, "A novel wide dynamic range silicon photodetector and linear imaging array," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1983, pp. 441–445.
[61] C. Mead, "A sensitive electronic photoreceptor," in *1985 Chapel Hill Conf. VLSI*, pp. 463–471.
[62] J. Mann, "Implementing early visual processing in analog VLSI: Light adaptation," *Visual Information Processing: From Neurons to Chips, Proc. SPIE*, vol. 1473, pp. 128–132, 1991.
[63] N. Ricquier and B. Dierickx, "Pixel structure with logarithmic response for intelligent and flexible imager architectures," *Microelectron. Eng.*, vol. 19, pp. 631–634, 1992.
[64] ———, "Active pixel CMOS image sensor with on-chip nonuniformity correction," presented at *1995 IEEE Workshop on CCD's and Advanced Image Sensors*, Dana Point, CA, Apr. 20–22, 1995.
[65] B. Dierickx, D. Scheffer, G. Meynants, W. Ogiers, and J. Vlummens, "Random addressable active pixel image sensors," *AFPAEC Europto, Proc. SPIE*, vol. 2950, p. 1, 1996.
[66] P. Lee, R. Gee, M. Guidash, T. Lee, and E. R. Fossum, "An active pixel sensor fabricated using CMOS/CCD process technology," presented at *1995 IEEE Workshop on CCD's and Advanced Image Sensors*, Dana Point, CA, Apr. 20–22, 1995.
[67] S. Mendis, B. Pain, R. Nixon, and E. R. Fossum, "Design of a low-light-level image sensor with an on-chip sigma-delta analog-to-digital conversion," *Charge-Coupled Devices and Optical Sensors III, Proc. SPIE*, vol. 1900, pp. 31–39, 1993.
[68] J. Nakamura, S. E. Kemeny, and E. R. Fossum, "A CMOS active pixel image sensor with simple floating gate pixels," *IEEE Trans. Electron Devices*, vol. 42, pp. 1693–1694, Sept. 1995.
[69] *Visual Information Processing: From Neurons to Chips, Proc. SPIE*, vol. 1473, 1991.
[70] C. H. Koch and H. Li, Eds., *Vision Chips: Implementing Vision Algorithms with Analog VLSI Circuits*. New York: IEEE Computer Soc. Press, 1995.
[71] J. Nakamura and E. R. Fossum, "Design of an image sensor using a neuron MOSFET with image smoothing capability,"*Charge-Coupled Devices and Solid State Optical Sensors IV, Proc. SPIE*, vol. 2172, pp. 30–37, 1994.
[72] A. Dickinson, B. Ackland, E.-S. Eid, D. Inglis, and E. R. Fossum, "A 256×256 CMOS active pixel image sensor with motion detection," in *ISSCC Dig. Tech. Papers*, 1995, pp. 226–227.
[73] A. Simoni, G. Torelli, F. Maloberti, A. Sartori, S. Plevridis, and A. Birbas, "A single-chip optical sensor with analog memory for motion detection," *IEEE J. Solid-State Circuits*, vol. 30, pp. 800–805, July 1995.
[74] Z. Zhou, S. E. Kemeny, B. Pain, R. C. Gee, and E. R. Fossum, "A CMOS active pixel sensor with amplification and reduced fixed pattern noise," presented at *1995 IEEE Workshop on CCD's and Advanced Image Sensors*, Dana Point, CA, Apr 20–22, 1995.
[75] S. E. Kemeny, B. Pain, R. Panicacci, L. Matthies, and E. R. Fossum, "CMOS active pixel sensor array with programmable multiresolution readout," presented at *1995 IEEE Workshop on CCD's and Advanced Image Sensors*, Dana Point, CA, Apr 20–22, 1995.
[76] K. Aizawa, H. Ohno, Y. Egi, T. Hamamoto, M. Hatori, and J. Yamazaki, "On sensor video compression," presented at *1995 IEEE Workshop on CCD's and Advanced Image Sensors*, Dana Point, CA, Apr. 20–22, 1995.
[77] O. Yadid-Pecht and E. R. Fossum, "Readout schemes to increase dynamic range of image sensors," *NASA Tech. Briefs*, vol. 21, no. 1, pp. 32–33, Jan. 1997.
[78] V. Brajovic and T. Kanade, "New massively parallel technique for global operations in embedded imagers," presented at *1995 IEEE*

Workshop on CCD's and Advanced Image Sensors, Dana Point, CA, Apr. 20–22, 1995.
[79] J. Kramer, P. Sietz, and H. Baltes, "Industrial CMOS technology for the integration of optical metrology systems (photo-ASIC's)," *Sens. Actuators*, vol. A34, pp. 21–30, 1992.
[80] R. Miyagawa and T. Kanade, "Integration-time based computational sensors," presented at *1995 IEEE Workshop on CCD's and Advanced Image Sensors*, Dana Point, CA, Apr. 20–22, 1995.
[81] A. Dickinson, S. Mendis, D. Inglis, K. Azadet, and E. R. Fossum, "CMOS digital camera with parallel analog-to-digital conversion architecture," presented at *1995 IEEE Workshop on CCD's and Advanced Image Sensors*, Dana Point, CA, Apr. 20–22, 1995.
[82] U. Ringh, C. Jansson, and K. Liddiard, "Readout concept employing novel on-chip 16 bit ADC for smart IR focal plane arrays," *Infrared Readout Electronics III, Proc. SPIE*, vol. 2745, pp. 99–109, 1996.
[83] M. Dahlin *et al*., "Development of high-speed IR sensor chip technologies," *Infrared Readout Electronics III, Proc. SPIE*, vol. 2745, pp. 22–39, 1996.
[84] Z. Zhou, B. Pain, R. Panicacci, B. Mansoorian, J. Nakamura, and E. R. Fossum, "On-focal-plane ADC: recent progress at JPL," *Infrared Readout Electronics III, Proc. SPIE*, vol. 2745, pp. 111–122, 1996.
[85] B. Pain and E. R. Fossum, "Approaches and analysis for on-focal-plane analog-to-digital conversion," *Infrared Readout Electronics II, Proc. of SPIE*, vol. 2226, pp. 208–218, 1994.
[86] G. Torelli, L. Gonzo, M. Gottardi, F. Maloberti, A. Sartori, and A. Simoni, "Analog to digital conversion architectures for intelligent optical sensor arrays," *Advanced Focal Plane Arrays and Electronic Cameras, Proc. SPIE*, vol. 2950, pp. 254–264, 1996.
[87] W. Mandl, J. Kennedy, and M. Chu, "MOSAD IR focal plane per pixel A/D development," *Infrared Readout Electronics III, Proc. SPIE*, vol. 2745, pp. 90–98, 1996.
[88] B. Fowler, A. Gamal, and D. Yang, "A CMOS area image sensor with pixel-level A/D conversion," *ISSCC Dig. Tech. Papers*, 1994, pp. 226–227.
[89] B. Pain and E. R. Fossum, "Design and operation of self-biased high-gain amplifier arrays for photon-counting sensors," *Infrared Readout Electronics III, Proc. SPIE*, vol. 2745, pp. 69–77, 1996.
[90] E. R. Fossum and P. Wong, "Future prospects for CMOS active pixel sensors," presented at *1995 IEEE Workshop on CCD's and Advanced Image Sensors*, Dana Point, CA, Apr. 20–22, 1995.
[91] P. Wong, "Technology and scaling considerations for CMOS imagers," *IEEE Trans. Electron Devices*, vol. 43, pp. 2131–2142, Dec. 1996.



Eric R. Fossum (S'80–M'84–SM'91) received the B.S. degree in physics and engineering from Trinity College, Hartford, CT, in 1979, and the Ph.D. degree in electrical engineering from Yale University, New Haven, CT, in 1984.

From 1984 to 1990, he was a member of the Electrical Engineering Faculty at Columbia University, NY, where he and his students performed research on CCD focal-plane image processing and high-speed III–V CCD's. In 1990, he joined the Jet Propulsion Laboratory (JPL), California Institute of Technology, Pasadena, CA, where he managed image sensor and focal-plane technology research and advanced development. He led the development of CMOS active pixel sensors and subsequent transfer of the technology to U.S. industry. Since 1996, he has been a Chief Scientist at Photobit, La Crescenta, CA, a company he helped found in 1995. He also serves as Adjunct Professor of Electrical Engineering at the University of California, Los Angeles. He has published over 180 technical papers.

Dr. Fossum has received several awards including the Yale Becton Prize in 1984, the IBM Faculty Development Award in 1984, the National Science Foundation Presidential Young Investigator Award in 1986, the JPL Lew Allen Award for Excellence in 1992; and the NASA Exceptional Achievement Medal in 1996. He founded the biannual IEEE Workshops on CCD's and Advanced Image Sensors and the SPIE Conferences on Infrared Readout Electronics.

Samsung Exhibit 1052, Page 10 of 10