UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR LLC,

Petitioner,

v.

W&WSENS DEVICES INC.,

Patent Owner.

Case PGR2025-00082
Patent No. 12,243,948

PETITION FOR POST-GRANT REVIEW

TABLE OF CONTENTS

I. Preliminary Statement 1
II. State of the Art 2
A. Photodetectors 2
B. Microstructure-Enhanced Photodetectors 3
III. The '948 Patent 4
A. Specification 4
B. Prosecution History 6
C. Claim Construction 6
IV. Statement of Precise Relief Requested 7
A. Prior Art 7
B. Challenges 8
V. Level of Ordinary Skill in the Art 8
VI. The Challenged Claims Are Unpatentable 8
A. Ground 1: Claims 1-3 and 7-12 Are Obvious over *Kuboi* 8
1. Overview of *Kuboi* 8
2. *Kuboi* Is Analogous Art to the '948 Patent 14
3. Independent Claim 1 14
a. [1(pre)] "An integrated structure comprising:" 14
b. [1a(1)] "an array of pillars comprising Si, Ge, and/or SiGe alloy semiconductor material," 15
c. [1a(2)] "wherein at least some of the pillars are configured to include photodetectors and have

respective light-receiving surfaces and respective sides;” 18

d. [1b] “wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;” 22

e. [1c] “one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other shapes at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;” 26

f. [1d] “wherein at least some of the holes are elongated along the respective light-receiving surfaces;” 32

g. [1e] “side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;” 33

h. [1f] “a solid dielectric material forming a base dielectric region for the array;” 34

i. [1g] “electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;” 37

j. [1h] “wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes.” 40

4. Claim 2 52

a. "The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices."....52

5. Claim 3....54

a. "The integrated structure of claim 1, wherein each of at least some of the pillars has a plurality of the elongated holes."....54

6. Claim 7....55

a. "The integrated structure of claim 1, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors."....55

7. Claim 8....59

a. "The integrated structure of claim 1, in which two or more of the photodetectors share one of the electrical contacts."....59

8. Claim 9....62

a. "The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission."....62

9. Claim 10....63

a. "The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors."....63

10. Claim 11....64

a. "The integrated structure of claim 1, in which each of at least some of the photodetectors is configured

such that the light passes through at least a part **of the one of** the P-doped region and N-doped region of the photodetector before reaching any part of the other doped region of the photodetector.” 64

11. Claim 12 67

a. “The integrated structure of claim 1, in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the P-doped region before reaching any part of the N-doped region.” 67

B. Ground 2: Claims 4-6 and 13-16 Are Obvious Over *Kuboi* in View of *Vasylyev* 69

1. Overview of *Vasylyev* 69

2. *Kuboi* and *Vasylyev* Are Analogous Art to the ’948 Patent 77

3. Motivation to Apply *Vasylyev*’s Teaching of a Single Light Input Port in Pairwise Optical Relationship with a Microlens to *Kuboi*’s Blue Pixel 53B 77

4. Motivation to Apply *Vasylyev*’s Teaching of a Light Input Port Extending Along a “Substantial Portion” of the Light-Receiving Surface to *Kuboi*’s Green and Red Pixels (53G, 53R) 90

5. Motivation to Additionally Incorporate a Single Light Input Port in the Blue Pixel 53B of the *Kuboi-Vasylyev-2* Imaging Device Based on *Vasylyev*’s Teaching 100

6. Claim 4 105

a. “The integrated structure of claim 1, wherein each of at least some of the pillars has only one of the elongated holes.” 105

7. Claim 5 109

a. "The integrated structure of claim 1, in which the light-receiving surfaces have respective widths, and the elongated holes extend along less than the widths of the light-receiving surfaces of at least some of the pillars in which the holes are fabricated."....109

8. Claim 6....111

a. "The integrated structure of claim 5 in which each of at least some of the elongated holes has at least one closed contour remote from respective side edges of the light-receiving surface in which the hole is fabricated."....111

9. Independent Claim 13....112

a. [13(pre)] "An integrated structure comprising:"....112

b. [13a(1)] "an array of pillars comprising Si, Ge, and/or alloyed SiGe semiconductor material,"....113

c. [13a(2)] "wherein at least some of the pillars have respective sides and respective light-receiving surfaces with selected widths and comprise at least one photodetector;"....113

d. [13b] "wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;"....114

e. [13c] "one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars,"....114

f. [13d(1)] wherein each of the holes (i) has an elongated shape extending in length over less than the width of the light-receiving surface in which the hole is fabricated, (ii) has at least one closed

contour at the light-receiving surface in which the hole is fabricated,” 114

g. [13d(2)] “([iii]) extends into the pillar in which the hole is fabricated to a depth of 100 to 10000 nm, and (iv) is filled at least partly with solid dielectric material;” 117

h. [13e] “side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;” 118

i. [13f] “a solid dielectric material forming a base dielectric region for the array;” 118

j. [13g] “electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;” 118

k. [13h] “wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the holes; and” 118

l. [13i] “wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission.” 119

10. Claim 14 119

a. “The integrated structure of claim 13, in which each of at least some of the pillars has only one of the elongated holes fabricated therein.” 119

11. Claim 15 121

a. “The integrated structure of claim 13, in which each of at least some of the pillars has at least two of the elongated holes.” 121

12. Claim 16 122

a. "The integrated structure of claim 13, in which each of at least some of the photodetectors includes at least one of the holes." 122

C. Ground 3: Claims 1-3 and 7-12 Are Obvious Over *Kuboi* in View of *Shinohara* 123

1. Overview of *Shinohara* 123

2. *Kuboi* and *Shinohara* Are Analogous to the '948 Patent 125

3. Motivation to Apply *Shinohara*'s Monolithic Integration Teachings in in *Kuboi* 125

4. Independent Claim 1 128

a. [1(pre)]-[1e], [1g]-[1h] 128

b. [1f] 128

5. Claim 2 132

6. Claims 3 and 7-8 132

7. Claim 9 133

8. Claim 10 133

9. Claims 11-12 134

D. Ground 4: Claims 4-6 and 13-16 Are Obvious Over *Kuboi* in View of *Vasylyev* and *Shinohara* 134

1. Motivation to modify *Kuboi* in view of *Vasylyev* and *Shinohara* 134

2. Claims 4-6 137

3. Claim 13 137

a. [13(pre)]-[13e], [13g]-[13h] 137

b. [13f] 138

c. [13i]....138

4. Claims 14-16 138

E. Ground 5: Claims 1-16 Lack Enablement Under §112....138

1. The Claims Are Not Enabled If the Prior Art's Disclosure Is Deemed Insufficient 139

2. Because the Claims Cover Single-Hole Structures, the Full Scope of Claims 1, 4, 13, and 14 Is Not Enabled....140

3. Because the Claims Cover Millimeter-Sized Pillars, the Full Scope of Claims 1 and 13 Is Not Enabled....141

VII. Mandatory Notices....143

A. Real Parties-in-Interest 143

B. Related Matters....143

C. Lead and Backup Counsel, and Service Information....143

VIII. Grounds for Standing....145

IX. Timing....145

X. Conclusion 145

PETITIONER'S EXHIBIT LIST

Exhibit	Description
Ex-1001	U.S. Patent No. 12,243,948 B2 to Wang et al. ("'948 Patent").
Ex-1002	Declaration of Dr. Michael Lebby
Ex-1003	Prosecution History of the '948 Patent (downloaded from Public PAIR).
Ex-1004	U.S. Patent Application Publication No. 2012/0049044 A1 to Kuboi ("*Kuboi*").
Ex-1005	U.S. Patent Application Publication No. 2012/0012741 A1 to Vasylyev ("*Vasylyev*").
Ex-1006	U.S. Patent Application Publication No. 2012/0033119 A1 to Shinohara ("*Shinohara*").
Ex-1007	European Patent Application EP 2 172 974 A1 to NXP B.V. ("*NXP*").
Ex-1008	Zhihong Huang et al., *Microstructured silicon photodetector*, Applied Physics Letters, Vol. 89 (2006), pp. 033506-1 to -3.
Ex-1009	Richard A. Myers et al., *Enhancing near-infrared avalanche photodiode performance by femtosecond laser microstructuring*, Applied Optics, Vol. 45, No. 35 (Dec. 2006), pp. 8825-31.
Ex-1010	Abbas El Gamal et al., *CMOS Image Sensors*, IEEE Circuits & Devices Magazine (May/June 2005), pp. 6-20.
Ex-1011	*Electrical Engineering Dictionary* – CRC*netBase 2000* (Phillip A. Laplante editor-in-chief, CRC Press LLC 2000), pp. 1-11.
Ex-1012	S.M. Sze et al., *Semiconductor Devices - Physics and Technology* (John Wiley & Sons, Inc. 3d ed. 2012), pp. 6-9, 205-10, 325-30, 392-406, 416-17, 466-67.
Ex-1013	John P. Uyemura, *CMOS Logic Circuit Design* (Kluwer Academic Publishers 2002), pp. 64, 74-102, 315-17, 458-60.
Ex-1014	Khalil Jumah Tawfiq Hamam, Organic Solar Cells Based on High Dielectric Constant Materials: An Approach to Increase Efficiency (June 2013) (Ph.D. dissertation, Western Michigan University), pp. 1-122.

Exhibit	Description
Ex-1015	P. Kalugasalam et al., *Dielectric and AC Conduction Studies of Lead Phthalocyanine Thin Film*, Chalcogenide Letters, Vol. 6, No. 9 (Sept. 2009), pp. 469-76.
Ex-1016	Matthew Sauceda, *Porphyrin Thin Film Dielectrics*, SUNFEST Technical Report TR-CST01NOV04, Center for Sensor Technologies, Univ. of Pennsylvania, Philadelphia, PA (2004), pp. 181-98.
Ex-1017	N. Venkatramaiah et al., *Spectroscopic and dielectric studies of meso-tetrakis(p-sulfonatophenyl) porphyrin doped hybrid borate glasses*, Journal of Alloys and Compounds, Vol. 509 (2011), pp. 2797-803.
Ex-1018	Tom J. Savenije, *Photogeneration and transport of charge carriers in a porphyrin p/n heterojunction*, Physical Review B, Vol. 55, No. 15 (Apr. 1997), pp. 9685-92.
Ex-1019	Ümit Salan et al., *Synthesis, characterization, electrical and dielectric permittivity measurements of 2,9,16,23-tetra(4-ferrocenylimino-3-nitrophenoxy)phthalocyanines*, Journal of Porphyrins and Phthalocyanines, Vol. 10 (2006), pp. 1263-70.
Ex-1020	Teresa M. Figueira-Duarte et al., *Pyrene-Based Materials for Organic Electronics*, Chemical Reviews, Vol. 111 (2011), pp. 7260-314.
Ex-1021	Jurgen Michel et al., *Advances in fully CMOS integrated photonic devices*, Proceedings of SPIE, Vol. 6477 (2007), pp. 64770P-1 to -11.
Ex-1022	Mark Beals et al., *Process Flow Innovations for Photonic Device Integration in CMOS*, Proceedings of SPIE, Vol. 6898 (2008), pp. 689804-1 to -14.
Ex-1023	Donald A. Neaman, *Semiconductor Physics and Devices – Basic Principles* (McGraw Hill 3d ed. 2003), pp. 247-50, 260-61.
Ex-1024	Laurent Frey et al., *Color filters including infrared cut-off integrated on CMOS image sensor*, Optics Express, Vol. 19, No. 14 (2011), pp. 13073-80.
Ex-1025	U.S. Patent Application Publication No. 2012/0153124 A1 to Yu et al.

Exhibit	Description
Ex-1026	U.S. Patent No. 8,390,036 B2 to Goto.
Ex-1027	U.S. Patent Application Publication No. 2008/0157141 A1 to Han.
Ex-1028	Horst Zimmermann, *Integrated Silicon Optoelectronics* (Springer. 2d ed. 2010), pp. 1-7.
Ex-1029	Ran Aharoni et al., *Basic model of absorption depth and injection levels in silicon under intermediate illumination levels*, Optics Communications, Vol. 291 (2013), pp. 1-6.
Ex-1030	M.M. El-Nahass et al., *Structural and optical properties of Ni (II) tetraphenyl porphyrin thin films*, Eur. Phys. J. Appl. Phys., Vol. 57 (2012), pp. 30201-p1 to -p13.
Ex-1031	Martin A. Green, *Self-consistent optical parameters of intrinsic silicon at 300K including temperature coefficients*, Solar Energy Materials & Solar Cells, Vol. 92, (2008), pp. 1305-10.
Ex-1032	P.A. Lane et al., *Electroabsorption studies of phthalocyanine/perylene solar cells*, Solar Energy Materials & Solar Cells, Vol. 63 (2000), pp. 3-13.
Ex-1033	Connie J. Chang-Hasnain et al., *High-contrast gratings for integrated optoelectronics*, Advances in Optics and Photonics, Vol. 4 (2012), pp. 379-440.
Ex-1034	H.H. Li, *Refractive Index of Silicon and Germanium and Its Wavelength and Temperature Derivatives*, J. Phys. Chem. Ref. Data, Vol. 9, No. 3 (1980), pp. 561-658.
Ex-1035	U.S. Patent No. 8,378,339 B2 to Nomura et al.
Ex-1036	M.M. El-Nahass et al., *Structural and optical properties of thermally evaporated zinc phthalocyanine thin films*, Proc. 2nd Saudi Sci. Conf. (Mar. 2004), pp. 277-93.
Ex-1037	M.E. Azim-Araghi et al., *Electrical and optical properties of an organic semiconductor metal-free phthalocyanine ($C_{32}H_{18}N_8$)*, Eur. Phys. J. Appl. Phys., Vol. 58 (2012), pp. 30201-p1 to -p6.
Ex-1038	International Patent Publication No. WO 2011/085297 A1 to Han et al. ("*Han*").

Exhibit	Description
Ex-1039	J.S. Arney et al., *Color Properties of Specular Reflections*, IS&T's NIP20: 2004 International Conference on Digital Printing Technologies, pp. 445-49.
Ex-1040	Andrew Blakers et al., *Thin Single Crystalline Elongate Silicon Solar Cells*, Energy Procedia, Vol. 15 (2012), pp. 58-66.
Ex-1041	A. El Amrani et al., *Solar Module Fabrication*, International Journal of Photoenergy, Article ID 27610 (2007), pp. 1-5.
Ex-1042	Ji-Tao Liu et al., *Curing Determination of EVA for Solar Panel Application by DSC*, Application Note, PerkinElmer (2010), pp. 1-3.
Ex-1043	Chen ShuoFu et al., *A comprehensive consideration of bias voltage and temperature to extract the intrinsic frequency response of photodiodes*, Chinese Science Bulletin, Vol. 55, No. 32 (2010), pp. 3727-33.
Ex-1044	Richard S. Quimby, *Photonics and Lasers - An Introduction* (John Wiley & Sons, Inc. 2006), pp. 249-79.
Ex-1045	U.S. Patent No. 8,013,238 B2 to Hockaday.
Ex-1046	A. Vandenbroucke et al., *Influence of temperature and bias voltage on the performance of a high resolution PET detector built with position sensitive avalanche photodiodes*, IOP Publishing for Sissa Medialab (2012), pp. 1-30.
Ex-1047	U.S. Patent No. 8,274,122 B2 to Shimotsusa.
Ex-1048	Renato Turchetta et al., *Introduction to CMOS Image Sensors*, Molecular Expressions™ Optical Microscopy Primer: Digital Imaging in Optical Microscopy (July 16, 2004), pp. 1-9, *available at* https://web.archive.org/web/20120508153832/https://micro.magnet.fsu.edu/primer/digitalimaging/cmosimagesensors.html
Ex-1049	U.S. Patent Application Publication No. 2025/0194293 A1 to Wang et al. ("'948 Divisional").
Ex-1050	Prosecution History of the '948 Divisional (downloaded from Public PAIR).

Exhibit	Description
Ex-1051	Christopher Chase et al., *Size effect of high contrast gratings in VCSELs*, Optics Express, Vol. 17, No. 26 (Dec. 2009), pp. 24002-07.
Ex-1052	Eric R. Fossum, *CMOS Image Sensors: Electronic Camera-On-A-Chip*, IEEE Transactions on Electron Devices, Vol. 44, No. 10 (Oct. 1997), pp. 1689-98.
Ex-1053	U.S. Patent Application Publication No. 2008/0259981 A1 to Wang et al.
Ex-1054	Sunetra Mendis et al., *CMOS Active Pixel Image Sensor*, IEEE Transactions on Electron Devices, Vol. 41, No. 3 (Mar. 1994), pp. 452-53.
Ex-1055	U.S. Patent Application Publication No. 2008/0055432 A1 to Koseki.
Ex-1056	Certified English translation of Japanese Published Unexamined Patent Application No. P2007-129024A to Hasegawa ("*Hasegawa*")

I. Preliminary Statement

Petitioner Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor LLC (collectively, "Samsung") requests post-grant review of U.S. Patent No. 12,243,948 ("'948 Patent") (Ex-1001) and cancellation of claims 1-16.

The challenged claims concern photodetectors that employ microstructures to enhance light absorption. Specifically, the claims recite photodiodes with elongated holes—ranging from 100 to 10,000 nanometers in depth—that increase light absorption by at least 10% compared to photodetectors lacking such features. However, photodetectors incorporating such holes to enhance light absorption were well known prior to the alleged invention date. For instance, *Kuboi* (Ex-1004)—which was not considered during prosecution—discloses photodetectors with similar features. Furthermore, the holes in *Kuboi*'s photodetectors enhance light absorption by well over 10% compared to photodetectors that lack such features. Additional details not expressly disclosed in *Kuboi* are disclosed in *Vasylyev* (Ex-1005) and *Shinohara* (Ex-1006), which disclose similar optoelectronic devices.

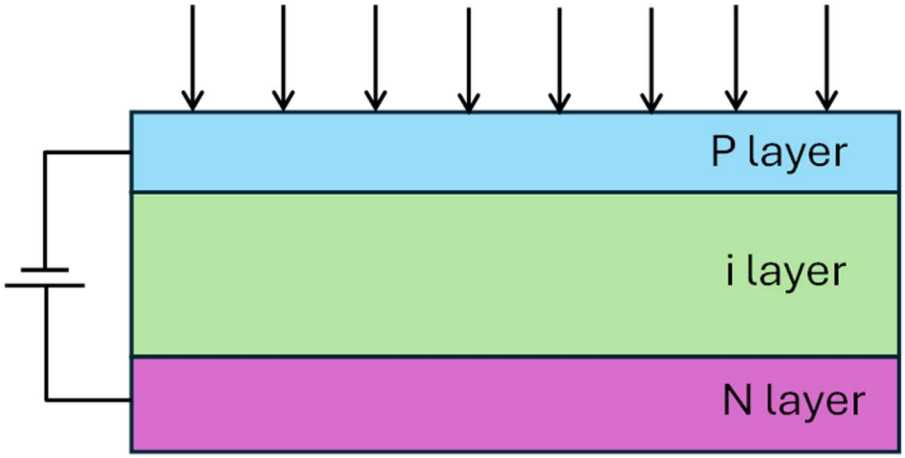
As detailed below and in the supporting declaration of Dr. Michael Lebby ("Lebby") (Ex-1002), Lebby, ¶¶1-368, the challenged claims are unpatentable for

multiple reasons. Lebby, ¶¶107-366. The Board should institute review and cancel all challenged claims.

II. State of the Art

A. Photodetectors

A photodetector is a semiconductor device that transforms photons into electrical signals, enabling electrical circuits to detect and measure incident light. Lebby, ¶53. As illustrated below, a PiN photodetector is a specific type of photodiode characterized by a "very lightly doped" or undoped intrinsic layer positioned between highly doped P-type and N-type semiconductor layers (hence the name "PiN"):



Lebby, ¶53; Ex-1044, 20-21. When light enters the photodetector, photons are absorbed in the intrinsic layer, generating electron-hole pairs. Applying a negative bias across the photodetector causes the separated electrons to move toward the N-

type layer and the holes toward the P-type layer, producing a measurable photocurrent. Lebby, ¶54.

B. Microstructure-Enhanced Photodetectors

Conventional silicon photodetectors exhibit high responsivity at wavelengths of less than 850 nm. Ex-1008, 1; Lebby, ¶55. The prior art recognized that tailoring the microstructure of silicon can extend the operability of these photodetectors to longer wavelengths, such as infrared. Lebby, ¶55. For instance, etching the surface of a silicon photodetector to create micron-sized pillars/grooves was known to enhance a photodetector's responsiveness at longer wavelengths. Ex-1008, 1-2; Ex-1009, 1-6; Lebby, ¶55.

Photodetectors featuring microstructures enhanced by etched holes were widely known and utilized well before the purported invention. Lebby, ¶56. For example, *NXP* (Ex-1007) discloses a single-chip device 1300 where a silicon PiN photodiode is integrated with CMOS signal processing circuitry (not shown below) on the same substrate 102. *NXP*, ¶¶[15], [32], [42], [85].

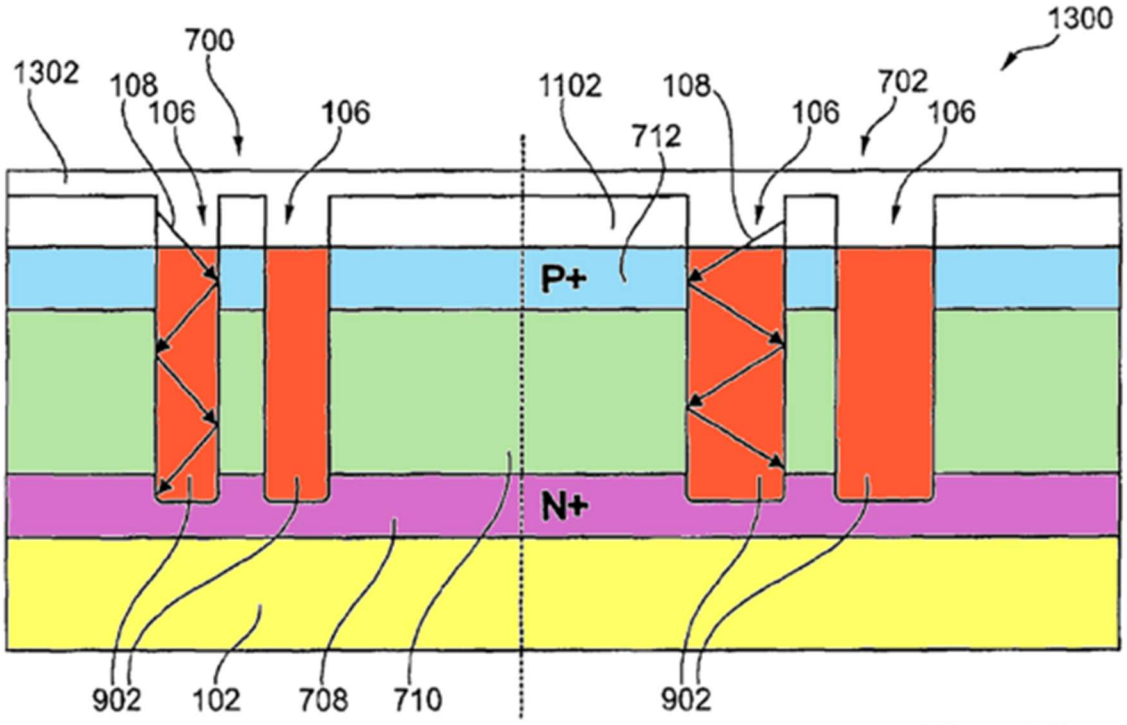


Fig. 13

NXP, Fig. 13.[1] The PiN photodiode above includes an intrinsic layer 710 disposed between an N^+ layer 708 and a P^+ layer 712 and pores 106 formed on the PiN layers by etching. *NXP*, ¶¶[77]-[78]. *NXP* discloses that the presence of pores 106 increases the quantum efficiency of the photodiode. *NXP*, ¶¶[13], [38]; Lebby, ¶57.

III. The '948 Patent

A. Specification

The '948 Patent's photodetector includes microstructures to enhance photoabsorption. '948 Patent, 2:41-42, 3:1-5, 4:1-8, 17:25-31. The photodetector

[1] All color and colored annotations in figures have been added.

includes a silicon substrate with a first layer (P^+ layer), a very low-doped N or P layer called the intermediate layer (i layer), and a second layer (N^+ layer) with holes etched in one or more of the PiN layers. *Id.*, 15:57-59, 16:9-36, 17:47-52. The photodetector (illustrated below) operates in reverse bias mode with negative voltage on the anode (P^+ layer) and positive voltage on the cathode (N^+ layer). *Id.*, 16:40-44, 11:45-51; Lebby, ¶68.

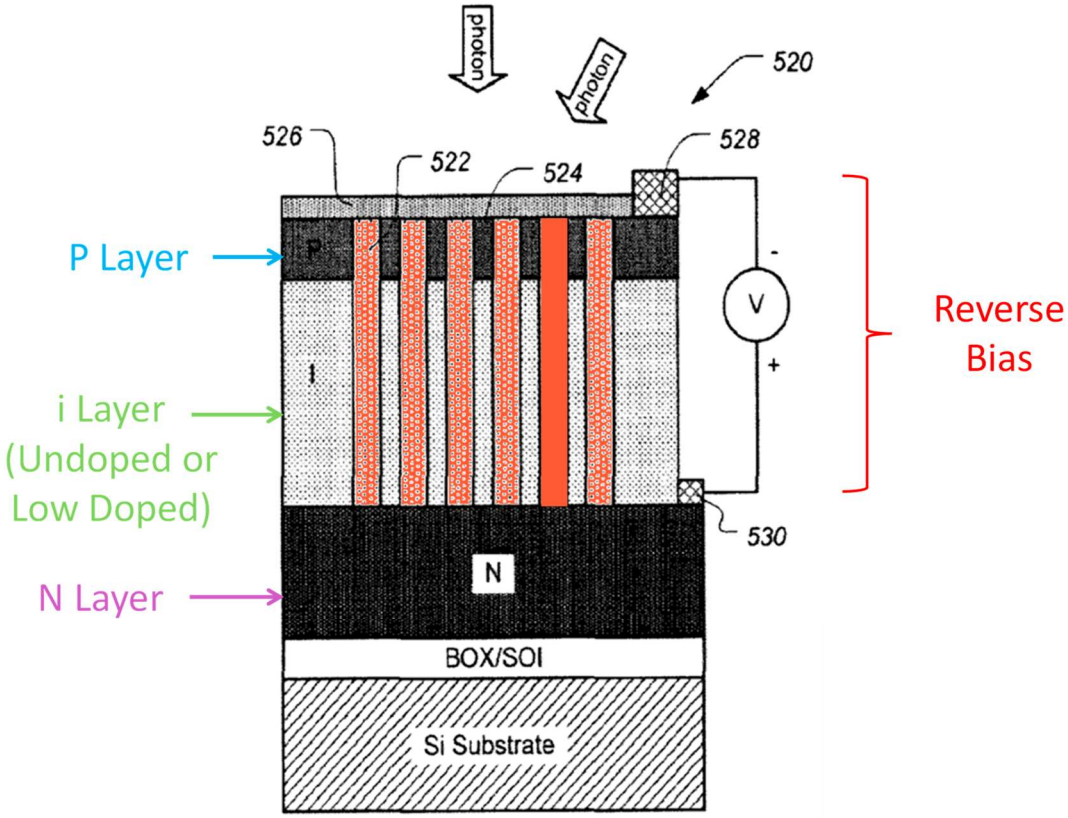


FIG. 5B

'948 Patent, Fig. 5B.

The ’948 Patent discloses that the microstructures increase the effective absorption coefficient of silicon, resulting in increased light absorption. *Id*., 8:18-54; Lebby, ¶69.

B. Prosecution History

During prosecution, independent claim 1 and several dependent claims were rejected as obvious over multiple references. *See* Ex-1003, 348-351, 302-312. In response, Patent Owner amended independent claim 1 to further recite that “at least some of the holes are elongated along the respective light-receiving surfaces.” Ex-1003, 249. Following this amendment, the claims were allowed. Ex-1003, 17-23.

As detailed below, *Kuboi*—which was not considered during prosecution—discloses this limitation. Lebby, ¶¶70-71. Its teachings, when evaluated from a POSITA’s perspective, demonstrate that the allowed claims are obvious in light of *Kuboi*’s disclosure. *Id*.

C. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.200(b). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan*

Broad Ocean Motor Co., 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy.[2]

IV. Statement of Precise Relief Requested

A. Prior Art

The application that resulted in the '948 Patent was filed on September 3, 2024, claiming priority to multiple patent applications, the earliest of which was filed on May 22, 2013.[3] Thus, the earliest claimed priority date is May 22, 2013.

- *Kuboi* (Ex-1004), U.S. Patent Application Publication No. 2012/0049044A1, which published on March 1, 2012, is prior art under 35 U.S.C. §102(a)(1) and (a)(2).
- *Vasylyev* (Ex-1005), U.S. Patent Application Publication No. 2012/0012741A1, which published on January 19, 2012, is prior art under 35 U.S.C. §102(a)(1) and (a)(2).
- *Shinohara* (Ex-1006), U.S. Patent Application Publication No. 2012/0033119A1, which published on February 9, 2012, is prior art under 35 U.S.C. §102(a)(1) and (a)(2).

[2] Petitioner retains the right to contend in another proceeding that certain limitations are indefinite.

[3] Petitioner retains the right to dispute the claimed priority in another proceeding.

B. Challenges

Ground	Challenged Claims	Basis	Prior Art/Further Detail
1	1-3 and 7-12	§103	*Kuboi*
2	4-6 and 13-16	§103	*Kuboi* and *Vasylyev*
3	1-3 and 7-12	§103	*Kuboi* and *Shinohara*
4	4-6 and 13-16	§103	*Kuboi*, *Vasylyev*, and *Shinohara*
5	1-16	§112	Lack of enablement

V. Level of Ordinary Skill in the Art

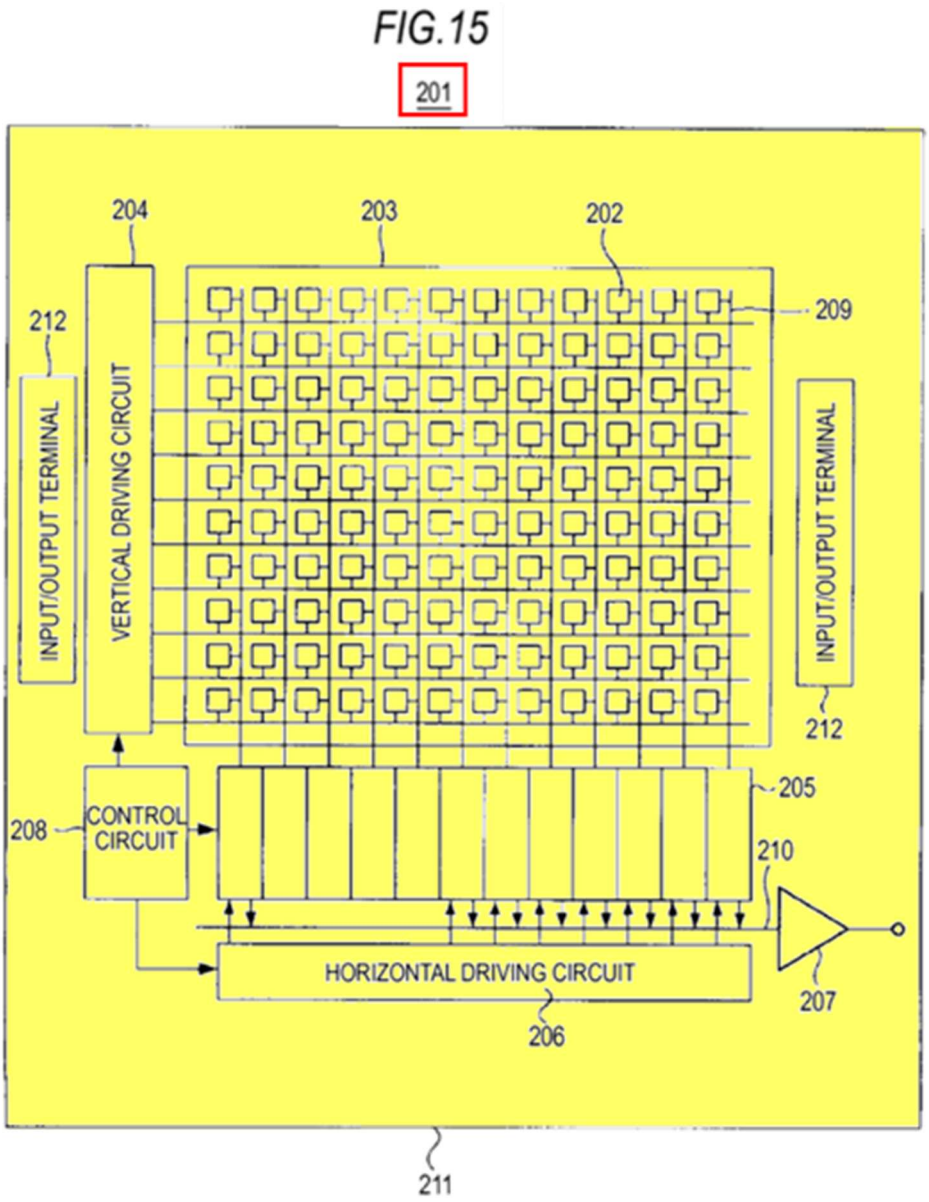
A person of ordinary skill in the art ("POSITA") would have had at least a master's degree in electrical engineering or a similar field and at least five years of experience working with semiconductor systems and semiconductor devices. Lebby, ¶107. Additional relevant work experience can compensate for less education and vice versa. *Id.*

VI. The Challenged Claims Are Unpatentable

A. Ground 1: Claims 1-3 and 7-12 Are Obvious over *Kuboi*

1. Overview of *Kuboi*

Kuboi's CMOS solid-state imaging device 201 includes a pixel region 203 and a peripheral circuit portion on a single semiconductor substrate 211. *Kuboi*, ¶[48].



Kuboi, Fig. 15. Pixel region 203 of substrate 211 comprises a plurality of pixels 202 arranged in a two-dimensional array. *Kuboi*, ¶[48]. Each pixel 202 contains one photoelectric conversion portion (or a photodiode) and four pixel transistors. *Id.* The peripheral circuit portion includes "logic[] circuits" (e.g., circuits 204-208), which process the electrical output of the pixels and then output

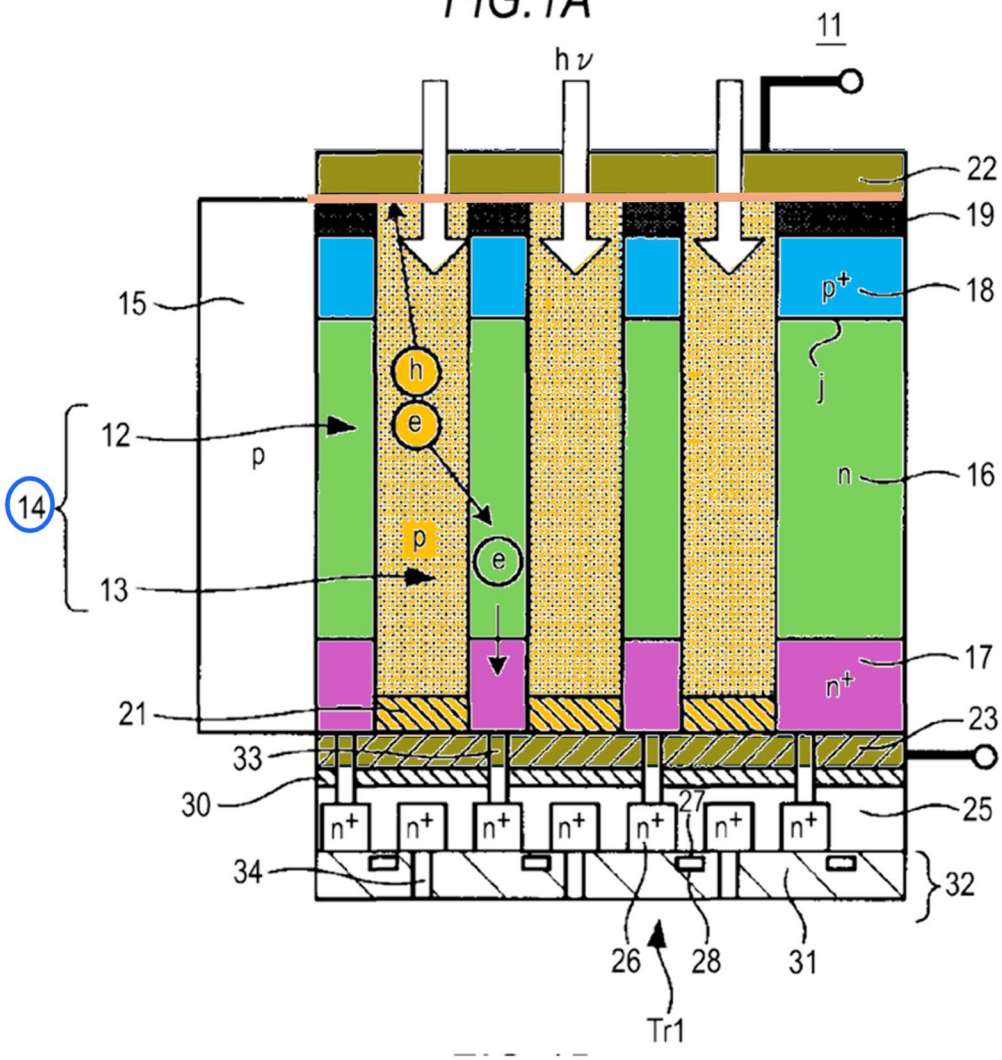
it. *Kuboi*, ¶¶[49]-[54]; Lebby, ¶¶75-78. The pixels and the peripheral circuit portion are fabricated on a single substrate, the pixel transistors are fabricated on another substrate, and the two substrates are bonded together. *Kuboi*, ¶¶[62], [70], [78]; Lebby, ¶78.

Kuboi describes photoelectric conversion portions suitable for use in imaging device 201. *Kuboi*, ¶[48]; Lebby, ¶79. For example, *Kuboi* discloses a basic pixel configuration with reference to Figures 1A-1B. *Kuboi*, ¶[55]. *Kuboi* likewise discloses a pixel configuration in Figures 6A-6B, explaining that the disclosed red and green pixels 53R and 53G have a structure that is the same as the basic configuration of Figures 1A-1B. *Kuboi*, ¶¶[90], [95], [69]. *Kuboi* also discloses that Figure 13 includes pixels 53R, 53G, and 53B, having configurations that are the same as the pixels of Figures 1A-1B. *Kuboi*, ¶[181]. *Kuboi* discloses that the CMOS imaging device of Figure 15 as applicable to all disclosed pixel configurations. *Kuboi*, ¶¶[34], [48]. Further, *Kuboi*'s Figures 4A-4F show a method of manufacturing the basic pixel configuration of Figures 1A-1B. *Kuboi*, ¶¶[69]-[76]. Thus, Figures 1A-1B, 6A-6B, and 13 all disclose the pixel configurations that can be used on the same imaging device 201 of Figure 15, and Figures 4A-4F disclose methods of manufacturing the same pixel configuration. Lebby, ¶79. Accordingly, this Petition relies on *Kuboi*'s Figures 1A-1B, 4A-4F,

6A-6B, 13, and 15, and associated disclosures as representative of the pixel configuration of the same imaging device. Lebby, ¶80.

Figure 1A illustrates a photoelectric conversion portion 14 in pixel 11. *Kuboi*, ¶¶[48], [55]-[56]. Pixel 11, including photoelectric conversion portion 14, can be utilized in imaging device 201. *Kuboi*, ¶¶[48], [55]; Lebby, ¶81.

FIG.1A



Kuboi, Fig. 1A. Photoelectric conversion portion 14 comprises a silicon semiconductor layer 12 that includes multiple embedded organic photoelectric films 13. *Kuboi*, ¶[55], [57]. Silicon semiconductor layer 12 is implanted with different impurities (or doped) to form n-type semiconductor (or "intermediate") region 16 with p^+-type semiconductor region 18 on one side and n^+-type semiconductor region 17 on the opposite side (i.e., stacked PiN regions). *Kuboi*, ¶¶[56], [71]; Lebby, ¶82.

After forming regions 18, 16, and 17, vertical holes 38 extending from p^+-type region 18 to n^+-type region 17 are etched into the PiN regions (below, right). *Kuboi*, ¶¶[71]-[72]; Lebby, ¶83.

FIG.4A

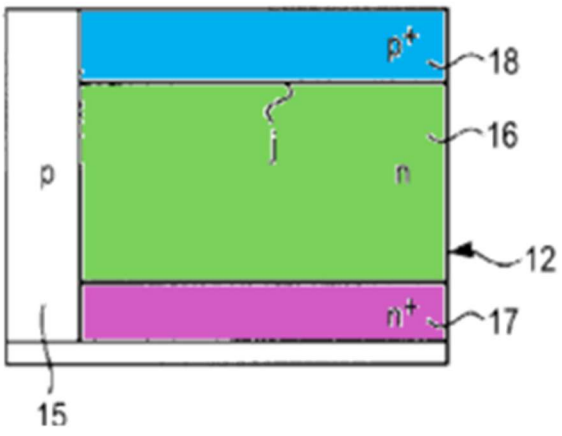
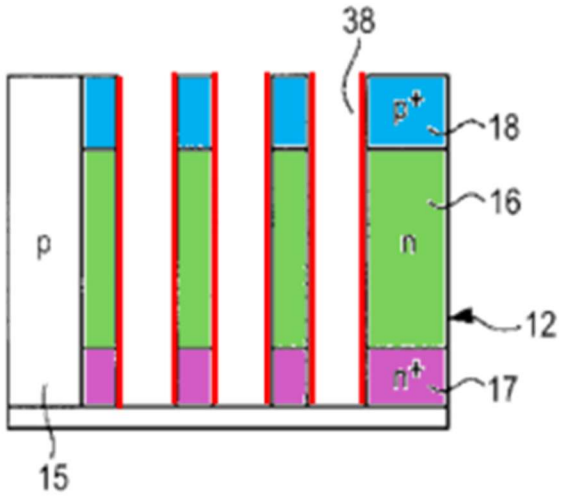


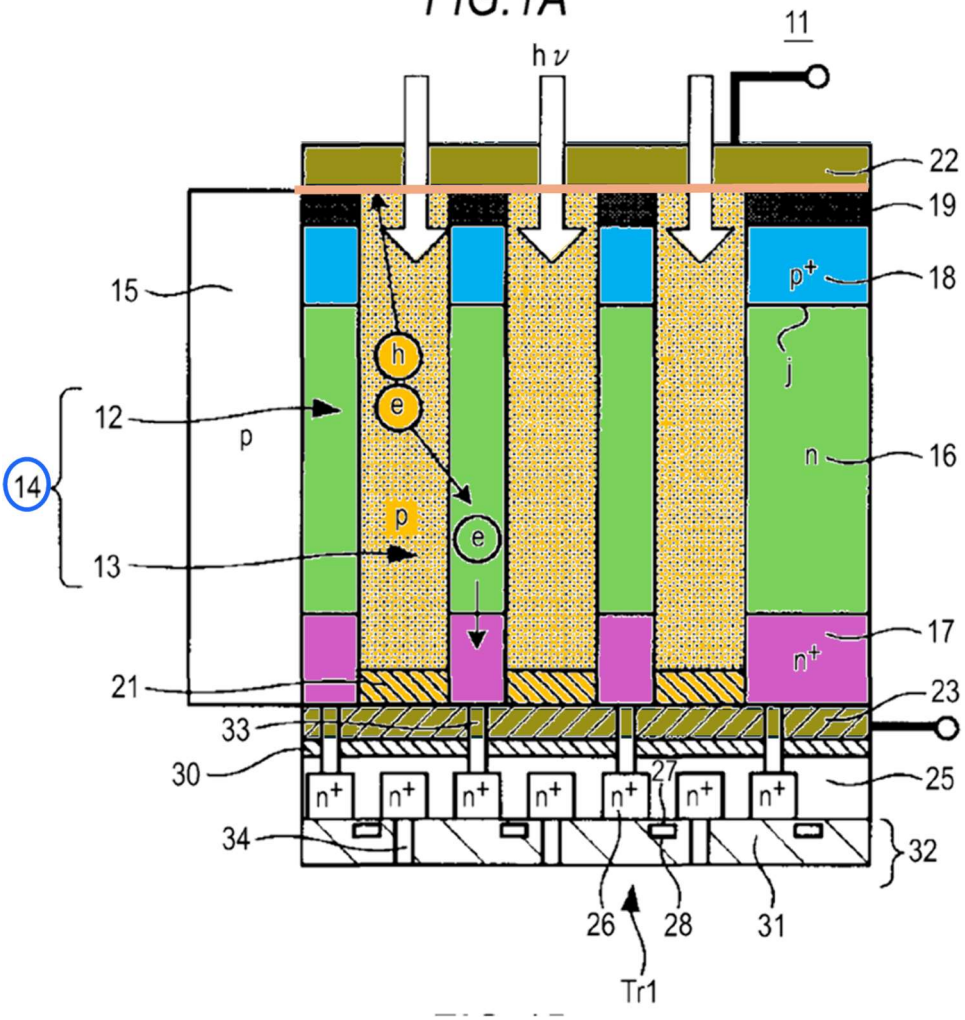
FIG.4B



Kuboi, Figs. 4A, 4B. Then, the organic material that forms photoelectric conversion film 13 is deposited in holes 38. *Kuboi*, ¶¶[72]-[73]. Lebby, ¶84.

A metal light shielding film 19 is then applied to region 18's surface such that only holes 38 containing films 13 are exposed to incident light (hν). *Kuboi*, ¶¶[59], [72]-[73], [76], Figs. 1A, 4F; Lebby, ¶85. An upper electrode 22 and a lower electrode 23 are formed on opposite sides of the PiN regions, and a reverse bias is applied. *Kuboi*, ¶¶[60], [64].

FIG.1A



Kuboi, Fig. 1A. Photoelectric conversion of the incident light (hν) within films 13 (inside holes 38) generates electron-hole pairs that pass through the depleted

semiconductor layer 12 into a charge accumulation region 26 of the transfer transistor (Tr1) of the corresponding pixel 11 (via conductors 33). *Kuboi*, ¶¶[62], [64], [73]; Lebby, ¶85. The electrical signals from pixel 11 are sent to the peripheral circuits for signal processing and output. *Kuboi*, ¶¶[48]-[49], [61]-[62].

2. *Kuboi* Is Analogous Art to the '948 Patent

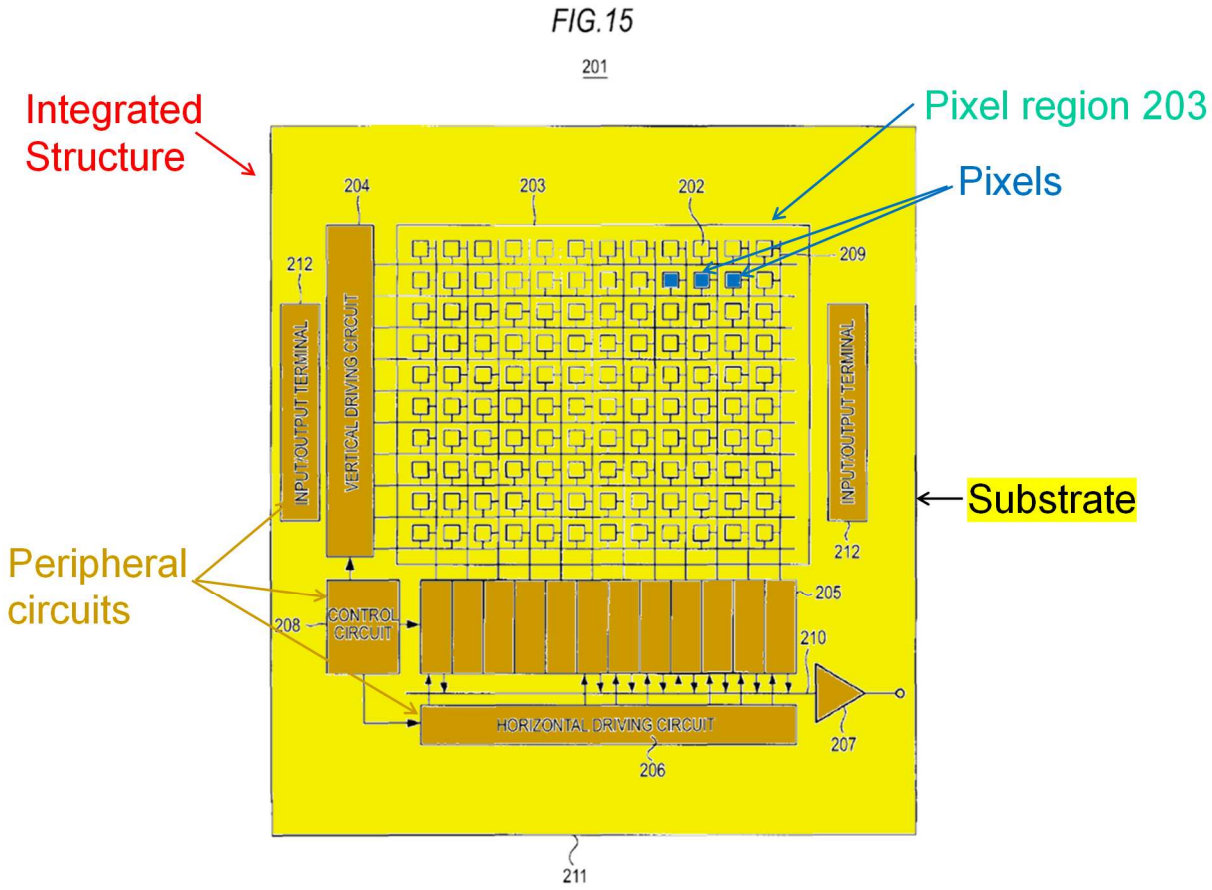
Kuboi is analogous art to the '948 Patent because, like the '948 Patent, *Kuboi* seeks to improve the light absorption efficiency of photoelectric devices. Lebby, ¶¶75-85. The '948 Patent is directed to techniques for enhancing photon absorption. '948 Patent, Abstract. Similarly, *Kuboi* is directed to a solid-state imaging device in which light absorption efficiency is increased to improve sensitivity. *Kuboi*, ¶¶[9]-[19].

3. Independent Claim 1

a. [1(pre)] "An integrated structure comprising:"

To the extent the preamble is limiting, *Kuboi* discloses it. Lebby, ¶¶110-112. *Kuboi*'s CMOS imaging device 201 includes pixel region 203 and a peripheral circuit portion on a single semiconductor substrate 211. *Kuboi*, ¶[48]. Substrate 211's pixel region 203 comprises a plurality of pixels 202, each of which contains a photoelectric conversion portion. *Id.* The pixels and peripheral circuit portion are fabricated on a single substrate. *Kuboi*, ¶¶[70], [78]. *Kuboi*'s imaging device is an "integrated structure" because it combines structures, such as pixels,

with photoelectric conversion portions and peripheral electric circuits. Lebby, ¶112. *Kuboi*'s integrated structure is shown below:

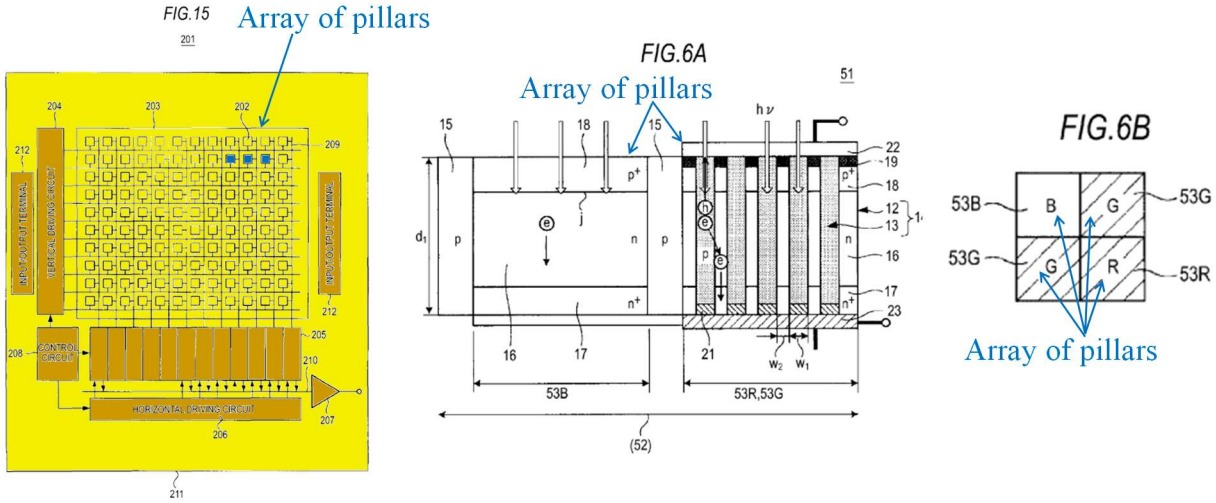


Kuboi, Fig. 15.

b. [1a(1)] "an array of pillars comprising Si, Ge, and/or SiGe alloy semiconductor material,"

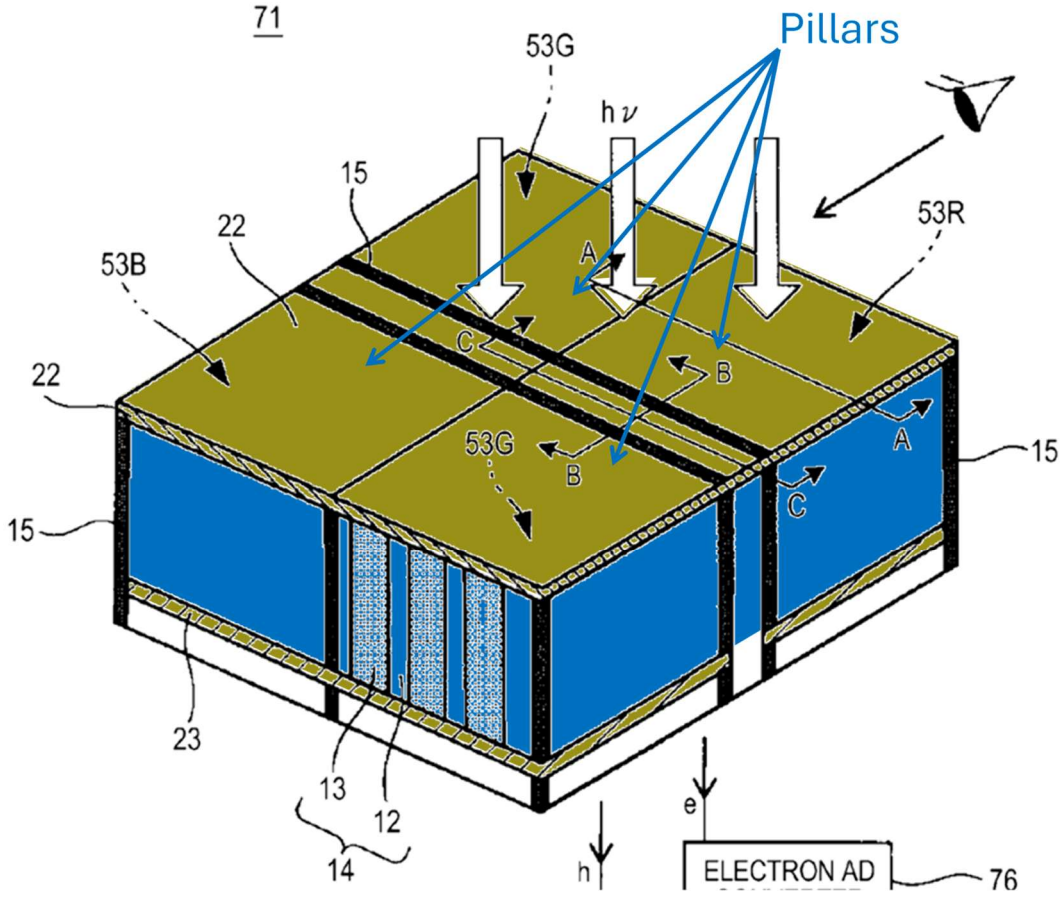
Kuboi discloses [1a(1)]. Lebby, ¶¶113-116. The pixel region of *Kuboi*'s imaging device 201 includes "a plurality of pixels 202 which include a photoelectric conversion portion and which are regularly arranged in a two-dimensional array." *Kuboi*, ¶[48]. Specifically, *Kuboi*'s imaging device includes

"red, blue, green, and green pixels … arranged in a two-dimensional array." *Kuboi*, ¶¶[90], [181].



Kuboi, Figs. 15, 6A-6B. A POSITA would have understood that each pixel in *Kuboi*'s imaging device is a pillar and the array of pixels constitutes an array of pillars. Lebby, ¶115. Figure 13 below provides a perspective view highlighting the pillar-like structure of red 53R, green 53G, and blue pixels 53B arranged in a Bayer configuration. *Kuboi*, ¶¶[180]-[181]; Ex-1048, 2 (explaining that a Bayer configuration is "a sequential pattern of red, green, and blue filters that are arranged in a mosaic pattern").

FIG.13



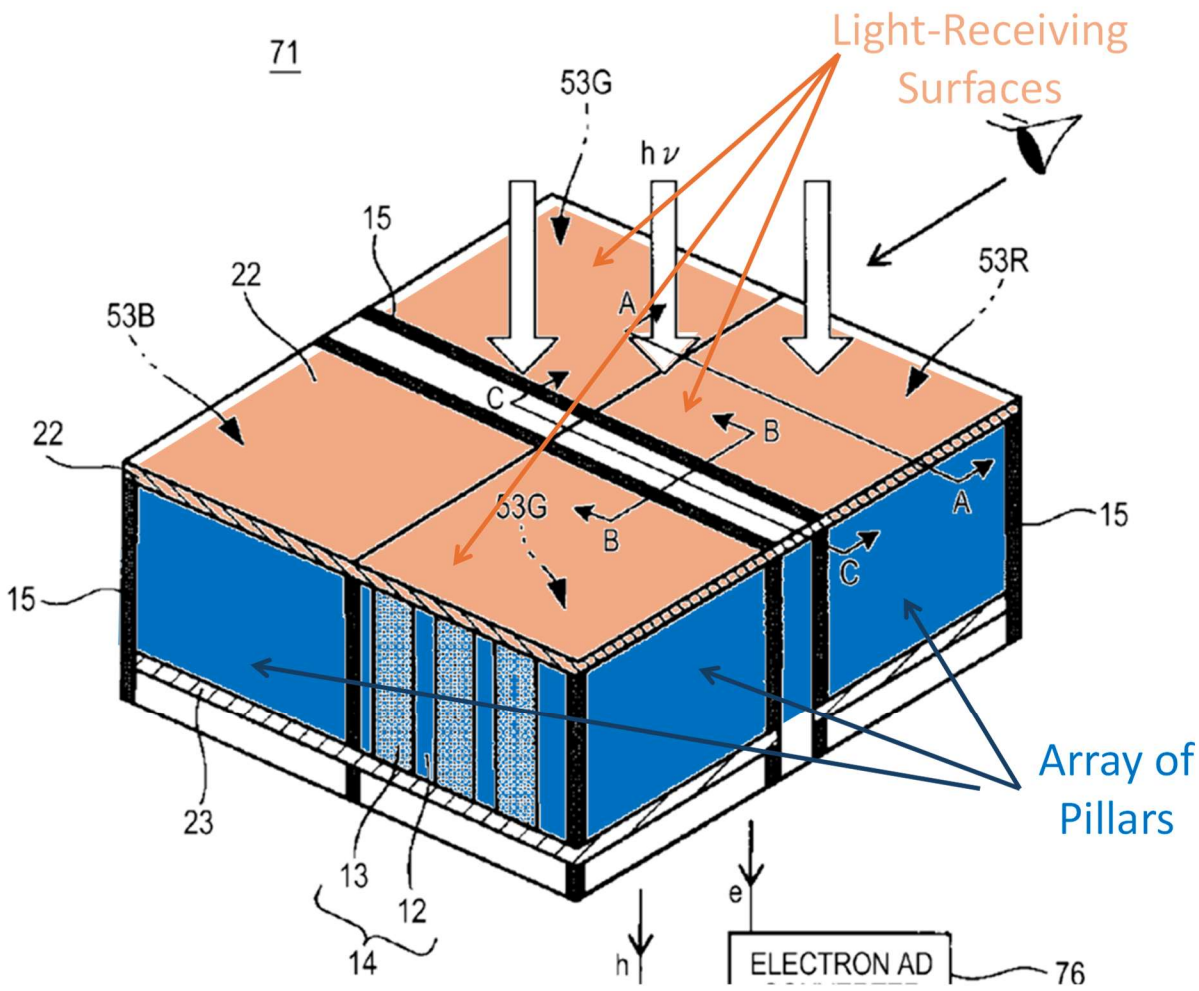
Kuboi, Fig. 13 (cropped).

Kuboi explains that "silicon semiconductor layer 12 is divided into respective pixels." *Kuboi*, ¶[91]. Because *Kuboi*'s pixels are formed in a silicon (or Si) semiconductor layer, *Kuboi*'s pixels (i.e., pillars) comprise Si. Lebby, ¶116.

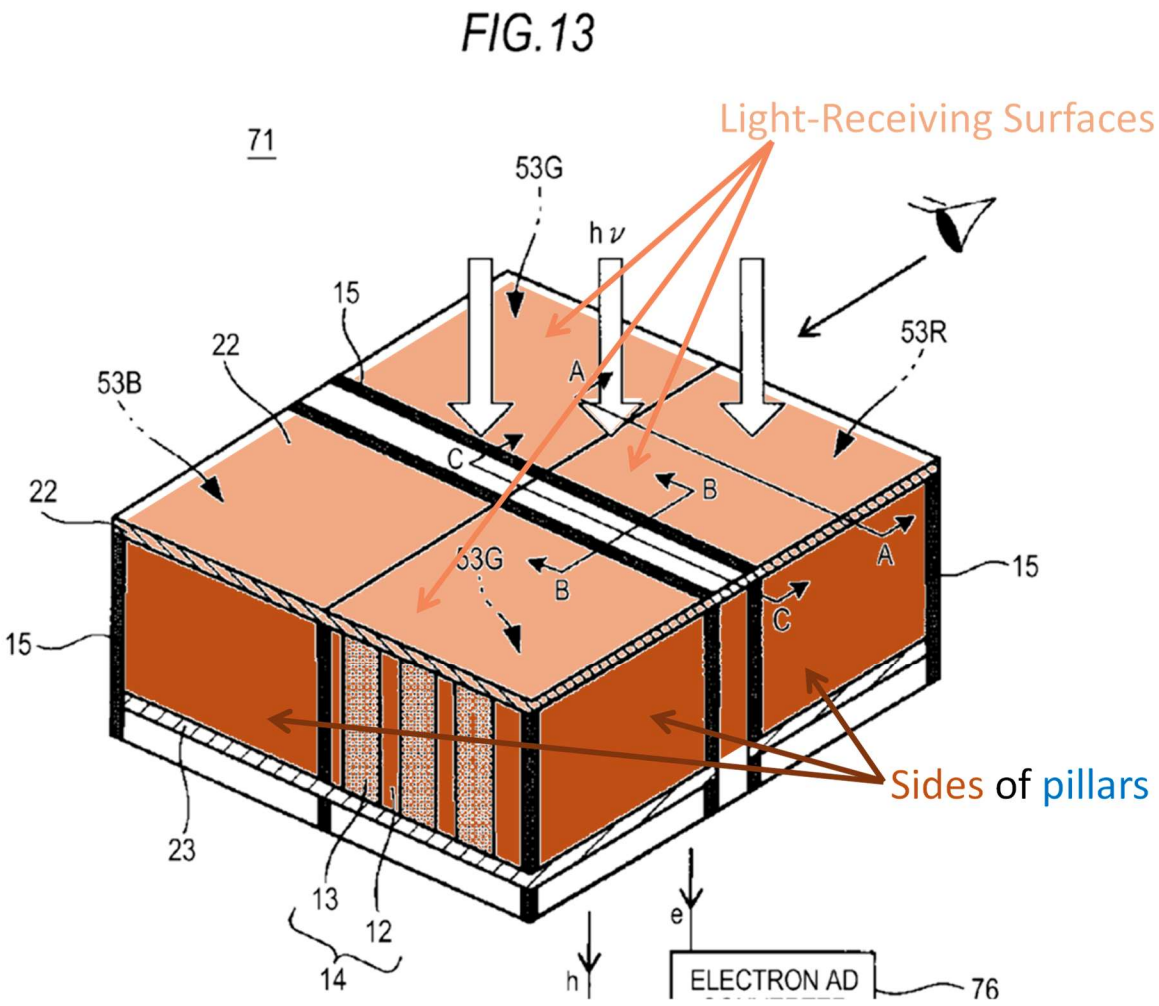
c. [1a(2)] "wherein at least some of the pillars are configured to include photodetectors and have respective light-receiving surfaces and respective sides;"

Kuboi discloses [1a(2)]. Lebby, ¶¶117-122. The pixel region of *Kuboi*'s "imaging device" includes "a plurality of pixels 202 which include a photoelectric conversion portion and which are regularly arranged in a two-dimensional array." *Kuboi*, ¶[48]. Specifically, *Kuboi*'s imaging device includes "red, blue, green, and green pixels … arranged in a two-dimensional array." *Kuboi*, ¶¶[90], [181]. "Light hν enters the p-type organic photoelectric conversion films 13" of *Kuboi*'s pixels. *Kuboi*, ¶¶[186], [64]. *Kuboi*'s "upper electrode 22 on the light incident side is formed of a transparent electrode." *Kuboi*, ¶[93]. A POSITA would have understood that the light incident side ("light-receiving surfaces") of *Kuboi*'s pixels (i.e., pillars) are located on upper electrode 22's lower surface because electrode 22 is formed *on* the light incident side. Lebby, ¶118. In the figures below, each pixel constitutes a pillar in the two-dimensional array and light hν is incident on and enters via each pixel's light-receiving surface.

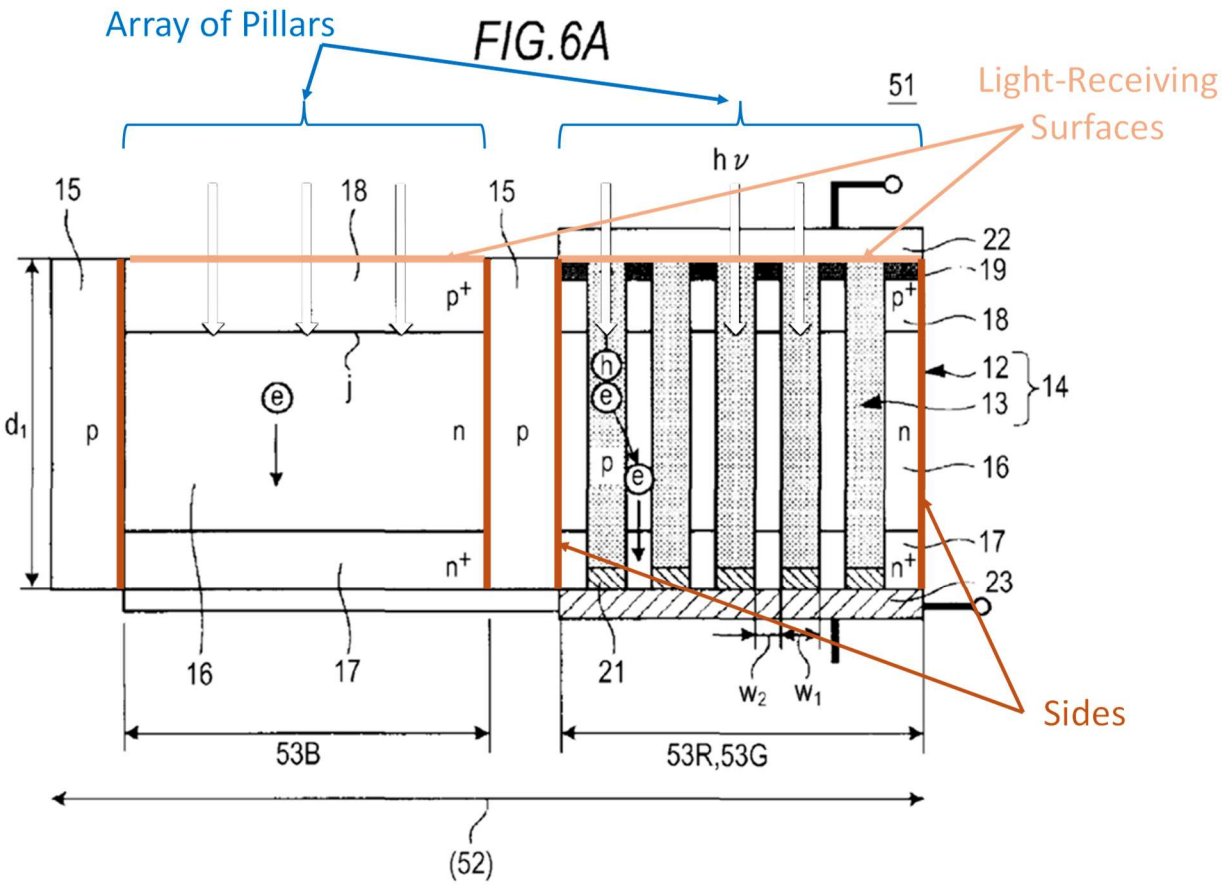
FIG.13



Kuboi, Fig. 13 (cropped). And the pixels (i.e., pillars) have sides:



Id. (cropped). A cross-sectional view of *Kuboi*'s array of pillars illustrating these features is shown below.



Kuboi, Fig. 6A.

Kuboi discloses that "blue pixel 53B is formed by a photoelectric conversion portion which is formed of a photodiode PD formed in a silicon semiconductor region, and the red pixel 53R, the green pixel 53G, and the green pixel 53G are formed by the hybrid photoelectric conversion portion 14 shown in FIGS. 1A and 1B." *Kuboi*, ¶[90]; *see also Kuboi*, ¶¶[48], [55], [69]-[71], [79]-[80], [91], [108], [181]. Thus, blue pixel 53B is a photodetector because it includes a photoelectric conversion portion. Lebby, ¶121.

Further, regarding red pixel 53R and green pixels 53G, *Kuboi* discloses that "[l]ight hν passes through the on-chip microlens to enter the p-type organic photoelectric conversion film 13 [embedded in these pixels], in which the light is subjected to photoelectric conversion, whereby electron-hole pairs are generated." *Kuboi*, ¶[64]. Accordingly, photoelectric conversion portions 14 of red and green pixels (53R, 53G) are also photodetectors because they generate electric charges by photoelectric conversion of received light. Lebby, ¶122.

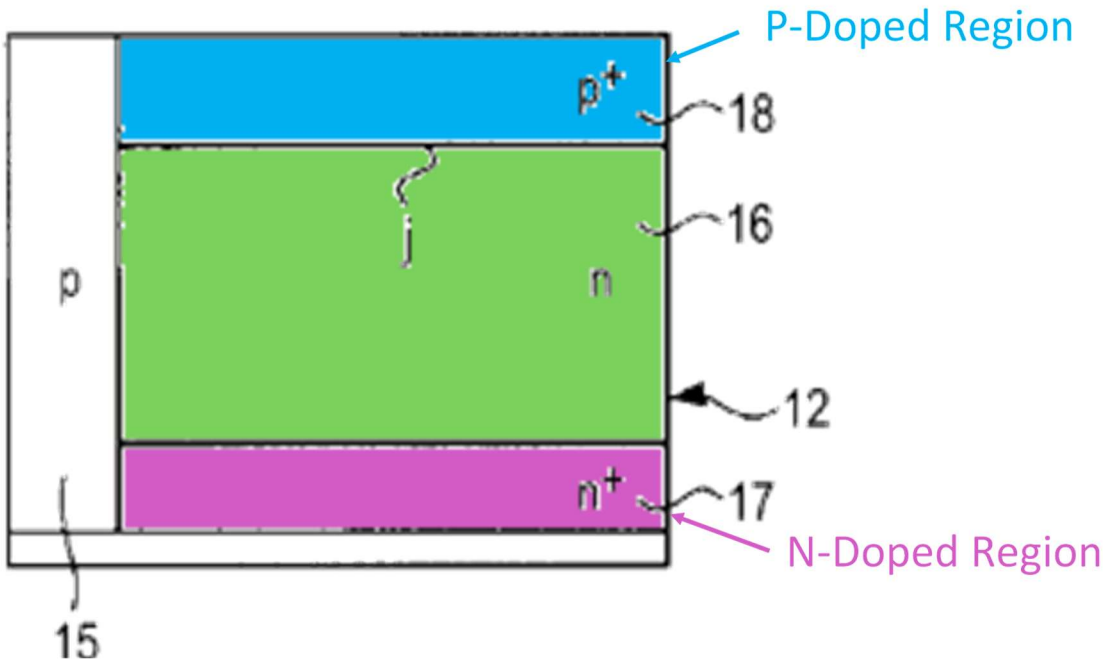
d. [1b] "wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;"

Kuboi discloses and/or renders obvious [1b]. Lebby, ¶¶123-133. *Kuboi*'s imaging device includes an array of pixels, each of which is a pillar. VI.A.3.b (claim [1a(1)]); *Kuboi*, ¶[90]. In blue pixel 53B (i.e., a pillar), "a p^+-type semiconductor region 18, an n-type semiconductor region 16, and a[n] n^+-type semiconductor region 17 are formed in that order from the light incident surface of the semiconductor layer 12 toward the opposite surface." *Kuboi*, ¶[91]; *see also* *Kuboi*, ¶¶[71], [181]. In red pixel 53R and green pixels 53G, "the same p^+-type semiconductor region 18, n-type semiconductor region 16, and n^+-type semiconductor region 17 are formed." *Kuboi*, ¶[91]. In other words, the red, blue,

and the green pixels of *Kuboi*'s imaging device have a p^+-type region 18, an n-type region 16, and an n^+-type region 17. Lebby, ¶124.

Kuboi's silicon "semiconductor layer 12 is implanted with impurities … [to form] a[n] n^+-type semiconductor region 17 having higher concentration [of impurities] than the n-type semiconductor region 16, and a [p^+-type] semiconductor region 18 of second conductivity type having higher concentration [of impurities] than the n-type semiconductor region 16." *Kuboi*, ¶¶[55]-[56]; *see also Kuboi*, ¶¶[111], [151], [7]. The process of implanting impurities into silicon is known as "doping." Lebby, ¶¶125-126 (citing Ex-1013, 4; Ex-1012, 37; Ex-1011, 5 ("doping")). Therefore, p^+-type region 18 is a "P-doped" region, and n^+-type region 17 is an "N-doped" region. Lebby, ¶¶127-128.

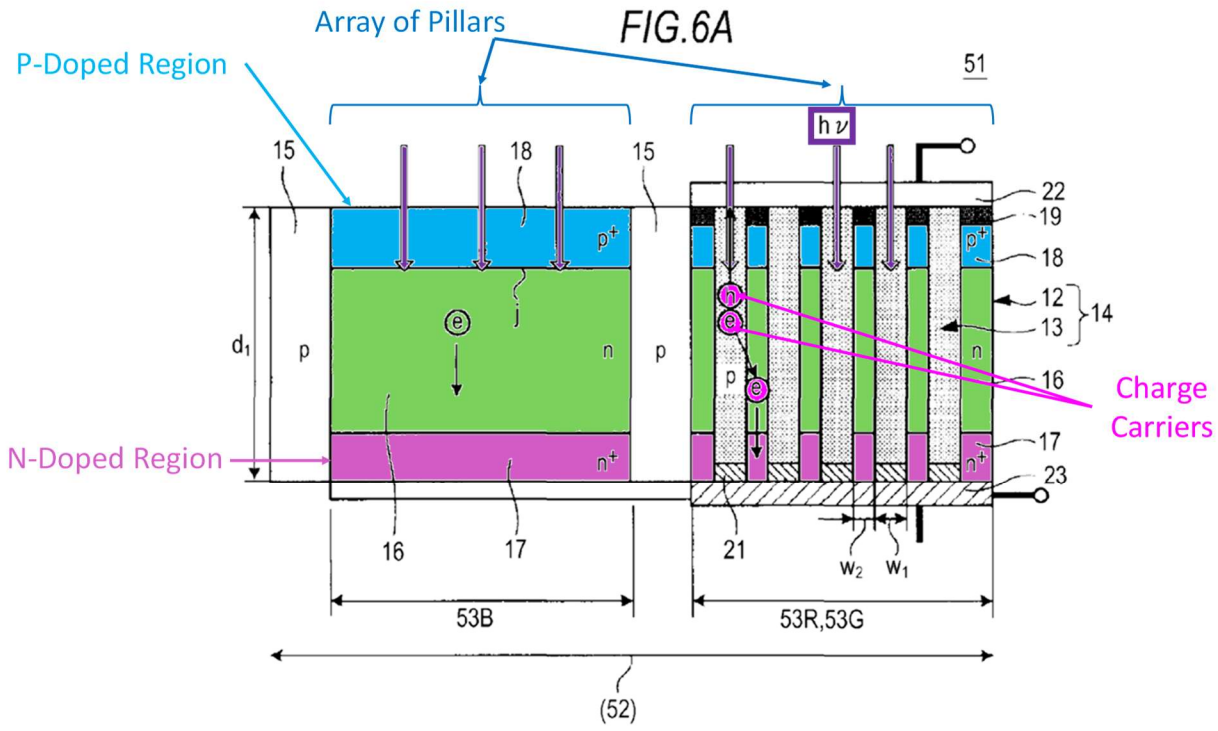
FIG.4A



Kuboi, Fig. 4A.

As explained for claim [1a(2)] (VI.A.3.c), *Kuboi*'s imaging device includes a pixel group composed of blue pixel 53B, red pixel 53R, and green pixels 53G, arranged in a two-dimensional Bayer configuration with corresponding color filters. Blue pixel 53B is formed by a photoelectric conversion portion comprising a photodiode (PD), while red pixel 53R and green pixels 53G are formed using the photoelectric conversion portion 14. *Kuboi*, ¶[90]. Photoelectric conversion portion 14 includes organic photoelectric conversion film 13 embedded in holes etched in the semiconductor layer 12. *Kuboi*, ¶¶[55], [67], [91], [181]. *Kuboi*

explains that light (hν) passes through the on-chip microlens and color filter to enter the organic photoelectric conversion film 13 of pixel 11, where it undergoes photoelectric conversion to generate electron-hole pairs (or charge carriers). *Kuboi*, ¶¶[64], [90], [93]. Thus, *Kuboi*'s pillars generate electron-hole pairs (charge carriers) when illuminated with light hν incident on the array of pillars. Lebby, ¶¶129-130; *Kuboi*, ¶¶[87], [107]. This is illustrated below.



Kuboi, Fig. 6A. *Kuboi* discloses that the silicon photodiode that comprises the blue pixel 53B also generates "charge carriers" when illuminated with light. Lebby, ¶¶131-132; *see Kuboi*, ¶¶[6], [149]. Thus, *Kuboi*'s blue pixel 53B, red pixel 53R,

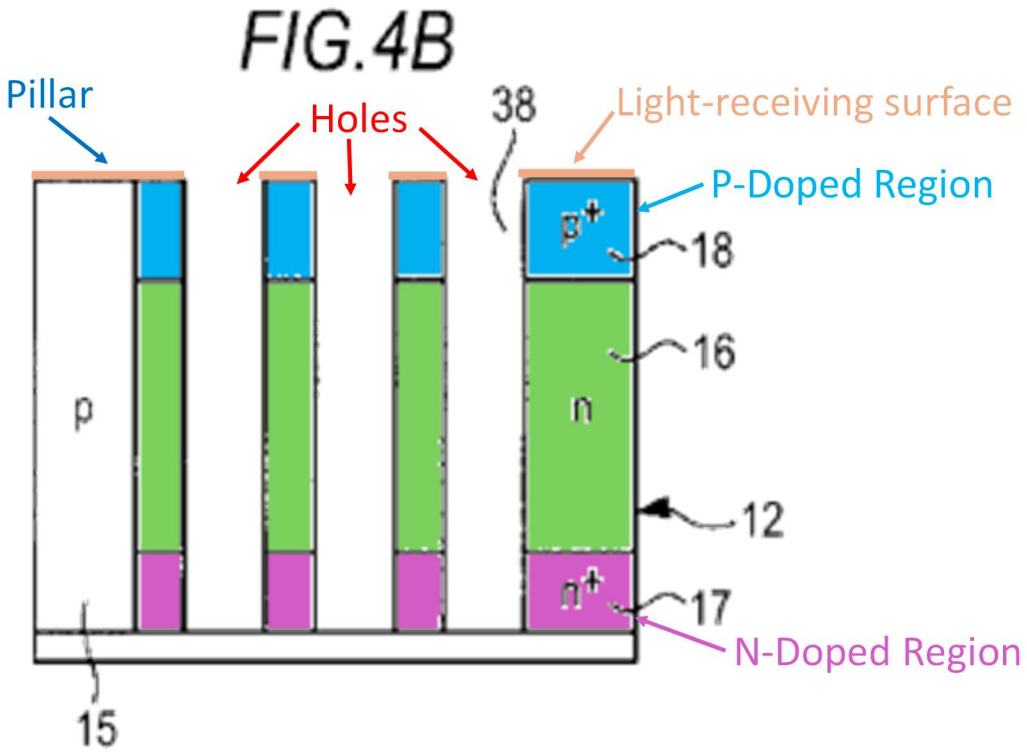
and two green pixels 53G ("pillars") generate "charge carriers" when illuminated with light (hν). *Kuboi*, ¶¶[87], [107].

Kuboi's imaging device can be used in the visible light region and in other wavelength bands, including infrared. *Kuboi*, ¶[190]. *Kuboi*'s organic material is sensitive to (i.e., generates electric charge carriers in response to) "visible light " but compounds sensitive to infrared rays can also be used. *Id.*; *see also Kuboi*, ¶[58]. A POSITA would have found it obvious that by selecting a suitable organic material, *Kuboi*'s photodetectors would respond to light in a wavelength range selected from the visible and infrared light spectrum, as claimed. Lebby, ¶133. A POSITA would also have had a reasonable expectation of success in doing so because *Kuboi* already discloses selecting the organic photoelectric film material to detect light in selected visible and/or infrared wavelength ranges. *Id.*; *Kuboi*, ¶[58].

e. [1c] "one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other shapes at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;"

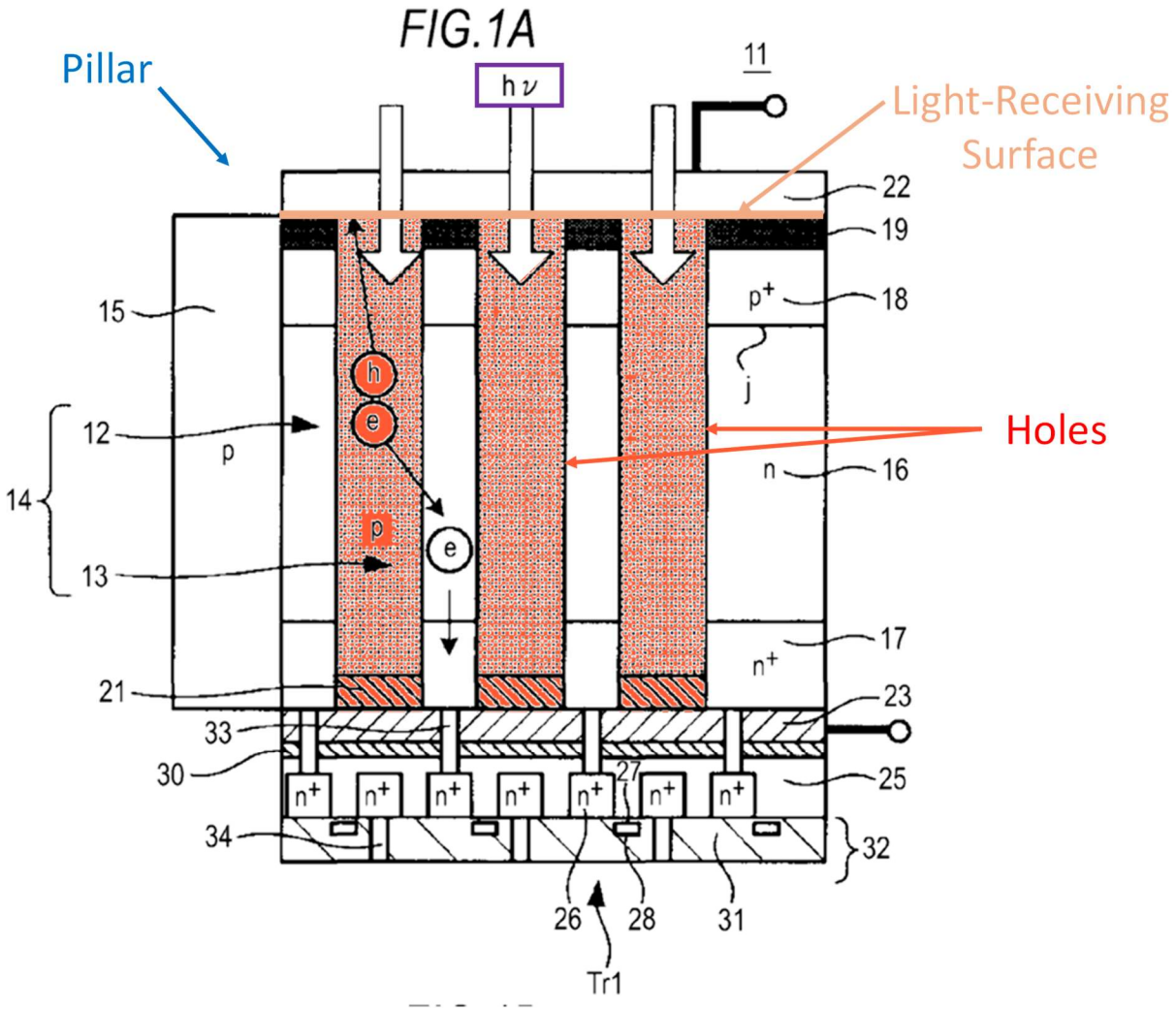
Kuboi discloses [1c]. Lebby, ¶¶134-155. *Kuboi* discloses that "hole 38 such as a trench or a via extending from the p^+-type semiconductor region 18 to the n^+-type semiconductor region [17] is formed in a region of the semiconductor layer 12

corresponding to one pixel by dry-etching." *Kuboi*, ¶[72]; *see also Kuboi*, ¶¶[13]-[14], [95].

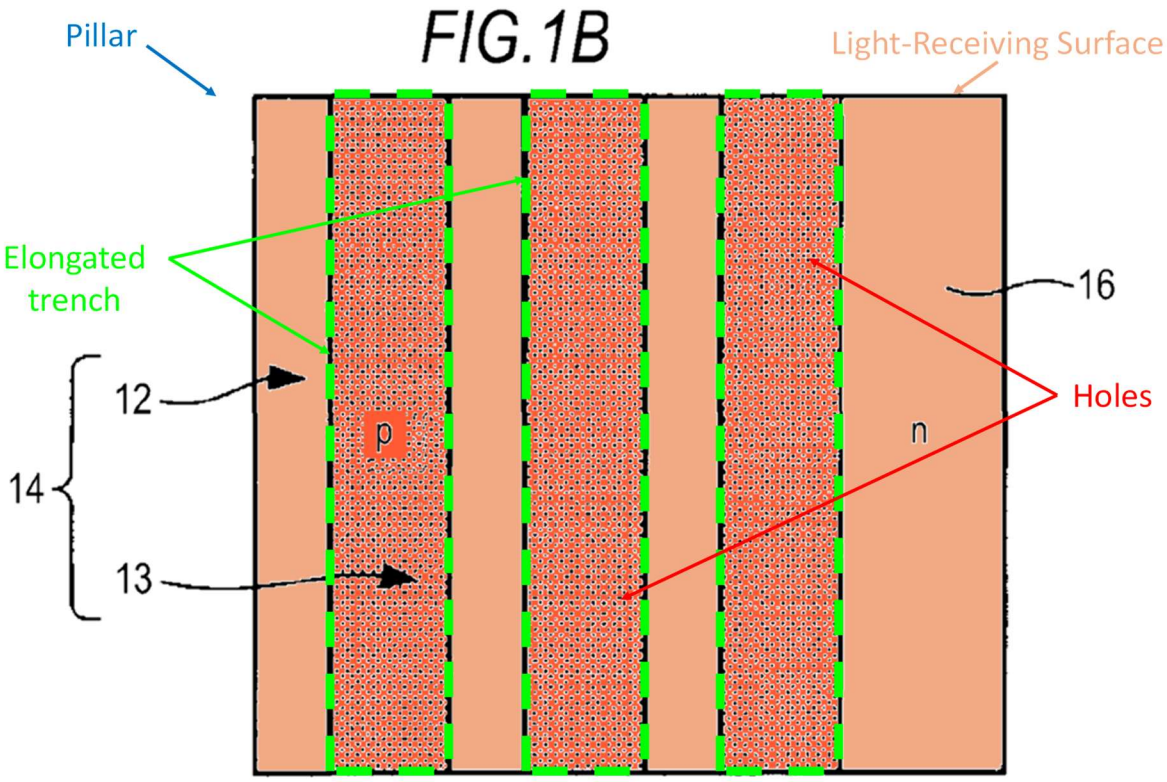


Kuboi, Fig. 4B. *Kuboi* explains that a "plurality of vertical holes 38 are formed at necessary intervals." *Kuboi*, ¶[72]. Because the holes 38 that extend from p^+-type region 18 to n^+-type region 17 are formed by dry-etching, *Kuboi*, ¶¶[72], [95], they are "fabricated." Lebby, ¶¶136-137.

Kuboi describes its vertical holes as "so-called … trench[es]." *Kuboi*, ¶[67]. "[A]s shown in FIG. 1A [below], the vertical holes 38 are formed in a stripe shape as seen in a planar view." *Kuboi*, ¶[72].



Kuboi, Fig. 1A. The "organic photoelectric conversion film 13 is deposited so as to be embedded in the vertical holes 38." *Kuboi*, ¶[73]. "[A]s shown in FIG. 1B [below], the plurality of organic photoelectric conversion films 13 are formed in a stripe shape so as to divide the semiconductor layer 12 into a plurality of parts as viewed from the upper surface." *Kuboi*, ¶[57].



Kuboi, Fig. 1B. As seen in the plan view of Figure 1B, above, the holes in the light-receiving surface of *Kuboi*'s pixel (i.e., pillar) have an elongated shape. Lebby, ¶¶140-143.

Although Figures 1A-1B illustrate only one pixel (i.e., pillar), as discussed for claim [1a(1)], *Kuboi*'s imaging device includes an array of pixels (53B, 53R and 53G). VI.A.3.b. Among these pixels, pixels 53R and 53G have structures similar to the pixel of Figures 1A-1B. *Kuboi*, ¶[90]. Thus, a POSITA would have understood that *Kuboi*'s imaging device has a plurality of pixels 53R and 53G (i.e., "pillars"), including multiple holes fabricated as recesses at the light-receiving

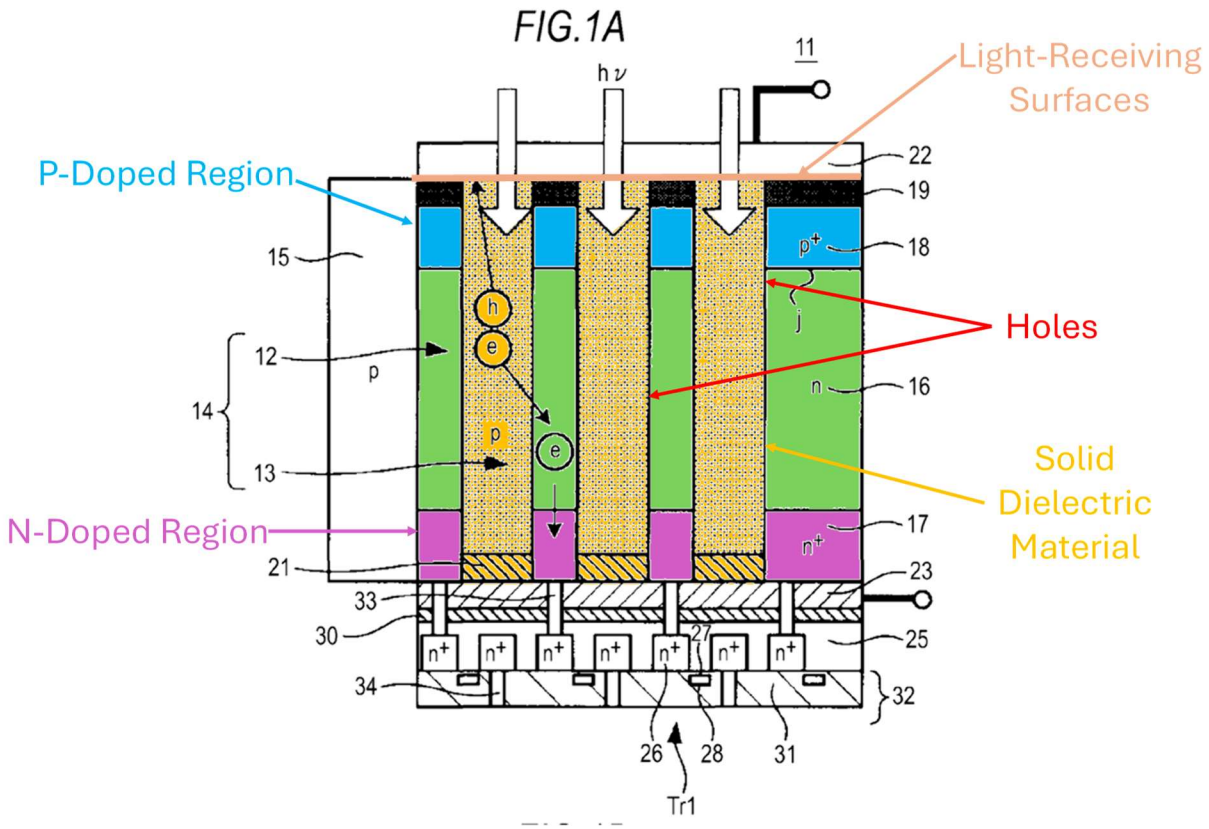
surfaces of these pixels, and that the holes in each of these pixels have an elongated shape parallel to the pixel's light-receiving surface. Lebby, ¶144.

Kuboi also discloses that "an electron blocking film 21 having a thickness of several tens of nm, for example[,] is formed on the bottom portions of the vertical holes 38." *Kuboi*, ¶¶[73], [91]. "[F]ilm 21 is formed by an insulating film such as, for example, a silicon nitride (Si_3N_4) film[or] a silicon [oxide] (SiO_2) film." *Kuboi*, ¶[73]. Silicon nitride (Si_3N_4) and silicon oxide (SiO_2) are solid dielectric materials. Lebby, ¶¶145-151 (citing Ex-1013, 34-35; Ex-1012, 20). Film 21 serves as an electron-blocking layer that prevents signal charges (electrical charges) from migrating from the organic film 13 in holes 38 to lower electrode 23. *Kuboi*, ¶¶[59]-[60], [64], [73]. Thus, the elongated holes in pixels 53G and 53R ("pillars") "are filled at least partly with solid dielectric material." Lebby, ¶152.

Like the organic material in the holes of the '948 Patent, an organic material is deposited to fill the remaining portions of the holes, thereby forming organic photoelectric conversion films 13 embedded within the hole. *Kuboi*, ¶¶[73], [58], [85], Fig. 4C; '948 Patent, 50:12-17. *Kuboi* discloses that "[a]s the p-type organic material [is] sensitive to a visible light region, perylene-based compounds, phthalocyanine compounds, quinacridone compounds, porphyrin compounds, merocyanine compounds, and the like can be used." *Kuboi*, ¶[58]. A POSITA would have understood that phthalocyanine, perylene-based, and porphyrin

compounds are solid dielectric materials. Lebby, ¶¶150-152 (citing Exs-1014-1020).

Thus, as illustrated below, electron blocking film 21 and photoelectric conversion film 13 together entirely fill *Kuboi*'s holes and are solid dielectric materials.



Kuboi, Fig. 1A.

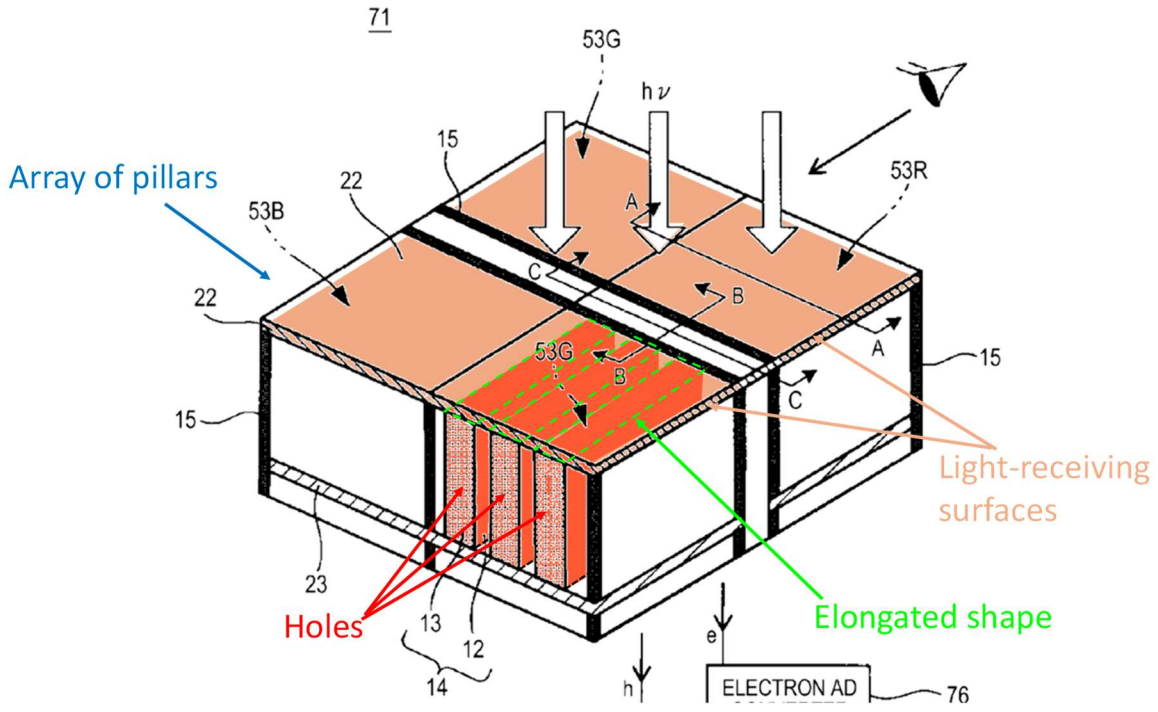
Kuboi also discloses that semiconductor layer 12's thickness d_1 is "about 1.4 μm," which equals 1400 nm. *Kuboi*, ¶[94], Fig. 6A; Lebby, ¶154. Because holes 38 extend from the top surface of p^+-type region 18 to the bottom surface of n^+-type

region 17 of semiconductor layer 12, *see Kuboi*, ¶[72], Fig. 4B, holes 38 extend into pixels 53G and 53R to a depth of 1400 nm, which falls within the claimed 100-10,000 nm range. Lebby, ¶¶154-155.

f. [1d] "wherein at least some of the holes are elongated along the respective light-receiving surfaces;"

Kuboi discloses [1d]. Lebby, ¶156. As explained for claim [1c], *Kuboi*'s imaging device includes multiple holes—stripe-shaped in a planar view—within pixels 53R and 53G, which are elongated along the light-receiving surface of the respective pixel. VI.A.3.e; *Kuboi*, ¶¶[11], [57], [72].

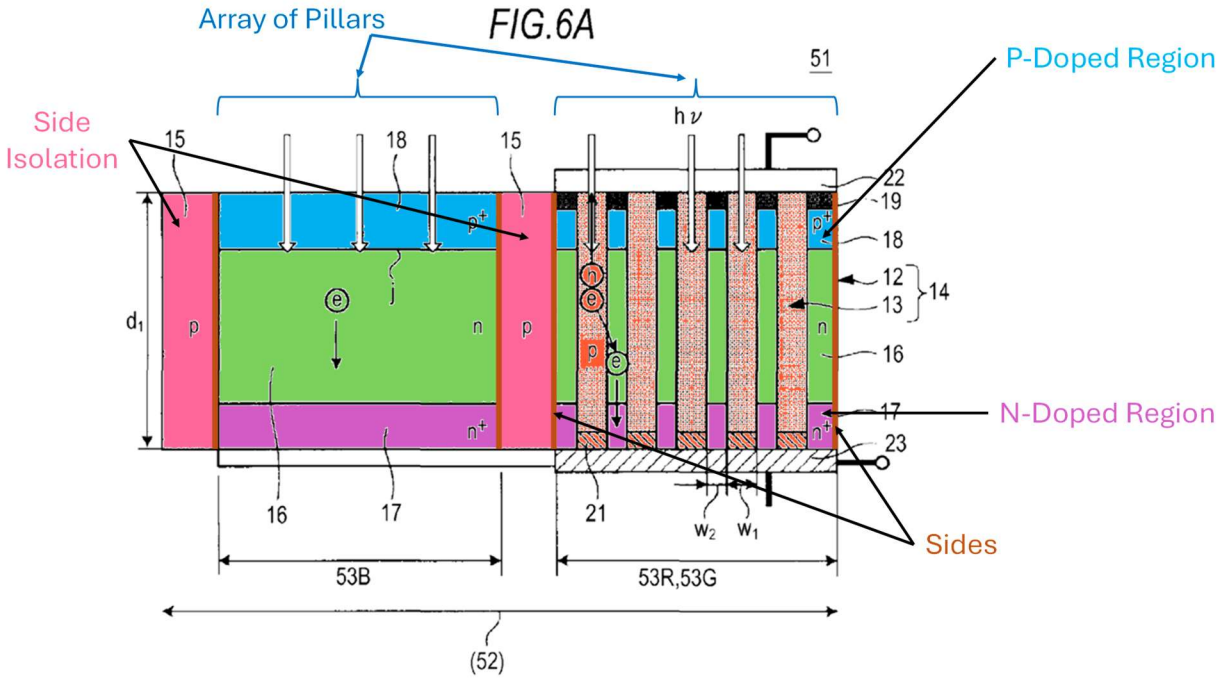
FIG.13



Kuboi, Fig. 13 (cropped).

g. [1e] "side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;"

Kuboi discloses [1e]. Lebby, ¶¶157-158. *Kuboi*'s "silicon semiconductor layer 12 is divided into respective pixels by an element separation region 15 which [can be] formed by a p-type semiconductor region." *Kuboi*, ¶¶[91], [55]-[56], [71], [182]. *Kuboi*'s "pixel 11 is [also] separated by an element separation region 15." *Kuboi*, ¶[55]. A POSITA would have understood that element separation region 15 provides side-isolation because it separates adjacent pixels, which each include photoelectric conversion portions. Lebby, ¶158; VI.A.3.c (claim [1a(2)]). Element separation region 15 is a region of ***silicon*** semiconductor layer 12. *Kuboi*, ¶[71]. A POSITA would have known that silicon is a solid semiconductor material. Lebby, ¶158. A POSITA would have understood that, because *Kuboi*'s p-type semiconductor region—including element separation region 15—is part of ***silicon*** semiconductor layer 12, element separation region 15 is a solid material. *Id.* *Kuboi*'s side-isolation is provided by element separation region 15 between at least portions of the sides of at least some of *Kuboi*'s pixels (pillars) as illustrated below.

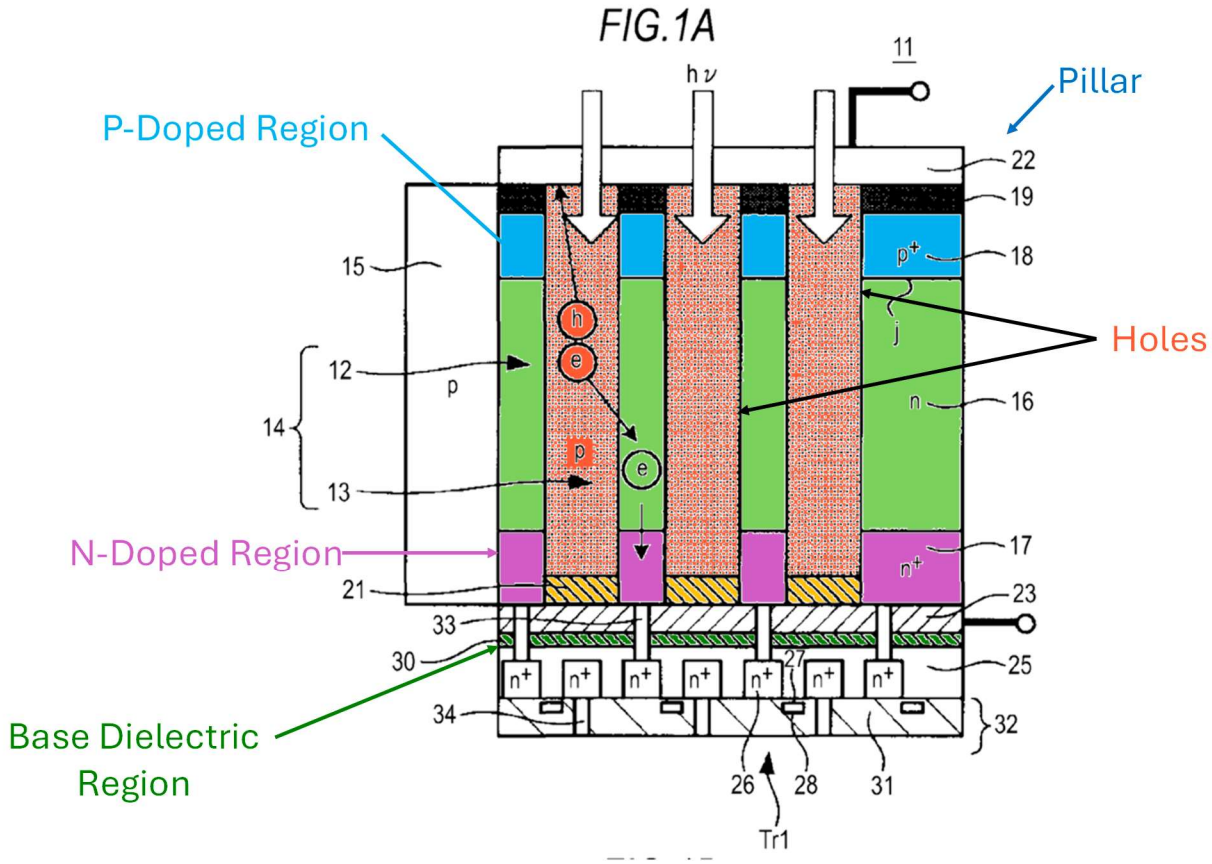


Kuboi, Fig. 6A.

h. [1f] "a solid dielectric material forming a base dielectric region for the array;"

Kuboi discloses and/or renders obvious [1f]. Lebby, ¶¶159-165. *Kuboi*'s "semiconductor region 25 formed of silicon … is disposed on the front surface side of the semiconductor layer 12, namely under the lower electrode 23 with an insulating film 30 disposed therebetween." *Kuboi*, ¶[61]. *Kuboi* discloses a semiconductor substrate on which the semiconductor region 25 having pixel transistors, the multilayer wiring layer 32, and the lower electrode 23 are formed. *Kuboi*, ¶[69]. *Kuboi*'s multilayer wiring layer 32 includes a plurality of layers of wiring with an interlayer insulating film 31 disposed therebetween. *Kuboi*, ¶[62].

Insulating film 30 and/or insulating interlayer film 31 are disposed at the base of *Kuboi*'s pillars and constitute the claimed base dielectric region. Lebby, ¶160.



Kuboi, Fig. 1A.

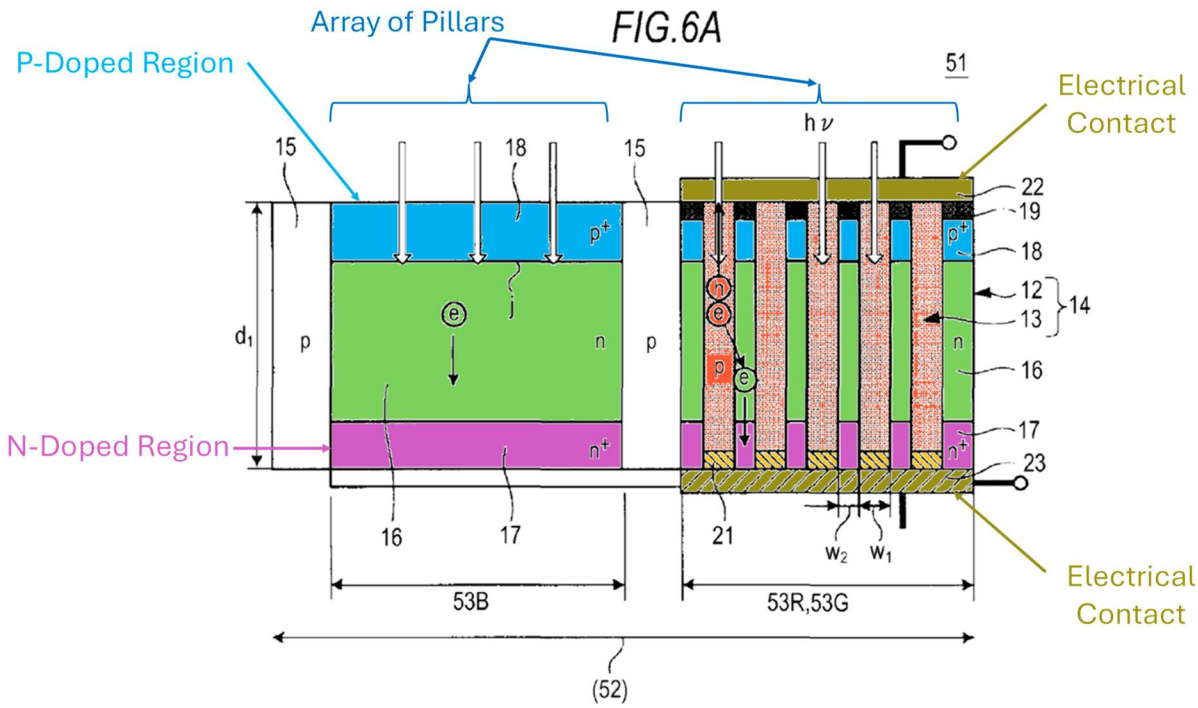
Although Figure 1A illustrates only one pixel, *Kuboi*'s imaging device includes a plurality of pixels (53R and 53G) arranged as an array of pixels. *See* VI.A.3.b (claim [1a(1)]). Pixels 53R and 53G have structures similar to the pixel of Figures 1A-1B. *Kuboi*, ¶[90]. A POSITA would have understood that *Kuboi*'s multilayer wiring board with film 31 is located below *Kuboi*'s array of pixels,

including pixels 53R and 53G. Lebby, ¶¶160-161. Thus, Figure 1A's base dielectric region is a base dielectric region for *Kuboi*'s array of pixels.

A POSITA would have understood that insulating films (i.e., 30 and/or 31) like those of *Kuboi* constitute dielectric materials like silicon oxide or silicon nitride, or at least would have been motivated to use such dielectric materials because such materials are conventionally used to separate metal lines in CMOS circuits, can be fabricated using standard CMOS fabrication processes, and provide good barriers to impurity and moisture diffusion. Lebby, ¶¶161-164 (citing Ex-1013, 9-14, 34-35; Ex-1012, 4, 5, 20, 34; Ex-1026, 26:7-14; Ex-1027, ¶¶[13]-[14]). Indeed, *Kuboi* uses "insulating film" to refer to films made of dielectric materials such as silicon nitride (Si_3N_4), silicon oxide (SiO_2) film, or similar materials. *See Kuboi*, ¶[59]. Thus, a POSITA would have found it obvious to form *Kuboi*'s insulating film 30 or 31 (i.e., base dielectric material) of a solid dielectric material like silicon oxide or silicon nitride. Lebby, ¶¶162-165. A POSITA would also have had a reasonable expectation of success in forming insulating film 30 or 31 using a solid dielectric material because methods for fabricating such films using dielectric materials were well known in the art. Lebby, ¶¶163-165.

i. [1g] "electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;"

Kuboi discloses [1g]. Lebby, ¶¶166-174. The photoelectric conversion portions of *Kuboi*'s pixels (including pixels 53B, 53G, and 53R) are photodetectors. VI.A.3.c (claim [1a(2)]). *Kuboi*'s "electrodes 22 and 23 [are] formed on the entire rear and [front] surfaces of the semiconductor layer 12" of the photoelectric conversion portions. *Kuboi*, ¶¶[60], [77], [93], [103]; Lebby, ¶167. "[U]pper electrode 22 on the rear surface side is formed by a transparent electrode formed of a transparent conductive film." *Kuboi*, ¶[60]. And "lower electrode 23 is formed of metal exhibiting ohmic properties." *Id. Kuboi*'s electrodes, which are electrical contacts to its photoelectric conversion portions, are illustrated below:



Kuboi, Fig. 6A.

Kuboi explains that "[l]ight hν passes through the on-chip microlens to enter the p-type organic photoelectric conversion film 13, in which the light is subjected to photoelectric conversion, whereby electron-hole pairs are generated." *Kuboi*, ¶[64]. A "necessary voltage is applied between the upper electrode 22 and the lower electrode 23." *Id. Kuboi* discloses "electrons e … move from the organic photoelectric conversion film 13 … toward the semiconductor layer 12 depleted by the applied bias voltage," and "hole h moves toward the upper electrode 22 through the organic photoelectric conversion film 13 and is discharged through the upper electrode 22." *Id.* Because the holes generated in *Kuboi*'s pixels (i.e., pillars) move through electrodes 22, and because electrons (e) move into semiconductor

layer 12 due to a bias voltage applied between electrodes 22 and 23, these electrodes provide electrical pathways to the photoelectric conversion portions (photodetectors) of at least some of *Kuboi*'s pixels. Lebby, ¶169; VI.A.3.c (claim [1a(2)]).

Kuboi discloses that "[a] necessary [bias] voltage is applied between the upper electrode 22 and the lower electrode 23 so that the upper electrode 22 has the negative potential, and the lower electrode 23 has the positive potential." *Kuboi*, ¶[64]. The "necessary bias voltage" is applied between electrodes 22 and 23 so that p^+-type region 18 of the photoelectric conversion portion is at a negative potential and n^+-type region 17 is at a positive potential. *Kuboi*, ¶[64]; Lebby, ¶¶169-171. A POSITA would have understood that applying a positive voltage to n^+-type region 17 with respect to p^+-type region 18 constitutes reverse-biasing the photoelectric conversion portion. Lebby, ¶171 (citing Ex-1023, 3-5, 8).

A POSITA would have understood that *Kuboi*'s imaging device selects the bias voltage for the level of reverse biasing needed to maintain performance under changing operating conditions. Lebby, ¶¶172-174 (citing Ex-1032, 1, 4-6, 10; Ex-1043, 1-6; Ex-1044, 4-17; Ex-1046, 4-29). According to Dr. Lebby, a POSITA would have understood that by selecting the "necessary voltage" based on the existing operating conditions, *Kuboi* enables stable operation across varied ambient conditions. *Id*.

Because *Kuboi* allows reverse biasing of particular pixels and allows for selection of *necessary* voltage for reverse biasing, a POSITA would have understood that *Kuboi*'s electrical contacts (electrodes 22 and 23) are configured to provide electrical pathways for selected reverse biasing as claimed. Lebby, ¶174.

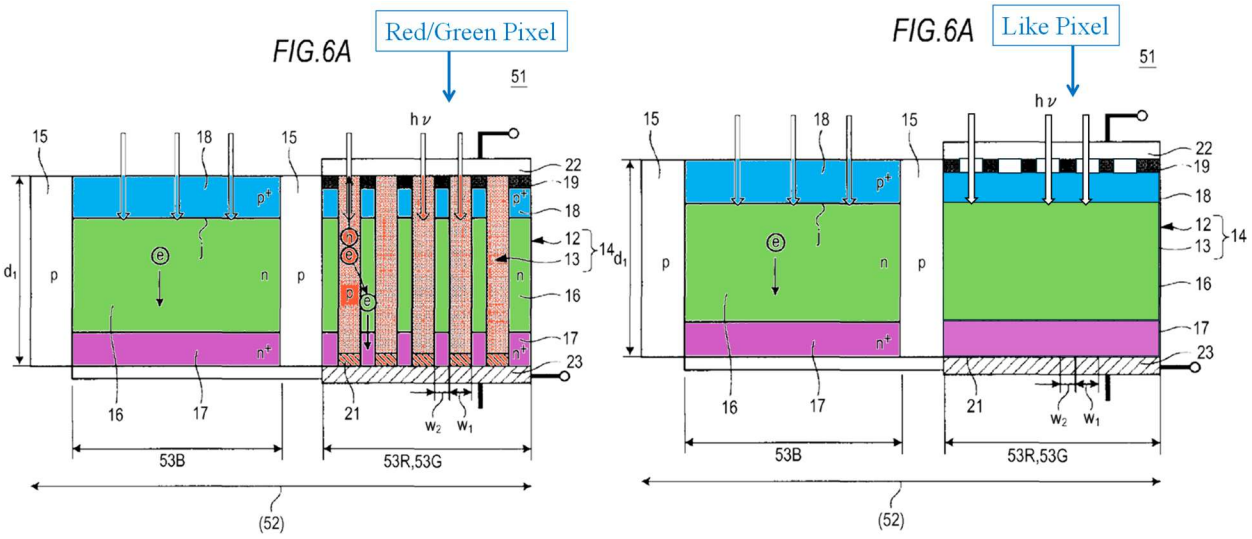
j. [1h] "wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes."

Kuboi discloses and/or renders obvious [1h] when considered in light of a POSITA's understanding prior to the priority date of the '948 Patent. Lebby, ¶¶175-201. Furthermore, Patent Owner's statements in the '948 Patent confirm this finding. Lebby, ¶¶175-176, 188-201.

A POSITA would have found *Kuboi* discloses [1h]. Lebby, ¶¶175-201. A POSITA would have understood that the amount of light absorbed by a material of thickness "d" can be determined using the Lambert-Beer expression as $I_0 (1- e^{\alpha d}) A$, where I_0 is the incident light intensity, α is the material absorption coefficient, and A is the light incidence area. Lebby, ¶176 (citing Ex-1028, 22-25; Ex-1029, 2-5). *Kuboi*'s red and green pixels have 1.4 μm deep holes filled with phthalocyanine and porphyrin compounds, respectively. *Kuboi*, ¶¶[92], [94]. Compared to silicon, the absorption coefficient of porphyrin compounds is higher in the green light wavelength range of 510-580 nm, and the absorption coefficient

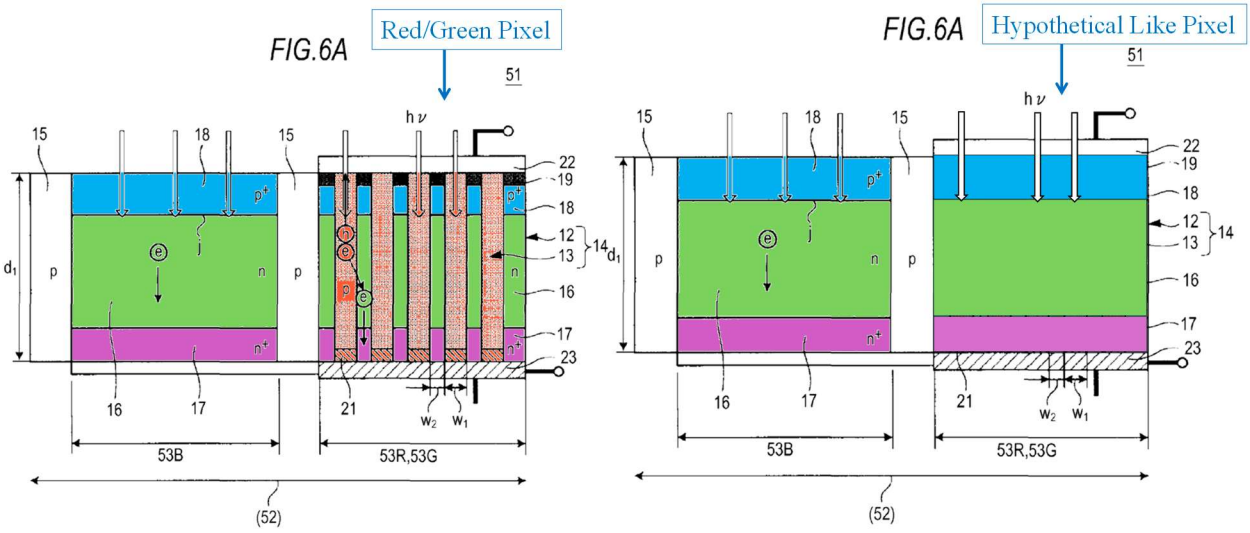
of phthalocyanine compounds is at least ten times larger for the red light wavelength range of 620-750 nm. Lebby, ¶¶177-179 (citing data from Ex-1030, 7 (Fig. 6); Ex-1031, 2-4 (Table 1); 1032, 3 (Fig. 1)). The higher absorption coefficient of *Kuboi*'s organic films increases light absorption by more than 10% over a comparable photodetector lacking holes. Lebby, ¶177.

The figures below illustrate the structure of *Kuboi*'s red or green pixels 53R or 53G (left) and a *like* pixel (right) lacking the holes. Lebby, ¶180. Because both *Kuboi*'s 53R or 53G pixel and the *like* pixel include *Kuboi*'s light shielding film 19, both have the same area of light incidence, defined by the light shielding film openings. *Id.*



Kuboi, Fig. 6A. The figures below illustrate the structure of *Kuboi*'s red or green pixels 53R or 53G (left) and a *hypothetical like* pixel (right) lacking the holes and the light shielding film. Lebby, ¶181. The light incidence area for *Kuboi*'s red or

green pixels (53R or 53G), as defined by the openings in the light shielding film is about 71% of the light incidence area for the *hypothetical like* pixel. Lebby, ¶182.



Kuboi, Fig. 6A.

Figure A below illustrates the ratio, $P_{abs\text{-}organic}$ / $P_{abs\text{-}silicon}$, for the green light wavelength range of 490-580 nm (Ex-1025, ¶[23]), where, $P_{abs\text{-}organic}$ represents the amount of light absorbed by *Kuboi*'s green pixel and $P_{abs\text{-}silicon}$ represents the amount of light absorbed by a pixel without holes. Lebby, ¶¶182-184.

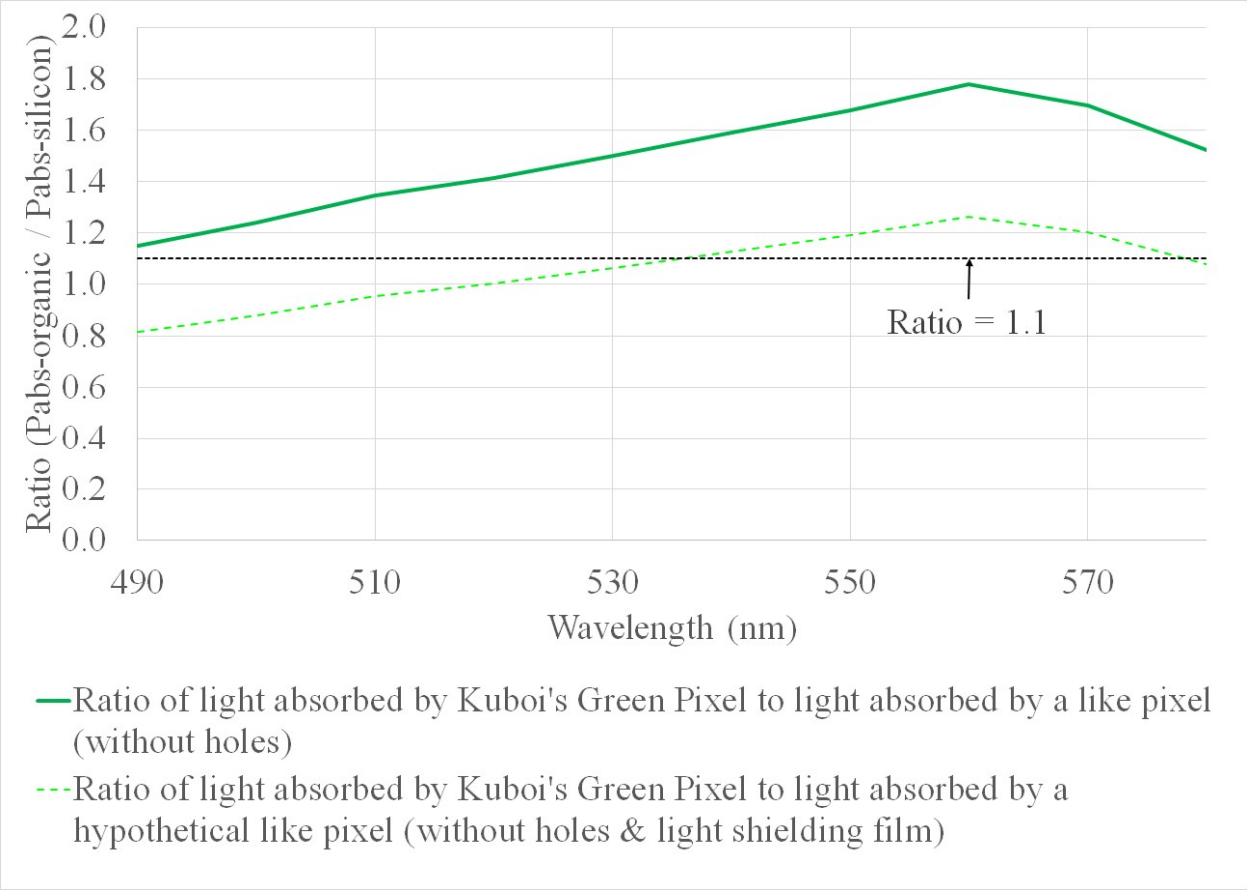


Figure A

In the above figure, the ratio $P_{abs\text{-}organic}$ / $P_{abs\text{-}silicon}$ for the *hypothetical like* pixel is obtained by scaling the same ratio for the *like* pixel by 71%. Lebby, ¶¶183-184. As illustrated, the ratio $P_{abs\text{-}organic}$ / $P_{abs\text{-}silicon}$ is greater than or equal to 1.1 (shown by the dashed black line) for the entire green light wavelength range for the *like* pixel and for the 540-570 nm wavelength range for the *hypothetical like* pixel. *Id.*

Figure B below illustrates the ratio, $P_{abs\text{-}organic}$ / $P_{abs\text{-}silicon}$, for *Kuboi*'s red pixels, in the red-light wavelength range of 620-780 nm (Ex-1025, ¶[23]). Lebby, ¶¶185-186.

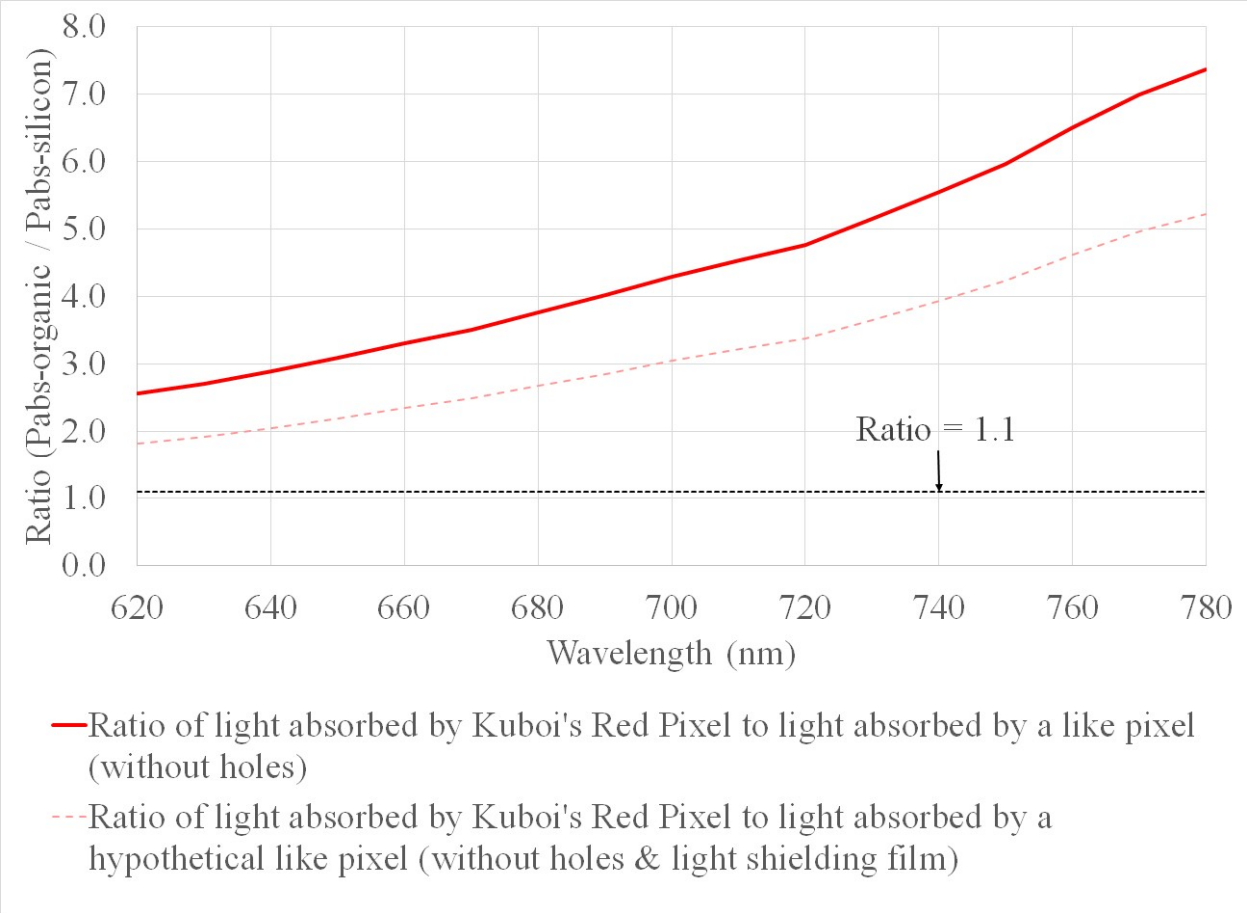


Figure B

As illustrated, the ratio $P_{abs\text{-}organic}$ / $P_{abs\text{-}silicon}$ is greater than or equal to 1.1 for the entire red light wavelength range for both the *like* pixel and the *hypothetical like* pixel. Thus, a POSITA would have understood that *Kuboi*'s photodetector with holes filled with organic material absorbs at least 1.1 times more light relative to a like photodetector having no holes at selected visible and infrared wavelength ranges of the light. Lebby, ¶¶186-187.

A POSITA would also have found [1h] disclosed in view of Patent Owner's statements in the '948 Patent. Lebby, ¶¶188-192. The '948 Patent details the cause or causes of the enhancement of the absorption coefficient, explaining:

> The cause or causes of the enhancement of the absorption coefficient are believed to include one or more of the following: an increase in optical field concentration, resonance effects, constructive and destructive optical interferences (amplitude and phase) effects, scattering, and *high contrast grating (HCG) effects*. [*See, e.g.*,] Chang-Hasnain et al[.], High contrast gratings for integrated optoelectronics, Advances in Optics and Photonics 4, 379-440 (2012), hereinafter "Chang-Hasnain." The HCG effects are at the near-wavelength regime ([*see*] Chang-Hasnain) where the optical wavelength in the material of the grating and the optical wavelength in the surrounding material of the grating is the range of the period of the grating.

'948 Patent, 11:52-64 (emphasis added). "The period of the 3D pillar/hole microstructured array can be seen as a 3D high contrast grating, whose period of the grating Λ can lie between λ/n_1 where n_1 is the optical refractive index of material M_1 and λ/n_2 where n_2 is the optical refractive index of material M_2." *Id*., 12:14-18. Further, "[i]f $n_1>n_2$ then $\lambda/n_1<\Lambda<\lambda/n_2$." *Id*., 12:18-19.

The ’948 Patent explains that the high contrast grating (HCG) effect may explain the high absorption coefficient of semiconductors with holes that satisfy the relationship $\lambda/n_1<\Lambda<\lambda/n_2$, stating:

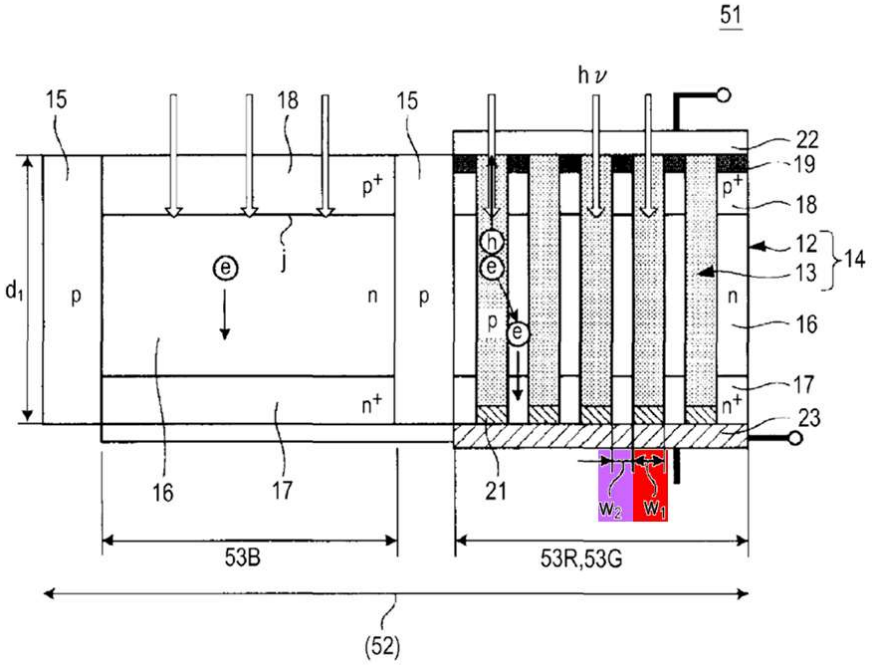
> The HCG effect that may explain the high enhancement of the absorption coefficient of the bulk material is that a single or multiple HCG layer (or a single microstructured pillar/hole array layer) due to its resonance effects and/or due to a varying of the microstructured pillar/hole period spacing, the optical signal resonating in the HCG/microstructured pillar-hole array can be directed to propagate in the plane of the HCG/microstructured pillar-hole array rather than normal to the surface. Together with resonance and in-plane propagation this can greatly increase the absorption path length in the HCG/microstructured pillar-hole array.

Id., 12:35-45. Finally, “[u]sing the phenomenon of near-wavelength and also deep-wavelength where the HCG period is much less than the optical wavelength, and the diffraction regime where the HCG period is greater than the optical wavelength (*see*, Chang-Hasnain) the microstructured pillar-hole-void array can have enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100.” *Id*., 12:49-55.

Relying on Chang-Hasnain (Ex-1033), Patent Owner thus represents in the '948 Patent that a microstructured pillar hole array having microstructure period Λ and satisfying the relationship λ/n1<Λ< λ/n2 forms a high contrast grating (HCG). Lebby, ¶¶188-192. Patent Owner also represents that if the microstructure pillar hole array forms an HCG, then the physical phenomenon of near-wavelength and deep-wavelength result in an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient. Lebby, ¶192.

Applying these representations to *Kuboi*, as illustrated below, *Kuboi* discloses width w1 of photoelectric conversion films 13 is 200 nm and width w2 of semiconductor layer 12 between the photoelectric conversion films is about 50 nm. *Kuboi*, ¶[94].

FIG.6A



Kuboi, Fig. 6A. The period Λ or center-to-center distance between holes for *Kuboi* is thus 250 nm. Lebby, ¶¶193-197. Visible light has wavelength in the range 400-700 nm and infrared light has wavelength in the range 750 nm-1000 μm. Lebby, ¶194 (citing Ex-1010, 4; Ex-1025, ¶[23]). The refractive index n_1 of silicon varies from about 3.5 (wavelength 1000 nm) to 5.8 (wavelength 300 nm). *Id.* (citing Ex-1047, 9:43-47, Fig. 4; Ex-1034, 48). The refractive index n_2 of the organic material in *Kuboi*'s holes ranges between 1.5-3.0. Lebby, ¶¶194-199 (citing Ex-1035, 86:35-48, 142:18-25; Ex-1030, 6, Fig. 5; Ex-1036, 13, Fig. 7; Ex-1037, Abstract).

Using the above values for wavelengths and refractive indices, Table A shows the calculated values of λ/n_1 and λ/n_2 for *Kuboi*'s green pixels with

porphyrin. *Kuboi*'s 250 nm hole pitch falls in the range λ/n_1 to λ/n_2 for at least part of the visible light spectrum (400-700 nm wavelengths) and at least part of the near infrared light spectrum (>700 nm wavelengths). Lebby, ¶¶194-199. For example, for the 550 nm green light wavelength, λ/n_1 (550/4.5 = 123) < Λ (250 nm) < λ/n_2 (550/2.0 = 275).

Table A				
λ (nm)	**n_1 (Silicon)**	**n_2 (Porphyrin)**	**λ/n_1(nm)**	**λ/n_2 (nm)**
400	5.8	1.7	68	235
550	4.5	2.0	123	275
700	3.8	1.6	186	438
750	3.7	1.8	203	417

Similarly, Table B shows the calculated values of λ/n_1 and λ/n_2 for *Kuboi*'s red pixels with phthalocyanine. *Kuboi*'s 250 nm hole pitch falls in the range λ/n_1 to λ/n_2 for at least part of the visible light spectrum (400-700 nm wavelengths) and at least part of the near infrared light spectrum (>700 nm wavelengths). Lebby, ¶197. For example, for the 650 nm red light wavelength, λ/n_1 (650/3.9 = 168) < Λ (250 nm) < λ/n_2 (650/2.1 = 302).

Table B				
λ (nm)	**n_1 (Silicon)**	**n_2 (Phthalocyanine)**	**λ/n_1(nm)**	**λ/n_2 (nm)**
400	5.8	1.9	68	211
650	3.9	2.1	168	302
700	3.8	1.8	186	389
750	3.7	2.3	203	326

Thus, the stated period of *Kuboi*'s pillar hole array falls within the range λ/n_1 to λ/n_2 for selected visible and infrared wavelength ranges of the light. Lebby, ¶198.

As a result, based on Patent Owner's representations, *Kuboi*'s pillar-hole array forms an HCG. Lebby, ¶¶188-199. And, under those same representations, such an HCG would produce an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient based on the near-wavelength and deep-wavelength phenomena. Lebby, ¶199. Thus, consistent with Patent Owner's representations, a POSITA would have understood that the absorption of light, at selected visible and infrared wavelength ranges, by at least some of *Kuboi*'s photodetectors with holes would be at least 1.1 times that of like photodetectors lacking said holes. *Id.*

Patent Owner's representations were also consistent with those of other prior art teachings. Lebby, ¶¶200-201. For example, *Han* (Ex-1038) is consistent with

Patent Owner's representations as to the impact of nanoholes on the ultimate efficiency associated with photon absorption before the '948 Patent priority date. *Han*, 7:19-8:5. According to *Han*, the ultimate efficiency for a device having a semiconductor thickness of about 1.4 μm without nanoholes is approximately 0.12, whereas the ultimate efficiency for a similar device having nanoholes is approximately 0.22. *Han*, Fig. 4; Lebby, ¶¶200-201.

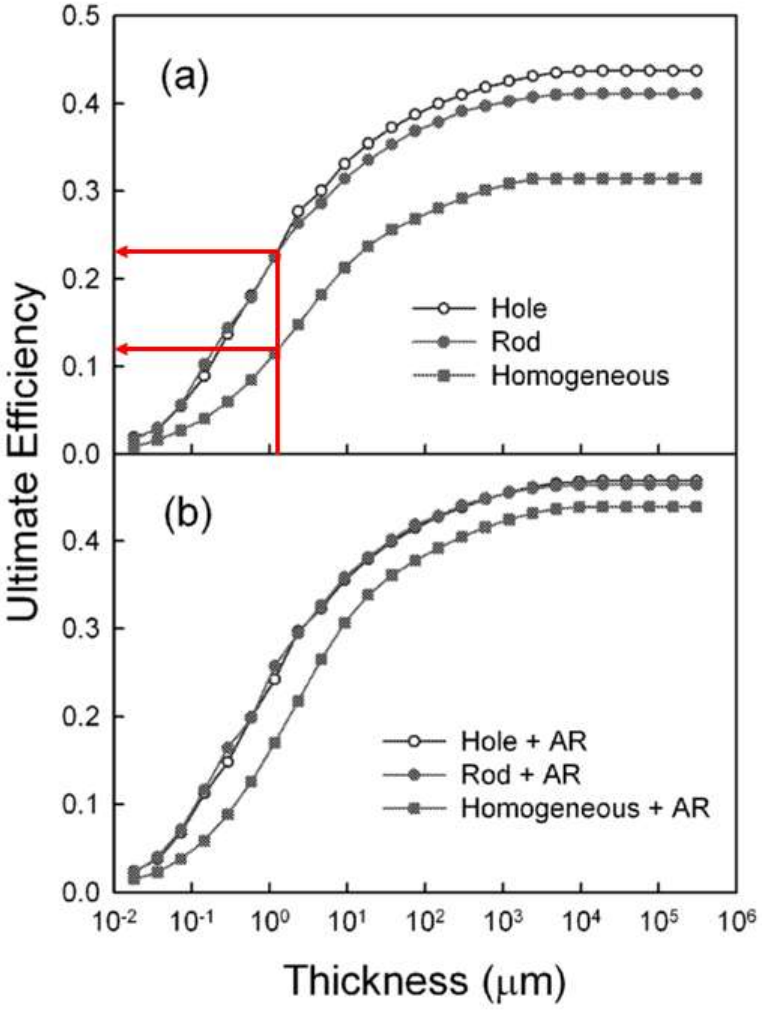


FIG. 4

Han, Fig. 4.

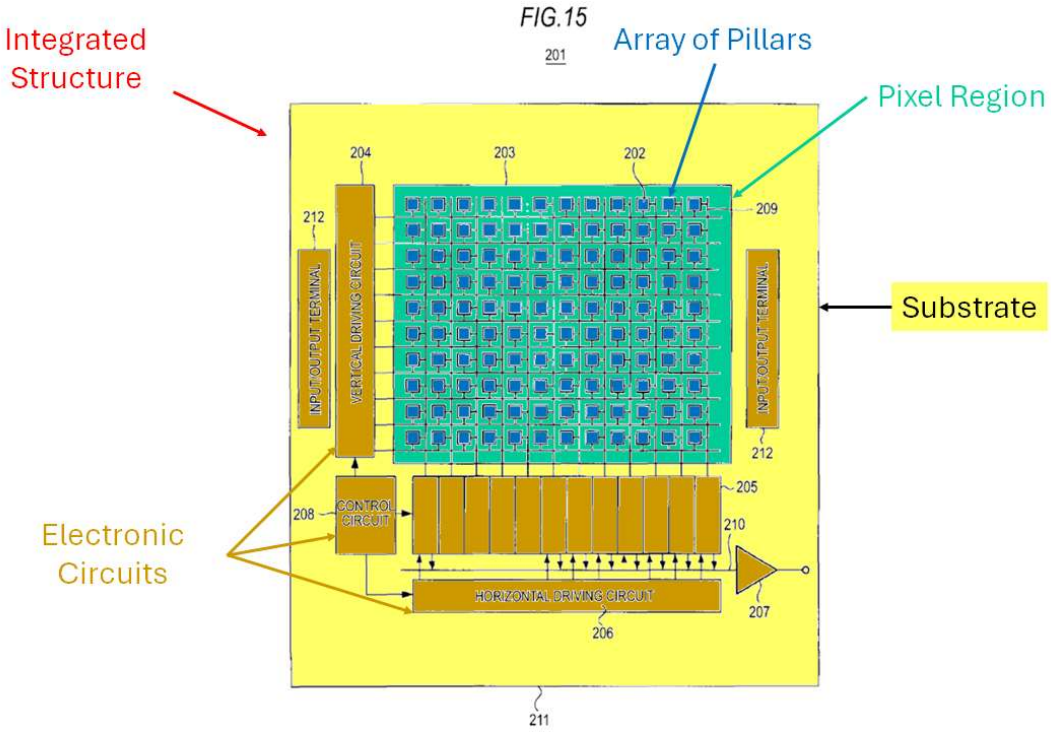
Thus, based on *Han*, a POSITA would have understood that *Kuboi*'s 1.4 μm hole depth would increase light absorption by a factor of 1.8 (0.22/0.12 = 1.8), which is significantly higher than 1.1. Lebby, ¶¶200-201; *Han*, Fig. 4. Accordingly, based on a POSITA's understanding of the state of the art before the '948 Patent's priority date, a POSITA would have understood that *Kuboi*'s 1.4 μm hole depth would have increased the absorption of light, at selected visible and infrared wavelength ranges, in at least some of *Kuboi*'s photodetectors by at least 1.1 times that of like photodetectors lacking said holes, and even if not readily understood, a POSITA would have found such a result not only obvious but also one having a reasonable expectation of success in achieving this increase because *Kuboi* discloses forming nanoholes of 1.4 μm depth. Lebby, ¶201.

4. Claim 2

a. "The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices."

Kuboi discloses this additional limitation. Lebby, ¶¶202-206. *Kuboi* discloses "a simplified exemplary configuration of a CMOS solid-state imaging device." *Kuboi*, ¶[48]. *Kuboi*'s imaging device 201 "include[s] a pixel region (so-called … imaging region) 203 and a peripheral circuit portion which are provided on a semiconductor substrate 211 (i.e., a silicon substrate)." *Id. Kuboi*'s "pixel [region] and logical circuit portion may be created in advance." *Kuboi*, ¶[78].

Thus, *Kuboi* teaches that the pixel region (i.e., array of pillars) is monolithically integrated with the logical circuit portion (including circuits 204-208). *Kuboi*, ¶¶[48]-[49]. A POSITA would have understood that circuits 204-208 include electronic devices. Lebby, ¶203 (citing Ex-1011, 3). This integrated structure is shown below:



Kuboi, Fig. 15.

Kuboi's disclosure, including Figure 15 and its method of fabrication, show that the pixels and the logical circuit portion are formed on a single substrate, substrate 211. *Kuboi*, ¶¶[70]-[78], [48]-[49]; Lebby, ¶¶204-206. A POSITA would have understood that because the logical circuit portion is formed on a silicon substrate, the logical circuit portion's electronic devices are Si electronic devices.

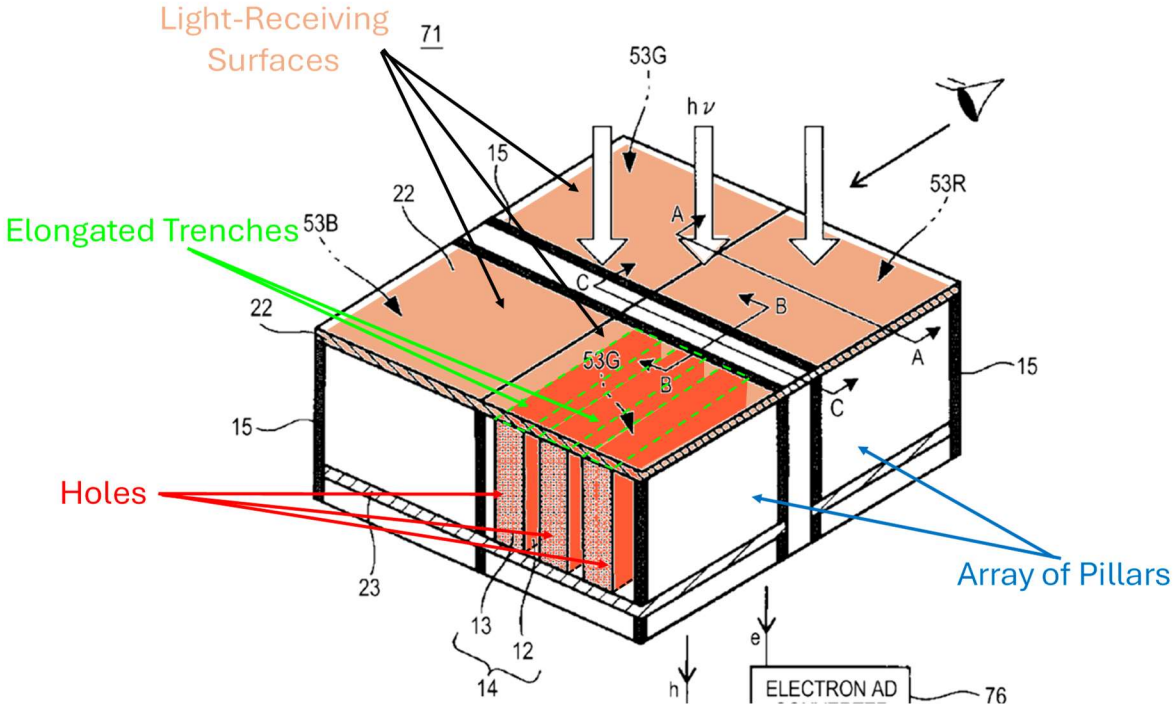
Lebby, ¶205 (citing Ex-1011, 3). And because the pixel region (including an array of pillars) and logical circuits (electronic devices) are formed in or on the same silicon substrate, *Kuboi* discloses monolithically integrating the array of pillars (pixel region) with Si electronic devices. *Id.*

5. Claim 3

a. "The integrated structure of claim 1, wherein each of at least some of the pillars has a plurality of the elongated holes."

Kuboi discloses this additional limitation. Lebby, ¶¶207-208. As explained above for claim [1c] and [1d], in *Kuboi*'s imaging device, each of pixels 53R and 53G have multiple holes 38 that are elongated (i.e., trenches) along the light-receiving surface of that pixel. VI.A.3.e, VI.A.3.f.

FIG.13



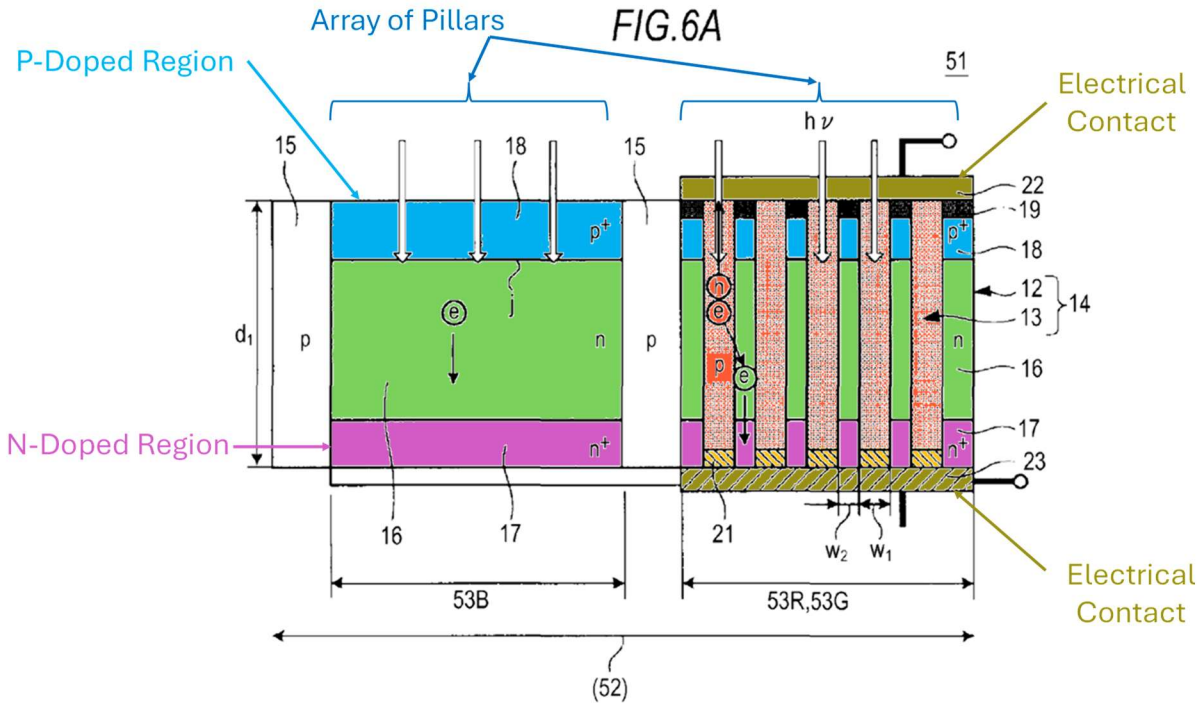
Kuboi, Fig. 13.

6. Claim 7

a. "The integrated structure of claim 1, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors."

Kuboi discloses this additional limitation. Lebby, ¶¶209-215. *Kuboi*'s electrodes 22 and 23 are "electrical contacts." VI.A.3.i (claim [1g]). In *Kuboi*, a "necessary voltage" is applied between upper and lower electrodes 22, 23 so that p^+-type region 18 is at a negative potential and n^+-type region 17 is at a positive potential. *Kuboi*, ¶[64]; Lebby, ¶210. As illustrated below, because electrodes 22 and 23 are positioned on opposite sides of photoelectric conversion portions 14

(photodetectors) of pixels (53G, 53R), the voltage applied between electrodes 22, 23 provides an electric field across those photodetectors. VI.A.3.i (claim [1g]); Lebby, ¶¶210-211.

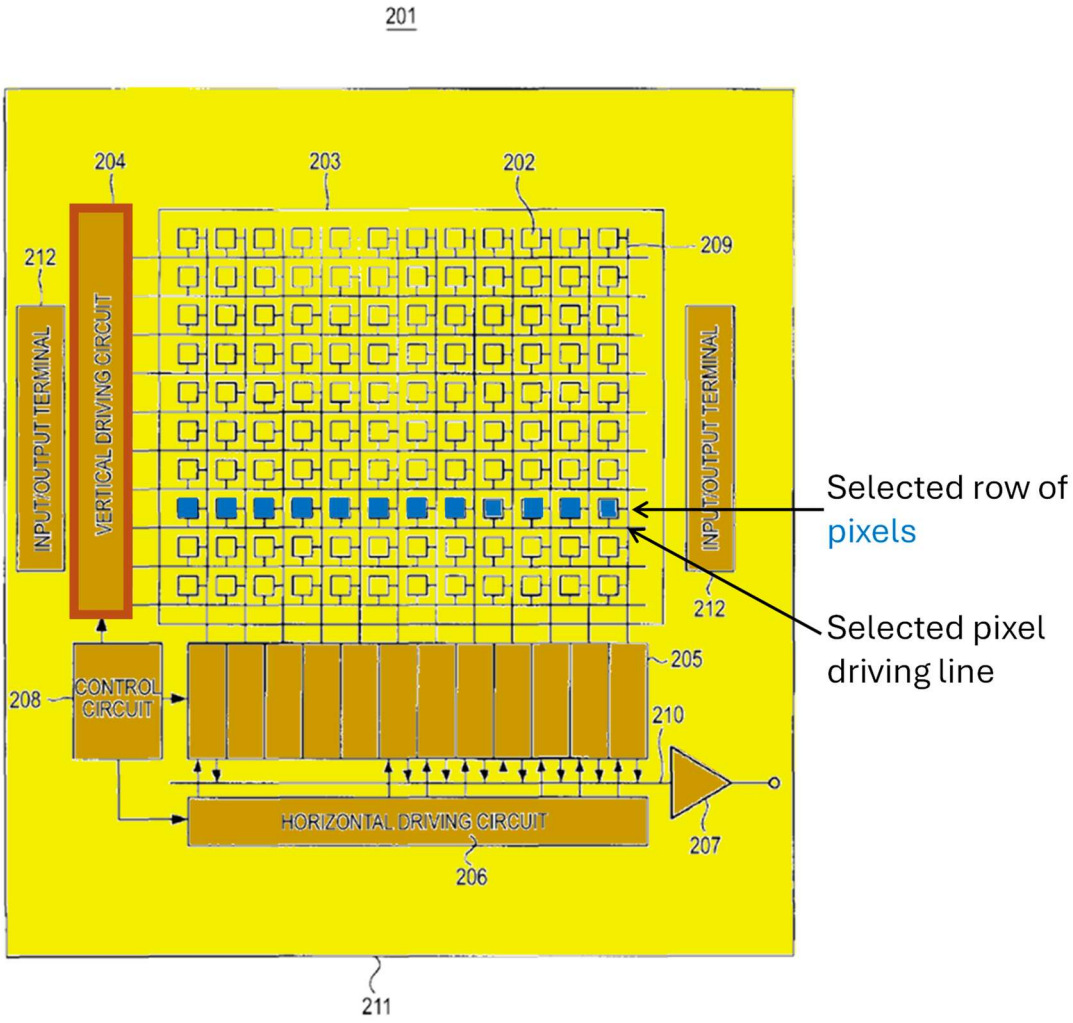


Kuboi, Fig. 6A. As explained in [1g], in *Kuboi*, the "necessary voltage" applied for reverse biasing is selected based on operating conditions. VI.A.3.i. A POSITA would have understood that varying the bias voltage alters the strength of the electric field generated within the device. Lebby, ¶211. For instance, higher reverse bias intensifies the electric field, while lower bias weakens it. Ex-1032, 1 ("[t]he electric field is proportional to the applied bias in devices"), 4-6, 10. Thus, by

applying a "necessary voltage" for biasing, electrodes 22 and 23 are arranged to selectively provide electric fields across at least some of the photodetectors.

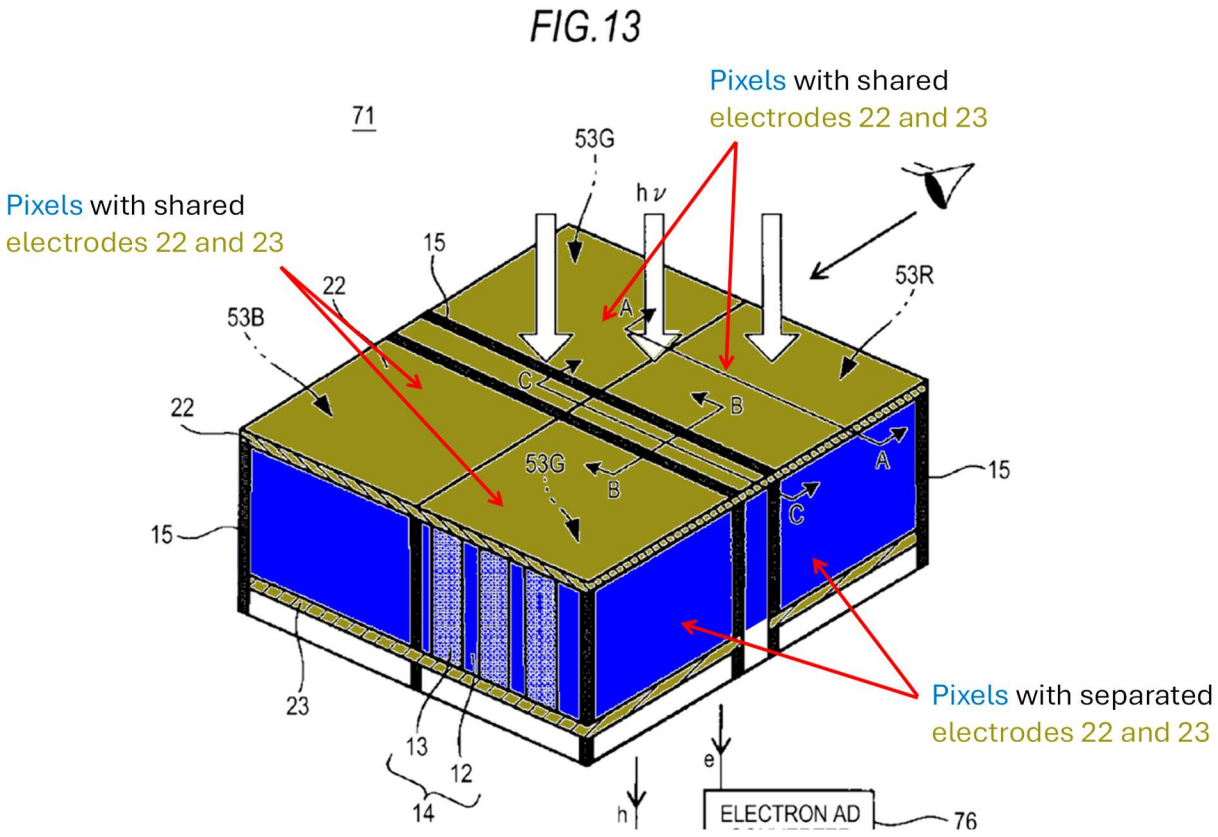
Moreover, in *Kuboi*, vertical driving circuit 204 activates a selected row of pixels by selectively applying voltage pulses to the upper and lower electrodes 22, 23 of pixels 202 in the selected row through the "selected pixel driving line," thereby establishing a reverse bias and generating an electric field across just those pixels. Lebby, ¶¶212-215; *Kuboi*, ¶¶[51], [64]; *see* Ex-1055, ¶[78].

FIG.15



Kuboi, Fig. 15.

To enable this selective application of voltage pulses to only the pixels in a selected row, *Kuboi* illustrates a pair of adjacent pixels (53B and 53G in the figure below) as sharing their upper and lower electrodes 22 and 23 and separated from the electrodes 22 and 23 of an adjacent pair of pixels (53G and 53R in the figure below). Lebby, ¶214.



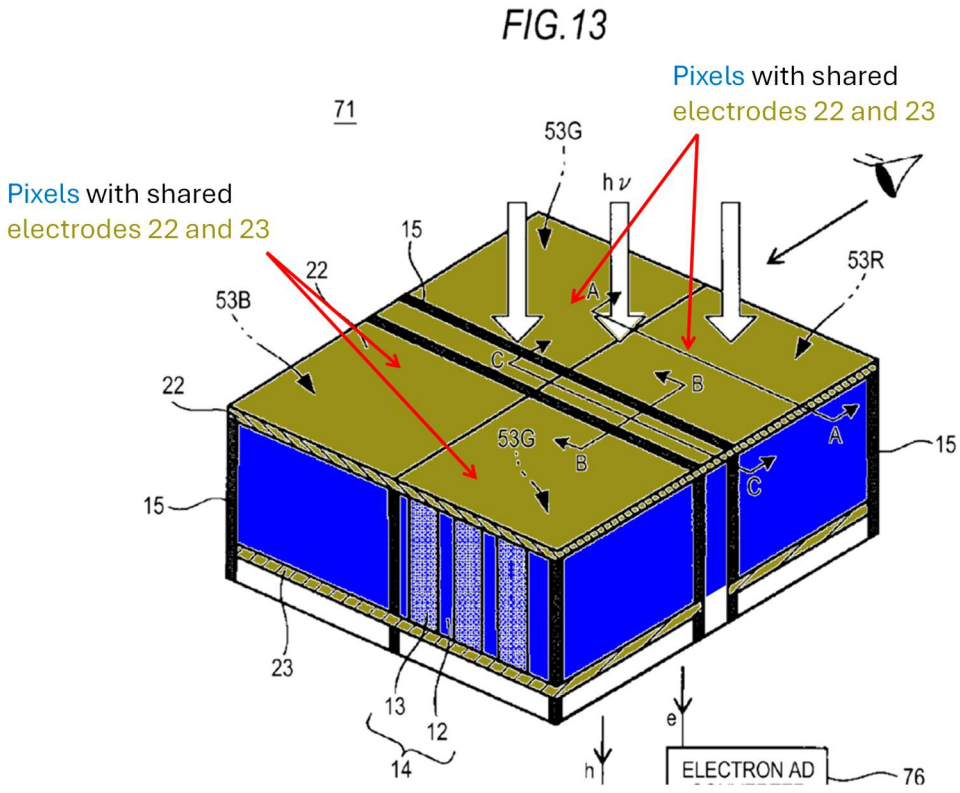
Kuboi, Fig. 13 (cropped). A POSITA would have understood that because *Kuboi* allows selective reverse biasing of pixels in a selected row, electrodes 22 and 23 (electrical contacts) are configured to selectively provide electrical fields across the photoelectric conversion portions of the selected row of pixels. Lebby, ¶215.

7. Claim 8

a. "The integrated structure of claim 1, in which two or more of the photodetectors share one of the electrical contacts."

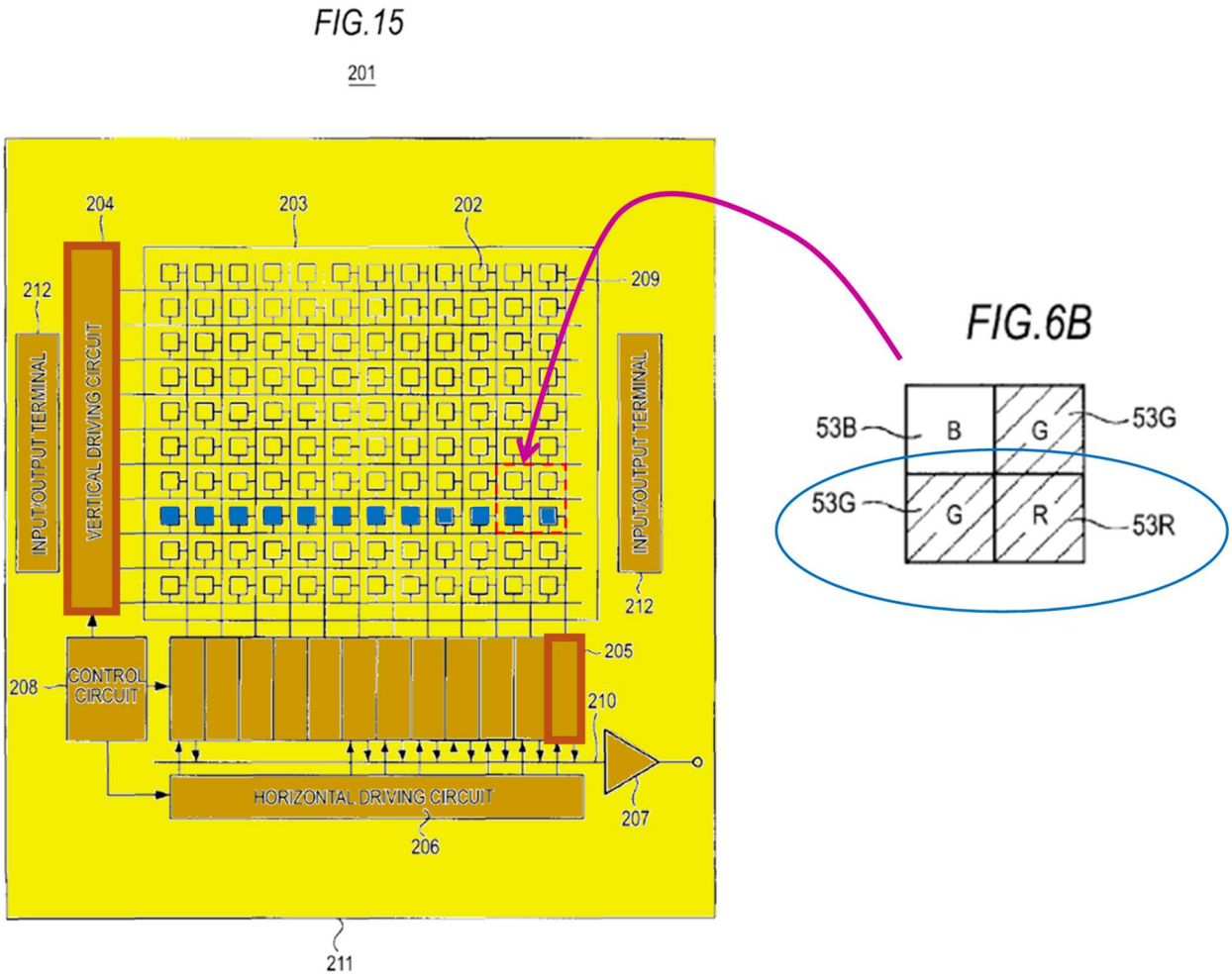
Kuboi discloses this additional limitation. Lebby, ¶¶216-219. *Kuboi*'s electrodes 22 and 23 are "electrical contacts." VI.A.3.i (claim [1g]). As explained for claim 7, *Kuboi* illustrates a pair of adjacent pixels 53B and 53G sharing their

upper electrodes 22 and lower electrodes 23, and another pair of adjacent pixels 53G and 53R as sharing their electrodes 22, 23. VI.A.6.a.



Kuboi, Fig. 13 (cropped).

Moreover, as explained for claim 7 (VI.A.6.a), vertical driving circuit 204 activates a selected row of pixels by simultaneously applying voltage pulses to the upper and lower electrodes 22 and 23 of all the pixels 202 in the selected row. Lebby, ¶218; *Kuboi*, ¶¶[51], [64].

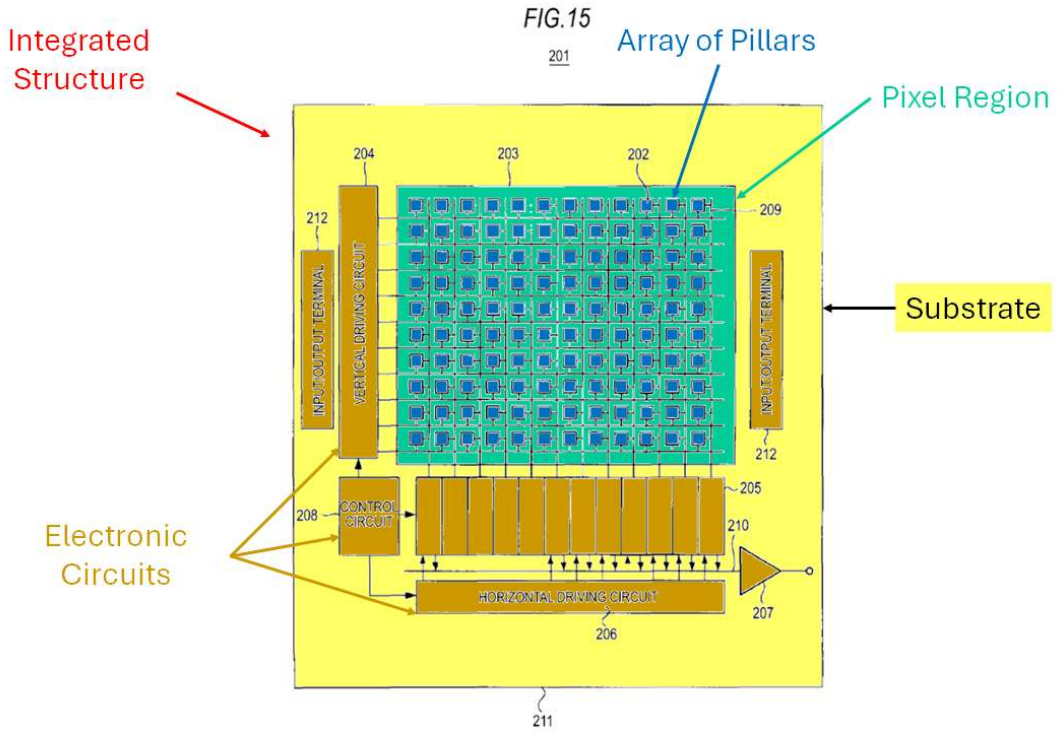


Kuboi, Figs. 15, 6B. A POSITA would have understood that, when the group of pixels of Figures 6A-6B are incorporated into imaging device 201 (as illustrated above), all pixels 202 in the selected row—including pixels 53G and 53R circled in Figure 6B above—would share common upper electrodes 22 and lower electrodes 23. *See* VI.A.1. This shared configuration enables vertical driving circuit 204 to apply a voltage bias simultaneously across the selected row of pixels. Lebby, ¶219; *Kuboi*, ¶[51].

8. Claim 9

a. "The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission."

Kuboi discloses this additional limitation. Lebby, ¶¶220-223. As explained for claim 2 (VI.A.4.a), *Kuboi*'s pixel region 203 (i.e., array of pillars) is monolithically integrated with the peripheral circuit portion (including logical circuits 204-208 with Si electronic devices) on silicon substrate 211. *Kuboi*, ¶¶[48]-[49]; Lebby, ¶220.



Kuboi, Fig. 15. Within the peripheral circuit portion, column signal processing circuits 205 "perform signal processing such as noise removal" on the signals received from pixels 202. *Kuboi*, ¶[52]. The resulting signals are then forwarded to

output circuit 207, which performs additional signal processing "and outputs the processed signals." *Kuboi*, ¶¶[49], [53]-[54]. Thus, in *Kuboi*, the array of pixels is monolithically integrated with Si electronic devices for signal processing and transmission. Lebby, ¶¶221-223.

9. Claim 10

a. "The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors."

Kuboi discloses this additional limitation. Lebby, ¶¶224-226. As explained for claim 9 (VI.A.8.a), *Kuboi*'s array of pixels is monolithically integrated with Si electronic devices for signal processing and transmission. *Kuboi*, ¶¶[48]-[54]. The processed signals output by output circuit 207 are processed electrical signals related to the accumulations of charge carriers in the photoelectric conversion portions (photodetectors) of the pixels. VI.A.3.d; Lebby, ¶224.

For instance, incident light enters the photoelectric conversion films 13 within the photoelectric conversion portion (photodetector) of a pixel, where it undergoes photoelectric conversion to generate electron-hole pairs (charge carriers). *Kuboi*, ¶[64]; Lebby, ¶225. The electrons (e) from these pairs, which function as signal charges, accumulate in a charge accumulation region of the pixel. *Kuboi*, ¶[64]. Vertical driving circuit 204 then transfers the accumulated

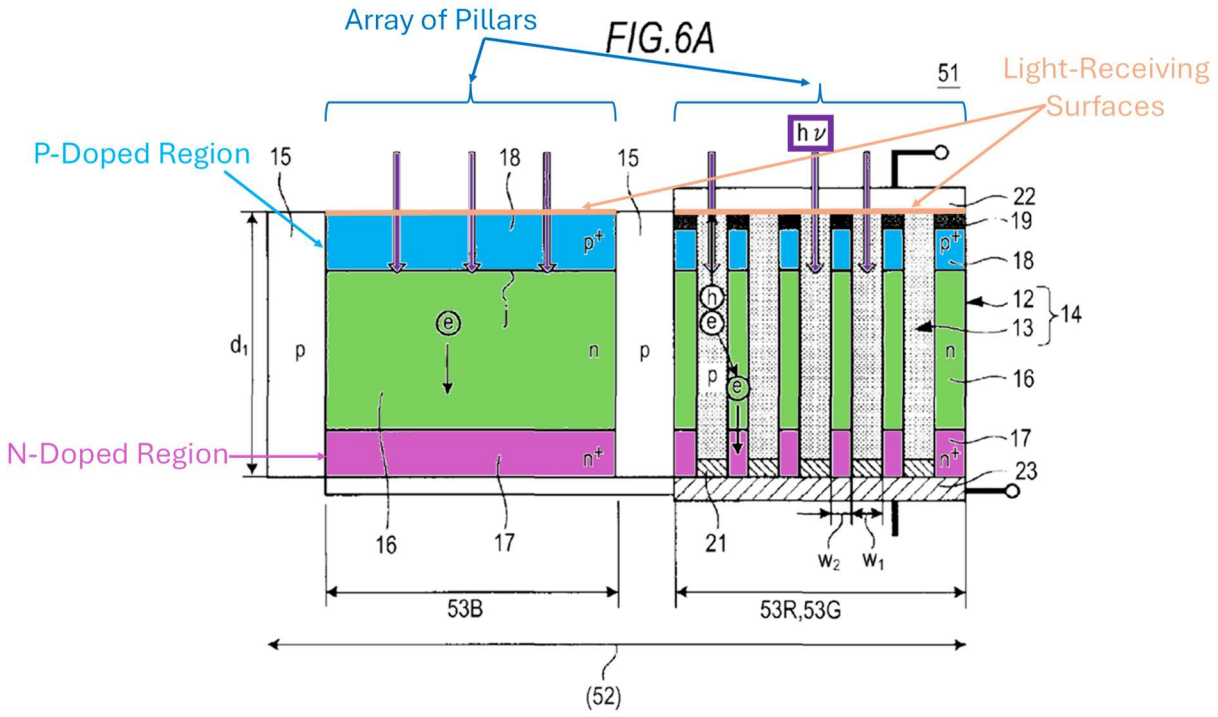
pixel signal to the corresponding column signal processing circuit 205, which performs noise reduction on the received signal. *Kuboi*, ¶¶[51]-[52]; VI.A.8.a (claim 9). The processed signal is subsequently sent to output circuit 207 for further processing and final output. *Kuboi*, ¶¶[53]-[54].

Circuits 204, 205, and 207 are logic circuits of the peripheral circuit portion that are monolithically integrated with the array of pixels on a single substrate 211. VI.A.4.a (claim 2); *Kuboi*, ¶¶[48]-[49]. Thus, in *Kuboi*, the array of pixels (pixel region 203) is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in the photoelectric conversion portions of at least some of the pixels.

10. Claim 11

a. "The integrated structure of claim 1, in which each of at least some of the photodetectors is configured such that the light passes through at least a part of the one of the P-doped region and N-doped region of the photodetector before reaching any part of the other doped region of the photodetector."

Kuboi discloses this additional limitation. Lebby, ¶¶227-233. As explained for claim [1b], in *Kuboi*'s semiconductor layer 12, p^+-type region 18 is the "P-doped" region, and n^+-type region 17 is the "N doped" region. VI.A.3.d; *Kuboi*, ¶¶[55]-[56].

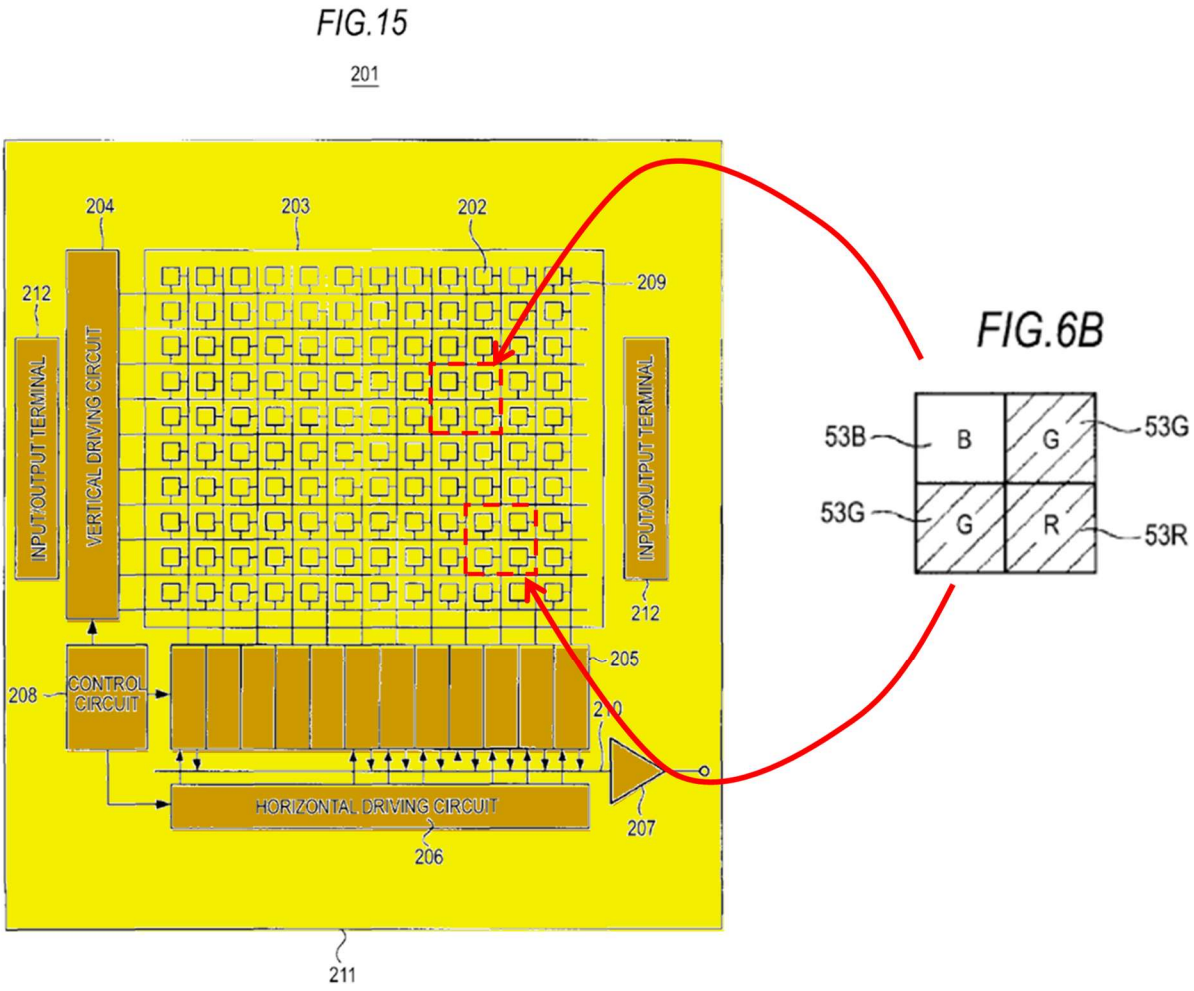


Kuboi, Fig. 6A. *Kuboi* discloses that p⁺-type region 18 ("P-doped region") is formed on the side of semiconductor layer 12 where light enters and n+-type region 17 ("N doped region") is formed on the side of semiconductor layer 12 where light does not enter. *Kuboi*, ¶[56]. *Kuboi*'s Figure 6A reproduced above shows light (hν) entering semiconductor layer 12 of the blue pixel 53B through p⁺-type region 18. Lebby, ¶229; *Kuboi*, Fig. 6A.

Accordingly, a POSITA would have recognized that the photoelectric conversion portion (photodetector) of blue pixel 53B is configured such that light passes first through at least a part of the p⁺-type region 18 ("P-doped region")—which is "one of" the p⁺-type region 18 and n+-type region 17—of the photodetector before reaching any part of n-type region 16. Lebby, ¶230.

If the term "other doped region" is construed as the name of a distinct region of the photodetector, then *Kuboi*'s n-type region 16 corresponds to the claimed "other doped region." Lebby, ¶231. Alternatively, if "other" in the phrase "other doped region" is construed in a relational sense—that is, to refer to the second of two previously mentioned regions (either the P-doped region or N-doped region)—then, *Kuboi*'s n^+-type region 17 is the claimed "other doped region." *Id*.

A POSITA would have understood that the phrase "at least some of" encompasses a single occurrence, but even if interpreted to require multiples, *Kuboi* discloses that Figure 15's imaging device 201 is applicable to all disclosed pixel configurations. *Kuboi*, ¶¶[34], [48]; VI.A.1. Accordingly, a POSITA would have understood that the two-dimensional array of pixels 53B, 53G, and 53R, *see Kuboi*, ¶¶[90]-[94], will be implemented within imaging device 201 as illustrated below. Lebby, ¶232.



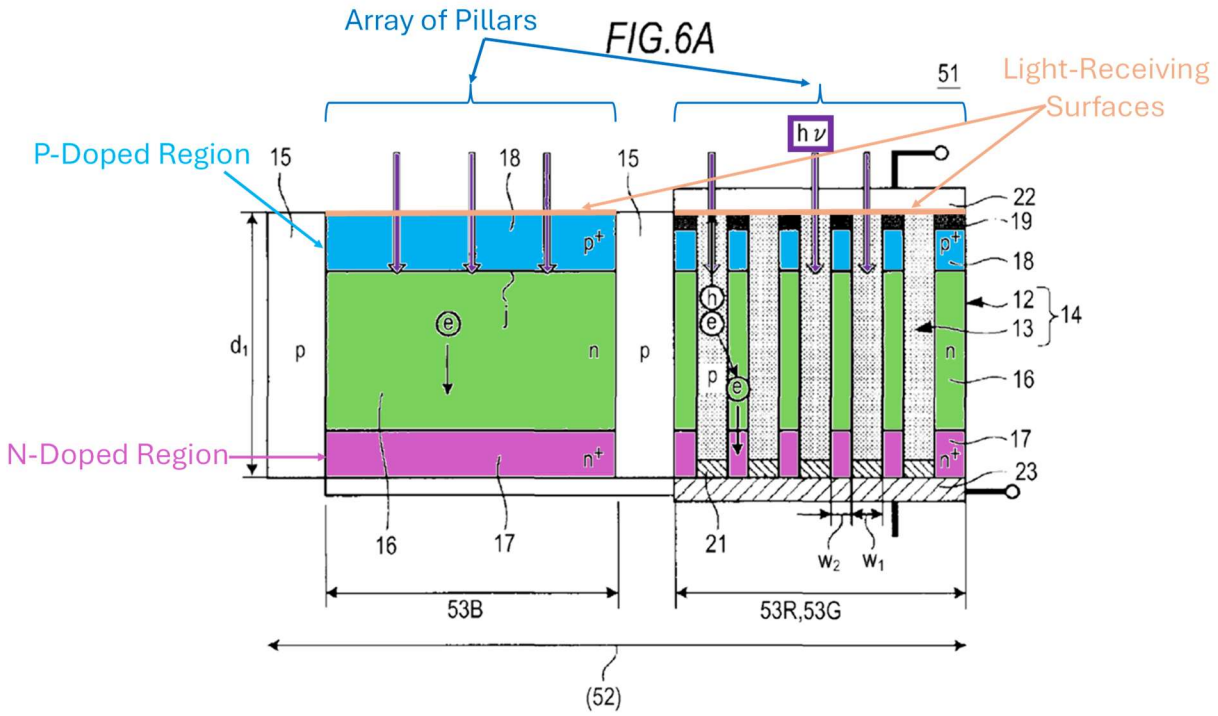
Kuboi, Figs. 15, 6B. Thus, a POSITA would have recognized that *Kuboi*'s imaging device includes multiple blue pixels 53B. Lebby, ¶233.

11. Claim 12

a. "The integrated structure of claim 1, in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the P-doped region before reaching any part of the N-doped region."

Kuboi discloses this additional limitation. Lebby, ¶¶234-237. As explained for claims [1b] and 11, in *Kuboi*'s semiconductor layer 12, p^+-type region 18 is the

"P-doped" region, and n^+-type region 17 is the "N doped" region, with p^+-type region 18 formed on the side where light enters and n+-type region 17 formed where light does not enter. VI.A.3.d, VI.A.10.a; *Kuboi*, ¶[56].



Kuboi, Fig. 6A. In *Kuboi*, p^+-type region 18 and n^+-type region 17 are positioned on opposing sides of n-type region 16. Lebby, ¶236; *see Kuboi*, ¶¶[56], [71]. A POSITA would have understood that the photoelectric conversion portion (photodetector) of blue pixel 53B includes a doped region configured such that incident light (hν) first traverses p^+-type region 18 (P-doped region) before reaching any portion of n^+-type region 17 (N-doped region). Lebby, ¶236. And as

explained, a POSITA would have recognized that *Kuboi*'s imaging device includes multiple blue pixels 53B. VI.A.10; Lebby, ¶237.

B. Ground 2: Claims 4-6 and 13-16 Are Obvious Over *Kuboi* in View of *Vasylyev*

1. Overview of *Vasylyev*

Vasylyev discloses a light harvesting system for "light detectors having light trapping microstructures … to improve absorption of light within the light sensitive layer." *Vasylyev*, ¶¶[6], [9], [16].

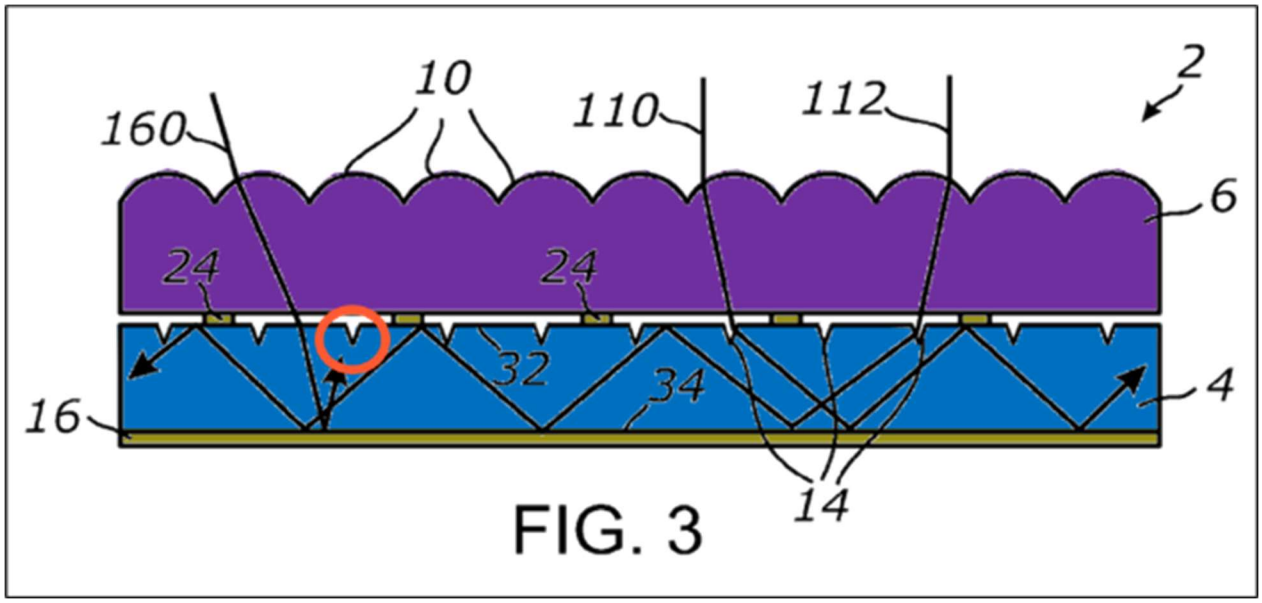


FIG. 3

Vasylyev, Fig. 3. In light harvesting system 2, a focusing array composed of microlenses 10 is disposed above a photo-responsive photovoltaic layer 4 to concentrate light onto layer 4. *Vasylyev*, ¶¶[65]-[67]. Photovoltaic layer 4 may incorporate any suitable structure capable of absorbing incident light and generating electrical charge carriers, and it may further include ohmic metallic or

non-metallic electrodes—such as front electrodes 24 and back electrodes 16. *Vasylyev*, ¶¶[75], [80]. *Vasylyev*'s photovoltaic layer 4 may be formed of crystalline silicon and configured with a PiN architecture, wherein an intrinsic (i-type or undoped) layer is positioned between a p-type layer and an n-type layer. *Vasylyev*, ¶¶[76]-[77]; Lebby, ¶¶86-100.

Layer 4 further includes light input ports 14 formed in its front surface 32 that receive light from microlens 10. *Vasylyev*, ¶[83].

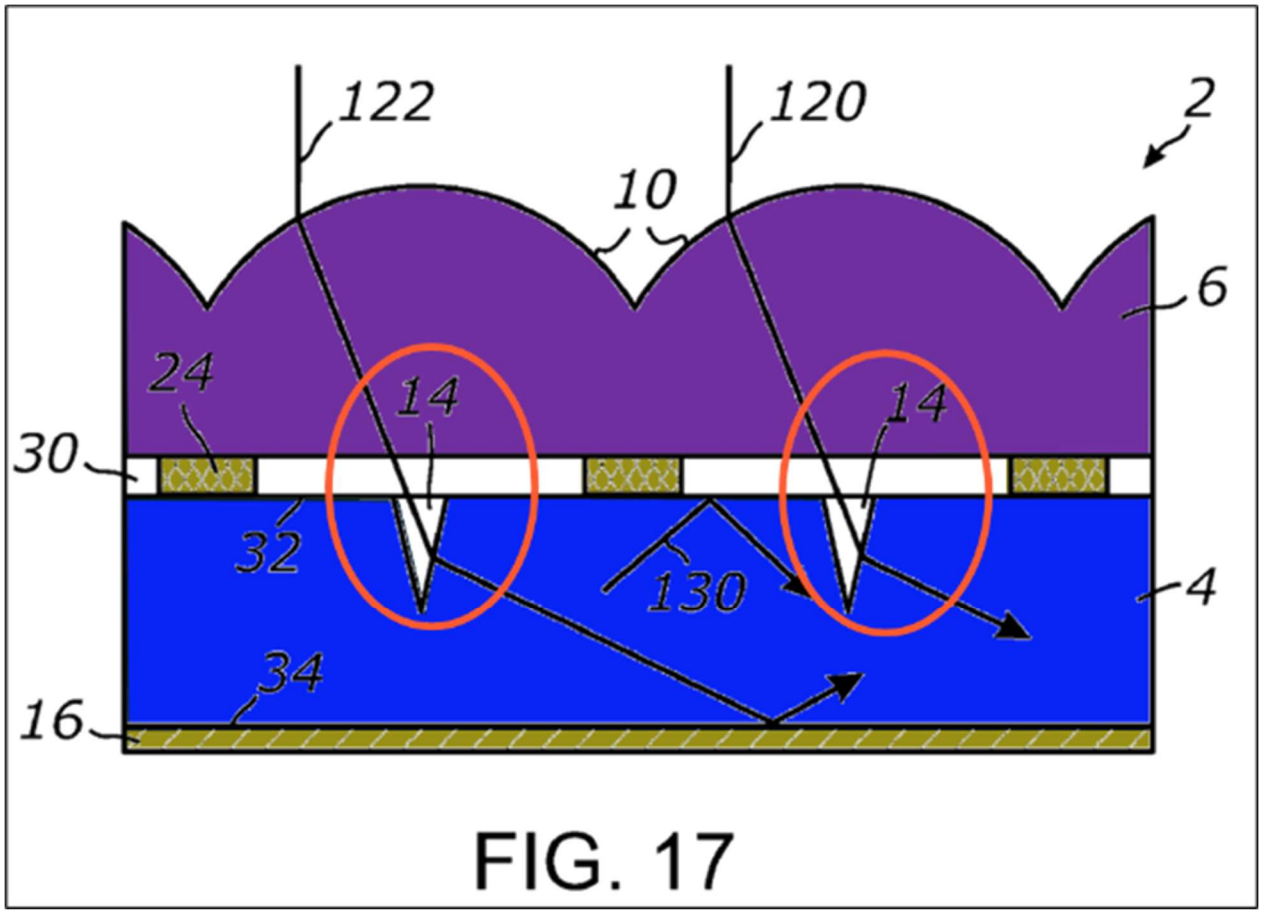


FIG. 17

Vasylyev, Fig. 17. The number of light input ports 14 is equal to the number of lenses 10 positioned above photovoltaic layer 4. *Vasylyev*, ¶[84]. Ports 14 are

spatially arranged on the light-receiving surface 32 of layer 4 such that there is a "pairwise optical relationship," or a one-to-one optical coupling, between each lens 10 and its associated port 14. *Id.* The receiving aperture of each port 14 is centered with respect to the optical axis of the associated lens 10. *Vasylyev*, ¶[85]. Accordingly, in *Vasylyev*'s system 2, a single port 14 is positioned beneath each lens 10. Lebby, ¶¶90-95.

Vasylyev explains that positioning a single port 14 beneath each lens 10 minimizes light reflection at the light-receiving surface 32 while enhancing light coupling and light-trapping efficiency. *Vasylyev*, ¶¶[10]-[14], [63]-[64], [93]-[94]. *Vasylyev* explains that crystalline silicon—a conventional photovoltaic material—exhibits a relatively high refractive index, which contributes to poor light coupling efficiency due to significant reflection losses at the light-receiving surface. *See Vasylyev*, ¶[12]. For instance, at a wavelength of 400 nm, crystalline silicon has a refractive index of 5.59, resulting in a Fresnel reflection of approximately 49% of the incident light. *Id*. *Vasylyev* discloses that conventional techniques for mitigating surface reflection—such as antireflection coatings and surface microstructuring—suffer from various limitations. *See id*. For example, the formation of a microstructure array on the light-receiving surface 32, as illustrated below, can result in a significant portion of incident light escaping photovoltaic layer 4 without being absorbed. *Vasylyev*, ¶¶[63]-[64].

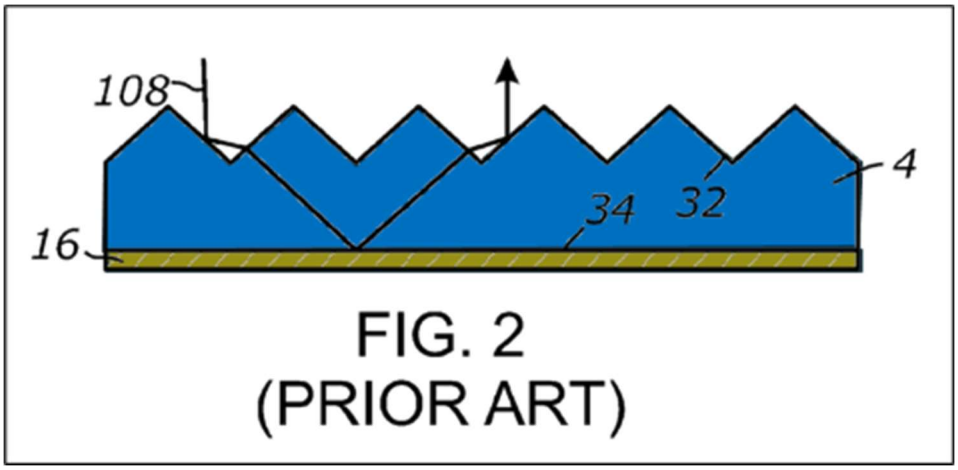


FIG. 2
(PRIOR ART)

Vasylyev, Fig. 2. According to *Vasylyev*, although the above microstructure array enhances light coupling compared to a flat surface lacking microstructures, a light ray 108 entering photovoltaic layer 4 and reflecting from the back contact 16 may still escape the layer upon its next encounter with the front surface 32, resulting in poor light-trapping efficiency. *Vasylyev*, ¶[64].

To address this problem with the prior art, *Vasylyev* teaches positioning a single port 14 on surface 32 beneath each lens 10 to enhance both light coupling and light-trapping effectiveness. *Vasylyev*, ¶¶[93]-[94].

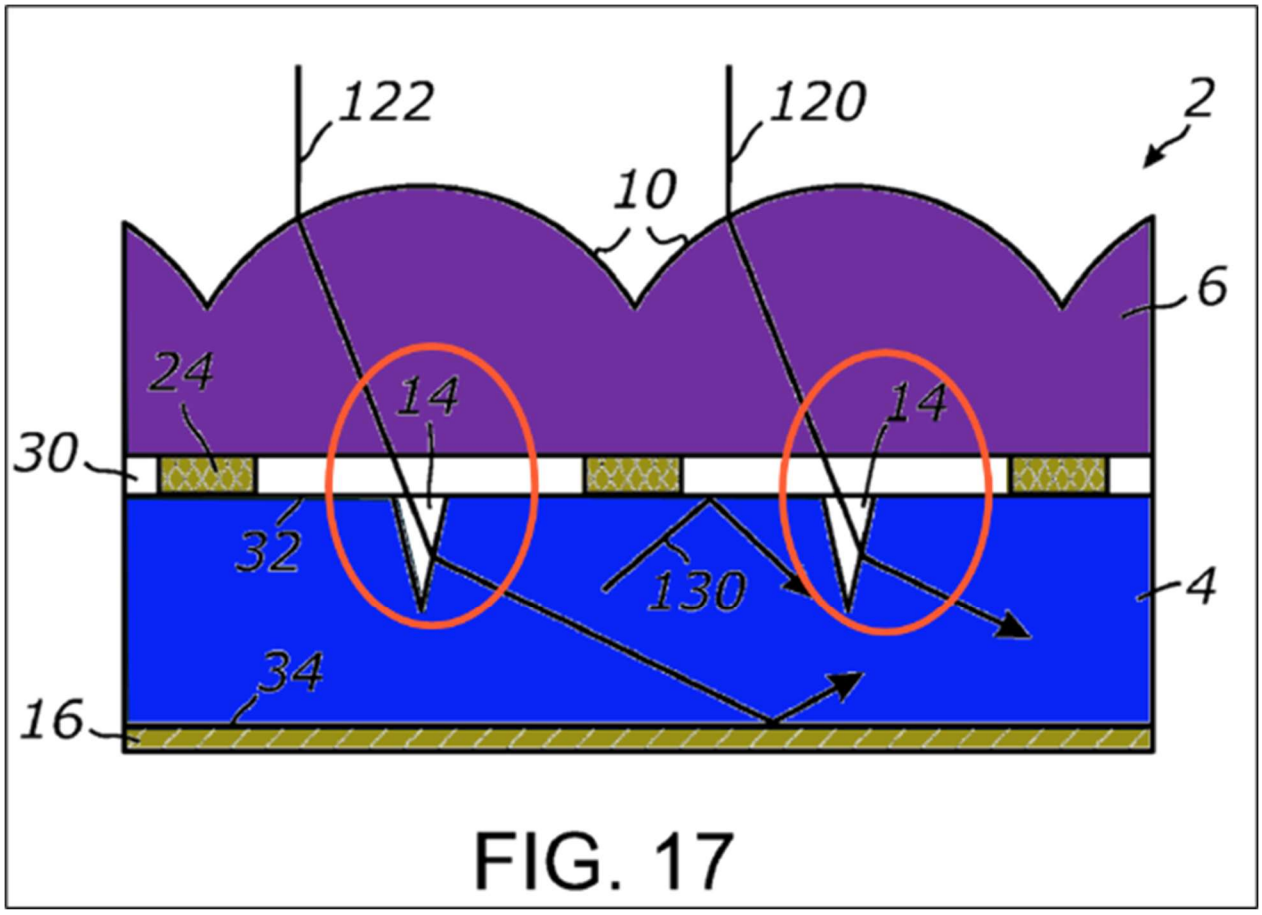


FIG. 17

Vasylyev, Fig. 17. For example, light ray 120 passing through lens 10 is directed onto corresponding port 14, where it undergoes refraction to enter photovoltaic layer 4 at an oblique angle, thereby enhancing light coupling efficiency. *Vasylyev*, ¶¶[93]-[94], [97]; Lebby, ¶94. Light introduced into photovoltaic layer 4 at an oblique angle becomes confined between its parallel surfaces, thereby extending the optical path length and resulting light absorption in layer 4, as illustrated by the trajectories of light rays 110 and 112 below. *Vasylyev*, ¶¶[64], [93].

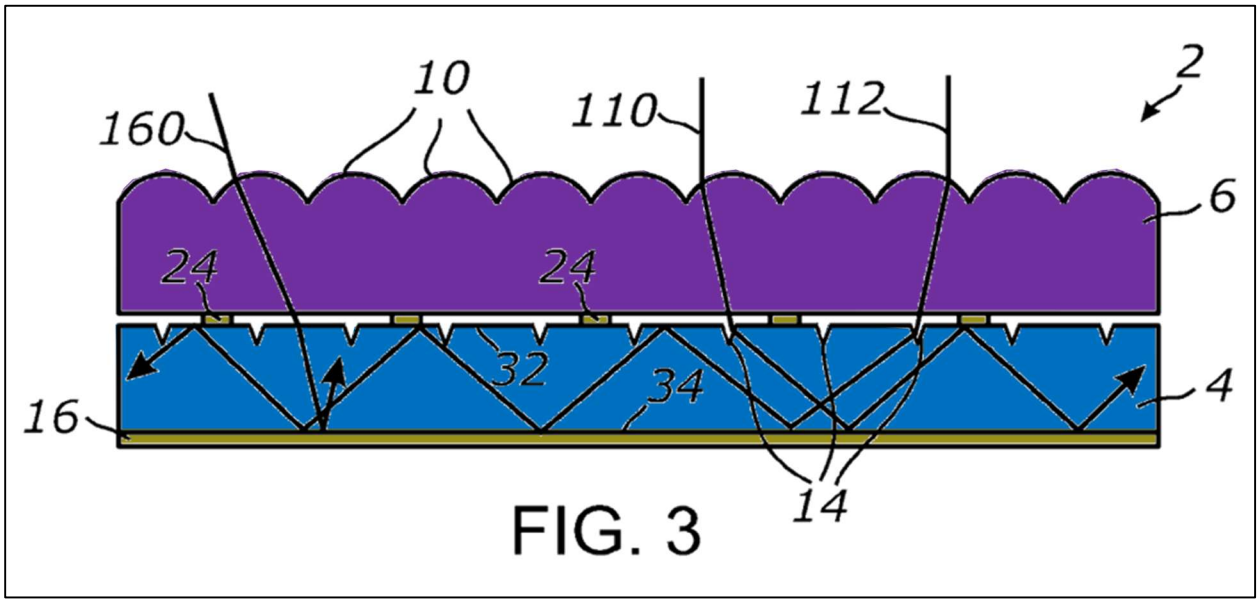
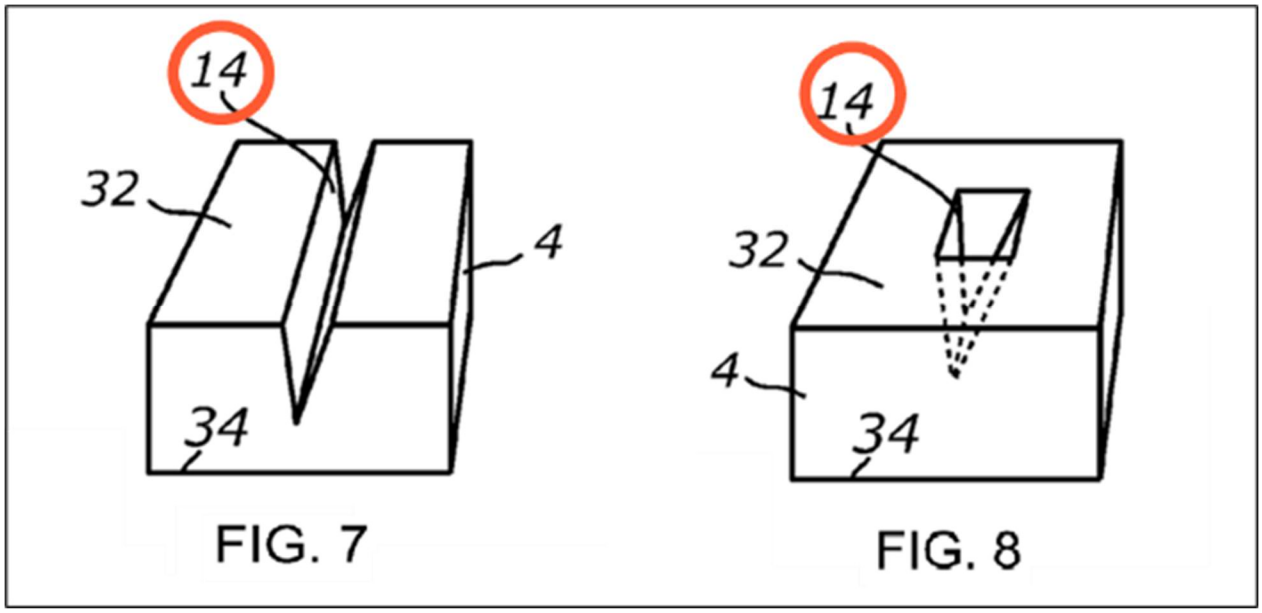


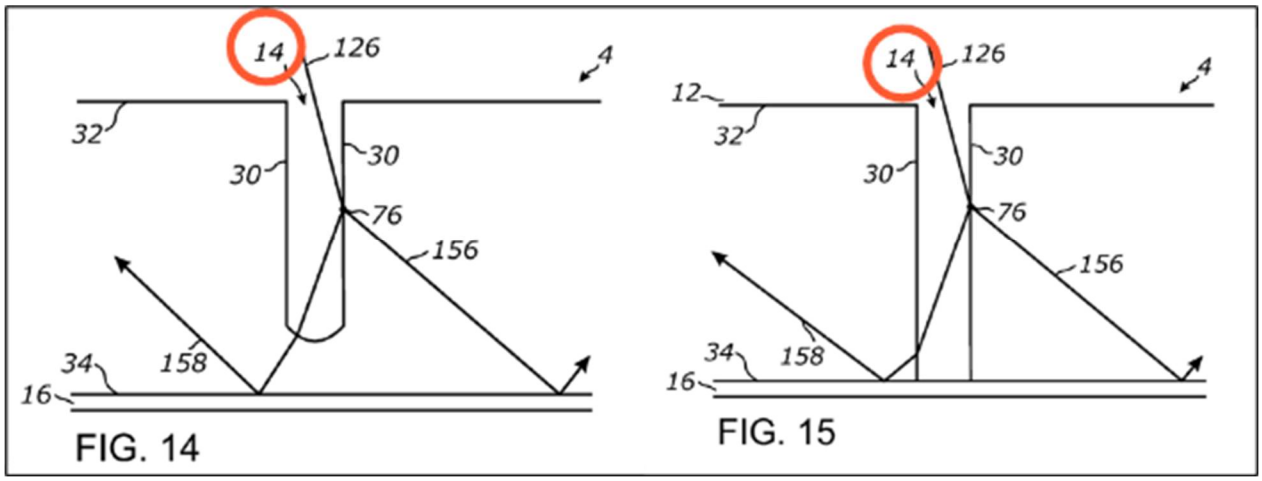
FIG. 3

Vasylyev, Fig. 3. Accordingly, placing a single port 14 on the light-receiving surface 32 beneath each lens 10 enhances light coupling efficiency and facilitates the confinement of incident light within the silicon photosensitive layer, thereby extending the optical path length and improving both light absorption and energy conversion efficiency. *Vasylyev*, ¶[14]; Lebby, ¶95.

Vasylyev discloses that port 14 may be any suitable microstructure, including "recesses, holes, [or] cavities" and may be fabricated on surface 32 using "chemical etching, ion beam etching, reactive ion etching, plasma etching or any other known method." *Vasylyev*, ¶[83]. Port 14 can have various shapes and profiles. *Id*.



Vasylyev, Figs. 7-8. For example, port 14 may have an "elongated shape" on surface 32 and "can extend all the way along surface 32 or its substantial portion." *Vasylyev*, ¶[89]. Port 14 may also be configured as a relatively deep cavity formed in surface 32, with the cavity walls oriented either perpendicularly or at an inclined angle relative to surface 32. *Vasylyev*, ¶[90].



Vasylyev, Figs. 14-15. For example, ports 14 may be configured as "deep linear trenches or grooves" extending along surface 32, which may be fabricated by wet or dry etching techniques. *Vasylyev*, ¶[108].

In *Vasylyev*'s light harvesting system 2, a transparent buffer layer 30 is positioned between microlens array 10 and photovoltaic layer 4, serving to encapsulate layer 4 and protect its electrical contacts from exposure to ambient air and moisture. *Vasylyev*, ¶[116].

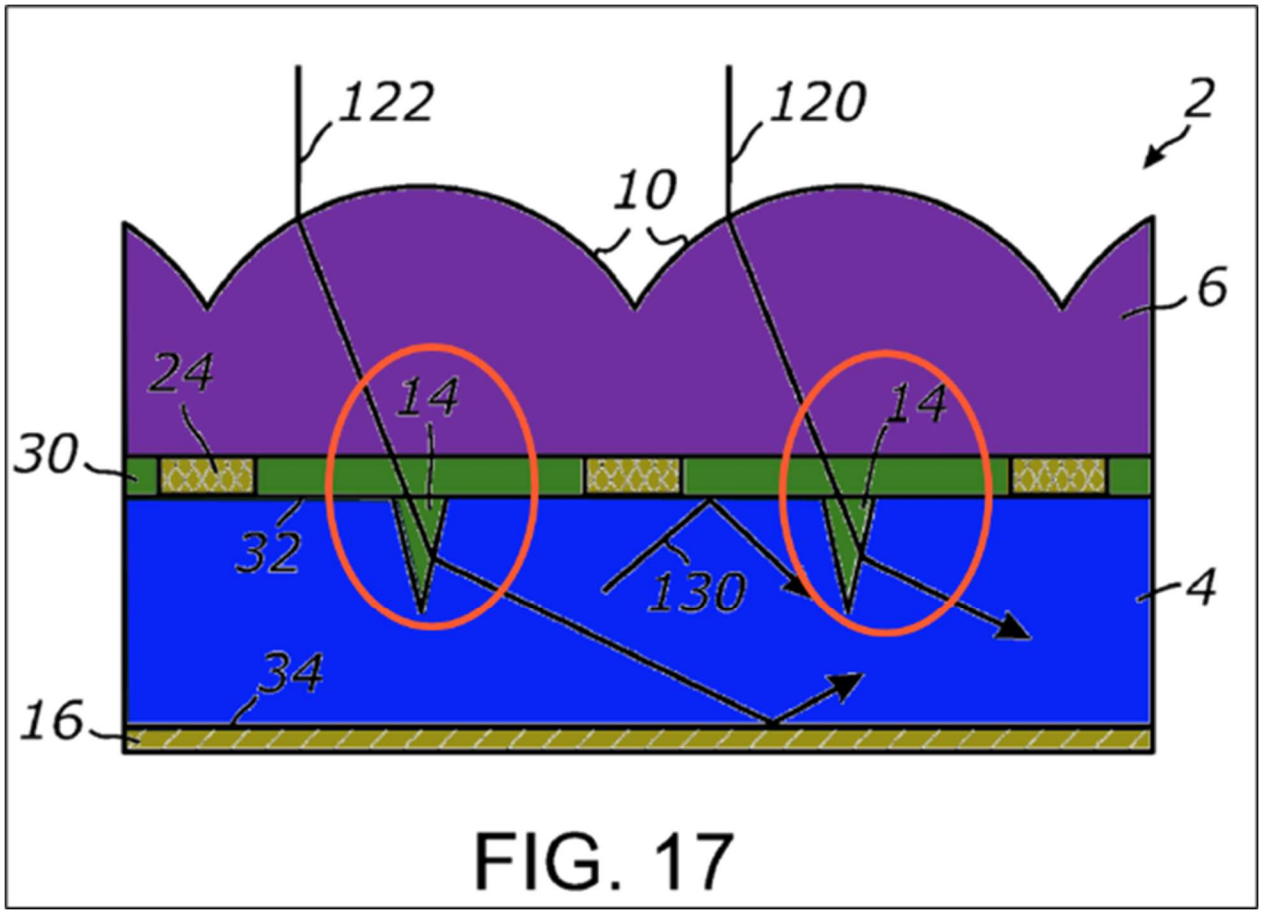


FIG. 17

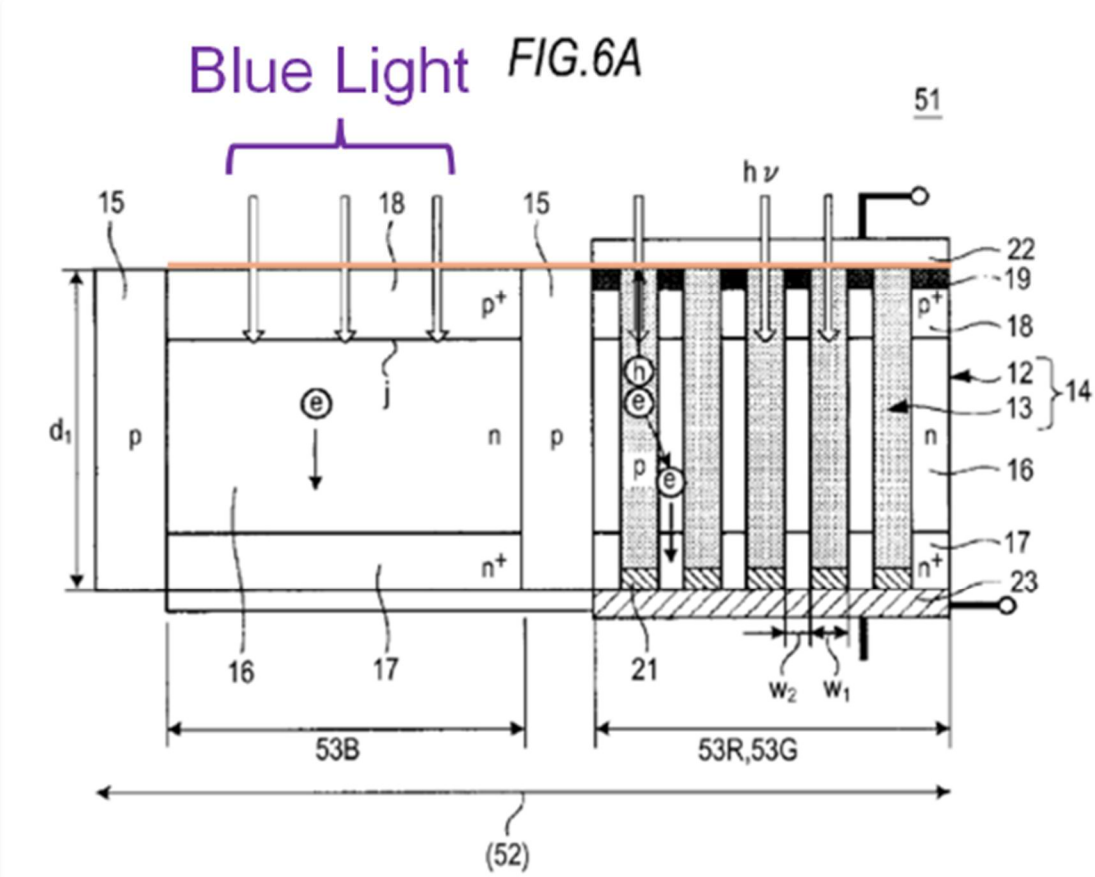
Vasylyev, Fig. 17. Buffer layer 30 may be a conventional encapsulating material such as ethylene vinyl acetate (EVA) or optically clear silicone. *Vasylyev*, ¶[111].

2. *Kuboi* and *Vasylyev* Are Analogous Art to the '948 Patent

Kuboi and *Vasylyev* are analogous art to the '948 Patent because, like the '948 Patent, *Kuboi* and *Vasylyev* seek to improve light absorption efficiency of their respective photoelectric devices. Lebby, ¶238. The '948 Patent is directed to techniques for enhancing photon absorption. '948 Patent, Abstract. Similarly, *Kuboi* is directed to a solid-state imaging device in which light absorption efficiency is increased to improve sensitivity. *Kuboi*, ¶[9]. Likewise, *Vasylyev* discloses techniques to light absorption and energy conversion efficiency in a photoelectric device. *Vasylyev*, ¶[14].

3. Motivation to Apply *Vasylyev*'s Teaching of a Single Light Input Port in Pairwise Optical Relationship with a Microlens to *Kuboi*'s Blue Pixel 53B

In *Kuboi*'s Bayer configuration image sensor, blue pixel 53B is positioned beneath an on-chip microlens and corresponding color filter, enabling it to receive light primarily within the blue wavelength range (or blue light). *Kuboi*, ¶¶[90], [107], [120]; Lebby, ¶239.



Kuboi, Fig. 6A. A POSITA would have understood that, in a Bayer configuration image sensor as depicted above, the blue color filter transmits blue light within a wavelength range of approximately 400-500 nm. Lebby, ¶240; Ex-1024, 6 (Fig. 4).

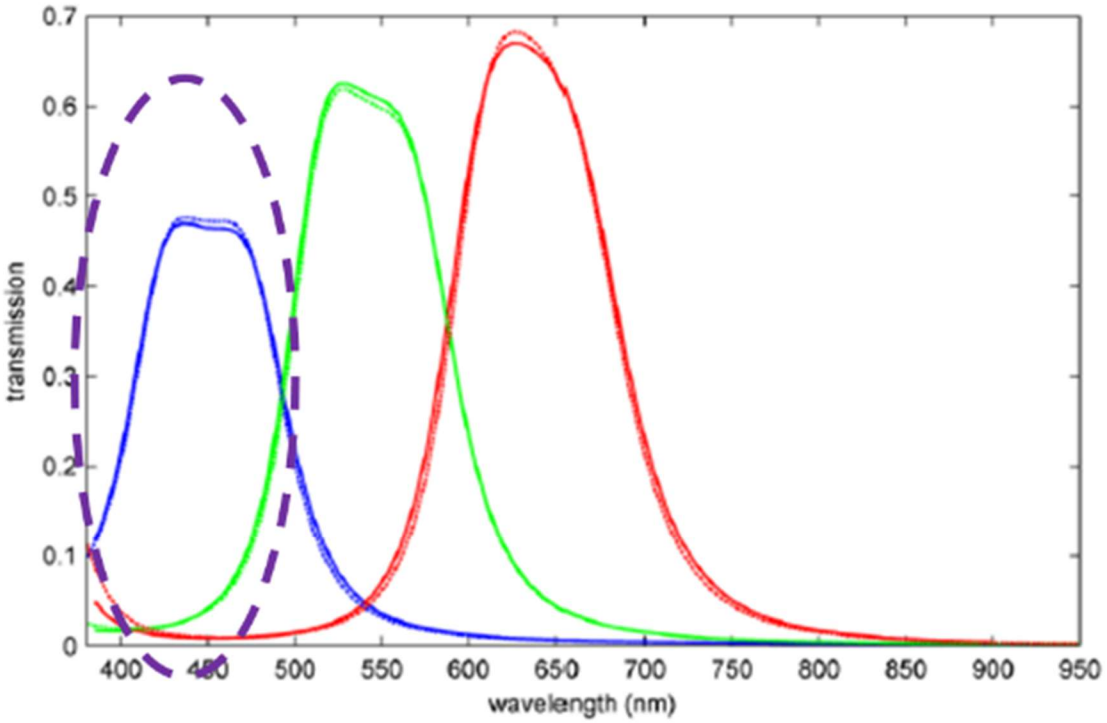


Fig. 4. Measured spectral responses (plain lines) of RGB metal/dielectric filters designed on glass wafer, compared with theory (dashed lines).

Ex-1024, 6 (Fig. 4). The graph above also shows that light transmission through the blue filter is lower than through the green and red filters, indicating that a greater portion of light is reflected by the blue filter. Lebby, ¶¶240-241.

Vasylyev discloses that "bulk crystalline Si, for example, has the refractive index of 3.57 at 1,000 (nanometers) and 5.59 at 400nm which results in the Fresnel reflection of 32% to 49% of the incident light at 1,000nm and 400nm." *Vasylyev*, ¶[12]. Based on *Vasylyev*'s disclosure, a POSITA would have understood that at a 400 nm wavelength—falling within the transmission range of a blue color filter—approximately 49% of incident light is reflected off the silicon light-receiving

surface of *Kuboi*'s blue pixel 53B due to Fresnel reflection. Lebby, ¶242; *Vasylyev*, ¶[12]; *Kuboi*, ¶¶[90]-[91].

Vasylyev teaches that incorporating a single port 14 on light-receiving surface 32 of its silicon photovoltaic layer 4, aligned with the optical axis of corresponding lens 10, improves light coupling efficiency by minimizing Fresnel reflection and further enhances light absorption and energy conversion efficiency by confining the incident light between the parallel surfaces of layer 4. VI.B.1; *Vasylyev*, ¶¶[14]-[16], [93]-[95]; Lebby, ¶243. *Vasylyev*'s arrangement is shown below:

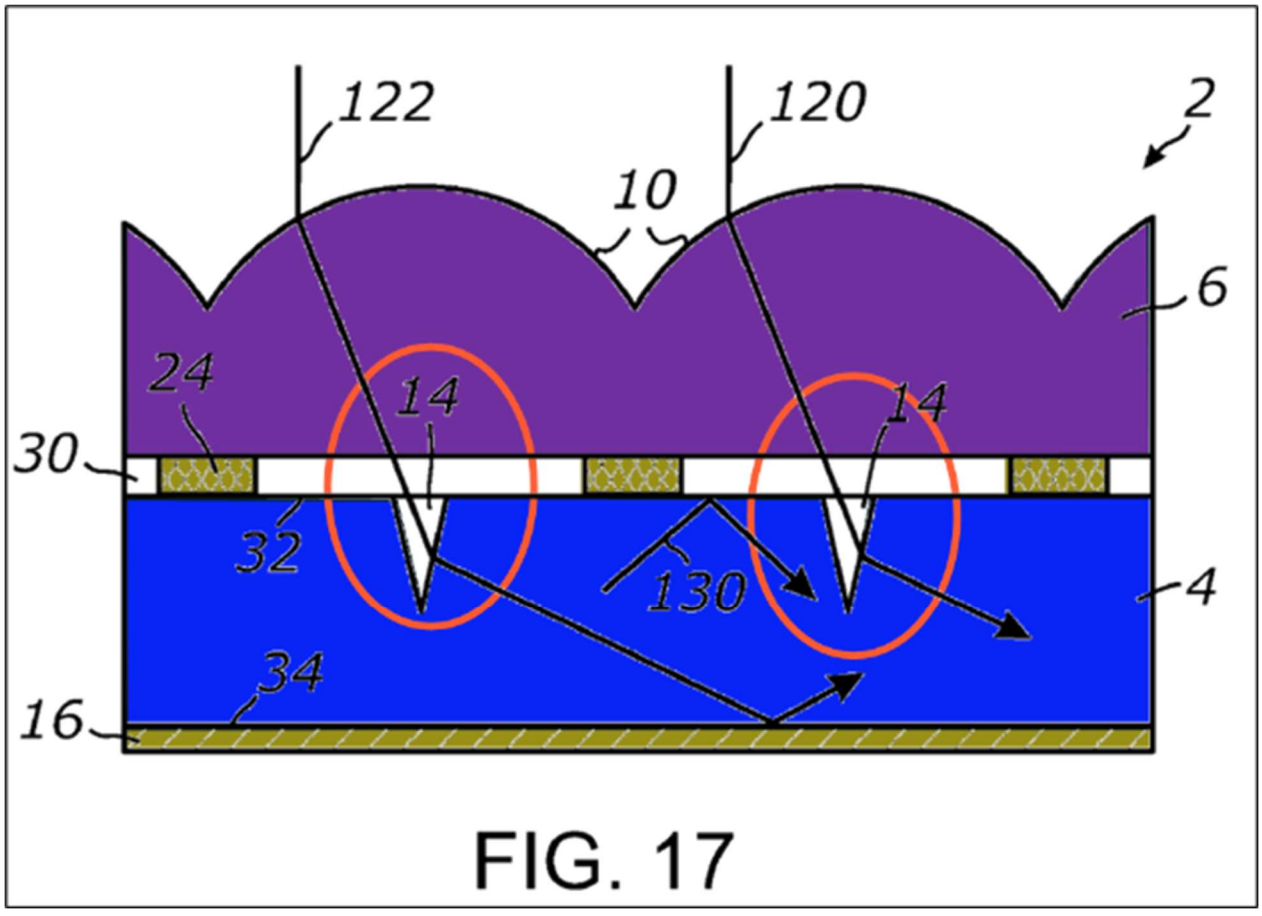
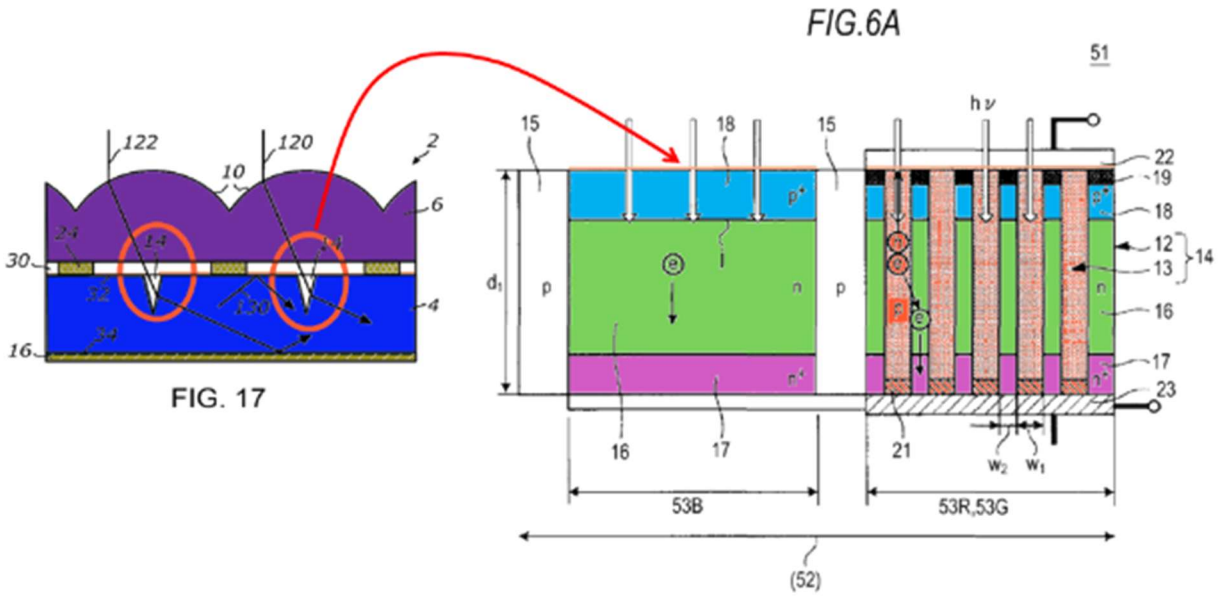


FIG. 17

Vasylyev, Fig. 17.

Based on *Vasylyev*'s teachings, it would have been obvious for a POSITA to implement single port 14 on the light-receiving surface of semiconductor layer 12 in blue pixel 53B, as depicted below, to enhance light coupling by reducing Fresnel reflection of blue light and to further improve light absorption and energy conversion efficiency of blue pixel 53B by confining the incident light within layer 12. Lebby, ¶¶244-246.



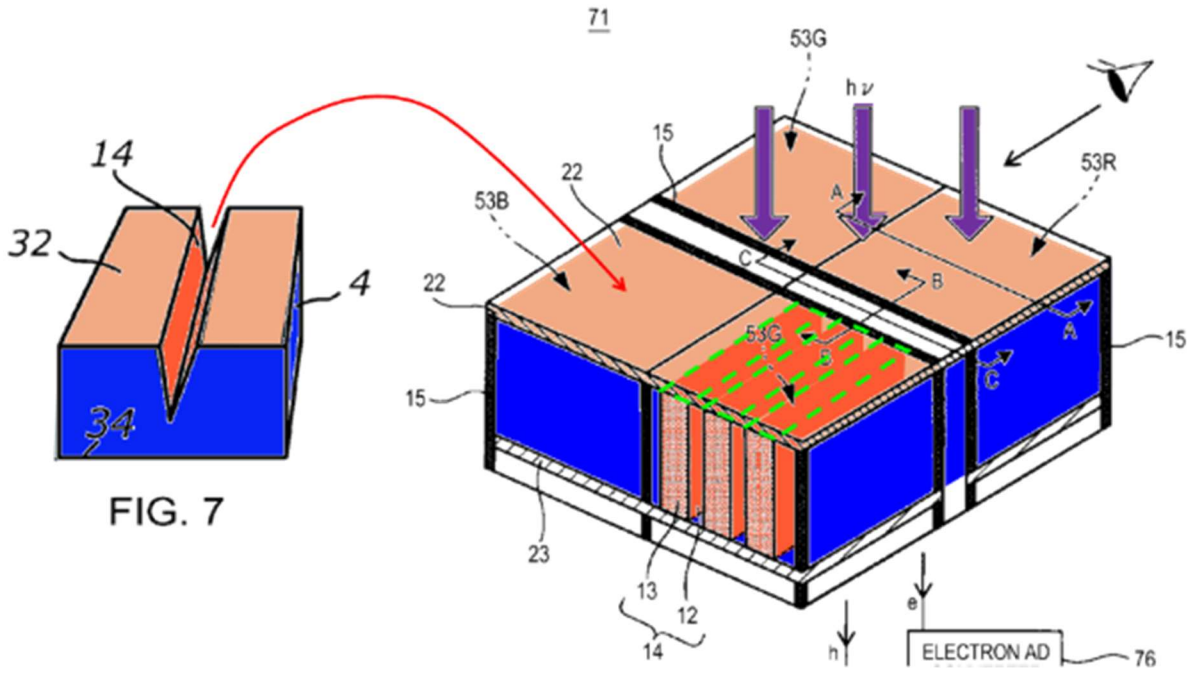
Vasylyev, Fig. 17 (left); *Kuboi*, Fig. 6A (right). Like *Vasylyev*'s photovoltaic layer 4, *Kuboi*'s semiconductor layer 12 forming each blue pixel 53B is a photo-absorptive layer composed of crystalline silicon with a PiN configuration positioned beneath a single lens. *Vasylyev*, ¶¶[65]-[66], [76]-[77]; *Kuboi*, ¶¶[90]-[91], [93]; Lebby, ¶245. Moreover, *Vasylyev*'s port 14 is fabricated by dry etching

the light-receiving surface, in a manner similar to the formation of holes 38 in *Kuboi*'s red and green pixels (53R, 53G) adjacent to blue pixel (53B). *Vasylyev*, ¶¶[83], [108]; *Kuboi*, ¶[72]; Lebby, ¶245.

A POSITA would have had a reasonable expectation of success in incorporating *Vasylyev*'s port 14 into blue pixel 53B as it constitutes a predictable application of known elements according to their established functions. Lebby, ¶246. Both references address optical coupling into a silicon semiconductor layer. *Id*. *Kuboi*'s blue pixel 53B is designed to receive light in the blue wavelength band. *Vasylyev* teaches that positioning single light input port 14 along the optical axis of a lens enhances light coupling and absorption by reducing Fresnel reflection of blue light and by confining incident light within the active layer. *Id*. Given that *Kuboi*'s semiconductor layer 12 and *Vasylyev*'s photovoltaic layer 4 perform analogous photoelectric functions, and that *Kuboi* already employs etched holes—similar in function, structure, and fabrication to *Vasylyev*'s light input port 14—in adjacent pixels using a common process, a POSITA would have reasonably expected that applying *Vasylyev*'s teachings to *Kuboi*'s blue pixel 53B would predictably result in a single hole on its light-receiving surface with similar performance benefits—without requiring inventive skill or undue experimentation. *Id*.

Vasylyev further teaches that each port 14 should have a small transverse dimension to limit surface coverage on light-receiving surface 32, while remaining large enough to intercept a substantial portion of the incident light; and that such a port may be fabricated as an elongated groove extending along surface 32 to satisfy these criteria. *Vasylyev*, ¶¶[86]-[89], [94]; Lebby, ¶247.

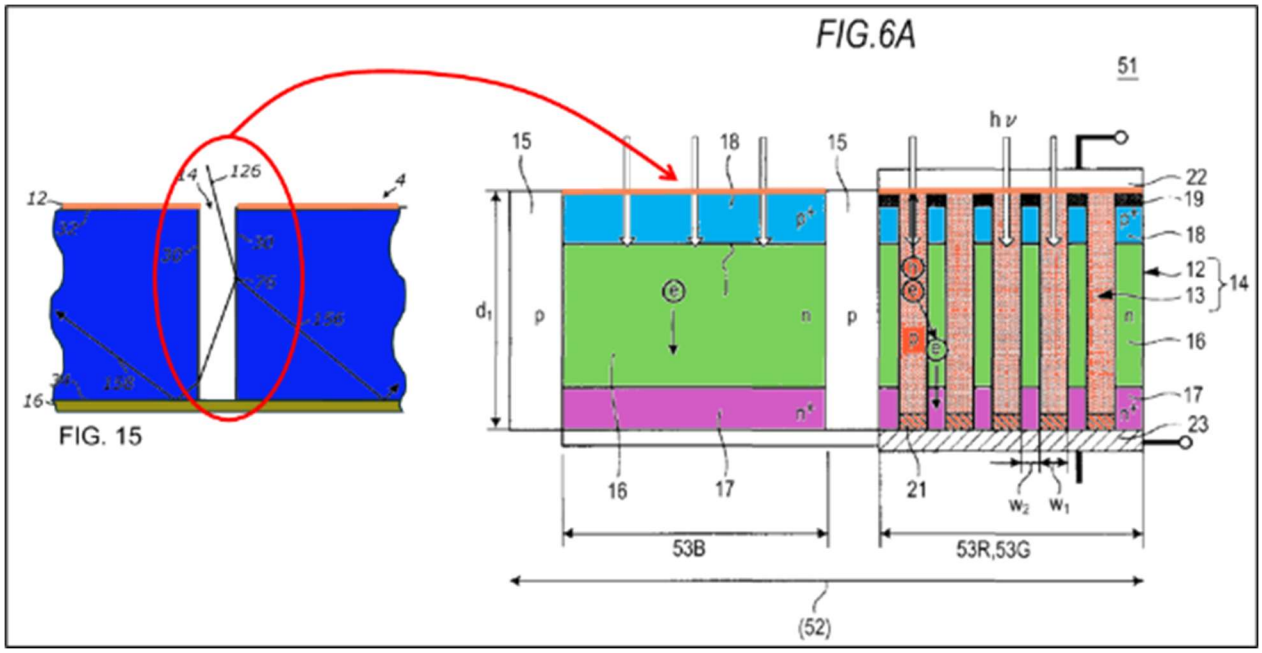
FIG.13



Vasylyev, Fig. 7 (left); *Kuboi*, Fig. 13 (right). For example, *Vasylyev* teaches that an elongated configuration of port 14 on surface 32 enhances light absorption efficiency by enabling interception of a substantial portion of incident light while reducing the chance that a light ray propagating within photovoltaic layer 4 will encounter another port and decouple from layer 4. Lebby, ¶248.

Based on *Vasylyev*'s teaching of port shape, a POSITA would have found it obvious to configure *Vasylyev*'s port 14—when incorporated into *Kuboi*'s blue pixel 53B—with an elongated shape on the light-receiving surface of the pixel's semiconductor layer 12 to similarly enhance light absorption efficiency. Lebby, ¶249. Given that *Kuboi* already employs elongated holes 38 in adjacent pixels (53R, 53G) for a similar purpose, and that both *Kuboi*'s holes 38 and *Vasylyev*'s ports 14 are formed using a dry etching process, a POSITA would have had a reasonable expectation that implementing *Vasylyev*'s teachings on port 14 in *Kuboi* would predictably result in a single hole with an elongated shape on the light-receiving surface of *Kuboi*'s blue pixel 53B. Lebby, ¶249; *Kuboi*, ¶[72].

Vasylyev further teaches that, as illustrated in Figure 15 below, ports 14 may be fabricated as "deep linear trenches or grooves with vertical or near vertical walls," extending through the full thickness of layer 4 such that—based on optical principles—a light ray entering photovoltaic layer 4 via a vertical trench wall has a greater angle relative to the surface normal than its angle of incidence upon entering port 14, thereby increasing the optical path length within layer 4 and enhancing light absorption. *Vasylyev*, ¶¶[107]-[108], Fig. 15; Lebby, ¶250.



Vasylyev, Fig. 15 (left); *Kuboi*, Fig. 6A (right).

Based on *Vasylyev*'s port configuration teaching, a POSITA would have found it obvious to configure *Vasylyev*'s port 14—when incorporated into *Kuboi*'s blue pixel 53B—as a vertical trench that extends the full depth of the pixel's semiconductor layer 12 to similarly enhance light absorption. Lebby, ¶251. A POSITA would also have been motivated to configure port 14 in this manner for an additional reason: because *Kuboi*'s elongated holes 38 in adjacent pixels (53R, 53G) extend through the full depth of the respective semiconductor layers and, like *Vasylyev*'s ports 14, are fabricated using dry etching, a POSITA would have recognized that etching both cavities to the same depth would enable simultaneous processing in a common fabrication step, thereby simplifying and reducing the cost of manufacturing. Lebby, ¶251; *Kuboi*, ¶[72], Figs. 1B, 4B. Given that both

Kuboi's holes 38 and *Vasylyev*'s ports 14 serve a similar function and are formed by the same process, a POSITA would have reasonably expected that configuring the single hole formed in *Kuboi*'s blue pixel 53B similar to the holes in the adjacent green and red pixels (53G, 53R) would predictably result in a single hole that extends the full depth of the semiconductor layer 12 of blue pixel 53B. Lebby, ¶251.

Vasylyev additionally teaches encapsulating photovoltaic layer 4 using a transparent buffer layer 30, such as ethylene vinyl acetate (EVA) or optically clear silicone, to protect it from ambient air and moisture while also increasing light trapping in layer 4 via total internal reflection. *Vasylyev*, ¶¶[111], [116]; Lebby, ¶252. *Vasylyev* discloses that increasing light trapping increases the light path through layer 4 and thus improves light absorption and energy conversion efficiency. *Vasylyev*, ¶[14]. A POSITA would have recognized that, as illustrated below, encapsulating layer 4 in this manner would also result in filling ports 14 on layer 4 with buffer layer 30. Lebby, ¶252. *Vasylyev* teaches that buffer layer 30 may comprise ethylene vinyl acetate (EVA) or optically clear silicone. *Vasylyev*, ¶[111]. A POSITA would have understood that both materials are widely used as dielectric coatings for encapsulating conductive wiring in optical systems. Lebby, ¶252; *see* Ex-1040, 2-5; Ex-1041, 2; Ex-1042, 2 ("EVA … provides good dielectric properties."); Ex-1045, 7:14-26.

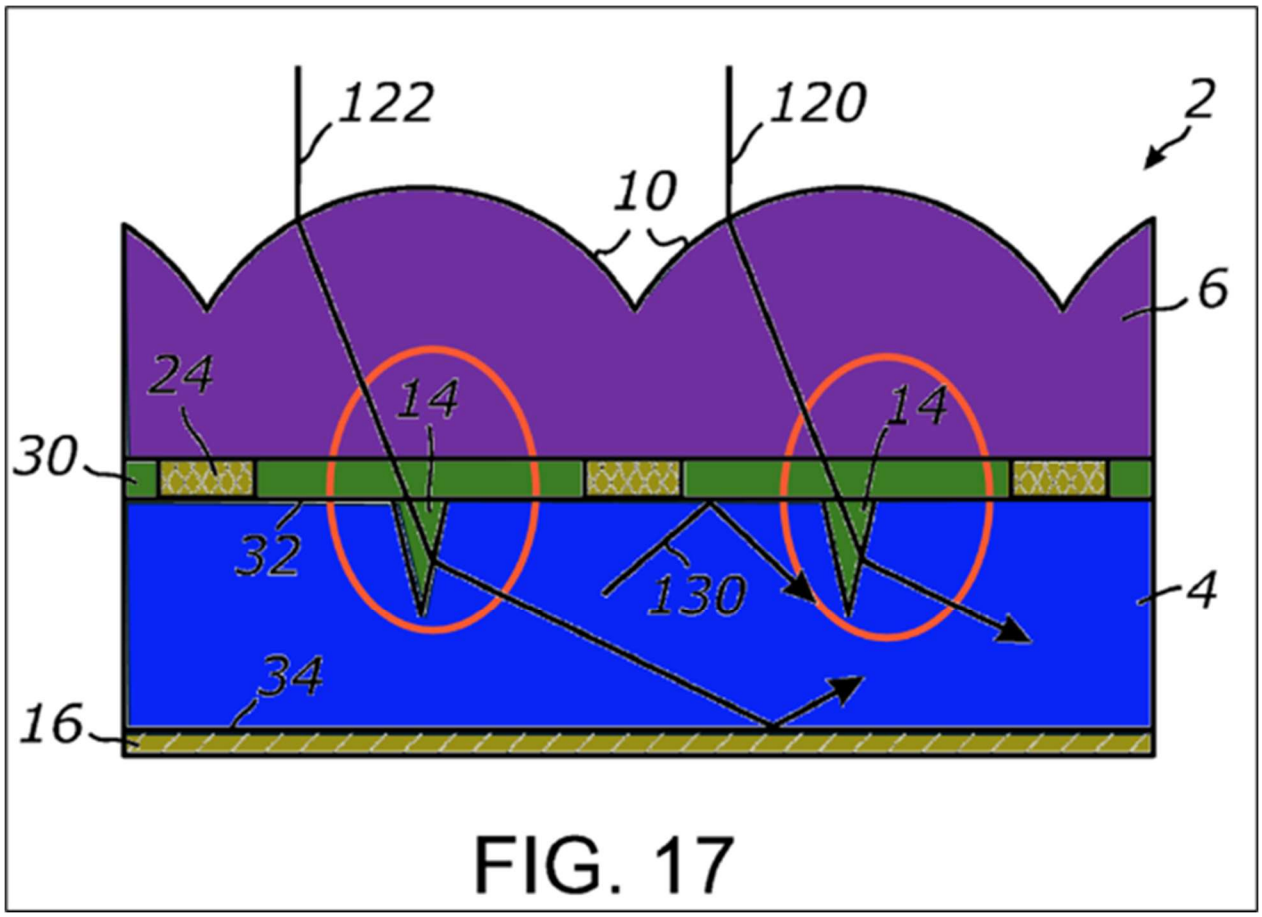


FIG. 17

Vasylyev, Fig. 17.

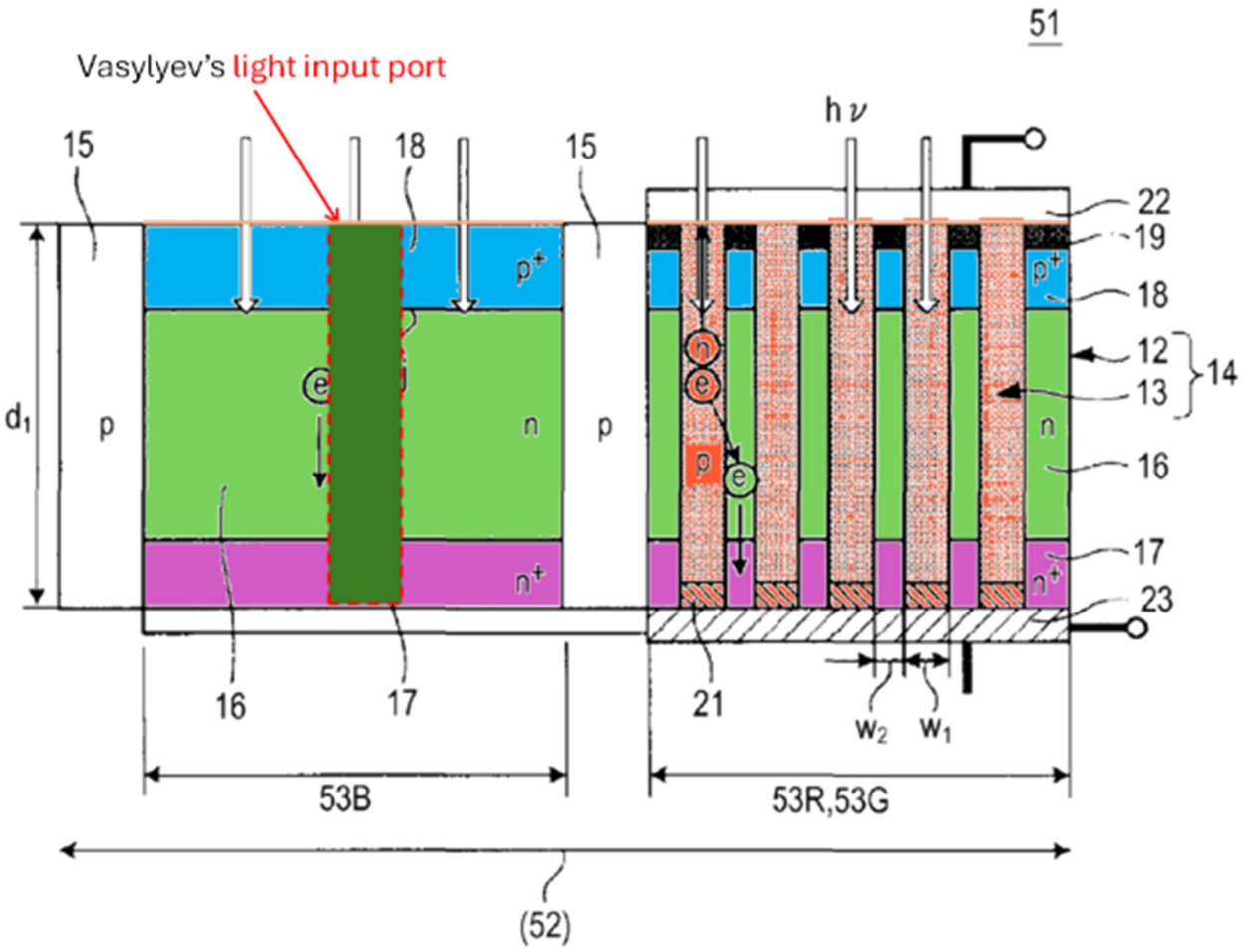
In light of *Vasylyev*'s teaching, a POSITA would have found it obvious to encapsulate port 14—when implemented in *Kuboi*'s blue pixel 53B—with *Vasylyev*'s transparent buffer layer 30 to similarly shield semiconductor layer 12 of *Kuboi*'s blue pixel 53B from ambient air and moisture while enhancing light trapping and thereby improving absorption and energy conversion efficiency. Lebby, ¶253. Moreover, it was well known that dielectric coatings are used "for capping doped films to prevent the loss of dopants, and for passivation to protect

devices from impurities, moisture, and scratches." Ex-1012, 12. Based on this established understanding, a POSITA would have reasonably expected that applying a dielectric coating like *Vasylyev*'s buffer layer 30 over the exposed doped surfaces and port on pixel 53B would preserve dopant integrity and protect the device from environmental degradation. Lebby, ¶253. This represents a predictable use of a known technique to address a known problem—modifying a similar device for a similar purpose to achieve known benefits—consistent with *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007).

Accordingly, as shown below, a POSITA would have found it obvious, in view of *Vasylyev*'s teachings, to implement single port 14—structured as an elongated, narrow trench extending through the full thickness of semiconductor layer 12 and encapsulated with *Vasylyev*'s transparent dielectric buffer layer—in *Kuboi*'s blue pixel 53B[4] to enhance the coupling and trapping of blue light and thereby improve absorption and energy conversion efficiency. Lebby, ¶254.

[4] This Petition refers to *Kuboi*'s imaging device with a single light input port having this configuration incorporated in blue pixel 53B, based on *Vasylyev*'s teachings, as the *Kuboi-Vasylyev-1* imaging device.

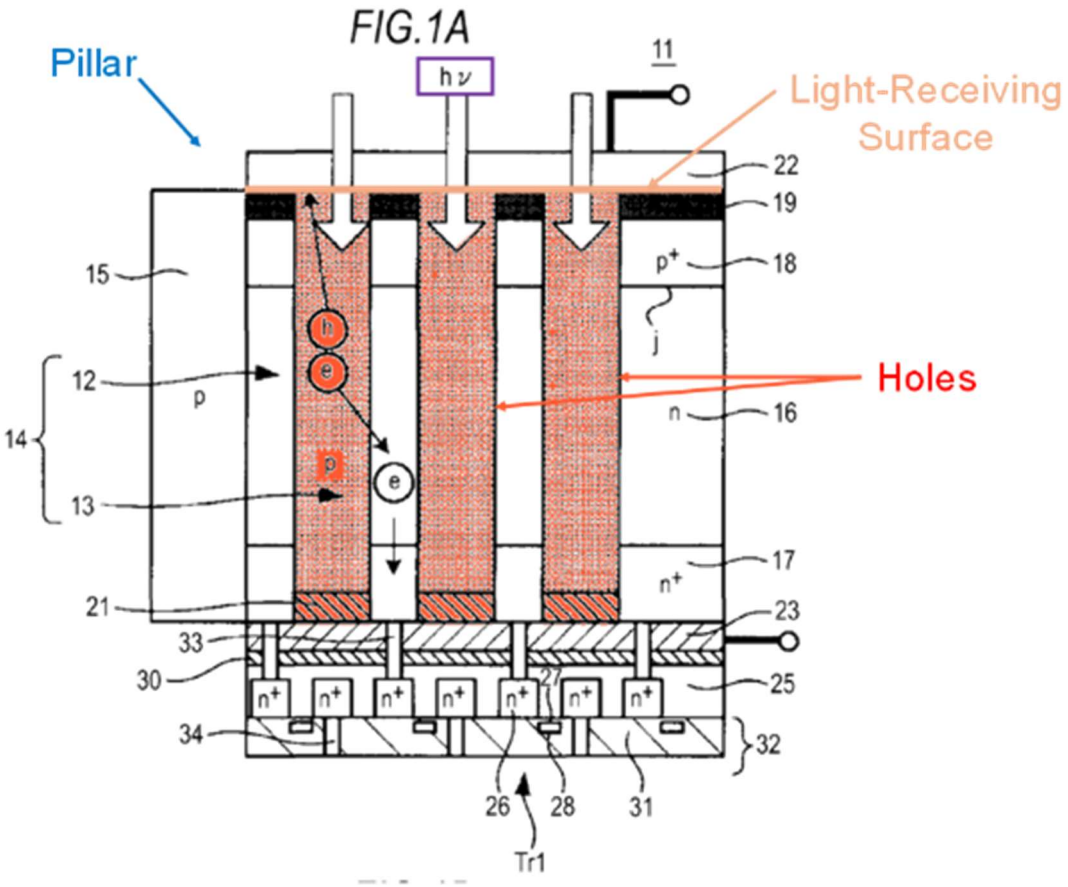
FIG.6A



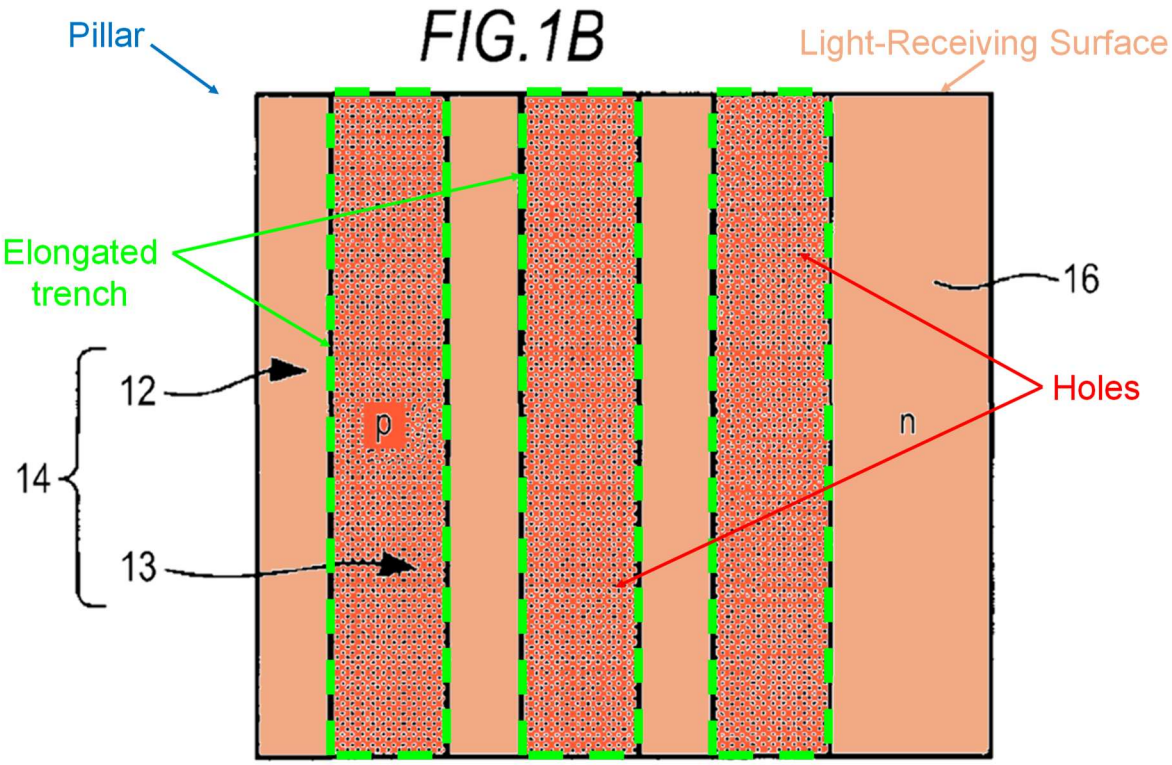
Kuboi, Fig. 6A. A POSITA would have reasonably expected success in this *Kuboi–Vasylyev* combination, as it involves the straightforward integration of known elements and fabrication techniques already disclosed by *Vasylyev*. Lebby, ¶255.

4. Motivation to Apply *Vasylyev*'s Teaching of a Light Input Port Extending Along a "Substantial Portion" of the Light-Receiving Surface to *Kuboi*'s Green and Red Pixels (53G, 53R)

In *Kuboi*'s image sensor, illustrated below, photoelectric conversion portion 14 of green and red pixels (53G, 53R) includes multiple vertical holes 38—such as elongated trenches—formed within semiconductor layer 12, incorporating organic photoelectric conversion film 13 and extending "in a stripe shape" across the entire light-receiving surface of photoelectric conversion portion 14. VI.A.3.e; *Kuboi*, ¶¶[72], [90]. *Kuboi* suggests that the shape of the photoelectric conversion film 13 may be modified from a stripe configuration to a shorter form, such as a "dot shape," to improve performance characteristics. Lebby, ¶256; *see Kuboi*, ¶[57].


FIG.1A
Pillar
hν
11
Light-Receiving Surface
22
19
18
15
12
p
14
13
h
e
p
e
j
Holes
n
16
17
n+
21
23
33
30
25
34
32
26
28
31
Tr1

Kuboi, Fig. 1A.

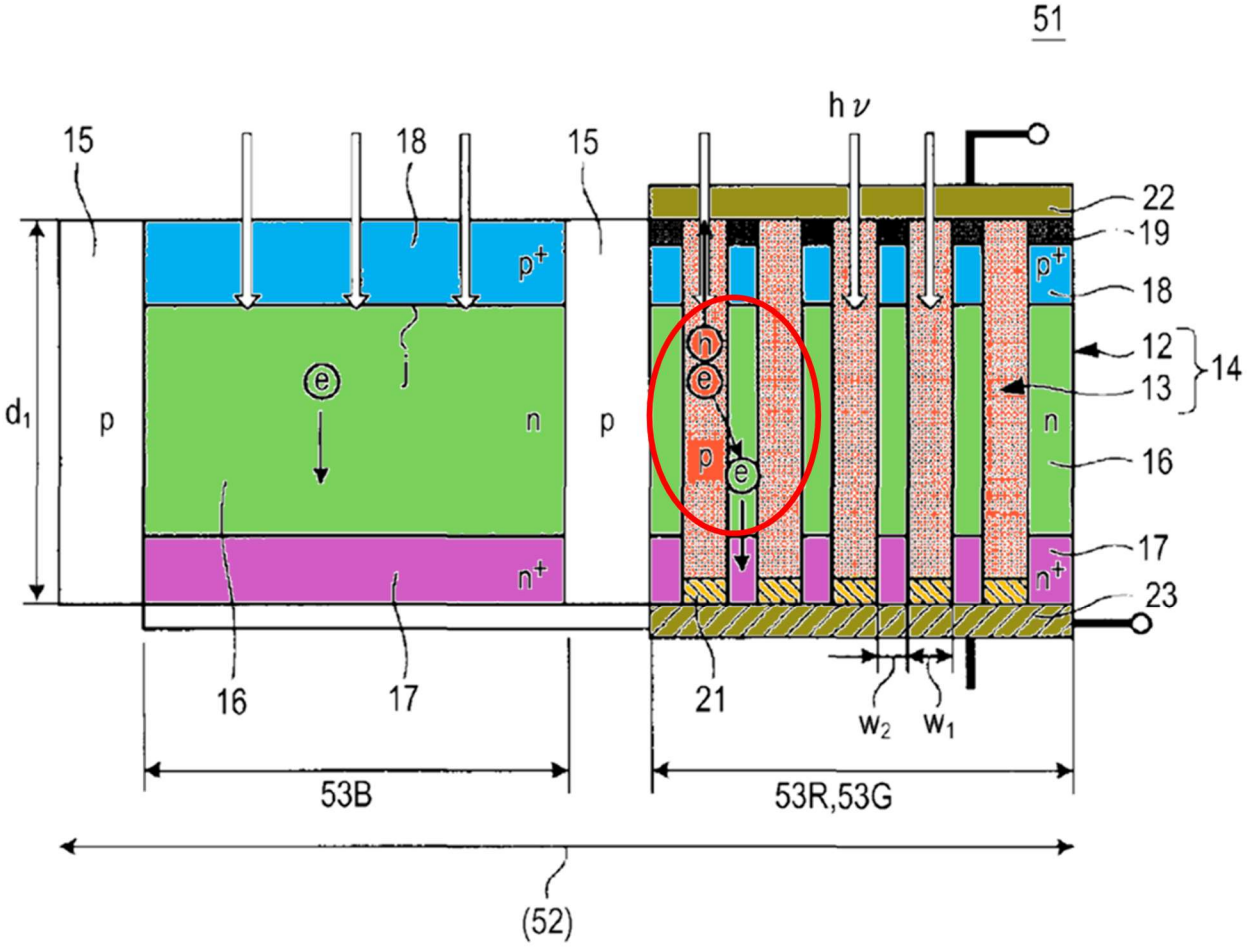


Kuboi, Fig. 1B.

In *Kuboi*, light (hν) passes through the on-chip microlens and enters film 13 located in holes 38, where photoelectric conversion occurs, generating electrons (e) that subsequently migrate into semiconductor layer 12 through the film/silicon interface for collection. *Kuboi*, ¶¶[11], [64].

According to *Kuboi*, although organic films 13 in green and red pixels (53G, 53R) exhibit greater light absorption than silicon, their electron mobility is comparatively lower, which reduces operational speed. *See Kuboi*, ¶¶[3], [8], [12], [80], [82], [92].

FIG.6A



Kuboi, Fig. 6A. To address this reduction in operational speed, holes 38 are designed to facilitate rapid transfer of the photogenerated electrons from films 13 into semiconductor layer 12. *Kuboi*, ¶¶[8], [12], [65]; Lebby, ¶¶256-259. Embedding multiple films 13 within a single pixel serves two purposes: (a) it shortens the average distance electrons must travel to reach the interface with semiconductor layer 12, and (b) it increases the interface area, promoting more

efficient electron transfer and improving the device's operating speed. Lebby, ¶259; *see Kuboi*, ¶¶[8], [12], [65].

Kuboi further discloses that increasing the silicon-film interface area beyond the initial configuration amplifies electron transport efficiency, resulting in an even greater improvement in device operating speed. Lebby, ¶260; *Kuboi*, ¶¶[8], [68], [72]. To further increase the interface area, a Bosch process may be used to form the holes' vertical walls in a concavo-convex shape. *Kuboi*, ¶¶[67]-[68], Fig. 9.

Like *Kuboi*, light enters *Vasylyev*'s photovoltaic layer 4 through its light input ports 14. VI.B.1; *Vasylyev*, ¶[97]. And like *Kuboi*'s holes 38, *Vasylyev*'s ports 14 (illustrated below) may be formed as "deep linear trenches" on the light-receiving surface 32. *Vasylyev*, ¶¶[107]-[108].

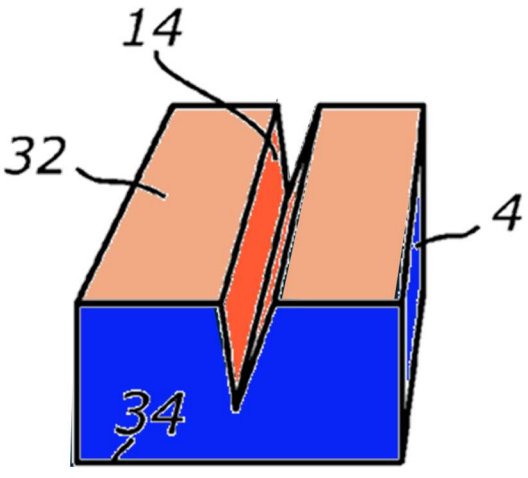


FIG. 7

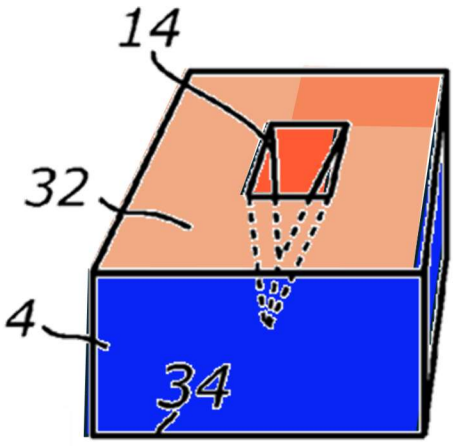
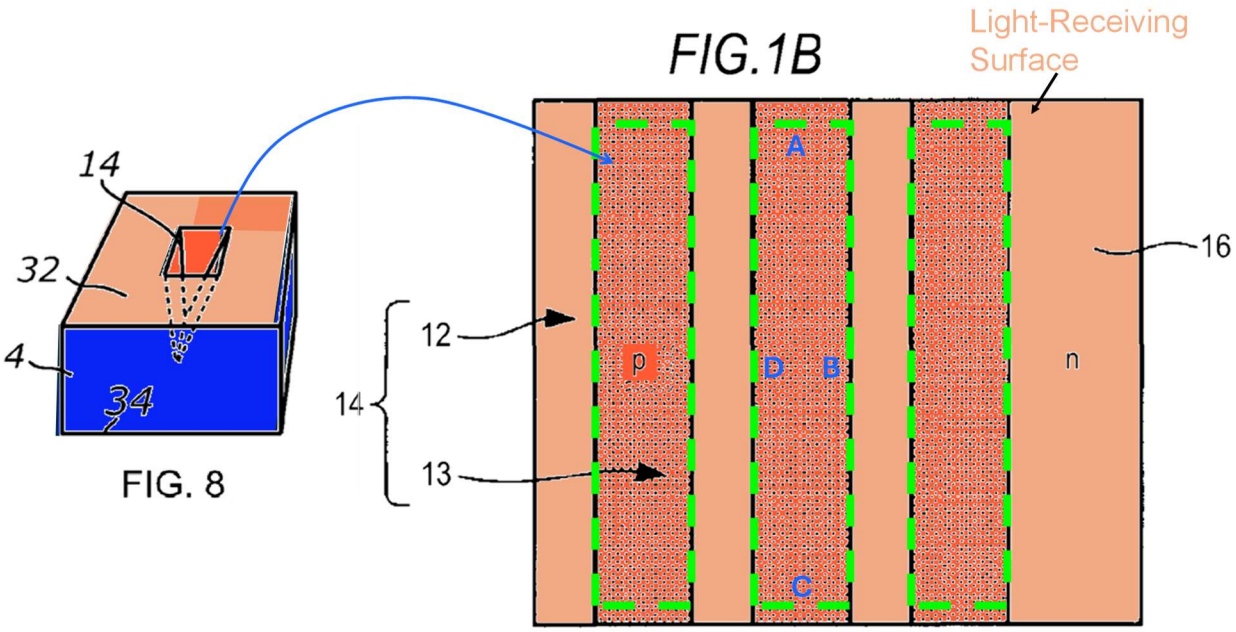


FIG. 8

Vasylyev, Figs. 7-8. *Vasylyev*'s port 14 can extend "all the way along [its light-receiving] surface 32 or its substantial portion." *Vasylyev*, ¶[89].

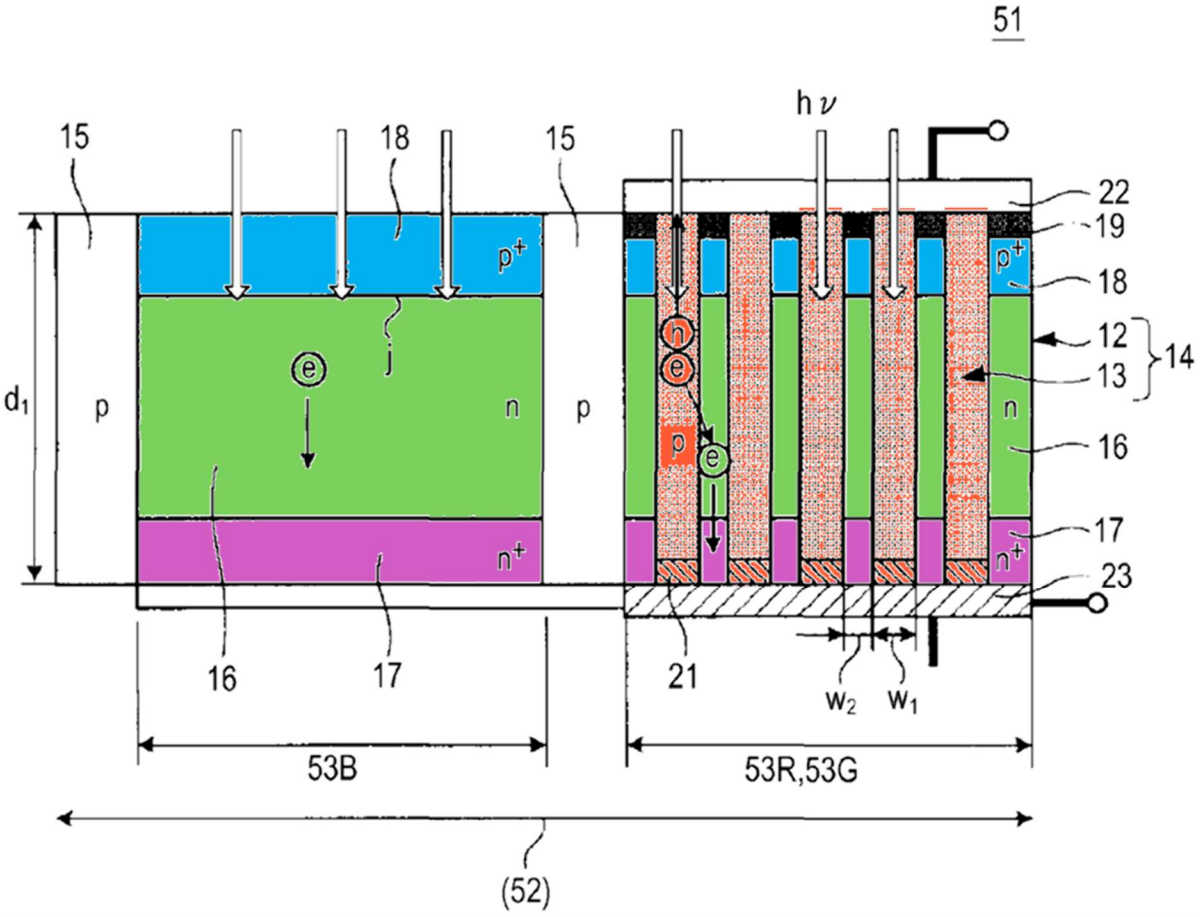
Based on *Vasylyev*'s teachings, it would have been obvious to a POSITA that extending holes 38 in photoelectric conversion portions 14 of *Kuboi*'s green and red pixels (53G, 53R) along a substantial portion—rather than the full extent—of the light-receiving surface would further reduce the average distance to the silicon-film interface, increase the interface area, and thereby improve device operating speed. Lebby, ¶¶262-263; *see Kuboi*, ¶¶[8], [68], [72]. Additionally, *Kuboi* explicitly proposes modifying the shape of the films 13 within the holes—such as shortening it from a stripe configuration—to enhance device performance. Lebby, ¶263; *see Kuboi*, ¶[57].



Vasylyev, Fig. 8 (left); *Kuboi*, Fig. 1B (right). A POSITA would have recognized that modifying holes 38 in *Kuboi*'s green and red pixels (53G, 53R) in this manner reduces the distance to the silicon-film interface by enabling electrons generated in film 13 to enter semiconductor layer 12 via the interfaces along edges A and C, in addition to those along edges B and D. Lebby, ¶¶264-266. Additionally, such a modification to the hole configuration would increase the silicon-film interface area. *Id*.

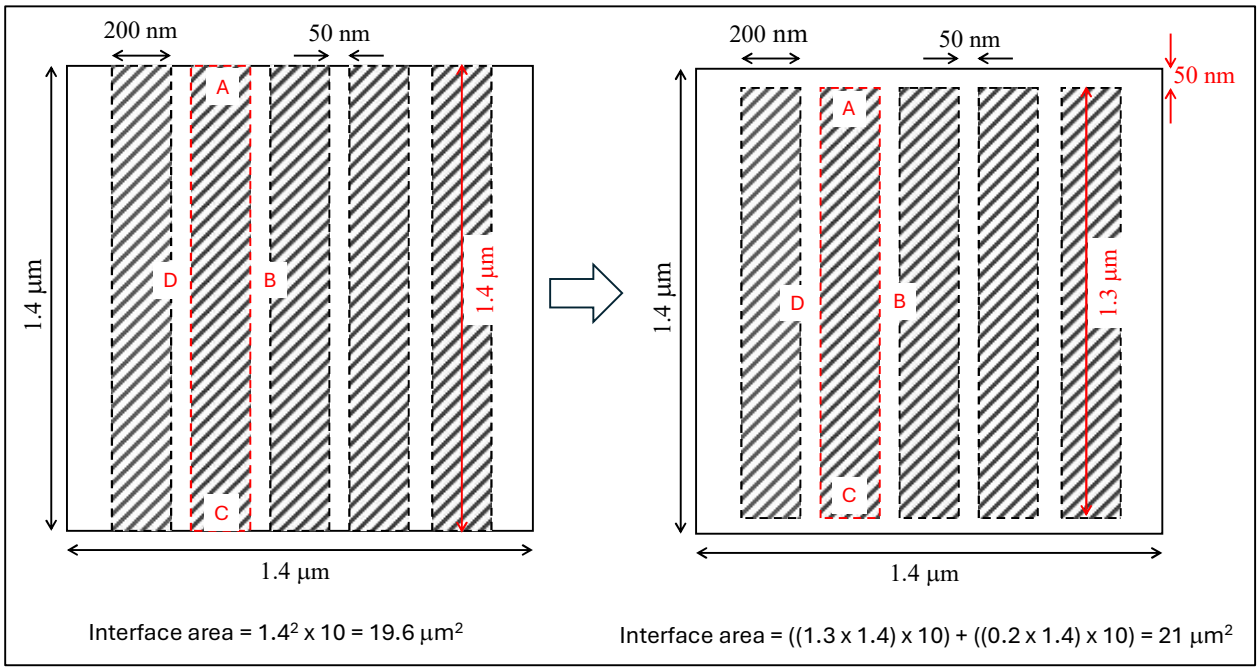
Photoelectric conversion portion 14 of *Kuboi*'s green and red pixels (53G, 53R) measures 1.4 μm X 1.4 μm, with a 1.4 μm semiconductor layer depth d_1. *Kuboi*, ¶[94].

FIG.6A



Kuboi, Fig. 6A. Five photoelectric conversion films 13, each having a 200 nm width (W_1), are embedded in semiconductor layer 12 at a 50 nm spacing (W_2). *Kuboi*, ¶[94]. In this configuration, disregarding the thickness of light shielding film 19 and electron blocking film 21—each measuring only several tens of nanometers (*Kuboi*, ¶¶[73], [75])—the area of the silicon-film interface is approximately 1.4^2 x 5 x 2 = 19.6 μm^2. Lebby, ¶266.

Modifying *Kuboi*'s holes 38 to extend along a substantial portion of the light-receiving surface—such as 1.3 µm instead of 1.4 µm, as illustrated below—increases the silicon-film interface area by approximately 7%. Lebby, ¶267.



Lebby, ¶¶267-268. Accordingly, based on *Vasylyev*'s teachings, it would have been obvious for a POSITA to modify holes 38 in *Kuboi*'s green and red pixels (53G,53R) to extend along a substantial portion—rather than the entire length—of the light-receiving surface, to reduce the average distance to the silicon-film

interface, enlarge the interface area, and thereby increase *Kuboi*'s operational speed.[5] Lebby, ¶268; *see Kuboi*, ¶¶[8]-[9].

A POSITA would have recognized that, even though reducing the length of each hole 38 by 100 nm slightly decreases the light incidence area of organic film 13 within hole 38, this reduction would have minimal impact on the light absorption performance of photoelectric conversion portion 14, owing to the high absorption efficiency (α) of organic films 13. Lebby, ¶269.

A POSITA would have had a reasonable expectation of success in incorporating *Vasylyev*'s teaching regarding port 14 in *Kuboi*'s red pixel 53R because it constitutes a predictable application of known elements according to their established functions. Lebby, ¶270. Both references address optical coupling into a silicon semiconductor layer using microstructured cavities. *Id.* Building on *Kuboi*'s teaching that increasing the silicon-film interface enhances electron transport and device speed, a POSITA would have understood that applying *Vasylyev*'s teaching of port 14 to the holes in *Kuboi*'s green and red pixels (53G, 53R) would further improve the imaging device's operating speed. Lebby, ¶270;

[5] This Petition refers to *Kuboi*'s imaging device with the holes of green and red pixels (53G, 53R) modified in this manner, based on *Vasylyev*'s teachings, as the *Kuboi-Vasylyev-2* imaging device.

Kuboi, ¶¶[8], [68], [72]. Moreover, since *Kuboi*'s semiconductor layer 12 and *Vasylyev*'s photovoltaic layer 4 perform analogous photoelectric functions, and that *Kuboi* already employs etched holes—similar in function, structure, and fabrication to *Vasylyev*'s port 14—in adjacent pixels using a common process, a POSITA would have reasonably expected that implementing *Vasylyev*'s teachings in *Kuboi*'s green and red pixels (53G, 53R) would predictably result in holes that extend along less than the full extent of the light-receiving surface of these pixels. Lebby, ¶270.

5. Motivation to Additionally Incorporate a Single Light Input Port in the Blue Pixel 53B of the *Kuboi-Vasylyev-2* Imaging Device Based on *Vasylyev*'s Teaching

As previously discussed, a POSITA would have found it obvious to modify the holes 38 in *Kuboi*'s green and red pixels (53G, 53R) so that they extend across a substantial portion—rather than the full length—of the light-receiving surface, thereby forming the *Kuboi-Vasylyev*-2 imaging device with increased operational speed. VI.B.4.

Based on *Vasylyev*'s teachings, a POSITA would have found it obvious to incorporate an additional single light input port 14 into the blue pixel 53B—configured as an elongated hole that extends along a substantial portion—rather than the full length—of the light-receiving surface, penetrates the full thickness of the semiconductor layer 12, and is encapsulated by *Vasylyev*'s transparent buffer

layer 30—to enhance blue light coupling and trapping, thereby improving light absorption and energy conversion efficiency in the *Kuboi-Vasylyev-2* imaging device. *See* VI.B.3; Lebby, ¶¶271-277.

Indeed, a POSITA would have understood that Fresnel reflection is greatest for blue light, and the prior art combination reduces the amount of this unwanted Fresnel reflection. Ex-1039, 2; Lebby, ¶273. *Vasylyev* further teaches that up to 49% of incident blue light at 400 nm may be lost due to Fresnel reflection at the surface of the blue pixel 53B. *Vasylyev*, ¶[12]. Accordingly, a POSITA would have been motivated to additionally incorporate *Vasylyev*'s single light input port 14 on the light-reflective surface of the blue pixel 53B in the *Kuboi-Vasylyev-2* imaging device to mitigate reflection losses and enhance light coupling and optical efficiency[6]. VI.B.3, VI.B.6.a (claim 4); Lebby, ¶273.

The holes in green and red pixels (53G, 53R) of the *Kuboi-Vasylyev-2* imaging device extend along a substantial portion—but not the full extent—of the light-receiving surface. VI.B.4. A POSITA would have found it obvious to configure *Vasylyev*'s light input port 14, incorporated in blue pixel 53B of the

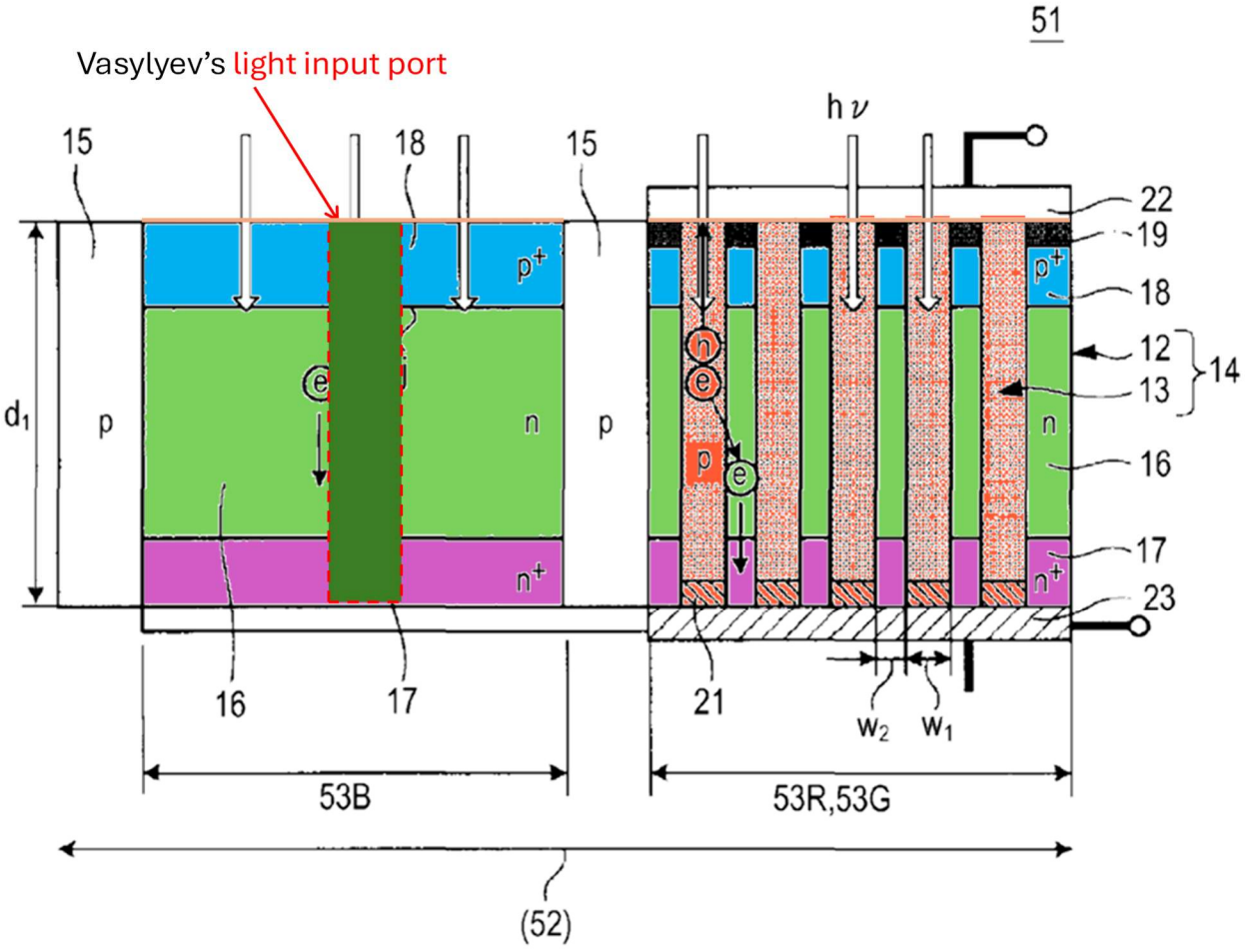
[6] This Petition refers to the *Kuboi-Vasylyev-2* imaging device additionally modified to incorporate a single light input port in the blue pixel (53B) based on *Vasylyev*'s teachings, as the *Kuboi-Vasylyev-3* imaging device.

Kuboi-Vasylyev-2 imaging device to match the shape of the holes in adjacent green and red pixels (53G, 53R) to simplify and reduce fabrication costs. Lebby, ¶274. A POSITA would have recognized that by limiting the lateral extent of *Vasylyev*'s port 14 incorporated in the light-receiving surface of *Kuboi*'s blue pixel, light can enter its photoelectric conversion portion from all four sides of the port rather than just two opposing sides. *Id.*; *see* VI.B.4. A POSITA would have known that this multidirectional light entry increases the effective optical path length in the photoelectric conversion portion thereby increasing light trapping and absorption. Lebby, ¶274. In contrast, a hole that spans the full width of the light-receiving surface restricts light entry to two sides, reducing the light interaction volume and diminishing absorption efficiency. *Id.*

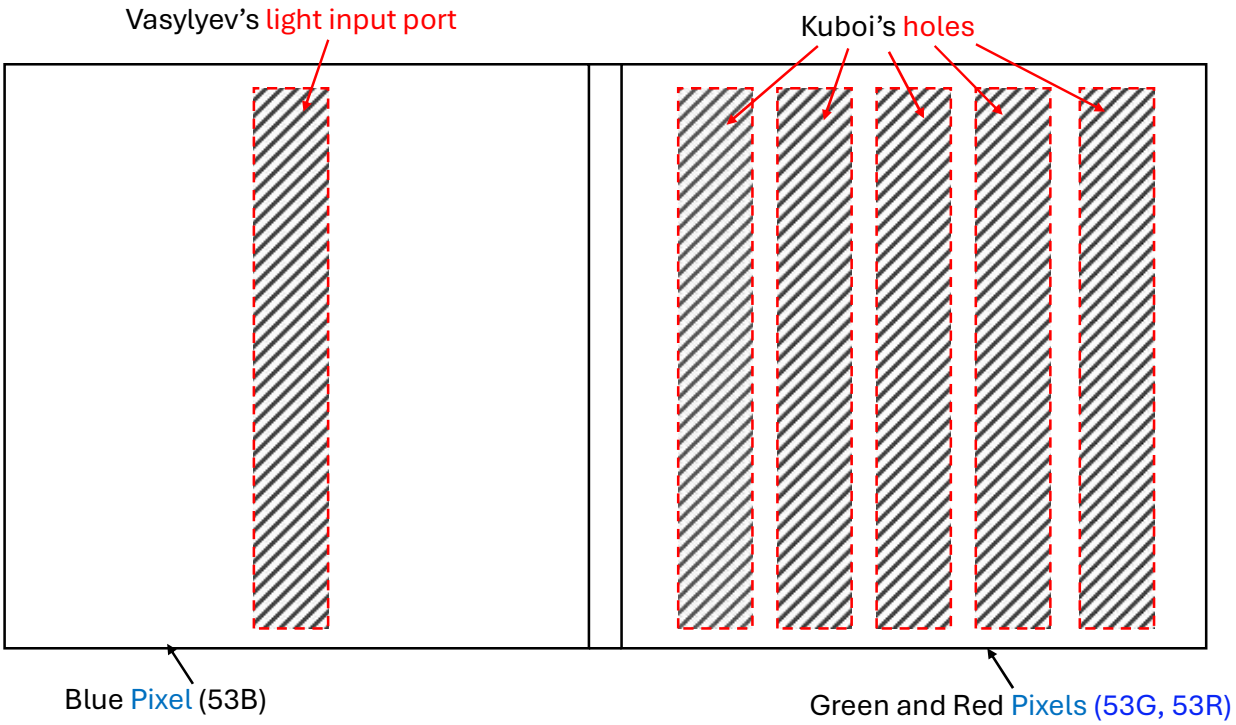
Moreover, because both *Vasylyev*'s ports and *Kuboi*'s holes are fabricated using dry etching, a POSITA would have recognized that shaping and etching the cavities across all pixels in a common masking and etching step would enable simultaneous processing, streamlining fabrication and lowering cost. Lebby, ¶275. Given that these cavities serve a similar function of increasing light absorption, and are produced using the same technique, a POSITA would have reasonably expected that configuring port 14 in the blue pixel 53B to resemble the holes in green and red pixels (53G, 53R) would yield predictable results. *Id.*

When the *Kuboi-Vasylyev-2* imaging device is further modified in this manner based on the teachings of *Vasylyev*, blue pixel 53B would have only a single elongated hole aligned with the optical axis of corresponding microlens, extending along a substantial portion—rather than the full length—of the light-receiving surface, penetrating the full thickness of semiconductor layer 12, and encapsulated by *Vasylyev*'s dielectric buffer layer 30. Lebby, ¶276. This is further illustrated below.

FIG.6A



Kuboi, Fig. 6A (modified).



Lebby, ¶¶276-277.

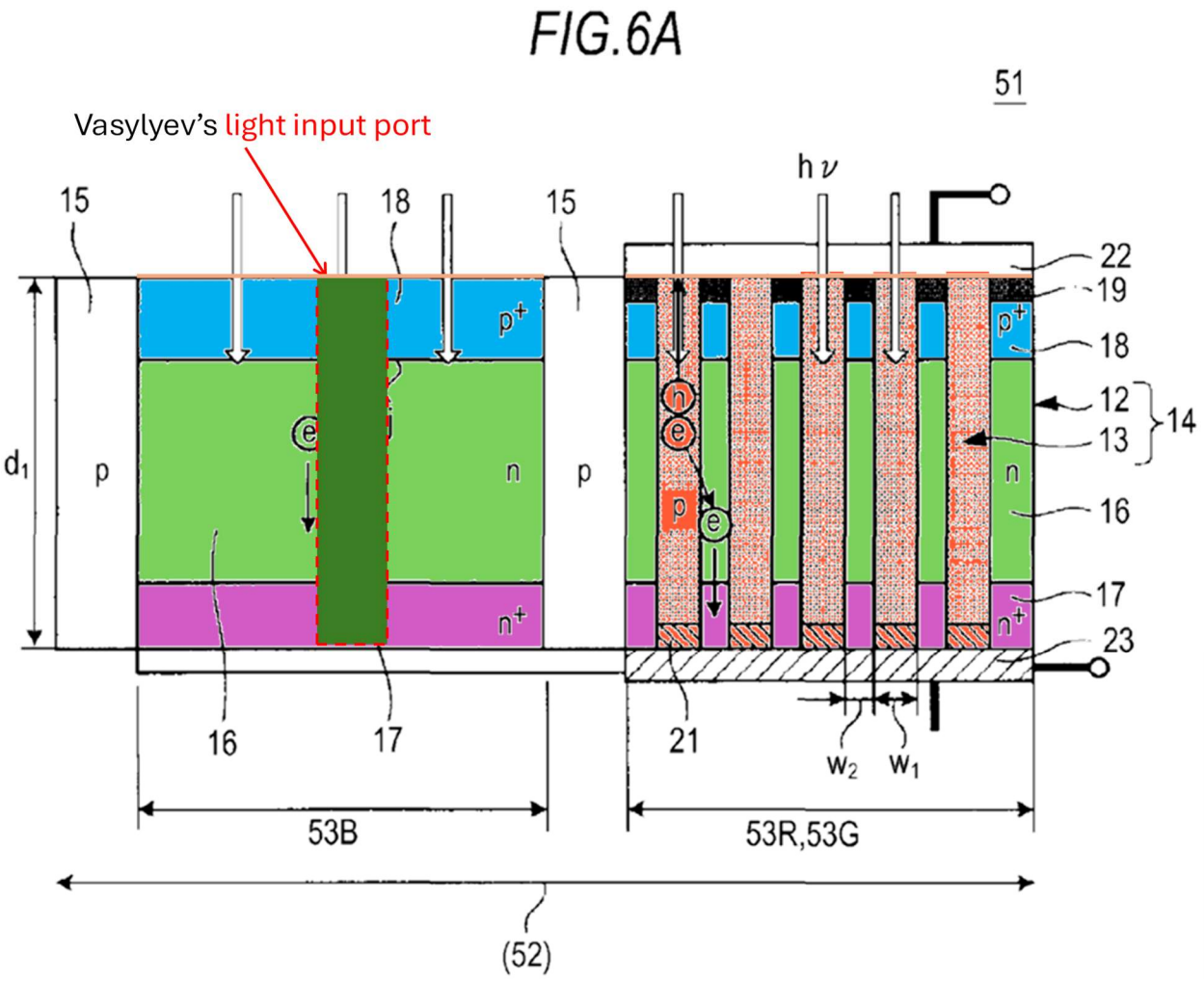
Since the thickness of blue pixel 53B (d_1) is 1400 nm, port 14 will extend into blue pixel 53B to a depth ranging from 100-10,000 nanometers. Lebby, ¶277; *Kuboi*, ¶[94].

6. Claim 4

a. "The integrated structure of claim 1, wherein each of at least some of the pillars has only one of the elongated holes."

Kuboi discloses and/or renders obvious the limitations of independent claim 1. VI.A.3. *Kuboi* in view of *Vasylyev* renders obvious this additional limitation. Lebby, ¶¶278-283.

As explained above, based on *Kuboi* and *Vasylyev*'s teachings and as illustrated below, a POSITA would have found it obvious to incorporate *Vasylyev*'s single port 14 into *Kuboi*'s blue pixel 53B. VI.B.3; Lebby, ¶279. In the resulting *Kuboi-Vasylyev-1* imaging device, port 14—designed as an elongated trench extending along the light-receiving surface and penetrating the full thickness of pixel 53B's semiconductor layer 12, and encapsulated by *Vasylyev*'s transparent buffer layer 30—enhances blue light coupling and trapping within the semiconductor layer, thereby improving the photodiode's light absorption and energy conversion efficiency. VI.B.3; Lebby, ¶279.

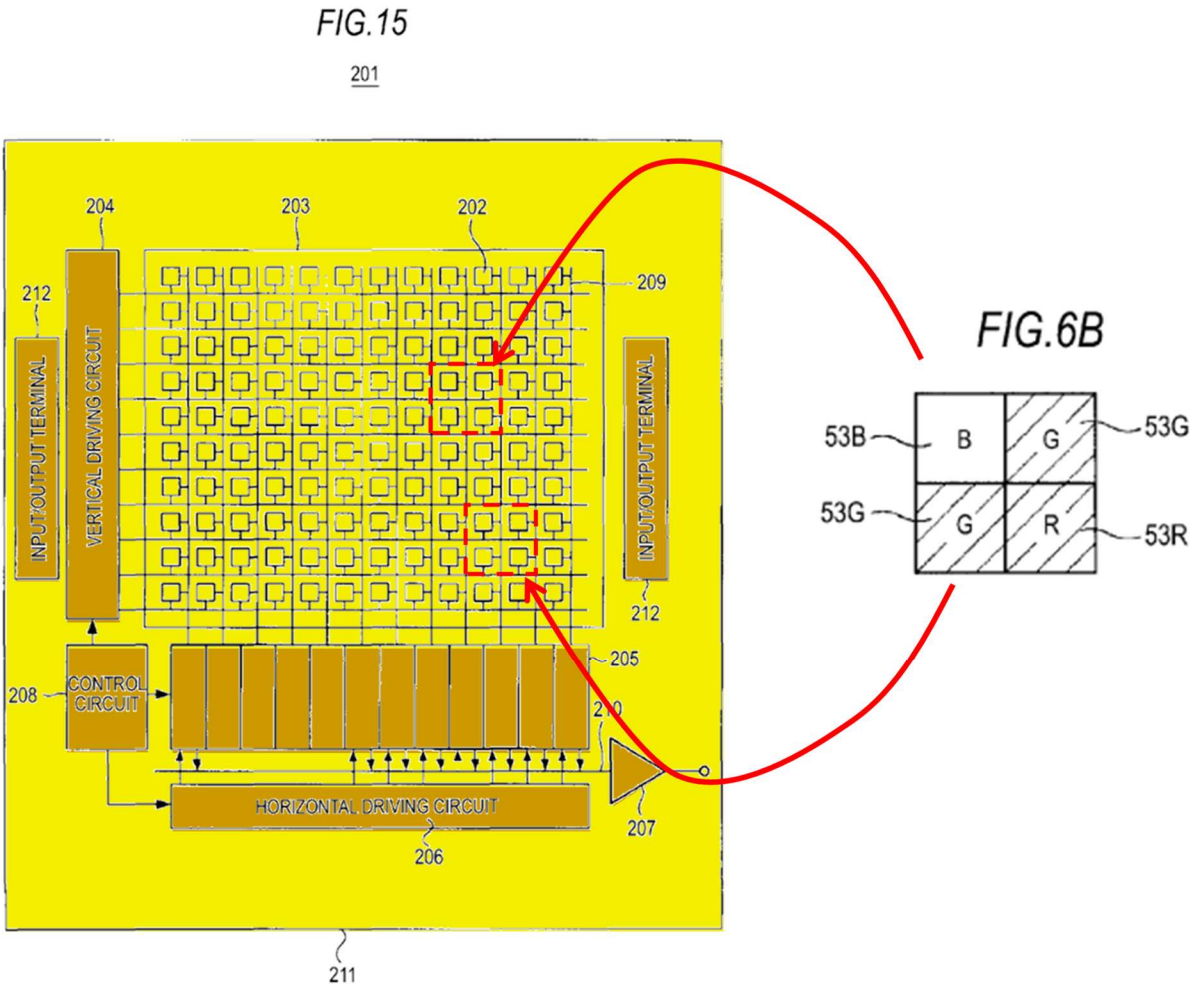


Kuboi, Fig. 6A (modified). A POSITA would have understood that, in the *Kuboi-Vasylyev-1* imaging device, single port 14—configured as an elongated hole aligned with the light-receiving surface—would be formed on blue pixel 53B, extending through the full thickness d_1 of semiconductor layer 12 and be at least partially filled with *Vasylyev*'s dielectric buffer layer. Lebby, ¶280; VI.B.3. Given

that d_1 = 1.4 μm = 1400 nm, the port extends into pixel 53B to a depth ranging from 100-10,000 nm. *Kuboi*, ¶[94].

Accordingly, a POSITA would have recognized that blue pixel 53B of the *Kuboi-Vasylyev-1* imaging device includes only one elongated hole. Lebby, ¶281. Because this hole is elongated along the light-receiving surface, extends into blue pixel 53B to a 1400 nm depth, and is at least partially filled with a solid dielectric material, it satisfies all the requirements of "the elongated hole" recited in claims [1c] and [1d]. Lebby, ¶281.

Even if it is determined that the term "at least some of the pillars" requires multiple pillars, a POSITA would have understood that pixels 53B, 53G, and 53R would be implemented in *Kuboi*'s imaging device 201 as shown below. Lebby, ¶282; VI.A.1, VI.A.10.a.



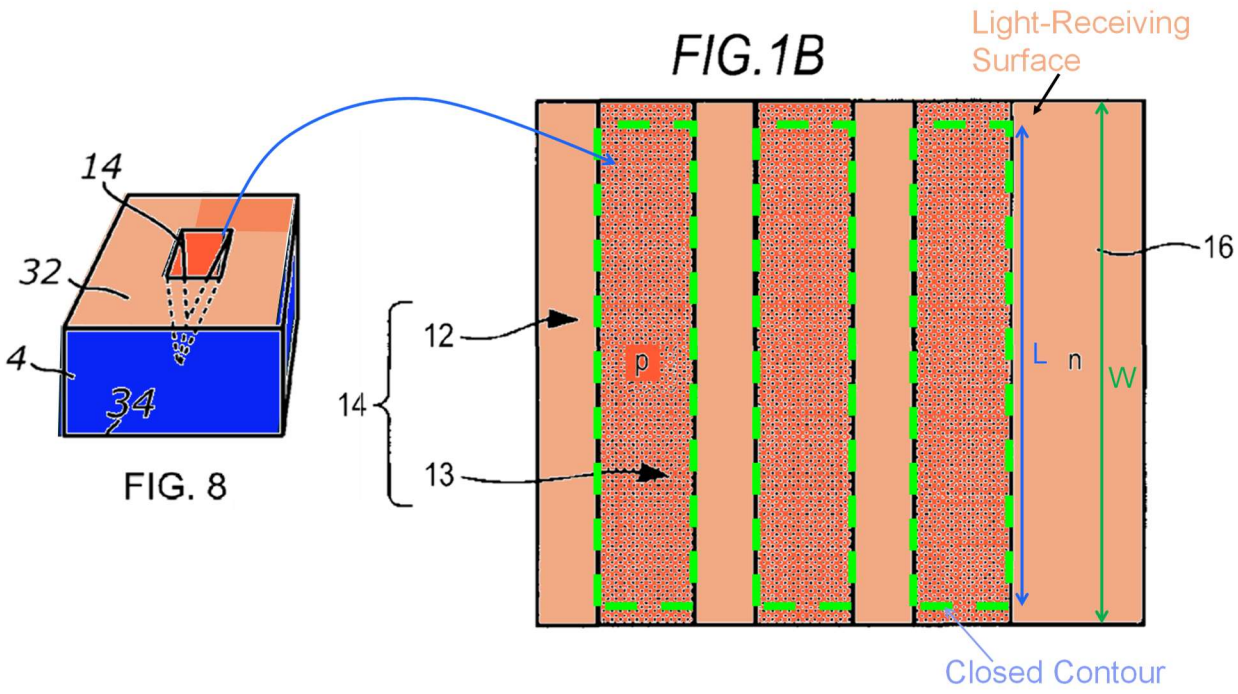
Kuboi, Figs. 6B, 15. Accordingly, a POSITA would have understood that the *Kuboi-Vasylyev-1* imaging device incorporates multiple blue pixels 53B with a single elongated hole. Lebby, ¶283.

7. Claim 5

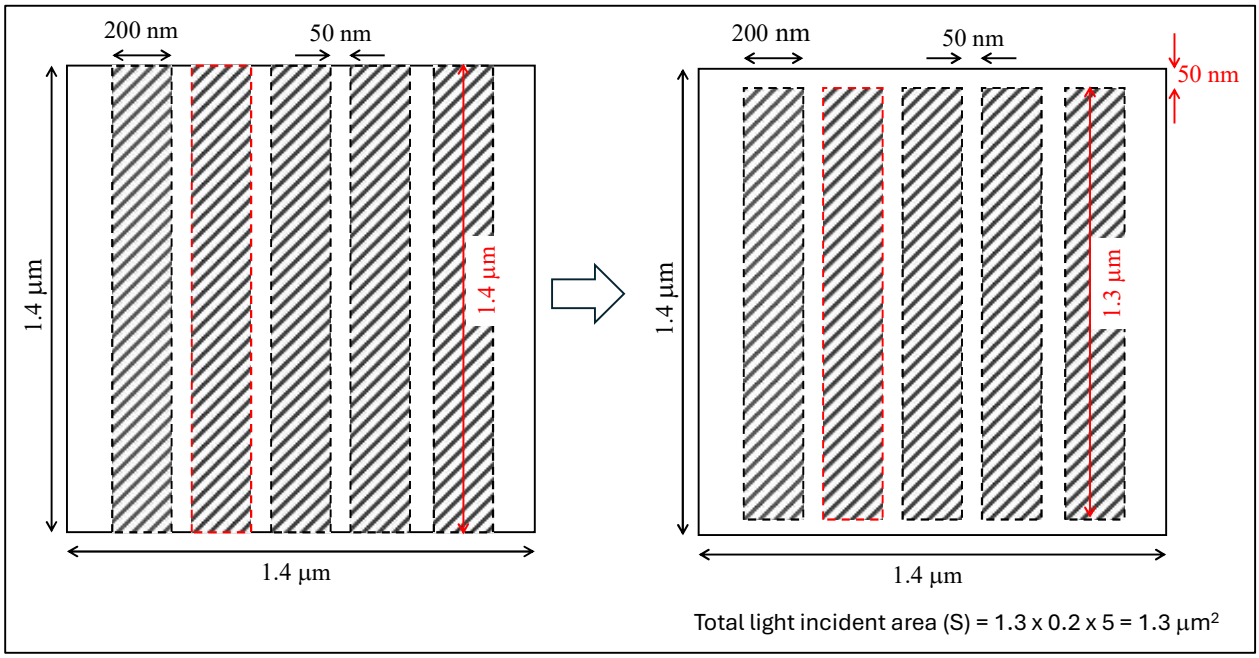
a. "The integrated structure of claim 1, in which the light-receiving surfaces have respective widths, and the elongated holes extend along less than the widths of the light-receiving surfaces of at least some of the pillars in which the holes are fabricated."

Kuboi discloses and/or renders obvious independent claim 1. VI.A.3. *Kuboi* in view of *Vasylyev* renders obvious this additional limitation. Lebby, ¶¶284-293.

As explained above, based on *Kuboi* and *Vasylyev*'s teachings, it would have been obvious to a POSITA to extend holes 38 in *Kuboi*'s green and red pixels (53G, 53R) along a substantial portion—rather than the full extent—of the light-receiving surface of photoelectric conversion portion 14 to reduce the average distance to the silicon-film interface, increase the interface area, and thereby improve device operating speed. VI.B.4; Lebby, ¶285; *Kuboi*, ¶¶[8], [68], [72]. This is illustrated below:



Vasylyev, Fig. 8 (left); *Kuboi*, Fig. 1B (right). A POSITA would have recognized that, in the resulting *Kuboi-Vasylyev-2* imaging device, the elongated holes in green and red pixels (53G, 53R) extend along a length (L) along less than the widths (W) of the light-receiving surfaces of these pixels (pillars). Lebby, ¶286. This dimensional reduction is illustrated below:



Lebby, ¶¶286-287.

According to Dr. Lebby, even with the reduced hole length, the *Kuboi-Vasylyev-1* imaging device meets the limitations of claim [1h]. Lebby, ¶¶287-293.

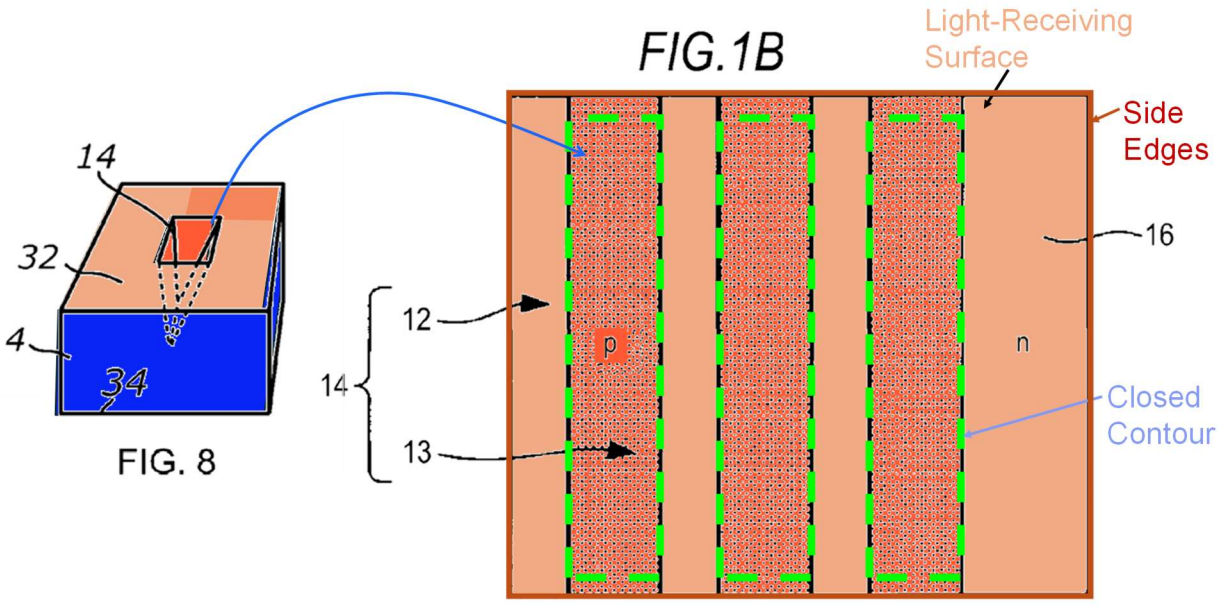
8. Claim 6

a. "The integrated structure of claim 5 in which each of at least some of the elongated holes has at least one closed contour remote from respective side edges of the light-receiving surface in which the hole is fabricated.

Kuboi in view of *Vasylyev* renders obvious these additional limitations. Lebby, ¶¶294-296.

As explained above, a POSITA would have found it obvious to extend holes 38 in *Kuboi*'s green and red pixels (53G, 53R) along a substantial portion of the light-receiving surface, as shown in the figure below, to reduce the average

distance to the silicon-film interface, expand interface area, and increase device speed. VI.B.4, VI.B.7.a; Lebby, ¶¶295-296.



Vasylyev, Fig. 8 (left); *Kuboi*, Fig. 1B (right). A POSITA would have understood that in the resulting the *Kuboi-Vasylyev-2* imaging device, each hole in green and red pixels (53G, 53R) has a closed contour positioned remote from the side edges of the light-receiving surface. Lebby, ¶296.

9. Independent Claim 13

a. [13(pre)] "An integrated structure comprising:"

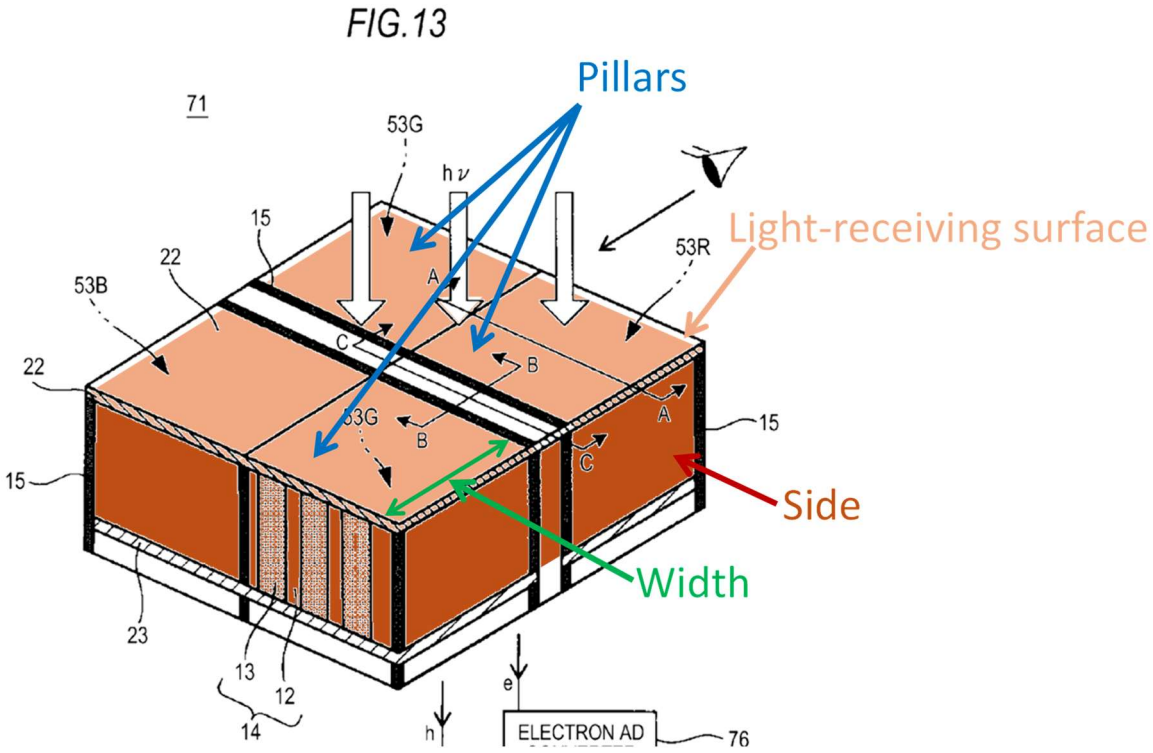
To the extent the preamble is limiting, *Kuboi* discloses this limitation. VI.A.3.a (claim [1(pre)]); Lebby, ¶297.

b. [13a(1)] "an array of pillars comprising Si, Ge, and/or alloyed SiGe semiconductor material,"

As discussed for claim [1a(1)], *Kuboi* discloses this portion of the limitation. VI.A.3.b; Lebby, ¶298.

c. [13a(2)] "wherein at least some of the pillars have respective sides and respective light-receiving surfaces with selected widths and comprise at least one photodetector;"

Kuboi discloses this portion of the limitation. Lebby, ¶¶299-300. As explained for claim [1a(2)], *Kuboi*'s pixels ("pillars") have respective sides and respective light-receiving surfaces and comprise at least one photoelectric conversion portion ("photodetector"). VI.A.3.c.



Kuboi, Fig. 13 (cropped). A POSITA would have understood that each pixel's light-receiving surface has a selected width. Lebby, ¶300.

d. [13b] "wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;"

This limitation is identical to claim [1b]. Lebby, ¶301. *Kuboi* discloses and/or renders obvious this limitation. VI.A.3.d.

e. [13c] "one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars,"

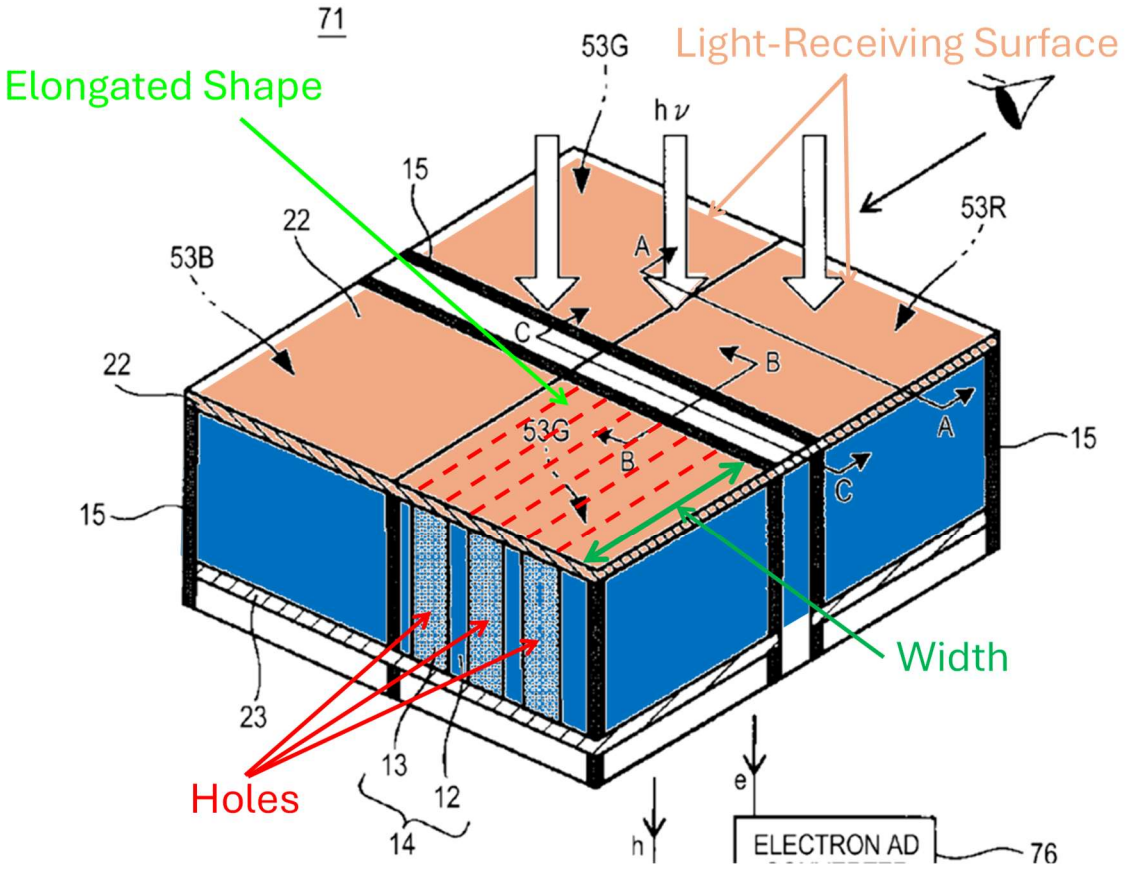
Claim [1c] includes these limitations. Lebby, ¶302. As explained for claim [1c], *Kuboi* discloses these limitations. VI.A.3.e.

f. [13d(1)] wherein each of the holes (i) has an elongated shape extending in length over less than the width of the light-receiving surface in which the hole is fabricated, (ii) has at least one closed contour at the light-receiving surface in which the hole is fabricated,"

Kuboi in view of *Vasylyev* renders obvious this portion of the limitation. Lebby, ¶¶303-308.

As explained for claims [1c] and [1d], each hole 38 in *Kuboi*'s green and red pixels (53G, 53R) has an elongated shape on the light-receiving surface of the respective pixel (i.e., pillar). VI.A.3.e, VI.A.3.f.

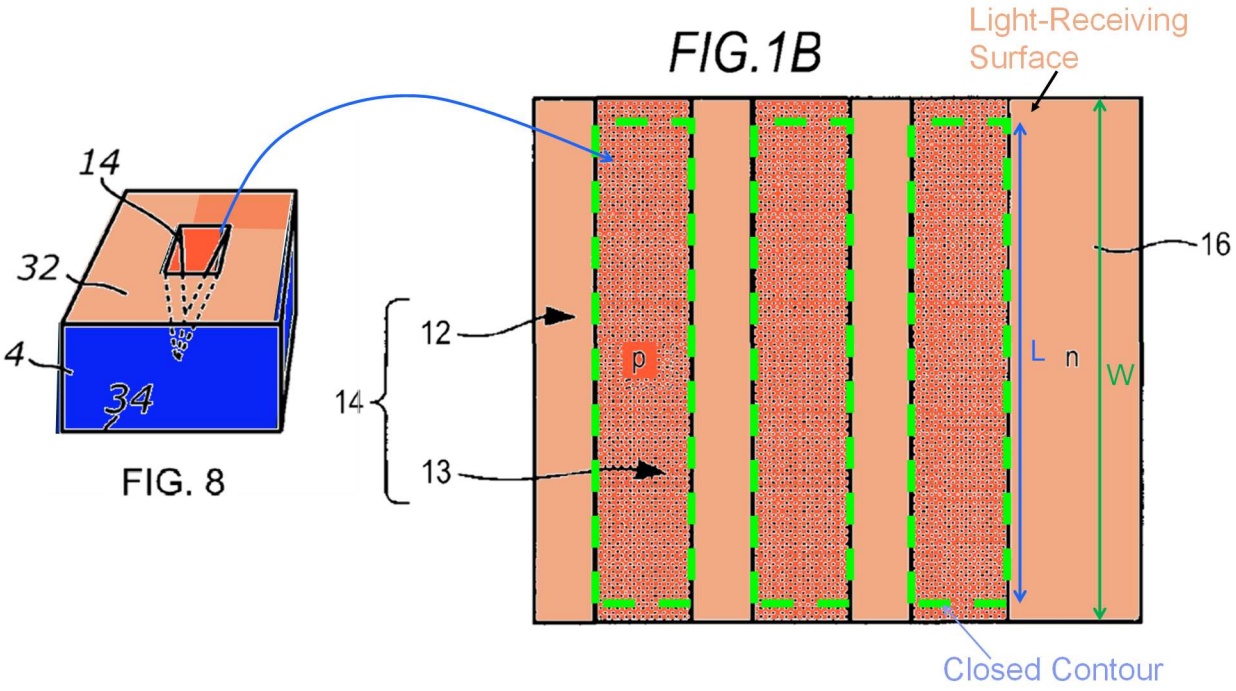
FIG.13



Kuboi, Fig. 13. *Kuboi* does not expressly disclose that the elongated shape of holes 38 extend in length over less than the width of the light-receiving surface in which the hole is fabricated. Lebby, ¶¶304-305.

However, as explained for claim 5 and illustrated below, based on the teachings of *Kuboi* and *Vasylyev*, it would have been obvious to a POSITA to extend holes 38 in *Kuboi*'s green and red pixels (53G, 53R) along a substantial portion—rather than the full extent—of the pixels' light-receiving surface to

reduce the average distance to the silicon-film interface, increase the interface area, and thereby further improve device operating speed. VI.B.4, VI.B.7; Lebby, ¶306.

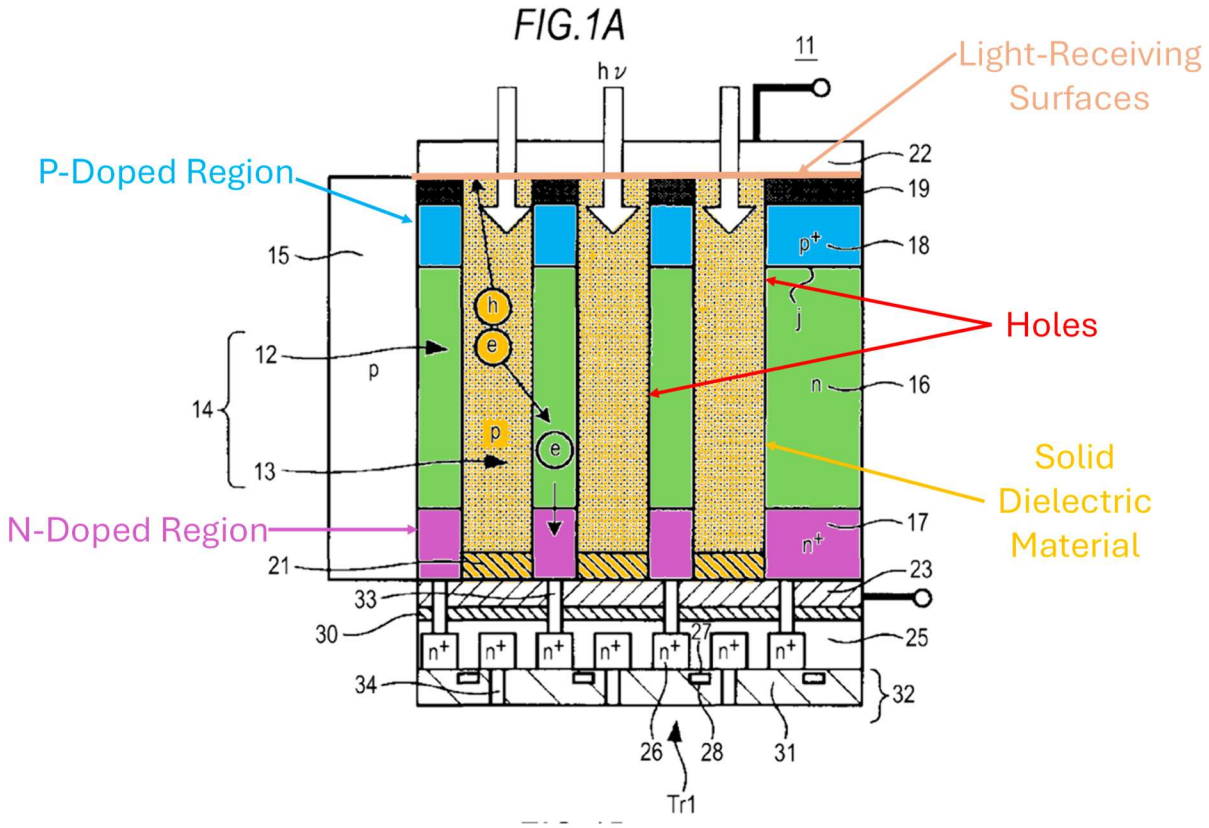


Vasylyev, Fig. 8 (left); *Kuboi*, Fig. 1B (right). A POSITA would have recognized that, in the resulting *Kuboi-Vasylyev-2* imaging device, the elongated holes of green and red pixels (53G, 53R) extend over a length L less than the width W of the light-receiving surface of respective pixels 53G, 53R (pillars). Lebby, ¶307.

As explained for claim 6, a POSITA would have understood that, in the *Kuboi-Vasylyev-2* imaging device, the elongated holes in green and red pixels (53G, 53R) have a closed contour on the light-receiving surface in which the hole is fabricated. VI.B.8.a; Lebby, ¶308.

g. [13d(2)] "([iii]) extends into the pillar in which the hole is fabricated to a depth of 100 to 10000 nm, and (iv) is filled at least partly with solid dielectric material;"

Kuboi discloses this portion of the limitation. Lebby, ¶¶309-310. As explained for claim [1c] and illustrated below, each hole 38 in *Kuboi*'s green and red pixels (53G, 53R) extends into the pixel by a depth d_1 of "about 1.4 μm" (i.e., 1400 nm). VI.A.3.e; *Kuboi*, ¶[94]; Lebby, ¶309.



Kuboi, Fig. 1A. As also explained for claim [1c], in *Kuboi*, holes 38 are filled with electron blocking film 21 and photoelectric conversion films 13, both of which are composed of a solid dielectric materials. VI.A.3.e; *Kuboi*, ¶¶[73], [91].

h. [13e] "side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;"

This limitation is identical to claim [1e]. Lebby, ¶311. *Kuboi* discloses this limitation. VI.A.3.g.

i. [13f] "a solid dielectric material forming a base dielectric region for the array;"

This limitation is identical to claim [1f]. Lebby, ¶312. *Kuboi* discloses and/or renders obvious this limitation. VI.A.3.h.

j. [13g] "electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;"

This limitation is identical to claim [1g]. Lebby, ¶313. *Kuboi* discloses this limitation. VI.A.3.i.

k. [13h] "wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the holes; and"

This limitation is substantively the same as claim [1h]. Lebby, ¶314. *Kuboi* discloses and/or renders obvious this limitation. VI.A.3.j.

l. [13i] "wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission."

This limitation is identical to the additional limitation of claim 9, and *Kuboi* discloses it for the same reasons. VI.A.8.a; Lebby, ¶315.

10. Claim 14

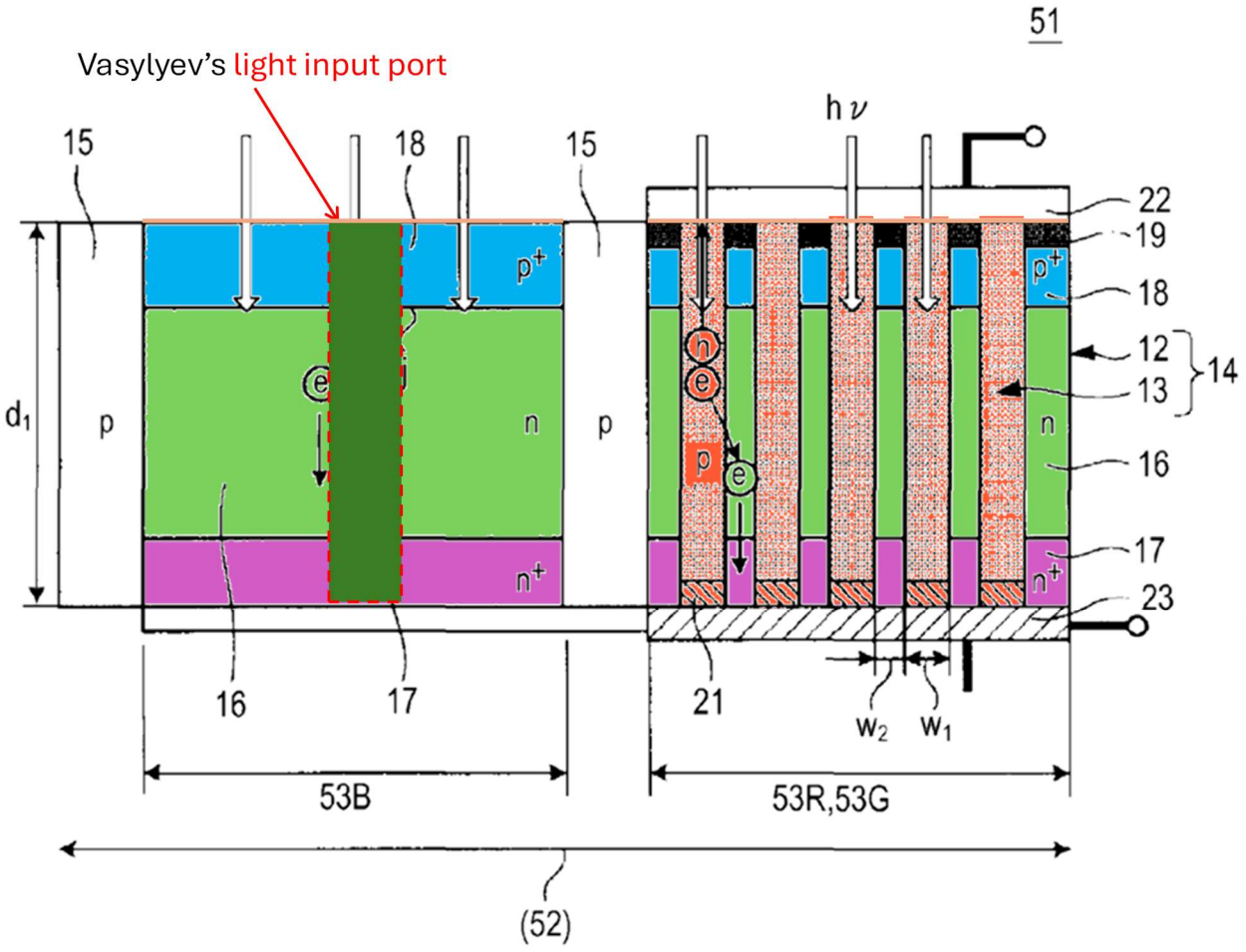
a. "The integrated structure of claim 13, in which each of at least some of the pillars has only one of the elongated holes fabricated therein."

Kuboi in view of *Vasylyev* renders obvious these additional limitations. Lebby, ¶¶316-318.

As previously explained, in addition to modifying holes 38 in *Kuboi*'s green and red pixels (53G, 53R) such that they extend across a substantial portion—rather than the entire length—of the light-receiving surface, a POSITA would have found it obvious to incorporate a single light input port 14 in the blue pixel 53B to reduce blue light reflection and enhance light absorption and energy conversion efficiency, resulting in the *Kuboi-Vasylyev-3* imaging device. VI.B.5; VI.B.9.f-VI.B.9.g (claims [13d(1)]-[13d(2)]); Lebby, ¶317. Based on *Vasylyev*'s teachings, the single light input port 14 in the *Kuboi-Vasylyev-3* imaging device is an elongated trench that extends along a substantial portion —but not the entirety—of the light-receiving surface, penetrates the full 1400 nm thickness (d_1) of the

semiconductor layer 12 of pixel 53B, and is encapsulated by *Vasylyev*'s transparent buffer layer 30. VI.B.5; Lebby, ¶317. This is further illustrated below.

FIG.6A



Kuboi, Fig. 6A (modified).

Since the single port 14 in blue pixel 53B of the *Kuboi-Vasylyev-3* imaging device has an elongated shape that spans less than the full width of its light-receiving surface, forms a closed contour on that surface, extends into the pixel to a depth of 1400 nm, and is at least partially filled with solid dielectric material, it

also satisfies the requirements of claims [13d(1)] and [13d(2)]. Lebby, ¶318; VI.B.5, VI.B.9.f-VI.B.9.g.

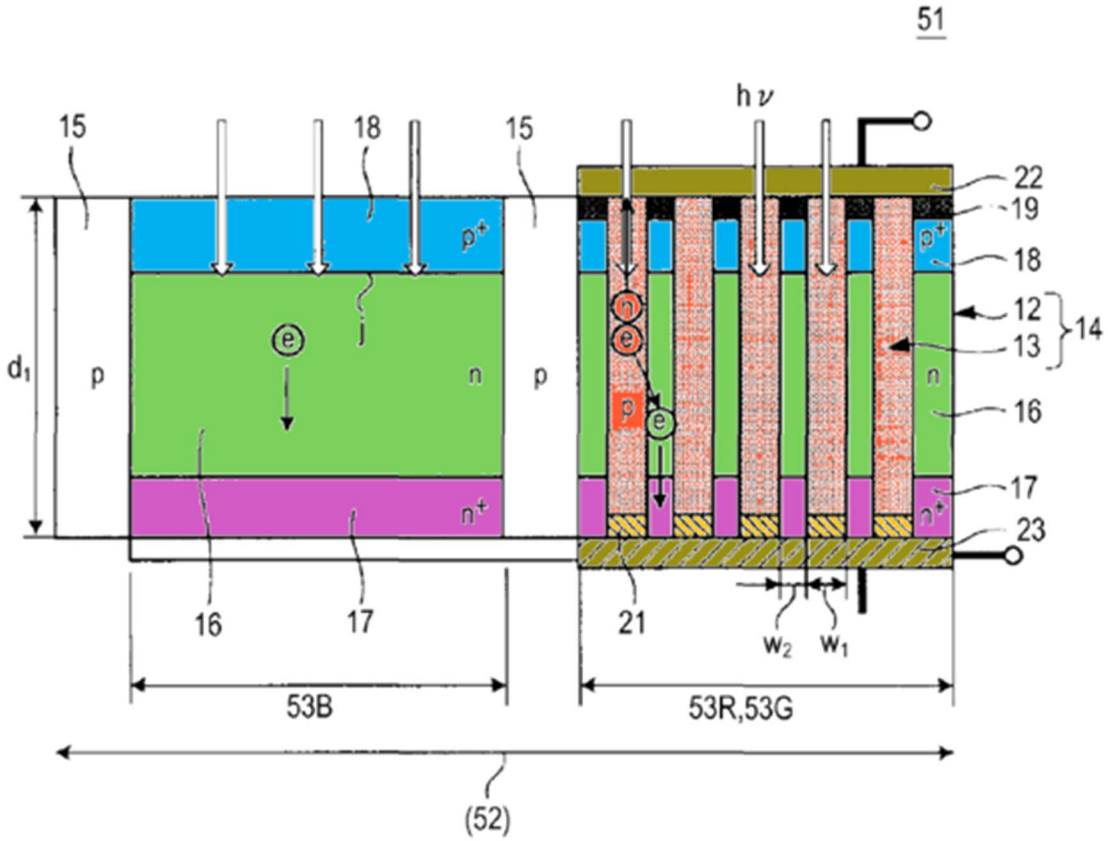
11. Claim 15

a. "The integrated structure of claim 13, in which each of at least some of the pillars has at least two of the elongated holes."

Kuboi in view of *Vasylyev* renders obvious these additional limitations. Lebby, ¶¶319-321.

Kuboi discloses that a "plurality of vertical holes 38 are formed at necessary intervals," and "organic photoelectric conversion film 13 is deposited so as to be embedded in the vertical holes 38." *Kuboi*, ¶¶[72]-[73]. As explained for claims [1d] and [13d(1)], these holes have an elongated shape. VI.A.3.f, VI.B.9.f. In green and red pixels (53G, 53R) below, as illustrated below, "[f]ive organic photoelectric conversion films 13 are disposed in the semiconductor layer 12." *Kuboi*, ¶[94].

FIG.6A



Kuboi, Fig. 6A. Accordingly, in the *Kuboi-Vasylyev-2* imaging device, green and red pixels (53G, 53R) (pillars) have at least two of the elongated holes. Lebby, ¶¶320-321.

12. Claim 16

a. "The integrated structure of claim 13, in which each of at least some of the photodetectors includes at least one of the holes."

Kuboi in view of *Vasylyev* renders obvious these additional limitations. Lebby, ¶322. As explained for claim 15, in the *Kuboi-Vasylyev-2* imaging device, green and red pixels (53G, 53R) (pillars) have at least two of the elongated holes.

Supra VI.B.11.a. In *Kuboi*, green pixel 53G and red pixel 53R are each formed by photoelectric conversion portion 14 (photodetector). *Kuboi*, ¶[90]. Photoelectric conversion portion 14 includes a plurality of organic material layers 13 embedded in holes. *Kuboi*, ¶¶[55], [71]-[73]. Accordingly, in the *Kuboi-Vasylyev-2* imaging device, photoelectric conversion portions 14 (photodetectors) of green pixel 53G and red pixel 53R include at least one of the holes. Lebby, ¶322. Additionally, as explained for claim 14, the photoelectric conversion portion of the blue pixel 53B of the *Kuboi-Vasylyev-3* imaging device also includes one of the holes. VI.B.10.a.

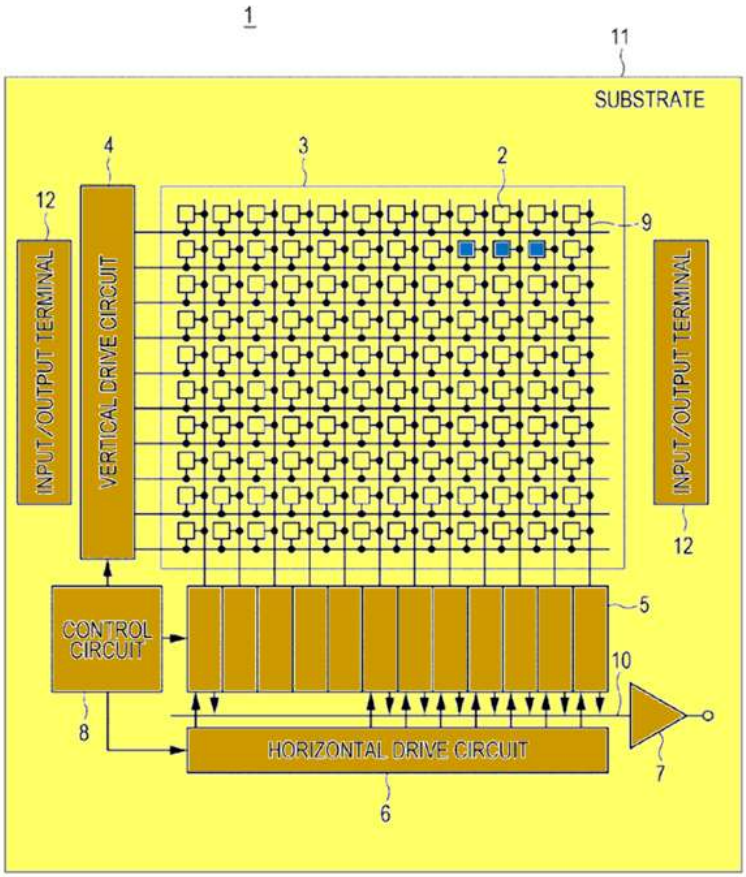
C. Ground 3: Claims 1-3 and 7-12 Are Obvious Over *Kuboi* in View of *Shinohara*

1. Overview of *Shinohara*

Shinohara discloses "a solid-state imaging device which suppresses the generation of white spots and dark current and the occurrence of color mixture and which improves the sensitivity." *Shinohara*, ¶[13]. *Shinohara* discloses "one example of a MOS solid-state imaging device." *Shinohara*, ¶[51]. Solid-state imaging device 1 "includes a pixel region (so-called imaging region) 3 in which a plurality of pixels 2 each having a photoelectric conversion portion is regularly arranged in a semiconductor substrate 11, such as a silicon substrate, in a two-dimensional matrix and a peripheral circuit portion." *Id*. *Shinohara* discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring

layer *on the same substrate*. *Shinohara*, ¶¶[68]-[89]. "The peripheral circuit portion includes so-called logic circuits, such as a vertical drive circuit 4, a column signal processing circuit 5, a horizontal drive circuit 6, an output circuit 7, and a control circuit 8." *Shinohara*, ¶[52]; Lebby, ¶¶101-106. These features are illustrated below:

FIG. 1



Shinohara, Fig. 1.

2. *Kuboi* and *Shinohara* Are Analogous to the '948 Patent

Kuboi and *Shinohara* are analogous art to the '948 Patent because, like the '948 Patent, *Kuboi* and *Shinohara* also aim to improve the light absorption efficiency of their respective imaging devices. Lebby, ¶323. The '948 Patent is directed to techniques for enhancing photon absorption. '948 Patent, Abstract. Similarly, *Kuboi* is directed to a solid-state imaging device in which light absorption efficiency is increased to improve sensitivity. *Kuboi*, ¶[9]. Likewise, *Shinohara* discloses a solid-state imaging device that improves sensitivity by improving a pixel's light absorption, thereby reducing leakage of charge into an adjacent pixel. *Shinohara*, ¶¶[12]-[13]; Lebby, ¶323.

3. Motivation to Apply *Shinohara*'s Monolithic Integration Teachings in in *Kuboi*

A POSITA would have been motivated to implement *Shinohara*'s teaching of monolithic integration of the array of pixels with pixel transistors and electronic circuits for signal processing and transmission in *Kuboi*'s imaging device. Lebby, ¶¶324-328. Indeed, the integration of photodetectors, pixel transistors, and signal processing circuitry on a single substrate to form a single-chip device was known long before the purported invention date. Lebby, ¶¶324-328.

Kuboi discloses forming a pixel region and a peripheral circuit portion, including logic circuits, input and output circuits, and a control circuit on a

substrate. *Kuboi*, ¶¶[48]-[49], [69], [78]. This substrate "may be created in advance and be bonded to the semiconductor substrate on which the semiconductor region 25 having the pixel transistors, the multilayer wiring layer 32, the lower electrode 23, and the like are formed." *Kuboi*, ¶[78]. *Shinohara* discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring layer ***on the same substrate***. *Shinohara*, ¶¶[68]-[82]; Lebby, ¶325.

A POSITA would have understood that including the pixel region, peripheral circuit portion, pixel transistors, and wiring layer on the same substrate (i.e., monolithically integrating) provides several engineering and performance advantages. Lebby, ¶326. By integrating these components within a single silicon substrate, the fabrication process becomes more streamlined and cost-effective, allowing manufacturers to leverage established CMOS technology. *Id.* (citing *Hasegawa*, ¶[9]; Ex-1021, Abstract; Ex-1022, 2; *NXP*, ¶¶[16], [32], [37]). This configuration also enables a more compact design, which is particularly beneficial for applications where space constraints matter, such as mobile devices and embedded systems. *Id.* Electrically, the close proximity between photodiodes and their corresponding transistors minimizes parasitic capacitance and signal delay, resulting in faster charge transfer and improved readout speed. *Hasegawa*, ¶[9]; Lebby, ¶326. Furthermore, this single-substrate approach ensures efficient

electrical coupling, enhancing overall signal integrity. *Hasegawa*, ¶[9]; Lebby, ¶326.

It would have been obvious to a POSITA to apply *Shinohara*'s monolithic integration teachings to *Kuboi* by forming the pixel transistors, multilayer wiring layer 32, array of pixels 201, and logic circuits 204-208 of the peripheral circuit portion on a single substrate to create a monolithically integrated structure[7], motivated by the opportunity to streamline fabrication, lower costs, and enhance electrical performance. Lebby, ¶327. A POSITA would have recognized that applying *Shinohara*'s monolithic integration teachings to *Kuboi* involves nothing more than the use of a known technique—forming the pixel region and all associated electronic circuitry on the same substrate—to improve a similar device—*Kuboi*'s imaging device—in the same way, namely, by improving manufacturing reliability, reducing manufacturing cost and package size, reducing signal attenuation, reducing noise, and improving high-bandwidth performance of *Kuboi*'s device. *Id.*

A POSITA would have had a reasonable expectation of success in using *Shinohara*'s teachings to manufacture *Kuboi*'s imaging device. Lebby, ¶328.

[7] This Petition refers to *Kuboi*'s integrated structure as modified by *Shinohara*'s teachings as the *Kuboi-Shinohara* integrated structure.

Given that both *Kuboi* and *Shinohara* disclose similar CMOS imaging devices that include a pixel region, pixel transistors, and a peripheral circuit portion, manufacturing *Kuboi*'s pixel region and associated electronic circuitry, including *Kuboi*'s pixel transistors, using *Shinohara*'s techniques would have been well within a POSITA's skill. *Id.* A POSITA would have had a reasonable expectation of success in this modification because it merely requires combining well-known prior elements and manufacturing methods already taught by *Shinohara*. *Id*.

4. Independent Claim 1

Kuboi in view of *Shinohara* renders obvious these claims. Lebby, ¶¶329-335.

a. [1(pre)]-[1e], [1g]-[1h]

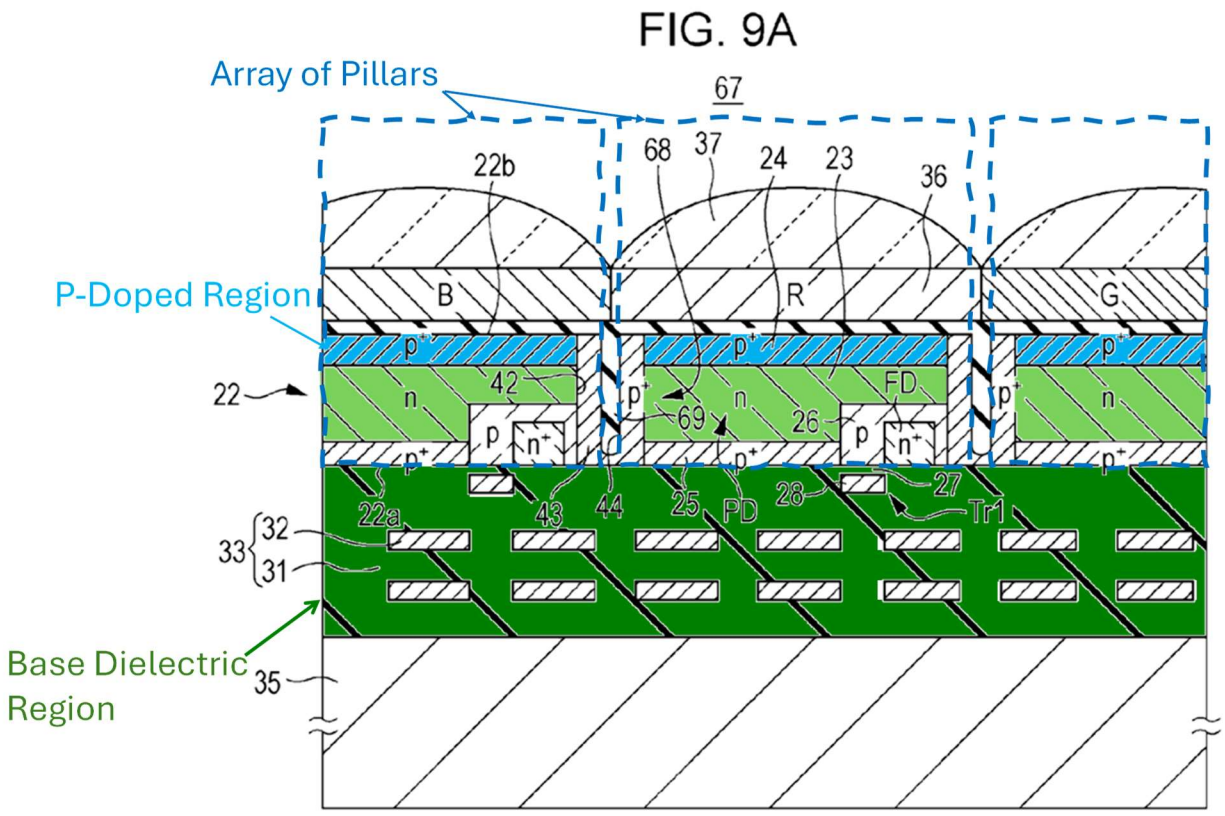
Kuboi discloses or renders obvious these limitations. VI.A.3.a-VI.A.3.g (claims [1(pre)][1e], VI.A.3.i-VI.A.3.j (claims [1g]-[1h]); Lebby, ¶330.

b. [1f]

Kuboi in view of *Shinohara* renders obvious [1e]. Lebby, ¶¶331-335. *Kuboi* discloses a semiconductor substrate that includes semiconductor region 25 with a multilayer wiring layer 32 that includes a plurality of layers of wirings with interlayer insulating film 31 disposed between the wirings. *Kuboi*, ¶¶[61]-[62], [69]; VI.A.3.h (claim [1f]). Further, *Kuboi* discloses bonding the silicon semiconductor substrate with pixels to the semiconductor substrate 25 that includes

multilayer wiring layer 32 with interlayer insulating film 31, with insulating film 30 disposed between the substrate with the pixels and semiconductor substrate 25. *Kuboi*, ¶¶[70], [61]-[62], [69]. Thus, *Kuboi* discloses bonding a first substrate, including insulating film 31 with a second substrate including *Kuboi*'s image sensor and peripheral circuits to form its imaging device. Lebby, ¶332.

Shinohara discloses forming multilayer wiring layer 33, including wires 32 and interlayer insulating film 31, on the same substrate 22 on which pixels B, R, G are formed. *Shinohara*, ¶¶[82], [68]-[89]; VI.C.1. *Shinohara*'s interlayer insulating film 31 is a base dielectric region because it is disposed at the base of *Shinohara*'s pixels B, R, G. *Shinohara*'s base dielectric region is illustrated below.



Shinohara, Fig. 9A; Lebby, ¶¶333-334.

Although *Shinohara* does not disclose the material used to make its semiconductor insulating films (30 and/or 31), a POSITA would have understood that insulating films for separating wires from each other or from an electrical contact, like *Kuboi*'s insulating films 30 or 31 or *Shinohara*'s insulating film 31, constitute silicon oxide or silicon nitride, which are dielectric materials, or at least would have been motivated to use silicon oxide or silicon nitride because these materials can be fabricated using standard silicon fabrication processes and because these materials provide good barriers to impurity and moisture diffusion.

Lebby, ¶334 (citing Ex-1012, 4-5, 20-21, 23, 34; Ex-1013, 34-35; Ex-1027, ¶¶[13]-[14]). Thus, a POSITA would have found it obvious to form *Shinohara*'s insulating film 31 (i.e., base dielectric material) of a solid dielectric material like silicon oxide or silicon nitride. *Id.* A POSITA would also have a reasonable expectation of success in making *Shinohara*'s insulating film 31 with a solid dielectric material because methods of formation with such materials in semiconductor fabrication were well known in the art before the '948 Patent. *Id.* (citing Ex-1012, 20-21, 23; Ex-1013, 34-35).

As explained above, a POSITA would have found it obvious to modify *Kuboi* in view of *Shinohara* to form the *Kuboi-Shinohara* integrated structure in which *Kuboi*'s array of pillars (i.e., photodetectors) and Si electronic devices are formed on the same substrate. VI.C.3. A POSITA would have also understood that applying *Shinohara*'s monolithic integration to form the *Kuboi-Shinohara* integrated structure would result in forming *Kuboi*'s insulating film 30 and interlayer insulating film 31 to be formed on the same substrate as *Kuboi*'s array of pillars (i.e., photodetectors). Lebby, ¶335. A POSITA would have further understood that in the *Kuboi-Shinohara* integrated structure, *Kuboi*'s insulating films 30 and 31 would be disposed below *Kuboi*'s array of pillars as illustrated in *Kuboi*'s Figure 1A. *Id.* Moreover, because *Kuboi*'s insulating films 30 and 31 are made of solid dielectric material, *Kuboi*'s insulating film 30 and/or 31 would form

the claimed base dielectric region below *Kuboi*'s array of pillars in the *Kuboi-Shinohara* integrated structure. *Id.*

5. Claim 2

Kuboi in view of *Shinohara* renders obvious the additional limitations of claim 2. Lebby, ¶¶336-340.

Kuboi teaches that the pixel array 201 and the peripheral circuit portion—including logic circuits 204-208 comprising Si electronic devices—are formed on a common substrate. VI.A.4.a (claim 2, Ground 1); *Kuboi*, ¶¶[48]-[49], [78]. In the *Kuboi-Shinohara* imaging device, the pixel array is monolithically integrated with the peripheral circuit portion. VI.C.3. Accordingly, a POSITA would have recognized that the pixel array is monolithically integrated with Si electronic devices in the *Kuboi-Shinohara* integrated structure. Lebby, ¶¶336-340.

6. Claims 3 and 7-8

Kuboi in view of *Shinohara* renders obvious these claims. Lebby, ¶¶341-342.

As explained above, a POSITA would have found it obvious to apply *Shinohara*'s teachings on monolithic integration to *Kuboi* by forming the pixel transistors, multilayer wiring layer 32, pixel array 201, and logic circuits 204-208 on a common substrate to form the *Kuboi-Shinohara* integrated structure. VI.C.3; Lebby, ¶342. For the same reasons previously set forth with respect to claims 3 and

7-8, the *Kuboi-Shinohara* integrated structure satisfies the limitations of these claims. VI.A.5, VI.A.6-VI.A.7.

7. Claim 9

Kuboi in view of *Shinohara* renders obvious the additional limitations of claim 9. Lebby, ¶¶343-344.

As discussed for claim 2 above, in the *Kuboi-Shinohara* integrated structure, the pixel array is monolithically integrated with logic circuits 204–208 comprising Si electronic devices. VI.C.5. *Kuboi*'s column signal processing circuits 205 perform signal processing on signals from pixels 202 and forward them to output circuit 207, which conducts further processing and outputs the final signals. *Kuboi*, ¶¶[49], [52]-[54]; VI.A.8. A POSITA would therefore have recognized that the pixel array is monolithically integrated with Si electronic devices for signal processing and transmission of electrical signals in the *Kuboi-Shinohara* integrated structure. Lebby, ¶344.

8. Claim 10

Kuboi in view of *Shinohara* renders obvious the additional limitations of claim 10. Lebby, ¶¶345-346.

As explained for claim 9 above, a POSITA would have recognized that, in the *Kuboi-Shinohara* integrated structure, the pixel array is monolithically integrated with Si electronic devices for transmission of electrical signals. VI.C.7;

Lebby, ¶346. As explained for claim 10 of Ground 1, these transmitted electrical signals are related to accumulations of the charge carriers in the photoelectric conversion portions of at least some of the pixels. VI.A.9.

9. Claims 11-12

Kuboi in view of *Shinohara* renders obvious these claims. Lebby, ¶¶347-348.

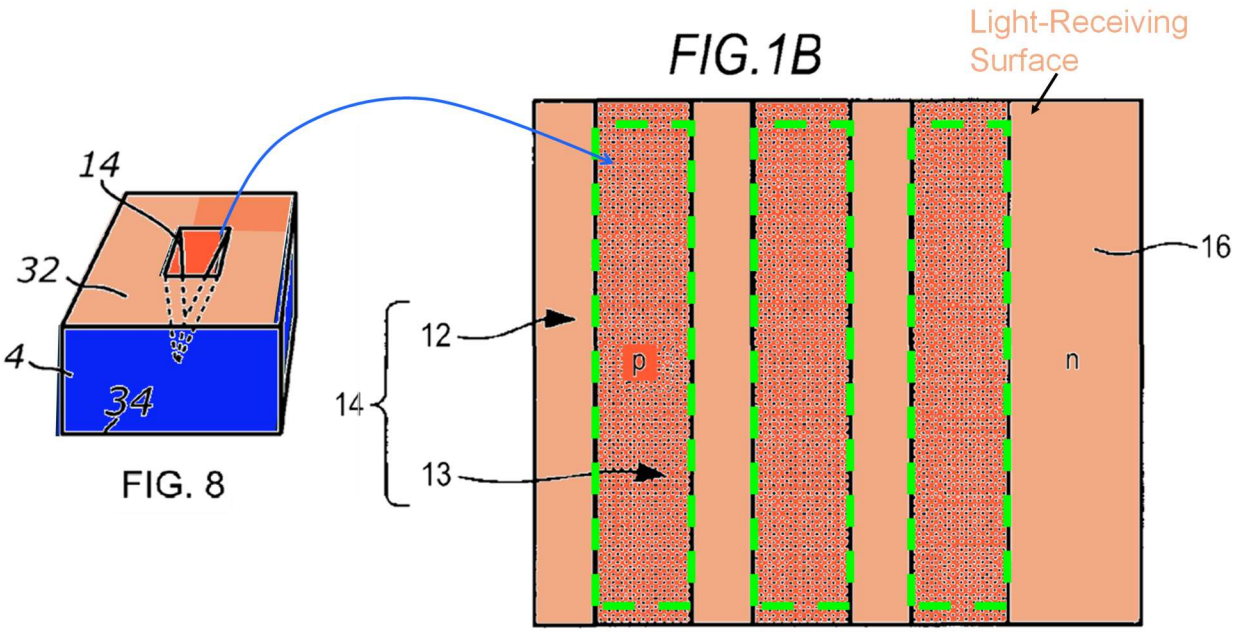
As explained above, a POSITA would have found it obvious to apply *Shinohara*'s teachings on monolithic integration to *Kuboi* to form the *Kuboi-Shinohara* integrated structure. VI.C.3; Lebby, ¶348. For the same reasons set forth with respect to claims 11-12 under Ground 1, the *Kuboi-Shinohara* integrated structure satisfies the limitations of these claims. VI.A.10-VI.A.11.

D. Ground 4: Claims 4-6 and 13-16 Are Obvious Over *Kuboi* in View of *Vasylyev* and *Shinohara*

1. Motivation to modify *Kuboi* in view of *Vasylyev* and *Shinohara*

As previously discussed, *Kuboi*, *Vasylyev*, and *Shinohara* are analogous art to the '948 Patent. VI.A.2, VI.B.2, VI.C.2. As discussed above in VI.B.4, in light of *Vasylyev*'s teachings, a POSITA would have found it obvious to modify *Kuboi*'s green and red pixels (53G, 53R) by extending holes 38 in photoelectric conversion portions 14 along a substantial portion—rather than the entire extent—of their

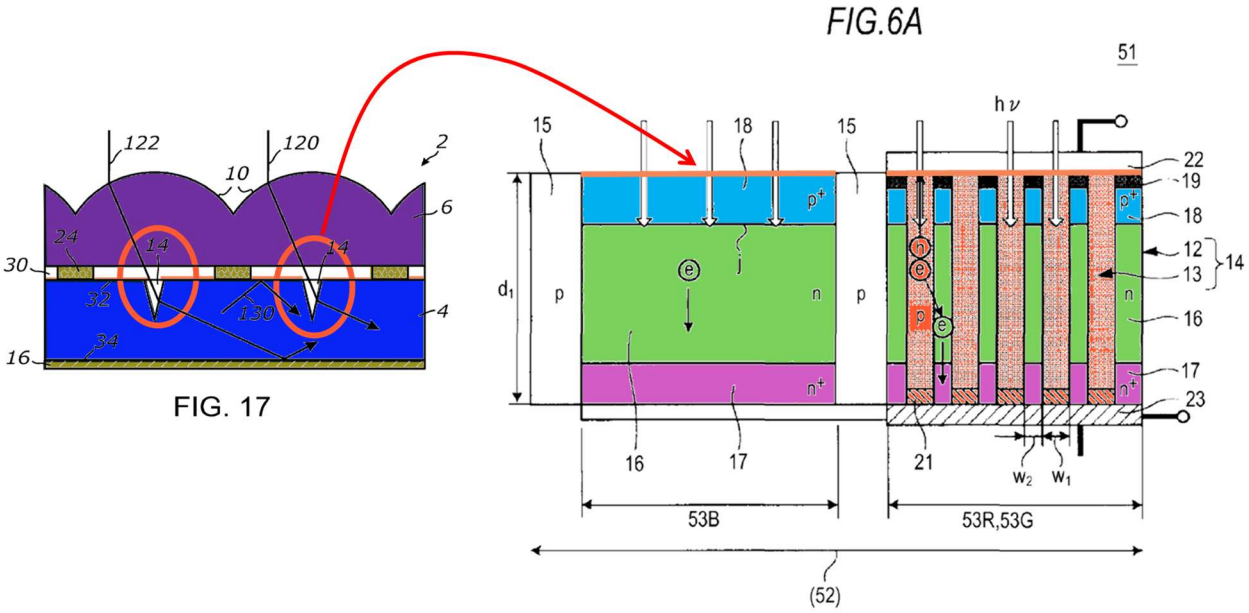
light-receiving surfaces to form the *Kuboi-Vasylyev*-2 imaging device. Lebby, ¶¶349-353.



Vasylyev, Fig. 8 (left); *Kuboi*, Fig. 1B (right). Based on *Kuboi*'s disclosure, a POSITA would have known that this modification to green and red pixels (53G, 53R) would reduce the average distance that photogenerated electrons in organic film 13 must travel to reach the silicon-film interface, increase the interface area, and thereby enhance the imaging device's operating speed. VI.B.4; *Kuboi*, ¶¶[8], [67]-[68]; Lebby, ¶350.

As explained in VI.B.5, to reduce reflection of blue light and increase optical efficiency, a POSITA would also have found it obvious to additionally incorporate a single light input port 14—configured as an elongated, narrow trench extending

through the full thickness of semiconductor layer 12 and at least partially filled with a dielectric material—into blue pixel 53B of the *Kuboi-Vasylyev*-2 imaging device and form the *Kuboi-Vasylyev*-3 imaging device. Lebby, ¶351; VI.B.10.a. This is illustrated below:



Vasylyev, Fig. 17 (left); *Kuboi*, Fig. 6A (right).

In addition to applying *Vasylyev*'s teachings to the blue, green, and red pixels (53B, 53G, 53R) in *Kuboi*'s imaging device, a POSITA would have found it obvious to further incorporate *Shinohara*'s teachings in the *Kuboi-Vasylyev*-3 imaging device to form a *Kuboi-Vasylyev-Shinohara* imaging device to streamline fabrication, reduce fabrication cost, and improve electrical performance. Lebby, ¶352; VI.C.3. A POSITA would have recognized that the *Kuboi-Vasylyev-Shinohara* imaging device would be a monolithically integrated device with the

pixel array 201 and associated electronic circuits—such as pixel transistors, multilayer wiring layer 32, and peripheral logic circuits 204-208—on a single substrate with *Shinohara*'s interlayer insulating film 31 as a base dielectric region. VI.C.3, VI.C.4.b; Lebby, ¶352. A POSITA would have had a reasonable expectation of success in combining the known teachings of *Kuboi*, *Vasylyev*, and *Shinohara* as each addresses similar technical challenges and proposes solutions that operate according to well-understood principles and are aimed at improving the same device functionality. VI.B.3-VI.B.5, VI.C.3; Lebby, ¶353.

2. Claims 4-6

Kuboi discloses and/or renders obvious the limitations of independent claim 1. VI.A.3. Claim 4-6 further depend from claim 1, and for the same reasons set forth for claims 4-6 under Ground 2, the *Kuboi-Vasylyev-Shinohara* device satisfies the limitations of these claims. VI.B.6-VI.B.8; Lebby, ¶354.

3. Claim 13

a. [13(pre)]-[13e], [13g]-[13h]

Kuboi in view of *Vasylyev* and *Shinohara* renders obvious these limitations. Lebby, ¶355; VI.B.9.a-VI.B.9.h (claims [13(pre)]-[13e]), VI.B.9.j-VI.B.9.k (claims [13h]-[13i]).

b. [13f]

Kuboi in view of *Vasylyev* and *Shinohara* renders obvious [13f]. Lebby, ¶356. This limitation is identical to claim [1f], and as discussed for claim [1f] in Ground 3, *Kuboi* in view of *Shinohara* renders obvious claim [1f]. VI.C.4.b. *Kuboi* in view of *Vasylyev* and *Shinohara* likewise renders obvious this limitation. Lebby, ¶356.

c. [13i]

This limitation is identical to claim 9, and as discussed above, *Kuboi* in view of *Shinohara* renders obvious claim 9. VI.C.7. *Kuboi* in view of *Vasylyev* and *Shinohara* likewise renders obvious this limitation. Lebby, ¶357.

4. Claims 14-16

Claims 14-16 depend from claim 13. As set forth under Ground 2, the *Kuboi-Vasylyev-3* imaging device satisfies claim 14, VI.B.10, and *Kuboi* satisfies claims 15 and 16. VI.B.11-VI.B.12; Lebby, ¶358. *Kuboi* in view of *Vasylyev* and *Shinohara* also renders obvious these limitations for the same reasons discussed above. Lebby, ¶358.

E. Ground 5: Claims 1-16 Lack Enablement Under §112

Independent claim 1 recites "wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes." Independent

claim 13 recites a similar limitation. As discussed in VI.A.3.j, based on Patent Owner's representations in the '948 Patent, a POSITA would have understood that the absorption of light, at selected visible and infrared wavelength ranges, by at least some of *Kuboi*'s photodetectors with holes would be at least 1.1 times that of like photodetectors lacking said holes.

1. The Claims Are Not Enabled If the Prior Art's Disclosure Is Deemed Insufficient

To the extent Patent Owner contends that the '948 Patent's representations as understood by a POSITA are insufficient to establish that the prior art disclosure in this petition meets any of the 1.1 requirements of any of the claims, the '948 Patent specification necessarily fails to enable such claims under §112(a). Lebby, ¶¶359-360. Relying on Chang-Hasnain (Ex-1033), Patent Owner represents in the '948 Patent that a microstructured pillar hole array having microstructure period Λ and satisfying the relationship $\lambda/n1<\Lambda<\lambda/n2$ forms a high contrast grating (HCG). VI.A.3.j. According to Patent Owner, if the microstructure pillar hole array forms an HCG, then the physical phenomenon of near-wavelength and deep-wavelength result in an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient. VI.A.3.j. But if this is insufficient to know whether a given photodetector with holes would be at least 1.1 times that of like photodetectors

lacking said holes, then the '948 Patent specification does not enable the full scope of claims 1-16. *See* §112(a).

2. Because the Claims Cover Single-Hole Structures, the Full Scope of Claims 1, 4, 13, and 14 Is Not Enabled

The claim language in claims 1 and 13 stating that "one or more holes [] are fabricated … under the light-receiving surface of each of at least some of the pillars" plainly encompasses embodiments in which each pillar includes a single hole. The phrase "one or more" is inclusive of the singular, and the structure of the claim permits configurations where only one hole is present per pillar. Lebby, ¶¶361-362. Furthermore, claims 4 and 14 specify that "at least some of the pillars has only one of the elongated holes." However, the '948 Patent does not enable such embodiments with respect to the claimed 1.1 requirement (VI.A.3.j). Lebby, ¶361.

The specification lacks sufficient guidance to allow a POSITA to make and use an embodiment with a single hole per pillar that achieves the claimed enhancement. Lebby, ¶362. It does not disclose how such a configuration would function to produce the required increase in absorption. *Id*. Instead, the described mechanism for determining increased absorption—such as the high contrast grating (HCG) effect that occurs when the microstructure period Λ satisfies the relationship $\lambda/n_1 < \Lambda < \lambda/n_2$—requires multiple holes arranged with a periodicity Λ,

which is absent in a single-hole embodiment. *Id*. For instance, a POSITA would have anticipated a substantial change in the HCG effect at lower values of the period Λ. Lebby, ¶362 (citing Ex-1051, 1-6). Accordingly, the patent does not enable a POSITA to practice the full scope of claims 1-16, rendering them not enabled under §112(a). *Id*.

3. Because the Claims Cover Millimeter-Sized Pillars, the Full Scope of Claims 1 and 13 Is Not Enabled

Application No. 19/036,506 (the '948 Divisional) is a pending application with claims substantively similar to those in the '948 Patent. *See* Ex-1050, 290-294; Ex-1049. For example, like claim 1 of the '948 Patent, independent claim 18 of the '948 Divisional recites an integrated structure comprising "an array of pillars … includ[ing] photodetectors," where at least some pillars include "P-doped and N-doped regions," "one or more holes" extending to depths of less than 10,000 nm, "wherein the presence of the one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes." Ex-1050, 290. Independent claim 32 contains similar limitations. *Id.*, 293-294.

The Examiner rejected independent claims 18 and 32 for lack of enablement, explaining that the specification does not support the full scope of the claims. Ex-1050, 8. According to the Examiner, the claims encompass "pillars [that] could be

sized to be on the order of magnitude of either millimeter or nanometer sized pillars," which are not disclosed in the application. *Id*. Instead, the specification "specifically centers the pillar dimensions at around 100 micrometers and micrometers in general." *Id*. (citation omitted).

As Dr. Lebby explains, the Examiner's reasoning for claims 18 and 32 of the '948 Divisional applies equally to claims 1 and 13 of the '948 Patent because the claims are substantively similar and are supported by the same disclosure. Lebby, ¶¶363-365. The '948 Patent does not provide sufficient detail for a POSITA to make and use the full scope of claims 1 and 13, which, as noted by the Examiner, encompass millimeter-sized pillars. *Id*. The '948 Patent fails to describe how to make and use an integrated structure with millimeter-sized pillars where "the presence of the one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes." Lebby, ¶¶363-365; *see* '948 Patent, 11:52-12:55, 20:43-64 ("The pillar diameter range from 50-1200 nm (smallest dimension can be 50 and largest dimension 1200 nm)."). Claims 1-16 are thus not enabled under §112(a).

VII. Mandatory Notices

A. Real Parties-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor LLC.

B. Related Matters

Patent Owner W&Wsens Devices, Inc. asserted the '948 Patent in *W&Wsens Devices Inc. v. Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor LLC*, Case No. 2:24-cv-00854-JRG (E.D. Tex.). Patent Owner also asserted U.S. Patent Nos. 10,446,700 ('700 Patent), 12,087,871 ('871 Patent), 11,621,360 ('360 Patent), 9,525,084 ('084 Patent), and 10,468,543 ('543 Patent) in that case, all of which are related to the '948 Patent.

Samsung has filed IPR petitions challenging multiple claims of these five patents—IPR2025-00996 ('700 Patent), IPR2025-00993 ('871 Patent), IPR2025-00994 ('360 Patent), IPR2025-00997 ('084 Patent), and IPR2025-00995 ('543 Patent). All petitions are currently awaiting institution decisions.

C. Lead and Backup Counsel, and Service Information

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Please address all correspondence to counsel at the address above. Petitioner consents to electronic service by email at the above email addresses.

VIII. Grounds for Standing

Petitioner certifies that the ’948 Patent is available for PGR and that Petitioner is not barred or estopped from requesting PGR challenging the patent claims on the grounds identified herein.

IX. Timing

Under 37 C.F.R. §42.202, “[a] petition for a post-grant review of a patent must be filed no later than the date that is nine months after the date of the grant of a patent or of the issuance of a reissue patent.” Petitioner is filing this Petition within nine months of the ’948 Patent’s issue date (March 4, 2025), and this Petition is therefore timely.

X. Conclusion

For the reasons above, Petitioner requests institution of PGR and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Date: August 28, 2025

Respectfully submitted,

By: / Joshua L. Goldberg /
Joshua L. Goldberg
Lead Counsel
Reg. No. 59,369

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, Petitioner certifies that the word count of Petitioner's Petition for Post-Grant Review (exclusive of any table of contents, table of authorities, mandatory notices under §42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 18,676.

Dated: August 28, 2025

By: / Joshua L. Goldberg /
Joshua L. Goldberg
Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§42.6(e) and 42.205(a), the undersigned certifies that on August 28, 2025, a copy of the foregoing **Petition for Post-Grant Review**, **the associated powers of attorney**, and **Exhibits 1001-1056** were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's public Patent Center system for U.S. Patent No. 12,243,948:

Mr. Ivan S. Kavrukov
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