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APPLICATION AS FILED - PART I									
FOR		(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE (\$)		FEE (\$)		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A		N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A				
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		x \$80 =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		x \$240 =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL				
APPLICATION AS AMENDED - PART II									
		(Column 1)		(Column 2)	(Column 3)				
AMENDMENT	09/16/2025	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 13	Minus	** 20	= 0	x \$80 =		0	
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	x \$240 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						PSS			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/TERRANCE R LAWRENCE/			
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The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

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(54) Title of Invention SEMICONDUCTOR DEVICE

(57) Abstract

Problem

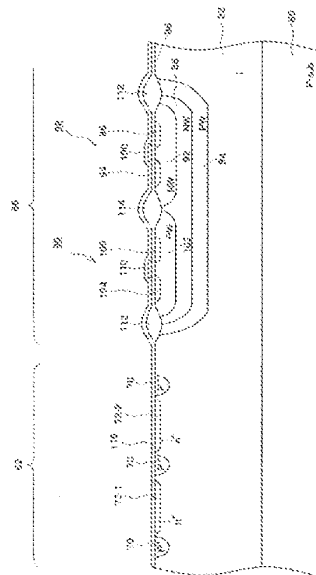
To make it possible to configure a CMOS on the same chip as an photodetection semiconductor element in which a PIN photodiode is provided on a light-receiving part.

Solution

A light-receiving part 62 and a signal-processing circuit part 66 are configured on a semiconductor substrate on which an epitaxial layer 82 is layered onto a P-sub layer 80. A PIN photodiode uses the P-sub layer 80 as an anode, and the epitaxial layer 82, which is between a cathode region 72 and the P-sub layer 80, is configured as the i-layer. In the signal-processing circuit part 66, a P-well 84 is formed at the boundary between an N-well 86 and the epitaxial layer 82, which form a CMOS.

Selected Figure

FIG. 3



CLAIMS

1. A semiconductor device, which comprises a light-receiving part and a circuit part that are formed on a semiconductor substrate that is common thereto, comprising:

a high specific resistance region, which is provided on a principle surface of the semiconductor substrate and is formed with high specific resistance owing to a low impurity concentration;

wherein:

the light-receiving part comprises:

a first electrode region, which is disposed in contact with the high specific resistance region, is a first conductive semiconductor region having a higher impurity concentration than the high specific resistance region, and to which a first voltage is applied; and

a second electrode region, which is disposed in contact with the high specific resistance region, is a second conductive semiconductor region having a higher impurity concentration than the high specific resistance region, and to which a second voltage is applied;

between the first electrode region and the second electrode region is placed in a reverse-bias state owing to the first voltage and the second voltage, and thereby a depletion layer is formed in the high specific resistance region; and

the circuit part comprises:

a circuit-element region, which is provided on the principle surface and is a first conductive semiconductor region on which a circuit element is formed in the interior; and

a junction-boundary region, which constitutes the boundary between the high specific resistance region and the circuit-element region and is a second conductive semiconductor region having a higher impurity concentration than the high specific resistance region.

2. The semiconductor device according to claim 1, wherein the high specific resistance region is the second conductive semiconductor region.

3. The semiconductor device according to claim 1 or 2, wherein the high specific resistance region has a specific resistance of 200 $\Omega \cdot \text{cm}$ or more.

4. The semiconductor device according to any one of claims 1–3, wherein the high specific resistance region is an epitaxial growth layer.

5. The semiconductor device according to any one of claims 1–4, wherein:

the second electrode region is an underlayer of the high specific resistance region; and

the first electrode region and the circuit-element region are each formed on surface-layer portions of the high specific resistance region.

6. The semiconductor device according to any one of claims 1–4, wherein the first electrode region, the second electrode region, and the circuit-element region are each formed on surface-layer portions of the high specific resistance region.

7. The semiconductor device according to claim 6, wherein another second electrode region is an underlayer of the high specific resistance region.

DETAILED DESCRIPTION OF THE INVENTION

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device that comprises a light-receiving part, which utilizes a depletion layer extending across a semiconductor region of high specific resistance, and generates signals by way of photoelectric conversion.

BACKGROUND ART

[0002]

Optical discs, such as CDs (compact disks) and DVDs (digital versatile disks) have, in recent years, come to occupy a major position in the marketplace as information recording media. Playback devices for these optical discs radiate laser light along a track of the optical disc via an optical pickup mechanism and detect the reflected light thereof. Furthermore, recorded data is played back based on the variation of the reflected light intensity.

[0003]

10 An optical disc-playback device performs servo control to control the positional relationship between the optical pickup mechanism and the optical disc while detecting data based on the reflected light. Specifically, tracking servo is performed for radiating the laser light along the center line of the track, and focusing servo is performed to maintain a constant distance between the optical disc and the optical pickup mechanism. In focusing servo control, for example, variable control is performed to vary the location of the optical pickup mechanism, using an actuator, based on an output signal from a photodetector that detects the laser reflected light, thereby maintaining a constant distance d to the optical disc. Thereby, fluctuation in the reflected light quantity in response to shifts in the focus of the radiated light on the front surface of the optical disc is curtailed, and thereby noise superimposed on the received-light signals is suppressed.

[0004]

20 To obtain information for this kind of servo control, something that partitions a reflected-light image into a plurality of blocks and receives light is used as the photodetector. FIG. 9 includes schematic diagrams that show a light-receiving part of the photodetector and the reflected-light image on the light-receiving part. The laser reflected light passes through a cylindrical lens and impinges on the photodetector. According to the principle of astigmatism, the dimensional proportions of the image of reflected light that has impinged a circular cross-section on the cylindrical lens and then passed through the lens will vary in two orthogonal directions in accordance with distance d between the optical pickup mechanism and the optical disc. Specifically, in the situation in which distance d is a target value, distance d is set so that the reflected-light image becomes a perfect circle 30 as shown in FIG. 9(b). In contrast, for example, in the situation in which distance d is over, the reflected-light image becomes an ellipse 32, which is vertically long as shown in FIG. 9(a), and in the situation in which distance d is under, the reflected-light image becomes an ellipse 34, which is horizontally long as shown in FIG. 9(c).

30 [0005]

The photodetector comprises, for example, the light-receiving part, which is divided into four blocks 36, 2×2 , where each of the blocks constitutes a light-receiving element that outputs received-light signals. The photodetector is disposed such that each diagonal direction along the 2×2 square array of light-receiving elements coincides with an axis of the vertically long ellipse 32 and an axis of the horizontally long ellipse 34, respectively. By such an arrangement, in FIG. 9, the shapes of the reflected-light images can be distinguished on the basis of the difference between the sum of the output signals of the two light-receiving elements aligned along the diagonal line in the vertical direction and the sum of the output signals of the two light-receiving elements aligned along the diagonal line in the horizontal direction, and thereby can be used to control distance d . In contrast, the reflected light intensity, in accordance with data, can be derived from the sum total of the output signals of the four light-receiving elements.

40

[0006]

Because the rate at which data is read from the optical disc is extremely high, the photodetector is configured from semiconductor elements in which PIN photodiodes having a fast response speed are used. FIG. 10 is a schematic, cross-sectional view of one light-receiving element that constitutes a conventional photodetector. This diagram shows the vertical cross-sectional structure of a PIN photodiode, which is the light-receiving element. In this semiconductor element, a p-type semiconductor substrate 40 becomes the anode region 42 of the photodiode, and an i-layer 44, which has a low impurity concentration and high specific resistance, is formed on the anode region 42 via epitaxial growth. The impurity concentration of the i-layer 44 is extremely low, and the specific resistance thereof is on the order of $100 \Omega \cdot \text{cm}$ and is higher, by an order of magnitude, than that of a semiconductor substrate used in other generic semiconductor elements. An n^+ region, which becomes a cathode region 48, is formed on the front surface of the i-layer 44. By disposing the low concentration i-layer 44 between the anode region 42 and the cathode region 48, a depletion layer can be formed in the i-layer 44 even when a reverse-bias voltage applied between the anode and the cathode becomes low, thereby enabling low-voltage driving of the photodetector.

50

[0007]

The anode region 42, the i-layer 44, and the cathode region 48 constitute the PIN photodiode that becomes each light-receiving element of the photodetector. The anode region 42 and the cathode region 48 of the PIN photodiode are each connected to a voltage terminal, and a reverse-bias voltage is applied between the

terminals. The depletion layer is formed in the i-layer 44 between the anode region 42 and the cathode region 48 in the reverse-bias state, and the electrons emitted owing to absorption of the incident light within the depletion layer move toward the cathode region 48 owing to the electrical field within the depletion layer and are output as the received-light signal.

[0008]

The thickness of the i-layer 44 is set to approximately the absorption length or more within the semiconductor for the light to be detected. For example, the absorption length in silicon with respect to light in the 780 nm band or the 650 nm band, which is employed in CDs and DVDs, is approximately 10–20 μm .

DISCLOSURE OF THE INVENTION

10 PROBLEMS TO BE SOLVED BY THE INVENTION

[0009]

The weak photo-electrical conversion signals generated by the light-receiving parts are amplified by an amplifier and output to a later-stage signal-processing circuit. Here, from the viewpoint of curtailing attenuation of the photo-electrical conversion signals and suppressing the superimposition of noise, the length of wiring between the light-receiving parts and the amplifier is configured to be as short as possible. Based on this viewpoint, and from the viewpoint of reducing the manufacturing cost of the photodetector, it would be ideal to form the circuits—such as the light-receiving parts, each of which has the PIN photodiode structure, and the amplifier—on the same semiconductor chip. In this situation, as shown in the schematic, cross-sectional view in FIG. 11, an N-well 50, which is an n-type impurity region, is formed in the front surface of the i-layer 44, which is formed on the low-concentration p-type region, and within this N-well 50, for example, a p-channel MOSFET (Metal Oxide Semiconductor Field Effect Transistor: MOS-type field effect transistor) 52 and an n-channel MOSFET 54 can be formed to constitute a CMOS (Complementary Metal Oxide Semiconductor). However, due to the impurity concentration of the i-layer 44 being extremely low, this configuration has the problem that the leakage current at the pn junction between the i-layer 44 and the N-well becomes large.

[0010]

The present invention was conceived in order to solve the above-mentioned problems, and an object of the present invention is to provide a semiconductor element for photodetection that can be driven at low voltage and high speeds and can achieve a reduction in cost.

MEANS FOR SOLVING THE PROBLEMS

30 [0011]

A semiconductor device of the present invention, which comprises a light-receiving part and a circuit part that are formed on a semiconductor substrate that is common thereto, comprising: a high specific resistance region, which is provided on a principle surface of the semiconductor substrate and is formed with high specific resistance owing to a low impurity concentration; wherein the light-receiving part comprises: a first electrode region, which is disposed in contact with the high specific resistance region, is a first conductive semiconductor region having a higher impurity concentration than the high specific resistance region, and to which a first voltage is applied; and a second electrode region, which is disposed in contact with the high specific resistance region, is a second conductive semiconductor region having a higher impurity concentration than the high specific resistance region, and to which a second voltage is applied; between the first electrode region and the second electrode region is placed in a reverse-bias state owing to the first voltage and the second voltage, and thereby a depletion layer is formed in the high specific resistance region; and the circuit part comprises: a circuit-element region, which is provided on the principle surface and is a first conductive semiconductor region on which a circuit element is formed in the interior; and a junction-boundary region, which constitutes the boundary between the high specific resistance region and the circuit-element region and is a second conductive semiconductor region having a higher impurity concentration than the high specific resistance region.

EFFECTS OF THE INVENTION

[0012]

According to the present invention, a junction-boundary region of a concentration higher than that of the high specific resistance region is provided at the boundary between the high specific resistance region and the circuit-element region to have a conductivity type that is the reverse of the circuit-element region. The expansion of a depletion layer that can generate electric charges due to thermal excitation or the like is curtailed and leakage current is inhibited at the pn junction portion that is formed by this junction-boundary region and this circuit-element region. As a result, a circuit part that includes a circuit element such as a CMOS can be provided together with the light-receiving part and formed on the same substrate, and thereby a low voltage and high-speed driven photodetection semiconductor element can be realized while curtailing costs.

BEST MODES FOR CARRYING OUT THE INVENTION

[0013]

Modes for implementing the present invention (referred to below as embodiments) are explained below on the basis of the drawings.

[0014]

[First Embodiment]

FIG. 1 is a schematic plan view of a photodetector, which is a semiconductor element of the embodiment. A photodetector 60 is formed on a semiconductor substrate composed of silicon, and a light-receiving part 62 is disposed in an opening portion (not shown) provided in a protective film that is layered on the front surface of the semiconductor substrate. The light-receiving part 62 comprises, for example, four PIN photodiodes (PD) 64, which are arrayed 2×2, and partitions light incident from an optical system onto the substrate front surface into four blocks, 2×2, and receives that light. A signal-processing circuit part 66, as well as the light-receiving part 62, is formed on the semiconductor substrate. The signal-processing circuit part 66 is disposed, for example, around the light-receiving part 62. The signal-processing circuit part 66 comprises, for example, circuit elements, such as CMOSs 68, and these circuit elements can be used to form, on the same semiconductor chip as the light-receiving part 62: an amplifier circuit for the output signals from the light-receiving part 62; or another signal-processing circuit.

[0015]

FIG. 2 is a more detailed plan view of the light-receiving part 62. Each of the PDs 64 is demarcated by an isolation region 70, which is formed on the front surface of the semiconductor substrate surrounding the PDs 64. The isolation region 70 is formed, for example, as a p⁺ region in which a high concentration of p-type impurities is diffused. The absorption of light generates electrons and electron holes in portions on the silicon substrate that correspond to the light-receiving part. A cathode region 72, in which electrons from among the generated electric charges are collected, is disposed in each of the PDs 64 as the cathode. Each of the cathode regions 72 is formed, for example, as an n⁺ region in which a high concentration of n-type impurities is diffused.

[0016]

The isolation region 70 and each of the cathode regions 72 is connected via a contact to a wiring formed in, for example, an aluminum (Al) layer or the like. A ground potential is applied to the isolation region 70, for example, via a wiring 74. In addition, the signal charges collected in the cathode regions 72 are read out via wirings 76.

[0017]

FIG. 3 is a schematic, cross-sectional view that shows the structure of the light-receiving part 62 and the signal-processing circuit part 66 in a vertical cross section of the semiconductor substrate through a straight line A-A', which is shown in FIG. 1 and FIG. 2, respectively. Two of the PDs 64 of the light-receiving part 62 and the CMOS 68 of the signal-processing circuit part 66 appear in this cross section.

[0018]

The present photodetector 60 is formed by employing a semiconductor substrate onto which a semiconductor layer, having a lower impurity concentration than a P-sub layer 80 and a high specific resistance, is layered onto one principle surface of the P-sub layer 80, which is a p-type silicon substrate into which p-type impurities have been introduced. The P-sub layer 80 constitutes the anode, which is common to all the PDs 64; and, for example, a ground potential from the substrate rear surface is applied to the P-sub layer 80. The semiconductor layer, which has high specific resistance and is layered onto the P-sub layer 80, is formed, for example, by epitaxial growth. This epitaxial layer 82 (high specific resistance region) constitutes the i-layer of each of the PDs 64 in the light-receiving part 62. The low-concentration impurity introduced into the epitaxial layer 82 is, for example, a p-type impurity. In addition, specific resistance ρ of the epitaxial layer 82 is at least 200 $\Omega \cdot \text{cm}$ or more, and here, ρ is approximately 500 $\Omega \cdot \text{cm}$. In addition, the thickness of the epitaxial layer 82 that constitutes the i-layer is set to approximately the absorption length or more within the semiconductor for the light to be detected. For example, the absorption length of silicon with respect to light in the 780 nm band or the 650 nm band, which is employed in CDs and DVDs, is approximately 10–20 μm . Accordingly, here, the thickness of the epitaxial layer 82 is set to 10–20 μm .

[0019]

The isolation region 70 and the cathode regions 72 described above are formed on the front surface of the epitaxial layer 82 in the light-receiving part 62. The introduction of impurities into the isolation region 70 and the cathode regions 72, respectively, is achieved by forming a mask, which is formed by photolithographic techniques, on the front surface of the silicon substrate on which this epitaxial layer 82 is formed, and employing this mask to selectively perform ion implantation of target regions.

[0020]

Incidentally, the impurities introduced by ion implantation at each of the locations at which the isolation region 70 and the cathode regions 72 are formed are further subject to a thermal diffusion process, as necessary, such that the impurities are pushed further in the depth direction of the substrate. That push amount

can be separately controlled for the isolation region 70 and the cathode regions 72, respectively. As described below, the isolation region 70, for example, functions to suppress crosstalk, among the PDs 64, of the signal charges collecting in the cathode regions 72. Therefore, the depth of the isolation region 70 can be set, for example, to deeper than the cathode regions 72. In contrast, by making the depth of the cathode regions 72 shallow, the depletion layer formed in the i-layer beneath each of the cathode regions 72 expands from proximate to the substrate front surface, and thereby an improvement in photoelectric conversion efficiency can be expected at each of the PDs 64. In this manner, in the situation in which the cathode regions 72 are to be formed shallower than the isolation region 70, it is ideal to perform the ion implantation and thermal diffusion of impurities into the isolation region 70 prior to ion implantation into the cathode regions 72.

10 {0021}

It is noted that, in the configuration of the present photodetector 60, the epitaxial layer 82 of high specific resistance exists as the i-layer between the isolation region 70 and the P-sub layer 80, without the isolation region 70 reaching as far as the P-sub layer 80. In addition, a ground potential is applied to the isolation region 70 via the wiring 74, which is provided on the substrate front-surface side as described above, and the isolation region 70 together with the P-sub layer 80 constitutes an anode.

{0022}

In contrast, in the signal-processing circuit part 66, a P-well 84 and an N-well 86 are formed in a surface-layer portion of the epitaxial layer 82 corresponding to a formation region for the CMOS 68. Here, the N-well 86 is a circuit-element region in which a circuit element is formed in the interior as described below, and the P-well 84 is a junction-boundary region that forms the boundary between the N-well 86 and the epitaxial layer 82. The P-well 84 and the N-well 86 are each formed, for example, by ion implantation. Specifically, ion implantation that forms the P-well 84 is performed first, then, the N-well 86 is formed, by ion implantation, in the interior of the P-well 84 such that the N-well 86 is shallower than the P-well 84. The depths of the P-well 84 and the N-well 86 can be made different from each other by adjusting the ion implantation energy or by selecting the ion type for each of the P-well 84 and the N-well 86. The concentration of the N-well 86 can be established in accordance with its relationship to the CMOS 68 formed within that region. The P-well 84 is configured to have a higher concentration than that of the epitaxial layer 82, and thereby inhibits junction leakage current between the epitaxial layer 82 and the N-well 86.

{0023}

30 A p-channel MOSFET 88 and an n-channel MOSFET 90, which constitute the CMOS 68, are formed inside the N-well 86. The p-channel MOSFET 88 is formed, for example, by additionally forming an N-well 92 inside the N-well 86 and forming a source region 94 and a drain region 96, which are p⁺ regions, on the front surface of the N-well 92. A gate electrode 100 is disposed above a channel region, which is between the source region 94 and the drain region 96, with a gate oxide film 98 interposed therebetween. The n-channel MOSFET 90 is formed by additionally forming a P-well 102 inside the N-well 86 and forming a source region 104 and a drain region 106, which are n⁺ regions, on the front surface of the P-well 102. A gate electrode 110 is disposed above a channel region, which is between the source region 104 and the drain region 106, with the gate oxide film 98 interposed therebetween. The gate electrodes 100, 110 are formed, for example, by using polysilicon, tungsten (W), or the like.

40 {0024}

It is noted that, LOCOSs (local oxidation film) 112 are formed, on the front surface of the epitaxial layer 82, at the boundary between the formation region of the CMOS 68 and the epitaxial layer 82 for the purpose of isolating the regions. In addition, a LOCOS 114 is formed at the boundary between the p-channel MOSFET 88 and the n-channel MOSFET 90 for the purpose of isolating elements.

{0025}

An anti-reflection film 116 is layered onto the substrate front surface on which the light-receiving part 62 and the signal-processing circuit part 66 are formed as described above. The anti-reflection film 116 is composed of, for example, a silicon nitride film. Furthermore, although a planarized film, a wiring layer, and a light-shielding layer are formed thereon, these are not shown in FIG. 3 for simplicity.

50 {0026}

FIG. 4 is a schematic view that shows a circuit configuration during operation of the present photodetector 60 and shows an electric potential distribution at a cross section of the light-receiving part. Similar to FIG. 3, the cross section of the light-receiving part 62 shown in FIG. 4 is along the straight line A-A', which is shown in FIG. 1 and FIG. 2. A reverse-bias voltage is applied, by a voltage source 120, between the

cathode regions 72 and the isolation region 70 and between the cathode regions 72 and the P-sub layer 80. Specifically, the wiring (the wirings 76 in FIG. 2) from each of the cathode regions 72 is connected to one of the input terminals of an op amp 122, and a positive voltage V_b is input from the voltage source 120 into the other input terminal of that op amp 122. The output terminal of each of the op amps 122 is connected to the corresponding cathode region 72 via a resistor, thereby constituting a current detector device. According to this configuration, positive voltage V_b is applied to the cathode regions 72 using the electrical potential of the isolation region 70 and the P-sub layer 80 as a reference, and a voltage that corresponds to the cathode current is extracted from the output terminal of each of the op amps 122. Incidentally, the current detector devices, which each includes the op amp 122, can be formed on the signal-processing circuit part 66.

10 {0027}

A number of equipotential lines are depicted in the cross-sectional view using dotted lines. This cross-sectional view indicates that the depletion layer expands in the epitaxial layer 82, which constitutes the i-layer, owing to a reverse-bias voltage being applied to the anode and cathode of each of the PIN photodiodes. The potential deepens, i.e., increases, with proximity to one of the cathode regions 72, and a potential well is formed for the electrons centered on each of the cathode regions 72.

{0028}

20 The potential at a boundary region 124—which is between the isolation region 70 and the P-sub layer 80—of the epitaxial layer 82 becomes less by applying a ground potential, which becomes a reverse bias, to the cathode regions 66, with the isolation region 70 and the P-sub layer 80 serving as the anode. That is, by providing a ground potential with the P-sub layer 80 as well as the isolation region 70 serving as the anode, the potential of the boundary region 124 beneath the isolation region 70 is pulled in a direction in which it becomes shallow. Thereby, a potential barrier is formed, against the movement of the electrons, between the potential wells corresponding to adjacent PDs 64 that sandwich the isolation region 70.

{0029}

30 For example, in FIG. 4, the electrons emitted by the i-layer beneath the left-side cathode region 72-1 owing to the light incident on the left-side PD 64 are able to move easily toward the cathode region 72-1 along the electric field of the left-side potential well; however, it is difficult for those electrons to move toward the right-side cathode region 72-2 because of the potential barrier that exists therebetween in the region 124. Consequently, the signal charges corresponding to the light incident on the left-side PD 64 collect primarily in the cathode region 72-1. Similarly, it is difficult for the signal charges corresponding to the light incident on the right-side PD 64 to move to the cathode region 72-1 owing to the existence of the potential barrier, and therefore, the signal charges collect primarily in the cathode region 72-2. The amount of electrons that collect in each of the cathode regions 72 is detected as the cathode current via the corresponding op amp 122.

{0030}

Thus, by making the P-sub layer 80 and the isolation region 70 serve as the anode, element isolation can be achieved between the PDs 64 regardless of whether the i-layer of the adjacent PDs 64 are connected beneath the isolation region 70, and thereby a received-light signal, in which crosstalk is suppressed, can be obtained.

{0031}

40 In addition, in the configuration of the present photodetector, the P-sub layer 80 serves as the anode, and this P-sub layer 80 extends beneath the signal-processing circuit part 66 as well. Here, the impurity concentration in the epitaxial layer 82 is extremely low. Consequently, in a configuration in which the epitaxial layer 82 contacts the N-well 86, the lower the electric potential in the P-sub layer 80, the easier it is for the depletion layer to expand into a junction portion at which the epitaxial layer 82 and the N-well 86 are joined. In the depletion layer, it is easier for electric charges to be emitted by thermal excitation or the like, which can cause leakage current to be generated. That is, in a configuration of a photodetector in which the common P-sub layer 80 is disposed beneath the light-receiving part 62 and the signal-processing circuit part 66, and a ground potential is applied with this P-sub layer 80 serving as the anode of the light-receiving part 62, it becomes easier for leakage current to be generated if the N-well 86 of the signal-processing circuit part 66 directly contacts the epitaxial layer 82. Given that point, in the present photodetector 60, the P-well 84, which has a higher impurity concentration than the epitaxial layer 82, is provided at the boundary between the N-well 86 and the epitaxial layer 82, and thereby the expansion of the depletion layer into the pn junction becomes small and curtailment of leakage current is achieved.

50

{0032}

In addition, the depletion layer in the epitaxial layer 82, which is the boundary with the N-well 86, expands not only at the lower-surface side of the N-well 86 but also at the side surfaces. At a boundary portion between the light-receiving part 62 and the signal-processing circuit part 66 in particular, because the isolation

region 70, which is the anode, is grounded and made to have a low electric potential, it is easy for the depletion layer to expand, and thereby it is easy for leakage current to be generated. However, by having a structure in which the P-well 84 is disposed at side portions of the N-well 86 as well, expansion of the depletion layer in the horizontal direction such that it enters the boundary portion between the light-receiving part 62 and the signal-processing circuit part 66 is also curtailed, and thereby a decrease in leakage current is achieved.

[0033]

It is noted that, in the light-receiving part 62 described above, the PDs 64 are disposed adjacent to each other with the isolation region 70 placed between them. Here, as one conventional technique for element isolation, the LOCOS method is known. According to that technique, for example, a thick oxide film that penetrates the substrate similar to the LOCOSs 112, 114 formed on the signal-processing circuit part 66 is caused to grow selectively in a p^+ region similar to the one in which the separation region 70 is formed. While on the one hand this technique can be applied to the light-receiving part 62 as well, this technique is not adopted in the present embodiment. Thus, by not forming a LOCOS oxide film on the isolation region 70, the light incident on the isolation region 70 from above is no longer attenuated by the LOCOS oxide film. Here, beneath the isolation region 70 is the i-layer, which can be depleted. Consequently, attenuation of the light is curtailed and the light incident on the isolation region 70 from above reaches the i-layer beneath the isolation region 70 and can generate the signal charge; thereby, detection efficiency for light that is incident on the light-receiving part 62 improves.

[0034]

In addition, the isolation region 70 can become a non-sensitive region with respect to detecting incidence light. Here, by not forming the LOCOS oxide film, diffusion in the horizontal direction of the isolation region 70 during that formation process is avoided. As a result, because the proportion of the isolation region 70 taking up the light-receiving part is curtailed, an improvement in the detection efficiency for the light incident on the light-receiving part is achieved even at this point.

[0035]

The structure of the light-receiving part 62 of the photodetector 60 is not limited to the configuration described above. FIG. 5 is a schematic, cross-sectional view that shows another structure of the light-receiving part 62 and shows a vertical cross section of the semiconductor substrate along the straight line A-A', which is shown in FIG. 1 and FIG. 2. It is noted that the plan view of this light-receiving part 62 is in common with that shown in FIG. 2. A feature of the light-receiving part 62 shown in FIG. 5 is that it has a lower-portion isolation region 150, which is a p^+ region that protrudes from the P-sub layer 80 at locations opposing the isolation region 70. This lower-portion isolation region 150 receives the voltage applied to the P-sub layer 80 and, together with the P-sub layer 80, functions as a substrate-side anode. Owing to the lower-portion isolation region 150, the distance between the anode that is constituted by the isolation region 70 and the substrate-side anode is reduced at the boundaries of the PDs 64. As a result, the potential barriers for the electrons are more suitably formed in the epitaxial layer 82 at the boundaries of the PDs 64, thereby improving the element isolation performance between the PDs 64.

[0036]

The lower-portion isolation region 150 is formed, for example, by introducing p-type impurities, through ion implantation, etc., at locations on the epitaxial layer 82 corresponding to the boundaries between the PDs 64 in the stage in which the epitaxial layer 82 is layered onto the P-sub layer 80 to a partial thickness. Thus, after the lower-portion isolation region 150 is formed, the epitaxial layer 82 is caused to grow to the remaining thickness. Thereafter, similar to the light-receiving part 62, which exhibits the cross-sectional structure shown in FIG. 3, the structure on the substrate front surface having the isolation region 70, the cathode regions 72, etc., is formed.

[0037]

In the situation in which the structure of the light-receiving part 62 shown in FIG. 5 is adopted instead of the structure of the light-receiving part 62 shown in FIG. 3, here, as well, the expansion of the depletion layer into the epitaxial layer 82 from the boundary with the N-well 86 can be curtailed by providing the P-well 84 on the signal-processing circuit part 66. As a result, the photodetector 60 is achieved in which junction leakage current at the junction between the epitaxial layer 82 and the N-well 86 is curtailed.

[0038]

[Second Embodiment]

Except for points where the structure of the light-receiving part 62 is different from the above-mentioned first embodiment, the photodetector 60, which is a second embodiment explained below, has a configuration that is basically the same as the above-mentioned first embodiment; in the present embodiment, constituent elements having the same functions and properties as those of the first embodiment are assigned reference numerals identical to those of the first embodiment. A schematic plan view of the photodetector 60 of the present embodiment is identical to that of FIG. 1, which is referenced here.

[0039]

FIG. 6 is a schematic plan view of the light-receiving part 62 of the present photodetector 60. Similar to the photodetector of the first embodiment, the present photodetector 60 is formed on the semiconductor substrate, which is composed of silicon, and the light-receiving part 62 is disposed in the opening portion (not shown) that is provided in the protective film layered on the front surface of the semiconductor substrate. The light-receiving part 62 partitions light incident on the substrate front surface into four blocks, 2×2 , and receives that light.

[0040]

10 Cathode regions 200 are disposed, corresponding to the PDs 64, on the front surface of the semiconductor substrate on the outer periphery of the light-receiving part 62. In addition, an anode region 202 is disposed on the front surface of the semiconductor substrate between adjacent PDs 64 to provide element isolation between the PDs 64.

[0041]

Each of the cathode regions 200 is formed as an n^+ region along the outer periphery of the light-receiving part, for example, by diffusing a high concentration of n-type impurities from the front surface of a trench 204 that is L-shaped in planar form. In contrast, the anode region 202 is formed as a p^+ region between adjacent PDs 64, for example, by diffusing a high concentration of p-type impurities from the front surface of a trench 206 that is plus-shaped in planar form. Each of the cathode regions 200 is connected via a contact to wiring (not shown) formed from, for example, an aluminum (Al) layer or the like, and functions as the cathode of the corresponding PD 64, which is a PIN photodiode. In contrast, the anode region 202 is connected via a contact to wiring (not shown), and functions as an anode that is common to all the PIN photodiodes.

[0042]

FIG. 7 is a schematic, cross-sectional view that shows the structure of the light-receiving part 62 and the signal-processing circuit part 66 in a vertical cross section of the semiconductor substrate through a straight line A-A', which is shown in FIG. 1 and FIG. 6, respectively. Two of the PDs 64 of the light-receiving part 62 and the CMOS 68 of the signal-processing circuit part 66 appear in this cross section. The epitaxial layer 82 having high specific resistance and layered onto one principle surface of the P-sub layer 80, which is a p-type silicon substrate, constitutes the i-layer of the PIN photodiodes. The trenches 204, 206, the cathode regions 200, and the anode region 202 described above are formed on the front surface of the epitaxial layer 82. The trenches 204, 206 are formed by etching the front surface of the semiconductor substrate. After forming the trenches 204, 206, a resist is applied to the front surface of the semiconductor substrate, the resist is patterned, and apertures are formed surrounded by the trenches 204. Ion implantation of n-type impurities is performed with this resist serving as a mask. By making the implantation direction inclined, ion implantation also occurs at the wall surfaces of the trenches 204, and the cathode regions 200 are formed on the front surface of each of the trenches 204, i.e., the wall surfaces and the bottom surface of each of the trenches 204. Similarly, a mask having an aperture corresponding to the trench 206 is formed using the resist, ion implantation of p-type impurities is performed, and thereby the anode region 202 is formed on the front surface of the trench 206, i.e., on the wall surfaces and bottom surface of the trench 206.

[0043]

40 It is noted that the processes for forming the cathode regions 200 and the anode region 202 can include a thermal diffusion step, as necessary, which is performed after the ion implantation described above. In addition, after forming the cathode regions 200 and the anode region 202, the trenches 204, 206 can be filled with an insulating film to achieve a structure in which the front surface of the light-receiving part is planarized.

[0044]

While the cathode regions 200 and the anode region 202 formed using the trenches 204, 206, respectively, as described above, constitute the anode and the cathode of each of the PIN photodiodes, they also surround the PDs 64 and function to isolate each of the PDs 64 from the outside thereof. Incidentally, this kind of configuration is known as the STI (Shallow Trench Isolation) technique.

[0045]

50 The epitaxial layer 82 appears on the front surface at the inner-side portions surrounded by the cathode regions 200 and the anode region 202 of the PDs 64. As described below, each of these portions becomes a semiconductor region (a light-receiving semiconductor region 208) that is sensitive to the light incident on the light-receiving part.

[0046]

FIG. 8 is a schematic view that shows a circuit configuration during operation of the present photodetector 60 and shows an electric potential distribution at a cross section of the light-receiving part 62. Similar to FIG. 7, the cross section of the light-receiving part 62 shown in FIG. 8 is along the straight line A-A', which is shown in FIG. 1 and FIG. 6. Each of the cathode regions 200 is placed in a reverse-bias state in relation

to the anode region 202 and the P-sub layer 80, which are made a ground potential using the voltage source 120. Specifically, the wiring from each of the cathode regions 200 is connected to one of the input terminals of the corresponding op amp 122, and the positive voltage V_b from the voltage source 120 is input to the other input terminal of that op amp 122. The output terminal of each of the op amps 122 is connected to the corresponding cathode region 200 via a resistor, to thereby constitute a current detector device. According to this configuration, V_b is applied to the cathode regions 200, and a voltage that corresponds to the cathode current is extracted from the output terminal of each of the op amps 92. Incidentally, the current detector devices, which each includes the op amp 122, can be formed on the signal-processing circuit part 66.

[0047]

- 10 A number of equipotential lines are depicted in the cross-sectional view using dotted lines. This cross-sectional view indicates that the depletion layer expands in the epitaxial layer 82, which constitutes the i-layer, owing to the reverse-bias voltage being applied to the cathode and the anode of each of the PIN photodiodes. The cathode regions 200 and the anode region 202 are both disposed on the front surface of the semiconductor substrate, and the light-receiving semiconductor regions 208 located in the vicinity of the front surface of the semiconductor substrate between the cathode regions 200 and the anode region 202 constitute the i-layer. According to this configuration, the depletion layer likewise expands to the vicinity of the front surface of the semiconductor substrate in correspondence to the light-receiving semiconductor regions 208 when the reverse-bias voltage is applied.

[0048]

- 20 The potential within the depletion layer increases from the anode region 202 toward the respective cathode region 200. That is, a potential well is formed at a location corresponding to each of the cathode regions 200. In addition, the potential becomes low at the boundary portions between adjacent PDs 64, which correspond to the location of the anode region 202, a potential barrier with respect to the movement of electrons is formed, and thereby element isolation between adjacent PDs 64 is achieved.

[0049]

- 30 The light incident on each of the PDs 64 generates electron-electron hole pairs, which function as the signal charges absorbed by the depletion layer, and the electrons of these pairs collect in the neighboring cathode regions 200. The amount of electrons that collect in each of the cathode regions 200 is detected by the corresponding op amp 122 as the cathode current. The signal charges are generated in each of the PDs 64 of the present photodetector 60 also owing to the light absorbed in the vicinity of the front surface of the corresponding light-receiving semiconductor region 208, and those signal charges can be detected from the corresponding cathode region 200. Thereby, it becomes possible to extract the signal charges generated by short-wavelength light absorbed in the vicinity of the front surface of the semiconductor substrate as the received-light signal, and thereby sensitivity to short-wavelength light can be obtained.

[0050]

- 40 Incidentally, by employing an anisotropic etching technique, such as RIE (Reactive Ion Etching), as the etching method for forming the trenches 204, 206, for example, the trenches 204, 206 can be finely formed, and thereby the proportion of the light-receiving semiconductor region 208 that takes up the surface area of the front surface of the semiconductor substrate at each of the PDs 64 can be made large. Thereby, an improvement in the sensitivity of the PDs 64 is achieved.

[0051]

In addition, because the junction surface area of the junctions between the cathode regions 200 and the epitaxial layer 82 and the junction between the anode region 202 and the epitaxial layer 82 can be made small, the inter-terminal capacitance between the cathode and anode of each of the PIN photodiodes is curtailed, and thereby it becomes possible to secure satisfactory responsiveness.

[0052]

- 50 In the configuration of the present photodetector 60, the N-well 86, in which the circuit elements are formed in the signal-processing circuit part 66, is formed inside the epitaxial layer 82, which has an extremely low impurity concentration. Consequently, the depletion layer expands easily to the epitaxial layer 82 at the boundary with the N-well 86, and thereby leakage current is easily generated. When the PIN photodiodes are used in the reverse-bias state in particular, the P-sub layer 80, which is the anode thereof, expands also to beneath the signal-processing circuit part 66. Although the epitaxial layer 82 is more easily depleted when the potential difference between the N-well 86 and the P-sub layer 80 is small (or is reverse biased), in the present photodetector 60, the P-well 84, which has a higher impurity concentration than the epitaxial layer 82, is provided at the boundary between the N-well 86 and the epitaxial layer 82, and thereby expansion of the depletion layer into the pn junction portion with the N-well 86 is reduced, and leakage current is curtailed.

[0053]

In addition, by having the structure in which the P-well 84 also covers the side surfaces of the N-well

86, the depletion layer in the horizontal direction from the N-well 86 is also curtailed, and a decrease in leakage current is achieved. There are also situations in which the PDs 64 are laid out such that the anode region 202 is adjacent to the N-well 86, and in that situation in particular, the depletion layer, which expands in the horizontal direction, is easily formed in the epitaxial layer 82 therebetween. However, in the present photodetector 60, by having the structure in which the P-well 84 is also disposed at the side portions of the N-well 86 as described above, in this situation as well, it becomes possible for the depletion layer to be suitably curtailed and the leakage current to be suitably inhibited.

BRIEF DESCRIPTION OF THE DRAWINGS

[0054]

- 10 FIG. 1 is a schematic plan view of a photodetector, which is an embodiment of the present invention.
 FIG. 2 is a plan view of a light-receiving part of the photodetector according to the first embodiment.
 FIG. 3 is a cross-sectional view of the photodetector according to the first embodiment.
 FIG. 4 is a schematic view that shows a circuit configuration during operation of the photodetector according to the first embodiment and shows an electric potential distribution at a cross section of the light-receiving part.
 FIG. 5 is a cross-sectional view of another light-receiving part of the photodetector according to the first embodiment.
 FIG. 6 is a plan view of a light-receiving part of a photodetector according to a second embodiment.
 20 FIG. 7 is a cross-sectional view of the light-receiving part of the photodetector according to the second embodiment.
 FIG. 8 is a schematic view that shows a circuit configuration during operation of the photodetector according to the second embodiment and shows an electric potential distribution at a cross section of the light-receiving part.
 FIG. 9 includes schematic diagrams that show a light-receiving part of the photodetector and the reflected-light image on the light-receiving part.
 FIG. 10 is a schematic, cross-sectional view of one light-receiving element that constitutes a conventional photodetector.
 FIG. 11 is a cross-sectional view of an element and is for explaining the problems of a photodetector in which circuits, such as the light-receiving part having a PIN photodiode structure, an amplifier, and the like, are
 30 formed on the same semiconductor chip.

EXPLANATION OF THE REFERENCE NUMBERS

[0055]

- | | |
|-------------|--------------------------------------|
| 60 | Photodetector |
| 62 | Light-receiving part |
| 64 | PIN photodiode (PD) |
| 66 | Signal-processing circuit part |
| 68 | CMOS |
| 70 | Isolation region |
| 72, 200 | Cathode regions |
| 40 74, 76 | Wirings |
| 80 | P-sub layer |
| 82 | Epitaxial layer |
| 84 | P-well |
| 86, 92 | N-wells |
| 88, 102 | p-channel MOSFETs |
| 90 | n-channel MOSFET |
| 94, 104 | Source regions |
| 96, 106 | Drain regions |
| 98 | Gate oxide film |
| 50 100, 110 | Gate electrodes |
| 112 | LOCOS |
| 116 | Anti-reflection film |
| 120 | Voltage source |
| 122 | Op amp |
| 202 | Anode region |
| 204, 206 | Trenches |
| 208 | Light-receiving semiconductor region |

FIG. 1

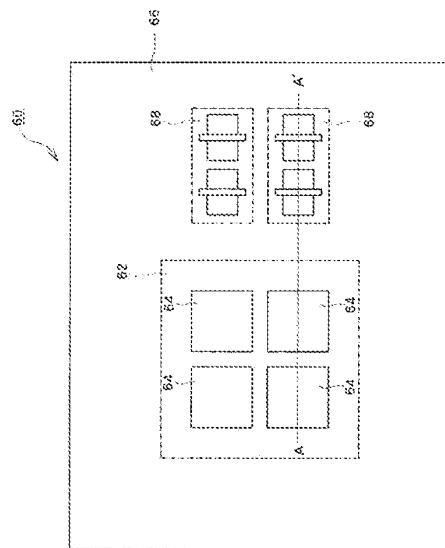


FIG. 2

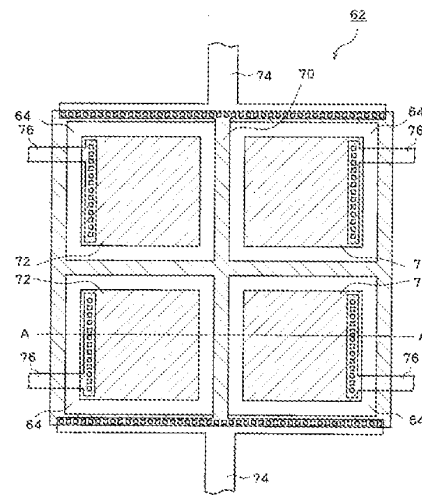


FIG. 3

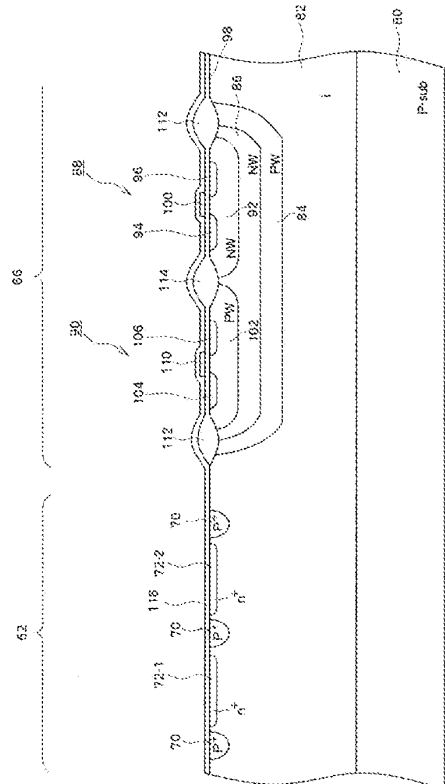


FIG. 4

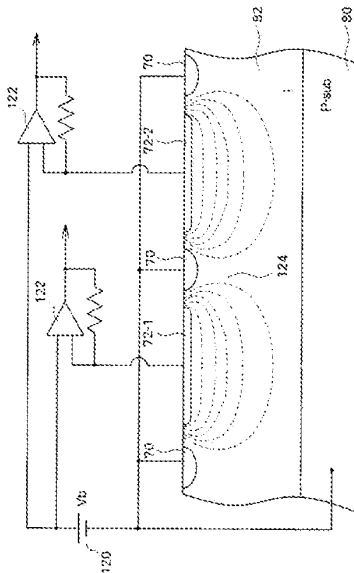


FIG. 5

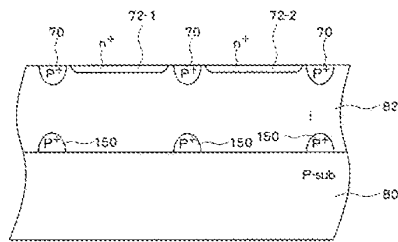


FIG. 6

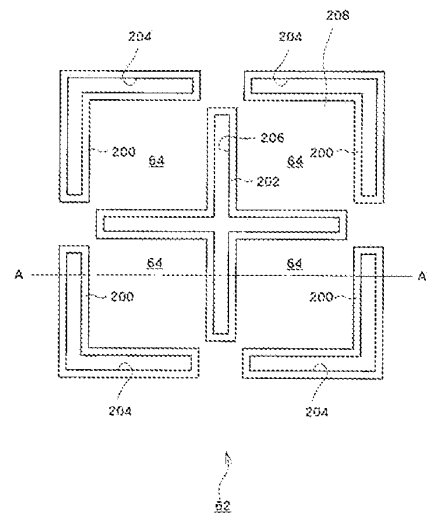


FIG. 7

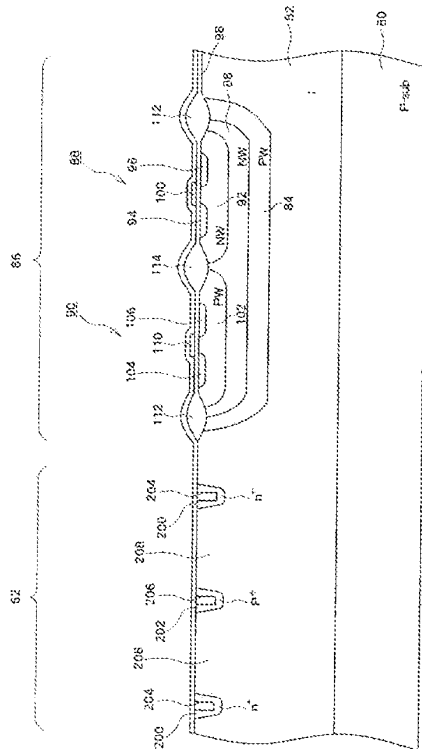
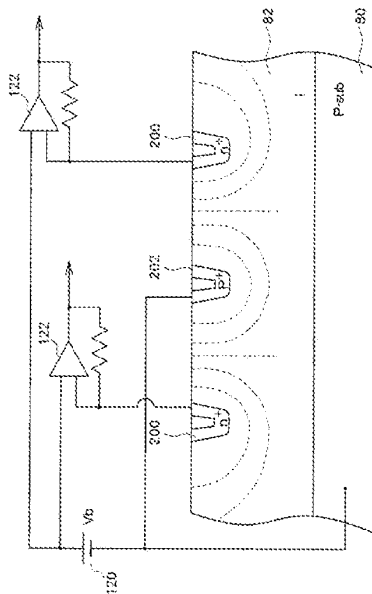


FIG. 8



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(21) 出願番号 (22) 出願日	特願2005-319513 (P2005-319513) 平成17年11月2日 (2005. 11. 2)	(71) 出願人 000001889 三洋電機株式会社 大阪府守口市京阪本通2丁目5番5号 (74) 代理人 110000154 特許業務法人はるか国際特許事務所 (72) 発明者 長谷川 昭博 大阪府守口市京阪本通2丁目5番5号 三 洋電機株式会社内 F ターム (参考) 4M118 AA10 AB10 BA02 CA05 5F049 MA04 MB02 NA03 NA10 NA15 NB08 QA03 RA04 RA10 SE01 SE05 SZ03 UA01 UA07 UA12 UA13 UA17 WA03
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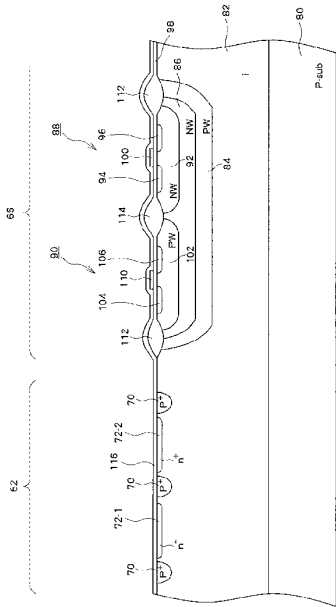
(54) 【発明の名称】 半導体装置

(57) 【要約】

【課題】 P I Nフォトダイオードを受光部に備える光検出用半導体素子において、同一チップ上に C M O Sを構成可能とする。

【解決手段】 P-sub層 8 0の上にエピタキシャル層 8 2を積層した半導体基板に受光部 6 2及び信号処理回路部 6 6を構成する。 P I Nフォトダイオードは P-sub層 8 0をアノードとし、カソード領域 7 2と P-sub層 8 0との間のエピタキシャル層 8 2を i 層として構成される。信号処理回路部 6 6において C M O Sを形成する Nウェル 8 6とエピタキシャル層 8 2との境界に Pウェル 8 4を形成する。

【選択図】 図 3



【特許請求の範囲】**【請求項 1】**

共通の半導体基板に形成された受光部及び回路部を有する半導体装置であって、
前記半導体基板の主面に設けられ、低不純物濃度により高比抵抗に形成される高比抵抗領域を有し、

前記受光部は、

前記高比抵抗領域に接して配置され、前記高比抵抗領域よりも高不純物濃度の第 1 導電型半導体領域であって第 1 電圧を印加される第 1 電極領域と、

前記高比抵抗領域に接して配置され、前記高比抵抗領域よりも高不純物濃度の第 2 導電型半導体領域であって第 2 電圧を印加される第 2 電極領域と、

を有し、

前記第 1 電極領域及び前記第 2 電極領域相互間は、前記第 1 電圧及び前記第 2 電圧により逆バイアス状態とされて、前記高比抵抗領域に空乏層を形成し、

前記回路部は、

前記主面に設けられ、内部に回路素子が形成される第 1 導電型半導体領域である回路素子領域と、

前記高比抵抗領域及び前記回路素子領域の間の境界を構成し、前記高比抵抗領域よりも高不純物濃度の第 2 導電型半導体領域である接合境界領域と、

を有することを特徴とする半導体装置。

【請求項 2】

請求項 1 に記載の半導体装置において、

前記高比抵抗領域は、第 2 導電型半導体領域であること、を特徴とする半導体装置。

【請求項 3】

請求項 1 又は請求項 2 に記載の半導体装置において、

前記高比抵抗領域は、 $200\ \Omega \cdot \text{cm}$ 以上の比抵抗を有すること、を特徴とする半導体装置。

【請求項 4】

請求項 1 から請求項 3 のいずれか 1 つに記載の半導体装置において、

前記高比抵抗領域は、エピタキシャル成長層であること、を特徴とする半導体装置。

【請求項 5】

請求項 1 から請求項 4 のいずれか 1 つに記載の半導体装置において、

前記第 2 電極領域は、前記高比抵抗領域の下地層であり、

前記第 1 電極領域及び前記回路素子領域はそれぞれ、前記高比抵抗領域の表層部に形成されること、

を特徴とする半導体装置。

【請求項 6】

請求項 1 から請求項 4 のいずれか 1 つに記載の半導体装置において、

前記第 1 電極領域、前記第 2 電極領域及び前記回路素子領域はそれぞれ、前記高比抵抗領域の表層部に形成されること、

を特徴とする半導体装置。

【請求項 7】

請求項 6 に記載の半導体装置において、

他の前記第 2 電極領域は、当該高比抵抗領域の下地層であること、を特徴とする半導体装置。

【発明の詳細な説明】**【技術分野】****【0001】**

本発明は、高比抵抗の半導体領域に広がる空乏層を利用した受光部を有し光電変換による信号を生成する半導体装置に関する。

【背景技術】

【0002】

近年、情報記録媒体として、C D (Compact Disk) や D V D (Digital Versatile Disk) といった光ディスクが大きな位置を占めるようになってきた。これら光ディスクの再生装置は、光ピックアップ機構により光ディスクのトラックに沿ってレーザ光を照射し、その反射光を検知する。そして、反射光強度の変化に基づいて記録データが再生される。

【0003】

光ディスク再生装置は、反射光に基づいてデータを検出しつつ、光ピックアップ機構と光ディスクとの位置関係をサーボ制御する。具体的には、レーザ光をトラックの中心線に沿って照射するためのトラッキングサーボ及び、光ディスクと光ピックアップ機構との距離を一定に保つフォーカスサーボが行われる。例えば、フォーカスサーボ制御は、レーザ反射光を検出する光検出器の出力信号に基づき、アクチュエータで光ピックアップ機構の位置を可変制御し、光ディスクとの距離 d を一定に保つ。これにより、光ディスクの表面での照射光のフォーカスのずれに応じた反射光量の変動が抑制され、受光信号に重畳されるノイズが抑制される。

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【0004】

このようなサーボ制御のための情報を得るために、光検出器として反射光像を複数区画に分割して受光するものが用いられる。図9は、光検出器の受光部及び、当該受光部上での反射光像を示す模式図である。レーザ反射光はシリンドリカルレンズを通して光検出器に入射される。非点収差法の原理により、円形状断面でシリンドリカルレンズに入射した反射光の当該シリンドリカルレンズ通過後の像は、光ピックアップ機構と光ディスクとの距離 d に応じて、直交する2方向の寸法比率が変化する。具体的には、距離 d が目標値である場合に、図9(b)に示すように、反射光像が真円30となるように設定される。一方、例えば、距離 d が、オーバーである場合には図9(a)に示すように、反射光像は縦長の楕円32となり、アンダーである場合には図9(c)に示すように、反射光像は横長の楕円34となる。

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【0005】

光検出器は例えば、 2×2 の4つの区画36に分割された受光部を有し、各区画はそれぞれ受光信号を出力する受光素子を構成する。光検出器は、受光素子の 2×2 の正方配列の対角方向が縦長楕円32及び横長楕円34それぞれの軸に一致するように配置される。このように配置することで、図9において垂直方向の対角線上に並ぶ2受光素子の出力信号の和と水平方向の対角線上に並ぶ2受光素子の出力信号の和との差に基づき、各反射光像の形状を判別し、距離 d の制御に用いることができる。一方、データに応じた反射光強度は、4つの受光素子の出力信号の総和により求められる。

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【0006】

光ディスクから読み出されるデータレートは非常に高いため、光検出器は、応答速度の速いP I Nフォトダイオードを用いた半導体素子で構成されている。図10は、従来の光検出器を構成する1つの受光素子の模式的な断面図である。この図は、受光素子であるP I Nフォトダイオードの垂直断面構造を表している。この半導体素子において、p型半導体基板40がフォトダイオードのアノード領域42となり、その上に不純物濃度が低く高比抵抗であるi層44がエピタキシャル成長により形成される。i層44の不純物濃度は極めて低く、その比抵抗は $100 \Omega \cdot \text{cm}$ のオーダーであり、この比抵抗は他の一般的な半導体素子に用いられる半導体基板に比べて桁違いに高い。i層44の表面にはカソード領域48となる n^+ 領域が形成される。低濃度のi層44をアノード領域42とカソード領域48との間に配することで、アノードとカソードとの間に印加する逆バイアス電圧を低くしてもi層44に空乏層を形成することができ、光検出器の低電圧駆動化が図られる。

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【0007】

これらアノード領域42、i層44、及びカソード領域48が光検出器の受光素子となるP I Nフォトダイオードを構成する。このP I Nフォトダイオードは、アノード領域42とカソード領域48とがそれぞれ電圧端子に接続され、それらの間に逆バイアス電圧が

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印加される。逆バイアス状態にてアノード領域42とカソード領域48との間のi層44には空乏層が形成され、空乏層内にて入射光の吸収により発生する電子が、空乏層内の電界でカソード領域48へ移動し、受光信号として出力される。

【0008】

i層44の厚さは、検出する光の半導体内での吸収長程度以上に設定される。例えば、CDやDVDに用いられている780nm帯や650nm帯の光に対するシリコンの吸収長は10～20μm程度である。

【発明の開示】

【発明が解決しようとする課題】

【0009】

受光部にて発生した微弱な光電変換信号は増幅器にて増幅され、後段の信号処理回路へ出力される。ここで、光電変換信号の減衰やノイズの重畳を抑制する観点から、受光部と増幅器との間の配線長をできるだけ短くするように構成される。この観点と、光検出器の製造コスト低減の観点とから、PINフォトダイオード構造の受光部と増幅器等の回路とは同一の半導体チップ上に形成することが好適である。この場合、図11の模式的な断面図に示すように、低濃度のp型領域に形成されたi層44の表面にn型不純物領域であるNウェル50を形成し、このNウェル50内に例えば、pチャネルMOSFET（Metal Oxide Semiconductor Field Effect Transistor：MOS型電界効果トランジスタ）52及びnチャネルMOSFET54を形成しCMOS（Complementary Metal Oxide Semiconductor）を構成することができる。しかし、この構成には、i層44の不純物濃度が極めて低いことに起因して、i層44とNウェル50とのpn接合でのリーク電流が大きくなるという問題があった。

【0010】

本発明は上記問題点を解決するためになされたものであり、低電圧で高速駆動可能であると共にコスト削減が図られる光検出用半導体素子を提供することを目的とする。

【課題を解決するための手段】

【0011】

本発明に係る半導体装置は、共通の半導体基板に形成された受光部及び回路部を有するものであって、前記半導体基板の主面に設けられ、低不純物濃度により高比抵抗に形成される高比抵抗領域を有し、前記受光部が、前記高比抵抗領域に接して配置され、前記高比抵抗領域よりも高不純物濃度の第1導電型半導体領域であって第1電圧を印加される第1電極領域と、前記高比抵抗領域に接して配置され、前記高比抵抗領域よりも高不純物濃度の第2導電型半導体領域であって第2電圧を印加される第2電極領域と、を有し、前記第1電極領域及び前記第2電極領域相互間が、前記第1電圧及び前記第2電圧により逆バイアス状態とされて、前記高比抵抗領域に空乏層を形成し、前記回路部が、前記主面に設けられ、内部に回路素子が形成される第1導電型半導体領域である回路素子領域と、前記高比抵抗領域及び前記回路素子領域の間の境界を構成し、前記高比抵抗領域よりも高不純物濃度の第2導電型半導体領域である接合境界領域と、を有するものである。

【発明の効果】

【0012】

本発明によれば、高比抵抗領域と回路素子領域との境界に回路素子領域とは反対の導電型で高比抵抗領域より高濃度の接合境界領域が設けられる。この接合境界領域と回路素子領域とが形成するpn接合部分においては、熱励起等に起因して電荷を発生し得る空乏層の拡がりや抑制され、リーク電流が抑制される。その結果、CMOS等の回路素子を含む回路部を受光部に併設して同一基板に形成することができ、コストを抑制しつつ低電圧かつ高速駆動の光検出用半導体素子を実現することができる。

【発明を実施するための最良の形態】

【0013】

以下、本発明の実施の形態（以下実施形態という）について、図面に基づいて説明する。

【0014】

〔実施形態1〕

図1は、実施形態の半導体素子である光検出器の概略の平面図である。本光検出器60はシリコンからなる半導体基板に形成され、半導体基板表面上に積層される保護膜に設けられた開口部分（図示せず）に受光部62が配置される。受光部62は、例えば、 2×2 に配列された4つのPINフォトダイオード（PD）64を含み、光学系から基板表面へ入射する光を 2×2 の4区画に分割して受光する。半導体基板には受光部62だけでなく、信号処理回路部66が形成される。例えば、信号処理回路部66は受光部62の周囲に配置される。信号処理回路部66は例えば、CMOS68等の回路素子を含み、これら回路素子を用いて受光部62からの出力信号に対する増幅回路やその他の信号処理回路を受光部62と同一の半導体チップに形成することができる。

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【0015】

図2は、受光部62のより詳しい平面図である。各PD64はそれらの周囲の半導体基板表面に形成される分離領域70により区切られる。分離領域70は、例えば、高濃度のp型不純物を拡散された p^+ 領域として形成される。シリコン基板の受光部に対応した部分では、光の吸収により電子及び正孔が生成される。各PD64には、そのカソードとして、生成した電荷のうち電子を集めるカソード領域72が配置される。カソード領域72は、例えば、高濃度のn型不純物を拡散された n^+ 領域として形成される。

【0016】

分離領域70及び各カソード領域72はそれぞれコンタクトを介して、例えばアルミ（A1）層等で形成された配線に接続される。分離領域70は、配線74により例えば、接地電位を印加される。また、各カソード領域72に集められた信号電荷は、配線76を介して読み出される。

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【0017】

図3は、図1及び図2にそれぞれ示す直線A-A'を通り半導体基板に垂直な断面での受光部62及び信号処理回路部66の構造を示す模式的な断面図である。この断面には受光部62の2つのPD64と信号処理回路部66のCMOS68とが現れている。

【0018】

本光検出器60は、p型不純物が導入されたp型シリコン基板であるP-sub層80の一方主面に、P-sub層80より不純物濃度が低く高比抵抗を有する半導体層が積層された半導体基板を用いて形成される。P-sub層80は各PD64に共通のアノードを構成し、例えば、基板裏面から接地電位を印加される。P-sub層80の上に積層される高比抵抗の半導体層は、例えばエピタキシャル成長により形成される。このエピタキシャル層82（高比抵抗領域）は、受光部62にてPD64のi層を構成する。エピタキシャル層82に導入される低濃度不純物は、例えばp型不純物である。また、エピタキシャル層82の比抵抗 ρ は、少なくとも $200 \Omega \cdot \text{cm}$ 以上であり、ここでは、 ρ は $500 \Omega \cdot \text{cm}$ 程度であるとする。また、i層を構成するエピタキシャル層82の厚さは、検出する光の半導体内での吸収長程度以上に設定される。例えば、CDやDVDに用いられている 780 nm 帯や 650 nm 帯の光に対するシリコンの吸収長は $10 \sim 20 \mu\text{m}$ 程度である。よって、ここではエピタキシャル層82の厚さは、 $10 \sim 20 \mu\text{m}$ に設定される。

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【0019】

受光部62において、エピタキシャル層82の表面には、上述の分離領域70及びカソード領域72が形成される。分離領域70及びカソード領域72への不純物の導入はそれぞれ、このエピタキシャル層82を形成されたシリコン基板の表面にフォトリソグラフィ技術で形成されたマスクを形成し、このマスクを用いてイオン注入を対象領域へ選択的に行うことにより実現される。

【0020】

ちなみに、分離領域70、カソード領域72を形成する位置にそれぞれイオン注入により導入された不純物は、さらに必要に応じて熱拡散工程を行って、基板深さ方向に押し込まれる。その押し込み量は、分離領域70、カソード領域72それぞれについて別個に制

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御され得る。例えば、分離領域 70 は、後述するように、各カソード領域 72 に集められる信号電荷の PD 64 間でのクロストークを抑制する機能を担っている。そこで分離領域 70 の深さは、例えば、カソード領域 72 に比べて深く設定され得る。一方、カソード領域 72 の深さを浅くすることで、その下の i 層に形成される空乏層が基板表面近くから広がることとなり、PD 64 での光電変換効率の向上が期待できる。このようにカソード領域 72 を分離領域 70 より浅く形成する場合には、カソード領域 72 へのイオン注入に先立って、分離領域 70 への不純物のイオン注入及び熱拡散を行うのが好適である。

【0021】

なお、本光検出器 60 の構成では、分離領域 70 は P-sub 層 80 までは到達せず、分離領域 70 と P-sub 層 80 との間には、高比抵抗のエピタキシャル層 82 が i 層として存在する。また、分離領域 70 は、上述したように基板表面側に設けられた配線 74 により接地電位を印加され、P-sub 層 80 と共にアノードを構成する。

【0022】

一方、信号処理回路部 66 においては CMOS 68 の形成領域に対応して、エピタキシャル層 82 の表層部に P ウェル 84 及び N ウェル 86 が形成される。ここで、N ウェル 86 は、後述するように内部に回路素子が形成される回路素子領域であり、P ウェル 84 は N ウェル 86 とエピタキシャル層 82 との境界を形成する接合境界領域である。例えば、P ウェル 84 及び N ウェル 86 はそれぞれイオン注入により形成される。具体的には、先に P ウェル 84 を形成するイオン注入を行い、その後、N ウェル 86 をイオン注入により P ウェル 84 より浅く形成し、P ウェル 84 の内側に N ウェル 86 を形成する。P ウェル 84 と N ウェル 86 との深さは、それぞれのイオン注入のエネルギーの調整やイオン種の選択によって、互いに異ならせることができる。N ウェル 86 の濃度はその領域内に形成される CMOS 68 との関係に応じて定めることができる。P ウェル 84 は、エピタキシャル層 82 よりも高濃度に設定され、エピタキシャル層 82 と N ウェル 86 との間の接合リーク電流を抑制する。

【0023】

N ウェル 86 内には、CMOS 68 を構成する p チャネル MOSFET 88 及び n チャネル MOSFET 90 が形成される。p チャネル MOSFET 88 は、例えば、N ウェル 86 内にさらに N ウェル 92 を形成し、その表面に p⁺ 領域であるソース領域 94、ドレイン領域 96 が形成される。ソース領域 94 とドレイン領域 96 との間のチャネル領域の上にはゲート酸化膜 98 を介してゲート電極 100 が配置される。n チャネル MOSFET 90 は、N ウェル 86 内にさらに P ウェル 102 を形成し、その表面に n⁺ 領域であるソース領域 104、ドレイン領域 106 が形成される。ソース領域 104 とドレイン領域 106 との間のチャネル領域の上にはゲート酸化膜 98 を介してゲート電極 110 が配置される。ゲート電極 100、110 は例えば、ポリシリコンやタングステン (W) 等を用いて形成される。

【0024】

なお、エピタキシャル層 82 の表面において、CMOS 68 の形成領域とエピタキシャル層 82 との境界には、領域間の分離のために LOCOS (局所酸化膜) 112 が形成される。また、p チャネル MOSFET 88 と n チャネル MOSFET 90 との境界にも素子分離のために LOCOS 114 が形成される。

【0025】

以上のように受光部 62 及び信号処理回路部 66 が形成された基板表面に反射防止膜 116 が積層される。反射防止膜 116 は例えばシリコン窒化膜で構成される。さらにこの上に平坦化膜や配線層、遮光層が形成されるが、簡略化のため図 3 においては図示を省略している。

【0026】

図 4 は、本光検出器 60 の動作時における回路構成及び、受光部 62 の断面でのポテンシャル分布を示す模式図である。図 4 に示す受光部 62 の断面は図 3 と同様、図 1、図 2 に示す直線 A-A' に沿ったものである。電圧源 120 によって、カソード領域 72 と分

離領域 7 0 及び P-sub 層 8 0 との間には逆バイアス電圧が印加される。具体的には、各カソード領域 7 2 からの配線（図 2 の配線 7 6）はそれぞれオペアンプ 1 2 2 の一方入力端子に接続され、当該オペアンプ 1 2 2 の他方入力端子に電圧源 1 2 0 からの正電圧 Vb が入力される。オペアンプ 1 2 2 は、抵抗を介して出力端子がカソード領域 7 2 に接続され、電流検出器を構成する。この構成により、カソード領域 7 2 は分離領域 7 0 及び P-sub 層 8 0 の電位を基準として正の電圧 Vb を印加され、かつカソード電流に応じた電圧がオペアンプ 1 2 2 の出力端子に取り出される。ちなみに、オペアンプ 1 2 2 を含む電流検出器は、信号処理回路部 6 6 に形成することができる。

【0027】

断面図にはいくつかの等電位線を点線で示している。この断面図は、PIN フォトダイオードのアノードとカソードとに逆バイアス電圧を印加したことにより、i 層を構成するエピタキシャル層 8 2 に空乏層が広がっていることを示している。ポテンシャル電位はカソード領域 7 2 に近いほど深く、すなわち高くなり、各カソード領域 7 2 を中心として電子に対する電位井戸が形成されることとなる。

【0028】

分離領域 7 0 及び P-sub 層 8 0 をアノードとしてカソード領域 6 6 に対し逆バイアスとなる接地電位を印加したことにより、エピタキシャル層 8 2 の分離領域 7 0 と P-sub 層 8 0 との間の境界領域 1 2 4 のポテンシャル電位は浅くなる。つまり、P-sub 層 8 0 に加えて分離領域 7 0 をアノードとして接地電位としたことにより、分離領域 7 0 下の境界領域 1 2 4 のポテンシャル電位が浅くなる方向に引っ張られる。これにより、分離領域 7 0 を挟んで隣り合う各 PD 6 4 に対応する電位井戸の間に、電子の移動に対する電位障壁が形成される。

【0029】

例えば、図 4 において左側の PD 6 4 への入射光によって、その左側のカソード領域 7 2-1 下の i 層で発生した電子は、当該左側の電位井戸の電界に沿ってカソード領域 7 2-1 へは容易に移動可能であるが、右側のカソード領域 7 2-2 へは領域 1 2 4 に電位障壁が間に存在するため移動しにくい。そのため、左側の PD 6 4 への入射光に対応する信号電荷は、専らカソード領域 7 2-1 に集められることとなる。同様に、右側の PD 6 4 への入射光に対応する信号電荷は、電位障壁の存在によりカソード領域 7 2-1 へは移動しにくく、専らカソード領域 7 2-2 に集められる。各カソード領域 7 2 に集められた電子の量は、カソード電流としてオペアンプ 1 2 2 を介して検出される。

【0030】

このように P-sub 層 8 0 に加えて分離領域 7 0 をアノードとしたことにより、分離領域 7 0 の下で隣接 PD 6 4 の i 層がつながっているにも関わらず、PD 6 4 相互の素子分離が実現され、クロストークが抑制された受光信号が得られる。

【0031】

また、本光検出器の構成では、P-sub 層 8 0 がアノードとされ、この P-sub 層 8 0 は信号処理回路部 6 6 の下にも広がる。ここで、エピタキシャル層 8 2 の不純物濃度が極めて薄い。そのため、エピタキシャル層 8 2 が N ウェル 8 6 に接する構成では、P-sub 層 8 0 の電位が低いほど、N ウェル 8 6 との接合部分のエピタキシャル層 8 2 に空乏層が広がりやすい。空乏層では熱励起等による電荷が発生しやすく、これに起因してリーク電流が生じ得る。すなわち、受光部 6 2 及び信号処理回路部 6 6 の下に共通の P-sub 層 8 0 が配され、この P-sub 層 8 0 が受光部 6 2 のアノードとして接地電位を印加される光検出器の構成において、信号処理回路部 6 6 の N ウェル 8 6 を直接、エピタキシャル層 8 2 に接するとリーク電流が生じやすくなり得る。そこで、本光検出器 6 0 では、N ウェル 8 6 とエピタキシャル層 8 2 との境界に、エピタキシャル層 8 2 より不純物濃度の高い P ウェル 8 4 を設け、pn 接合部分での空乏層の広がりを小さくし、リーク電流の抑制を図っている。

【0032】

また、N ウェル 8 6 との境界のエピタキシャル層 8 2 の空乏層は、N ウェル 8 6 の下面側だけでなく、側面にも拡がり得る。特に、受光部 6 2 と信号処理回路部 6 6 との境界部

分では、アノードである分離領域 70 が接地されて低い電位とされるため、空乏層が拡がり易く、リーク電流が発生し易い。しかし、P ウェル 84 が N ウェル 86 の側部にも配置される構造とすることで、この受光部 62 と信号処理回路部 66 との境界部分におけるような横方向への空乏層も抑制され、リーク電流の低減が図られる。

【0033】

なお、上述の受光部 62 では複数の PD 64 が間に分離領域 70 を置いて隣接配置される。ここで、素子分離の 1 つの従来技術として、LOCOS 法が知られている。その技術によれば、例えば、分離領域 70 に形成したような p^+ 領域に選択的に、信号処理回路部 66 に形成した LOCOS 112, 114 のような基板に食い込む厚い酸化膜を成長させる。受光部 62 においても、当該技術を適用することができる一方で、本実施形態では当該技術を採用していない。このように分離領域 70 の上に LOCOS 酸化膜を形成しないことにより、分離領域 70 の上方からの入射光が、LOCOS 酸化膜で減衰されることがなくなる。ここで、分離領域 70 の下は i 層であり空乏化され得る。そのため、減衰を抑制されて分離領域 70 の上方から入射した光は、分離領域 70 下の i 層にまで到達して信号電荷を発生し得ることとなり、受光部 62 へ入射する光に対する検出効率が向上する。

【0034】

また、分離領域 70 は入射光検出に対して不感領域となり得る。ここで、LOCOS 酸化膜を形成しないことにより、その形成工程での分離領域 70 の横方向の拡散が回避される。その結果、受光部に占める分離領域 70 の割合が抑制されるので、この点でも受光部へ入射する光に対する検出効率の向上が図られる。

【0035】

光検出器 60 の受光部 62 の構造は上述のものに限られない。図 5 は、受光部 62 の他の構造を示す模式的な断面図であり、図 1、図 2 に示す直線 A-A' を通り半導体基板に垂直な断面を示している。なお、この受光部 62 の平面図は、図 2 に示すものと共通である。図 5 に示す受光部 62 の特徴は、分離領域 70 に対向する位置に、P-sub 層 80 から突出した p^+ 領域である下部分離領域 150 を有する点にある。この下部分離領域 150 は、P-sub 層 80 に印加される電圧を受けて、P-sub 層 80 と共に基板側のアノードとして機能する。下部分離領域 150 により、分離領域 70 が構成するアノードと基板側のアノードとの距離が、PD 64 の境界にて狭まる。その結果、PD 64 の境界におけるエピタキシャル層 82 に、電子に対する電位障壁がより好適に形成され、PD 64 間の素子分離性能が向上する。

【0036】

例えば、下部分離領域 150 は、P-sub 層 80 にエピタキシャル層 82 を一部の厚さだけ積層した段階にて、当該エピタキシャル層 82 の PD 64 の境界に対応する位置にイオン注入等により p 型不純物を導入して形成される。このように下部分離領域 150 を形成した後、エピタキシャル層 82 の残りの厚さを成長させる。しかる後、図 3 に断面構造を示した受光部 62 と同様にして分離領域 70、カソード領域 72 等の基板表面の構造を形成する。

【0037】

図 3 に示す受光部 62 の構造に代えて、図 5 に示す受光部 62 の構造とした場合にも、信号処理回路部 66 に P ウェル 84 を設けることで、N ウェル 86 の境界からエピタキシャル層 82 へ広がる空乏層を抑制することができる。その結果、エピタキシャル層 82 と N ウェル 86 との間の接合リーク電流が抑制された光検出器 60 が実現される。

【0038】

〔実施形態 2〕

以下説明する第 2 の実施形態である光検出器 60 は、受光部 62 の構造が上記第 1 の実施形態と相違する点を除けば、基本的に上記第 1 の実施形態と同様の構成であり、本実施形態において、第 1 の実施形態と同じ符号は、同一の機能・性質を有する構成要素を示す。本実施形態の光検出器 60 の概略の平面図は、図 1 と同じであり、これを援用する。

【0039】

図6は、本光検出器60の受光部62の模式的な平面図である。本光検出器60は第1の実施形態の光検出器と同様、シリコンからなる半導体基板に形成され、半導体基板表面上に積層される保護膜に設けられた開口部分（図示せず）に受光部62が配置される。受光部62は、基板表面へ入射する光を 2×2 の4区画に分割して受光する。

【0040】

受光部62の外周の半導体基板表面には、各PD64それぞれに対応してカソード領域200が配置される。また、各PD64相互間の半導体基板表面には、アノード領域202が配置され、これが各PD64間の素子分離を行う。

【0041】

カソード領域200は、受光部の外周に沿った、例えばL字型の平面形状を有するトレンチ204の表面から高濃度のn型不純物を拡散し、 n^+ 領域として形成される。一方、アノード領域202は、PD64相互間に、例えば十字型の平面形状を有するトレンチ206の表面から高濃度のp型不純物を拡散し p^+ 領域として形成される。各カソード領域200は、それぞれコンタクトを介して例えばA1層等で形成された配線（図示せず）に接続され、PINフォトダイオードである各PD64のカソードとして機能する。一方、アノード領域202は、コンタクトを介して配線（図示せず）に接続され、各PINフォトダイオードに共通のアノードとして機能する。

【0042】

図7は、図1及び図6にそれぞれ示す直線A-A'を通り半導体基板に垂直な断面での受光部62及び信号処理回路部66の構造を示す模式的な断面図である。この断面には受光部62の2つのPD64と信号処理回路部66のCMOS68とが現れている。p型シリコン基板であるP-sub層80の一方主面に積層された高比抵抗のエピタキシャル層82は、PINフォトダイオードのi層を構成する。エピタキシャル層82の表面には、上述のトレンチ204、206、カソード領域200及びアノード領域202が形成される。トレンチ204、206は、半導体基板の表面をエッチングして形成される。トレンチ204、206の形成後、半導体基板表面にレジストを塗布し、当該レジストをパターンニングしてトレンチ204を開く開口部を形成する。このレジストをマスクとして、n型不純物のイオン注入を行う。その注入方向を斜めとすることで、トレンチ204の壁面にもイオン注入が行われ、トレンチ204の表面、すなわちトレンチ204の壁面及び底面にカソード領域200が形成される。同様にして、トレンチ206に対応した開口部を有するマスクをレジストを用いて形成し、p型不純物のイオン注入を行って、トレンチ206の表面、すなわちトレンチ206の壁面及び底面にアノード領域202を形成する。

【0043】

なお、カソード領域200及びアノード領域202の形成工程は、必要に応じて、上述のイオン注入後に行われる熱拡散工程を含み得る。また、カソード領域200、アノード領域202を形成した後、トレンチ204、206に絶縁膜を埋め込んで、受光部表面を平坦化した構造とすることができる。

【0044】

トレンチ204、206を用いて形成したカソード領域200、アノード領域202は、上述のように、PINフォトダイオードのカソード及びアノードを構成する一方、各PD64を取り囲んで、各PD64をその外側から分離する機能も有している。ちなみに、このような構成は、STI (Shallow Trench Isolation) 技術として知られている。

【0045】

各PD64のカソード領域200及びアノード領域202で囲まれた内側部分には、エピタキシャル層82が表面に現れる。後述するように、この部分が、受光部への入射光に対して感度を有する半導体領域（受光半導体領域208）となる。

【0046】

図8は、本光検出器60の動作時における回路構成及び、受光部62の断面でのポテンシャル分布を示す模式図である。図8に示す受光部62の断面は図7と同様、図1、図6に示す直線A-A'に沿ったものである。カソード領域200は、電圧源120によって

、接地電位とされたアノード領域 202 及び P-sub 層 80 に対して逆バイアス状態とされる。具体的には、各カソード領域 200 からの配線はそれぞれオペアンプ 122 の一方入力端子に接続され、当該オペアンプ 122 の他方入力端子に電圧源 120 からの正電圧 Vb が入力される。オペアンプ 122 は、抵抗を介して出力端子がカソード領域 200 に接続され、電流検出器を構成する。この構成により、カソード領域 200 は Vb を印加され、かつカソード電流に応じた電圧がオペアンプ 92 の出力端子に取り出される。ちなみに、オペアンプ 122 を含む電流検出器は、信号処理回路部 66 に形成することができる。

【0047】

断面図にはいくつかの等電位線を点線で示している。この断面図は、PIN フォトダイオードのカソードとアノードとに逆バイアス電圧を印加したことにより、i 層を構成するエピタキシャル層 82 に空乏層が広がっていることを示している。カソード領域 200 及びアノード領域 202 は、共に半導体基板表面に配置され、かつそれらの間にて半導体基板表面近傍に位置する受光半導体領域 208 は i 層を構成する。この構成により、逆バイアス電圧印加時に、受光半導体領域 208 に対応した半導体基板表面近傍にも空乏層が広がる。

【0048】

空乏層内のポテンシャル電位は、アノード領域 202 からカソード領域 200 に向けて深くなる。つまり、各カソード領域 200 に応じた位置に電位井戸が形成される。また、アノード領域 202 の位置に対応した PD 64 相互の境界部分は、ポテンシャル電位が浅くなり、電子の移動に対する電位障壁を形成し、PD 64 相互の素子分離を実現する。

【0049】

各 PD 64 に入射した光は、空乏層にて吸収され信号電荷として電子-正孔の対を生じ、それらのうち電子が近傍のカソード領域 200 に集められる。各カソード領域 200 に集められた電子の量は、カソード電流としてオペアンプ 122 を介して検出される。本光検出器 60 の PD 64 では、受光半導体領域 208 の表面近傍で吸収される光によっても信号電荷が生成され、当該信号電荷をカソード領域 200 から検出することができる。これにより、半導体基板表面近傍で吸収される短波長の光によって発生する信号電荷を受光信号として取り出すことが可能となり、短波長光に対する感度を得ることができる。

【0050】

ちなみに、トレンチ 204、206 を形成するエッチング方法として例えば、RIE (Reactive Ion Etching) 等の異方性エッチング技術を用いることで、トレンチ 204、206 を細く形成することができ、各 PD 64 の半導体基板表面での面積に占める受光半導体領域 208 の割合を大きくすることができる。これにより、各 PD 64 の感度向上が図られる。

【0051】

また、カソード領域 200 及びアノード領域 202 とエピタキシャル層 82 との接合面積を小さくすることができるので、PIN フォトダイオードのカソードとアノードとの端子間容量が抑制され、良好な応答性を確保することが可能となる。

【0052】

本光検出器 60 の構成では、信号処理回路部 66 において回路素子が内部に形成される N ウェル 86 が、極めて不純物濃度が低いエピタキシャル層 82 内に形成される。そのため、N ウェル 86 との境界のエピタキシャル層 82 に空乏層が拡がり易く、これに起因してリーク電流が生じ易い。特に、PIN フォトダイオードは逆バイアス状態で使用され、そのアノードである P-sub 層 80 が信号処理回路部 66 の下にも広がる。N ウェル 86 と P-sub 層 80 との電位差が小さい（又は逆バイアスである）とエピタキシャル層 82 はより空乏化し易いが、本光検出器 60 では、N ウェル 86 とエピタキシャル層 82 との境界に、エピタキシャル層 82 より不純物濃度の高い P ウェル 84 を設け、N ウェル 86 との p-n 接合部分での空乏層の広がりを小さくし、リーク電流の抑制を図っている。

【0053】

また、P ウェル 84 が N ウェル 86 の側面も覆う構造とすることで、N ウェル 86 から

横方向への空乏層も抑制されリーク電流の低減が図られる。特に、PD 64 はアノード領域 202 がNウェル 86 に隣接するレイアウトとされる場合もあり、その場合にはそれらの間のエピタキシャル層 82 に横方向に拡がる空乏層が形成され易い。しかし、本光検出器 60 では、上述のようにPウェル 84 がNウェル 86 の側部にも配置される構造とすることで、この場合にも空乏層を好適に抑制しリーク電流を抑制することが可能となる。

【図面の簡単な説明】

【0054】

【図1】本発明の実施形態である光検出器の概略の平面図である。

【図2】第1の実施形態に係る光検出器の受光部の平面図である。

【図3】第1の実施形態に係る光検出器の断面図である。

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【図4】第1の実施形態に係る光検出器の動作時における回路構成及び、受光部の断面でのポテンシャル分布を示す模式図である。

【図5】第1の実施形態に係る光検出器の他の受光部の断面図である。

【図6】第2の実施形態に係る光検出器の受光部の平面図である。

【図7】第2の実施形態に係る光検出器の受光部の断面図である。

【図8】第2の実施形態に係る光検出器の動作時における回路構成及び、受光部の断面でのポテンシャル分布を示す模式図である。

【図9】光検出器の受光部及び、当該受光部上での反射光像を示す模式図である。

【図10】従来の光検出器を構成する1つの受光素子の模式的な断面図である。

【図11】PINフォトダイオード構造の受光部と増幅器等の回路とを同一の半導体チップ上に形成した光検出器の問題点を説明する素子断面図である。

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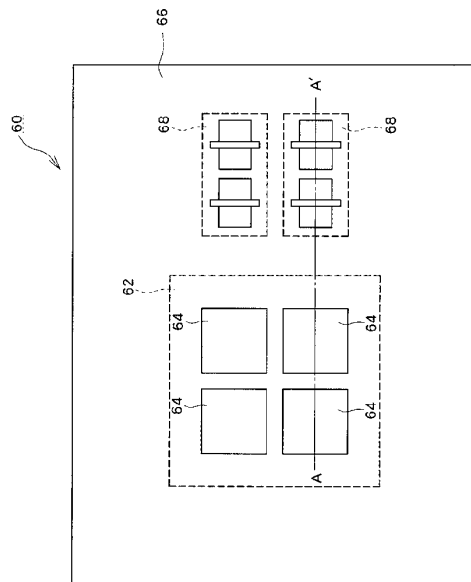
【符号の説明】

【0055】

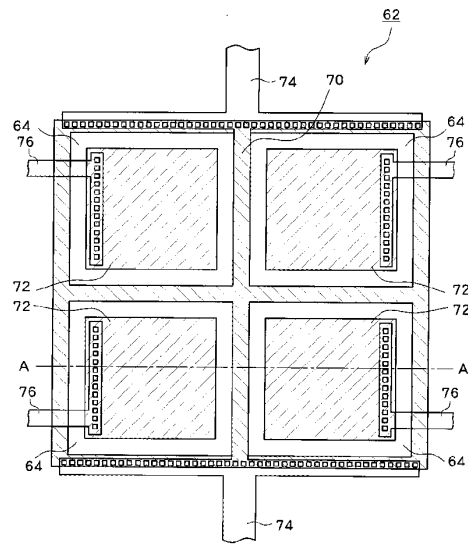
60 光検出器、62 受光部、64 PINフォトダイオード(PD)、66 信号処理回路部、68 CMOS、70 分離領域、72, 200 カソード領域、74, 76 配線、80 P-sub層、82 エピタキシャル層、84 Pウェル、86, 92 Nウェル、88, 102 pチャネルMOSFET、90 nチャネルMOSFET、94, 104 ソース領域、96, 106 ドレイン領域、98 ゲート酸化膜、100, 110 ゲート電極、112 LOCOS、116 反射防止膜、120 電圧源、122 オペアンプ、202 アノード領域、204, 206 トレンチ、208 受光半導体領域。

30

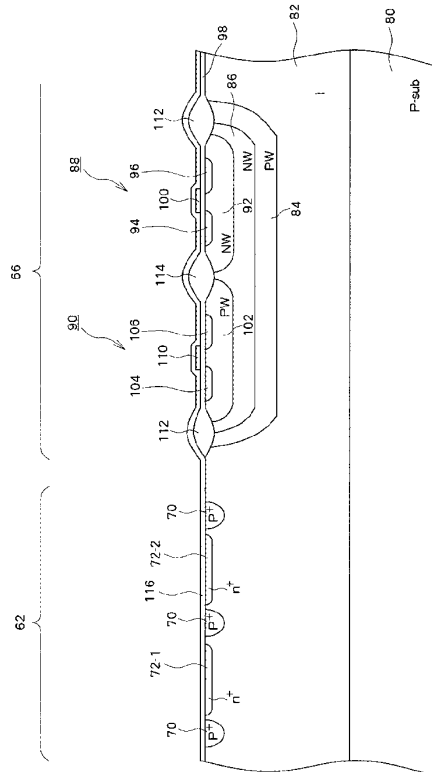
【図 1】



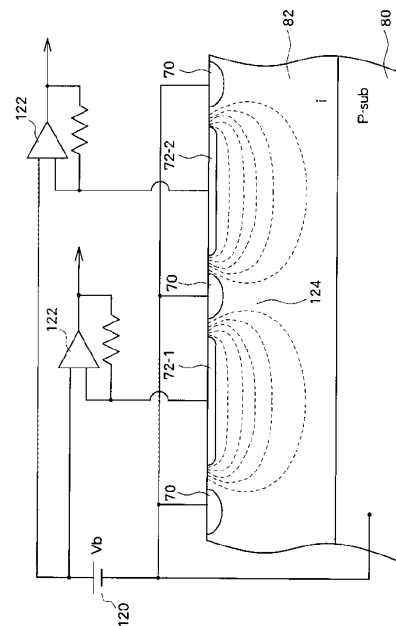
【図 2】



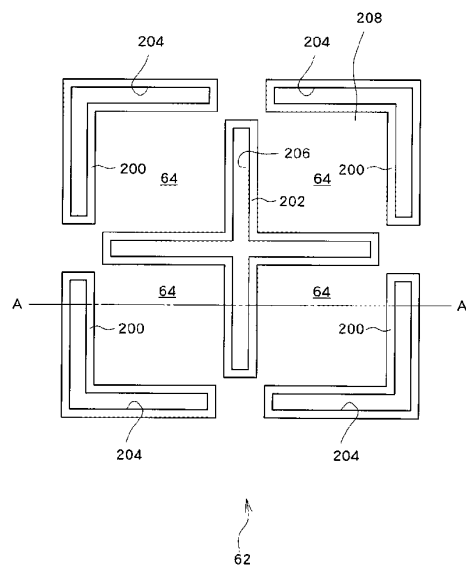
【図 3】



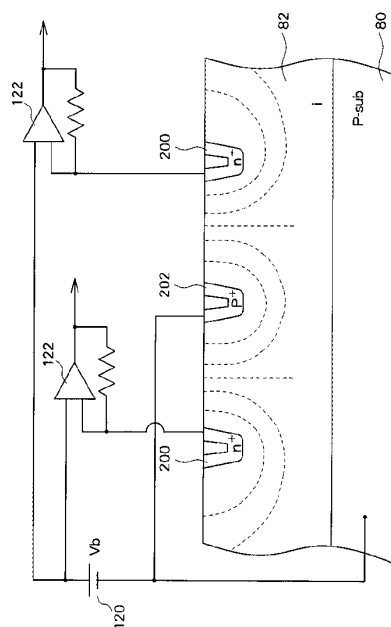
【図 4】



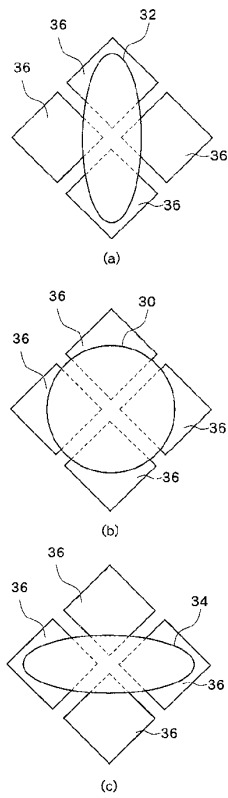
【图 6】



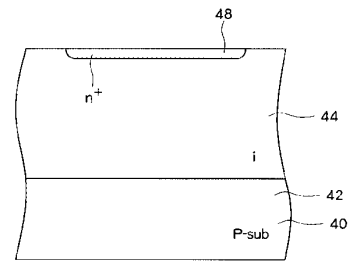
【图 8】



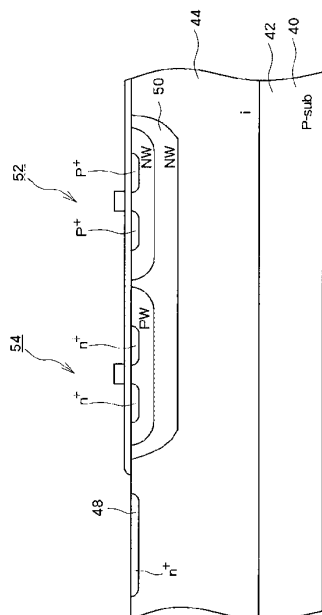
【図 9】



【図 10】



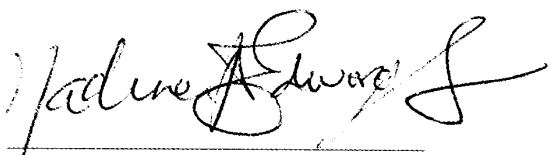
【図 11】



I, Nadine A. Edwards, declare as follows:

1. I am over 21 years of age and am competent to make this declaration.
2. I am a native speaker of English.
3. I am fluent in Japanese.
4. I have 14 years of experience translating Japanese to English.
5. I translated the attached patent document "JP2007129024A" from Japanese to English.
6. I certify that the above-mentioned translation of the document "JP2007129024A" is, to the best of my knowledge, a true and accurate translation from Japanese to English.
7. In signing this declaration, I understand that the translation and this declaration may be filed as evidence in a contested case. I acknowledge that I may be subject to cross-examination within the United States.
8. I declare under penalty of perjury that all statements made herein are true and accurate to the best of my knowledge and belief, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed: April 2, 2025

By: 
Nadine A. Edwards



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ELECTRONIC PAYMENT RECEIPT

APPLICATION #
19/036,506

RECEIPT DATE / TIME
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ATTORNEY DOCKET #
309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 4276

FILED BY Mary Ellen Finnegan

PATENT CENTER # 72308372

AUTHORIZED BY Gerard Wissing

CUSTOMER # 139982

FILING DATE 01/24/2025

CORRESPONDENCE
ADDRESS -

FIRST NAMED
INVENTOR Shih-Yuan WANG

Payment Information

PAYMENT METHOD
CARD / 8026

PAYMENT TRANSACTION ID
E20259FB53265631

PAYMENT AUTHORIZED BY
Mary Ellen Finnegan

PRE-AUTHORIZED ACCOUNT
600125

PRE-AUTHORIZED CATEGORY
37 CFR 1.21 (Miscellaneous fees and charges)

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
2806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	112.00	1	112.00
2253	EXTENSION FOR RESPONSE WITHIN THIRD MONTH, EXCEPT PROVISIONAL APPLICATIONS	636.00	1	636.00
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	19036506
	Filing Date	2025-01-24
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0015USCIPDIV2

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	2	20120033119		2012-02-09	Shinohara			
	3	20120153124		2012-06-21	Yu et al.			
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	19036506
	Filing Date	2025-01-24
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0015USCIPDIV2

	1	2002314116	JP		2002-10-25	Harada et al.		☐
	2	2007129024	JP		2007-05-24	Hasegawa		☐
	3	2172974	EP		2010-04-07	NXP B.V.		☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Yahaya, NA, Characterization of light absorption in thin-film silicon with periodic nanohole arrays, 11 March 2013/Vol. 21, No. 5/OPTICS EXPRESS 5924-5930. (7 pages)	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	19036506
	Filing Date	2025-01-24
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0015USCIPDIV2

TIMING STATEMENT			
Please see 37 CFR 1.97(e) to make the appropriate selection(s):			
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Signature	/Gerard M. Wissing/	Date (YYYY-MM-DD)	2025-09-16
Name/Print	Gerard M. Wissing	Registration Number	36,309

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	19036506
	Filing Date	2025-01-24
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0015USCIPDIV2

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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(12) Published Unexamined Patent Application (A)

Patent Owner, W&Wsens - Ex. 2034, p. 38

CLAIMS

1. A lateral-type semiconductor light-receiving element having a PIN structure in which interfaces between an i-layer and a p-layer and between the i-layer and an n-layer, respectively, of the PIN structure are formed perpendicular to a semiconductor substrate surface, and light that enters the i-layer is converted into electric current and detected, wherein:

a hole, which extends from a light-receiving surface to a prescribed depth of the i-layer, is provided in a light-receiving region.

DETAILED DESCRIPTION OF THE INVENTION

[0001]

TECHNICAL FIELD PERTAINING TO THE INVENTION

The present invention relates to a lateral-type semiconductor light-receiving element having a PIN structure.

[0002]

BACKGROUND ART

In a vertical-type photodiode, in which a p-n junction surface is formed parallel to a semiconductor substrate surface, light impinges a depletion layer after passing through a p-layer or an n-layer; in contrast, in a lateral-type photodiode, in which the p-n junction surface is formed perpendicular to the semiconductor substrate surface, light directly impinges the depletion layer (without passing through the p-layer or the n-layer). Consequently, the lateral-type photodiode is advantageous in that it has better light-receiving efficiency than the vertical-type photodiode.

[0003] Conventionally, an i-layer (intrinsic layer) is provided in the photodiode between the p-layer and the n-layer to make the depletion layer thick. In a vertical-type photodiode having this kind of PIN structure, the i-layer is formed to a thickness that is the absorption length or more to make the light-receiving sensitivity high. Thereby, a quantum efficiency of 70% or more can be obtained at wavelengths of approximately 700 nm to 870 nm.

[0004] A lateral-type photodiode having a PIN structure (a photodiode in which interfaces between the i-layer and the p-layer and between the i-layer and the n-layer of the PIN structure are formed to be perpendicular to the semiconductor substrate surface) is produced by, for example: providing a region, which has an extremely light impurity concentration and will become the i-layer, on a front surface portion of the semiconductor substrate; and then forming the p-layer and the n-layer by adding and diffusing p-type impurities and n-type impurities respectively from an upper surface at locations that are at a prescribed spacing from this region, wherein the spacing between both the layers remains as the i-layer.

[0005] Consequently, in the case of the lateral-type photodiode having a PIN structure, when attempting to make the thickness of the i-layer (the depth from a light-incident surface) large, the p-layer and the n-layer must also be formed deeply. To form the p-layer and the n-layer deeply while maintaining a uniform width (i.e., the distance between the p-layer and the n-layer) of the i-layer in the thickness direction of the substrate, the distance between the p-layer and the n-layer must be made large at the substrate front surface. When the distance between the p-layer and the n-layer is made large at the substrate front surface, the width of the i-layer becomes large. When the width of the i-layer is large, the migration distance for an electron generated on the p-layer side of the i-layer to the n-layer electrode becomes long, and the response speed becomes slow.

[0006] Accordingly, in the lateral-type photodiode having a PIN structure, making the thickness (the depth from the

light-incident surface) of the i-layer large cannot simply be adopted as a method of further increasing the light-receiving sensitivity. Consequently, providing an anti-reflection film on the upper surface of the i-layer and making the incidence efficiency of the i-layer high is effective as a method of further increasing the light-receiving sensitivity of the lateral-type photodiode having a PIN structure.

[0007]

PROBLEMS TO BE SOLVED BY THE INVENTION

However, there is a problem in that, in the lateral-type photodiode having a PIN structure, which has the anti-reflection film on the upper surface of the i-layer, the response speed becomes low in the situation in which the photodiode is used as an element for receiving high-speed light signals. In view of such problems in the related art, an object of the present invention is to improve light-receiving sensitivity of a lateral-type semiconductor light-receiving element having a PIN structure without causing a decrease in response speed.

[0008]

MEANS FOR SOLVING THE PROBLEMS

To solve the above-mentioned problem, the present invention provides a lateral-type semiconductor light-receiving element having a PIN structure in which interfaces between an i-layer and a p-layer and between the i-layer and an n-layer, respectively, of the PIN structure are formed perpendicular to a semiconductor substrate surface, and light that enters the i-layer is converted into electric current and detected, wherein a hole, which extends from a light-receiving surface to a prescribed depth (a shallower location than the depths of the p-layer and the n-layer) of the i-layer, is provided in a light-receiving region.

[0009]

EMBODIMENTS OF THE INVENTION

An embodiment of the present invention is explained below. FIG. 1 is a cross-sectional view that shows a photodiode corresponding to one embodiment of the present invention. FIG. 2 is a diagram that shows one example of a planar shape in the situation in which the photodiode of this embodiment is formed in an array. FIG. 1 corresponds to a cross-sectional view through line A-A in FIG. 2.

[0010] This photodiode is a lateral-type photodiode (semiconductor light-receiving element) in which a PIN structure is formed perpendicular to a substrate surface of a silicon substrate (semiconductor substrate) 1, and holes 4 are provided in a light-receiving region 2 (the region sandwiched between a p-layer 5 and an n-layer 7 of an i-layer 15), the holes 4 extending from a light-receiving surface 3 to a prescribed depth in the i-layer 15 and perpendicular to the surface of the silicon substrate 1.

[0011] A p-electrode 6 and an n-electrode 8 are formed on the upper surface of the p-layer 5 and the n-layer 7, respectively. A p-electrode 11 is formed on the lower surface of the silicon substrate 1. In addition, an element-protection layer 9, which is composed of a silicon oxide film or the like, is formed to a prescribed thickness on the upper surface of the silicon substrate 1 on portions outside of the locations having both of the electrodes 6, 8 and the holes 4. This photodiode can be produced, for example, by the following method.

[0012] First, an n-well (a region having an extremely low impurity concentration) 10 is provided on a surface-layer portion of the p-type silicon substrate 1. Next, p-type impurities are added to and diffused into one of two regions of the n-well 10, and n-type impurities are added to and diffused into the other region of the n-well 10, with a prescribed spacing between the two regions. Thereby, the p-layer 5 and the n-layer 7 are formed in the n-well 10, and a

portion of the n-well 10 that is between the p-layer 5 and the n-layer 7 remains as the i-layer 15. Next, the electrodes 6, 8 are formed on the p-layer 5 and the n-layer 7, respectively, and then the element-protection layer 9 is formed.

[0013] Next, a focused ion beam processing apparatus (FIB) is employed to irradiate the portion sandwiched by both the electrodes 6, 8 on the upper surface of the silicon substrate 1 with an ion beam so as to etch the element-protection layer 9 and the i-layer 15, thereby creating the holes 4, which extend from the light-receiving surface 3 to a prescribed depth (a location shallower than the depth of the p-layer 5 and the n-layer 7) in the i-layer 15 in the thickness direction of the silicon substrate 1.

[0014] Here, the dimension of the holes 4 in the direction between the p-layer 5 to the n-layer 7 is set to the dimension at which the i-layer 15 of a prescribed thickness exists between the holes 4 and the p-layer 5 and between the holes 4 and the n-layer 7, respectively. In addition, in the situation in which the light-receiving surface 3 between the pairs of electrodes is large, preferably a plurality of the holes 4 is provided within the light-receiving surface 3, as shown in FIG. 2. In this situation, for example, width W1 of each of the electrodes 6, 8 is 1 μm , spacing W2 between the electrodes 6, 8 is 2–4 μm , pitch K of the holes 4 is 2–4 μm , and the diameter of each of the holes 4 is 1 μm .

[0015] By connecting a power supply between the n-electrode 8 that contacts the upper surface of the n-layer 7 and the p-electrode 11 on the lower surface of the substrate 1, with the n-layer 7 side as the positive, applying a reverse-bias voltage, and connecting the p-electrode 6, which contacts the upper surface of the p-layer 5, to an output circuit, this photodiode can convert the light incident on the i-layer 15 from the light-receiving surface 3 into electric current to detect the light. In addition, in this photodiode, the light (a portion of which is shown in FIG. 1 by chain, double-dashed lines) that enters the interior of the hole 4 from the light-receiving surface 3 directly enters the light-receiving region 2 from a bottom surface and side surfaces of the hole 4, and by being reflected from the bottom surface and the side surfaces, the light travels from the bottom surface toward the side surfaces and enters the light-receiving region 2, and travels from one side surface toward the opposing side surface and enters the light-receiving region 2. Consequently, the light-receiving efficiency at the light-receiving region 2 becomes higher than in the situation in which no holes 4 are present.

[0016] In the situation in which the light-receiving surface 3 is merely made large without providing the holes 4 in order to make the light-receiving surface area large, the migration time increases for the electrons generated on the p-layer side of the i-layer to reach the electrode on the n-layer, and the response speed becomes slow because parasitic capacitance increases. In contrast, by providing the holes 4, the light-receiving surface area in this photodiode becomes larger, to the extent of the side surfaces of the holes 4, than in the situation in which no holes 4 are present. Consequently, in this photodiode, in no situation will the migration time for the electrons generated on the p-layer side of the i-layer to reach the electrode on the n-layer become longer than in the situation in which the light-receiving surface 3 is the same size with no holes 4 being provided. In addition, the parasitic capacitance of this photodiode becomes smaller than the situation in which the light-receiving surface 3 is the same

size with no holes 4 being provided. Hence, according to this photodiode, the light-receiving surface area can be made large and light-receiving efficiency can be made high without reducing response speed.

[0017] Furthermore, by having the holes 4, localized electric-field intensity applied to a portion of the i-layer 15 that surrounds the holes 4 becomes large in this photodiode. Thereby, compared with the situation in which there are no holes 4, response speed becomes faster because the light is absorbed at the portion of the i-layer 15 that surrounds the holes 4, and generated electron holes and electrons can migrate through the i-layer 15 at high speed. Accordingly, according to this photodiode, by providing the holes 4, the light-receiving efficiency at the light-receiving region 2 becomes high, which improves light-receiving sensitivity and also increases response speed.

[0018] It is noted that, although the lateral-type photodiode having a PIN structure is explained in this embodiment, the lateral-type semiconductor light-receiving element of the present invention, which has a PIN structure, is not limited thereto, and the present invention can also be applied to a lateral-type phototransistor, etc., in which the base and the collector portions have a PIN structure.

[0019]

EFFECTS OF THE INVENTION As explained above, according to the lateral-type semiconductor light-receiving element having a PIN structure according to the present invention, light-receiving sensitivity can be improved without causing a decrease in response speed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view that shows a photodiode corresponding to one embodiment of the present invention and is a diagram that corresponds to a cross-sectional view through line A-A in FIG. 2.

FIG. 2 is a diagram that shows one example of a planar shape in the situation in which the photodiode in FIG. 1 is formed in an array.

EXPLANATION OF THE REFERENCE NUMBERS

1	Silicon substrate (semiconductor substrate)
10	n-well
11	p-electrode
15	i-layer
2	Light-receiving region
3	Light-receiving surface
4	Hole
5	p-layer
6	p-electrode
7	n-layer
8	n-electrode
9	Element-protection layer

FIG. 1

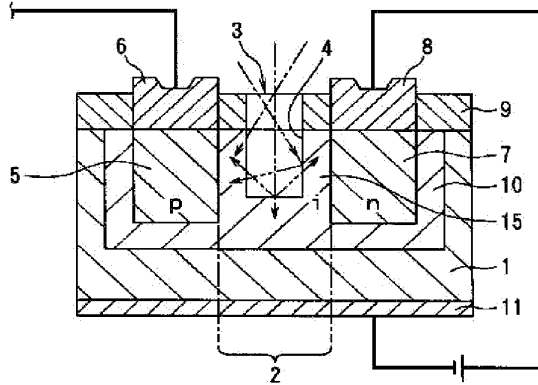
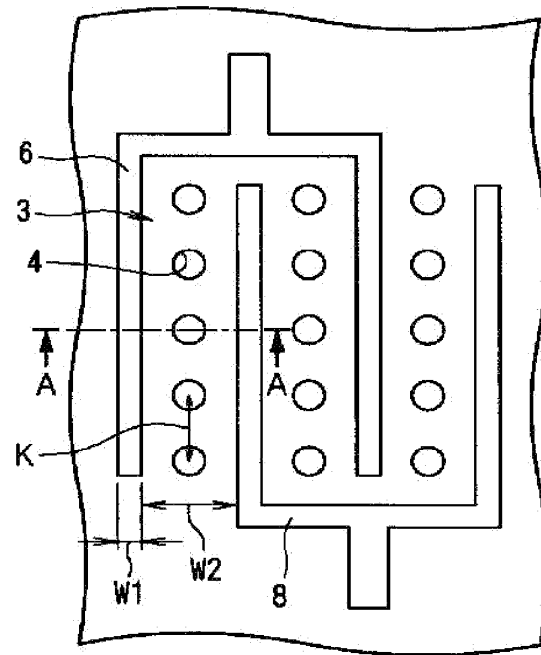


FIG. 2



Continuation of front page

(72) Inventor: Shojiro KITAMURA

F terms (reference) 5F049

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NA15

c/o SEIKO EPSON
CORPORATION
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Suwa City, Nagano

PA14 PA20 QA01 QA20
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(74) 代理人 100095728

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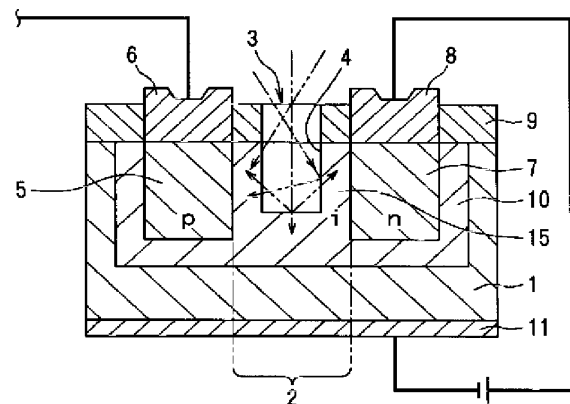
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(54) 【発明の名称】 P I N構造のラテラル型半導体受光素子

(57) 【要約】 (修正有)

【課題】 応答速度を低下させることなく受光感度を向上させたP I N構造のラテラル型半導体受光素子を提供する。

【解決手段】 P I N構造のi層15とp層5とn層7との界面が半導体基板面に対して垂直に形成され、i層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域2に、受光面3からi層15の所定深さまで延びる穴4を設けた。



【特許請求の範囲】

【請求項1】 P I N構造の i 層と p 層および n 層との界面が半導体基板面に対して垂直に形成され、 i 層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域に、受光面から i 層の所定深さまで延びる穴を設けたことを特徴とする P I N構造のラテラル型半導体受光素子。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、P I N構造のラテラル型半導体受光素子に関する。

【0002】

【従来の技術】p n 接合面が半導体基板面に対して平行に形成されている縦型フォトダイオードでは、p 層または n 層を通して空乏層に光が入射されるのに対して、p n 接合面が半導体基板面に対して垂直に形成されているラテラル型フォトダイオードでは、空乏層に直接 (p 層や n 層を介さずに) 光が入射される。そのため、ラテラル型フォトダイオードは縦型フォトダイオードよりも、受光効率の点で有利である。

【0003】従来より、フォトダイオードにおいては、p 層と n 層との間に i 層 (真性層) を設けて、空乏層を厚くすることが行われている。このような P I N 構造を有する縦型フォトダイオードでは、受光感度を高くするために、i 層を吸収長以上の厚さに形成することが行われている。これにより、波長 700 nm ~ 870 nm 前後において、70% 以上の量子効率が得られるようになる。

【0004】P I N 構造のラテラル型フォトダイオード (P I N 構造の i 層と p 層および n 層との界面が半導体基板面に対して垂直に形成されたフォトダイオード) は、例えば、i 層をなす不純物濃度の極めて薄い領域を半導体基板の表層部に設けた後、この領域の所定間隔を開けた各位置に、上面から p 型不純物及び n 型不純物をそれぞれ添加して拡散させることにより p 層及び n 層を形成し、両層の間を i 層として残すことによって作製される。

【0005】そのため、P I N 構造のラテラル型フォトダイオードの場合に i 層の厚さ (光入射面からの深さ) を大きくしようとすると、p 層及び n 層を深く形成する必要がある。基板の厚さ方向で i 層の幅 (p 層と n 層との距離) を均一に保持しながら、p 層及び n 層を深く形成するためには、基板表面での p 層と n 層との距離を大きくとる必要がある。基板表面での p 層と n 層との距離を大きくすると i 層の幅が大きくなる。i 層の幅が大きいと、i 層の p 層側で生じた電子が n 層の電極に達するまでの移動距離が長くなって、応答速度が遅くなる。

【0006】したがって、P I N 構造のラテラル型フォトダイオードでは、受光感度をより高くする方法とし

て、i 層の厚さ (光入射面からの深さ) を大きくすることを単純に採用することができない。そのため、P I N 構造のラテラル型フォトダイオードの受光感度をより高くする方法としては、i 層の上面に反射防止膜を設けて i 層への入射効率を高くすることが有効である。

【0007】

【発明が解決しようとする課題】しかしながら、i 層の上面に反射防止膜を有する P I N 構造のラテラル型フォトダイオードには、高速の信号を受光する素子とした場合に応答速度が低くなるという問題点がある。本発明は、このような従来技術の問題点に着目してなされたものであり、P I N 構造のラテラル型半導体受光素子において、応答速度を低下させることなく受光感度を向上させることを課題とする。

【0008】

【課題を解決するための手段】上記課題を解決するために、本発明は、P I N 構造の i 層と p 層および n 層との界面が半導体基板面に対して垂直に形成され、i 層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域に、受光面から i 層の所定深さ (p 層および n 層の深さより浅い位置) まで延びる穴を設けたことを特徴とする P I N 構造のラテラル型半導体受光素子を提供する。

【0009】

【発明の実施の形態】以下、本発明の実施形態について説明する。図1は本発明の一実施形態に相当するフォトダイオードを示す断面図である。図2は、この実施形態のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。図1は図2の A-A 線断面図に相当する。

【0010】このフォトダイオードは、P I N 構造がシリコン基板 (半導体基板) 1 の基板面に対して垂直に形成されたラテラル型フォトダイオード (半導体受光素子) であり、受光領域 (i 層 15 の p 層 5 と n 層 7 とで挟まれた領域) 2 に、受光面 3 から i 層 15 の所定深さまで、シリコン基板 1 面に垂直に延びる穴 4 が設けてある。

【0011】p 層 5 および n 層 7 の上面には、p 電極 6 および n 電極 8 がそれぞれ形成されている。シリコン基板 1 の下面には p 電極 11 が形成されている。また、シリコン基板 1 の上面の両電極 6, 8 および穴 4 の位置を除いた部分に、シリコン酸化膜等からなる素子保護層 9 が所定の厚さで形成されている。このフォトダイオードは、例えば以下の方法で作製できる。

【0012】まず、p 型のシリコン基板 1 の表層部に n ウエル (不純物濃度の極めて薄い領域) 10 を設ける。次に、n ウエル 10 の所定間隔を開けた 2 つの領域の一方に p 型不純物を、他方に n 型不純物をそれぞれ添加して拡散させる。これにより、n ウエル 10 に p 層 5 及び n 層 7 が形成され、n ウエル 10 の p 層 5 と n 層 7 との

間の部分がi層15として残る。次に、p層5及びn層7の上に電極6、8を形成した後、素子保護層9を形成する。

【0013】次に、集束イオンビーム加工装置(FIB)を用い、シリコン基板1上面の両電極6、8で挟まれた部分にイオンビームを照射して、素子保護層9とi層15をエッチングすることにより、受光面3からi層15の所定深さ(p層5およびn層7の深さより浅い位置)まで、シリコン基板1の厚さ方向に延びる穴4を開ける。

【0014】ここで、穴4のp層5-n層7間方向の寸法は、穴4とp層5との間および穴4とn層7との間にそれぞれ所定厚さのi層15が存在する寸法に設定する。また、各電極対間の受光面3が大きい場合には、図2に示すように、受光面3内に複数の穴4を設けることが好ましい。この場合には、例えば、電極6、8の幅W1を $1\mu\text{m}$ 、電極6、8の間隔W2を $2\sim 4\mu\text{m}$ 、穴4のピッチKを $2\sim 4\mu\text{m}$ 、穴4の直径を $1\mu\text{m}$ とする。

【0015】このフォトダイオードは、n層7の上面に接触するn電極8と基板1の下面のp電極11との間に、n層7側を正として電源を接続して逆バイアス電圧を付与し、p層5の上面に接触するp電極6を出力回路に接続することにより、受光面3からi層15に入射された光を電流に変換して検出することができる。また、このフォトダイオードでは、受光面3から穴4内に入射された光(一部を図1に2点鎖線で表示)は、穴4の底面や側面から受光領域2に直接入射するとともに、底面や側面で反射されることで、底面から側面に向かって受光領域2に入射されたり、側面から対向する側面に向かって受光領域2に入射されたりする。そのため、穴4が無い場合よりも受光領域2での受光効率が高くなる。

【0016】受光面積を大きくするために穴4を設けず単純に受光面3を大きくした場合には、i層のp層側で生じた電子がn層の電極に達するまでの移動時間が長くなるとともに、寄生容量が大きくなるため、応答速度が遅くなる。これに対して、このフォトダイオードでは、穴4を設けることで、穴4が無い場合よりも穴4の側面の分だけ受光面積が大きくなっている。そのため、このフォトダイオードでは、i層のp層側で生じた電子がn層の電極に達するまでの移動時間が、受光面3が同じ大きさで穴4を設けない場合よりも長くなることはない。また、このフォトダイオードの寄生容量は、受光面3が

同じ大きさで穴4を設けない場合よりも小さくなる。これらのことから、このフォトダイオードによれば、応答速度を遅くすることなく、受光面積を大きくして受光効率を高くすることができる。

【0017】さらに、このフォトダイオードは、穴4を有することによって、i層15の穴4の周囲部分に掛かる電界強度が局所的に大きくなっている。これにより、i層15の穴4の周囲部分で光を吸収して発生した正孔と電子はi層15を高速で移動することができるため、穴4の無い場合と比較して応答速度が速くなる。したがって、このフォトダイオードによれば、穴4を設けることによって、受光領域2での受光効率が高くなって受光感度が向上するとともに、応答速度も高くなる。

【0018】なお、この実施形態では、PIN構造のラテラル型フォトダイオードについて説明しているが、本発明のPIN構造のラテラル型半導体受光素子はこれに限定されず、ベースとコレクタの部分がPIN構造になっているラテラル型フォトトランジスタ等にも適用される。

【0019】

【発明の効果】以上説明したように、本発明のPIN構造のラテラル型半導体受光素子によれば、応答速度を低下させることなく受光感度を向上させることができる。

【図面の簡単な説明】

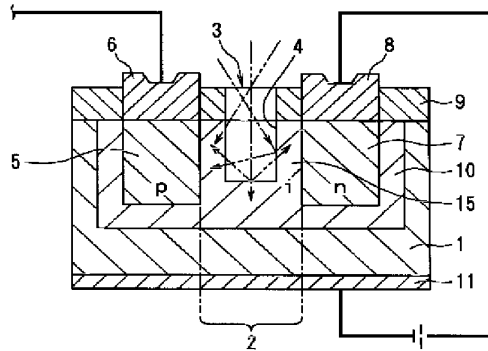
【図1】本発明の一実施形態に相当するフォトダイオードを示す断面図であって、図2のA-A線断面図に相当する図である。

【図2】図1のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。

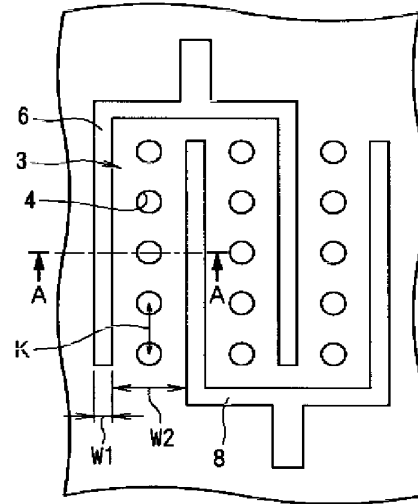
【符号の説明】

- 1 シリコン基板(半導体基板)
- 10 nウェル
- 11 p電極
- 15 i層
- 2 受光領域
- 3 受光面
- 4 穴
- 5 p層
- 6 p電極
- 7 n層
- 8 n電極
- 9 素子保護層

【図1】



【図2】



フロントページの続き

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Fターム(参考) 5F049 MA04 MB03 NA01 NA03 NA15
PA14 PA20 QA01 QA20 SZ13

I, Nadine A. Edwards, declare as follows:

1. I am over 21 years of age and am competent to make this declaration.
2. I am a native speaker of English.
3. I am fluent in Japanese.
4. I have 14 years of experience translating Japanese to English.
5. I translated the attached patent document "JP2002314116A" from Japanese to English.
6. I certify that the above-mentioned translation of the document "JP2002314116A" is, to the best of my knowledge, a true and accurate translation from Japanese to English.
7. In signing this declaration, I understand that the translation and this declaration may be filed as evidence in a contested case. I acknowledge that I may be subject to cross-examination within the United States.
8. I declare under penalty of perjury that all statements made herein are true and accurate to the best of my knowledge and belief, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed: April 2, 2025

By: 
Nadine A. Edwards

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Shih-Yuan WANG et al.
Serial No.: 19/036,506
Examiner: EDUARDO A RODELA
Group Art Unit 2893
Filing Date: 01/24/2025
For: MICROSTRUCTURE ENHANCED ABSORPTION
PHOTOSENSITIVE DEVICES
Conf. No. 4276

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CERTIFICATE OF ELECTRONIC FILING

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/Mary Ellen Finnegan/

(Signature of person signing transmittal)

RESPONSE TO OFFICE ACTION DATED 03/18/2025

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Amendments to the Claims begin on page 2; and

Remarks begin on page 5.

AMENDMENTS TO THE CLAIMS

Please cancel claims 1-17 and add the following claims 18-30:

18. (New) A structure comprising:

an array of elongated pillars of semiconductor material in which each of at least some of the pillars has:

- (i) a respective light-receiving surface,
- (ii) respective sides,
- (iii) width of 50-2000 nm,
- (iv) height of 100-10000 nm, and
- (v) at least one photodetector of Si, Ge, and/or alloyed SiGe semiconductor material formed in the pillar;

wherein each of the photodetectors:

- (i) has P-doped and N-doped regions of the semiconductor material,
- (ii) is configured to generate electrical charge carriers in the semiconductor material of the photodetector in response to light that (a) is in the visible and infrared wavelengths, and (b) illuminates along a light direction the light-receiving surface of the pillar in which the photodetector is formed;

one or more in-pillar holes each of which:

- (i) is fabricated as a recess in each of the pillars in which at least one of the photodetectors is formed, and
- (ii) extends along the light direction into the semiconductor material of the pillar in which the in-pillar hole is fabricated;

side-isolation comprising solid dielectric material between at least portions of the sides of at least some of the pillars;

electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for selected reverse-biasing at least some of the photodetectors;

wherein the presence of the in-pillar holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors in pillars lacking said holes.

19. (New) The structure of claim 18, in which the array is monolithically integrated with Si electronic devices.

20. (New) The structure of claim 18, in which at least one of the in-pillar holes in each of at least some of the pillars is elongated in the light direction.

21. (New) The structure of claim 18, in which each of at least some of the holes is elongated in a direction along the light-receiving surface of the pillar in which the hole is fabricated.

22. (New) The structure of claim 21, in which the array is monolithically integrated with Si electronic devices.

23. (New) The structure of claim 21, in which each of at least some of the pillars has a plurality of the elongated holes.

24. (New) The structure of claim 21, in which each of at least some of the pillars has only one of the elongated holes.

25. (New) The structure of claim 21, in which each of at least some of the elongated holes has at least one closed contour remote from side edges of the light-receiving surface of the pillar in which the hole is fabricated.

26. (New) The structure of claim 18, in which each of at least some of the pillars includes only one of the photodetectors.
27. (New) The structure of claim 18, in which two or more of the photodetectors are connected electrically in parallel.
28. (New) The structure of claim 18, wherein the array of pillars is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors.
29. (New) The structure of claim 18 in which at least some of the holes extend 100 to 10000 nm in the light direction into the semiconductor material of the pillars in which the holes are formed.
30. (New) The structure of claim 18, in which the pillars in which the photodetectors are formed are elongated in the light direction.

REMARKS

Priority and Paragraph 112(a)

Examples of support are outlined below in the subject application and in the 2013 provisional applications that are incorporated by reference and to which priority is claimed.

FIG. 5B of the subject application illustrates an example of an array of vertical pillars of semiconductor material such as Si, and FIG. 49 illustrates an example of an in-pillar hole (pillar with hole). Both are reproduced below.

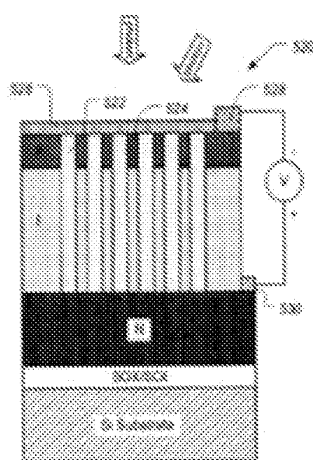


FIG. 5B

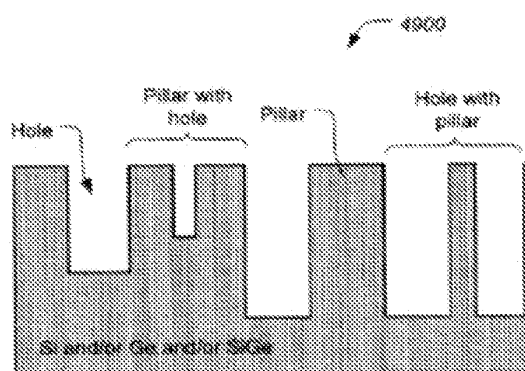


FIG. 49

As seen in FIG. 5B and explained in the text of the subject application, each pillar 524 has a light receiving surface that is on top of the pillar in this example, illuminated with light (photons) in the direction of one or both arrows, has sides, and has at least one photodetector of Si, Ge, or SiGe formed in the pillar.

The width of a pillar can be 50-2000 nm¹ and the height of a pillar can be 100-10000 nm.² Each photodetector has P-doped and N-doped regions and is configured to generate electrical charge carriers in the semiconductor material of the photodetector formed in the pillar in response to light that is in the visible and infrared wavelengths and illuminates the light-receiving surface of the pillar.

¹ Provisional application 61/826,446 filed May 22, 2013, page 12; "The shape of the pillar can be... rectangle.... The pillar diameter range from 50-2000 nm",

² Provisional application 61/826,446 filed May 22, 2013, page 12: "[P]illars can be 100-10000 nm in length...."

Each of the pillars in the array of FIG. 5B can be a “pillar with a hole” as in the example of FIG. 49.³ Each in-pillar hole extends into the pillar in the direction of the light, down into the pillar in this example.

Dielectric material 522 such as oxide forms solid isolation between pillar side walls and, with in-pillar holes in the pillars, fills at least a part of the holes,⁴ and the in-pillar holes can be oxidized.⁵ Electrical contacts as seen in the example of FIG. 5B provide pathways to the photodetectors and can reverse-bias them.⁶ The presence of the in-pillar holes increases absorption by a factor of at least 1.1 compared to like photodetectors without holes or to bulk semiconductor without holes.⁷

The array of pillars can be monolithically integrated with Si electronic devices.⁸ The in-pillar holes can be elongated – FIG. 46 of the subject application illustrates some examples of holes that are longer in one direction than in an orthogonal direction along the light-receiving surface of a pillar and additionally illustrate that a pillar can have a single hole or multiple holes and that at least one contour of a hole can be away from the outline of a pillar as seen in top view.⁹

Section 103

The references identified in the Office Action, page 8, post-date the 2013 priority of the subject application.

IPRs and PGR regarding commonly assigned patents

³ See also provisional application 61/826,446 filed May 22, 2013, page 16: “[T]he microstructure can have both pillars and holes coexist, can be concentric (pillar within a hole or hole within a pillar or multiple concentric hole/pillar, not necessarily circular....”

⁴ See also Figure 8 in page 6 of provisional application 61/826,446 filed May 22, 2013.

⁵ See also provisional application 61/826,446 filed May 22, 2013, page 16: “[P]artial filling of the holes with filler” Page 10: “[T]hermal oxidation of exposed surfaces”

⁶ See also provisional application 61/826,446 filed May 22, 2013, page 14: “The photodiode is reversed biased . . .”

⁷ Subject application paragraph 114 (factor of 1.1 to over 100), and provisional application 61/826,446 filed May 22, 2013, Table 8 in page 8, and page 16 (enhancement of the bulk absorption constant). Subject application paragraph [00114].

⁸ Provisional application 61/826,446 filed May 22, 2013, page 1: “Compatible with Si Photonics, CMOS processes ... integration with CMOS highly desirable.” Provisional application 61/834,873 filed June 13, 2013, pages 1-2: “[T]he detector array can be monolithically integrated with Si electronic devices such as bipolar transistors, CMOS”

⁹ See also Fig. 12 in provisional application 61/834,873 filed June 13, 2013.

IPR and PGR petitions were filed challenging claims in six patents in the family of the subject application,¹⁰ five of which are in a patent infringement action.¹¹

The references that the IPRs and the PGR assert are:

1. **Kuboi** US 2012/0049044
2. **Shinohara** US 2012/0033119
3. **Yu** US 2012/0153124
4. **Harada** Kokai No. 2002-314116 (P2002-314116A)
5. **Hasegawa** Kokai 2007-129024 (P2007-129024A)
6. **NXP** EP 2 172 974 A1
7. **Yahaya**, NA, Characterization of light absorption in thin-film silicon with periodic nanohole arrays, 11 March 2013/Vol. 21, No. 5/OPTICS EXPRESS 5924-5930.
8. **Vasylysev** US 2012/0012741

Applicant submits that claims 18-30 differ patentably from these seven references taken individually or in combination, at least because:

Kuboi proposes a standard semiconductor PIN photodiode 53R with no in-pillar holes and additionally proposes pixels 53R, 53G that generate electrical output only in organic material 13, not in semiconductor material of a photodetector. See Kuboi FIGs. 6A and 10A.

Shinohara proposes an array of standard photodiodes with no in-pillar holes.

Yu proposes nanowires or nanopillars that also lack in-pillar holes.

Harada proposes a lateral photodiode with no pillars along the light direction and no in-pillar holes.

Hasegawa proposes standard photodiodes, lacking in-pillar holes, used in optical disc drive tracking.

¹⁰ The IPRs are: (1) Case IPR2025-00993 on patent 12,087,871, (2) Case IPR2025-00994 on patent 11,621,360; (3) Case IPR2025-00995 on patent 10,468,543; (4) Case IPR2025-00996 on patent 10,446,700; and (5) Case IPR-00997 on patent 9,525,084. Applicant is concurrently submitting an IDS identifying the total of 7 references on which the 5 IPRs rely to challenge patentability under Sections 102 or 103. The PGR is Case PGR2025-00082 for patent 12,243,948.

¹¹ The action is: W&Wsens Devices Inc. v. Samsung Elecs. Co., Case No. 2:24-cv-00854-JRG (E.D. Tex.). Defendants have filed pleadings identifying purported prior art, which are available through Pacer. Applicant offers to any of the several hundred patents, published applications, and non-patent publication listed in such pleadings if the Office requests it.

NXP proposes standard photodiodes, with no in-pillar holes.

Yahaya proposes a solar cell panel with surface structures but lacks a teaching of pillars of semiconductor material that are electrically isolated from each other and have reverse-biased photodetectors fabricated in the pillars and in-pillar holes with solid dielectric material.

Vasylyev also proposes a solar cell panel with surface structures but lacks a teaching of pillars of semiconductor material that are electrically isolated from each other and have reverse-biased photodetectors fabricated in the pillars and in-pillar holes with solid dielectric material.

The Preliminary Amendment filed 01/24/2025 in the subject application addresses references cited in application Ser. No. 18/385,213, now patent 12,243,948. They are **Yu** US 2011/0309331), **Lunev** US 2014/001660, **Counil** US 2010/0116332, and **Arimoto** US 5,759,292. Applicant submits that claims 18-30 patentably differ from these references at least for the reasons discussed in the Preliminary Amendment filed 01/24/2025 but also for additional reasons.

Applicant invites the Examiner to telephone the undersigned if the Examiner finds that it may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

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(54) **Wavelength selective electromagnetic radiation detector using pores as photonic crystal**

(57) A device (100) for detecting electromagnetic radiation, the device (100) comprising a substrate (102), an electromagnetic radiation sensitive structure (104) arranged on and/or in the substrate (102), and a plurality of pores (106) formed on and/or in the substrate (102) in such a manner that electromagnetic radiation to be de-

tected propagates partly through the pores (106) before propagating into the electromagnetic radiation sensitive structure (104), wherein different ones of the plurality of pores (106) differ regarding at least one physical parameter so that each of the plurality of pores (106) is sensitive to an assigned wavelength range of electromagnetic radiation.

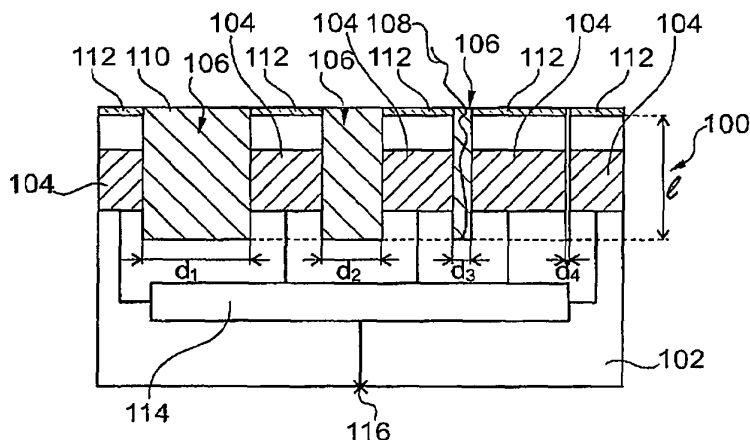


Fig. 6

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Description

FIELD OF THE INVENTION

- 5 [0001] The invention relates to a device for detecting electromagnetic radiation.
 [0002] Moreover, the invention relates to a method of detecting electromagnetic radiation.

BACKGROUND OF THE INVENTION

- 10 [0003] A PIN (P-type/Intrinsic/N-type or positive intrinsic negative) diode can be used as a photodiode. Under reverse bias, the diode ordinarily does not conduct. A photon entering the intrinsic region frees a carrier. The reverse bias field sweeps the carrier out of the region and creates a current. In order to make a wavelength detector, it may be necessary to filter the light before it reaches the intrinsic region.
- 15 [0004] US 5,726,440 discloses a wavelength selective photodetector including a substrate having a buried insulator layer for electrically isolating a lower section of the substrate located below the insulator layer from an upper section of the substrate located above the insulator layer, and a photon detector formed on the upper section of the substrate for detecting photons in a selected wavelength range, wherein the upper section has a selected thickness and the thickness determines at least in part the selected wavelength range of the detected photons.
- [0005] However, conventional wavelength selective photodetectors may lack sufficient detection accuracy.

OBJECT AND SUMMARY OF THE INVENTION

- [0006] It is an object of the invention to enable electromagnetic radiation detection with sufficient accuracy.
- 25 [0007] In order to achieve the object defined above, a device for detecting electromagnetic radiation, and a method of detecting electromagnetic radiation according to the independent claims are provided.
- [0008] According to an exemplary embodiment of the invention, a device for detecting electromagnetic radiation (such as light) is provided, the device comprising a substrate (such as a semiconductor wafer), an electromagnetic radiation sensitive structure (such as a photodiode) arranged on and/or in the substrate, and a plurality of pores (such as empty or filled trenches in a surrounding material) formed on and/or in the substrate in such a manner that electromagnetic radiation to be detected propagates through at least a part of the plurality of pores (for instance may be reflected once or several times at walls thereof) before propagating into (or penetrating into) the electromagnetic radiation sensitive structure (which structure may be arranged to extend deeper into the substrate or with a larger distance to a surface of the device, which surface is to be irradiated with the incoming electromagnetic radiation, than the plurality of pores), wherein different ones of the plurality of pores differ regarding at least one physical parameter so that each of the plurality of pores is sensitive to an assigned wavelength range of electromagnetic radiation (wherein assigned wavelength ranges of different pores or pore groups may be different or may be at least overlapping).
- 30 [0009] According to another exemplary embodiment of the invention, a method of detecting electromagnetic radiation is provided, the method comprising directing electromagnetic radiation to be detected towards a plurality of pores formed on and/or in a substrate in such a manner that the electromagnetic radiation to be detected propagates through at least a part of the plurality of pores, and subsequently propagating the electromagnetic radiation into an electromagnetic radiation sensitive structure arranged on and/or in the substrate, wherein different ones of the plurality of pores differ regarding at least one physical parameter so that each of the plurality of pores is sensitive to an assigned wavelength range of the electromagnetic radiation.
- 40 [0010] The term "substrate" may denote any suitable material, such as a semiconductor, glass, plastic, etc. According to an exemplary embodiment, the term "substrate" may be used to define generally the elements for layers that underlie and/or overlie a layer or portions of interest. Also, the substrate may be any other base on which a layer is formed.
- [0011] The term "electromagnetic radiation" may particularly denote photons in an appropriate wavelength range. In an embodiment, such an electromagnetic radiation may be in a range between 400 nm and 800 nm, so that optical light is the electromagnetic radiation then. However, alternatively, other wavelength ranges are possible such as ultraviolet radiation, infrared radiation or the like. For instance for silicon, a usable electromagnetic radiation range goes from 190 nm to 1100 nm. However, with other materials for photodetectors, ranges can be different and may, for example, be extended to far infrared or far ultraviolet.
- 50 [0012] The term "pore" may particularly denote a trench formed in and/or on a substrate and having an aspect ratio, which is defined by the ratio between depth of the trench in the substrate and diameter of the trench in a surface portion of the substrate. For instance, such pores may have a cylindrical shape or alternatively may have a rectangular cross section, an oval cross section, a polygonal cross section or the like. In an embodiment, the aspect ratio may be larger than three, particularly larger than five, more particularly larger than ten. A diameter of the pores may be less than 1000 nm, particularly less than 700 nm. Generally, it may be advantageous to use, as a diameter dimension, a value in the

order of the wavelength to get a sufficiently pronounced diffraction effect. For instance, a 700 nm hole may particularly impact radiation of about 700 nm wavelength. The term "electromagnetic radiation sensitive structure" may particularly denote a member, which is capable of detecting electromagnetic radiation such as a CMOS sensor, a CCD pixel, or the like. For instance, photodiodes (such as a simple pn-junction) may be used for such detection purposes. However, alternative detection options are possible as well.

[0013] The term "physical parameter" may particularly denote any physical or structural or dimensional property of the pores, which may have an impact on the propagation characteristics of electromagnetic radiation of a certain wavelength in the pore. Such a physical parameter may change the propagation characteristics of electromagnetic radiation depending on the wavelength of the electromagnetic radiation. Examples for such a physical property are a diameter of the pores, a geometry of the pores, a depth of the pores, an aspect ratio of the pores, a surface area of the pores, a material filled in the pores, etc.

[0014] According to an exemplary embodiment, the detection of electromagnetic radiation in a wavelength specific manner is possible. For this purpose, pores having different physical parameters such as geometrical parameters or material parameters may be provided, for example pores having different diameters. The propagation properties of the electromagnetic radiation within the pores may depend particularly on the wavelength of the electromagnetic radiation so that each of the pores may be used as a wavelength specific filter being sensitive only to electromagnetic radiation in a specific wavelength range or of a specific wavelength. Thus, by providing multiple pores having different physical properties, each pore may be used as a band-pass filter in a dedicated or assigned wavelength range.

[0015] In an embodiment, a wavelength detector in silicon may be provided. Such an embodiment may combine a PIN (P-type/Intrinsic/N-type or positive intrinsic negative) diode with pore technology to manufacture the wavelength detector. A gist of an embodiment is to make holes of different diameters in a vertical PIN structure and to use diffraction to select wavelength and recombination of electron-hole pair in the intrinsic region.

[0016] With silicon electronics, it is possible to make a wavelength detector performing a feedback loop function on a complete solid state lighting solution. Phototransistors may serve as a good detector, but have a low internal gain (compared to a photodiode). So a large area may be necessary. Embodiments of the invention may allow making very small wavelength detectors in silicon that can be integrated in a small package. The trend to use solid-state lighting like LEDs is increasing as it has a very small footprint and is very efficient. Their major drawback is the intensity variation due to environmental factors like temperature, aging, etc. By putting a very small light detector near the light source (a mobile phone flash for example), this can control a feedback loop to control the intensity or wavelength of the light flux. It is also possible to integrate embodiments of the detector with passive electronics and with LED drivers to obtain a low cost solution. A corresponding packaging may be more reliable and smaller and may be simple in manufacture.

[0017] Because of integration of sensor and LEDs, calibration may be done by manufacturers and not by an end user who is buying LED and sensors separately. The benefit of a PIN diode is that the depletion region exists almost completely within the intrinsic region, which is a constant width (or almost constant) regardless of the reverse bias applied to the diode. This intrinsic region can be made large, increasing the area where electron-hole pairs can be generated. For these reasons many photodetector devices may include at least one PIN diode in their construction, for example PIN photodiodes and phototransistors (in which the base-collector junction is a PIN diode).

[0018] Next, further exemplary embodiments of the device will be described. However, these embodiments also apply to the method.

[0019] The plurality of pores may be formed to extend parallel to one another. For example, the pores may be arranged in a row or in a matrix-like manner on a surface of the substrate. An alignment direction of the pores may be parallel to one another and perpendicular to a surface of the substrate so that the manufacture of all pores is possible with a common lithography procedure. The electromagnetic radiation to be detected may be directed perpendicular to the surface of the substrate or basically parallel to an alignment of the pores.

[0020] Different ones of the plurality of pores may have a different diameter or a different surface area in a surface plane of the substrate, which surface is to be irradiated with the incoming electromagnetic radiation. For example, first pores may have a first diameter, second pores may have a second diameter differing from the first diameter, third pores may have a third diameter differing from the first and the second diameter, etc. In this context, a diameter may be the diameter of a circle in a surface of the pore, may be the length of a diagonal of a rectangle, or the like.

[0021] Different ones of the plurality of pores may extend up to a different depth into the substrate, which depth may be calculated as a distance from a surface to be irradiated with the incoming electromagnetic radiation. Also by modifying the depth up to which the pores extend into the substrate, the wavelength specific propagation characteristic of the different pores may be further refined, involving another design parameter for a wavelength filter or a wavelength specific detector. For example, by using different aspect ratios for the different pores, it is possible that some of the pores extend into layers into which other pores do not extend. This may allow to define the specific wavelength selective properties with high accuracy.

[0022] A cross-section of the pores may be constant along the extension of the pores into the substrate.

[0023] The plurality of pores may be grouped into groups of pores. Pores of each one of the groups may have a

common diameter in a surface plane of the substrate and may extend up to a different depth into the substrate. Hence, for the different pores of a common group, the same pore diameter may be used but different extensions in a vertical direction. On the other hand, pores of different ones of the groups may have a different diameter in a surface plane of the substrate. Hence, a two-dimensional array of pores may be provided, wherein one design parameter is the diameter and another design parameter is the depth up to which the pores extend into the substrate. By taking this measure, a highly wavelength selective filter may be obtained.

[0024] The plurality of pores may be trenches extending perpendicular with respect to a main surface of the substrate. The main surface may be the surface at which a semiconductor wafer is usually processed. Vertical pores can be formed in such a semiconductor substrate as trenches by a lithography and etching procedure.

[0025] The plurality of pores may be at least partially filled with a filling material being transparent for the electromagnetic radiation, particularly being optically transparent. Such a material, for instance silicon dioxide as a CMOS compatible material, may fill the pores so that the device is not prone to dust or dirt. However, other materials may be appropriate as well, for instance a silicon filled material such as polysilicon. More generally, any appropriate semiconductor material such as polysilicon, silicon dioxide, silicon nitride, germanium, may be used. Hence, the filling material may be selected so as to not influence the detection purposes, but to provide for a mechanical stable structure, which can even be employed under harsh conditions. In another embodiment, the filling material of the pores may be used as a design parameter for adjusting the wavelength-dependent propagation properties of the pores. In still another embodiment, the pores may remain unfilled, that is may remain hollow bodies.

[0026] The electromagnetic radiation sensitive structure may comprise a photodiode structure, particularly a photodiode such as a PIN photodiode or a PN photodiode. Such a structure can be formed as a layer structure with simple deposition procedures known from semiconductor technology, wherein an orientation of such layers may be perpendicular to an extension of the trenches as the pores. A photodiode can simply be formed by correspondingly doping different portions of a semiconductor substrate, thereby providing for a pn-junction. Upon irradiation with electromagnetic radiation such as light, electron-hole pairs may be generated at the pn-junction, which can be detected as a fingerprint of the presence of the corresponding electromagnetic radiation.

[0027] The electromagnetic radiation sensitive structure may comprise a stack of layers differing regarding a doping profile of the respective layer, wherein the plurality of pores may be formed to penetrate through at least a part of the layers. For example, the layers may be planar layers which are formed on top of the substrate, and the pores may be formed at least partially in this layer stack perpendicular to a sequence of application of the layers. By taking this measure, simple and well-known manufacture procedures of silicon technology may be employed and simultaneously a powerful wavelength selective filter may be formed.

[0028] A thickness of at least a part of the layers may differ in portions adjacent to different ones of the plurality of pores. By forming the layers of different thicknesses, it is possible that adjacent pores are neighbored to different thicknesses of a respective material, for instance an n-doped material and/or a p-doped material. This may have an influence on the interaction between surrounding matter and the electromagnetic radiation, thereby further refining the wavelength selectivity of the system.

[0029] The device may comprise a patterned cover layer arranged to expose the plurality of pores and to cover surface portions between adjacent ones of the plurality of pores. Such a patterned cover layer may be arranged on top (or close to the top) of the layer sequence forming the device and may prevent electromagnetic radiation from propagating into portions between adjacent pores, which could deteriorate the detection performance.

[0030] Such a cover layer may, for instance, have electrically conductive properties so as to allow serving as electrodes for the photodiodes as well. When such a cover layer is made of an opaque material, it can have a shielding effect preventing optical light to propagate through portions between the pores, which could result in undesired crosstalk.

[0031] It is also possible to provide a cover layer made of an anti-reflective material (at least above the pores) so as to prevent reflection of electromagnetic radiation to thereby improve the detection efficiency. Hence, the amplitude of the detection signals may be kept sufficiently large.

[0032] The device may comprise a signal processing circuit formed on and/or in the substrate and being adapted for processing detection signals generated by the electromagnetic radiation sensitive structure. Such a signal processing circuit may be monolithically integrated within the substrate and may comprise active and/or passive electric components, for instance may comprise resistors, capacitances, transistors, logic gates, memory cells, processors, or the like. Hence, it is possible that the signal processing circuit processes the signal provided by the electromagnetic radiation sensitive structure to evaluate the wavelength dependence of the impinging electromagnetic radiation. In an embodiment (see for instance Fig. 15), all devices are fully integrated on a silicon wafer. This may be called SoC (System on Chip). SoC is advantageous regarding parasitic effects. In another embodiment (see Fig. 16), devices are mounted on a support, this may be called SiP (System in Package). SiP may be preferred for ease of process.

[0033] In an embodiment, the electromagnetic radiation sensitive structure may be realized as a photodiode which may be electrically biased by a bias voltage to enable accurate detection of electric signals in response to the presence of electromagnetic radiation.

[0034] For example, the device may additionally comprise an electromagnetic radiation source such as a light emitting diode (LED) which may be adapted for generating electromagnetic radiation such as light and may be controlled by a control signal generated by the signal processing circuit based on the detection signals. Hence, a combined light emitting diode and photodetector may be manufactured which allows to regulate the emission characteristics of the light emitting diode based on the detected signal of the light emitting diode which allows for a wavelength specific analysis of the emission characteristic of the light source.

[0035] For example, the device may be monolithically integrated in and/or on the substrate. Hence, at least a part of the components of the device may be manufactured in semiconductor technology or microprocessing technology and the resulting system may be very small in size.

[0036] An embodiment of the invention may use the fundamental physical laws of diffraction of light in a hole combining to a vertical PIN diode. Choosing the right design and silicon electronics can result in a variety of devices. In an embodiment, it is possible to make a specific wavelength detector with two different diameters only. Other possible applications are a wide range light detector to measure the absolute intensity of a light source. For example, it can be used to tune the flash intensity by a feedback loop. Another application is a light filter for wavelengths below or above a specific value. If the detector is used for a non-mobile application, the detector can be put far away from the light source. It can be used as a presence detector. Any other applications are possible as well.

[0037] In an embodiment, a completely integrated silicon solution may be provided which may be more reliable than a discrete solution. This may allow for a better control due to submicron patterning. Embodiments of the invention may be applied to mobile applications where small packaging is advantageous. According to an embodiment, with a unique process, any kind of wavelength detector can be made as it is only depending of the via diameter. It is even possible to make different detectors on the same silicon wafer. Furthermore, it is possible to use standard semiconductor processes with standard dimensions and standard material. With a silicon wafer, the wavelength detection range may be from 190 nm (or less) to 1100 nm (or more). For higher wavelength detection (above 1 μm), a device made from germanium may be advantageous.

[0038] Embodiments of the invention may have advantages such as excellent linearity of output current as a function of incident light, a spectral response from 190 nm (or less) to 1100 nm (or more), low noise, robustness to mechanical stress, long lifetime, high quantum efficiency (typically 80% or more), and no high voltage required.

[0039] As the detector may be designed in a silicon substrate by deep silicon etch, it is possible to reach a high-density detector compared to a planar detector, and it may be possible to compensate a low gain. In an embodiment, it is possible to combine pore etching and PIN junction formation to realize a wavelength filter.

[0040] By a unique process, it may be possible to create different diameter holes (just by using a lithography mask), so it is possible to detect several wavelengths. As different diameter holes may be used at the same time, any drift in a lithographic step would be the same for all detector elements, meaning that one single offset would be obtained for all detectors. As it is a silicon process, it is possible to add active and passive components on the silicon. It is possible to get a complete integrated solution of a detector and a signalprocessing module. The combination of a multiple wavelength detector coupled with a signalprocessing module allows sampling.

[0041] In an embodiment, as the signal detection is a function of the hole diameter but also the depth of the intrinsic zone, it is possible to design a matrix of detectors with rows of various diameter hole and columns of various depth of intrinsic zone. This may improve the wavelength selection range for a better sampling performance. It is possible to use pore technology to make a very accurate detector thanks to a lithography resolution and to a thin film deposition control.

[0042] The manufacturing method may be carried out in CMOS technology, since the described procedures are compatible with CMOS technology.

[0043] For any method step, any conventional procedure as known from semiconductor technology may be implemented. Forming layers or components may include deposition techniques like CVD (chemical vapour deposition), PECVD (plasma enhanced chemical vapour deposition), ALD (atomic layer deposition), or sputtering. Removing layers or components may include etching techniques like wet etching, vapour etching, etc., as well as patterning techniques like optical lithography, UV lithography, electron beam lithography, etc.

[0044] Embodiments of the invention are not bound to specific materials, so that many different materials may be used. For conductive structures, it may be possible to use metallization structures, silicide structures or polysilicon structures. For semiconductor regions or components, crystalline silicon may be used. For insulating portions, silicon oxide or silicon nitride may be used.

[0045] The structure may be formed on a purely crystalline silicon wafer or on an SOI wafer (Silicon On Insulator).

[0046] Any process technologies like CMOS, BIPOLAR, BICMOS may be implemented.

[0047] The aspects defined above and further aspects of the invention are apparent from the examples of embodiment to be described hereinafter and are explained with reference to these examples of embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

[0048] The invention will be described in more detail hereinafter with reference to examples of embodiment but to which the invention is not limited.

Fig. 1 and Fig. 2 show a geometrical condition illustrating an interaction of electromagnetic radiation with a pore.
 Fig. 3 shows intensities for different wavelengths as a function of depth for a via diameter of 0.5 μm and shows that for certain depths, attenuation is depending of the wavelength.
 Fig. 4 shows intensities for different wavelengths as a function of depth for a via diameter of 0.6 μm , so that by subtracting the intensity of hole of 0.6 μm and 0.5 μm it is possible to clearly differentiate wavelengths :
 Fig. 5 shows subtraction of intensity of a 0.6 μm hole minus intensity of a 0.5 μm hole for 300 nm and 400 nm light and shows that it is possible to extract UV-B light intensity (280 nm to 315 nm) from a light source.
 Fig. 6 illustrates a wavelength selective filter according to an exemplary embodiment of the invention.
 Fig. 7 to Fig. 13 show cross-sectional views of layer sequences obtained during a method of manufacturing a wavelength selective filter according to an exemplary embodiment of the invention.
 Fig. 14 shows a plan view of a wavelength selective filter according to an exemplary embodiment of the invention.
 Fig. 15 to Fig. 17 show cross-sectional views of wavelength selective filters in combination with a light emitting diode according to exemplary embodiments of the invention.
 Fig. 18 and Fig. 19 show a wavelength selective characteristic of a system according to an exemplary embodiment of the invention.
 Fig. 20 shows a cross-sectional view of a wavelength selective filter according to an exemplary embodiment of the invention.

DESCRIPTION OF EMBODIMENTS

[0049] The illustration in the drawing is schematical. In different drawings, similar or identical elements are provided with the same reference signs.

[0050] Embodiments of the invention allow for diffraction in a micrometric cylindrical trench.

[0051] Diffraction refers to various phenomena associated with the bending of waves when they interact with obstacles in their path. Its effects are generally most pronounced for waves where the wavelength is in the order of the size of the diffracting objects. Diffraction is based on the Huygens-Fresnel principle which predicts the future position of a wave when its earlier position is known. Every point on a wave front can be considered as a source of tiny wavelets that spread out in the forward direction at the speed of the wave itself. The new wave front is the envelope of all the wavelets - that is, tangent to them.

[0052] In optics, Fresnel diffraction or near-field diffraction is a process of diffraction which occurs when a wave passes through an aperture and diffracts in the near field, causing any diffraction pattern observed to differ in size and shape, relative to the distance. It occurs due to the short distance in which the diffracted waves propagate. When the distance is increased, outgoing diffracted waves become planar and Fraunhofer diffraction occurs. In the following, calculations of the magnitude of the electric field given by Fresnel integral in application of Huygens-Fresnel principle in a cylindrical trench will be explained. The diffracted light from the aperture of the cylindrical trench is absorbed by the silicon lateral surface and by a photon-electron interaction can generate a built-in potential in the semiconductor.

[0053] The diffraction angles depend on the wavelength and on the size of the diffracting object. As a consequence, the magnitude of the electric field along the side surface of the cylindrical trench at a fixed distance of the aperture depends on the wavelength.

[0054] Next, wave magnitude calculation will be described.

[0055] In application of Huygens-Fresnel principle in a circular aperture, the phase and amplitude of each of the Huygens wavelets at each point P in space is given by a double integral in cylindrical coordinates.

[0056] This is indicated schematically in Fig. 1:

$$A(\rho) = \int_{\theta} \int_r \frac{1}{r} A(\theta, r) \exp j \frac{2\pi r}{\lambda} \cos(r, z) r d\theta dr \quad (1)$$

[0057] In a circular aperture, A(p) is supposed independent of the angle Φ . Along the side surface of the cylindrical trench, the elementary surface at each point P introduces the angle α between p and the perpendicular radius.

[0058] The double integral is calculated in the cylindrical trench as represented in Fig. 2. Every point on the circular aperture can be considered as a source each point with the same amplitude K.

[0059] The phase and amplitude of each of the Huygens wavelets at each point P along the side surface of the cylindrical trench at a fixed distance z of the aperture is given by a double integral

$$A(P) = K \int_{\theta} \int_r \frac{1}{\rho} \exp j \frac{2\pi \rho}{\lambda} (\cos \alpha) (\cos \beta) r d\theta dr \quad (2)$$

[0060] Herein, α is the angle between ρ and the perpendicular radius at P, and a is the radius of the aperture

$$M = \begin{bmatrix} r \cos \theta \\ r \sin \theta \\ 0 \end{bmatrix} \quad P = \begin{bmatrix} a \\ 0 \\ z \end{bmatrix}$$

$$\rho = [(a - r \cos \theta)^2 + (r \sin \theta)^2 + z^2]^{1/2} \quad (3)$$

$$\cos \alpha = \left(\frac{a - r \cos \theta}{\rho} \right) \quad (4)$$

$$\cos \beta = \frac{z}{\rho} \quad (5)$$

$$A(P) = 2K \int_0^{\pi} \int_0^a \frac{1}{\rho} \exp j \frac{2\pi \sqrt{(a - r \cos \theta)^2 + (r \sin \theta)^2 + z^2}}{\lambda} \left(\frac{a - r \cos \theta}{\rho} \right) \frac{z}{\rho} r d\theta dr \quad (6)$$

[0061] $A(P)$ is a complex number with phase and amplitude at each point P. The complete amplitude in a nano-ring dz along the side surface of the cylindrical trench is:

$$\left[\int_0^{2\pi} A(P) a d\phi \right] dz = a 2\pi A(P) dz \quad (7)$$

[0062] The intensity of light at each point P in space is:

$$I(p) = A(P)A(P)^* = |A(P)|^2 \quad (8)$$

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[0063] Simulations of equation (6) are presented with following parameters: aperture radius $0.5 \mu\text{m}$ z varies from $0.05 \mu\text{m}$ to $2 \mu\text{m}$.

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λ_1	λ_2	λ_3	λ_4	λ_5
$0.3 \mu\text{m}$	$0.4 \mu\text{m}$	$0.5 \mu\text{m}$	$0.6 \mu\text{m}$	$0.7 \mu\text{m}$
$A_{1a}(z)$	$A_{2a}(z)$	$A_{3a}(z)$	$A_{4a}(z)$	$A_{5a}(z)$

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[0064] Fig. 3 shows a diagram 300 having an abscissa 302 along which a z axis distance is plotted in μm . Along an ordinate 304, A-values corresponding to λ_1 to λ_5 are plotted.

[0065] Aperture radius $0.6 \mu\text{m}$ z varies from $0.05 \mu\text{m}$ to $2 \mu\text{m}$

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λ_1	λ_2	λ_3	λ_4	λ_5
$0.3 \mu\text{m}$	$0.4 \mu\text{m}$	$0.5 \mu\text{m}$	$0.6 \mu\text{m}$	$0.7 \mu\text{m}$
$A_{1b}(z)$	$A_{2b}(z)$	$A_{3b}(z)$	$A_{4b}(z)$	$A_{5b}(z)$

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[0066] Fig. 4 shows a diagram 400 having an abscissa 302 along which a z axis distance is plotted in μm . Along an ordinate 304, A-values corresponding to λ_1 to λ_5 are plotted.

[0067] Fig. 5 shows a diagram 500 having an abscissa 302 along which a z axis distance is plotted in μm . Along an ordinate 502, differential amplitudes are plotted.

[0068] Fig. 6 illustrates a device 100 for detecting a light beam 108 in a wavelength selective manner according to an exemplary embodiment of the invention.

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[0069] The wavelength selective filter 100 comprises a silicon substrate 102. A photodiode 104 as a light sensitive structure is embedded within the silicon substrate 102. The photodiode 104 may be formed by a number of horizontally deposited planar layers which are doped accordingly. A plurality of trenches or pores 106 are formed in a surface portion of the substrate 102 in order to penetrate through the layers forming the photodiode 104. As can be taken from Fig. 6, the pores 106 have different diameters $d_1 > d_2 > d_3 > d_4$ and are formed by a common lithography and etching procedure in the substrate 102, more precisely in a surface portion of the substrate 102 including the photodiode layer sequence 104. As can be further taken from Fig. 6, all of the pores 106 extend up to the same depth, 1, into the substrate 102.

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[0070] Since the inner diameters d_1, d_2, d_3, d_4 of the pores 106 differ, the light detection properties are wavelength selective and different for each of the pores 106, so that each of the pores 106 is capable of detecting a specific wavelength range of impinging light 108.

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[0071] The combination of the detection signals of all pores 106 may allow to obtain wavelength-resolved information about a spectrum of the light 108.

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[0072] The pores 106 are formed parallel to one another in the substrate 102 and have the different diameters d_1, d_2, d_3, d_4 in a surface plane of the substrate 102. Since all of them have the same depth 1 in the substrate 102, their aspect ratios are different. The pores 106 are formed as trenches extending perpendicular to a main surface of the substrate 102 and perpendicular to the layer sequence 104 forming the photodiode. The pores 106 are filled with silicon dioxide material or any other semiconductor-based material as an optically transparent material so that the light beam 108 impinging on the device 100 can propagate through the filling material 110.

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[0073] A patterned cover layer 112 covers surface portions of the layer sequence between adjacent pores 106 to absorb electromagnetic radiation impinging between different ones of the pores 106 to further increase the signal-to-noise ratio. The opaque top layer 112 may further be electrically conductive so as to serve as an electrode for contacting the photodiodes 104 or other components of the integrated circuit 100, if desired or necessary.

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[0074] A signal processing unit 114 is provided as a buried integrated circuit within the silicon substrate 102 and is supplied with the detection signals from the photodiode 104. The processing circuit 114 may evaluate the wavelength characteristic of the detected light 108 and may output, at an interface 116, a signal indicative of the result of the detection. The output at the interface 116 may alternatively also be used for control purposes, for instance for controlling a light emitting diode.

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[0075] In the following, referring to Fig. 7 to Fig. 13, a method of manufacturing a device according to an exemplary embodiment will be explained. Such a manufacturing method may result in a colour filter which may serve for light emitting diode control purposes.

[0076] In Fig. 7 to Fig. 13, a common silicon substrate 102 is processed to manufacture a λ_1 wavelength detector 700 and a λ_2 wavelength detector 702, wherein $\lambda_1 \neq \lambda_2$.

[0077] Fig. 7 shows a layer sequence 704 obtained by PIN epitaxy applied to a silicon substrate 102, thereby forming an n⁺-doped layer 708 on the silicon substrate 102, followed by an intrinsic layer 710 and a p⁺-doped layer 712. Starting from the silicon substrate, the PIN structure 708, 710, 712 is grown by epitaxy (n⁺-silicon region 708, intrinsic region 710 and p⁺-region 712).

[0078] In order to obtain a layer sequence 800 shown in Fig. 8, trenches 106 are formed to entirely penetrate through layers 712, 710, and to partially penetrate into layer 708. These trenches 106 may be formed by a deep silicon etch. The deep silicon via holes 106 are formed into the PIN structure 708, 710, 712. Diameters of the holes 106 are different from one to another area in order to detect different wavelengths.

[0079] In order to obtain a layer sequence 900 shown in Fig. 9, light transparent silicon dioxide or another transparent semiconductor-based material 902 is deposited on the layer sequence 800 to fill the trenches 106.

[0080] In order to obtain a layer sequence 1000 shown in Fig. 10, the deposited silicon oxide material may be etched back, for instance using CMP (Chemical Mechanical Polishing), wherein silicon is at the top of the trench. In another embodiment, when silicon shall be used as a stop layer, it may be possible to add a dummy layer to stop CMP to get selectivity.

[0081] Hence, in Fig. 9, the holes 106 are filled with light transparent material 902 (such as undoped silicon, silicon dioxide SiO₂), and in Fig. 10 a back etching (etching without litho mask) is performed to remove this material 902 on top of the p⁺-region 712.

[0082] In order to obtain a layer sequence 1100 shown in Fig. 11, an opaque/metal layer 1102 is deposited over the layer sequence 1000. As a material for the metal layer 1102, aluminium or tungsten may be used, for instance.

[0083] In order to obtain a layer sequence 1200 shown in Fig. 12, the cover layer 1102 is patterned to expose the pores 106.

[0084] Referring to Fig. 11 and Fig. 12, the metal layer 1102 or opaque material is deposited and patterned only on the detector area 106.

[0085] In order to obtain a device 1300 according to an exemplary embodiment as shown in Fig. 13, a silicon nitride layer 1302 is deposited on a surface of the layer sequence 1200, which silicon nitride layer 1302 acts as an antireflective coating on the openings 108 but also as a passivation layer.

[0086] The described process flow does not show the interconnects to collect current from light. Based on theoretical calculations, it is possible to make numerical computing to get values to make the layout of the detector.

[0087] A corresponding design may be such that the PIN diodes 708, 710, 712 have an intrinsic region 710 buried between 0.5 μm and 1 μm into the silicon with a hole 106 diameter of 600 nm for one circuit part and 500 nm for the other circuit part. For UV-B light source, the current intensity of the 600-nm-hole circuit (A1 and A2 intensities) is higher than for the 500-nm-hole circuit (A1b and A2b intensities).

[0088] By triggering the detector to take into account only positive intensities in the area of 0.5 μm 1 μm deep (intrinsic region), a simple device can be made to detect UV-B (280 nm to 315 nm) and filter UV-A (315 nm to 400 nm).

[0089] An even more accurate filter can be made by optimizing via diameter and combination of different sizes of holes 106.

[0090] Fig. 14 shows a plan view of a device similar to the device 100 shown in Fig. 6 in which four different pore groups 106 with four different diameters and thus different wavelength selectivity are shown. Four different wavelengths can be detected with the four pores 106 of the different sizes shown in Fig. 14.

[0091] Fig. 15 shows a device 1500 according to another exemplary embodiment of the invention.

[0092] The device 1500 further comprises a light emitting diode (LED) 1502 emitting light 108. A part of the light 108 is transmitted towards a device 100 for detecting the wavelength composition of the light 108. A corresponding detection result may be transmitted from the device 100 to a signal processing circuit 114 which may generate a control signal for controlling the LED 1500 in a feedback architecture. The light emitting diode 1500 may be connected to the silicon substrate 102 using solder bumps 1504 or the like.

[0093] Fig. 16 shows a device according to another exemplary embodiment of the invention which differs from Fig. 15 in that the substrate 102 is substituted by a printed circuit board (PCB) 1602. In the embodiment of Fig. 16, the detector 100 is assembled on the PCB sub-mount 1602 via solder bumps 1504. Also the feedback loop circuitry 114 is connected to the PCB sub-mount 1602 using solder bumps 1504.

[0094] Fig. 17 shows a device 1700 according to another exemplary embodiment of the invention.

[0095] In this embodiment, the light emitting diode 1502 has a transparent substrate. Thus, the detector 100 can also be arranged under the light emitting diode 1502 as there may be also light emission below the light emitting diode 1502.

[0096] Fig. 18 schematically illustrates how different detectors 1802, 1804, 1806 may detect different wavelength ranges of an overall signal 1808. Reference numeral 1810 illustrates signal sampling from a first detector 1802 and a second detector 1804.

[0097] Fig. 19 shows a diagram 1900 having an abscissa 1902 along which a light energy is plotted in electron volts.

Along an ordinate 1904, a spectral distribution of a signal 108 is plotted. Sampling results in measuring the individual wavelength ranges 1906.

[0098] Fig. 20 shows a device according to another exemplary embodiment in which a thickness of the layer 712 differs for the two wavelength detectors 700, 702 shown in Fig. 20. For wavelength detector 700, layer 712 has a thickness b_1 which is smaller than a thickness b_2 for a second wavelength detector 702. Thus, the depth of the intrinsic zone 712 may be tuned by a recess 2002 of p⁺-layer 712. Such a recess 2002 of the p-region 712 can be manufactured by mask lithography and dry silicon etch.

[0099] Finally, it should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be capable of designing many alternative embodiments without departing from the scope of the invention as defined by the appended claims. In the claims, any reference signs placed in parentheses shall not be construed as limiting the claims. The word "comprising" and "comprises", and the like, does not exclude the presence of elements or steps other than those listed in any claim or the specification as a whole. The singular reference of an element does not exclude the plural reference of such elements and vice-versa. In a device claim enumerating several means, several of these means may be embodied by one and the same item of software or hardware. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage.

Claims

1. A device (100) for detecting electromagnetic radiation, the device (100) comprising
 - a substrate (102);
 - an electromagnetic radiation sensitive structure (104) arranged on and/or in the substrate (102);
 - a plurality of pores (106) formed on and/or in the substrate (102) in such a manner that electromagnetic radiation to be detected propagates through at least a part of the plurality of pores (106) before propagating into the electromagnetic radiation sensitive structure (104), wherein different ones of the plurality of pores (106) differ regarding at least one physical parameter so that each of the plurality of pores (106) is sensitive to an assigned wavelength range of electromagnetic radiation.
2. The device (100) according to claim 1, wherein the plurality of pores (106) are aligned parallel to one another.
3. The device (100) according to claim 1, wherein different ones of the plurality of pores (106) have a different diameter or surface area in a surface plane of the substrate (102).
4. The device (100) according to claim 1, wherein different ones of the plurality of pores (106) extend up to a different depth into the substrate (102).
5. The device (100) according to claim 1, wherein the plurality of pores (106) are grouped into pore groups, wherein pores (106) of each one of the pore groups have a common diameter or surface area in a surface plane of the substrate (102) and extend up to a different depth into the substrate (102), and wherein pores (106) of different ones of the pore groups have a different diameter or surface area in a surface plane of the substrate (102).
6. The device (100) according to claim 1, wherein the plurality of pores (106) are trenches extending perpendicular to a main surface of the substrate (102).
7. The device (100) according to claim 1, wherein the plurality of pores (106) are at least partially filled with a filling material (110) being transparent for the electromagnetic radiation, particularly being optically transparent.
8. The device (100) according to claim 1, wherein the electromagnetic radiation sensitive structure (104) comprises a photodiode structure, particularly a positive-intrinsic-negative photodiode structure.
9. The device (100) according to claim 1, wherein the electromagnetic radiation sensitive structure (104) comprises a stack of layers, wherein different ones of the layers differ from one another regarding a doping profile, wherein the plurality of pores (106) are formed to penetrate through at least a part of the layers.
10. The device (100) according to claim 9, wherein a thickness of at least a part of the layers differs in portions adjacent to different ones of the plurality of pores (106).

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11. The device (100) according to claim 1, comprising a patterned cover layer (112) arranged to expose the plurality of pores (106) and to cover surface portions between adjacent ones of the plurality of pores (106).
- 5 12. The device (100) according to claim 11, wherein the cover layer (112) comprises at least one of the group consisting of an electrically conductive material, and an opaque material.
13. The device (1300) according to claim 1, comprising an anti-reflective layer (1302) covering at least the plurality of pores (106).
- 10 14. The device (100) according to claim 1, comprising a signal processing circuit (114) formed on and/or in the substrate (102) and being adapted for processing detection signals generated by the electromagnetic radiation sensitive structure (104).
- 15 15. The device (1500) according to claim 14, comprising an electromagnetic radiation source (1502) adapted for generating electromagnetic radiation and being controlled by a control signal generated by the signal processing circuit (114) based on the detection signals.
16. The device (100) according to claim 1, monolithically integrated in and/or on the substrate (102).
- 20 17. The device (100) according to claim 1, wherein the substrate (102) is a semiconductor substrate, particularly one of the group consisting of a group IV semiconductor substrate, a silicon substrate, a germanium substrate, a group III-group V semiconductor substrate, and a GaAs substrate.
- 25 18. A method of detecting electromagnetic radiation, the method comprising directing electromagnetic radiation to be detected towards a plurality of pores (106) formed on and/or in a substrate (102) in such a manner that the electromagnetic radiation to be detected propagates through at least a part of the plurality of pores (106); subsequently propagating the electromagnetic radiation into an electromagnetic radiation sensitive structure (104) arranged on and/or in the substrate (102); wherein different ones of the plurality of pores (106) differ regarding at least one physical parameter so that each of the plurality of pores (106) is sensitive to an assigned wavelength range of the electromagnetic radiation.
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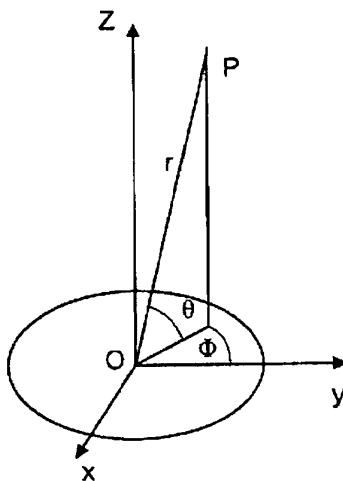


Fig. 1

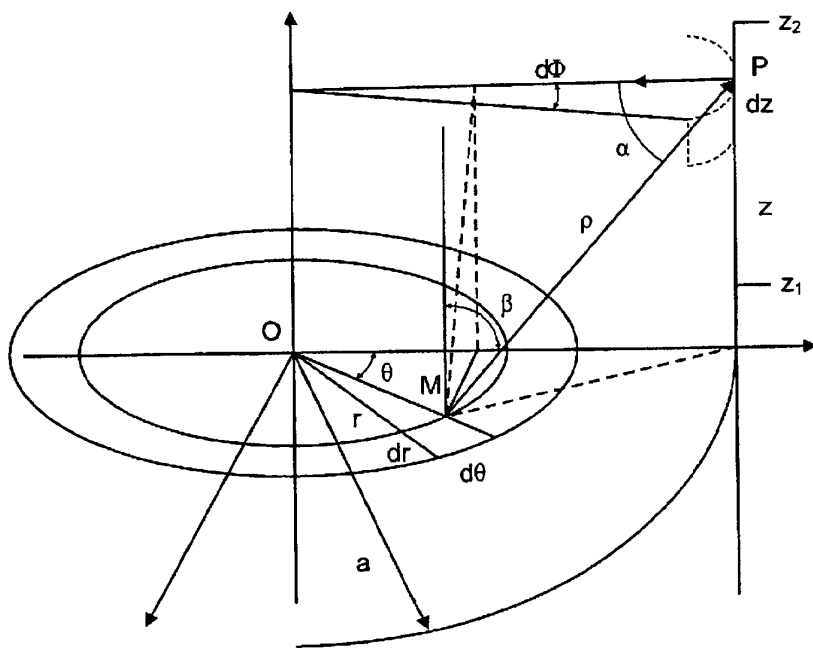
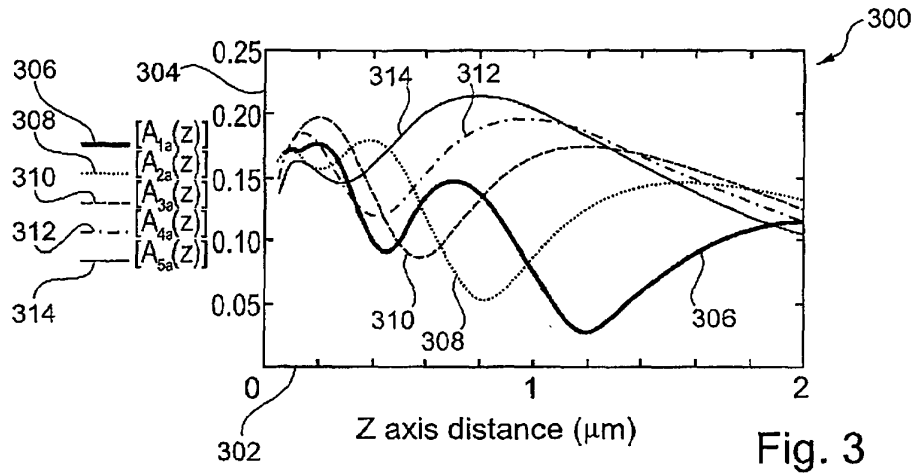
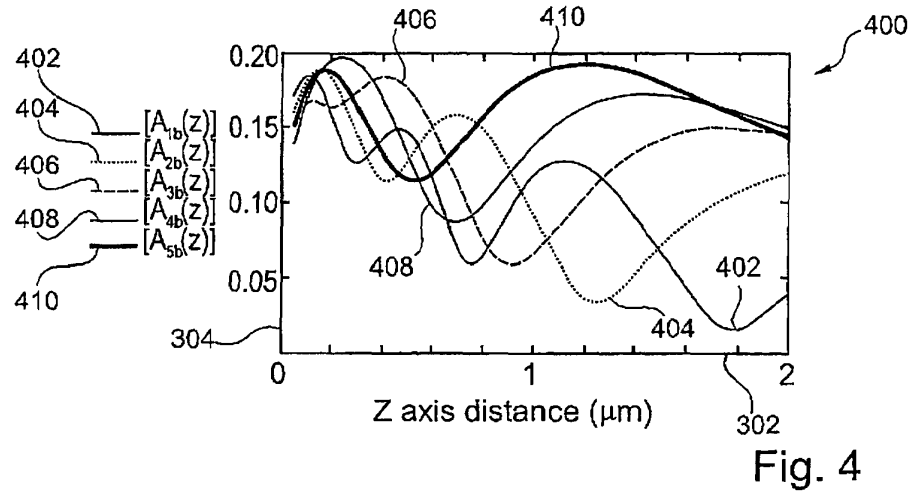
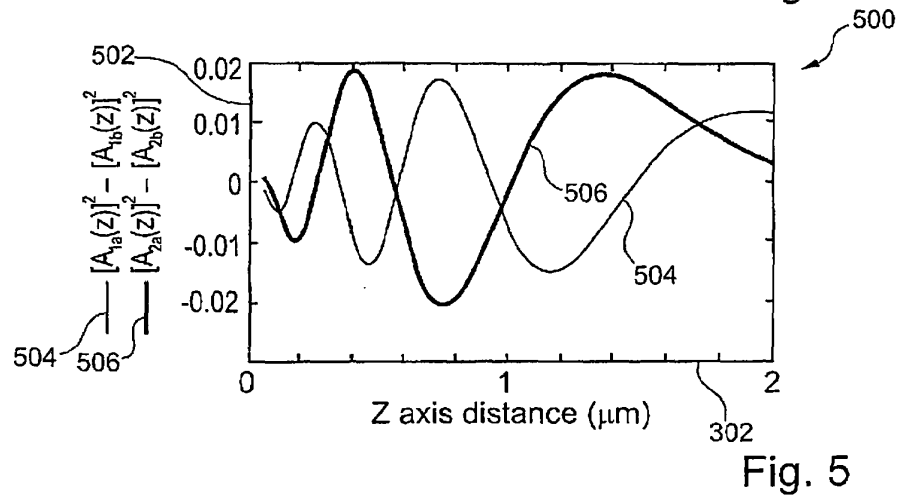
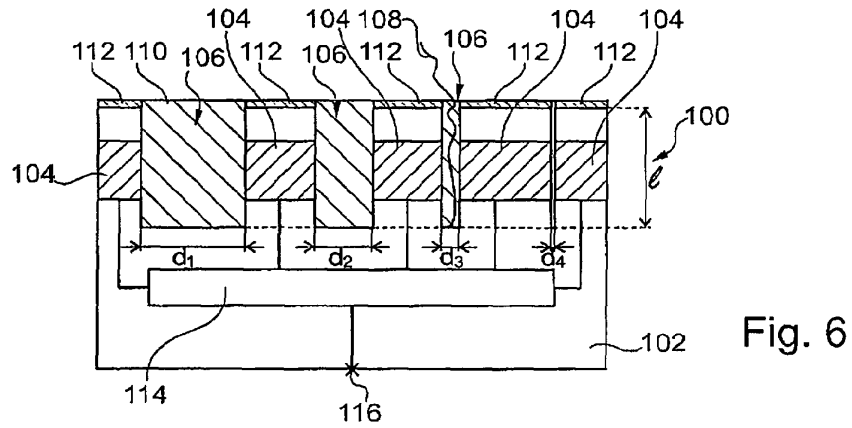
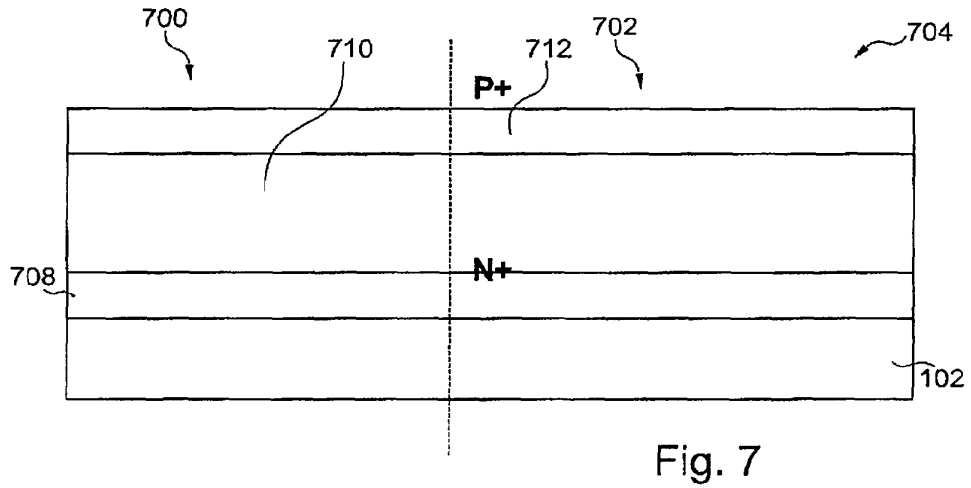
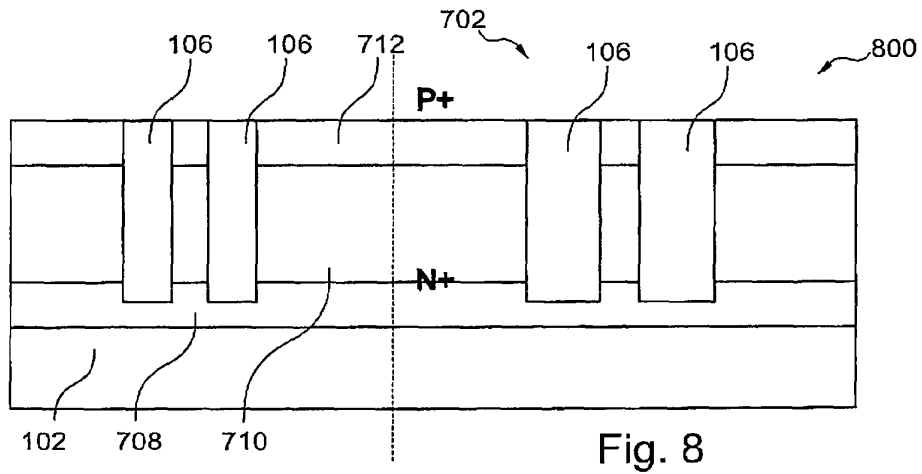
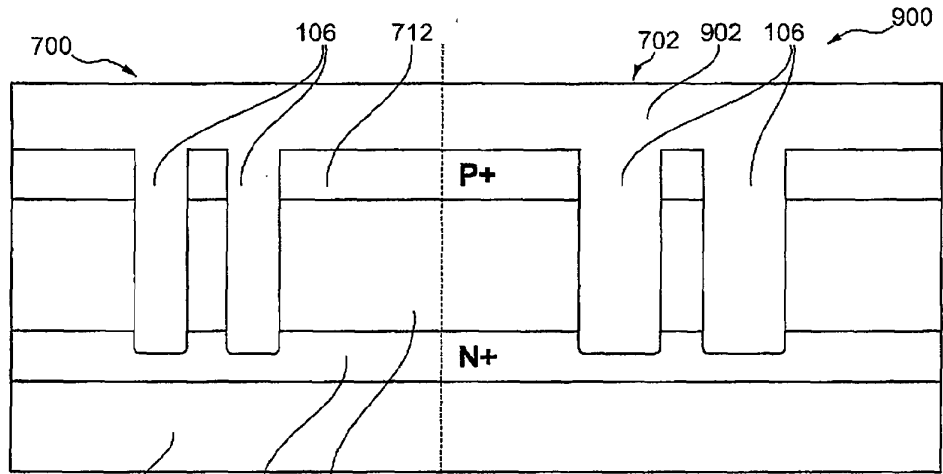
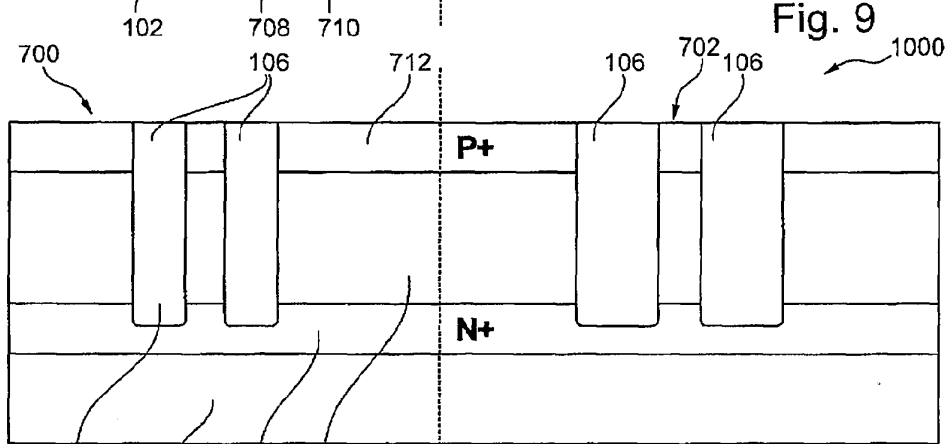
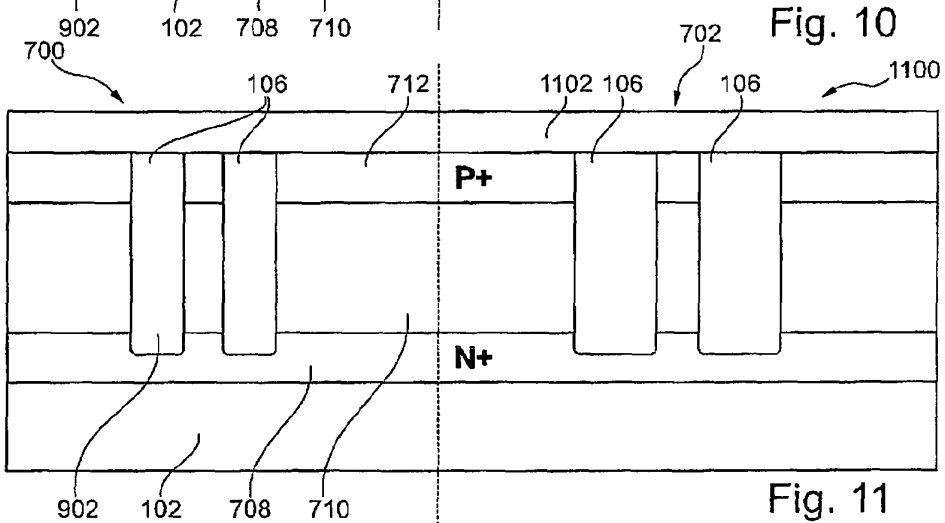


Fig. 2







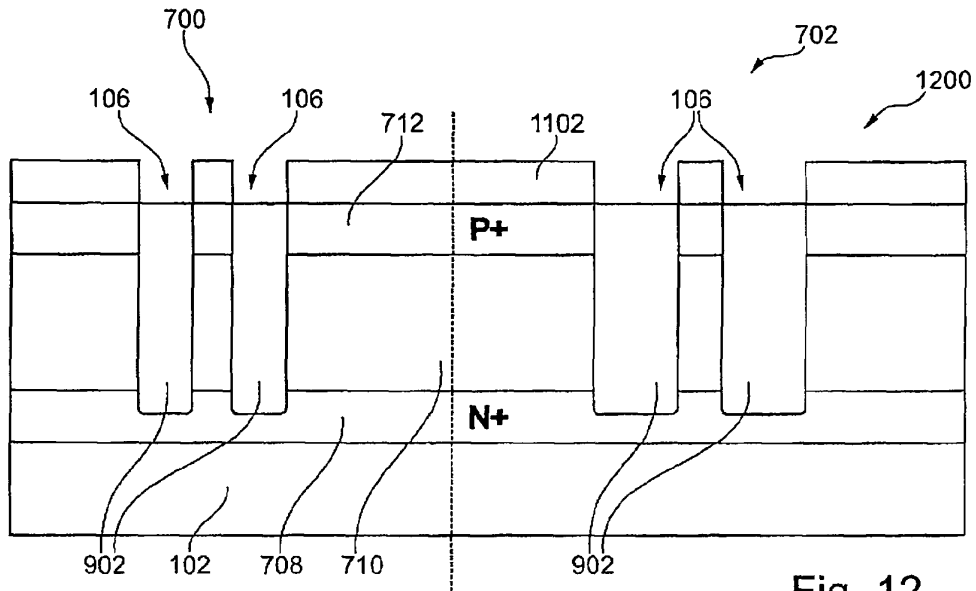


Fig. 12

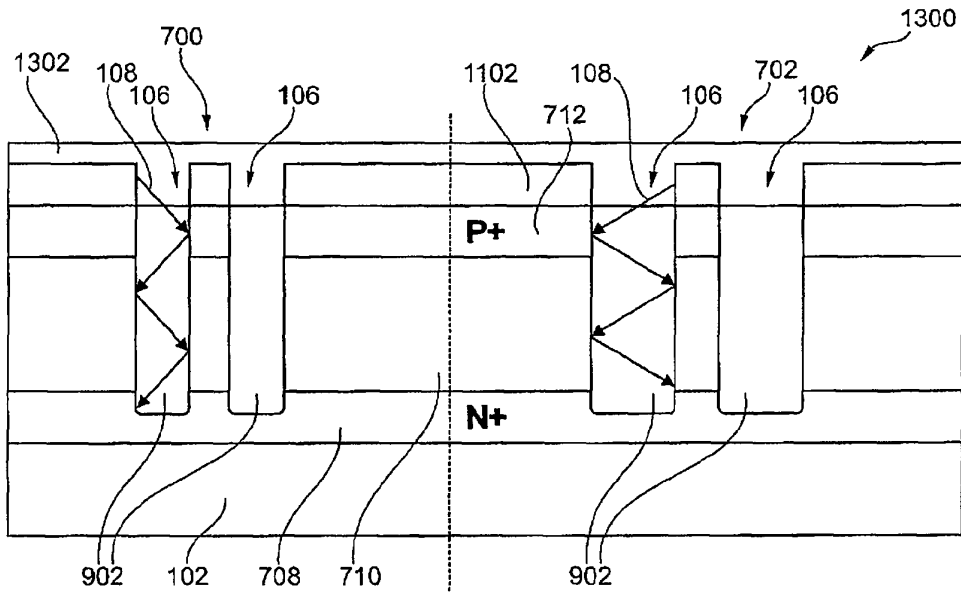


Fig. 13

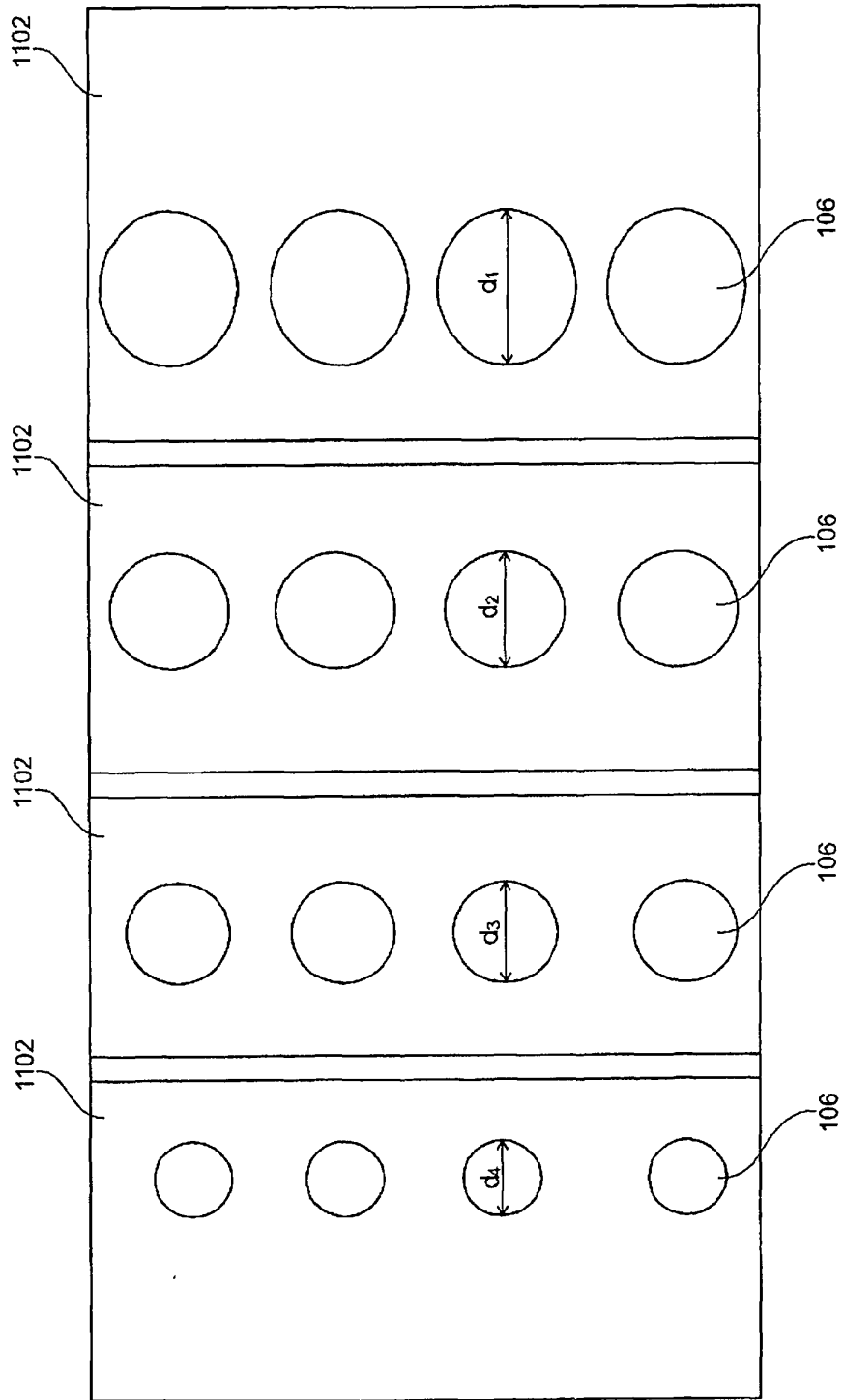


Fig. 14

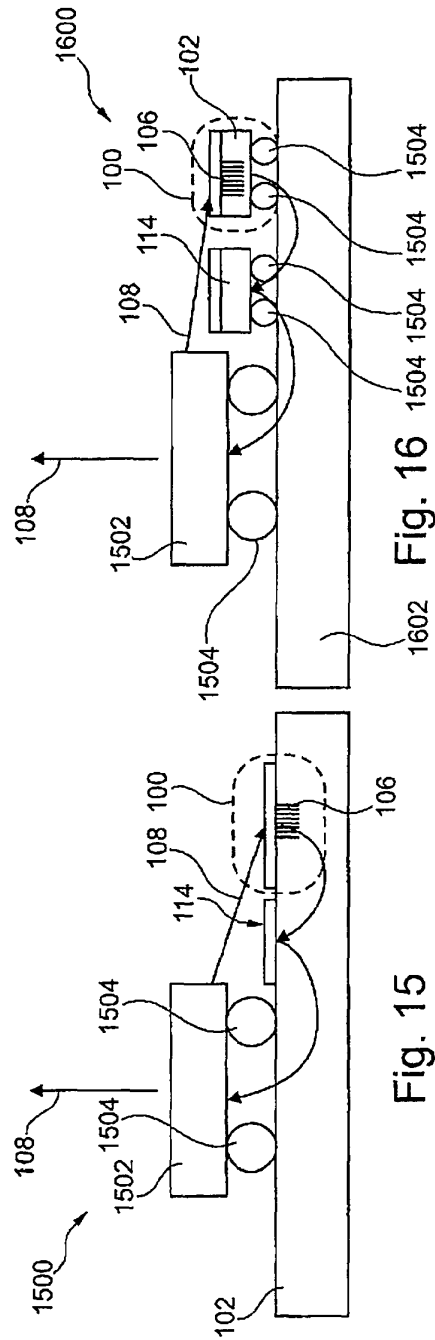


Fig. 15

Fig. 16

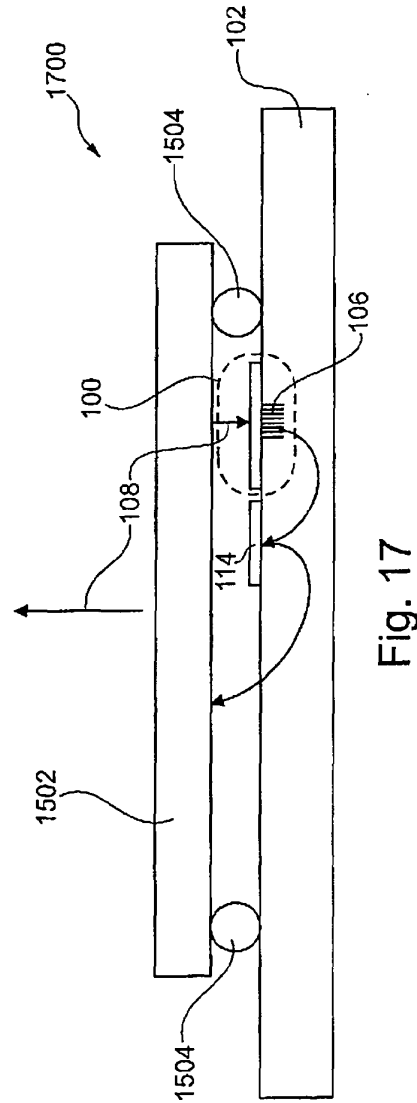
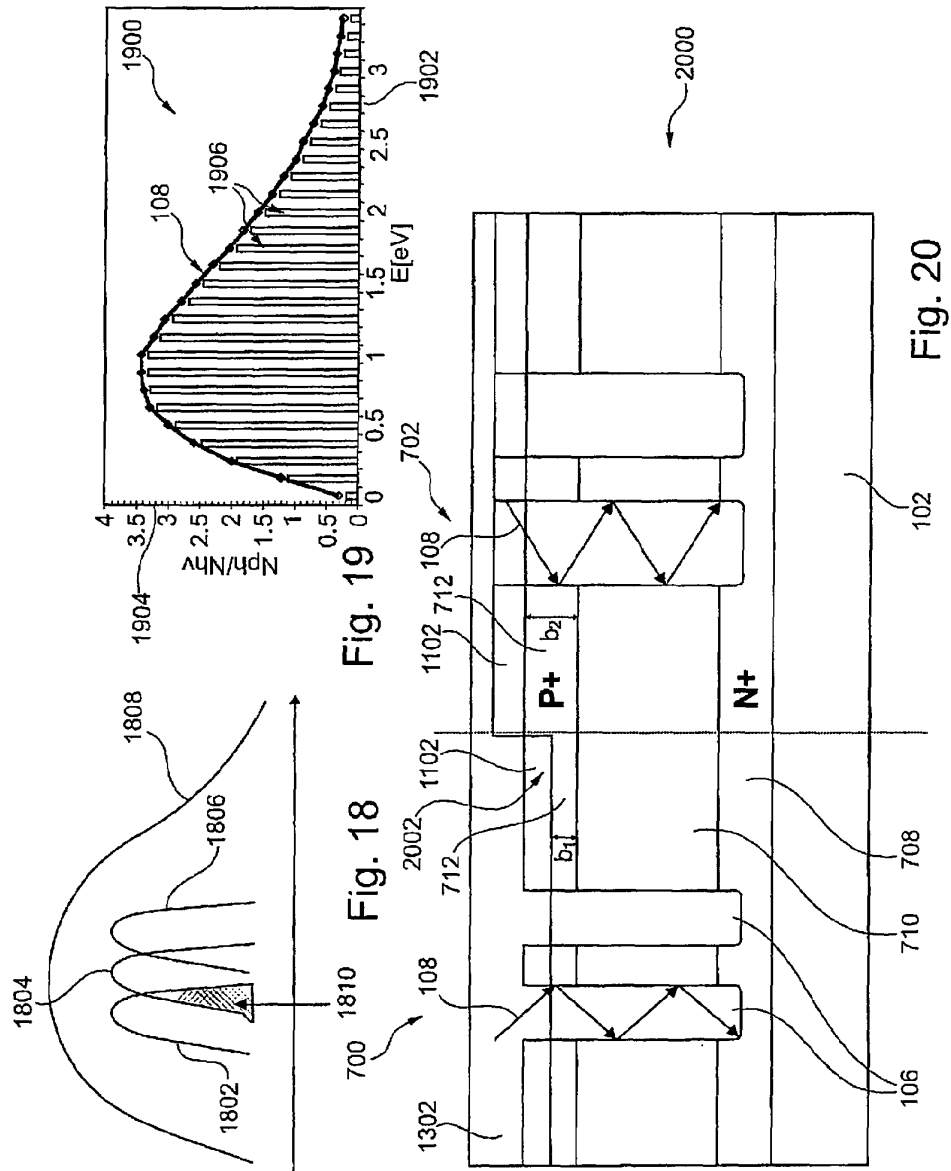


Fig. 17





EUROPEAN SEARCH REPORT

Application Number
EP 08 29 0924

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The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 16 June 2009	Examiner Heising, Stephan
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EPO FORM 1503 (03.02) (P4/C01)



EUROPEAN SEARCH REPORT

Application Number
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The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 16 June 2009	Examiner Heising, Stephan
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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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Attorney Docket No.: 309-0015USCIPDIV2
Confirmation No.: 4276

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<p>In re Application of: Shih-Yuan WANG et al.</p> <p>Application No.: 19/036,506</p>	<p>Examiner: Eduardo A. Rodela</p> <p>Art Unit: 2893</p>
<p>Filed: January 24, 2025</p> <p>Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES</p>	<p>CERTIFICATE OF TRANSMISSION</p> <p>I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</p> <p style="text-align: right;">/Mary Ellen Finnegan/ Name: Mary Ellen Finnegan</p> <p>Date: Sept. 16, 2025</p>

VIA EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

Applicant submits the accompanying Information Disclosure Statement for the Examiner's consideration.

This application is a division of Application No. 18/822,880 filed September 3, 2024, now U.S. Patent No. 12,243,948, which is a division of Application No. 18/385,213 filed October 30, 2023, now U.S. Patent No. 12,087,871, which is a continuation in-part of 17/974,325 filed October 26, 2022, now U.S. Patent No. 11,830,954 and also a continuation in-part of Application No. 18/113,474 filed February 23, 2023. Pursuant to 37 CFR 1.98(d)(1), Applicant respectfully directs the Examiner to the documents set forth in the Information Disclosure Statements submitted in these parent applications and the documents cited by the Examiners in these parent applications. Applicant respectfully requests that all items submitted

or cited in the parent applications be considered and acknowledged by the Examiner in this subject application. Applicant also respectfully requests that all documents submitted or cited in the parent applications be listed in any patent issuing from the subject application.

It is respectfully requested that the documents listed on the concurrently submitted Information Disclosure Statement form and the documents identified pursuant to 37 CFR 1.98(d)(1) above be considered and acknowledged by the Examiner in connection with the present application and be made of record therein.

Non-U.S. Patent Documents

In compliance with 37 CFR 1.98, copies of the non-U.S. patent documents referenced on the concurrently submitted Information Disclosure Statement are enclosed herewith. For any non-English language patent documents identified in the Information Disclosure Statement form, copies of the original patent documents along with an English language translation of the original patent documents or an English language translation of the Abstracts of the original patent documents are enclosed herewith.

Information Disclosure Statement Size Fee – Written Assertion Under 37 CFR 1.98

Submitted herewith is an Information Disclosure Statement Size Fee – Written Assertion Under 37 CFR 1.98. The cumulative number of documents submitted by the Applicant in the present application, including documents identified in the present Information Disclosure Statement, is 8. The cumulative number of documents submitted by the Applicant does not include the documents referred to the Examiner pursuant to 37 CFR 1.98(d)(1).

Commonly-owned Related Patents

Applicant brings to the attention of the Examiner the following commonly owned patents:

1. Application No. 16/528,958 filed August 1, 2019, now U.S. Patent No. 11,121,271;
2. Application No. 17/182,954 filed February 23, 2021, now U.S. Patent No. 11,791,432; and

3. Application No. 17/532,831 filed November 22, 2021, now U.S. Patent No. 11,309,444.

Commonly-owned Related Patents Involved in IPRs and PCGs

Applicant brings to the attention of the Examiner the following commonly owned patents currently involved in pending IPR proceedings:

1. Case IPR2025-00993 on patent 12,087,871;
2. Case IPR2025-00994 on patent 11,621,360;
3. Case IPR2025-00995 on patent 10,468,543;
4. Case IPR2025-00996 on patent 10,446,700; and
5. Case IPR-00997 on patent 9,525,084.

The following U.S. Patent is currently involved in a pending PGR proceeding:

1. Case PGR2025-00082 for patent 12,243,948

In the concurrently submitted Information Disclosure Statement, Applicant has identified seven (7) references on which the above five (5) IPRs rely to challenge patentability of the relevant patents under 35 U.S.C. §§102 or 103.

Commonly-owned Related Patents Involved in Litigation

Applicant also brings to the attention of the Examiner currently pending litigation W&WSENS DEVICES INC., v. SAMSUNG ELECTRONICS CO., LTD, and SAMSUNG ELECTRONICS AMERICA, INC., pending in United States District Court for the Eastern District of Texas, Marshall Division (W&Wsens v. Samsung) involving the following patents:

1. U.S. Patent No. 12,087,871;
2. U.S. Patent No. 11,621,360;
3. U.S. Patent No. 10,468,543;
4. U.S. Patent No. 10,446,700; and
5. U.S. Patent No. 9,525,084.

Applicant attaches hereto as Exhibit A (43 pages), Defendant's Invalidity Contentions in the W&WSens v. Samsung litigation. The Defendant's Invalidity Contentions include an exhaustive list of references that the Defendant apparently may be relied on to invalidate one or more claims of the above-identified patents without providing any basis supporting any contention.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125
any payment due and to credit any overpayment thereto.

Respectfully submitted,

/Gerard M. Wissing/

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EXHIBIT A

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

W&WSENS DEVICES INC.,

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD, and
SAMSUNG ELECTRONICS AMERICA, INC.,

Defendants.

Case No. 2:24-CV-00854-JRG

JURY TRIAL DEMANDED

DEFENDANTS' INVALIDITY CONTENTIONS

Pursuant to Local Patent Rules 3-3 and 3-4 and the Court's Docket Control Order (Dkt. 38), Defendants Samsung Electronics Co., Ltd. ("SEC") and Samsung Electronics America, Inc. ("SEA"), (collectively, "Samsung" or "Defendants") provide these Invalidity Contentions and accompanying document production to Plaintiff W&Wsens Devices Inc. ("W&W").

I. Overview

In this action, Plaintiff asserted in its P.R. 3-1 and 3-2 Disclosures of January 7, 2025 ("Infringement Contentions") that Defendants allegedly infringe claims 1-4, 6-8, 10-12, and 14-18 of U.S. Patent No. 12,087,871 (the "'871 patent"), claims 1, 3, 5, 6, 8, and 9 of U.S. Patent No. 11,621,360 (the "'360 patent"), claims 1, 3, 7, 9, 10, 16, 20, 24, 26, 28-30, and 32 of U.S. Patent No. 10,468,543 (the "'543 patent"), claims 1, 3, 7, 9, 10, 16, 20, 24, 26, 28-30, and 32 of U.S. Patent No. 10,446,700 (the "'700 patent"), and 1-3, 5, 7, 8, 11-15, 17-19, and 21 of U.S. Patent No. 9,525,084 (the "'084 patent") (collectively, the "Patents-in-Suit" and the "Asserted Claims").

This Court has not yet construed any of the terms in the Patents-in-Suit. Defendants' Invalidity Contentions are based on Defendants' present understanding of Plaintiff's apparent interpretation of the Asserted Claims, as advanced by Plaintiff in its Complaint and Infringement Contentions, and Defendants' own understanding of the scope of the Asserted Claims. Defendants take no position on any matter of claim construction or interpretation in these contentions. Defendants' contentions herein are not, and should in no way be seen as, admissions about or adoptions of any particular claim scope or construction, or any admission that any particular element is met in any particular way. Defendants object to any attempt to imply claim constructions from any identification or application of potential prior art. Any statement herein describing or tending to describe any claim element is provided solely for the purpose of understanding the relevant prior art. By including prior art that anticipates or renders obvious claims based on Plaintiff's apparent claim construction, Defendants do not thereby adopt Plaintiff's apparent claim construction.

Moreover, nothing herein should be construed as an admission that Defendants agree with Plaintiff's claim interpretations or that Plaintiff has a plausible basis to allege infringement. Similarly, nothing herein shall be construed as an admission regarding the application of the Asserted Claims to any of Defendants' accused products. Defendants do not agree with Plaintiff's application of the claims to the accused products, and Defendants deny infringement. Furthermore, these contentions do not represent an agreement with Plaintiff's views as to the meaning, definiteness, written description support for, or enablement of any of the Asserted Claims. In fact, Defendants provide grounds for invalidity under § 112 below. Pursuant to the Court's Docket Control Order (Dkt. 34), Defendants reserve the right to include arguments directed to indefiniteness in their *Markman* briefing. Nothing stated herein shall be construed as a waiver of

A. Prior Art Patents, Patent Applications, and Publications

Table 1: Prior Art Patents and Patent Applications

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	4,981,525	February 9, 1989	January 1, 1991	Kiyama et al.	SAM-W & W_ 00032972- SAM-W & W_ 00032994
US	5,055,900	October 11, 1989	October 8, 1991	Fossum et al.	SAM-W & W_ 00032995- SAM-W & W_ 00033011
US	5,061,977	January 8, 1991	October 29, 1991	Funaba	SAM-W & W_ 00036105- SAM-W & W_ 00036117
US	5,410,175	June 18, 1992	April 25, 1995	Kyomasu et al.	SAM-W & W_ 00033012- SAM-W & W_ 00033042
US	5,448,099	March 1, 1994	September 5, 1995	Yano	SAM-W & W_ 00036118- SAM-W & W_ 00036142
US	6,222,951	April 3, 2000	April 24, 2001	Huang	SAM-W & W_ 00036143- SAM-W & W_ 00036153
US	6,485,998	June 11, 1999	November 26, 2002	Frahm et al.	SAM-W & W_ 00036154- SAM-W & W_ 00036158
US	6,593,635	July 3, 2002	July 15, 2003	Yanagisawa et al.	SAM-W & W_ 00033043- SAM-W & W_ 00033058
US	6,667,528	January 3, 2002	December 23, 2003	Cohen et al.	SAM-W & W_ 00033059- SAM-W & W_ 00033082
US	6,680,495	August 1, 2001	January 20, 2004	Fitzergald	SAM-W & W_ 00036159- SAM-W & W_ 00036175
US	6,800,914	August 19, 2002	October 5, 2004	Ito et al.	SAM-W & W_ 00033083- SAM-W & W_ 00033102
US	6,858,912	August 8, 2001	February 22, 2005	Marshall et al.	SAM-W & W_ 00036176- SAM-W & W_ 00036197

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	6,914,008	May 6, 2004	July 5, 2005	Den et al.	SAM-W&W_00036198- SAM-W&W_00036219
US	6,919,609	April 1, 2004	July 19, 2005	Lindemann et al.	SAM-W&W_00036220- SAM-W&W_00036253
US	7,049,640	June 30, 2004	May 23, 2006	Boisvert et al.	SAM-W&W_00036254- SAM-W&W_00036260
US	7,083,998	July 1, 2004	August 1, 2006	Chu et al.	SAM-W&W_00037903- SAM-W&W_00037924
US	7,109,517	November 15, 2002	September 19, 2006	Zaidi	SAM-W&W_00033103- SAM-W&W_00033141
US	7,153,720	June 1, 2005	December 26, 2006	Augusto	SAM-W&W_00037925- SAM-W&W_00037961
US	7,453,129	October 13, 2004	November 18, 2008	King et al.	SAM-W&W_00037962- SAM-W&W_00037977
US	7,456,452	December 15, 2005	November 25, 2008	Wells et al.	SAM-W&W_00035725- SAM-W&W_00035743
US	7,498,574	July 8, 2005	March 3, 2009	Puscasu et al.	SAM-W&W_00037978- SAM-W&W_00038011
US	7,518,172	January 30, 2007	April 14, 2009	Moon et al.	SAM-W&W_00038012- SAM-W&W_00038041
US	7,521,737	March 2, 2005	April 21, 2009	Augusto	SAM-W&W_00033142- SAM-W&W_00033178
US	7,525,170	October 4, 2006	April 28, 2009	Hsu et al.	SAM-W&W_00033179- SAM-W&W_00033195
US	7,576,404	December 13, 2006	August 18, 2009	Wilson et al.	SAM-W&W_00038042- SAM-W&W_00038050
US	7,595,213	September 7, 2006	September 29, 2009	Kwon et al.	SAM-W&W_00038051- SAM-W&W_00038065

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	7,608,824	September 20, 2007	October 27, 2009	Korsah et al.	SAM-W&W_00038066- SAM-W&W_00038077
US	7,646,943	September 4, 2008	January 12, 2010	Wober	SAM-W&W_00040084- SAM-W&W_00040105
US	7,659,627	December 5, 2007	February 9, 2010	Miyachi et al.	SAM-W&W_00033196- SAM-W&W_00033212
US	7,701,629	April 19, 2007	April 20, 2010	Wang et al.	SAM-W&W_00033213- SAM-W&W_00033236
US	7,714,368	June 26, 2006	May 11, 2010	Yang et al.	SAM-W&W_00040034- SAM-W&W_00040054
US	7,759,703	June 20, 2008	July 20, 2010	Nam et al.	SAM-W&W_00038078- SAM-W&W_00038092
US	7,795,686	September 16, 2008	September 14, 2010	Shioya et al.	SAM-W&W_00038093- SAM-W&W_00038104
US	7,800,193	March 8, 2007	September 21, 2010	Fujikata et al.	SAM-W&W_00033237- SAM-W&W_00033265
US	7,847,362	July 2, 2008	December 7, 2010	Ogino et al.	SAM-W&W_00038105- SAM-W&W_00038145
US	7,880,255	July 19, 2004	February 1, 2011	Baggenstoss	SAM-W&W_00035761- SAM-W&W_00035781
US	7,910,965	June 13, 2008	March 22, 2011	Lee et al.	SAM-W&W_00038146- SAM-W&W_00038161
US	7,920,781	June 18, 2008	April 5, 2011	Onuki	SAM-W&W_00033266- SAM-W&W_00033308
US	7,964,925	January 17, 2007	June 21, 2011	Fattal et al.	SAM-W&W_00038162- SAM-W&W_00038176
US	7,972,885	September 24, 2009	July 5, 2011	Dutta et al.	SAM-W&W_00033309- SAM-W&W_00033336

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	7,977,637	August 20, 2009	July 12, 2011	Yap et al.	SAM-W&W_00033337- SAM-W&W_00033360
US	8,003,883	January 11, 2007	August 23, 2011	Korevaar et al.	SAM-W&W_00033361- SAM-W&W_00033381
US	8,022,390	August 17, 2007	September 20, 2011	Kim et al.	SAM-W&W_00033382- SAM-W&W_00033399
US	8,035,184	September 25, 2009	October 11, 2011	Dutta et al.	SAM-W&W_00038177- SAM-W&W_00038204
US	8,039,800	April 19, 2010	October 18, 2011	Soma et al.	SAM-W&W_00038205- SAM-W&W_00038218
US	8,049,203	June 15, 2007	November 1, 2011	Samuelson et al.	SAM-W&W_00033400- SAM-W&W_00033433
US	8,063,424	November 16, 2009	November 22, 2011	Gebara et al.	SAM-W&W_00033434- SAM-W&W_00033443
US	8,093,488	August 28, 2008	January 10, 2012	Richter et al.	SAM-W&W_00038219- SAM-W&W_00038225
US	8,106,289	December 31, 2007	January 31, 2012	Dutta	SAM-W&W_00038226- SAM-W&W_00038247
US	8,119,434	August 14, 2009	February 21, 2012	Cohen	SAM-W&W_00038248- SAM-W&W_00038259
US	8,120,079	March 13, 2009	February 21, 2012	Augusto	SAM-W&W_00038260- SAM-W&W_00038288
US	8,129,710	October 31, 2008	March 6, 2012	Cho et al.	SAM-W&W_00038289- SAM-W&W_00028303
US	8,138,013	February 14, 2011	March 20, 2012	Fattal et al.	SAM-W&W_00038304- SAM-W&W_00038315
US	8,143,687	December 17, 2009	March 27, 2012	Wehner et al.	SAM-W&W_00038316- SAM-W&W_00038325

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	8,174,059	April 7, 2009	May 8, 2012	Dutta	SAM-W&W_00038326- SAM-W&W_00038372
US	8,183,612	July 7, 2009	May 22, 2012	Chong et al.	SAM-W&W_00038373- SAM-W&W_00038380
US	8,224,134	April 3, 2009	July 17, 2012	Baeyens et al.	SAM-W&W_00038381- SAM-W&W_00038393
US	8,232,617	June 4, 2009	July 31, 2012	Ma et al.	SAM-W&W_00033444- SAM-W&W_00033463
US	8,237,175	September 23, 2011	August 7, 2012	Moustakas et al.	SAM-W&W_00038394- SAM-W&W_00038467
US	8,253,211	September 24, 2009	August 28, 2012	Cheng et al.	SAM-W&W_00038468- SAM-W&W_00038501
US	8,257,997	October 17, 2008	September 4, 2012	Chen et al.	SAM-W&W_00038502- SAM-W&W_00038540
US	8,258,557	April 10, 2007	September 4, 2012	Gaebler et al.	SAM-W&W_00033464- SAM-W&W_00033504
US	8,269,303	March 9, 2009	September 18, 2012	Fujikata et al.	SAM-W&W_00038541- SAM-W&W_00038570
US	8,279,519	September 15, 2010	October 2, 2012	Takahashi et al.	SAM-W&W_00038571- SAM-W&W_00038619
US	8,304,759	June 22, 2010	November 6, 2012	Dutta	SAM-W&W_00038620- SAM-W&W_00038631
US	8,314,400	January 27, 2011	November 20, 2012	Nikolic et al.	SAM-W&W_00033505- SAM-W&W_00033533
US	8,330,090	April 29, 2008	December 11, 2012	Agarwal	SAM-W&W_00038632- SAM-W&W_00038646
US	8,338,857	August 28, 2010	December 25, 2012	Morse et al.	SAM-W&W_00038647- SAM-W&W_00038657

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	8,357,960	September 17, 2009	January 22, 2013	Dutta	SAM-W&W_0003534- SAM-W&W_0003565
US	8,384,007	October 7, 2009	February 26, 2013	Yu et al.	SAM-W&W_0003566- SAM-W&W_0003597
US	8,415,713	February 17, 2009	April 9, 2013	Ogura	SAM-W&W_00038658- SAM-W&W_00038681
US	8,431,817	June 8, 2010	April 30, 2013	Kim et al.	SAM-W&W_00038682- SAM-W&W_00038746
US	8,436,370	December 22, 2009	May 7, 2013	Park et al.	SAM-W&W_00033598- SAM-W&W_00033623
US	8,472,802	March 10, 2008	June 25, 2013	Ahn et al.	SAM-W&W_00038747- SAM-W&W_00038771
US	8,476,637	June 8, 2010	July 2, 2013	Kim et al.	SAM-W&W_00038772- SAM-W&W_00038836
US	8,487,396	August 11, 2011	July 16, 2013	Mazzillo	SAM-W&W_00033624- SAM-W&W_00033645
US	8,507,840	December 21, 2010	August 13, 2013	Yu et al.	SAM-W&W_00033646- SAM-W&W_00033676
US	8,515,216	November 3, 2009	August 20, 2013	Abad et al.	SAM-W&W_00038837- SAM-W&W_00038858
US	8,603,849	August 28, 2009	December 10, 2013	Kim et al.	SAM-W&W_00038859- SAM-W&W_00038875
US	8,637,951	January 9, 2009	January 28, 2014	Okamoto et al.	SAM-W&W_00038876- SAM-W&W_00038897
US	8,659,037	June 8, 2010	February 25, 2014	Kim et al.	SAM-W&W_00038898- SAM-W&W_00038961
US	8,664,739	May 26, 2011	March 4, 2014	King et al.	SAM-W&W_00038962- SAM-W&W_00038977

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	8,670,471	February 23, 2010	March 11, 2014	Kim et al.	SAM-W&W_00033677- SAM-W&W_00033700
US	8,692,301	September 4, 2009	April 8, 2014	Samuelson et al.	SAM-W&W_00038978- SAM-W&W_00038989
US	8,772,623	October 30, 2012	July 8, 2014	Wanlass et al.	SAM-W&W_00038990- SAM-W&W_00039022
US	8,829,410	August 21, 2013	September 9, 2014	Kuboi	SAM-W&W_00033701- SAM-W&W_00033732
US	8,829,566	March 15, 2007	September 9, 2014	Morse et al.	SAM-W&W_00033733- SAM-W&W_00033743
US	8,835,905	March 15, 2011	September 16, 2014	Wober et al.	SAM-W&W_00039023- SAM-W&W_00039061
US	8,861,909	February 16, 2012	October 14, 2014	Lipson et al.	SAM-W&W_00033744- SAM-W&W_00033762
US	8,941,005	July 26, 2010	January 27, 2015	Ohmi	SAM-W&W_00039062- SAM-W&W_00039071
US	8,941,203	September 12, 2012	January 27, 2015	Wehner et al.	SAM-W&W_00039072- SAM-W&W_00039091
US	8,967,859	April 20, 2010	March 3, 2015	Harmon et al.	SAM-W&W_00039092- SAM-W&W_00039136
US	8,994,136	September 4, 2013	March 31, 2015	Park et al.	SAM-W&W_00039137- SAM-W&W_00039153
US	9,025,074	January 2, 2014	May 5, 2015	Kishi	SAM-W&W_00033763- SAM-W&W_00033785
US	9,059,055	February 5, 2013	June 16, 2015	Konno et al.	SAM-W&W_00039154- SAM-W&W_00039177
US	9,105,789	March 24, 2011	August 11, 2015	Mazzillo et al.	SAM-W&W_00039178- SAM-W&W_00039202

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	9,153,610	January 14, 2013	October 6, 2015	Kobayashi et al.	SAM-W&W_00033786- SAM-W&W_00033813
US	9,209,345	November 19, 2013	December 8, 2015	Haddad et al.	SAM-W&W_00033814- SAM-W&W_00033826
US	9,231,014	October 21, 2014	January 5, 2016	Frey et al.	SAM-W&W_00039203- SAM-W&W_00039211
US	9,231,019	December 6, 2013	January 5, 2016	Shimotsusa	SAM-W&W_00039212- SAM-W&W_00039227
US	9,236,548	March 18, 2013	January 12, 2016	Yan et al.	SAM-W&W_00039228- SAM-W&W_00039256
US	9,257,583	May 25, 2011	February 9, 2016	Watanabe et al.	SAM-W&W_00033827- SAM-W&W_00033847
US	9,288,380	June 23, 2014	March 15, 2016	Nomura	SAM-W&W_00039257- SAM-W&W_00039279
US	9,312,422	November 29, 2011	April 12, 2016	Miura et al.	SAM-W&W_00039280- SAM-W&W_00039297
US	9,324,891	December 22, 2010	April 26, 2016	Shigeta et al.	SAM-W&W_00039298- SAM-W&W_00039345
US	9,395,489	October 8, 2014	July 19, 2016	Cheng et al.	SAM-W&W_00039346- SAM-W&W_00039369
US	9,496,428	June 22, 2010	November 15, 2016	Nishi et al.	SAM-W&W_00039370- SAM-W&W_00039388
US	9,568,606	March 13, 2013	February 14, 2017	Ikemoto	SAM-W&W_00033848- SAM-W&W_00033874
US	9,595,628	August 11, 2014	March 14, 2017	Okandan et al.	SAM-W&W_00033875- SAM-W&W_00033891
US	9,680,046	December 31, 2013	June 13, 2017	Dutta et al.	SAM-W&W_00039389- SAM-W&W_00039409

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	9,698,295	March 16, 2016	July 4, 2017	Pagani	SAM-W&W_00033892- SAM-W&W_00033910
US	9,748,306	November 15, 2013	August 29, 2017	Morgan	SAM-W&W_00039410- SAM-W&W_00039425
US	9,761,746	March 11, 2013	September 12, 2017	Kang et al.	SAM-W&W_00039426- SAM-W&W_00039442
US	9,794,457	June 20, 2014	October 17, 2017	Masuda et al.	SAM-W&W_00039443- SAM-W&W_00039483
US	9,813,152	September 30, 2008	November 7, 2017	Pinguet et al.	SAM-W&W_00033911- SAM-W&W_00033931
US	10,134,926	June 30, 2015	November 20, 2018	Akkaya et al.	SAM-W&W_00035545- SAM-W&W_00035563
US	10,866,343	April 15, 2014	December 15, 2020	Noda et al.	SAM-W&W_00035782- SAM-W&W_00035803
US	2004/0021062	November 15, 2002	February 5, 2004	Zaidi	SAM-W&W_00031766- SAM-W&W_00031806
US	2004/0201042	May 6, 2004	October 14, 2004	Den et al.	SAM-W&W_00031807- SAM-W&W_00031826
US	2005/0106767	September 27, 2004	May 19, 2005	Takahashi et al.	SAM-W&W_00031827- SAM-W&W_00031838
US	2005/0109388	October 25, 2004	May 26, 2005	Murakami et al.	SAM-W&W_00031839- SAM-W&W_00031863
US	2006/0008933	August 14, 2003	January 12, 2006	Muller et al.	SAM-W&W_00031864- SAM-W&W_00031871
US	2006/0076589	March 14, 2005	April 13, 2006	Gao et al.	SAM-W&W_00031872- SAM-W&W_00031888
US	2006/0207647	March 16, 2005	September 21, 2006	Tsakalakos et al.	SAM-W&W_00035804- SAM-W&W_00035839

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	2006/0261430	March 28, 2006	November 23, 2006	Holz	SAM-W & W_ 00031889- SAM-W & W_ 00031905
US	2006/0273358	May 31, 2006	December 7, 2006	Hasegawa	SAM-W & W_ 00031906- SAM-W & W_ 00031916
US	2007/0152289	December 30, 2005	July 5, 2007	Morse et al.	SAM-W & W_ 00035840- SAM-W & W_ 00035846
US	2007/0170476	January 20, 2006	July 26, 2007	Giziewicz et al.	SAM-W & W_ 00031917- SAM-W & W_ 00031931
US	2008/0048283	August 21, 2007	February 28, 2008	Han	SAM-W & W_ 00035847- SAM-W & W_ 00035852
US	2008/0246106	April 3, 2007	October 9, 2008	Beausoleil et al.	SAM-W & W_ 00031932- SAM-W & W_ 00031960
US	2008/0259981	April 19, 2007	October 23, 2008	Wang et al.	SAM-W & W_ 00031961- SAM-W & W_ 00031983
US	2008/0295882	May 27, 2008	December 4, 2008	Stephens et al.	SAM-W & W_ 00031984- SAM-W & W_ 00032034
US	2009/0121306	December 21, 2005	May 14, 2009	Ishikawa	SAM-W & W_ 00032036- SAM-W & W_ 00032055
US	2009/0159123	December 15, 2008	June 25, 2009	Kothari et al.	SAM-W & W_ 00035853- SAM-W & W_ 00035921
US	2009/0194160	February 3, 2009	August 6, 2009	Chin et al.	SAM-W & W_ 00035922- SAM-W & W_ 00035955
US	2010/0032786	August 5, 2009	February 11, 2010	Jung	SAM-W & W_ 00040073- SAM-W & W_ 00040083
US	2010/0089443	September 24, 2009	April 15, 2010	Bloomstein et al.	SAM-W & W_ 00032056- SAM-W & W_ 00032100
US	2010/0117108	April 10, 2007	May 13, 2010	Gaebler et al.	SAM-W & W_ 00032101- SAM-W & W_ 00032144

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	2010/0127153	April 28, 2008	May 27, 2010	Agarwal	SAM-W&W_00032145- SAM-W&W_00032158
US	2010/0148221	December 8, 2009	June 17, 2010	Yu et al.	SAM-W&W_00035956- SAM-W&W_00036004
US	2010/0289103	December 13, 2006	November 18, 2010	Yamamoto et al.	SAM-W&W_00032159- SAM-W&W_00032175
US	2010/0307557	May 27, 2010	December 9, 2010	Yamazaki et al.	SAM-W&W_00032176- SAM-W&W_00032233
US	2010/0308428	January 9, 2009	December 9, 2010	Okamoto et al.	SAM-W&W_00032234- SAM-W&W_00032255
US	2011/0126891	November 29, 2010	June 2, 2011	Goto et al.	SAM-W&W_00036005- SAM-W&W_00036046
US	2011/0147877	December 17, 2009	June 23, 2011	Wehner et al.	SAM-W&W_00032256- SAM-W&W_00032265
US	2011/0226937	November 12, 2010	September 22, 2011	Yu et al.	SAM-W&W_00032266- SAM-W&W_00032320
US	2011/0227138	September 17, 2010	September 22, 2011	Haddad et al.	SAM-W&W_00032321- SAM-W&W_00032346
US	2011/0240099	March 30, 2010	October 6, 2011	Ellinger et al.	SAM-W&W_00032347- SAM-W&W_00032370
US	2011/0253208	November 27, 2009	October 20, 2011	Ohmi	SAM-W&W_00036047 - SAM-W&W_00036060
US	2011/0315988	May 12, 2011	December 29, 2011	Yu et al.	SAM-W&W_00032371- SAM-W&W_00032464
US	2012/0012741	July 12, 2011	January 19, 2012	Vasylyev	SAM-W&W_00032465- SAM-W&W_00032485
US	2012/0033119	August 2, 2011	February 9, 2012	Shinohara	SAM-W&W_00032486- SAM-W&W_00032509

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	2012/0049044	August 19, 2011	March 1, 2012	Kuboi	SAM-W&W_00032510- SAM-W&W_00032542
US	2012/0111396	May 4, 2011	May 10, 2012	Saylor et al.	SAM-W&W_00036061- SAM-W&W_00036081
US	2012/0146172	June 20, 2011	June 14, 2012	Carey et al.	SAM-W&W_00032543- SAM-W&W_00032562
US	2012/0153124	December 21, 2010	June 21, 2012	Yu et al.	SAM-W&W_00032563- SAM-W&W_00032590
US	2012/0154919	December 14, 2010	June 21, 2012	Hu et al.	SAM-W&W_00040013- SAM-W&W_00040033
US	2012/0186638	July 22, 2011	July 26, 2012	Ohmi	SAM-W&W_00032591- SAM-W&W_00032604
US	2012/0213468	February 16, 2012	August 23, 2012	Lipson et al.	SAM-W&W_00032605- SAM-W&W_00032625
US	2012/0273911	December 17, 2010	November 1, 2012	Shigeta et al.	SAM-W&W_00032626- SAM-W&W_00032657
US	2012/0313201	May 8, 2012	December 13, 2012	Hebert et al.	SAM-W&W_00032658- SAM-W&W_00032685
US	2013/0014814	January 10, 2011	January 17, 2013	Han et al.	SAM-W&W_00036082- SAM-W&W_00036104
US	2013/0082343	September 12, 2012	April 4, 2013	Fudaba, et al.	SAM-W&W_00032686- SAM-W&W_00032695
US	2013/0094865	September 30, 2008	April 18, 2013	Pinguet et al.	SAM-W&W_00032696- SAM-W&W_00032715
US	2013/0105927	December 22, 2010	May 2, 2013	Shigeta et al.	SAM-W&W_00032716- SAM-W&W_00032743
US	2013/0182163	January 14, 2013	July 18, 2013	Kobayashi et al.	SAM-W&W_00032744- SAM-W&W_00032770

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
US	2013/0320479	March 15, 2013	December 5, 2013	Ahn et al.	SAM-W&W_00037842- SAM-W&W_00037859
US	2013/0342722	August 21, 2013	December 26, 2013	Kuboi	SAM-W&W_00032771- SAM-W&W_00032803
US	2014/0175372	December 21, 2012	June 26, 2014	Aberg et al.	SAM-W&W_00032804- SAM-W&W_00032822
US	2015/0053923	August 21, 2014	February 26, 2015	Frey et al.	SAM-W&W_00032823- SAM-W&W_00032830
US	2015/0312461	April 27, 2015	October 29, 2015	Kim et al.	SAM-W&W_00037860- SAM-W&W_00037902
US	2016/0015987	February 27, 2014	January 21, 2016	Perraud et al.	SAM-W&W_00032831- SAM-W&W_00032848
US	2016/0126381	May 22, 2014	May 5, 2016	Wang et al.	SAM-W&W_00032849- SAM-W&W_00032925
US	2018/0182806	October 30, 2017	June 28, 2018	Jin et al.	SAM-W&W_00035679- SAM-W&W_00035724
CN	103400872A	June 30, 2013	November 20, 2013	Guo et al.	SAM-W&W_00024560- SAM-W&W_00024600; SAM-W&W_00039902- SAM-W&W_00039940
CN	103400872B	June 30, 2013	August 26, 2015	Guo et al.	SAM-W&W_00040055- SAM-W&W_00040072
CN	103050498	December 28, 2012	April 17, 2013	Jian et al.	SAM-W&W_00034690- SAM-W&W_00034702; SAM-W&W_00037122- SAM-W&W_00037134
DE	102009009814 AI	February 20, 2009	August 26, 2010	Leipold et al.	SAM-W&W_00025325- SAM-W&W_00025388

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
DE	102012216433 A1	September 14, 2012	March 20, 2014	Kautzsch	SAM-W&W_00025389- SAM-W&W_00025466
EP	0064918B1	April 29, 1982	November 13, 1985	Rebondy et al.	SAM-W&W_00025485- SAM-W&W_00025491
EP	0696747A2	August 8, 1995	February 14, 1996	Tatsuya et al.	SAM-W&W_00025492- SAM-W&W_00025538
EP	2172974A1	October 1, 2008	April 7, 2010	NXP B.V.	SAM-W&W_00025539- SAM-W&W_00025561
JP	S59-16385	July 19, 1982	January 27, 1984	Sakura et al.	SAM-W&W_00035333- SAM-W&W_00035335
JP	H09-017993A	December 8, 1995	January 17, 1997	Michiguchi et al.	SAM-W&W_00035269- SAM-W&W_00035281
JP	H09-246586A	March 5, 1996	September 19, 1997	Doi et al.	SAM-W&W_00035282- SAM-W&W_00035292
JP	H11-195810A	December 26, 1997	July 21, 1999	Toda	SAM-W&W_00035293- SAM-W&W_00035300
JP	H11-195806A	December 26, 1997	July 21, 1999	Toda	SAM-W&W_00035301- SAM-W&W_00035309
JP	2002-314116A	April 9, 2001	October 25, 2002	Harada et al.	SAM-W&W_00026604- SAM-W&W_00026621; SAM-W&W_00027055- SAM-W&W_00027063
JP	2003-031790A	July 17, 2001	January 31, 2003	Uda et al.	SAM-W&W_00034765- SAM-W&W_00034786
JP	2003-133251A	October 24, 2001	May 9, 2003	Wada et al.	SAM-W&W_00034787- SAM-W&W_00034795
JP	2004-193527A	December 13, 2002	July 8, 2004	Kuriyama et al.	SAM-W&W_00034796- SAM-W&W_00034822

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
JP	2004-319664A	April 15, 2003	November 11, 2004	Ishi et al.	SAM-W&W_00034823- SAM-W&W_00034836
JP	2005-159002A	November 26, 2003	June 16, 2005	Koyama et al.	SAM-W&W_00034837- SAM-W&W_00034852
JP	2006-173329A	December 15, 2004	June 29, 2006	Masamitsu et al.	SAM-W&W_00026622- SAM-W&W_00026668; SAM-W&W_00034853- SAM-W&W_00034899; SAM-W&W_00039941- SAM-W&W_00040007
					SAM-W&W_00034900- SAM-W&W_00034922
					SAM-W&W_00034923- SAM-W&W_00034932
					SAM-W&W_00034933- SAM-W&W_00034940
JP	2006-245163A	March 2, 2005	September 14, 2006	Hirano et al.	SAM-W&W_00026669- SAM-W&W_00026691; SAM-W&W_00026954- SAM-W&W_00026982
JP	2006-339533A	June 3, 2005	December 14, 2006	Hasegawa	SAM-W&W_00026692- SAM-W&W_00026711
JP	2007-059615A	August 24, 2005	March 8, 2007	Kayao et al.	SAM-W&W_00026712- SAM-W&W_00026776
JP	2007-129024A	November 2, 2005	May 24, 2007	Hasegawa et al.	SAM-W&W_00034970- SAM-W&W_00034987
JP	2007-165359A	December 9, 2005	June 28, 2007	Makita et al.	SAM-W&W_00034988- SAM-W&W_00035004
JP	2007-273832A	March 31, 2006	October 18, 2007	Okamoto	
JP	2007-281266A	April 10, 2006	October 25, 2007	Inoguchi	
JP	2008-028421A	October 10, 2007	February 7, 2008	Yagyu et al.	

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
JP	2008-311562A	June 18, 2007	December 25, 2008	Obara et al.	SAM-W&W_00026777- SAM-W&W_00026803; SAM-W&W_00026983- SAM-W&W_00027019
JP	2008-544559A	June 28, 2006	December 4, 2008	Morse et al.	SAM-W&W_00035042- SAM-W&W_00035055
JP	2009-130276A	November 27, 2007	June 11, 2009	Tai et al.	SAM-W&W_00026804- SAM-W&W_00026883
JP	2009-206304A	February 28, 2008	September 10, 2009	Ishimura et al.	SAM-W&W_00035056- SAM-W&W_00035066
JP	2010-212347A	March 9, 2009	September 24, 2010	Imai	SAM-W&W_00035067- SAM-W&W_00035086
JP	2010-212469A	March 11, 2009	September 24, 2010	Yokoyama	SAM-W&W_00035087- SAM-W&W_00035120
JP	2010-232264A	March 26, 2009	October 14, 2010	Miura et al.	SAM-W&W_00026884- SAM-W&W_00026940
JP	2011-077370A	September 30, 2009	April 14, 2011	Otsuki	SAM-W&W_00035121- SAM-W&W_00035136
JP	2011-135058A	November 24, 2010	July 7, 2011	Hiruma et al.	SAM-W&W_00035137- SAM-W&W_00035183
JP	2011-139058A	December 15, 2010	July 14, 2011	Wehner et al.	SAM-W&W_00035184- SAM-W&W_00035196
JP	2012-178457A	February 25, 2011	September 13, 2012	Enomoto	SAM-W&W_00035197- SAM-W&W_00035233
JP	2013-033864A	August 2, 2011	February 14, 2013	Sasaki et al.	SAM-W&W_00035234- SAM-W&W_00035268
JP	2013-157567A	January 31, 2012	August 15, 2013	Noda et al.	SAM-W&W_00035310- SAM-W&W_00035332

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JP	05343729A	June 12, 1992	December 24, 1993	Ajisawa et al.	SAM-W&W_00027020- SAM-W&W_00027035
JP	3912024B2	April 9, 2001	May 9, 2007	Harada et al.	SAM-W&W_00026941- SAM-W&W_00026953
JPWO	2009/088071	January 9, 2009	May 26, 2011	Okamoto et al.	SAM-W&W_00027036- SAM-W&W_00027054
KR	100439760B1	June 18, 2002	July 12, 2004	Noh et al.	SAM-W&W_00027064- SAM-W&W_00027079
KR	2004-0036338	October 24, 2002	April 30, 2004	Choi et al.	SAM-W&W_00035336- SAM-W&W_00035341
KR	2004-0076331	February 25, 2003	September 1, 2004	Kim et al.	SAM-W&W_00035342- SAM-W&W_00035360
KR	100851759B1	May 3, 2007	August 11, 2008	Shim	SAM-W&W_00027080- SAM-W&W_00027105
KR	2010-0135548	June 17, 2009	December 27, 2010	Cho et al.	SAM-W&W_00035361- SAM-W&W_00035416
WO	2006/129427	April 18, 2006	December 7, 2006	Katoh et al.	SAM-W&W_00033932- SAM-W&W_00033960
WO	2009/034623	September 12, 2007	March 19, 2009	Masuoka et al.	SAM-W&W_00039487- SAM-W&W_00039539
WO	2008/052067	October 24, 2007	May 2, 2008	Munteanu et al.	SAM-W&W_00039484- SAM-W&W_00039486
WO	2010/037830	October 1, 2009	April 8, 2010	Neuilly	SAM-W&W_00033961- SAM-W&W_00033993
WO	2011/047359	October 15, 2010	April 21, 2011	Lal et al.	SAM-W&W_00039540- SAM-W&W_00039621
WO	2011/083674	December 17, 2010	July 14, 2011	Shigeta et al.	SAM-W&W_00039622- SAM-W&W_00039677

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
WO	2011/083694	December 22, 2010	July 14, 2011	Shigeta et al.	SAM-W&W_00039678- SAM-W&W_00039727
WO	2011/085297	May 22, 2014	May 5, 2016	Han et al.	SAM-W&W_00033994- SAM-W&W_00034036
WO	2012/053491	October 17, 2011	April 26, 2012	Hiroaki et al.	SAM-W&W_00034037- SAM-W&W_00034167
WO	2012/056782	July 29, 2011	May 3, 2012	Masuoka, et al.	SAM-W&W_00034168- SAM-W&W_00034281
WO	2012/117469	October 31, 2011	September 7, 2012	Honma	SAM-W&W_00039728- SAM-W&W_00039765
WO	2012/121706	March 8, 2011	September 13, 2012	Oh et al.	SAM-W&W_00034282- SAM-W&W_00034318
WO	2012/160662	May 25, 2011	November 10, 2015	Watanabe et al.	SAM-W&W_00034319- SAM-W&W_00034371
WO	2012/167282	June 4, 2012	December 6, 2012	Pacifici et al.	SAM-W&W_00039766- SAM-W&W_00039807
WO	2013/111173	January 23, 2013	August 1, 2013	Oda et al.	SAM-W&W_00039808- SAM-W&W_00039847
WO	2013/136022	February 27, 2014	September 12, 2014	Simon et al.	SAM-W&W_00034473- SAM-W&W_00034488
WO	2013/189932	June 18, 2013	December 27, 2013	Wilhelm	SAM-W&W_00034372- SAM-W&W_00034423
WO	2013/190646	June 20, 2012	December 27, 2013	Watanabe et al.	SAM-W&W_00039848- SAM-W&W_00039897
WO	2014/136022	February 27, 2014	September 12, 2014	Perraud et al.	SAM-W&W_00034424- SAM-W&W_00034472
WO	2014/190189	May 22, 2014	November 27, 2014	Wang et al.	SAM-W&W_00034489- SAM-W&W_00034627

Table 2: Non-Patent Publications

Title	Publication Date	Author(s)	Publisher	Bates Range
Adhesive Chemistry: Developments and Trends	1984	Lieng-Huang Lee (ed.)	Plenum Press	SAM-W&W_00036266-SAM-W&W_00037111
Integrated Electronic and Photonic Devices	1985	Margalit et al.	Bell Telephone Laboratories, Inc.	SAM-W&W_00026509-SAM-W&W_00026569
Monolithic Optoelectronic Integration: A New Component Technology for Lightwave Communications	December 1985	Forrest	IEEE	SAM-W&W_00027151-SAM-W&W_00027166
CMOS Active Pixel Image Sensor	March 3, 1994	Mendis et al.	IEEE	SAM-W&W_00024533-SAM-W&W_00024534
Mechanisms of recombination in GaN photodetectors	1996	Binet et al.	Applied Physics Letters	SAM-W&W_00027133-SAM-W&W_00027136
Intel Releases 971 PC Camera Kit For Production Of Affordable, Easy-To-Use, Portable PC Cameras	1997	Intel	Intel	SAM-W&W_00034749-SAM-W&W_00034751
CMOS Image Sensors: Electronic Camera-on-a-Chip	October 10, 1997	Fossum	IEEE	SAM-W&W_00024550-SAM-W&W_00024559
CMOS Image Sensors Challenge CCDs	1998	Diefendorff	Microdesign Resources, Microprocessor Report	SAM-W&W_00034681-SAM-W&W_00034685
A 19.8% Efficient Honeycomb Multicrystalline Silicon Solar Cell with Improved Light Trapping	October 10, 1999	Zhao et al.	IEEE	SAM-W&W_00024431-SAM-W&W_00024436

Title	Publication Date	Author(s)	Publisher	Bates Range
Advanced Optoelectronic Devices: Chapter 4 Photodetectors	1999	Dragoman et al.	Springer	SAM-W&W_00024465- SAM-W&W_00024521
Electrical Engineering Dictionary	2000	Laplante et al.	CRC Press LLC	SAM-W&W_00025575- SAM-W&W_00026348
Performance Analysis of a Color CMOS Photogate Image Sensor	2000	Blanksby et al.	IEEE	SAM-W&W_00037112- SAM-W&W_00037121
IEEE 100 The Authoritative Dictionary of IEEE Standard Terms (7th Edition)	2000	IEEE	IEEE	SAM-W&W_00026454- SAM-W&W_00026457
Signal Processing in CMOS Image Sensors	2000	Nair et al.	IEEE	SAM-W&W_00035508- SAM-W&W_00035517
CMOS Logic Circuit Design	2001	Uyemura	Kluwer Academic Publishers	SAM-W&W_00024660- SAM-W&W_00025208
OMNIVISION Announces 1.3-Megapixel CMOS Image Sensors	2001	OmniVision	OmniVision	SAM-W&W_00037143- SAM-W&W_00037145
OMNIVISION Announces Expanded Image Sensor	2001	OmniVision	OmniVision	SAM-W&W_00037146- SAM-W&W_00037150
OMNIVISION Datasheet OV9610/OV9110 CMOS Image Sensors	2001	OmniVision	OmniVision	SAM-W&W_00037229- SAM-W&W_00037241
The effect of indium tin oxide as an ohmic contact for the 850 nm GaAs oxide-confined VCSELs	February 2002	Jiang et al.	Elsevier Science Ltd.	SAM-W&W_00031762- SAM-W&W_00031765

Title	Publication Date	Author(s)	Publisher	Bates Range
Deeply Etched Grating Structures for Enhanced Absorption in Thin C-Si Solar Cells	2002	Zaidi et al.	IEEE	SAM-W&W_00037139- SAM-W&W_00037142
CMOS Sensor Inc. website describing Contact Image Sensor (CIS)	2002	CMOS Sensor Inc.	CMOS Sensor Inc.	SAM-W&W_00037151- SAM-W&W_00037151
Silicon-on-insulator waveguide photodetector with Ge/Si self-assembled islands	2002	El Kurdi et al.	Journal of Applied Physics	SAM-W&W_00030532- SAM-W&W_00030536
Silicon Substrates with Buried Distributed Bragg Reflectors for Resonant Cavity-Enhanced Optoelectronics	2002	Emsley et al.	IEEE	SAM-W&W_00035518- SAM-W&W_00035525
Semiconductor Physics and Devices Basic Principles (3d Edition)	2003	Neamen	McGraw Hill	SAM-W&W_00029760- SAM-W&W_00029767
Integration of 10Gb/sec Silicon Lateral Trench Photodetector with High-Performance CMOS	2003	Yang et al.	IEEE	SAM-W&W_00026577- SAM-W&W_00026578
Silicon Optoelectronic Integrated Circuits	2004	Zimmermann	Springer	SAM-W&W_00030159- SAM-W&W_00030524
Optical Microscopy Primer: Introduction to CMOS Image Sensors	July 16, 2004	Turchetta et al.	The Florida State University & Michael W. Davidson	SAM-W&W_00027641- SAM-W&W_00027649

Title	Publication Date	Author(s)	Publisher	Bates Range
Characterization of CsI photocathodes at grazing incidence for use in a unit quantum efficiency x-ray streak camera	October 2004	Lowney et al.	American Institute of Physics	SAM-W&W_00024646-SAM-W&W_00024652
A 3.9-mm Pixel Pitch VGA Format 10-b Digital Output CMOS Image Sensor With 1.5 Transistor/Pixel	December 2004	Takahashi et al.	IEEE J. Solid-State Circuits	SAM-W&W_00034660-SAM-W&W_00034668
CMOS Image Sensors	May 2005	El Gamal et al.	IEEE	SAM-W&W_00024535-SAM-W&W_00024549
Aligned Single-Crystalline Si Nanowire Arrays for Photovoltaic Applications	August 18, 2005	Peng et al.	Wiley Online Library	SAM-W&W_00035487-SAM-W&W_00035492
Shared pixels for CMOS image sensor arrays	2005	McGrath et al.	IEEE	SAM-W&W_00035453-SAM-W&W_00035457
Highly Integrated VCSEL-Based 10Gb/s Miniature Optical Sub-Assembly	2005	Bernabe et al.	IEEE	SAM-W&W_00026448-SAM-W&W_00026453
Roadmap for High Efficiency Solid-State Neutron Detectors	October 2005	Nikolic et al.	Digital Commons	SAM-W&W_00029151-SAM-W&W_00029161
Integration of Photonic Detectors in Standard SiGe HBT BiCMOS	2006	Meinhardt et al.	The Electrochemical Society	SAM-W&W_00026579-SAM-W&W_00026593
1/2-inch 7.2MPixel CMOS Image Sensor with 2.25µm Pixels Using 4-Shared Pixel Structure for Pixel-Level Summation	2006	Kim et al.	IEEE -- International Solid State Circuits Conference	SAM-W&W_00035424-SAM-W&W_00035433

Title	Publication Date	Author(s)	Publisher	Bates Range
MT9T031 Image Sensor – Product Brief	2006	Micron Technology	Micron Technology	SAM-W&W_00037217- SAM-W&W_00037228
Advances in fully CMOS integrated photonic devices	February 9, 2007	Michel et al.	SPIE	SAM-W&W_00024522- SAM-W&W_00024532
Deep Trench Isolation for Crosstalk Suppression in Active Pixel Sensors with 1.7 m Pixel Pitch	April 24, 2007	Park et al.	Japanese Journal of Applied Physics	SAM-W&W_00035479- SAM-W&W_00035482
High Sensitivity of Dielectric films Structure for Advanced CMOS Image Sensor Technology	June 7-10, 2007	Chang et al.	IEEE	SAM-W&W_00026427- SAM-W&W_00026431
Strong broadband optical absorption in silicon NW films	July 17, 2007	Tsakalakos et al.	Society of Photo-Optical Instrumentation Engineers	SAM-W&W_00035534- SAM-W&W_00035544
Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications	October 10, 2007	Hu et al.	American Chemical Society	SAM-W&W_00034742- SAM-W&W_00034747
Nanophotonic Materials Photonic Crystals, Plasmonics, and Metamaterials	November 2007	Wehrspohn et al.	Wiley-VCH	SAM-W&W_00027190- SAM-W&W_00027638
Gr Gb difference in 3M CMOS Image Sensor with 1.75µm pixel	2007	Kim et al.	International Image Sensors Society (IISS)	SAM-W&W_00035434- SAM-W&W_00035437
Nanoelectrode Lithography: Chemical Nanoimprint that Transfers a Pattern by Electrochemical Reaction	August 2008	Yokoo et al.	NTT Technical Review	SAM-W&W_00027182- SAM-W&W_00027189

Title	Publication Date	Author(s)	Publisher	Bates Range
Optical confinement methods for continued scaling of CMOS image sensor pixels	November 25, 2008	Fesenmaier et al.	Optical Society of America	SAM-W&W_00027670- SAM-W&W_00027683
Advanced image sensor technology for pixel scaling down toward 1.0µm	2008	Ahn et al.	IEEE	SAM-W&W_00034672- SAM-W&W_00034675
Process Flow Innovations for Photonic Device Integration in CMOS	2008	Beals et al.	Society of Photo-Optical Instrumentation Engineers (SPIE)	SAM-W&W_00029133- SAM-W&W_00029146
Monolithic Integration of Photonic and Electronic Circuits in a CMOS Process	2008	Mekis et al.	SPIE	SAM-W&W_00027137- SAM-W&W_00027150
Photonic Crystals: Physics and Technology	2008	Sibilia et al.	Springer	SAM-W&W_00028844- SAM-W&W_00029132
Photonic Crystals Molding the Flow of Light 2d Edition	2008	Joannopoulos et al.	Princeton University Press	SAM-W&W_00027684- SAM-W&W_00027988
Through Silicon Vias Technology for CMOS Image Sensors Packaging	2008	Henry et al.	IEEE	SAM-W&W_00037832- SAM-W&W_00037841
Photonic Crystals Towards Nanoscale Photonic Devices 2d Edition	2008	Benisty et al.	Springer	SAM-W&W_00027989- SAM-W&W_00028502
Porous Silicon Carbide and Gallium Nitride	2008	Feenstra et al.	John Wiley & Sons, Ltd.	SAM-W&W_00028503- SAM-W&W_00028843

Title	Publication Date	Author(s)	Publisher	Bates Range
Absorption Enhancement in Thin-Film Silicon Solar Cells in SOI Configuration Using Physical and Geometrical Optics	2008	Prinja et al.	IEEE	SAM-W&W_00024452- SAM-W&W_00024455
CMOS Image Sensor with two-shared pixel and staggered readout architecture	June 26-28, 2009	Bogaerts et al.	International Image Sensor Workshop	SAM-W&W_00034686- SAM-W&W_00034689
Silicon Nanowire-Based Solar Cells on Glass: Synthesis, Optical Properties and Cell Parameters	March 12, 2009	Sivakov et al.	American Chemical Society	SAM-W&W_00034654- SAM-W&W_00034653
Focused ion beam technology and ultimate applications	March 20, 2009	Gierak	Semiconductor Science and Technology	SAM-W&W_00026385- SAM-W&W_00026407
Optical absorption enhancement in silicon nanowire arrays with a large lattice constant for photovoltaic applications	October 26, 2009	Lin et al.	Optical Society of America	SAM-W&W_00035442- SAM-W&W_00035452
Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic application	2010	Lin et al.	IEEE	SAM-W&W_00035477- SAM-W&W_00035478
Optical absorption enhancement in nanopore textured-silicon thin film for photovoltaic application	January 1, 2010	Wang et al.	Optical Society of America	SAM-W&W_00027650- SAM-W&W_00027652
Optical Absorption Enhancement in Silicon Nanohole Arrays for Solar Photovoltaics	February 8, 2010	Han et al.	American Chemical Society	SAM-W&W_00027655- SAM-W&W_00027658

Title	Publication Date	Author(s)	Publisher	Bates Range
Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications	February 14, 2010	Kelzenberg et al.	Macmillan Publishers Limited	SAM-W&W_00035417- SAM-W&W_00035423
A grazing incidence x-ray streak camera for ultrafast, single-shot measurements	March 29, 2010	Feng et al.	American Institute of Physics Publishing	SAM-W&W_00024437- SAM-W&W_00024441
High-Performance Silicon Nanohole Solar Cells	May 2010	Peng et al.	American Chemical Society	SAM-W&W_00026445- SAM-W&W_00026447
NREL's Black Silicon Increases Solar Cell Efficiency by Reducing Reflected Sunlight	November 2010	National Renewable Energy Laboratory	National Renewable Energy Laboratory	SAM-W&W_00027180- SAM-W&W_00027181
Light Trapping in Silicon Nanowire Solar Cells	2010	Garnett et al.	American Chemical Society	SAM-W&W_00027117- SAM-W&W_00027122
Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications	2010	Lin et al.	SPIE	SAM-W&W_00027659- SAM-W&W_00027669
Integrated microsystem for blue/ultraviolet detection	2010	Pauchard et al.	MCB University Press	SAM-W&W_00026570- SAM-W&W_00026576
Semiconductor Devices Physics and Technology (3d Edition)	2012	Sze et al.	IEEE	SAM-W&W_00037242- SAM-W&W_00037831
Controlling Light in Optically Induced Photonic Lattices	2011	Terhalle	Springer Theses	SAM-W&W_00025209- SAM-W&W_00025324
Silicon Nanowires for Photovoltaic Solar Energy Conversion	2011	Peng et al.	Advanced Materials	SAM-W&W_00030141- SAM-W&W_00030158

Title	Publication Date	Author(s)	Publisher	Bates Range
Review of the 1.4 μm Pixel Generation	2011	Fontaine	International Image Sensors Society (IISS)	SAM-W&W_00034719- SAM-W&W_00034722
Pixel-to-Pixel isolation by Deep Trench technology: Application to CMOS Image Sensor	2011	Tournier et al.	International Image Sensors Society (IISS)	SAM-W&W_00035530- SAM-W&W_00035533
A 300nm Wafer-Size CMOS Image Sensor with In-Pixel Voltage-Gain Amplifier and Column-Level Differential Readout Circuitry	2011	Yamashita	IEEE International Solid-State Circuits Conference	SAM-W&W_00034669- SAM-W&W_00034671
A photonic-plasmonic structure for enhancing light absorption in thin film solar cells	September 30, 2011	Bhattacharya et al.	Applied Physics Letters	SAM-W&W_00024442- SAM-W&W_00024445
Optical Absorption Enhancement in Silicon Nanohole Arrays for Photovoltaics	2011	Chen et al.	IEEE	SAM-W&W_00035474- SAM-W&W_00035476
Ge-on-Si optoelectronics	October 29, 2011	Liu et al.	Elsevier	SAM-W&W_00034723- SAM-W&W_00034729
Design and fabrication of photonic crystals in epitaxial free silicon for ultrathin solar cells	November 13-16, 2011	Meng et al.	IEEE	SAM-W&W_00035458- SAM-W&W_00035464
A simple and low-cost technique for silicon nanowire arrays based solar cells	December 7, 2011	Huang et al.	Elsevier B.V.	SAM-W&W_00024446- SAM-W&W_00024451
Light harvesting by planar photonic crystals in solar cells: the case of amorphous silicon	January 12, 2012	Gomard et al.	IOP Publishing Ltd.	SAM-W&W_00034730- SAM-W&W_00034741

Title	Publication Date	Author(s)	Publisher	Bates Range
Black Silicon Antireflection Technology	February 14, 2012	Dennis J. Flood	InterPV	SAM-W&W_00035472- SAM-W&W_00035473; SAM-W&W_00040106- SAM-W&W_00040110
A 1920x1080 3.65 µm-Pixel 2D/3D Image Sensor with Split and Binning Pixel Structure in 0.11 µm Standard CMOS	February 22, 2012	Kim et al.	ISSCC	SAM-W&W_00035493- SAM-W&W_00035495
Electrical Properties of ITO/Crystalline-Silicon Contact at Different Deposition Temperatures	March 2012	De Cesare et al.	IEEE	SAM-W&W_00034716- SAM-W&W_00034718
Experimental Study of Design Parameters in Silicon Micropillar Array Solar Cells Produced by Soft Lithography and Metal-Assisted Chemical Etching	April 2012	Shin et al.	IEEE	SAM-W&W_00026380- SAM-W&W_00026384
Design, fabrication and optical characterization of photonic crystal assisted thin film monocrystalline-silicon solar cells	May 11, 2012	Meng et al.	Optical Society of America (OSA)	SAM-W&W_00034705- SAM-W&W_00034715
Efficient Light Trapping in Inverted Nanopyramid Thin Crystalline Silicon Membranes for Solar Cell Applications	May 21, 2012	Mavrokefalos et al.	Nano Letter	SAM-W&W_00040008- SAM-W&W_00040012

Title	Publication Date	Author(s)	Publisher	Bates Range
Efficient Light-Trapping in Inverted Nano-Pyramid Thin Crystalline Silicon Membranes for Solar Cell Applications	June 13, 2012	Mavrokefalos et al.	American Chemical Society	SAM-W&W_00036261-SAM-W&W_00036265
Current-Voltage Characteristics of ITO/p-Si and ITO/n-Si Contact Interfaces	June 2012	Pethuraja et al.	Advances in Materials Physics and Chemistry	SAM-W&W_00037135-SAM-W&W_00037138
Sony develops 'Exmor RS,' the world's first stacked CMOS image sensor	August 20, 2012	Sony	Phys Org	SAM-W&W_00024420-SAM-W&W_00024423
High-contrast gratings for integrated optoelectronics	September 4, 2012	Chang-Hasnain, et al.	Advances in Optics and Photonics	SAM-W&W_00037155-SAM-W&W_00037216
Characteristics of large-scale nanohole arrays for thin-silicon photovoltaics	October 1, 2012	Chen et al.	Wiley Online Library	SAM-W&W_00024636-SAM-W&W_00024645
Natcore Builds World's First Black Silicon Solar Cell Using Scalable Production Process	November 7, 2012	Inhabitat	Inhabitat	SAM-W&W_0027639-SAM-W&W_0027640
A CMOS Image Sensor Based on Unified Pixel Architecture With Time-Division Multiplexing Scheme for Color and Depth Image Acquisition	November 2012	Kim et al.	IEEE	SAM-W&W_00035496-SAM-W&W_00035507
High responsivity MSM black silicon photodetector	December 21, 2012	Su et al.	Elsevier	SAM-W&W_00026438-SAM-W&W_00026444

Title	Publication Date	Author(s)	Publisher	Bates Range
Advanced Imaging Research and Development at DARPA	2012	Dhar et al.	SPIE	SAM-W&W_00024456- SAM-W&W_00024464
Suppression of Crosstalk by Using Backside Deep Trench Isolation for 1.12µm Backside Illuminated CMOS Image Sensor	2012	Kitamura et al.	IEEE	SAM-W&W_00035438- SAM-W&W_00035441
Characterization of light absorption in thin-film silicon with periodic nanohole arrays	March 4, 2013	Yahaya et al.	Optical Society of America	SAM-W&W_00024653- SAM-W&W_00024659
Canon develops 35 mm full-frame CMOS sensor for video capture	March 4, 2013	Canon	Canon	SAM-W&W_00024632- SAM-W&W_00024633
Silicon/organic hybrid heterojunction infrared photodetector operating in the telecom regime	March 14, 2013	Bednorz et al.	Elsevier B.V.	SAM-W&W_00030525- SAM-W&W_00030531
Resolution Limits of Electron-Beam Lithography toward the Atomic Scale	March 14, 2013	Manfrinato et al.	American Chemical Society	SAM-W&W_00029147- SAM-W&W_00029150
Optical absorption enhancement in partially aperiodic silicon nanohole structures for photovoltaics	2013	Lin et al.	Optical Society of America	SAM-W&W_00027653- SAM-W&W_00027654
Advances in Infrared Detector Array Technology	2013	Dhar et al.	InTech	SAM-W&W_00026467- SAM-W&W_00026508
SiOnyx Announces First Products	April 4, 2013	Image Sensors World	Image Sensors World	SAM-W&W_00034628- SAM-W&W_00034635

Title	Publication Date	Author(s)	Publisher	Bates Range
SNR Metric and Crosstalk in Color Image Sensor of Small Size Pixel	April 22-24, 2013	Ahn et al.	IEEE	SAM-W&W_00034676- SAM-W&W_00034677
DSS 2013: SiOnyx sees digitally with 'black' silicon	May 6, 2013	Optics.org	Optics.org	SAM-W&W_00034652- SAM-W&W_00034653
Canon EOS 70D Specs (New Sensor), to be announced on July 2	June 27, 2013	Cameraegg	Cameraegg	SAM-W&W_00024611- SAM-W&W_00024613
Canon develops new Dual Pixel CMOS AF technology for significantly improved autofocus performance during Live View shooting and when shooting movies	July 2, 2013	Canon	Canon	SAM-W&W_00024634- SAM-W&W_00024635
Monolithic VCSEL-PIN Photodiode Integration for Bidirectional Optical Data Transmission	August 2013	Kern et al.	IEEE	SAM-W&W_00027167- SAM-W&W_00027179
A novel silicon nanostructure with effective light trapping for polycrystalline silicon thin film solar cells by means of metal-assisted wet chemical etching	September 20, 2013	Xue	Wiley Online Library	SAM-W&W_00039898- SAM-W&W_00039901
Natcore Aims To Make Black Silicon Solar Cells Even Cheaper	December 9, 2013	Tina Casey	CleanTechnica	SAM-W&W_00035465- SAM-W&W_00035471
The Evolution of CMOS Image Sensors	2013	Hirayama	IEEE	SAM-W&W_00035526- SAM-W&W_00035529

Title	Publication Date	Author(s)	Publisher	Bates Range
HOT infrared photodetectors	2013	Martyniuk et al.	Opto-Electronics Review	SAM-W&W_00026408- SAM-W&W_00026426
A 1/4-inch 8Mpixel CMOS Image Sensor with 3D Backside-Illuminated 1.12µm Pixel with Front-Side Deep-Trench Isolation and Vertical Transfer Gate	February 9-13, 2014	Ahn et al.	IEEE	SAM-W&W_00034678- SAM-W&W_00034680
Light management for photovoltaics using high-index nanostructures	April 22, 2014	Brongersma et al.	Nature Materials	SAM-W&W_00027123- SAM-W&W_00027132
High quantum efficiency photocathode simulation for the investigation of novel structured designs	Presented June 2, 2014	Opachich et al.	Review of Scientific Instruments	SAM-W&W_00026432- SAM-W&W_00026437
Si Nanostructures based solar cells	2014	Lei	Nanyang Technological University – School of Electrical and Electronic Engineering	SAM-W&W_00029768- SAM-W&W_00029953
Si nanostructures based solar cells	2014	Hong	Nanyang Technological University, School of Electrical and Electronic Engineering	SAM-W&W_00029954- SAM-W&W_00030140
The Art of Electronics (3d Edition)	2016	Horowitz et al.	Cambridge University Press	SAM-W&W_00030537- SAM-W&W_00031761

Title	Publication Date	Author(s)	Publisher	Bates Range
This new phone highlights Samsung's growing photography prowess	December 14, 2016	Deidre R.	SamMobile	SAM-W&W_00040111- SAM-W&W_00040114
High-performance mobile 'Tetracell image sensor' wins Minister's Award at Multimedia Technology Awards!	June 2, 2017	Samsung Semiconductor	Samsung Semiconductor	SAM-W&W_00026349- SAM-W&W_00026355; SAM-W&W_00027107- SAM-W&W_00027113
IR sensitivity enhancement of CMOS Image Sensor with diffractive light trapping pixels	June 19, 2017	Yokogawa et al.	Scientific Reports	SAM-W&W_00026458- SAM-W&W_00026466
Sony Enhances IR Sensitivity by 80% with Pyramidal Structure	June 20, 2017	Image Sensors World	Image Sensors World	SAM-W&W_00024424- SAM-W&W_00024430
Cameras with Black Silicon Sensors Reach the Market	September 22, 2017	Image Sensors World	Image Sensors World	SAM-W&W_00034636- SAM-W&W_00034643
Samsung Electronics Launches Two New Ultra-Compact High-Definition Image Sensors ISOCELL	October 11, 2017	Samsung Semiconductor	Samsung Semiconductor	SAM-W&W_00026356- SAM-W&W_00026359; SAM-W&W_00027114- SAM-W&W_00027116
Samsung's new dual pixel mobile sensor wants to eliminate dual cameras in smartphones	October 12, 2017	John Aldred	DIY Photography	SAM-W&W_00029168- SAM-W&W_00029169
Samsung Honored for Outstanding Design and Engineering with 36 CES 2018 Innovation Awards	November 10, 2017	Yoon Sang-ho	Digital Daily	SAM-W&W_00029162- SAM-W&W_00029167

Title	Publication Date	Author(s)	Publisher	Bates Range
2017 Pixel Technology in Review	December 19, 2017	Image Sensors World	Image Sensors World	SAM-W&W_00034644-SAM-W&W_00034651
An All Pixel PDAF CMOS Image Sensor with $0.64\mu\text{m} \times 1.28\mu\text{m}$ Photodiode Separated by Self-aligned In-pixel Deep Trench Isolation for High AF Performance	2017	Choi et al.	IEEE	SAM-W&W_00034703-SAM-W&W_00034704
Canon Autofocus Series: Dual Pixel CMOS AF Explained	April 27, 2018	Canon	Canon	SAM-W&W_00024601-SAM-W&W_00024610
Pixel Technology for Improving IR Quantum Efficiency of Backsideilluminated CMOS Image Sensor	2019	Park et al.	International Image Sensors Society (IIS)	SAM-W&W_00035483-SAM-W&W_00035486
Canon Technology Explainer: What is Dual Pixel CMOS AF?	December 16, 2022	Canon	Snapshot	SAM-W&W_00024614-SAM-W&W_00024631
CMOS Sensor Inc: About LinkedIn	July 18, 2024	CMOS Sensor Inc.	LinkedIn	SAM-W&W_00037152-SAM-W&W_00037154
Intel 971 PC Camera Kit (1997)	2024	Digitalcamera Museum	Digitalcamera Museum	SAM-W&W_00034748-SAM-W&W_00034748
Intro to Dual Pixel Autofocus (DPAF)	2025	Winston	Canon	SAM-W&W_00026594-SAM-W&W_00026603
DUAL PIXEL CMOS AF	2025	EOS Magazine	EOS Magazine	SAM-W&W_00025478-SAM-W&W_00025484
Everything you wanted to know about autofocus (AF)	2025	Canon	Canon	SAM-W&W_00026360-SAM-W&W_00026379

Defendants further incorporate by reference all “U.S. Patent Documents” and “Other Publications” cited on the face of the Patents-in-Suit. Any citation to one or more of the above prior art references, or other prior art references regarding any method or system, should be construed to constitute not only a citation to the prior art reference itself, but also a reference to the system itself. Discovery has only just begun in this case, and Defendants will supplement if and when more information becomes available from Plaintiff or third parties.

B. Prior Art Disclosures—Known/Use/Sales/Offers for Sale

Defendants believe that there were prior art disclosures in the form of sales, offers for sale, and/or uses by others of products that qualify as prior art under pre-AIA 35 U.S.C. § 102(a) and/or (b) or under AIA 35 U.S.C. § 102(a)(1) against one or more of the Asserted Claims of the Patents-in-Suit. The below-identified prior art products include products Defendants are currently aware of through an on-going diligent and reasonable investigation at this early stage of discovery and/or based on publicly available information. Details regarding such offers for sale and public uses may be within the possession of third parties. As discovery progresses, Defendants intend and reserve the right to promptly supplement and/or amend the lists below to include additional prior art products that anticipate and/or render obvious the asserted claims. To the extent Plaintiff contends that any systems presented below do not qualify as prior art to one or more Patents-in-Suit, Defendants reserve the right to rely on any of such systems as evidence of simultaneous development as an indicia of obviousness.

Table 3: Prior Art Products

System	Sale or Use Date
Intel Corp.'s 971 PC Camera Kit including CMOS Image Sensor for "portable PC cameras for home and business users"	At least as early as November 3, 1997
OMNIVISION Technologies, Inc.'s CMOS Image Sensors, including 1.3-Megapixel CMOS Image Sensors, OV8610 and OV8110 SVGA Sensors, OV5116 TV Sensor, OV6630 and OV6130 CIF Sensors.	At least as early as April 23, 2001
CMOS Image Sensor, Inc.'s CMOS image sensors.	At least as early as May 3, 2002
SiOnyx XQE CMOS sensors, including XQE-1310, XQE-0920, XQE-0570	At least as early as 2013

System	Sale or Use Date
Natcore black silicon solar cells	At least as early as 2012
Solar Cells with Inverted Nanopyramid Thin Crystalline Silicon Membranes for Efficient Light Trapping	At least as early as 2012
Samsung's ISOCELL products with dual-PD or similar PDAF features	At least as early as 2016
Samsung CMOS Image Sensor products with RGB Bayer or similar pixel-binning features	At least as early as 2016
Canon Dual Pixel Autofocus CMOS sensor products	At least as early as 2013
DARPA infrared detector	At least as early as 2012
Sony CMOS Image Sensors	At least as early as 2008

For the public uses identified herein, Defendants are investigating the identities of the individuals who knew about and/or were involved in the making, first public use, offer for sale and/or sale of these products and systems. Defendants are also investigating the exact date that these products and systems were first made, first publicly used, offered for sale and/or sold. In addition, Defendants are currently investigating the dates of conception and reduction to practice of these products and systems and when these products and systems were first known or used by others.

In the course of their investigation, Defendants may identify additional prior art documents describing these products, systems, and/or disclosures that may also anticipate and/or render obvious as invalidating printed publications. Any citation to one or more of prior art references regarding these products, systems, and/or disclosures should be construed to constitute not only a citation to the prior art reference itself, but also a reference to the associated products, systems, and/or disclosures.

3. '543 Patent

**Table 6: Exemplary Anticipatory and Combinations
for the Asserted Claims of the '543 Patent**

Chart	Prior Art References
C1	Kuboi either alone or in combination with one or more of the knowledge of a person of ordinary skill in the art.
C2	NXP either alone or in combination with one or more of Kuboi and Obara.
C3	Wang189 either alone or in combination with one or more of Kuboi, NXP, Obara, and Wang981.
C4	Obara either alone or in combination with one or more of Kuboi and NXP.
C5	Canon Product either alone or in combination with one or more of DARPA Imaging Sensor, Solar Cells, and Kuboi.
C6	Sony CMOS Product either alone or in combination with one or more of DARPA Imaging Sensor, Solar Cells, NXP, Obara, and Kuboi.
C7	Omnivision CMOS Product either alone or in combination with one or more of DARPA Imaging Sensor, Solar Cells, and Kuboi.
C8	Samsung Product under Plaintiff's apparent interpretation of the asserted claims

The prior art identified above, and in the attached '543 charts, individually anticipate and/or can properly be combined in multiple ways to demonstrate the obviousness of the Asserted Claims of the '543 patent. Various combinations of the references would have naturally been considered as part of the exercise of ordinary skill by one skilled in the art. The references disclosed in the attached charts and herein are also directed to the same or similar features as the purported invention claimed in the Asserted Claims of the '543 patent. To the extent Plaintiff contends that any of these features solved a problem in the art, the references cited herein show that that problem was known to those of ordinary skill and had already been solved using obvious solutions.

Dated: May 2, 2025

/s/ Benjamin R. Schlesinger

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Samsung Electronics America, Inc.*

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on May 2, 2025, copies of the foregoing Defendants' Invalidity Contentions and Exhibits have been served to Plaintiff through its counsel of record via email.

/s/ Seth D. Katz
Seth D. Katz
Case Manager



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
19/036,506

RECEIPT DATE / TIME
09/16/2025 11:52:23 AM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 4276

FILED BY Mary Ellen Finnegan

PATENT CENTER # 72308372

FILING DATE 01/24/2025

CUSTOMER # 139982

FIRST NAMED INVENTOR Shih-Yuan WANG

CORRESPONDENCE ADDRESS -

AUTHORIZED BY Gerard Wissing

Documents

TOTAL DOCUMENTS: 8

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV2_IDS_Trans_Filed_16Sep2025_w_Exhibits.pdf	47	Transmittal Letter	360 KB
309-0015USCIPDIV2_IDS_Filed_16Sep2025.pdf	5	Information Disclosure Statement (IDS) Form (SB08)	1315 KB
309-0015USCIPDIV2_Resp_NFOA_Mailed_18Mar2025_Final-APP.TEXT.docx	8	Application body structured text document	169 KB

Warning: The claims appear to contain an improper dependency with at least one claim that depends on a missing or canceled claim. Please review and revise if necessary. The automatic document description has been replaced. The claims appear to contain

an improper dependency with at least one claim that depends on a missing or canceled claim. Please review and revise if necessary.

JP2002314116A_orig_certifiedEnglTrans.pdf	9	Foreign Reference	3633 KB
JP2007129024A__orig_certifiedEnglTrans.pdf	29	Foreign Reference	13823 KB
EP2172974A1.pdf	23	Foreign Reference	1486 KB
Yahaya_Characterization of light absorption.pdf	7	Non Patent Literature	2611 KB
309-0015USCIPDIV2_Resp_NFOA_Mailed_18Mar2025_Final.pdf	8	Auxiliary PDF of Application	249 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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F293C57420A77559550CEDF4F609F84

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875			Application or Docket Number 19/036,506		Filing Date 01/24/2025		☐ To be Mailed	
ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO								
APPLICATION AS FILED - PART I								
FOR		(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE (\$)		FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A		N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		x \$80 =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		x \$240 =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))								
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL			
APPLICATION AS AMENDED - PART II								
		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	09/26/2025	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 13	Minus	** 20	= 0	x \$80 =		0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	x \$240 =		0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
						TOTAL ADD'L FEE		0
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =		
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =		
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
						TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE		
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/ANTJUAN M RIVERA/		
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".								
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.								

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Shih-Yuan WANG et al.
Serial No.: 19/036,506
Examiner: EDUARDO A RODELA
Group Art Unit 2893
Filing Date: 01/24/2025
For: MICROSTRUCTURE ENHANCED ABSORPTION
PHOTOSENSITIVE DEVICES
Conf. No. 4276

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
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CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: September 26, 2025

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Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE TO OFFICE ACTION DATED 03/18/2025

Amendments to the Claims begin on page 2; and
Remarks begin on page 5.

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of the claims in the application.

1-17. (Canceled)

18-36. (Canceled)

37. (New) A structure comprising:

an array of elongated pillars of semiconductor material in which each of at least some of the pillars has:

- (i) a respective light-receiving surface,
- (ii) respective sides,
- (iii) width of 50-2000 nm,
- (iv) height of 100-10000 nm, and
- (v) at least one photodetector of Si, Ge, and/or alloyed SiGe semiconductor material formed in the pillar;

wherein each of the photodetectors:

- (i) has P-doped and N-doped regions of the semiconductor material,
- (ii) is configured to generate electrical charge carriers in the semiconductor material of the photodetector in response to light that (a) is in the visible and infrared wavelengths, and (b) illuminates along a light direction the light-receiving surface of the pillar in which the photodetector is formed;

one or more in-pillar holes each of which:

- (i) is fabricated as a recess in each of the pillars in which at least one of the photodetectors is formed, and
- (ii) extends along the light direction into the semiconductor material of the pillar in which the in-pillar hole is fabricated;

side-isolation comprising solid dielectric material between at least portions of the sides of at least some of the pillars;
electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for selected reverse-biasing at least some of the photodetectors;
wherein the presence of the in-pillar holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors in pillars lacking said holes.

38. (New) The structure of claim 37, in which the array is monolithically integrated with Si electronic devices.
39. (New) The structure of claim 37, in which at least one of the in-pillar holes in each of at least some of the pillars is elongated in the light direction.
40. (New) The structure of claim 37, in which each of at least some of the holes is elongated in a direction along the light-receiving surface of the pillar in which the hole is fabricated.
41. (New) The structure of claim 40, in which the array is monolithically integrated with Si electronic devices.
42. (New) The structure of claim 40, in which each of at least some of the pillars has a plurality of the elongated holes.
43. (New) The structure of claim 40, in which each of at least some of the pillars has only one of the elongated holes.
44. (New) The structure of claim 40, in which each of at least some of the elongated holes has at least one closed contour remote from side edges of the light-receiving surface of the pillar in which the hole is fabricated.

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46. (New) The structure of claim 37, in which two or more of the photodetectors are connected electrically in parallel.

47. (New) The structure of claim 37, wherein the array of pillars is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors.

48. (New) The structure of claim 37, in which at least some of the holes extend 100 to 10000 nm in the light direction into the semiconductor material of the pillars in which the holes are formed.

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With this Supplemental Response, Applicant corrects a claim numbering issue noticed after filing its Response to the Non-Final Office Action dated September 16, 2025. More specifically, in the Preliminary Amendment filed on January 24, 2025, Applicant canceled claims 1-17 and added new claims 18-36. In the Response to the Non-Final Office Action dated September 16, 2025, Applicant again canceled claims 1-17, did not cancel claims 18-36 and added new claims 18-30, which is inconsistent with Office rules. Therefore, in this Supplemental Response, Applicant recognizes that claims 1-17 were previously canceled, has canceled claims 18-36 and adds new claims 37-49 (which are the same as improperly number new claims 18-30).

Interview Summary

Applicant's representative would like to thank Examiner Rodela for his time and professionalism during the interview conducted on September 26, 2025 (the "Interview"). During the Interview, Applicant's representatives, Gerard Wissing and Ivan Kavrukov, advised the Examiner of the above described claim numbering issue and provided the Examiner with additional background information regarding U.S. Publication No. US 2012/0049044 to **Kuboi** identified on page 8 of this Response. There was no discussion regarding claim amendments, except to suggest to Examiner Rodela that Applicant is willing to discuss claim amendments in order to advance prosecution of the subject application.

Priority and Paragraph 112(a)

Examples of support are outlined below in the subject application and in the 2013 provisional applications that are incorporated by reference and to which priority is claimed.

FIG. 5B of the subject application illustrates an example of an array of vertical pillars of semiconductor material such as Si, and FIG. 49 illustrates an example of an in-pillar hole (pillar with hole). Both are reproduced below.

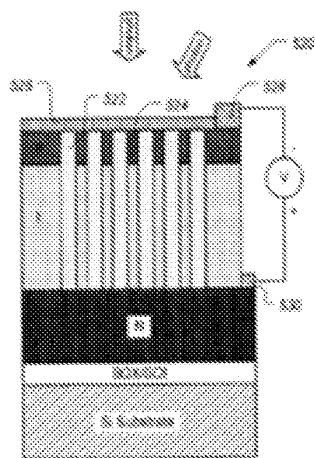


FIG. 5B

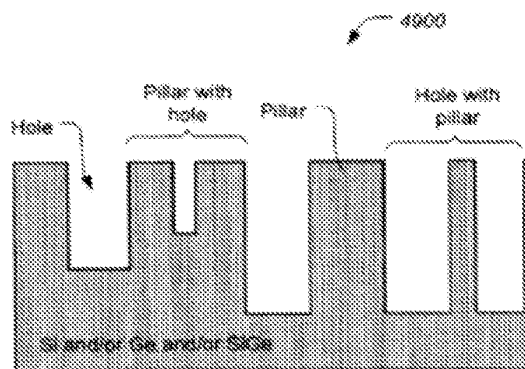


FIG. 49

As seen in FIG. 5B and explained in the text of the subject application, each pillar 524 has a light receiving surface that is on top of the pillar in this example, illuminated with light (photons) in the direction of one or both arrows, has sides, and has at least one photodetector of Si, Ge, or SiGe formed in the pillar.

The width of a pillar can be 50-2000 nm¹ and the height of a pillar can be 100-10000 nm.² Each photodetector has P-doped and N-doped regions and is configured to generate electrical charge carriers in the semiconductor material of the photodetector formed in the pillar in response to light that is in the visible and infrared wavelengths and illuminates the light-receiving surface of the pillar.

Each of the pillars in the array of FIG. 5B can be a “pillar with a hole” as in the example of FIG. 49.³ Each in-pillar hole extends into the pillar in the direction of the light, down into the pillar in this example.

Dielectric material 522 such as oxide forms solid isolation between pillar side walls and, with in-pillar holes in the pillars, fills at least a part of the holes,⁴ and the in-pillar holes can be

¹ Provisional application 61/826,446 filed May 22, 2013, page 12; “The shape of the pillar can be... rectangle.... The pillar diameter range from 50-2000 nm”,

² Provisional application 61/826,446 filed May 22, 2013, page 12: “[P]illars can be 100-10000 nm in length....”

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⁴ See also Figure 8 in page 6 of provisional application 61/826,446 filed May 22, 2013.

oxidized.⁵ Electrical contacts as seen in the example of FIG. 5B provide pathways to the photodetectors and can reverse-bias them.⁶ The presence of the in-pillar holes increases absorption by a factor of at least 1.1 compared to like photodetectors without holes or to bulk semiconductor without holes.⁷

The array of pillars can be monolithically integrated with Si electronic devices.⁸ The in-pillar holes can be elongated – FIG. 46 of the subject application illustrates some examples of holes that are longer in one direction than in an orthogonal direction along the light-receiving surface of a pillar and additionally illustrate that a pillar can have a single hole or multiple holes and that at least one contour of a hole can be away from the outline of a pillar as seen in top view.⁹

Section 103

The references identified in the Office Action, page 8, post-date the 2013 priority of the subject application.

IPRs and PGR regarding commonly assigned patents

IPR and PGR petitions were filed challenging claims in six patents in the family of the subject application,¹⁰ five of which are in a patent infringement action.¹¹

⁵ See also provisional application 61/826,446 filed May 22, 2013, page 16: “[P]aternal filling of the holes with filler” Page 10: “[T]hermal oxidation of exposed surfaces”

⁶ See also provisional application 61/826,446 filed May 22, 2013, page 14: “The photodiode is reversed biased”

⁷ Subject application paragraph 114 (factor of 1.1 to over 100), and provisional application 61/826,446 filed May 22, 2013, Table 8 in page 8, and page 16 (enhancement of the bulk absorption constant). Subject application paragraph [00114].

⁸ Provisional application 61/826,446 filed May 22, 2013, page 1: “Compatible with Si Photonics, CMOS processes ... integration with CMOS highly desirable.” Provisional application 61/834,873 filed June 13, 2013, pages 1-2: “[T]he detector array can be monolithically integrated with Si electronic devices such as bipolar transistors, CMOS”

⁹ See also Fig. 12 in provisional application 61/834,873 filed June 13, 2013.

¹⁰ The IPRs are: (1) Case IPR2025-00993 on patent 12,087,871, (2) Case IPR2025-00994 on patent 11,621,360; (3) Case IPR2025-00995 on patent 10,468,543; (4) Case IPR2025-00996 on patent 10,446,700; and (5) Case IPR-00997 on patent 9,525,084. Applicant is concurrently submitting an IDS identifying the total of 7 references on which the 5 IPRs rely to challenge patentability under Sections 102 or 103. The PGR is Case PGR2025-00082 for patent 12,243,948.

¹¹ The action is: W&Wsens Devices Inc. v. Samsung Elecs. Co., Case No. 2:24-cv-00854-JRG (E.D. Tex.). Defendants have filed pleadings identifying purported prior art, which are available through Pacer. Applicant offers to any of the several hundred patents, published applications, and non-patent publication listed in such pleadings if the Office requests it.

The references that the IPRs and the PGR assert are:

1. **Kuboi** US 2012/0049044
2. **Shinohara** US 2012/0033119
3. **Yu** US 2012/0153124
4. **Harada** Kokai No. 2002-314116 (P2002-314116A)
5. **Hasegawa** Kokai 2007-129024 (P2007-129024A)
6. **NXP** EP 2 172 974 A1
7. **Yahaya**, NA, Characterization of light absorption in thin-film silicon with periodic nanohole arrays, 11 March 2013/Vol. 21, No. 5/OPTICS EXPRESS 5924-5930.
8. **Vasylysev** US 2012/0012741

Applicant submits that claims 18-30 differ patentably from these seven references taken individually or in combination, at least because:

Kuboi proposes a standard semiconductor PIN photodiode 53R with no in-pillar holes and additionally proposes pixels 53R, 53G that generate electrical output only in organic material 13, not in semiconductor material of a photodetector. See Kuboi FIGs. 6A and 10A.

Shinohara proposes an array of standard photodiodes with no in-pillar holes.

Yu proposes nanowires or nanopillars that also lack in-pillar holes.

Harada proposes a lateral photodiode with no pillars along the light direction and no in-pillar holes.

Hasegawa proposes standard photodiodes, lacking in-pillar holes, used in optical disc drive tracking.

NXP proposes standard photodiodes, with no in-pillar holes.

Yahaya proposes a solar cell panel with surface structures but lacks a teaching of pillars of semiconductor material that are electrically isolated from each other and have reverse-biased photodetectors fabricated in the pillars and in-pillar holes with solid dielectric material.

Vasylyev also proposes a solar cell panel with surface structures but lacks a teaching of pillars of semiconductor material that are electrically isolated from each other and have reverse-biased photodetectors fabricated in the pillars and in-pillar holes with solid dielectric material.

The Preliminary Amendment filed 01/24/2025 in the subject application addresses

references cited in application Ser. No. 18/385,213, now patent 12,243,948. They are **Yu** US 2011/0309331), **Lunev** US 2014/001660, **Counil** US 2010/0116332, and **Arimoto** US 5,759,292. Applicant submits that claims 18-30 patentably differ from these references at least for the reasons discussed in the Preliminary Amendment filed 01/24/2025 but also for additional reasons.

Applicant invites the Examiner to telephone the undersigned if the Examiner finds that it may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

/Gerard M. Wissing/

WISSING MILLER LLP
Attorney for Applicant
By: Gerard M. Wissing

Reg. No. 36,309
Tel.: 516-901-7027



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
19/036,506

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309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 4276

FILED BY Mary Ellen Finnegan

PATENT CENTER # 72479737

FILING DATE 01/24/2025

CUSTOMER # 139982

FIRST NAMED INVENTOR Shih-Yuan WANG

CORRESPONDENCE ADDRESS -

AUTHORIZED BY Gerard Wissing

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV2_Supp_Res p_NFOA_Mailed_18Mar2025 _Final.pdf	10	Supplemental Response or Supplemental Amendment	249 KB

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309-0015USCIPDIV2_Supp_Resp_NFOA_Mailed_18Mar2025_Final.pdf	D0C29B087E6234FDB3A6ED207F906320588B0B4C6DA27A0091E8B042059BCE8AA7B9C3D604ACAC2821E21C54FD123C4BFE2757184E384EC8324714925219399D

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Shih-Yuan WANG et al.
Serial No.: 19/036,506
Examiner: EDUARDO A RODELA
Group Art Unit 2893
Filing Date: 01/24/2025
For: MICROSTRUCTURE ENHANCED ABSORPTION
PHOTOSENSITIVE DEVICES
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Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, New York 10001

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(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

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Amendments to the Claims begin on page 2; and

Remarks begin on page 5.

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This listing of claims will replace all prior versions and listings of the claims in the application.

1-17. (Canceled)

18-36. (Canceled)

37. (New) A structure comprising:

an array of elongated pillars of semiconductor material in which each of at least some of the pillars has:

- (i) a respective light-receiving surface,
- (ii) respective sides,
- (iii) width of 50-2000 nm,
- (iv) height of 100-10000 nm, and
- (v) at least one photodetector of Si, Ge, and/or alloyed SiGe semiconductor material formed in the pillar;

wherein each of the photodetectors:

- (i) has P-doped and N-doped regions of the semiconductor material,
- (ii) is configured to generate electrical charge carriers in the semiconductor material of the photodetector in response to light that (a) is in the visible and infrared wavelengths, and (b) illuminates along a light direction the light-receiving surface of the pillar in which the photodetector is formed;

one or more in-pillar holes each of which:

- (i) is fabricated as a recess in each of the pillars in which at least one of the photodetectors is formed, and
- (ii) extends along the light direction into the semiconductor material of the pillar in which the in-pillar hole is fabricated;

side-isolation comprising solid dielectric material between at least portions of the sides of at least some of the pillars;
electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for selected reverse-biasing at least some of the photodetectors;
wherein the presence of the in-pillar holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors in pillars lacking said holes.

38. (New) The structure of claim 37, in which the array is monolithically integrated with Si electronic devices.

39. (New) The structure of claim 37, in which at least one of the in-pillar holes in each of at least some of the pillars is elongated in the light direction.

40. (New) The structure of claim 37, in which each of at least some of the holes is elongated in a direction along the light-receiving surface of the pillar in which the hole is fabricated.

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46. (New) The structure of claim 37, in which two or more of the photodetectors are connected electrically in parallel.

47. (New) The structure of claim 37, wherein the array of pillars is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors.

48. (New) The structure of claim 37, in which at least some of the holes extend 100 to 10000 nm in the light direction into the semiconductor material of the pillars in which the holes are formed.

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Examples of support are outlined below in the subject application and in the 2013 provisional applications that are incorporated by reference and to which priority is claimed.

FIG. 5B of the subject application illustrates an example of an array of vertical pillars of semiconductor material such as Si, and FIG. 49 illustrates an example of an in-pillar hole (pillar with hole). Both are reproduced below.

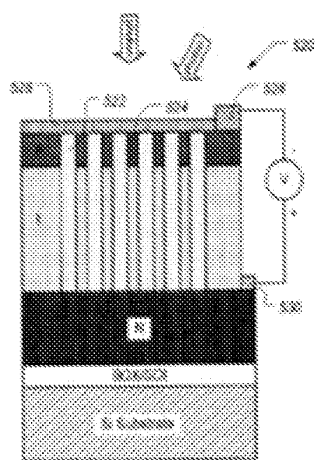


FIG. 5B

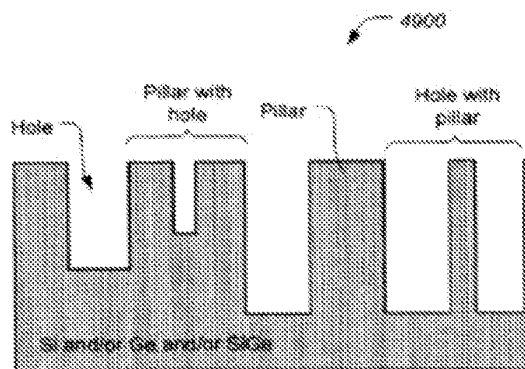


FIG. 49

As seen in FIG. 5B and explained in the text of the subject application, each pillar 524 has a light receiving surface that is on top of the pillar in this example, illuminated with light (photons) in the direction of one or both arrows, has sides, and has at least one photodetector of Si, Ge, or SiGe formed in the pillar.

The width of a pillar can be 50-2000 nm¹ and the height of a pillar can be 100-10000 nm.² Each photodetector has P-doped and N-doped regions and is configured to generate electrical charge carriers in the semiconductor material of the photodetector formed in the pillar in response to light that is in the visible and infrared wavelengths and illuminates the light-receiving surface of the pillar.

Each of the pillars in the array of FIG. 5B can be a “pillar with a hole” as in the example of FIG. 49.³ Each in-pillar hole extends into the pillar in the direction of the light, down into the pillar in this example.

Dielectric material 522 such as oxide forms solid isolation between pillar side walls and, with in-pillar holes in the pillars, fills at least a part of the holes,⁴ and the in-pillar holes can be

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² Provisional application 61/826,446 filed May 22, 2013, page 12: “[P]illars can be 100-10000 nm in length....”

³ See also provisional application 61/826,446 filed May 22, 2013, page 16; “[T]he microstructure can have both pillars and holes coexist, can be concentric (pillar within a hole or hole within a pillar or multiple concentric hole/pillar, not necessarily circular....”

⁴ See also Figure 8 in page 6 of provisional application 61/826,446 filed May 22, 2013.

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Section 103

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⁹ See also Fig. 12 in provisional application 61/834,873 filed June 13, 2013.

¹⁰ The IPRs are: (1) Case IPR2025-00993 on patent 12,087,871, (2) Case IPR2025-00994 on patent 11,621,360; (3) Case IPR2025-00995 on patent 10,468,543; (4) Case IPR2025-00996 on patent 10,446,700; and (5) Case IPR-00997 on patent 9,525,084. Applicant is concurrently submitting an IDS identifying the total of 7 references on which the 5 IPRs rely to challenge patentability under Sections 102 or 103. The PGR is Case PGR2025-00082 for patent 12,243,948.

¹¹ The action is: W&Wsens Devices Inc. v. Samsung Elecs. Co., Case No. 2:24-cv-00854-JRG (E.D. Tex.). Defendants have filed pleadings identifying purported prior art, which are available through Pacer. Applicant offers to any of the several hundred patents, published applications, and non-patent publication listed in such pleadings if the Office requests it.

The references that the IPRs and the PGR assert are:

1. **Kuboi** US 2012/0049044
2. **Shinohara** US 2012/0033119
3. **Yu** US 2012/0153124
4. **Harada** Kokai No. 2002-314116 (P2002-314116A)
5. **Hasegawa** Kokai 2007-129024 (P2007-129024A)
6. **NXP** EP 2 172 974 A1
7. **Yahaya**, NA, Characterization of light absorption in thin-film silicon with periodic nanohole arrays, 11 March 2013/Vol. 21, No. 5/OPTICS EXPRESS 5924-5930.
8. **Vasylysev** US 2012/0012741

Applicant submits that claims 18-30 differ patentably from these seven references taken individually or in combination, at least because:

Kuboi proposes a standard semiconductor PIN photodiode 53R with no in-pillar holes and additionally proposes pixels 53R, 53G that generate electrical output only in organic material 13, not in semiconductor material of a photodetector. See Kuboi FIGs. 6A and 10A.

Shinohara proposes an array of standard photodiodes with no in-pillar holes.

Yu proposes nanowires or nanopillars that also lack in-pillar holes.

Harada proposes a lateral photodiode with no pillars along the light direction and no in-pillar holes.

Hasegawa proposes standard photodiodes, lacking in-pillar holes, used in optical disc drive tracking.

NXP proposes standard photodiodes, with no in-pillar holes.

Yahaya proposes a solar cell panel with surface structures but lacks a teaching of pillars of semiconductor material that are electrically isolated from each other and have reverse-biased photodetectors fabricated in the pillars and in-pillar holes with solid dielectric material.

Vasylyev also proposes a solar cell panel with surface structures but lacks a teaching of pillars of semiconductor material that are electrically isolated from each other and have reverse-biased photodetectors fabricated in the pillars and in-pillar holes with solid dielectric material.

The Preliminary Amendment filed 01/24/2025 in the subject application addresses

references cited in application Ser. No. 18/385,213, now patent 12,243,948. They are **Yu** US 2011/0309331), **Lunev** US 2014/001660, **Counil** US 2010/0116332, and **Arimoto** US 5,759,292. Applicant submits that claims 18-30 patentably differ from these references at least for the reasons discussed in the Preliminary Amendment filed 01/24/2025 but also for additional reasons.

Applicant invites the Examiner to telephone the undersigned if the Examiner finds that it may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

/Gerard M. Wissing/

WISSING MILLER LLP
Attorney for Applicant
By: Gerard M. Wissing

Reg. No. 36,309
Tel.: 516-901-7027



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
19/036,506	09/26/2025 04:25:02 PM Z ET	309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4276	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	72481485	FILING DATE	01/24/2025
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Gerard Wissing

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV2_Supp_Res p_NFOA_Mailed_18Mar2025 _Final-APP.TEXT.docx	10	Application body structured text document	171 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV2_Supp_Res p_NFOA_Mailed_18Mar2025_Fin al-APP.TEXT.docx	5B5FFBC7C086E116175C6F26D39A34B457A5DAF5382ADD06 AA5E0D3E94B60AA7601534404AB7D97666861A2CCB6784723 A82886B74C8B5E632DB9CA0523831F8

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

139982 7590 10/27/2025
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
RODELA, EDUARDO A	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 10/27/2025

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
19/036,506	01/24/2025	Shih-Yuan WANG	309-0015USCIPDIV2	4276

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$516	\$0.00	\$0.00	\$516	01/27/2026

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

139982 7590 10/27/2025
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
19/036,506	01/24/2025	Shih-Yuan WANG	309-0015USCIPDIV2	4276

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$516	\$0.00	\$0.00	\$516	01/27/2026

EXAMINER	ART UNIT	CLASS-SUBCLASS
RODELA, EDUARDO A	2893	136-256000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/ALA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/ALA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
19/036,506	01/24/2025	Shih-Yuan WANG	309-0015USCIPDIV2	4276
139982	7590	10/27/2025	EXAMINER	
Wissing Miller LLP Industrious at Hudson Yards 31 Hudson Yards, 11th Floor New York, NY 10001			RODELA, EDUARDO A	
			ART UNIT	PAPER NUMBER
			2893	
DATE MAILED: 10/27/2025				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).

<https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf>

Routine uses of the information in this record may include disclosure to:

- 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
- 2) a federal, state, local, or international agency, in response to its request;
- 3) a contractor of the USPTO having need for the information in order to perform a contract;
- 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
- 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
- 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
- 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
- 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
- 9) the Office of Personnel Management (OPM) for personnel research purposes; and
- 10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Notice of Allowability	Application No. 19/036,506	Applicant(s) WANG et al.	
	Examiner Eduardo A Rodela	Art Unit 2893	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 9/26/2025.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 37-49. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____	7. ☐ Other _____
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date <u>9/26/2025</u> .	

	/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893
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DETAILED ACTION

This correspondence is in response to the communications received September 26, 2025.

Claims 37-49 are pending.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority

In light of Applicant's clarification regarding priority in the remarks dated September 26, 2025, Examiner agrees with Applicant's assessment of priority.

Claim Rejections - 35 USC § 112

The 112a rejections to (previous) claims 18 and 32 have been withdrawn in light of the remarks provided on September 26, 2025.

REASONS FOR ALLOWANCE

Claims 37-49 are allowed.

The following is an Examiner's statement of reasons for allowance: The pillar shaped light photodiode array as recited in the claims of the instant invention fail to be taught by the prior art cited of interest.

Regarding claim 37, the prior art discloses pillar shaped light photodiode array, but fails to disclose the specific characteristic recited in the claims of the instant invention e.g. the combination of claimed features of the specified semiconductor material based pillars with n and p doped regions, holes in the light entry surface, side isolation, electrical contacts, in conjunction with the limitations of,

“including for selected reverse-biasing at least some of the photodetectors;

...

wherein the presence of the in-pillar holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors in pillars lacking said holes.”

A prior art rejection in view of Dutta (US 8,357,960) in view of Hsu et al. (US 2008/0083963) in view of Dutta (US 8,106,289), was attempted, however, several of the claim limitations were not able to be addressed by the prior art.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A Rodela whose telephone number is (571)272-8797.

The examiner can normally be reached M-F, 8:30-5:00pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yara B Green can be reached on (571) 270-3035. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: <https://patentcenter.uspto.gov>. Visit <https://www.uspto.gov/patents/apply/patent-center> for more information about Patent Center and <https://www.uspto.gov/patents/docx> for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDUARDO A RODELA/
Primary Examiner, Art Unit 2893

<i>Examiner-Initiated Interview Summary</i>	Application No. 19/036,506	Applicant(s) WANG et al.		
	Examiner Eduardo A Rodela	Art Unit 2893	AIA (First Inventor to File) Status Yes	Page 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	Title	Type
Eduardo A Rodela	Primary Examiner	Telephonic
Gerard M. Wissing	Attorney	
Ivan Kavrukov	Attorney	

Date of Interview: 26 September 2025

Issues Discussed:

35 U.S.C. 112

Applicant's Representatives further clarified the support for the claim content which was identified in the previous 112a written description rejection to claims 18 and 32.

Other

Applicant's Representatives explained the purpose of presenting the information and prior art references in the discussion around the section of remarks titled, "IPRs and PGR regarding commonly assigned patents".

		/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893
<p>Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04</p> <p>Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing</p>		

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

<i>Notice of References Cited</i>	Application/Control No. 19/036,506		Applicant(s)/Patent Under Reexamination WANG et al.	
	Examiner Eduardo A Rodela		Art Unit 2893	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Name	CPC Classification	US Classification
*	A	US-8357960-B1	2013-01-22	Dutta; Achyut Kumar	B82Y20/00	257/292
*	B	US-20080083963-A1	2008-04-10	Hsu; Louis Lu-Chen	H10F77/147	257/431
*	C	US-8106289-B2	2012-01-31	Dutta; Achyut Kumar	H10F77/148	136/258
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title, Date, Publisher, Edition or Volume, Pertinent Pages
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in YYYY-MM-DD format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 19/036,506	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

CPC - Searched*		
Symbol	Date	Examiner
(H10F39/014,024,8027,806,8067; H10F71/121,1212,1215; H10F77/14,147,40,413,488,70,703; H10F77/703; H10F30/223; H10F77/122; H10F77/1226; H10F77/14; H10F77/1437; H10F77/147; H10F77/413	10/02/2025	EAR
H10F77/122,143,1437,147,70,703,413	10/02/2025	EAR

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E search - see history for complete details	10/02/2025	EAR
Inventor & Applicant search	10/02/2025	EAR
Similarity search	10/02/2025	EAR

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
noted CPC search area	in conjunction with a text limited search	10/02/2025	EAR

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Issue Classification 	Application/Control No. 19/036,506	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

CPC						
Symbol					Type	Version
H10F	/	77	/	703	F	2025-01-01
H10F	/	77	/	14	I	2025-01-01
H10F	/	30	/	223	I	2025-01-01
H10F	/	77	/	122	I	2025-01-01
H10F	/	77	/	147	I	2025-01-01
H10F	/	77	/	413	I	2025-01-01
H10F	/	77	/	1226	I	2025-01-01
H10F	/	77	/	1437	I	2025-01-01

CPC Combination Sets					
Symbol				Type	Set
	/		/		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	13	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	02 October 2025	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	37	5B, 49

U.S. Patent and Trademark Office

Part of Paper No.: 20250926

Issue Classification 	Application/Control No. 19/036,506	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H10F	/	77	/ 1437
H10F	/	77	/ 122
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	13	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	02 October 2025	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	37	5B, 49

U.S. Patent and Trademark Office

Part of Paper No.: 20250926

Issue Classification 	Application/Control No. 19/036,506	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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	4		13		22		31	4	40	13	49				
	5		14		23		32	5	41						
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	7		16		25		34	7	43						
	8		17		26		35	8	44						
	9		18		27		36	9	45						

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 13	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893 (Primary Examiner) _____ (Date) 02 October 2025		O.G. Print Claim(s) 37	O.G. Print Figure 5B, 49

U.S. Patent and Trademark Office

Part of Paper No.: 20250926

Doc code: IDS

PTO/SB/08 (01-25)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 11/30/2027. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	19036506
	Filing Date	2025-01-24
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0015USCIPDIV2

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Inventor of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1							
If you wish to add additional U.S. Patent citation information, please click the Add button.							Add	
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Inventor or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	20120049044		2012-03-01	Kuboi			
	2	20120033119		2012-02-09	Shinohara			
	3	20120153124		2012-06-21	Yu et al.			
	4	20120012741		2012-01-19	Vasylyev			
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	19036506
	Filing Date	2025-01-24
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0015USCIPDIV2

	1	2002314116	JP		2002-10-25	Harada et al.		☐
	2	2007129024	JP		2007-05-24	Hasegawa		☐
	3	2172974	EP		2010-04-07	NXP B.V.		☐

If you wish to add additional Foreign Patent Document citation information, please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Yahaya, NA, Characterization of light absorption in thin-film silicon with periodic nanohole arrays, 11 March 2013/Vol. 21, No. 5/OPTICS EXPRESS 5924-5930. (7 pages)	☐

If you wish to add additional non-patent literature document citation information, please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/EDUARDO A. RODELA/	Date Considered	09/29/2025
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*EXAMINER: Initial if reference considered and whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	19036506
	Filing Date	2025-01-24
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0015USCIPDIV2

TIMING STATEMENT

Please see 37 CFR 1.97(e) to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached timing statement under 37 CFR 1.97(e).

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TIMING FEE

☒ The fee set forth in 37 CFR 1.17(p) has been submitted herewith.

COPIES

☒ An identification of an earlier application pursuant to 37 CFR 1.98(d)(1) is attached.

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Please see 37 CFR 1.17(v) and the [IDS Auto-Load Instructions](#) for completing this form to make the appropriate selection of an assertion under 37 CFR 1.98. For the information disclosure statement (IDS) submitted herewith, the applicant or patent owner certifies the following with respect to the cumulative number of applicant-provided or patent-owner provided items of information submitted to date including those in the accompanying IDS (select only one):

☒ No IDS size fee is required under 37 CFR 1.17(v) at this time.

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SIGNATURE

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Gerard M. Wissing/	Date (YYYY-MM-DD)	2025-09-16
Name/Print	Gerard M. Wissing	Registration Number	36,309

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	19036506
	Filing Date	2025-01-24
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0015USCIPDIV2

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L34	36	((US-11347001-B2 OR US-9425126-B2 OR US-8147704-B2 OR US-9105867-B2 OR US-8778195-B2 OR US-8453319-B2 OR US-10739189-B2 OR US-11037794-B2 OR US-8501020-B2 OR US-7046441-B2 OR US-12174398-B2 OR US-9406824-B2 OR US-8344241-B1 OR US-8814622-B1 OR US-8357960-B1 OR US-11211419-B2 OR US-11830594-B2 OR US-11830954-B2 OR US-9331116-B2).did. AND USPT.dbnm.) OR ((US-20110036396-A1 OR US-20100203235-A1 OR US-20080067721-A1 OR US-20070049028-A1 OR US-20240339475-A1 OR US-20240304641-A1 OR US-20240276114-A1 OR US-20230238468-A1 OR US-20100221866-A1 OR US-20170133415-A1 OR US-20180359434-A1 OR US-20180182806-A1 OR US-20200135776-A1 OR US-20100271524-A1 OR US-20140167066-A1).did. AND PGPB.dbnm.) OR ((CN-116110986-A OR CN-110518093-A).did. AND FTDB.dbnm.)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/23 10:44 AM
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L47	2	"9252177".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 03:43 PM
L48	3	("20050213221" "20090040345" "20110037869").pn. OR ("9252177").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 03:43 PM
L49	60336	(micrometer OR micro OR (micro NEAR structur\$3)) WITH (pillars OR columns) WITH (plurality OR matrix OR array)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 04:04 PM
L50	15285465	silicon OR "SiGe" OR (silicon NEAR germanium) OR germanium	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 04:04 PM
L51	102189812	recess\$2 OR hole OR aperture OR orifice OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2025/09/29 04:04 PM

		opening OR pit OR hollow	AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L52	3873614	(dielectric OR oxide OR nitride OR glass OR insulat\$3) near3 (fill\$3 OR lin\$3)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 04:04 PM
L53	460	(L1 same3 L3 SAME L4) AND L2	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 04:04 PM
L54	159	(L1 same3 L3 SAME L4) AND L2	(US-PGPUB; USPAT)	OR	ON	ON	2025/09/29 04:04 PM
L55	49	("4983251" "6316793" "6486502" "6583454" "6682659" "8147704" "8608468" "8993380" "9000584" "9048222" "9048233" "9064879" "9111949" "9209068" "9263511" "9281254"	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM

		"9299649" "9368460" "9372206" "9425126" "9431368" "9443783" "9461018" "9484482" "9496189" "9564414" "9666502" "9735131" "9899355" "10366962" "20010017370" "20030201459" "20090154871" "20100216294" "20110008484" "20110036396" "20120156321" "20130279844" "20150037044" "20150194337" "20150378095" "20160190093" "20160315452" "20170092626" "20170207600" "20180308834" "20190004247").pn. OR ("11347001").urpn. AND (PGPB USPT USOC).dbnm.					
L56	15	("7189635" "20020133129" "20070049028" "20080061214" "20080067721" "20080217819" "20100203235").pn. OR ("8147704").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L57	13	("2010/0203235").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L58	7	("2007/0049028").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L59	41067	H10F39/014,024,8027, 806,8067.cpc. OR H10F71/121,1212,1215 .cpc. OR H10F77/14,147,40,413, 488,70,703.cpc.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L60	17	H10F77/703.cpc. AND L1 AND L3	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L61	39	H10F77/703.cpc. AND L1 AND L3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU,	OR	ON	ON	2025/09/29 04:04 PM

			CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L62	418	L12 AND L1 AND L3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 04:04 PM
L63	138	L12 AND L1 AND L3	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L64	0	("2023/0238468").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L65	194	("4358851" "4634272" "4676599" "4702600" "4744667" "4851664" "5267016" "5288992" "5760899" "5982552" "6014232" "6133989" "6255133" "6374024" "6414746" "6690019" "6721262" "7091462" "D531525" "7170542" "7295298" "7345271" "7421159" "7433042" "7808706" "7848478" "7969558" "8013983" "8089618" "8130367" "D659030" "8319949" "8330840" "8374405" "8384997" "8494252" "8675181" "8717488" "8742325" "8743176" "8761495" "8767190" "8829406" "8836922" "8848039" "9041915"	OR	ON	ON	2025/09/29 04:04 PM	

		"9063549" "9071763" "9086273" "9111444" "9157790" "9164511" "9176051" "9229109" "9285464" "9285477" "9299731" "9368936" "9369689" "9383753" "9425654" "9435891" "9470520" "9489601" "9525863" "9529079" "9551791" "9992477" "10063849" "10183541" "10222458" "10222475" "20020072684" "20030006676" "20030047752" "20040061502" "20040223071" "20050030409" "20060244851" "20070007563" "20070060806" "20070228262" "20080153189" "20090016642" "20090040629" "20090179142" "20090295910" "20100008588" "20100020306" "20100110275" "20100123893" "20100204964" "20110025843" "20110032398" "20110037849" "20110116262" "20110216304" "20120044476" "20120140109" "20120154914" "20120182464" "20120287417" "20120320164" "20130044310" "20130141549" "20130206967" "20130294089" "20130300840" "20140118335" "20140118493" "20140153001" "20140158900" "20140168631" "20140176933" "20140211194"				
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		"20140285628"					
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		"20140313519"					
		"20140375977"					
		"20140376092"					
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		"20150293224"					
		"20150316473"					
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		"20160047901"					
		"20160047903"					
		"20160049765"					
		"20160097858"					
		"20160150963"					
		"20160161600"					
		"20160218727"					
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		"20170269209"					
		"20170269215"					
		"20170289524"					
		"20170350983"					
		"20180059222"					
		"20180067209"					
		"20180069838"					
		"20180136042"					
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		"20180329060"					
		"20180329061"					
		"20180329062"					
		"20180329066"					
		"20180359460"					
		"20190011556"					

L66	7	"20190011561" "20190011562" "20190011567" "20190018111" "20190146088" "20190064355").pn. OR ("10739189").urpn. AND (PGPB USPT USOC).dbnm. ("4407695" "6835317" "8501020" "9675790" "9993948" "20080047929" "20170110330").pn. OR ("11037794").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L67	19	("4407695" "7046441" "7483130" "7700520" "20060002656" "20060228722" "20070177647" "20070184204" "20070284570" "20080047929" "20100087723" "20100221866" "20100244079" "20110195201" "20120152353" "20120170033").pn. OR ("8501020").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L68	19	("4117506" "4403239" "5211761" "8344241" "20010013362" "20020011263" "20020192441" "20040084080" "20040109666" "20050098205" "20050121068" "20060118166" "20060207647" "20090194152" "20090283139" "20100096013" "20100186802" "20110162706" "20130048070").pn. OR ("9406824").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L69	69978	(H10F77/703 OR H10F30/223 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2025/09/29 04:04 PM

		H10F77/122 OR H10F77/1226 OR H10F77/14 OR H10F77/1437 OR H10F77/147 OR H10F77/413).cpc.	AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L70	43660	L12 OR L22	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L71	139	L23 AND L1 AND L3	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L72	32	("4814847" "5266814" "6667528" "7015139" "7132677" "7183127" "20050255581" "20070158661" "20070210349" "20080105296").pn. OR ("8357960").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L73	5	((("W&W") near3 ("SENS") near3 ("DEVICES") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT)	OR	ON	ON	2025/09/29 04:04 PM
L74	869	((("WANG") near3 ("Shih-Yuan")) OR (("WANG") near3 ("Shih-Ping"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2025/09/29 04:04 PM
L75	2	(L26 OR L27) AND ((pillars)(photodetectors)light NEAR receiving NEAR surfac\$2)(light)(respond)visible OR infrared)(wavelength\$1 (holes)(recess\$3)(filled) (dielectric NEAR material)(absorption)).cl m.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2025/09/29 04:04 PM
L76	40	("5315147" "5759292" "6879014" "7276749" "7396696" "7525170"	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2025/09/29 04:04 PM

		"8129710" "8357960" "8558336" "8946675" "9000492" "9184202" "9263519" "9515218" "10411053" "10522582" "11211419" "11309444" "11728457" "20050145779" "20080083963" "20100320444" "20110156195" "20110297214" "20110309331" "20120012741" "20120153127" "20120153416" "20120196401" "20130125965" "20140016660" "20160240579" "20170141153" "20180012918" "20180102442" "20180182806" "20190001989" "20190166317" "20200006407" "20200006416").pn. OR ("12243948").urpn. AND (PGPB USPT USOC).dbnm.					
L77	10	("20150372034" "20160112614" "20170104020" "20170117309" "20180151759" "20180182806" "20180359434").pn. OR ("11211419").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2025/09/29 04:04 PM
L78	1	"11830594".pn.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2025/09/29 04:04 PM
L79	1	"11830954".pn.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2025/09/29 04:04 PM
L80	9	("9209320" "9331116" "9876045" "11594657" "20100271524" "20140167066" "20180033895" "20200135776" "20210305440").pn. OR ("11830954").urpn.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2025/09/29 04:04 PM

L81	36	AND (PGPB USPT USOC).dbnm. ((US-11347001-B2 OR US-9425126-B2 OR US-8147704-B2 OR US-9105867-B2 OR US-8778195-B2 OR US-8453319-B2 OR US-10739189-B2 OR US-11037794-B2 OR US-8501020-B2 OR US-7046441-B2 OR US-12174398-B2 OR US-9406824-B2 OR US-8344241-B1 OR US-8814622-B1 OR US-8357960-B1 OR US-11211419-B2 OR US-11830594-B2 OR US-11830954-B2 OR US-9331116-B2).did. AND USPT.dbnm.) OR ((US-20110036396-A1 OR US-20100203235- A1 OR US- 20080067721-A1 OR US-20070049028-A1 OR US-20240339475- A1 OR US- 20240304641-A1 OR US-20240276114-A1 OR US-20230238468- A1 OR US- 20100221866-A1 OR US-20170133415-A1 OR US-20180359434- A1 OR US- 20180182806-A1 OR US-20200135776-A1 OR US-20100271524- A1 OR US- 20140167066-A1).did. AND PGPB.dbnm.) OR ((CN-116110986-A OR CN-110518093-A).did. AND FTDB.dbnm.)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 04:04 PM
L82	34	((US-11347001-B2 OR US-9425126-B2 OR US-8147704-B2 OR US-9105867-B2 OR US-8778195-B2 OR US-8453319-B2 OR US-10739189-B2 OR US-11037794-B2 OR US-8501020-B2 OR US-7046441-B2 OR US-12174398-B2 OR	(US-PGPUB; USPAT)	OR	ON	ON	2025/09/29 04:04 PM

L83	36	US-9406824-B2 OR US-8344241-B1 OR US-8814622-B1 OR US-8357960-B1 OR US-11211419-B2 OR US-11830594-B2 OR US-11830954-B2 OR US-9331116-B2).did. AND USPT.dbnm.) OR ((US-20110036396-A1 OR US-20100203235- A1 OR US- 20080067721-A1 OR US-20070049028-A1 OR US-20240339475- A1 OR US- 20240304641-A1 OR US-20240276114-A1 OR US-20230238468- A1 OR US- 20100221866-A1 OR US-20170133415-A1 OR US-20180359434- A1 OR US- 20180182806-A1 OR US-20200135776-A1 OR US-20100271524- A1 OR US- 20140167066-A1).did. AND PGPB.dbnm.) OR ((CN-116110986-A OR CN-110518093-A).did. AND FTDB.dbnm.) ((US-11347001-B2 OR US-9425126-B2 OR US-8147704-B2 OR US-9105867-B2 OR US-8778195-B2 OR US-8453319-B2 OR US-10739189-B2 OR US-11037794-B2 OR US-8501020-B2 OR US-7046441-B2 OR US-12174398-B2 OR US-9406824-B2 OR US-8344241-B1 OR US-8814622-B1 OR US-8357960-B1 OR US-11211419-B2 OR US-11830594-B2 OR US-11830954-B2 OR US-9331116-B2).did. AND USPT.dbnm.) OR ((US-20110036396-A1 OR US-20100203235- A1 OR US- 20080067721-A1 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 04:04 PM
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L84	36	US-20070049028-A1 OR US-20240339475-A1 OR US-20240304641-A1 OR US-20240276114-A1 OR US-20230238468-A1 OR US-20100221866-A1 OR US-20170133415-A1 OR US-20180359434-A1 OR US-20180182806-A1 OR US-20200135776-A1 OR US-20100271524-A1 OR US-20140167066-A1).did. AND PGPB.dbnm.) OR ((CN-116110986-A OR CN-110518093-A).did. AND FTDB.dbnm.) ((US-11347001-B2 OR US-9425126-B2 OR US-8147704-B2 OR US-9105867-B2 OR US-8778195-B2 OR US-8453319-B2 OR US-10739189-B2 OR US-11037794-B2 OR US-8501020-B2 OR US-7046441-B2 OR US-12174398-B2 OR US-9406824-B2 OR US-8344241-B1 OR US-8814622-B1 OR US-8357960-B1 OR US-11211419-B2 OR US-11830594-B2 OR US-11830954-B2 OR US-93311116-B2).did. AND USPT.dbnm.) OR ((US-20110036396-A1 OR US-20100203235-A1 OR US-20080067721-A1 OR US-20070049028-A1 OR US-20240339475-A1 OR US-20240304641-A1 OR US-20240276114-A1 OR US-20230238468-A1 OR US-20100221866-A1 OR US-20170133415-A1 OR US-20180359434-A1 OR US-20180182806-A1 OR US-20200135776-A1	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 04:04 PM
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L85	9	OR US-20100271524-A1 OR US-20140167066-A1).did. AND PGPB.dbnm.) OR ((CN-116110986-A OR CN-110518093-A).did. AND FTDB.dbnm.) "10050078".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 04:04 PM
L86	37	("9853073" "20100276572" "20130181114" "20140021574" "20140146208" "20150171146" "20160054172" "8941200" "8946610" "8970751" "9313433" "9577012").P N.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 04:04 PM
L87	13	("6882364" "7110034" "8208052" "8289422" "8294076" "8384818" "20020135825" "20100019129" "20120212656" "20140055649").pn. OR ("9853073").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L88	2	("20130182155").pn. OR ("8970751").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L89	2	"9252177".pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY,	OR	ON	ON	2025/09/29 04:04 PM

			CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L90	3	("20050213221" "20090040345" "20110037869").pn. OR ("9252177").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/09/29 04:04 PM
L91	17	((("W&WSens") near3 ("Devices") near3 ("Inc"))).AS,AANM.	(US-PGPUB; USPAT)	OR	ON	ON	2025/09/29 05:04 PM
L92	869	((("WANG") near3 ("Shih-Yuan")) OR ((("WANG") near3 ("Shih-Ping"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2025/09/29 05:15 PM
L93	50	(Artificial Intelligence) Similar to: 19/036,506 with 0 CPC Selections and 0 Text Selections Text: (US-20250194293-A1 OR US-12087871-B2 OR US-12243948-B2 OR US-20240429332-A1 OR KR-20220164070-A OR KR-20220019844-A OR US-11621360-B2 OR KR-102472078-B1 OR KR-102593511-B1 OR US-20240063317-A1 OR KR-20160039150-A OR US-20190019899-A1 OR US-10700225-B2 OR EP-3000134-B1 OR US-9559240-B1 OR US-11309444-B1 OR KR-102358584-B1 OR WO-2019018846-A2 OR US-20220246775-A1 OR WO-2014190189-A9 OR US-20230215962-A1 OR US-20160254407-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN))	OR	ON	ON	2025/09/29 05:15 PM

L94	59241	A1 OR US- 20160126381-A1 OR KR-20180060969-A OR WO-2014190189-A2 OR US-9496435-B2 OR US-10622498-B2 OR CN-116454144-A OR US-11791432-B2 OR CN-111133590-B OR US-20180151759-A1 OR DE-102017123338- B4 OR JP-7429084-B2 OR KR-102162408-B1 OR KR-20080028385-A OR US-20220102563- A1 OR US- 20200020816-A1 OR EP-3772104-A1 OR US-20130125965-A1 OR US-20160258867- A1 OR US-9909989-B2 OR US-10707361-B2 OR US-9182338-B2 OR US-20140329352-A1 OR US-8890271-B2 OR US-20140045209-A1 OR US-11393937-B2 OR US-20170263790- A1 OR CN-111133590- A OR US-9406824- B2).did. H10F77/122,143,1437, 147,70,703,413.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 05:19 PM
L95	93510	(H10F77/703 OR H10F30/223 OR H10F77/122 OR H10F77/1226 OR H10F77/14 OR H10F77/1437 OR H10F77/147 OR H10F77/413 OR H10F30/221 OR H10F30/225 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO,	OR	ON	ON	2025/09/29 05:23 PM

L96	3	H10F77/40 OR H10F77/407).cpc. (L94 OR L95) AND ((pillars)(photodetectors) (light NEAR receiving NEAR surfac\$2)(light)(respond) (visible OR infrared)(wavelength\$1) (holes)(recess\$3)(filled) (dielectric NEAR material)(absorption))	NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2025/09/29 05:25 PM
L97	199	(L94 OR L95) AND L1 AND L3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/09/29 05:26 PM
L98	40	((US-11347001-B2 OR US-9425126-B2 OR US-8147704-B2 OR US-9105867-B2 OR US-8778195-B2 OR US-8453319-B2 OR US-10739189-B2 OR US-11037794-B2 OR US-8501020-B2 OR US-7046441-B2 OR US-12174398-B2 OR US-9406824-B2 OR US-8344241-B1 OR US-8814622-B1 OR US-8357960-B1 OR US-11211419-B2 OR US-11830594-B2 OR US-11830954-B2 OR US-9331116-B2 OR	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/10/01 03:51 PM

L99	38	US-9853073-B2 OR US-8970751-B2 OR US-9252177-B2).did. AND USPT.dbnm.) OR ((US-20110036396-A1 OR US-20100203235- A1 OR US- 20080067721-A1 OR US-20070049028-A1 OR US-20240339475- A1 OR US- 20240304641-A1 OR US-20240276114-A1 OR US-20230238468- A1 OR US- 20100221866-A1 OR US-20170133415-A1 OR US-20180359434- A1 OR US- 20180182806-A1 OR US-20200135776-A1 OR US-20100271524- A1 OR US- 20140167066-A1 OR US-20130182155- A1).did. AND PGPB.dbnm.) OR ((CN- 116110986-A OR CN- 110518093-A).did. AND FTDB.dbnm.) ((US-11347001-B2 OR US-9425126-B2 OR US-8147704-B2 OR US-9105867-B2 OR US-8778195-B2 OR US-8453319-B2 OR US-10739189-B2 OR US-11037794-B2 OR US-8501020-B2 OR US-7046441-B2 OR US-12174398-B2 OR US-9406824-B2 OR US-8344241-B1 OR US-8814622-B1 OR US-8357960-B1 OR US-11211419-B2 OR US-11830594-B2 OR US-11830954-B2 OR US-9331116-B2 OR US-9853073-B2 OR US-8970751-B2 OR US-9252177-B2).did. AND USPT.dbnm.) OR ((US-20110036396-A1 OR US-20100203235- A1 OR US- 20080067721-A1 OR	(US-PGPUB; USPAT)	OR	ON	ON	2025/10/01 03:51 PM
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L100	40	US-20070049028-A1 OR US-20240339475-A1 OR US-20240304641-A1 OR US-20240276114-A1 OR US-20230238468-A1 OR US-20100221866-A1 OR US-20170133415-A1 OR US-20180359434-A1 OR US-20180182806-A1 OR US-20200135776-A1 OR US-20100271524-A1 OR US-20140167066-A1 OR US-20130182155-A1).did. AND PGPB.dbnm.) OR ((CN-116110986-A OR CN-110518093-A).did. AND FTDB.dbnm.) ((US-11347001-B2 OR US-9425126-B2 OR US-8147704-B2 OR US-9105867-B2 OR US-8778195-B2 OR US-8453319-B2 OR US-10739189-B2 OR US-11037794-B2 OR US-8501020-B2 OR US-7046441-B2 OR US-12174398-B2 OR US-9406824-B2 OR US-8344241-B1 OR US-8814622-B1 OR US-8357960-B1 OR US-11211419-B2 OR US-11830594-B2 OR US-11830954-B2 OR US-9331116-B2 OR US-9853073-B2 OR US-8970751-B2 OR US-9252177-B2).did. AND USPT.dbnm.) OR ((US-20110036396-A1 OR US-20100203235-A1 OR US-20080067721-A1 OR US-20070049028-A1 OR US-20240339475-A1 OR US-20240304641-A1 OR US-20240276114-A1 OR US-20230238468-A1 OR US-20100221866-A1 OR	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/10/02 09:09 AM
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L101	38	US-20170133415-A1 OR US-20180359434-A1 OR US-20180182806-A1 OR US-20200135776-A1 OR US-20100271524-A1 OR US-20140167066-A1 OR US-20130182155-A1).did. AND PGPB.dbnm.) OR ((CN-116110986-A OR CN-110518093-A).did. AND FTDB.dbnm.) ((US-11347001-B2 OR US-9425126-B2 OR US-8147704-B2 OR US-9105867-B2 OR US-8778195-B2 OR US-8453319-B2 OR US-10739189-B2 OR US-11037794-B2 OR US-8501020-B2 OR US-7046441-B2 OR US-12174398-B2 OR US-9406824-B2 OR US-8344241-B1 OR US-8814622-B1 OR US-8357960-B1 OR US-11211419-B2 OR US-11830594-B2 OR US-11830954-B2 OR US-9331116-B2 OR US-9853073-B2 OR US-8970751-B2 OR US-9252177-B2).did. AND USPT.dbnm.) OR ((US-20110036396-A1 OR US-20100203235-A1 OR US-20080067721-A1 OR US-20070049028-A1 OR US-20240339475-A1 OR US-20240304641-A1 OR US-20240276114-A1 OR US-20230238468-A1 OR US-20100221866-A1 OR US-20170133415-A1 OR US-20180359434-A1 OR US-20180182806-A1 OR US-20200135776-A1 OR US-20100271524-A1 OR US-20140167066-A1 OR	(US-PGPUB; USPAT)	OR	ON	ON	2025/10/02 09:09 AM
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L102	35	US-20130182155-A1).did. AND PGPB.dbnm.) OR ((CN-116110986-A OR CN-110518093-A).did. AND FTDB.dbnm.) (nm OR nanometer\$1 OR "um" OR "mu" OR micrometer\$1 OR micron\$1) AND L101	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/10/02 09:16 AM
L103	5	(silicon WITH pillar) AND L101	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/10/02 01:37 PM
L104	92	(silicon WITH pillar) AND H10F77/1437.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/10/02 01:41 PM
L105	47	(silicon WITH pillar) AND H10F77/1437.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2025/10/02 01:41 PM

L106	72	(silicon WITH pillar) AND H10F77/147.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2025/10/02 01:54 PM
L107	1	"9252177".pn.	(US-PGPUB; USPAT)	OR	ON	ON	2025/10/02 02:53 PM
L108	3	("20050213221" "20090040345" "20110037869").pn. OR ("9252177").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/10/02 02:59 PM
L109	261	((divot OR dent of hole OR groove OR texture OR (inverted NEAR pyramid)) WITH ((top OR upper OR upward) NEAR (face OR surface))) AND H10F77/147,1437.cpc.	(US-PGPUB; USPAT)	OR	ON	ON	2025/10/02 03:00 PM
L110	71	("2009/0165844").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/10/02 03:11 PM
L111	1	"11830954".pn.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/10/02 03:19 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	2	(L26 OR L27) AND ((pillars)(photodetectors) (light NEAR receiving NEAR surfac\$2)(light)(respond) (visible OR infrared)(wavelength\$1 (holes)(recess\$3)(filled) (dielectric NEAR material)(absorption)).cl m.	(US-PGPUB; USPAT)	AND	ON	ON	2025/09/29 05:24 PM
N2	2	(L94 OR L95) AND ((pillars)(photodetectors) (light NEAR receiving NEAR surfac\$2)(light)(respond) (visible OR infrared)(wavelength\$1 (holes)(recess\$3)(filled) (dielectric NEAR material)(absorption))	(US-PGPUB; USPAT)	AND	ON	ON	2025/09/29 05:25 PM
N3	2	(L91 OR L92) AND ((pillars)(photodetectors) (light NEAR receiving NEAR surfac\$2)(light)(respond) (visible OR	(US-PGPUB; USPAT)	AND	ON	ON	2025/10/02 03:45 PM

		infrared)(wavelength\$1) (holes)(recess\$3)(filled) (dielectric NEAR material)(absorption)).cl m.					
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Bibliographic Data

Application No: 19/036,506

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☐ No ☐ Met After Allowance

Verified and Acknowledged: /EDUARDO A RODELA/

Examiner's Signature

Initials

Title:

MICROSTRUCTURE ENHANCED ABSORPTION
PHOTOSENSITIVE DEVICES

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
01/24/2025	136	2893	309-0015USCIPDIV2
RULE			

APPLICANTS

W&WSens Devices, Inc, Los Altos, CA, UNITED STATES

INVENTORS

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Shih-Ping Wang, Los Altos, CA, UNITED STATES

CONTINUING DATA

This application is a DIV of 18822880 09/03/2024 PAT 12243948

18822880 is a DIV of 18385213 10/30/2023 PAT 12087871

18385213 is a CIP of 18113474 02/23/2023

18385213 is a CIP of 17974325 10/26/2022 PAT 11830954

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

02/28/2025

** SMALL ENTITY **

STATE OR COUNTRY

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New York, NY 10001

UNITED STATES

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
19/036,506	01/24/2025	2893	1082	309-0015USCIPDIV2	19	2

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

CONFIRMATION NO. 4276
CORRECTED FILING RECEIPT



0000000097290423

Date Mailed: 11/12/2025

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping Wang, Los Altos, CA;

Applicant(s)

W&WSens Devices, Inc., Los Altos, CA;

Power of Attorney: The patent practitioners associated with Customer Number 139982

Domestic Applications for which benefit is claimed

This application is a DIV of 18/822,880 09/03/2024 PAT 12,243,948
which is a DIV of 18/385,213 10/30/2023 PAT 12,087,871
which is a CIP of 17/974,325 10/26/2022 PAT 11,830,954
and is a CIP of 18/113,474 02/23/2023

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - **None**.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/28/2025

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 19/036,506**

Projected Publication Date: Not Applicable.

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Preliminary Class

136

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

page 2 of 4

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

Doc Code: PET.OP

Document Description: Petition for Review by the Office of Petitions

PTO/SB/445 (01-25)

Approved for use through 11/30/2027. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C. 119(e) (37 CFR 1.78(c)) AND/OR TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C. 120, 121, 365(c), or 386(c) (37 CFR 1.78(e)) FOR THE BENEFIT OF A PRIOR-FILED APPLICATION

Page 1 of 5

First named inventor: Shih-Yuan WANG
Application No.: 19/036,506 Art Unit: 2893
Filed: January 24, 2025 Examiner: Eduardo A. Rodela
Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX 571-273-8300

When filing via USPTO patent electronic filing system, use Doc Code PET.PCT (Petition for review by the PCT Legal Office) for applications filed under 35 U.S.C. 371 and/or if the reference to the prior-filed application(s) includes an international application or an international design application. In all other instances, use Doc Code PET.OP (Petition for review by the Office of Petitions).

NOTE: If information or assistance is needed in completing this form, please contact the Office of Petitions at 571-272-3282.

APPLICANT HEREBY PETITIONS FOR ACCEPTANCE OF AN UNINTENTIONALLY DELAYED BENEFIT CLAIM TO A PRIOR-FILED APPLICATION UNDER 37 CFR 1.78(c) AND/OR 37 CFR 1.78(e).

NOTE: For a petition under 37 CFR 1.78(e), the above-identified application must have been filed during the pendency of the prior application or during the pendency of an intermediate application similarly entitled to the benefit of the filing date of the prior application. For a petition under 37 CFR 1.78(c), the above-identified application must have been filed within 12 months of the filing date of the provisional application or be entitled to claim the benefit under 35 U.S.C. 120, 121, or 365(c) of an application that was filed within 12 months of the filing date of the provisional application, except as provided in 37 CFR 1.78(b).

NOTE: A grantable petition requires the following items:

- (1) the reference required by 35 U.S.C. 119(e) and 37 CFR 1.78(a)(3) to the prior-filed provisional application and/or the reference required by 35 U.S.C. 120 and 37 CFR 1.78(d)(2) to the prior-filed nonprovisional application, international application designating the United States, or international design application designating the United States, unless previously submitted;
- (2) the petition fee set forth in 37 CFR 1.17(m) and the applicable fee (if any) set forth in 37 CFR 1.17(w); and
- (3) a statement that the entire delay between the date the benefit claim was due under 37 CFR 1.78(d)(3) and/or 37 CFR 1.78(a)(4) and the date the benefit claim was filed was unintentional. The Director may require additional information where there is a question as to whether the delay was unintentional.

1. The required reference to the prior-filed application:

- ☒ The above-identified application was filed on or after September 16, 2012, and the reference is either set forth in the attached corrected application data sheet (ADS) or in a corrected ADS that was previously submitted.
- ☐ The above-identified application was filed prior to September 16, 2012, and the reference is either (1) set forth in a supplemental ADS, (2) set forth in the attached amendment to the first sentence(s) of the specification, or (3) set forth in a supplemental ADS or amendment to the first sentence(s) of the specification that was previously submitted. See 37 CFR 1.78(h).

Reminder: Any ADS which corrects or updates the information of record must comply with 37 CFR 1.76(c)(2) (or for applications filed prior to September 16, 2012, pre-AIA 37 CFR 1.76(c)).

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0032. Public burden for this form is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**PETITION TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C. 119(e)
(37 CFR 1.78(c)) AND/OR TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C.
120, 121, 365(c), or 386(c) (37 CFR 1.78(e)) FOR THE BENEFIT OF A PRIOR-FILED APPLICATION**

Page 2 of 5

2. Petition fee:

(A) For delay greater than two years:

37 CFR 1.17(m)(1)

- ☐ Other than a small or micro entity (undiscounted) fee \$ _____ (Fee Code 1469).
- ☐ Small entity fee \$ _____ (Fee Code 2469). Applicant asserts small entity status. See 37 CFR 1.27.
- ☐ Micro entity fee \$ _____ (Fee Code 3469). Applicant has established or is establishing micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

(B) For delay less than or equal to two years:

37 CFR 1.17(m)(2)

- ☐ Other than a small or micro entity (undiscounted) fee \$ _____ (Fee Code 1454).
- ☒ Small entity fee \$ 904.00 (Fee Code 2454). Applicant asserts small entity status. See 37 CFR 1.27.
- ☐ Micro entity fee \$ _____ (Fee Code 3454). Applicant has established or is establishing micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

3. Statement: The entire delay between the date the benefit claim was due under 37 CFR 1.78(d)(3) and/or 37 CFR 1.78(a)(4) and the date the benefit claim was filed was unintentional.

Petitioner is reminded that a change in circumstance or a delay resulting from a deliberately chosen course of action does not become an "unintentional" delay because, for example:

- the applicant does not consider any patent to be of sufficient value to justify the financial expense of obtaining the patent; or
- the applicant remains interested in eventually obtaining a patent, but simply seeks to defer patent fees and patent prosecution expenses.

NOTE: Where the petition under 37 CFR 1.78(c) and/or 37 CFR 1.78(e) is filed more than two years after the date the priority or benefit claim was due, the United States Patent and Trademark Office requires an additional explanation of the circumstances surrounding the delay that establishes the entire delay was unintentional. This requirement is in addition to the requirement to provide a statement that the entire delay was unintentional. See *Clarification of the Practice for Requiring Additional Information in Petitions Filed in Patent Applications and Patents Based on Unintentional Delay*, 85 FR 12222 (March 2, 2020). See MPEP 711.03(c)(II)(C)-(F) for additional guidance on the information required to establish that the entire delay was unintentional.

☐ Because this petition under 37 CFR 1.78(c) and/or 37 CFR 1.78(e) is being filed more than two years after the date the priority or benefit claim was due, additional explanation of the circumstances surrounding the delay that establishes the entire delay was unintentional is enclosed herewith. Note: If this box is checked, section 2A must also be completed.

Reminder: Presentation of a benefit claim may prompt a requirement to pay the continuing application fee set forth in 37 CFR 1.17(w), if the actual filing date of the application is more than six years after the earliest benefit date. See 37 CFR 1.78(d)(3)(i) and 37 CFR 1.17(w).

**PETITION TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C. 119(e)
(37 CFR 1.78(c)) AND/OR TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C.
120, 121, 365(c), or 386(c) (37 CFR 1.78(e)) FOR THE BENEFIT OF A PRIOR-FILED APPLICATION**

Page 3 of 5

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

/Gerard M. Wissing/

Signature*

Gerard M. Wissing

Typed or Printed Name

Industrious at Hudson Yards, 31 Hudson Yards, 11th Floor

Address

New York, New York 10001

Address

November 14, 2025

Date

36309

Registration Number, if applicable

(516) 901-7027

Telephone Number

* This petition must be signed in accordance with 37 CFR 1.33. Please see 37 CFR 1.4(d) for the signature requirements. Submit multiple forms if more than one signature is required.

Enclosures:

☒ Application Data Sheet (see instructions starting on page 4)

☒ Fee (along with supporting documentation, if required)

☐ Other: _____

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

☐ Deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

☒ Transmitted by the USPTO patent electronic filing system or by facsimile to 571-273-8300, to the USPTO on the date shown.

November 14, 2025

Date

/Gerard M. Wissing/

Signature

Gerard M. Wissing

Typed or printed name of person signing certificate

Instructions for Petition to Accept an Unintentionally Delayed Claim under 35 U.S.C. 119(e) (37 CFR 1.78(c)) and/or to Accept an Unintentionally Delayed Claim under 35 U.S.C. 120, 121, 365(c), or 386(c) (37 CFR 1.78(e)) for the Benefit of a Prior-Filed Application

(Not to be Submitted to the USPTO)

When filing electronically via the USPTO patent electronic filing system, use Doc Code PET.PCT (Petition for review by the PCT Legal Office) for applications filed under 35 U.S.C. 371 and/or if the reference to the prior-filed application(s) includes an international application or an international design application. In all other instances, use Doc Code PET.OP (Petition for review by the Office of Petitions).

1. The reference required to the prior-filed application:

a. For applications filed on or after September 16, 2012, the reference must be set forth in a corrected application data sheet (ADS). See 37 CFR 1.76.

Note: Any ADS filed after the filing of the application is considered a corrected (or updated) ADS even if an ADS was not previously submitted. A corrected ADS must identify the information that is being changed with underlining for insertions and strike-through or brackets for text removed. In general, the identification of the information being changed should be made relative to the most recent filing receipt. For example, where the most recent filing receipt for the application shows no benefit claim, the entire benefit claim must be shown with underlining in the corrected ADS. In addition, if the ADS identified an incorrect provisional application number and the most recent filing receipt included the incorrect provisional application number, the corrected ADS should identify the incorrect provisional application number being deleted with strike-through or brackets, and should identify the correct provisional application number being added with underlining. For more information regarding a corrected ADS in an application filed on or after September 16, 2012, see MPEP 601.05(a), subsection II.

A corrected ADS may include all of the section headings listed in 37 CFR 1.76(b) with all appropriate data for each heading or only those sections (including the section headings) containing changed or updated information. See 37 CFR 1.76(c)(2). A corrected ADS must identify the application by application number and be properly signed.

Use of the corrected Web-based ADS is recommended for registered users of the USPTO patent electronic filing system because it will pre-populate with information of record; applicants can then type in the desired changes, and the system will create a PDF version with the appropriate strike-through and underlining. For more information, see the Quick Start Guide for "Application Data Sheet to Update and/or Correct Information" available at <https://www.uspto.gov/sites/default/files/documents/Corrected-WebADS-QSG.pdf>

Applicants may also use Form PTO/AIA/14, which may be printed and marked up to comply with 37 CFR 1.76(c).

Instructions for Petition to Accept an Unintentionally Delayed Claim under 35 U.S.C. 119(e) (37 CFR 1.78(c)) and/or to Accept an Unintentionally Delayed Claim under 35 U.S.C. 120, 121, 365(c), or 386(c) (37 CFR 1.78(e)) for the Benefit of a Prior-Filed Application

(Not to be Submitted to the USPTO)

b. For applications filed before September 16, 2012, the reference to the prior-filed application may be made in a supplemental ADS in compliance with pre-AIA 37 CFR 1.76(c) or in an amendment in the first sentence(s) of the specification following the title. See 37 CFR 1.78(h).

Note: For applications filed before September 16, 2012, any ADS submitted after the filing date of the application is a supplemental ADS, regardless of whether an original ADS was submitted with the application papers on filing. Supplemental ADS papers must be labeled Supplemental ADS or Supplemental Application Data Sheet, include each of the seven section headings listed in pre-AIA 37 CFR 1.76(b) with all appropriate data for the section heading, and identify the information that is being changed. See pre-AIA 37 CFR 1.76(c). A supplemental ADS must also identify the application by application number and be properly signed. For more information regarding a supplemental ADS in an application filed before September 16, 2012, see MPEP 601.05(b), subsection II.

2. Petition fee:

The petition fee is set forth in 37 CFR 1.17(m) and must be included with the petition. Petitioner is advised to refer to the current fee schedule at <https://www.uspto.gov/learning-and-resources/fees-and-payment/uspto-fee-schedule>.

Note: Effective January 19, 2025, presentation of a benefit claim under 35 U.S.C. 120, 121, 365(c), or 386(c) may prompt a requirement to pay the continuing application fee set forth in 37 CFR 1.17(w), if the actual filing date of the application is more than six years after the earliest benefit date. See 37 CFR 1.78(d)(3)(i) and 37 CFR 1.17(w).

3. Statement:

37 CFR 1.78(c) and 37 CFR 1.78(e) require a statement that the entire delay between the date the benefit claim was due and the date the benefit claim was filed was unintentional. The required statement(s) is included in this form.

Note: the Director may require additional information where there is a question whether the delay was unintentional.

[Page 5 of 5]

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013). <https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf>

Routine uses of the information in this record may include disclosure to: 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law; 2) a federal, state, local, or international agency, in response to its request; 3) a contractor of the USPTO having need for the information in order to perform a contract; 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record; 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record; 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations; 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals; 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)); 9) the Office of Personnel Management (OPM) for personnel research purposes; and 10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV 2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--

Inventor Information:

Inventor 1						Remove	
Legal Name							
Prefix	Given Name	Middle Name	Family Name	Suffix			
	Shih-Yuan		WANG				
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service							
City	Palo Alto	State/Province	CA	Country of Residence	US		
Mailing Address of Inventor:							
Address 1		766 Encina Grande Drive					
Address 2							
City	Palo Alto	State/Province	CA				
Postal Code	94306	Country	US				
Inventor 2						Remove	
Legal Name							
Prefix	Given Name	Middle Name	Family Name	Suffix			
	Shih-Ping		WANG				
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service							
City	Los Altos	State/Province	CA	Country of Residence	US		
Mailing Address of Inventor:							
Address 1		38 Third Street, Suite 307					
Address 2							
City	Los Altos	State/Province	CA				
Postal Code	90422	Country	US				
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.							

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

☐ An Address is being provided for the correspondence information of this application.

Customer Number

Email Address

Add Email

Remove Email

Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		
Attorney Docket Number	309-0015USCIPDIV2	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	48	Suggested Figure for Publication (if any)	58

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	139982		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
19036506	Division of	18822880	2024-09-03

Application Data Sheet 37 CFR 1.76			Attorney Docket Number		309-0015USCIPDIV2	
			Application Number		19/036,506	
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES				
Prior Application Status		Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
18822880	Division of	18385213	2023-10-30	12087871	2024-09-10	
Prior Application Status		Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
18385213	Continuation in part of	17974325	2022-10-26	11830954	2023-11-28	
Prior Application Status		Pending			Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)			
18385213	Continuation in part of	18113474	2023-02-23			
Prior Application Status		Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
18113474 ¹⁸¹¹³⁷⁴⁷	Division of	17707429	2022-03-29	11621360	2023-04-04	
Prior Application Status		Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
17707429	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17	
Prior Application Status		Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14	
Prior Application Status		Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
16528958	Continuation in part of	15797821	2017-10-30	10446700	2019-10-15	
Prior Application Status		Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
18113474	Division of	17707429	2022-03-29	11621360	2023-04-04	
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.						

Application Data Sheet 37 CFR 1.76			Attorney Docket Number		309-0015USCIPDIV2	
			Application Number		19/036.506	
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES				

Prior Application Status		<u>Patented</u>				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
17707429	Division of	17532831	2021-11-22	11309444	2022-04-19	
Prior Application Status		<u>Patented</u>				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
17532831	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17	
Prior Application Status		<u>Patented</u>				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14	
Prior Application Status		<u>Abandoned</u>				Remove
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
16528958		Continuation in part of		PCTUS1667977	2016-12-21	
Prior Application Status		<u>Patented</u>				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
16528958	Continuation in part of	16042535	2018-07-23	10700225	2020-06-30	
Prior Application Status		<u>Patented</u>				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
16528958	Continuation in part of	16296985	2019-03-08	10468543	2019-10-16	
Prior Application Status		<u>Patented</u>				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
18113474	Division of	177077429	2022-03-29	11621360	2023-04-04	
Prior Application Status		<u>Patented</u>				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
177077429	Division of	17532831	2021-11-22	11309444	2022-04-19	
Prior Application Status		<u>Patented</u>				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
17532831	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17	
Prior Application Status		<u>Patented</u>				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)	
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14	

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		Application Number		19/036.506	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES				

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	14947718	2015-11-20	10622498	2020-03-25
Prior Application Status		Abandoned		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Continuation in part of	PCTUS1667977	2016-12-21		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-20	10446700	2019-08-25
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16042535	2018-07-23	10700225	2020-06-30
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16296985	2019-03-08	10468543	2019-10-16
Prior Application Status		Abandoned		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Continuation in part of	PCTUS1843289	2018-07-23		
Prior Application Status		Abandoned		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Continuation in part of	PCTUS1857963	2018-10-29		
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Claims benefit of provisional	62713455	2018-08-01		
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Claims benefit of provisional	62716310	2018-08-08		

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62717750	2018-08-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62719689	2018-08-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62724449	2018-08-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62733476	2018-09-19

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		Application Number	19/036.506	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status	Expired	Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
16/528958	Claims benefit of provisional	62/737062	2018-09-26	
Prior Application Status	Expired	Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
16/528958	Claims benefit of provisional	62/750016	2018-10-24	
Prior Application Status	Expired	Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
16/528958	Claims benefit of provisional	62/770656	2018-11-21	
Prior Application Status	Expired	Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
16/528958	Claims benefit of provisional	62/772498	2018-11-28	
Prior Application Status	Expired	Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
16/528958	Claims benefit of provisional	62/777157	2018-12-09	
Prior Application Status	Expired	Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
16/528958	Claims benefit of provisional	62/779693	2018-12-14	
Prior Application Status	Expired	Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
16/528958	Claims benefit of provisional	62/784342	2018-12-21	
Prior Application Status	Expired	Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
16/528958	Claims benefit of provisional	62/794330	2019-01-18	
Prior Application Status	Expired	Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
16/528958	Claims benefit of provisional	62/797141	2019-01-25	

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/797263	2019-01-26
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/800371	2019-02-01
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/802171	2019-02-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/802718	2019-02-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/805850	2019-02-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/808949	2019-02-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/819604	2019-03-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/819669	2019-03-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/820695	2019-03-19

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/828976	2019-04-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/841798	2019-05-01
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/843206	2019-05-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/846554	2019-05-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/853280	2019-05-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/860115	2019-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/863231	2019-06-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/863852	2019-06-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/867186	2019-06-26

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0015USCIPDIV2	
		Application Number		19/036.506	
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/868911	2019-06-29		
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/870533	2019-07-03		
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/873891	2019-07-13		
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/874418	2019-07-15		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
PCT/US18/57963	Continuation of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/797821	Continuation in part of	14/947718	2015-11-20	10622498	2020-03-25
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/797821	Continuation in part of	15/309922	2016-11-09	9818893	2017-10-25
Prior Application Status		Abandoned		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
15/797821	Continuation in part of	PCT/US16/67977	2016-12-21		
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
15/797821	Claims benefit of provisional	62/465734	2017-03-01		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	<u>19/036,506</u>
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
<u>15/797821</u>	<u>Claims benefit of provisional</u>	<u>62/474179</u>	<u>2017-03-21</u>
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
<u>15/797821</u>	<u>Claims benefit of provisional</u>	<u>62/484474</u>	<u>2017-04-12</u>
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
<u>15/797821</u>	<u>Claims benefit of provisional</u>	<u>62/487606</u>	<u>2017-04-20</u>
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
<u>15/797821</u>	<u>Claims benefit of provisional</u>	<u>62/488998</u>	<u>2017-04-24</u>
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
<u>15/797821</u>	<u>Claims benefit of provisional</u>	<u>62/500581</u>	<u>2017-05-03</u>
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
<u>15/797821</u>	<u>Claims benefit of provisional</u>	<u>62/505974</u>	<u>2017-05-14</u>
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
<u>15/797821</u>	<u>Claims benefit of provisional</u>	<u>62/509093</u>	<u>2017-05-20</u>
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
<u>15/797821</u>	<u>Claims benefit of provisional</u>	<u>62/510249</u>	<u>2017-05-23</u>
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
<u>15/797821</u>	<u>Claims benefit of provisional</u>	<u>62/514889</u>	<u>2017-06-04</u>

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/521504	2017-06-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/522169	2017-06-20
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/527962	2017-06-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/530281	2017-07-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/533078	2017-07-16
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/533603	2017-07-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/542243	2017-08-07

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP00v2 <small>Type text here</small>
		Application Number	19/036.506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/547728	2017-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/542243	2017-08-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639472	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/628764	2018-02-09

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/643010	2018-03-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/640522	2018-03-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/599246	2017-12-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/645810	2018-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/666005	2018-05-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/607860	2017-12-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/631630	2018-02-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/677609	2018-05-29

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		Application Number	<u>19/036.506</u>
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/634692	2018-02-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/652830	2018-04-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/591072	2017-11-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639356	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/615314	2018-01-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/623971	2018-01-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/637945	2018-03-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/651053	2018-03-30

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/682909	2018-06-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/659072	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/659067	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/669194	2018-05-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/675130	2018-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/547728	2017-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/651087	2018-03-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/646871	2018-03-22

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		Application Number		19/036,506	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES				

Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/662217	2018-04-24		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/639920	2018-03-07		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/633514	2018-02-21		
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/296985	Continuation of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/042535	Continuation in part of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/535801	2017-07-21		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/540524	2017-08-02		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/542243	2017-08-07		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/547728	2017-08-18		

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/591072	2017-11-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/599246	2017-12-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/607860	2017-12-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/615314	2018-01-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/623971	2018-01-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/628764	2018-02-09

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/631630	2018-02-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/633514	2018-02-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/634692	2018-02-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/637945	2018-03-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639356	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639472	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639920	2018-03-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/640522	2018-03-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/643010	2018-03-14

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

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		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/645810	2018-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/646871	2018-03-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/651053	2018-03-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/651087	2018-03-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/652830	2018-04-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/659067	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/659072	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/662217	2018-04-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/666005	2018-05-02

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/669194	2018-05-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/675130	2018-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/677609	2018-05-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/682909	2018-06-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/270577	2015-12-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/304907	2016-03-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/290391	2016-02-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/334934	2016-05-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/338263	2016-05-18

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/346850	2016-06-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/359349	2016-07-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/366188	2016-07-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/368109	2016-07-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/374828	2016-08-13
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/376869	2016-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/380364	2016-08-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/383391	2016-09-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/383479	2016-09-04

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Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/394222	2016-09-14		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/398607	2016-09-23		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/401126	2016-09-28		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/406999	2016-10-12		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/414671	2016-10-29		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/415339	2016-10-31		
Prior Application Status	Abandoned		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
15/309922	a 371 of international	PCT/US15/61120	2015-11-17		
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/309922	Continuation of	14/943898	2015-11-17	9530905	2016-12-27
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/309922	Continuation of	14/945003	2015-11-18	9525084	2016-12-20

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

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		Application Number	19/036.506
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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/175855	2015-06-15

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/090879	2014-12-11

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/182602	2015-06-21

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/100025	2015-01-05

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943888	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943888	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/188876	2015-07-06

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/111582	2015-02-03

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Abandoned	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/947718	Continuation of	PCT/US14/39208	2014-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/826446	2013-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/843021	2013-07-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/905109	2013-11-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/834873	2013-06-13
Prior Application Status	Abandoned	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/892821	a 371 of international	PCT/US14/39208	2014-05-22

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES		
<p>This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.</p> <p>☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.</p>			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2 <small>not here</small>
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1			
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
<input type="button" value="Clear"/>			
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117	
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor: <input type="text"/>			
If the Applicant is an Organization check here. ☒			
Organization Name	W&WSens Devices, Inc.		
Mailing Address Information For Applicant:			
Address 1	38 Third Street, Suite 307		
Address 2			
City	Los Altos	State/Province	CA
Country	US	Postal Code	94022
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country ⁱ		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is <u>not</u> checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).				
This Application Data Sheet <u>must</u> be signed by a patent practitioner if one or more of the applicants is a juristic entity (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, <u>all</u> joint inventors who are the applicant, <u>or</u> one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of <u>all</u> joint inventor-applicants.				
See 37 CFR 1.4(d) for the manner of making signatures and certifications.				
Signature	/Ivan S. Kavrukov/ <u>Gerard M. Wissing</u>		Date (YYYY-MM-DD)	<u>2025-11-14</u> <u>2025-01-24</u>
First Name	Ivan S. <u>Gerard</u>	Last Name	Kavrukov <u>Wissing</u>	Registration Number 25,161 <u>36,309</u>
Additional Signature may be generated within this form by selecting the Add button.				

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	19/036,506
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Attorney Docket No.: 309-0015USCIPDIV2
Confirmation No.: 4276

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

<p>In re Application of: Shih-Yuan WANG et al.</p> <p>Application No.: 19/036,506</p> <p>Filed: January 24, 2025</p> <p>Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES</p>	<p>Examiner: Eduardo A. Rodela</p> <p>Art Unit: 2893</p> <hr/> <p>CERTIFICATE OF TRANSMISSION</p> <p>I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</p> <p style="text-align: right;">/Mary Ellen Finnegan/ Name: Mary Ellen Finnegan</p> <p>Date: Nov. 14, 2025</p>
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Mail Stop Petitions

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CORRECTED FILING RECEIPT

Applicant hereby submits this Request for Corrected Filing Receipt to recognize Applicant's Priority Claim set forth in the Corrected Application Data Sheet filed concurrently herewith.

On November 12, 2025 the Office mailed a Corrected Filing Receipt that did not recognize one or more benefit claims listed in the Domestic Benefit section of the ADS filed with the Application on January 24, 2025 (the "Original ADS"). Applicant then reviewed the benefit claims listed in the Domestic Benefit section of the Original ADS and noticed a typographical error in one application listed.

To correct the typographical error and restore the original chain of priority, Applicant hereby submits:

1. A Corrected Application Data Sheet with underlining to correct the priority claims in the Domestic Benefit section of the Original ADS;

2. A Petition to Accept an Unintentionally Delayed Priority Claim; and
3. The required Petition Fee.

Applicant respectfully requests the Office issue a Corrected Filing Receipt in accordance with the Corrected Application Data Sheet submitted herewith.

The Office is hereby authorized to charge any fees that may be required in connection herewith and to credit any overpayment to our Deposit Account No. 600125.

Respectfully submitted,

/Gerard M. Wissing/

Gerard M. Wissing
Registration No. 36,309
Attorney for Applicant

Date: November 14, 2025

Wissing Miller LLP
Address: (associated with Customer Number: 139982)
Phone: (516) 901-7027



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PATENT AND TRADEMARK OFFICE

Page 1 of 2
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
19/036,506

RECEIPT DATE / TIME
11/14/2025 04:26:45 PM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 4276

FILED BY Mary Ellen Finnegan

PATENT CENTER # 73187611

FILING DATE 01/24/2025

CUSTOMER # 139982

FIRST NAMED
INVENTOR Shih-Yuan WANG

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Gerard Wissing

Documents

TOTAL DOCUMENTS: 3

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV2_Req_Correct_Filing_Rcpt_Filed_14Nov2025.pdf	2	Request for Corrected Filing Receipt	94 KB
309-0015USCIPDIV2_Petition_Change_Priority_Claim_Filed_14Nov2025.pdf	6	Petition for review by the Office of Petitions	308 KB
309-0015USCIPDIV2_Corrected_ADS_Filed__14Nov2025.pdf	37	Application Data Sheet	21300 KB

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DOCUMENT	MESSAGE DIGEST(SHA-512)
309- 0015USCIPDIV2_Req_Correct _Filing_Rcpt_Filed 14Nov2025.pdf	55973BCE7FFF0271B550EEBF644DF6E80705CD11D8AE31712 8A6F69130773544008B9466B33429287558FBAF022E1A068CB ABDB36457158887CCBE09942768DB
309- 0015USCIPDIV2_Petition_Cha nge_Priority_Claim_Filed_14No v2025.pdf	29162D7DE3AA26BB21C479F5052238082058C64F15802C9CD C7BE05F46330496DA5A8B48CD4E04BDCF2E5FAB98FC32783 A1C29B7A8C7441ADC65FEFA8637091C
309- 0015USCIPDIV2_Corrected_A DS_Filed__14Nov2025.pdf	5021FD35117AE1215BBE4C825EA6319E88D0CD335750D3F3B 166AAA05B704569271A08B586331307F77E177BBC3E35935BC 4E89D4201F17C884F841E2B3E5DE3

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If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #
19/036,506

RECEIPT DATE / TIME
11/14/2025 04:26:45 PM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 4276

FILED BY Mary Ellen Finnegan

PATENT CENTER # 73187611

AUTHORIZED BY Gerard Wissing

CUSTOMER # 139982

FILING DATE 01/24/2025

CORRESPONDENCE
ADDRESS -

FIRST NAMED
INVENTOR Shih-Yuan WANG

Payment Information

PAYMENT METHOD
CARD / 8026

PAYMENT TRANSACTION ID
E2025ADG27486067

PAYMENT AUTHORIZED BY
Mary Ellen Finnegan

PRE-AUTHORIZED ACCOUNT
600125

PRE-AUTHORIZED CATEGORY
37 CFR 1.21 (Miscellaneous fees and charges)

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
2454	PETITION FOR THE DELAYED SUBMISSION OF A PRIORITY OR BENEFIT CLAIM, OR TO RESTORE THE RIGHT OF PRIORITY OR BENEFIT	904.00	1	904.00
TOTAL AMOUNT:				\$904.00

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
19/036,506	01/24/2025	Shih-Yuan WANG	309-0015USCIPDIV2	4276
139982	7590	11/21/2025	EXAMINER	
Wissing Miller LLP			RODELA, EDUARDO A	
Industrious at Hudson Yards			ART UNIT	
31 Hudson Yards, 11th Floor			PAPER NUMBER	
New York, NY 10001			2893	
			NOTIFICATION DATE	DELIVERY MODE
			11/21/2025	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Application No. : 19036506
Applicant : Wang
Filing Date : 01/24/2025
Date Mailed : 11/21/2025

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given two (2) months from the mail date of this Notice within which to respond. This time period for reply is extendable under 37 CFR 1.136(a) for only TWO additional MONTHS.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED.

See attachment(s).

*A copy of this notice **MUST** be returned with the reply. Please address response to
"Mail Stop Issue Fee, Commissioner for Patents,
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/Chris Harmon/
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IDENTIFICATION OF DRAWING DEFICIENCIES

- ☐ There is a hole or the image thereof within the illustration. FIG(s)
- ☐ The illustration is penetrated or traversed by a solid or broken line that is not intended to be part of the drawing, such as a dark line caused by a flaw in the copying process. FIG(s)
- ☐ An ink stamp or the image thereof obscures part of the illustration. FIG(s)
- ☐ The drawing is marred by black smudges, obliterations, or fax/copier marks (for example, speckles or dots in a substantial portion of the drawing). FIG(s)
- ☐ Figure numbers are duplicated or missing. FIG(s)
- ☐ Drawing sheet or figure is missing. FIG(s)
- ☐ Numbers, letters, or reference characters in the drawing have been crossed out or are illegibly handwritten. FIG(s)
- ☐ The character of the lines, numbers, and letters is poor. FIG(s)
- ☐ The drawing's background shows that the original drawing was made on graph paper or other paper with a pattern or decoration. FIG(s)
- ☐ The FIG. number label is placed in a location that causes the drawing to be read upside down. FIG(s)
- ☒ Data, a reference number, or part of the drawing is truncated or missing, or a lead line has no reference number. FIG(s) 40,45
- ☐ The drawing and/or the FIG. label contain(s) foreign language. FIG(s)
- ☐ This utility application contains a photograph of a view that is capable of being illustrated as a line drawing. FIG(s)
- ☐ A petition under 37 CFR 1.84(a)(2) to accept color drawings has been granted, but the brief description of the drawings in the specification does not contain (or has not been amended to contain) the paragraph required by 37 CFR 1.84(a)(2)(iii).
- ☐ This reissue application contains added and/or amended drawings that are not labeled as "New" or "Amended" or "Canceled" as required by 37 CFR 1.173(b)(3). FIG(s)
- ☐ This Design reissue application contains a drawing that is labeled as "Canceled" but is not surrounded by brackets, or a drawing that is surrounded by brackets but is not labeled as "Canceled." See 37 CFR 1.173(b)(3). FIG(s)
- ☐ OTHER:
- ☐ COMMENTS: