

EXHIBIT C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re <i>Ex Parte</i> Reexamination of:	)	
	)	
U.S. Patent No. 12,087,871	)	
	)	
Issued: Sept. 10, 2024	)	Group Art Unit: To Be Assigned
	)	
Named Inventor: Shih-Yuan Wang et al.	)	Examiner: To Be Assigned
	)	
Control Number: To Be Assigned	)	
	)	
Filed: Oct. 30, 2023	)	
	)	
Title: Microstructure Enhanced Absorption	)	
Photosensitive Devices	)	

DECLARATION OF MICHAEL LEBBY PH.D.

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I. INTRODUCTION

1. I, Michael Lebby, Ph.D., have been retained as an independent expert by Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor LLC (“Petitioner” or “Samsung”) in connection with a request for *ex parte* reexamination of U.S. Patent No. 12,087,871 (“the ’871 patent”) (Ex-A). I have prepared this declaration in connection with Samsung’s request for *ex parte* reexamination.

2. Specifically, this document contains my opinions about the technology in claims 1-4, 6-8, and 10-18 of the ’871 patent and the grounds against these claims that have been asserted by Samsung. I was not asked to provide any opinions about the ’871 patent that are not expressed herein.

II. SUMMARY OF OPINIONS

3. This declaration considers claims 1-4, 6-8, and 10-18 of the ’871 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

4. Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of May 22, 2013), it is my opinion that claims 1-4, 6-8, and 10-18 of the ’871 patent would have been obvious based on the asserted grounds discussed below.

5. I am being compensated for my time at my normal hourly rate. My compensation is in no way contingent upon the nature of my findings, the presentation of my findings in testimony, or the outcome of this proceeding.

III. QUALIFICATIONS AND BACKGROUND

6. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A to this declaration.

7. Based on my education, research, and work experience, I am knowledgeable about the subject matter of the '871 patent and the related prior art.

8. In what follows, I provide a short summary of my qualifications.

9. I am an engineer with a Ph.D. in Electrical and Electronic Engineering and have worked extensively with optoelectronics, photonics, electrical and electronic circuits, optical systems, as well as integrated circuit semiconductors for both optoelectronic and electronic solutions. Overall, I have approximately 40 years of experience working in industry to develop new electronic, photonic, display, and optics-based products, which I have taken from research to manufacturing.

10. I received a Bachelor of Engineering degree in Electrical and Electronic Engineering in 1984 from the University of Bradford, United Kingdom. I received a Ph.D. in Electrical and Electronic Engineering in 1987 from the University of Bradford, United Kingdom. I also received a second doctorate degree: a Doctor of Engineering degree (D.Eng) in electrical and electronic engineering in 2004 from the University of Bradford, United Kingdom.

11. I am currently Chief Executive Officer (CEO) and Chief Technology Officer (CTO) of GenusTechnik Inc., which is my consulting company, through which I engage in my expert witness work.

12. I recently retired in late 2024 as Chairman and CEO of Lightwave Logic Inc. (NASDAQ: LWLG), where I served as a Director of the Board of Directors since 2015.

13. I am a named inventor on over 225 U.S. utility patents. My work has also led to me either being an inventor or co-inventor in subjects such as: semiconductors, electronics, optics, displays, high frequency optical and electronic products such as lasers and LEDs, as well as photonic integrated circuits. I am the author of more than 60 publications.

14. I am a Fellow grade of three professional organizations: IEEE (Institute of Electrical and Electronic Engineers), NAI (National Academy of Inventors), and Optica (Optical Society of America).

15. As described in this Section, and further detailed in my *curriculum vitae* (Appendix A) over the course of my 40-year career in electronics and optoelectronics, I have worked in nearly every aspect of the electronic, semiconductor, and optoelectronics business, ranging from wafers to components, to modules, displays, optics, connectors and cable technology. At the wafer level, I have experience in epitaxial wafer growth (compound semiconductors). I also have experience in electrical and optoelectronic device and circuit design, using modeling and simulation, electrical and optoelectronic device and component fabrication, testing, and qualification, implementation of devices such as laser diodes, light emitting diodes, photodetectors etc., into packages, connectors, and panels, both hermetic and non-hermetic, as well as analysis of package/panel materials such as plastics (including plastic housings such as resin-packaged lead frame housings), optical plastics, metallic-based packages, semiconductor-based packages, and ceramic-based packages for fiber optics, displays, and data-communications industries. I have also designed device packages (through-pin, surface mount, flip-chip, and various combinations thereof) for printed circuit board mounting as well as electrical and optical components for various industrial and environmental applications. Many of the designed components were implemented into technology applications both as manufactured

products as well as components for testing, characterization and analysis of qualified products for volume scaling. The components were designed to work at both optical and RF frequencies that include both optical and RF wireless as well as fiber-optics based applications. I have also worked in commercially based industrial research-and-development laboratories to bring new high-performance optoelectronic- and photonic-based technologies from the research proof-of-concept phase through prototyping up to and including qualified manufacturing for volume release. This has included both transfer of as well as the design of optics and optical systems for various commercial systems.

16. I have been both an entrepreneur (*e.g.*, Ignis Optics Inc, One Chip Photonics, Lightwave Logic Inc.), as well as an intrapreneur (*e.g.*, Motorola, Intel, TE Connectivity (previously Tyco Electronics), AT&T Bell Labs), creating innovative new high technology programs, both as venture backed start-ups as well as corporate funded divisions. I have built these entities to develop optical, electronic, optoelectronics, and photonics technology from the laboratory and fabrication clean room to production factories.

17. My career started in the late 1970s at the Ministry of Defense in the United Kingdom where I spent time at a number of their R&D facilities including Malvern (RSRE – Royal Signals and Radar Establishment). There, I worked on electronic and optoelectronic semiconductor device design, as well as basic and high frequency telecommunications and data-communications electronics for module, cable, connector, and circuit implementation. My research work in electronics then took me to AT&T Bell Laboratories in 1985, where I pursued research in novel electronic and optoelectronic semiconductor material systems that included laser diodes, LEDs, photodetectors, optical waveguides, optics, and standard electronic devices

as well as the processing and fabrication for such devices. The devices researched at Bell Labs became in part the subject of my Ph.D. thesis for which I was granted a doctoral degree in 1987.

18. I moved to Motorola in 1989 to further develop my skills in consumer commercial application of technology and focused on optoelectronics, and semiconductor engineering and development. I became a Research and Development Manager in Motorola, until I left the company in 1998. During my time at Motorola, I worked on many photonic, electronic, and optical technology projects that included projection, display, optics, LEDs, OLEDs, laser diodes, phosphors, cameras, as well as the packaging and reliability of mobile product prototypes. At that time, I was particularly interested in miniaturization of electronics, optics, and optoelectronics, and worked on novel optical designs that included portable heads-up displays, optical heads for storage, and various light-based prototypes as well as advanced prototypes of futuristic communications and consumer hardware and cameras.

19. The research work at Motorola also included work on displays and in particular, miniature displays, arrays, imagers, projection systems, and optics for pagers, clam-shell phones, and head-mounted displays that included mounting onto eyeglasses (similar in concept to Google glass™) as well as techniques for electrical and optical connections in these applications.

20. I also initiated Motorola's work in optical interconnect (Optobus™) technology, which incorporated both transfer and injection molded optical parts and included the design of electrical and optical connector technology. This project involved the research and development of a multi-channel electronic IC chip for parallel optical interconnects as well as optical simulations of performance.

21. I was one of Motorola's most prolific inventors, having over 150 issued utility patents as an inventor or a co-inventor by the late 1990s. Many of the photonics and optical

prototypes with which I was involved were subject to reliability and stress testing as well as optical measurement analysis. These consumer products all were driven using standard electronic ICs and electronic signaling where I had a role in design and simulation of these circuits.

22. Between 1998 and 1999, I worked as the Director of Technology/ BD (Fiber Optics) for Tyco Electronics (previously AMP). I joined Tyco Electronics as a business development director and director of advanced technology for the telecommunications and data-communications industries. I was responsible for growing the optical and optoelectronic technology business through external interactions that included mergers, acquisitions, strategic alliances, and technical strategic planning as well as leading new technology projects.

23. In 1999, I left Tyco and started employment at Intel. At Intel, I was involved heavily in photonic technology, especially technology that supported silicon photonic device platforms with different types of displays and optical systems. As a culmination of this work, I was one of Intel's founders of its silicon photonics division in the year 2000, and worked to set up a fabrication facility in South San Jose, California, USA. The work involved integrating silicon FET electronics with optoelectronics and optics onto the same silicon semiconductor wafer. This included CMOS detectors and arrays. I was also part of Intel Capital's optical investment team, and participated in over 30 photonics investment projects into photonics, optics, and optoelectronics. My focus included optical devices, packaging and modules for optical storage, consumer applications such as displays, cameras, projection, communications, and sensing. The technologies that I investigated included lasers, LEDs, optics, LCDs, optical waveguides, cameras, imagers, and optical displays.

24. At the end of 2000, I left Intel and raised venture capital funding for a company called Ignis Optics Inc. The main goal of the company was to design and manufacture, in high

volume, very high-performance optoelectronic modules. These fiber optic transceiver modules have the capability of transmitting and receiving optical signals that are controlled using programmable electronics and packaged optoelectronics chips, such as laser diodes, optical lenses, and photodetectors.

25. In 2005, I took up employment for a trade association, based in Washington, D.C., called IEEE Optoelectronics Industry Development Association (OIDA). As head of this trade association, and with electronics, photonics and optics manufacturers that included manufacturers of projection displays, optical systems, fiber optics, display, cameras, sensing, defense, aerospace, LED lighting, and automotive vendors as members, I was responsible, in part, for industry-based technology roadmaps; and I implemented common industry roadmap methodologies with common features such as “Red Brick Walls” and transferred them into technology roadmaps for the industry in which displays, optics, optical sensors, telecommunications cables, fiber-optic cables, fiber, cameras, and their associated technology platforms, were featured. OIDA roadmaps featured purple brick walls, to show differentiation from the semiconductor industry.

26. In 2010, I became the General Manager and CTO of Translucent, Inc., a high-tech start-up company which developed and manufactured silicon and rare earth oxide based epitaxial semiconductor wafers. I patented a number of optoelectronic and electronic device designs using rare earth oxides and phosphors while employed at Translucent.

27. Throughout my career, I have also had an active role in a number of technical professional organizations, including, among others, IEEE Components, Packaging, and Manufacturing Technology (CPMT), IEEE Electronic Components and Technology Conferences (ECTC); IEEE TC-10 (Technical Committee on Optoelectronics), and IEEE Optoelectronics

Industry Development Association (OIDA). Through these organizations, I have consistently been a part of committees, events, and workshops relating to semiconductor, optoelectronics, electronics, and packaging technology.

28. I also serve as a Technical Expert/Consultant for the European Commission. In my work at the European Commission, I review and advise on general optics, photonics, electronics, telecommunications, semiconductors, optoelectronics, imaging, sensing, cameras, display (*e.g.*, LCD, LED, OLED, etc.), and related Information and Communications Technology (ICT).

29. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which is attached to this declaration as Appendix A.

IV. MATERIALS CONSIDERED

30. In forming my opinions, I have analyzed the materials listed in the Table below. My opinions are based on my experience, knowledge of the relevant art, the documents identified in the Table below, as well as the documents directly cited in this declaration.

Exhibit	Description
Ex-A	U.S. Patent No. 12,087,871 B2 to Wang et al. (“’871 patent”)
Ex-B	Prosecution History of the ’871 patent (downloaded from Patent Center)
PA-1	U.S. Patent Application Publication No. 2012/0049044 A1 to Kuboi (“ <i>Kuboi</i> ”)
PA-2	U.S. Patent Application Publication No. 2012/0033119 to Shinohara (“ <i>Shinohara</i> ”)
PA-3	U.S. Patent Application Publication No. 2012/0153124 A1 to Yu et al. (“ <i>Yu</i> ”)
Ex-1001	<i>Electrical Engineering Dictionary</i> - CRCnetBase (Phillip A. Laplante editor-in-chief, CRC Press LLC 2000).
Ex-1002	M.E. Azim-Araghi et al., <i>Electrical and optical properties of an organic semiconductor metal-free phthalocyanine (C₃₂H₁₈N₈)</i> , Eur. Phys. J. Appl. Phys. (2012), Vol. 58, pp. 30201-p1 to 30201-p6.

Exhibit	Description
Ex-1003	M.M. El-Nahas et al., <i>Structural and optical properties of thermally evaporated zinc phthalocyanine thin films</i> , Proc. 2 nd Saudi Sc. Conf. (March 2004), pp. 277-293.
Ex-1004	M.M. El-Nahas et al., <i>Structural and optical properties of Ni (II) tetraphenyl porphyrin thin films</i> , Eur. Phys. J. Appl. Phys. (2012), Vol. 57, pp. 30201-p1 to 30201-p13.
Ex-1005	Horst Zimmerman, <i>Integrated Silicon Optoelectronics</i> (Springer. 2d ed. 2010), pp. 1-7.
Ex-1006	European Patent Application EP 2172974 A1 to NXP B.V. (“NXP”)
Ex-1007	U.S. Patent Application Publication No. 2008/0259981 A1 to Wang et al. (“Wang”)
Ex-1008	Martin A. Green, <i>Self-consistent optical parameters of intrinsic silicon at 300K including temperature coefficients</i> , Solar Energy Materials & Solar Cells, Vol. 92, (2008), pp. 1305-10.
Ex-1009	P.A. Lane et al., <i>Electroabsorption studies of phthalocyanine/perylene solar cells</i> , Solar Energy Materials & Solar Cells, Vol. 63, (2000), pp. 3-13.
Ex-1010	Zhihong Huang et al., <i>Microstructured silicon photodetector</i> , Applied Physics Letter, Vol. 89 (2006), pp. 033506-1 to -3.
Ex-1011	Richard A. Myers et al., <i>Enhancing near-infrared avalanche photodiode performance by femtosecond laser microstructuring</i> , Applied Optics, Vol. 45, No. 35 (Dec. 2006), pp. 8825-31.
Ex-1012	Abbas El Gamal et al., <i>CMOS Image Sensors</i> , IEEE Circuits & Devices Magazine (2005), pp. 6-20.
Ex-1013	Eric R. Fossum, <i>CMOS Image Sensors: Electronic Camera-On-A-Chip</i> , IEEE Transactions on Electron Devices, Vol. 44, No. 10 (Oct. 1997), pp. 1689-98.
Ex-1014	Sunetra Mendis et al., <i>CMOS Active Pixel Image Sensor</i> , IEEE Transactions on Electron Devices, Vol. 41, No. 3 (Mar. 1994), pp. 452-53.
Ex-1015	Renato Turchetta et al., <i>Introduction to CMOS Image Sensors</i> , Molecular Expressions TM Optical Microscopy Primer: Digital Imaging in Optical Microscopy - Introduction to CMOS Image Sensors (July 16, 2004), pp. 1-9, available at https://web.archive.org/web/20120508153832/https://micro.magnet.fsu.edu/primer/digitalimaging/cmosimagesensors.html
Ex-1016	U.S. Patent Application Publication No. 2013/0094865 A1 to Pinguet et al.
Ex-1017	U.S. Patent Application Publication No. 2012/026286 A1 to Na et al.
Ex-1018	S.M. Sze et al., <i>Semiconductor Devices Physics and Technology</i> (John Wiley & Sons, Inc. 3d ed. 2012), pp. 6-9, 205-10, 325-30, 392-406, 416-17, 466-67.

Exhibit	Description
Ex-1019	Rei Kitamura et al., <i>Optical constants of silica glass from extreme ultraviolet to far infrared at near room temperature</i> , Applied Optics, Vol. 46, No. 33 (November 20, 2007), pp. 8118-33.
Ex-1020	John P. Uyemura, <i>CMOS Logic Circuit Design</i> (Kluwer Academic Publishers 2002), pp. 64, 74-102, 315-17, 458-60.
Ex-1021	Khalil Jumah Tawfiq Hamam, <i>Organic Solar Cells Based on High Dielectric Constant Materials: An Approach to Increase Efficiency</i> (June 2013) (Ph.D. dissertation, Western Michigan University), pp. 1-122.
Ex-1022	P. Kalugasalam et al., <i>Dielectric and AC Conduction Studies of Lead Phthalocyanine Thin Film</i> , Chalcogenide Letters, Vol. 6, No. 9 (Sept. 2009), pp. 469-76.
Ex-1023	H. H. Li, <i>Refractive Index of Silicon and Germanium and Its Wavelength and Temperature Derivatives</i> , J. Phys. Chem. Ref. Data, Vol. 9, No. 3 (1980), pp. 561-658.
Ex-1024	U.S. Patent No. 8,390,036 B2 to Goto
Ex-1025	U.S. Patent Application Publication No. 2008/0157141 A1 to Han
Ex-1026	U.S. Patent No. 8,378,339 B2 to Nomura et al.
Ex-1027	U.S. Patent No. 8,274,122 B2 to Shimotsusa
Ex-1028	Certified English Language Translation of Japanese Patent Publication No. JP 2007-129024A to Hasegawa (“Hasegawa”)
Ex-1029	Jurgen Michel et al., <i>Advances in fully CMOS integrated photonic devices</i> , Proceedings of SPIE, Vol. 6477 (2007), pp. 64770P-1 to -11 (“Michel”).
Ex-1030	Mark Beals et al., <i>Process Flow Innovations for Photonic Device Integration in CMOS</i> , Proceedings of SPIE, Vol. 6898 (2008), pp. 689804-1 to -14 (“Beals”).
Ex-1031	Donald A. Neaman, <i>Semiconductor Physics and Devices – Basic Principles</i> (McGraw Hill 3d ed. 2003), pp. 247-50, 260-61.
Ex-1032	Japanese Patent Publication No. JP 2007-129024A
Ex-1033	International Patent Publication No. WO 2011/085297 A1 to Han et al. (“Han”)
Ex-1034	Matthew Saucedo, <i>Porphyrin Thin Film Dielectrics</i> , SUNFEST Technical Report TR-CST01NOV04, Center for Sensor Technologies, Univ. of Pennsylvania, Philadelphia, PA (2004), pp. 181-98.
Ex-1035	N. Venkatramaiah et al., <i>Spectroscopic and dielectric studies of meso-tetrakis(p-sulfonatophenyl) porphyrin doped hybrid borate glasses</i> , Journal of Alloys and Compounds, Vol. 509 (2011), pp. 2797-803.

Exhibit	Description
Ex-1036	Tom J. Savenije, <i>Photogeneration and transport of charge carriers in a porphyrin p/n heterojunction</i> , Physical Review B, Vol. 55, No. 15 (Apr. 1997), pp. 9685-92.
Ex-1037	Ümit Salan et al., <i>Synthesis, characterization, electrical and dielectric permittivity measurements of 2,9,16,23-tetra(4-ferrocenylimino-3-nitrophenoxy)phthalocyanines</i> , Journal of Porphyrins and Phthalocyanines, Vol. 10 (2006), pp. 1263-70.
Ex-1038	Teresa M. Figueira-Duarte et al., <i>Pyrene-Based Materials for Organic Electronics</i> , Chemical Reviews, Vol. 111 (2011), pp. 7260-314.
Ex-1039	Chen ShuoFu et al., <i>A comprehensive consideration of bias voltage and temperature to extract the intrinsic frequency response of photodiodes</i> , Chinese Science Bulletin, Vol. 55, No. 32 (2010), pp. 3727-33.
Ex-1040	Richard S. Quimby, <i>Photonics and Lasers - An Introduction</i> (John Wiley & Sons, Inc. 2006), pp. 249-79.
Ex-1041	A. Vandenbroucke et al., <i>Influence of temperature and bias voltage on the performance of a high resolution PET detector built with position sensitive avalanche photodiodes</i> , IOP Publishing for Sissa Medialab (2012), pp. 1-30.
L-1	<i>W&Wsens Devices Inc. v. Samsung Electronics Co. Ltd. et al.</i> , Case No. 2:24-cv-00854, Excerpts from Plaintiff's Infringement Contentions (Jan. 7, 2025)

V. LEGAL STANDARDS

31. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

32. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

33. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

34. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-4, 6-8, and 10-18 of the '871 patent from the perspective of a person of ordinary skill in the art at the '871 patent's earliest claimed priority date (May 22, 2013), as described in more detail below.

35. For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability.

36. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill

37. I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

38. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Prior Art

39. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as "prior art." I understand that prior art includes patents and printed publications that existed before the earliest

claimed priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the earliest filing date.

C. Anticipation

40. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if it is not novel, including if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

D. Obviousness

41. I have been informed that under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

42. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available). I am not aware of any evidence of secondary considerations

that would support a determination of non-obviousness of the claimed subject matter in the '871 patent.

43. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the Challenged Claims is May 22, 2013. My opinions would not change if I assumed a later date of invention.

44. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

45. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

46. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

47. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to

have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

48. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

49. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

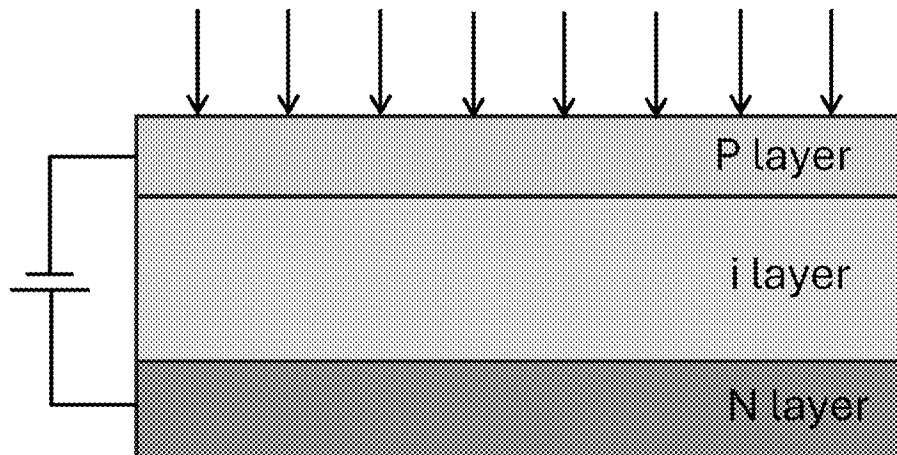
50. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is

considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. TECHNOLOGY BACKGROUND

A. Photodetectors

51. A photodetector is a semiconductor device that transforms photons into electrical signals, enabling electrical circuits to detect and measure incident light. Various types of photodetectors exist, including photodiodes and avalanche photodiodes. A PiN photodetector is a specific type of photodiode characterized by an intrinsic (undoped) layer positioned between highly doped P-type and N-type semiconductor layers (hence the name “PiN”):



52. When light enters the photodetector, the intrinsic layer absorbs photons, generating electron-hole pairs. Applying a negative bias across the photodetector causes the separated electrons to move towards the N-type layer and the holes towards the P-type layer, producing a measurable photocurrent.

B. Microstructure-Enhanced Photodetectors

53. Conventional silicon photodetectors exhibit high responsivity at wavelengths of light less than about 850 nm. Ex-1010, 1. The prior art recognized that tailoring silicon's microstructure extends photodetector operability to longer wavelengths. For instance, etching a silicon photodetector surface to create micron-sized pillars was known to enhance a photodetector's responsiveness at longer wavelengths. Ex-1010, 1-2; Ex-1011, 1-6. The images below illustrate photodiodes with laser-etched microstructures designed to enhance their responsiveness at longer wavelengths.

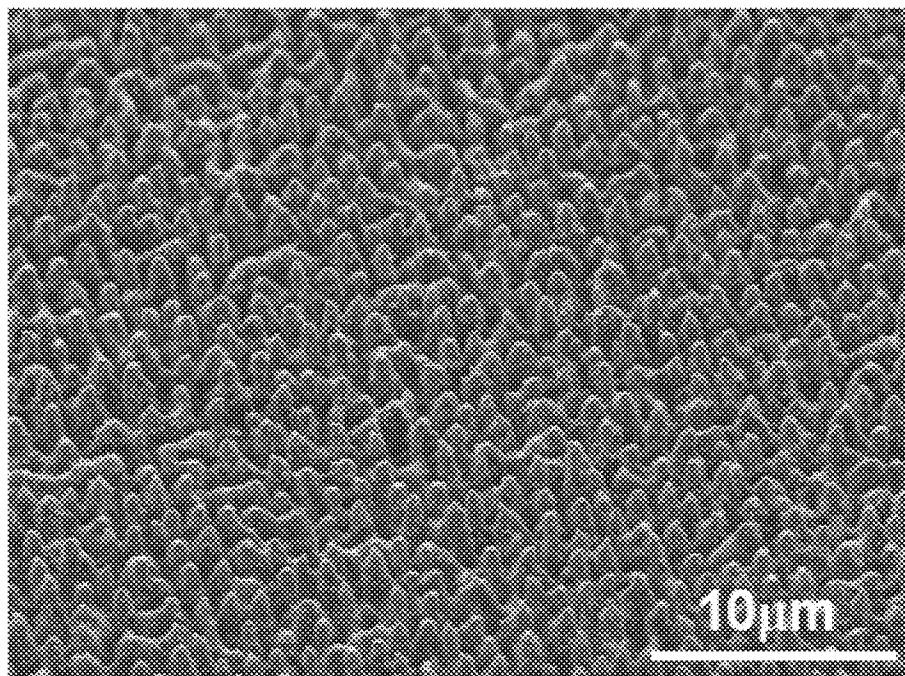


FIG. 1. Scanning electron micrographs of microstructured Si surface.

Ex-1010, 1.

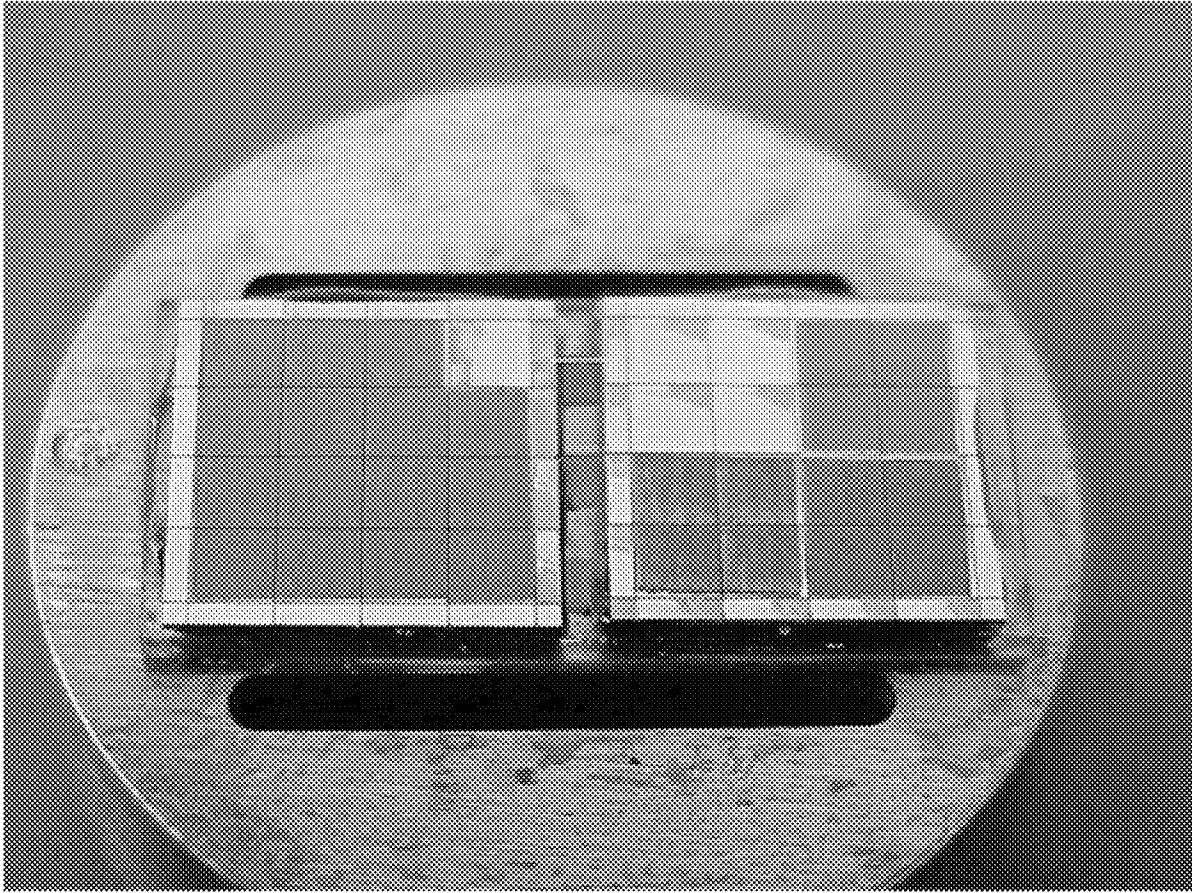


Fig. 1. (Color online) Picture of two microstructured APD arrays prior to packaging. Structuring was performed with an 800 nm fs laser operating at a fluence of 3.5 kJ/m^2 in an atmosphere of SF_6 . The array on the right had four different structured regions with a pulse number ranging from 0 to 300. The shiny area is the bare silicon.

Ex-1011, 2.

54. Photodetectors featuring microstructures enhanced by etched holes were widely known and utilized well before the purported invention. For example, *NXP* (Ex-1006) discloses a single-chip device 1300 where a silicon PIN photodiode is integrated with CMOS signal processing circuitry (not shown in Figure 13 below) on the same substrate 102. *NXP*, ¶¶[15], [32], [42], [85].

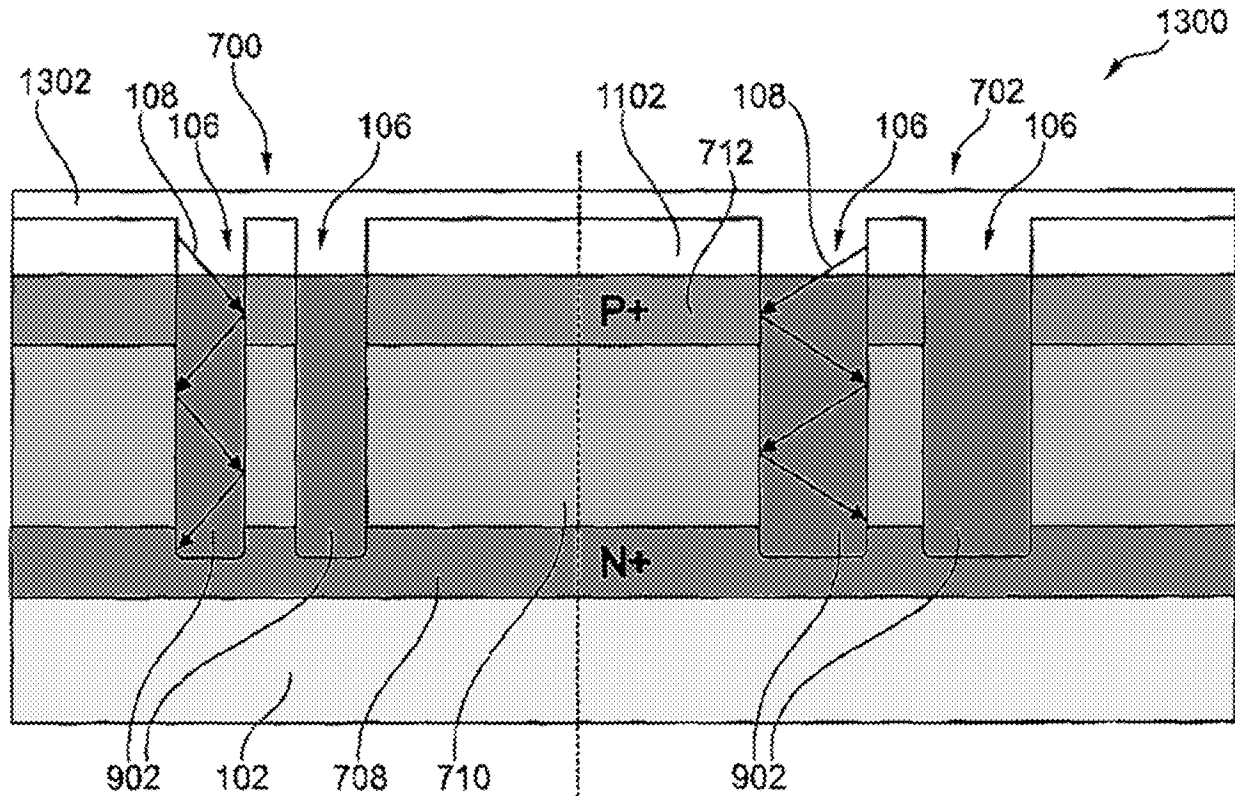


Fig. 13

NXP, Fig. 13.

55. The PiN photodiode above includes an intrinsic layer 710 disposed between an N⁺ layer 708 and a P⁺ layer 712 and holes or pores 106 formed on the PiN layers by etching. *NXP*, ¶¶[77]-[78]. *NXP* discloses that pores 106 increase the photodiode's quantum efficiency. *NXP*, ¶¶[13], [38]. Quantum efficiency is a measure of how effectively the photodiode converts incoming optical energy into electrical signals. *See* Ex-1012, 4; Ex-1013, 4.

56. As another example, *Wang* (Ex-1007) discloses a photonic device 100 comprising a PIN structure with a stacked p-semiconductor region 108, intrinsic semiconductor region 110, and an n-semiconductor region 106. *See Wang*, ¶[28], Figs. 1-2. A thin doped region 112 overlays the surface of the p-region 108, and a periodic array of holes or recesses 116 extends into the PIN structure through the overlying region 112. *Wang*, ¶¶[29]-[32].

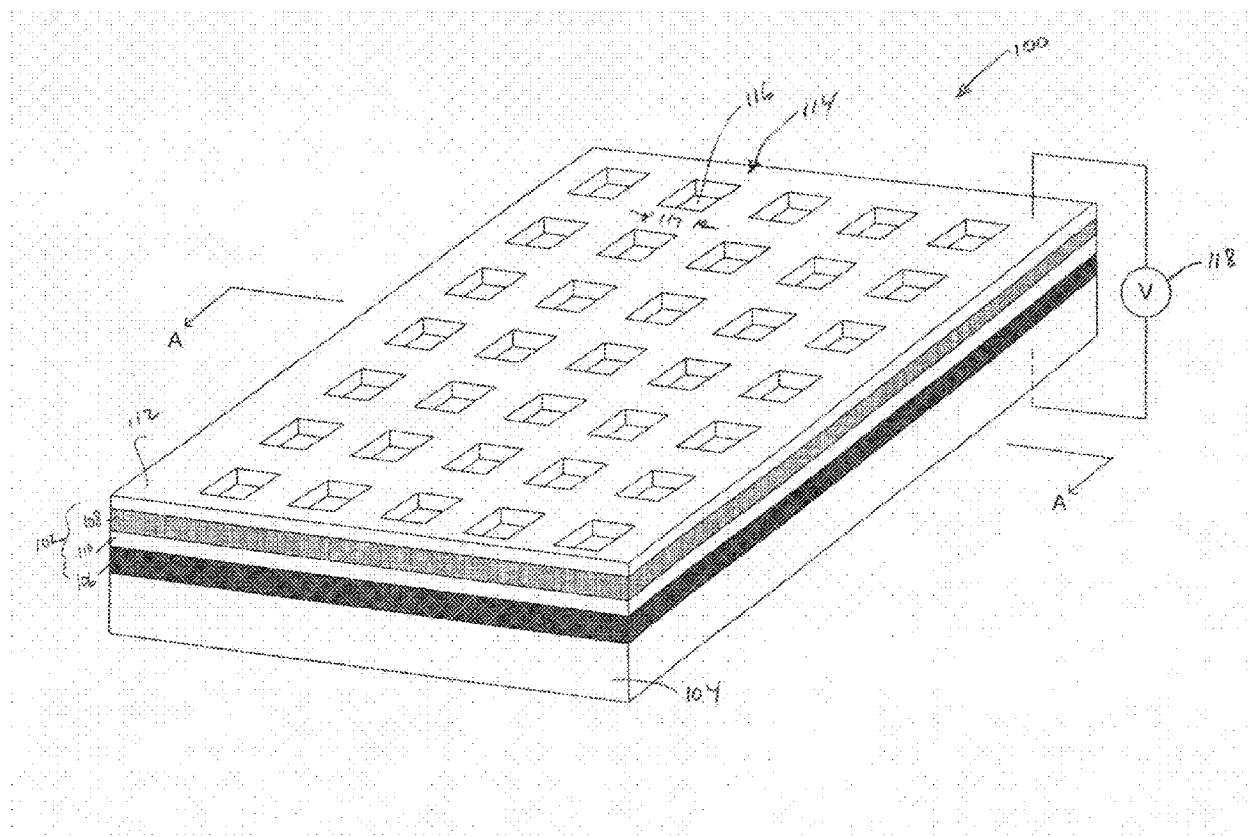
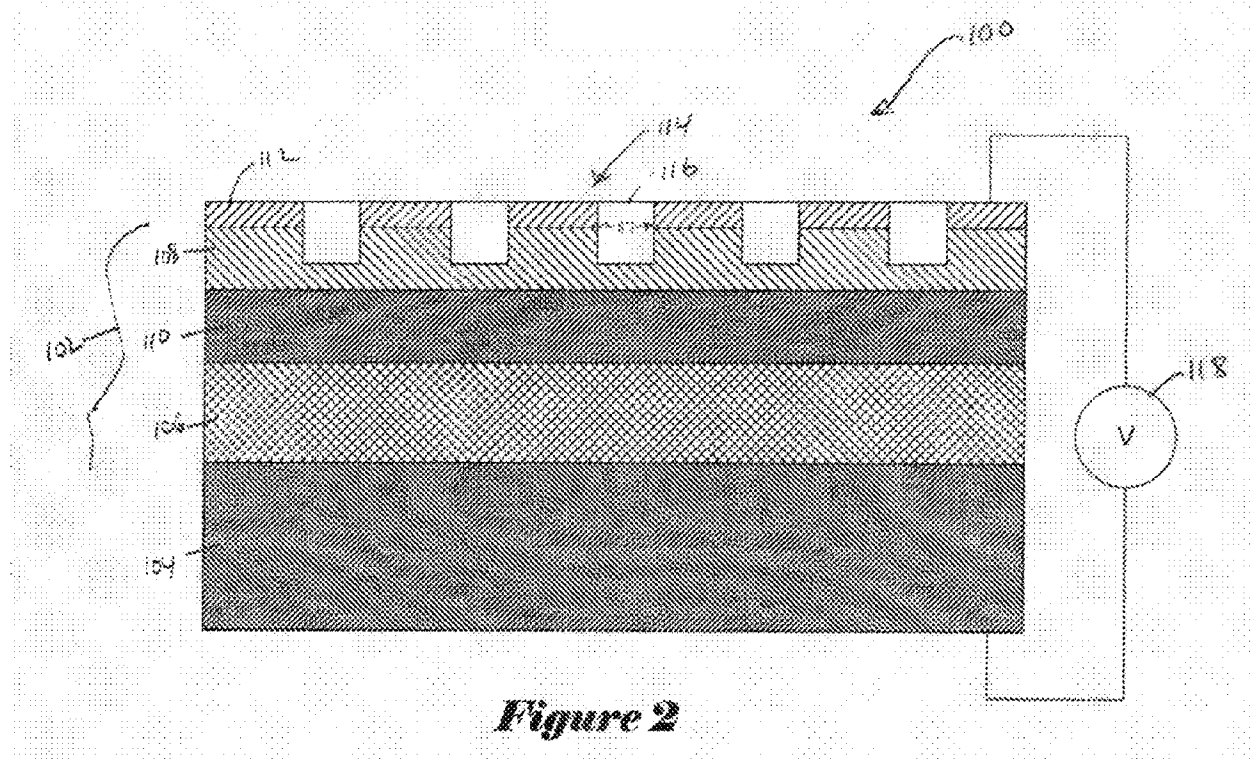


Figure 1

Wang, Fig. 1.



Wang, Fig. 2.

C. Photodetectors and Processing Circuitry on a Single Substrate

57. The integration of photodetectors and signal processing circuitry on a single substrate to form a single-chip device was known long before the purported invention date of the '871 patent. Ex-1012, 1-14; Ex-1013, 1-8; Ex-1014, 1-2. For instance, *NXP* teaches that integrating signal processing circuitry and the photodiode on the same substrate “may be more reliable than a discrete solution” and result in a smaller package, which is advantageous for mobile applications. *NXP*, ¶¶[16], [32], [37].

58. Beginning in the late 1980s, advancements in CMOS technology enabled the fabrication of both photodetectors and signal processing electronics on the same substrate. Ex-1012, 2-3, 10. For example, researchers at NASA’s Jet Propulsion Laboratory developed the CMOS active pixel sensor (“APS”), which integrated a photodiode, amplifier, and signal processing circuitry within each pixel of an image sensor. Ex-1012, 2-3. This allowed for on-

chip conversion of light to electrical signals and immediate processing. Ex-1012, 2-3; Ex-1013, 4. This CMOS APS is shown below:

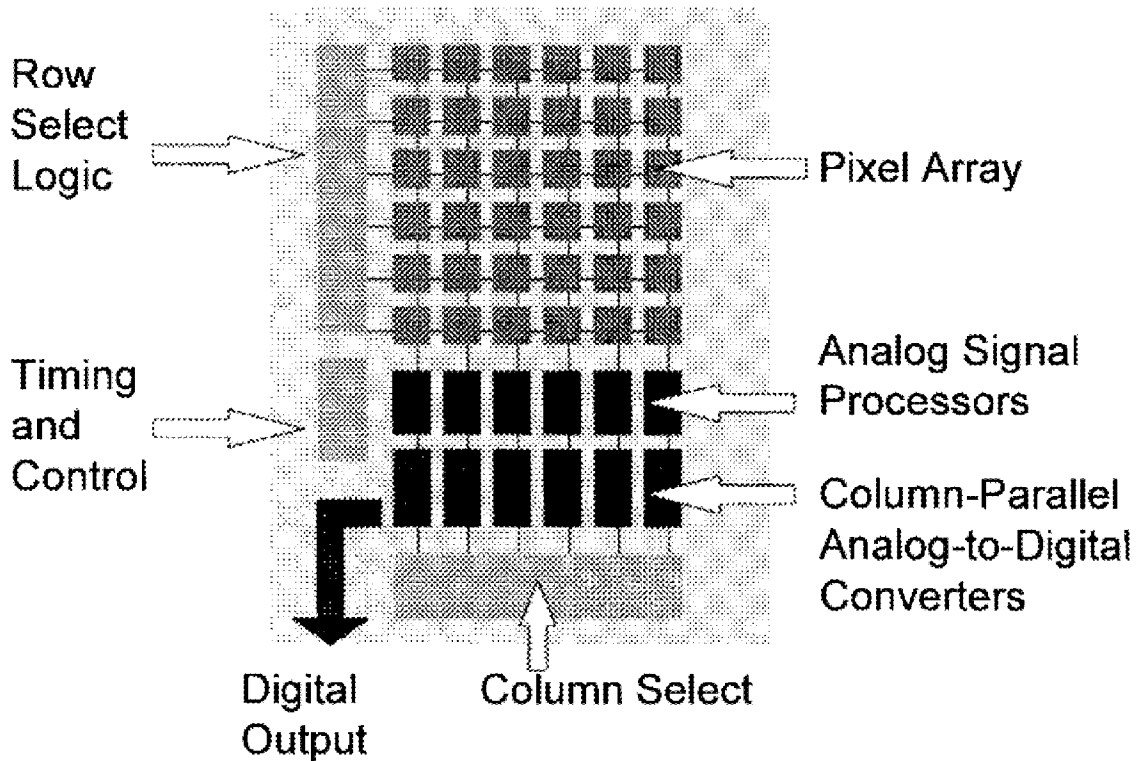
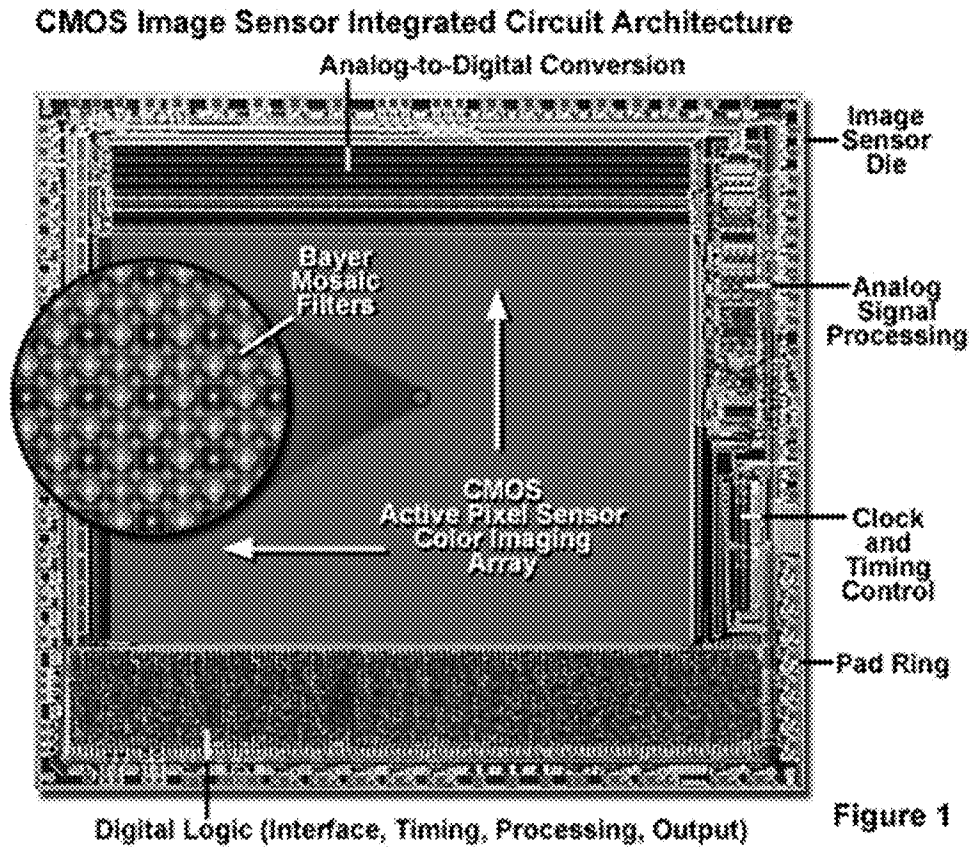


Fig. 2. CMOS APS integrates timing and control, ADC, and other circuitry on the same chip.

Ex-1013, 3.

59. The integration of the photodiode and processing circuitry on the same chip reduced power consumption, lowered manufacturing costs, and allowed for smaller, more efficient imaging devices. Ex-1012, 3, 10, 12; Ex-1013, 8.

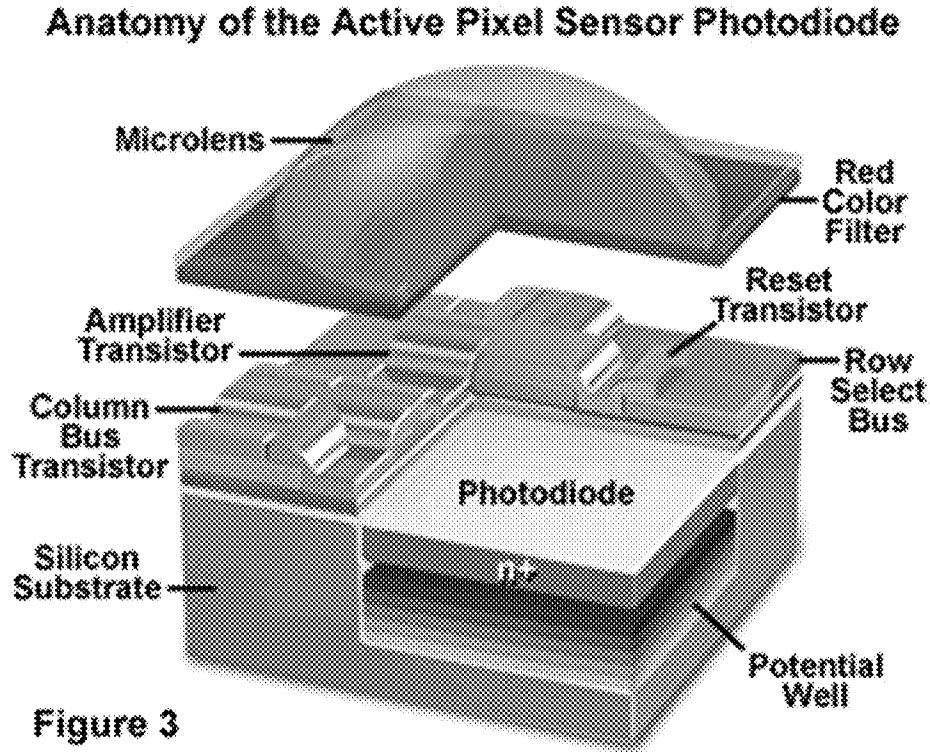
60. By the early 2000s, APS technology was prevalent in consumer electronics such as digital cameras, smartphones, and webcams. Ex-1012, 1-3; Ex-1015, 9. An image of a CMOS APS image sensor die is shown below.



Ex-1015, 1.

61. This image sensor die includes an array of photodiodes (640 x 480 pixels) located in the large reddish-brown central area of the chip and analog signal processing circuitry to collect and interpret the signals generated by the photodiode array. Ex-1015, 2-3, Fig. 1.

62. A three-dimensional cutaway drawing of the above image sensor is shown below, illustrating a single photodiode and associated transistors that process the signals produced by the photodiode on a single substrate. Ex-1015, 3-5.

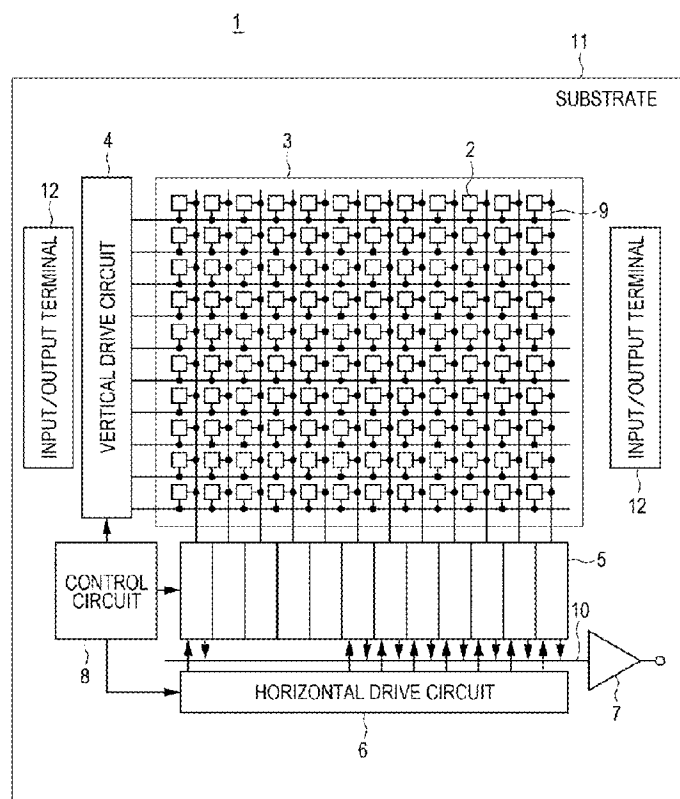


Ex-1015, 3.

63. To focus the incident light on the photodiode, the photodiode is positioned beneath a microlens and a color filter to capture color information from the incident light. Ex-1015, 3-4, Fig. 3.

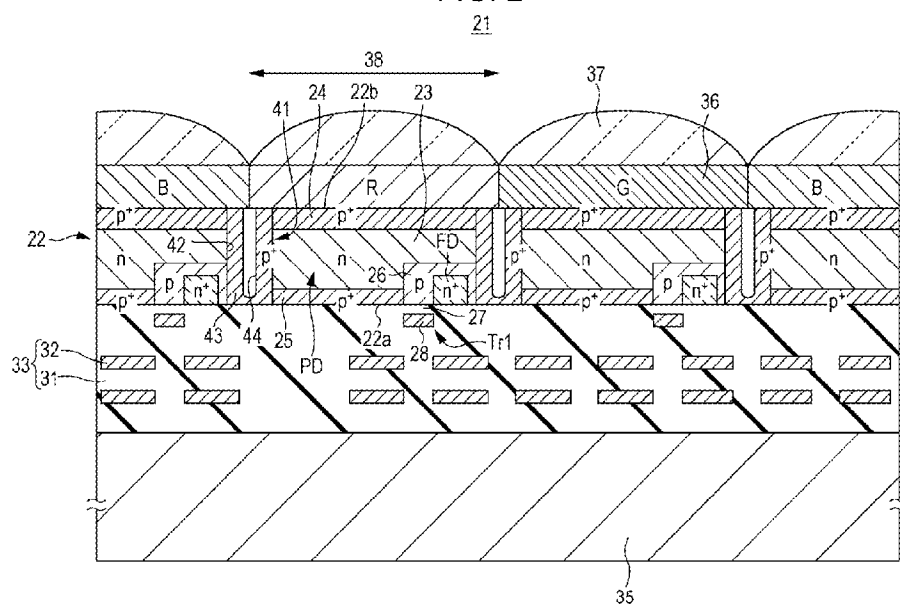
64. Well before the purported invention date of the '871 patent, numerous published references disclosed single-chip devices integrating photodetectors and signal processing circuitry on a single substrate. For example, *Kuboi* (PA-1), discussed below, describes such a device. *Infra* VIII.A. *Shinohara* (PA-2) discloses a similar single-chip device incorporating photodetectors and signal processing circuitry. See *Shinohara*, Figs. 1-2, ¶¶[51]-[63]; *infra* VIII.B.

FIG. 1



Shinohara, Fig. 1.

FIG. 2



Shinohara, Fig. 2.

65. Like *Kuboi*'s imaging device 201 (*see Kuboi*, Fig. 5, ¶¶[48]-[54]), *Shinohara*'s imaging device 1 features a pixel region 3 with a two-dimensional pixel array 2 and a peripheral circuit portion integrated on the same semiconductor substrate 11. *See Shinohara*, ¶[51]; *see infra* VIII.A. In *Shinohara*, each pixel 2 contains a photoelectric conversion portion and four pixel transistors, similar to *Kuboi*. *Shinohara*, ¶[51]; *see Kuboi*, ¶[48]; *see infra* VIII.A. Additionally, similar to *Kuboi*, *Shinohara*'s peripheral circuit portion includes various logic circuits, such as a vertical drive circuit 4, a column signal processing circuit 5, a horizontal drive circuit 6, an output circuit 7, and a control circuit 8. *Shinohara*, ¶[52]; *see Kuboi*, ¶[49]; *see infra* VIII.A. In *Shinohara*'s imaging device 1, the photodiode-based photoelectric conversion portion and pixel transistors are formed on a single semiconductor substrate (substrate 22), along with the logic circuits of the peripheral circuit portion. *See Shinohara*, ¶¶[3]-[4], [58], [81].

VII. THE '871 PATENT

A. Alleged Invention of the '871 patent

66. The '871 patent describes a photodetector that includes microstructures to enhance photoabsorption. '871 patent, 2:41-42, 3:1-5, 4:1-8, 17:25-27. The photodetectors of the '871 patent include a silicon substrate that has a first layer (P⁺ layer), a very low doped N or P layer called the intermediate layer (or I layer), and a second layer (N⁺ layer), and further includes holes etched in one or more of the PIN layers. '871 patent, 15:57-59, 16:9-35, 17:47-52. The '871 patent also discloses the photodetector can be operated in a reverse-bias mode, in which a negative voltage is applied to the anode (P⁺ layer) and a positive voltage is applied to the cathode (N⁺ layer). '871 patent, 16:40-43; *see also* '871 patent, 11:45-51. Figure 5B (below) illustrates the photodetector of the '871 patent:

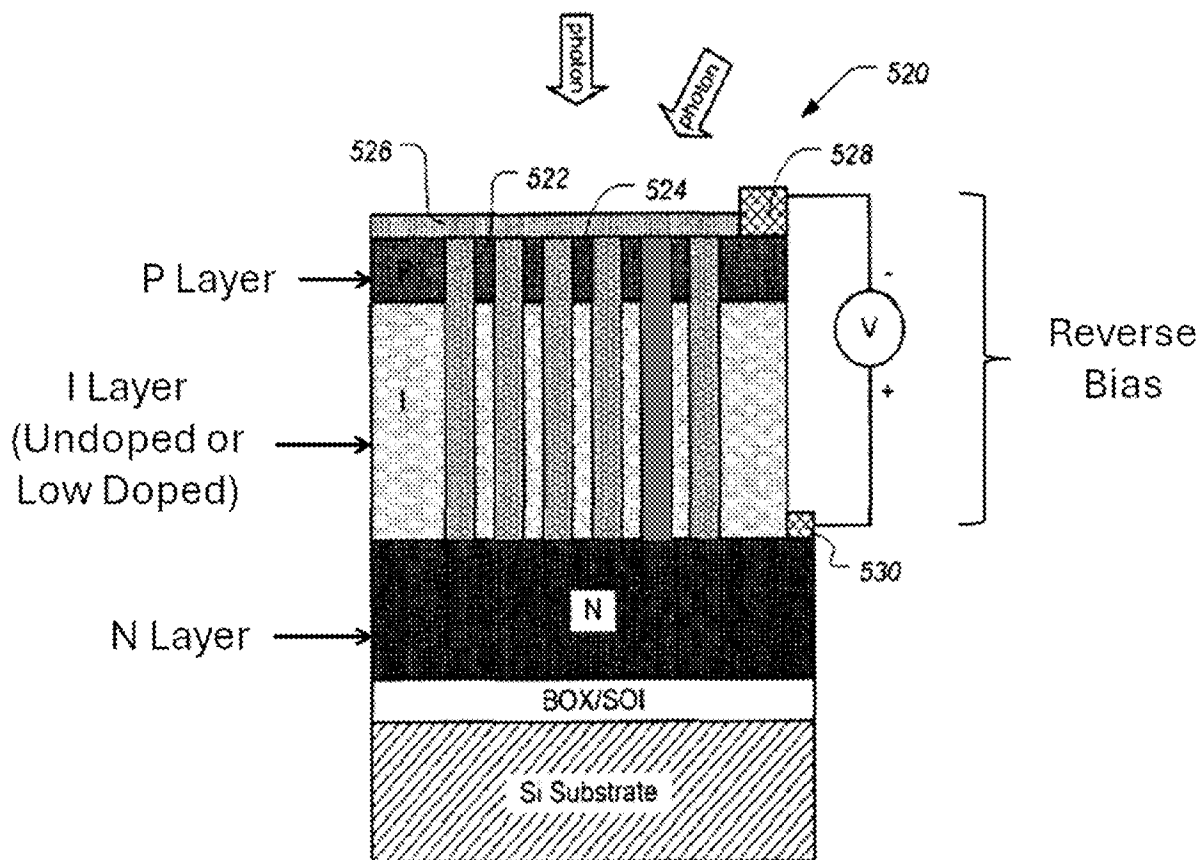


FIG. 5B

'871 patent, Fig. 5B (annotated).

67. The '871 patent discloses that optical signals or light can impinge on the light-receiving surface of the photodetector either perpendicular (normal) to the light-receiving surface or at an angle off normal. '871 patent, 16:48-49. The '871 patent discloses that one of the causes of enhancement of the absorption coefficient of the incident light includes high contrast grating (HCG) effects. '871 patent, 11:52-57. The '871 patent explains that its microstructured pillar-hole-void array can enhance the absorption coefficient of the incident light relative to the bulk absorption coefficient by a factor of 1.1 to over 100 because of the HCG effect. '871 patent, 12:49-55. According to the '871 patent, its photodetector can be integrated with ASIC (application-specific integrated circuits) such as signal processing, signal amplification, optical

waveguides, integrated optics, and other integrated circuits for specific applications. '871 patent, 10:23-27.

B. Prosecution History

68. Applicant filed U.S. Application No. 18/385,213 (“the ’213 Application”) with 12 application claims. Ex-B, 651-53. Applicant also filed a Preliminary Amendment that replaced the previously filed applications claims with new application claims 1-12. Ex-B, 470-72.

69. The Examiner issued one non-final office action objecting to application claim 1 and rejecting all application claims 1-12 under 35 U.S.C. § 112. Ex-B, 412-16. In response, Applicant canceled application claims 1-12 and presented new application claims 13-30. Ex-B, 121-23. The Examiner allowed application claims 13-30 stating that “the integrated structure as recited in the claims of the instant invention fail to be taught by the prior art cited of interest.” Ex-B, 58, 67. However, as I explain in detail below, *Kuboi* or *Yu* in view of *Shinohara* discloses the very features the Examiner found patentable.

C. Claim Construction

70. I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures (Ex-A), and the patent’s prosecution history (Ex-B)—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent. I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term’s plain and ordinary

meaning. That special definition or limitation on scope may be provided in the patent's written description, the patent's prosecution history, or both.

71. I understand that claim interpretation may also be informed by "extrinsic evidence" (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the art (POSITA) in the relevant time period.

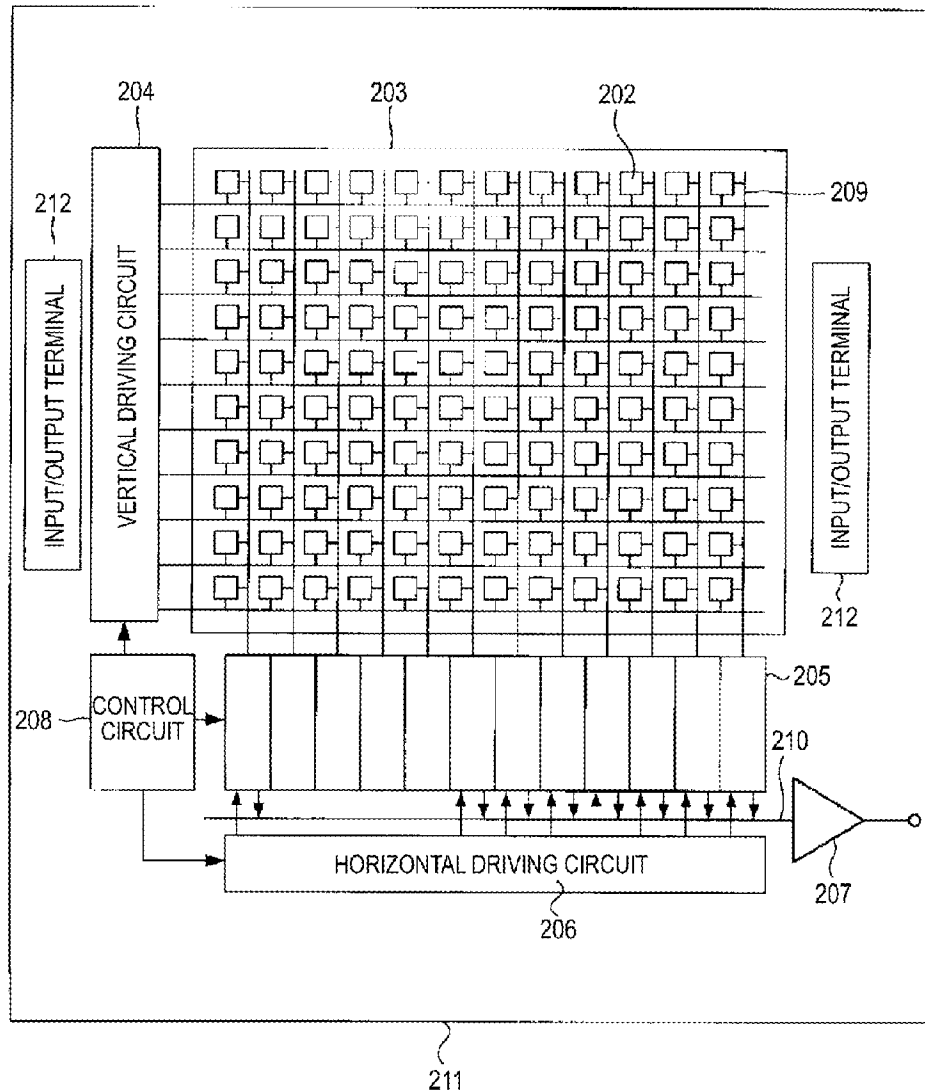
72. I have been asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '871 patent. Based on my review of the materials and my personal knowledge and experience, I have considered each term of the '871 patent as it would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '871 patent (May 22, 2013).

VIII. SUMMARY OF THE PRIOR ART

A. *Kuboi*

73. *Kuboi* is titled Solid-State Imaging Device, Manufacturing Method Thereof, and Electronic Apparatus, was filed on August 19, 2011, and published as U.S. Patent Application Publication No. 2012/0049044 (PA-1) on March 1, 2012. I understand that *Kuboi* is prior art to the '871 patent.

74. *Kuboi* discloses a complementary metal oxide semiconductor (CMOS) imaging device 201 that includes a pixel region 203 and a peripheral circuit portion formed on a single semiconductor substrate 211. *Kuboi*, ¶[48], Fig. 15. *Kuboi*'s imaging device is illustrated below.

FIG.15201*Kuboi*, Fig. 15.

75. According to *Kuboi*, and as shown in the above figure, pixel region 203 of substrate 211 includes a number of pixels 202 that are arranged in a two-dimensional array. *Kuboi*, ¶[48]. Each pixel 202 contains one photoelectric conversion portion (or a photodiode) and four pixel transistors. *Kuboi*, ¶[48]. *Kuboi* also discloses that the peripheral circuit portion includes logic circuits (such as a vertical driving circuit 204, column signal processing circuits

205, horizontal driving circuit 206, output circuit 207, and control circuit 208), which process the pixel's electrical signals and then output the processed electrical signals. *Kuboi*, ¶¶[49]-[54].

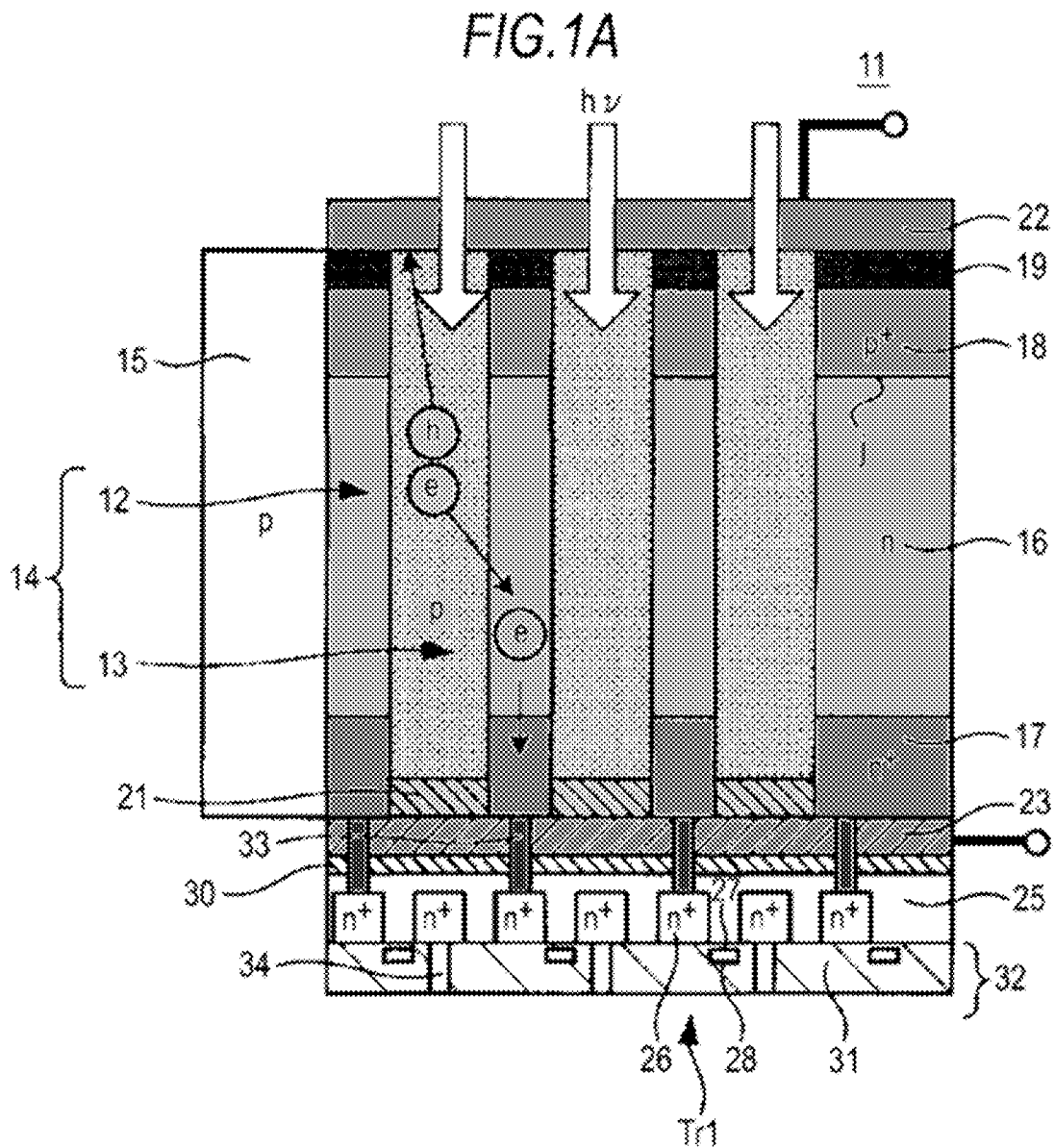
Kuboi discloses that the pixels and peripheral circuit portion are fabricated on one single substrate, the pixel transistors are fabricated on another substrate, and then two substrates are bonded together. *Kuboi*, ¶¶[62], [70], [78].

76. *Kuboi* describes photoelectric conversion portions suitable for use in the imaging device 201 shown in Figure 15. *Kuboi*, ¶[48]. For example, *Kuboi* discloses a basic pixel configuration for its imaging device with reference to Figures 1A/1B. *Kuboi*, ¶[55]. Similarly, *Kuboi* discloses a pixel configuration with reference to Figures 6A/6B, and explains that the disclosed red and green pixels 53R and 53G of Figures 6A/6B have a structure that is the same as the basic configuration of Figures 1A/1B. *Kuboi*, ¶¶[90], [95], [69]. *Kuboi* explains that Figure 13 includes pixels 53R, 53G, and 53B, having configurations that are the same as the pixels of Figures 1A/1B. *Kuboi*, ¶[181]. Similarly, *Kuboi* describes its Figure 15 as being applicable to all of *Kuboi*'s pixel configurations. *Kuboi*, ¶¶[35], [48]. With reference to its Figures 4A-4F, *Kuboi* discloses a method of manufacturing the basic pixel configuration of Figures 1A/1B. *Kuboi*, ¶¶[69]-[76].

77. In my opinion, based on *Kuboi*'s disclosure, a person of ordinary skill in the art would have recognized that the different pixels described by *Kuboi* and illustrated in its Figures 1A/1B, 6A/6B, 13, and 15 all disclose the pixel configuration of the same imaging device. Further, in my opinion, Figures 4A-4F of *Kuboi* and the associated description disclose methods of manufacturing that same pixel configuration. Accordingly, throughout this declaration, references to disclosures associated with Figures 1A/1B, 4A-4F, 6A/6B, 13, and 15 are deemed to be representative of the pixel configuration of the same imaging device 201. In addition, in my

opinion, a person of ordinary skill in the art would have found it obvious to combine the elements illustrated and disclosed with Figures 1A/1B, 4A-4F, 6A/6B, 13, and 15.

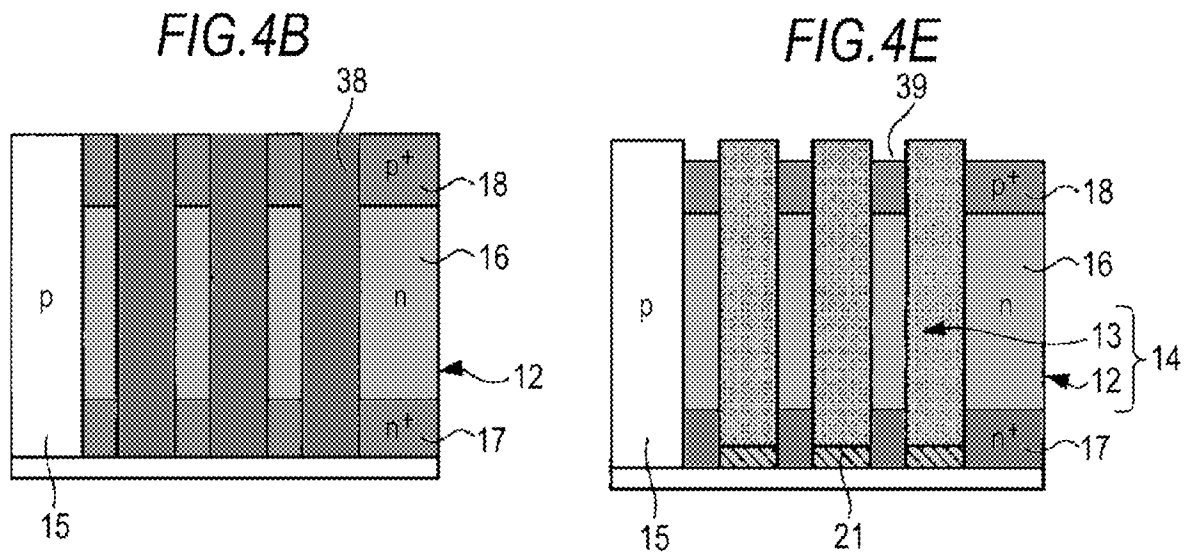
78. *Kuboi* discloses that pixel 11, including photoelectric conversion portion 14, can be utilized in imaging device 201. *Kuboi*, ¶¶[48], [55]. Figure 1A of *Kuboi*, illustrating a photoelectric conversion portion 14 in a pixel 11, is shown below. *Kuboi*, ¶¶[48], [55]-[56].



Kuboi, Fig. 1A (shaded).

79. *Kuboi* discloses that photoelectric conversion portion 14 comprises a silicon semiconductor layer 12 that includes multiple embedded organic material layers 13. *Kuboi*, ¶[55]. *Kuboi*'s silicon semiconductor layer 12 is implanted with different impurities (or doped) to form an n-type semiconductor (or "intermediate") region 16 with a p⁺ type semiconductor region 18 on one side and an n⁺-type semiconductor region 17 on the opposite side (i.e., stacked PIN regions). *Kuboi*, ¶¶[56], [71]. *Kuboi* discloses that the doping of layer 12 is such that region 18 and region 17 have a higher concentration of impurities than region 16. *Kuboi*, ¶[56].

80. *Kuboi* explains that after forming regions 18, 16, and 17, vertical holes 38 extending from p⁺ type region 18 to n⁺-type region 17 are etched into the PIN regions (illustrated in *Kuboi*'s Figure 4B, below, left). *Kuboi*, ¶¶[71]-[72]. *Kuboi* further discloses that after forming holes 38, the organic material that forms photoelectric conversion films 13 is deposited in holes 38 (illustrated in *Kuboi*'s Figure 4E, below, right). *Kuboi*, ¶¶[72]-[73].



Kuboi, Figs. 4B (left) (shaded), 4E (right) (shaded).

81. According to *Kuboi*, a metal shielding film 19 is applied to the surface of region 18 such that only holes 38 containing films 13 are exposed to incident light (hν). *Kuboi*,

¶¶[59], [72], [73], [76], Figs. 1A, 4F. Further, *Kuboi* discloses that an upper electrode 22 and a lower electrode 23 are formed on opposite sides of the PIN regions. *Kuboi*, ¶[60]. *Kuboi* discloses that a reverse bias is applied to electrodes 22 and 23. *Kuboi*, ¶[64]. Specifically, *Kuboi* discloses that a “necessary voltage is applied between the upper electrode 22 and the lower electrode 23 so that the upper electrode 22 has the negative potential, and the lower electrode 23 has the positive potential.” *Kuboi*, ¶[64].

82. *Kuboi* explains that photoelectric conversion of the incident light (hv) occurs within films 13 (inside holes 38) and results in generation of electron-hole pairs. *Kuboi*, ¶[64]. *Kuboi* discloses that the generated electrons move from the photoelectric conversion film 13 toward the depleted semiconductor layer 12 into a charge accumulation region 26 of the transfer transistor (Tr1) of the corresponding pixel 11 (via conductors 33). *Kuboi*, ¶¶[62], [64], [73]. *Kuboi* also discloses that the holes move toward upper electrode 22 through photoelectric conversion film 13. *Kuboi*, ¶[64]. *Kuboi* explains that after initial signal processing (e.g., amplification) by the pixel transistors, the electrical signals from the pixel 11 are sent to the peripheral circuit portions for further processing. *Kuboi*, ¶¶[48]-[49], [61]-[62].

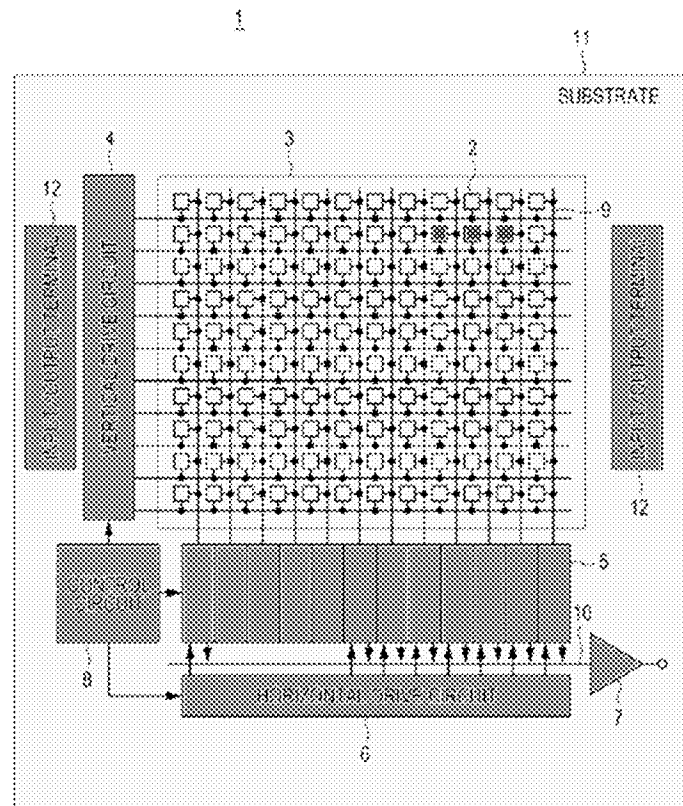
B. *Shinohara*

83. *Shinohara* is titled Solid-State Imaging Device, Manufacturing Method Thereof, and Electronic Apparatus, was filed on August 2, 2011, and published as U.S. Patent Application Publication No. 2012/0033119 on February 9, 2012. I understand that *Shinohara* is prior art to the '871 patent.

84. *Shinohara* discloses “a solid-state imaging device which suppresses the generation of white spots and dark current and the occurrence of color mixture and which improves the sensitivity.” *Shinohara*, ¶¶[13], [51]. Specifically, *Shinohara* discloses a solid-state

imaging device 1 that includes a pixel region (so-called imaging region) 3 and a peripheral circuit portion. *Shinohara*, ¶[51]. *Shinohara* explains that in its pixel region, a plurality of pixels 2 are arranged in a semiconductor substrate 11, such as a silicon substrate, in a two-dimensional matrix. *Shinohara*, ¶[51]. *Shinohara* also discloses that each of its pixels 2 includes a photoelectric portion. *Shinohara*, ¶[51]. Further, *Shinohara* discloses that [t]he peripheral circuit portion includes so-called logic circuits, such as a vertical drive circuit 4, a column signal processing circuit 5, a horizontal drive circuit 6, an output circuit 7, and a control circuit 8.” *Shinohara*, ¶[52]. *Shinohara*’s imaging device including these features is illustrated below:

FIG. 1

*Shinohara*, Fig. 1 (shaded).

85. *Shinohara* discloses that its photodiode PD includes a first conductivity type that functions as both photoelectric conversion and charge storage. *Shinohara*, ¶[58]. *Shinohara*

explains that the first conductivity type can be an n-type charge storage region 23. *Shinohara*, ¶[58]. *Shinohara* discloses that its PD also includes second conductivity types, for example, p-type semiconductor regions 25 and 24. *Shinohara*, ¶[58].

86. *Shinohara* also discloses a method for manufacturing the imaging device on a p-type silicon semiconductor substrate 22. *Shinohara*, ¶[68]. For example, *Shinohara* discloses forming an n-type semiconductor region 52, in a region corresponding to the pixel region, by ion-implanting an n-type impurity 51. *Shinohara*, ¶[69]. *Shinohara* discloses forming a trench 42 corresponding to the element isolation region and filling trench 42 with a p-type semiconductor region by epitaxial growth so as to form void 44 in trench 42. *Shinohara*, ¶[71]. *Shinohara* also discloses filling void 44 with an insulating film 69. *Shinohara*, ¶[91].

87. *Shinohara* discloses forming the p-type semiconductor well region 26 in a part of the n-type semiconductor region 52 at a surface side corresponding to each pixel isolated by the element isolation region 41. *Shinohara*, ¶[81]. Further, *Shinohara* discloses forming the floating diffusion portion FD in the p-type semiconductor well region 26 by an n-type semiconductor region. *Shinohara*, ¶[81]. *Shinohara* also discloses, forming the transfer gate electrode 28 transfer transistor Tr1 and other pixel transistors such as a reset transistor Tr2, an amplification transistor Tr3, and a selection transistor Tr4, in the p-type semiconductor well region 26.

Shinohara, ¶[81].

88. *Shinohara* discloses forming the multilayer wiring layer 33 with a plurality of layers of the wires 32 disposed with at least one interlayer insulating film 31 on the surface of the semiconductor substrate 22. *Shinohara*, ¶[82]. Subsequently, the rear surface 22b of the semiconductor substrate 22 is formed as a light-receiving surface, and the p-type semiconductor region 24 which forms the photodiode PD is formed in the rear surface 22b. *Shinohara*, ¶[85]. In

my opinion, a person of ordinary skill in the art would have understood from *Shinohara's* disclosure that the pixel region, the multilayer wiring, and the pixel transistors in *Shinohara's* imaging device are monolithically formed on a single substrate.

C. Yu

89. *Yu* is titled Vertically Structured Passive Pixel Arrays and Methods for Fabricating the Same, was filed on December 21, 2010, and published as U.S. Patent Application Publication No. 2012/0153124 (PA-3) on June 21, 2012. I understand that *Yu* is prior art to the '871 patent.

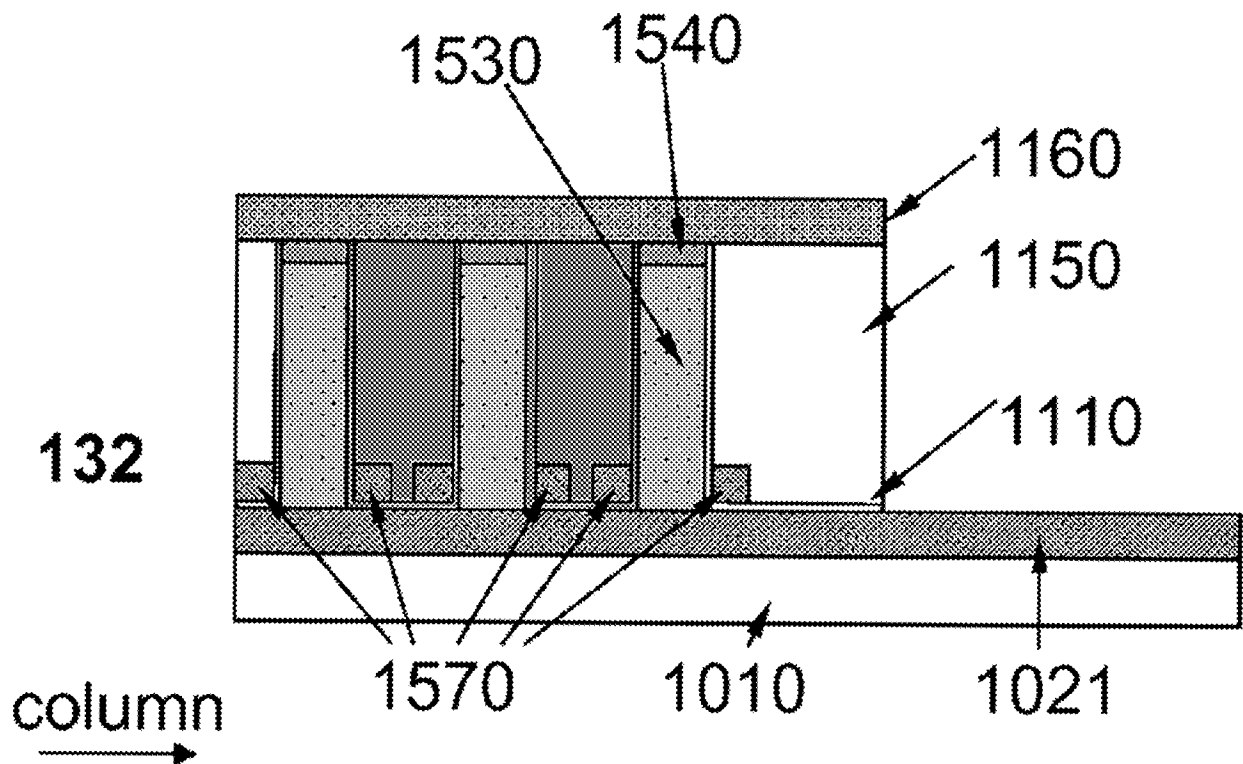
90. *Yu* discloses an image sensor that includes pixels having at least one nanopillar adapted to convert light to electrical signals. *Yu*, Abstract, ¶[48]. According to *Yu*, the “image sensor and the control circuit can be formed as an integrated circuit or chip.” *Yu*, ¶[115].

91. *Yu* discloses that the image sensor's pixels may include different size nanopillars. *Yu*, ¶[124]. For example, *Yu* discloses a three-nanopillar pixel and a four-nanopillar pixel. *Yu*, ¶[130]; Figs. 7A-7B. *Yu* further discloses that “the pixels are organized into a plurality of ‘rows’” and the “pixels can be organized into a plurality of ‘columns.’” *Yu*, ¶¶[51], [9], [17], [25], [48].

92. *Yu* discloses that “the nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si.” *Yu*, ¶¶[55], [27]. *Yu* discloses that its “substrate has an oxide layer 1010, a heavily doped layer (HDL) 1020 on the layer 1010 and an epi layer 1030 on the HDL layer 1020.” *Yu*, ¶[62]. *Yu* explains that the “substrate can have the following doping profiles: (i) the HDL layer 1020 is p+ (i.e. heavily doped to p type), the epi layer 1030 is p− (i.e. lightly doped to p type); [and] (ii) the HDL layer 1020 [is] p+, the epi layer 1030 is i (i.e., intrinsic).” *Yu*, ¶[62]. *Yu* further explains that the “epi layer 1030 can be about 3000 to 10000 nm thick.” *Yu*, ¶[62]. *Yu* discloses that “a junction layer 1040 is formed on

the epi layer 1030,” and that “junction layer 1040 is of the opposite conduction type as the HDL layer 1020, i.e., if the HDL 1020 is p type, the junction layer 1040 is n type.” *Yu*, ¶[63]. *Yu* discloses that “the exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500.” *Yu*, ¶[68], [76]. The deep etching produces holes between adjacent nanopillars.

93. *Yu* explains that the “portion of the metal layer 1140 deposited around the lower end of the nanopillars 1500 forms the gate electrodes and gate lines 1570.” *Yu*, ¶[85]. Further, *Yu* discloses that “a transparent conductive layer (TCL) 1160, such as ITO or aluminum doped zinc oxide (AZO) is deposited by a suitable technique such sputtering.” *Yu*, ¶[89], [27], [53]. These features of *Yu*’s pixel are illustrated below, including holes (shown in orange).



Yu, Fig. 1, step 132 (shaded).

94. Yu also discloses “a silicon-on-insulator (SOI)-type substrate or silicon-on-glass (SG)-type substrate.” Yu, ¶¶[62], [15], [102].

IX. LEVEL OF ORDINARY SKILL IN THE ART

95. In rendering the opinions set forth in this declaration, I have been asked to consider the '871 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as “one skilled in the art,” “skilled artisan,” “POSITA,” or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

96. Taking the factors described in the Legal Standards – Level of Ordinary Skill section into consideration, it is my opinion that a person of ordinary skill in the art pertinent to the '871 patent (May 22, 2013) would have had at least a master's degree in electrical engineering or a similar field and at least five years of experience working with semiconductor systems and semiconductor devices. Additional relevant work experience can compensate for less education, and *vice versa*.

97. As I discussed in the Qualifications and Background section, I received a Ph.D. in Electrical and Electronic Engineering in 1987 and a Doctor of Engineering degree (D.Eng) in electrical and electronic engineering in 2004, both well before the earliest priority date, May 22, 2013, of the '871 patent. As I also discussed there, I have over 40 years of experience in working with semiconductor systems and semiconductor dice. I also have additional work experience in imaging devices, photonics, and optics, as outlined in the Qualifications and Background section. Accordingly, I was at least a person of ordinary skill in the art as of May 22, 2013.

X. GROUNDS OF UNPATENTABILITY

98. Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art, it is my opinion that claims 1-4, 6-8, and 10-18 of the '871 patent would have been obvious to one of ordinary skill in the art.

99. In particular, it is my opinion that claims 1-4, 6-8, and 10-18 of the '871 patent would have been obvious to a person of ordinary skill in the art based on the prior art shown below:

Ground	Challenged Claims	Basis	Prior Art
1	1-4, 6-8, 10-16, and 18	§ 103	<i>Kuboi</i>
2	1-4, 6-8, 10-16, and 18	§ 103	<i>Kuboi</i> and <i>Shinohara</i>
3	1-4, 7, 8, 15, 17, and 18	§ 103	<i>Yu</i> , <i>Kuboi</i> , and <i>Shinohara</i>

XI. THE CHALLENGED CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

100. In my opinion, claims 1-4, 6-8, and 10-18 of the '871 patent would have been obvious to one skilled in the art as of the earliest priority date (May 22, 2013) of the '871 patent.

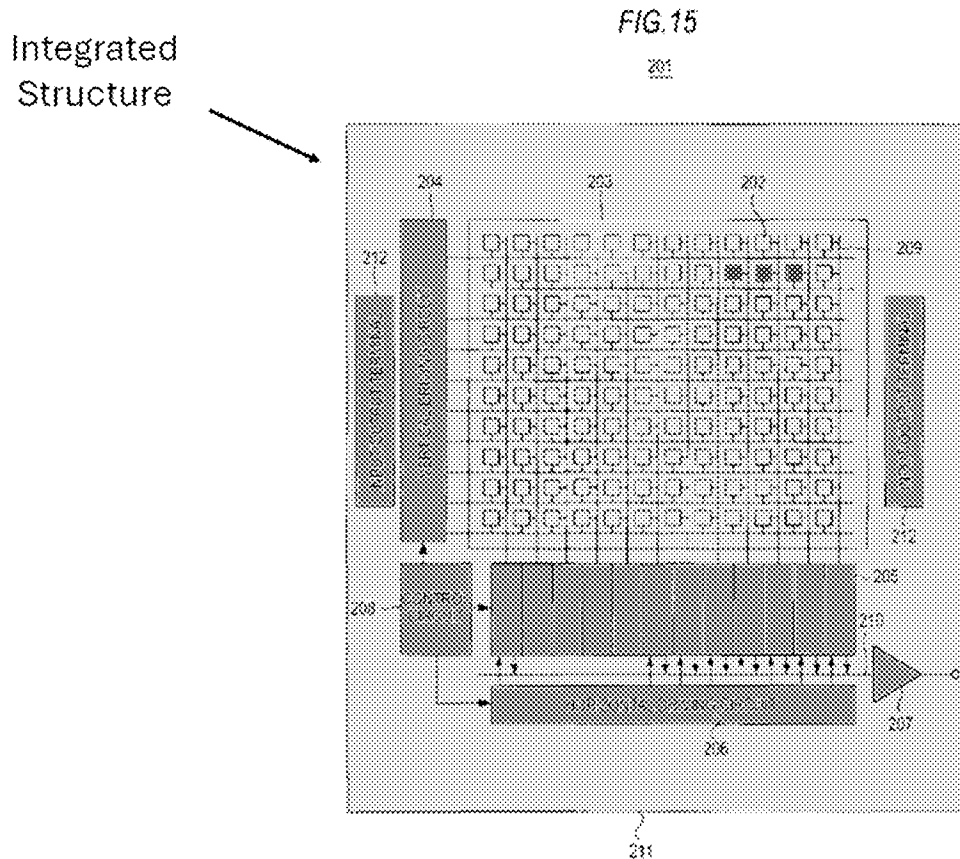
A. Claims 1-4, 7, 12, 14, 15, and 18 are Obvious Over *Kuboi* (Ground 1)**1. Independent Claim 1****a. [1pre]: “An integrated structure comprising:”**

101. In my opinion, to the extent the preamble limits the scope of claim 1, *Kuboi* discloses the preamble.

102. *Kuboi* discloses a CMOS imaging device 201 that includes a pixel region 203 and a peripheral circuit portion on a single semiconductor substrate 211. *Kuboi*, ¶[48]. *Kuboi* discloses that pixel region 203 of substrate 211 comprises a plurality of pixels 202, each of

which contains a photoelectric conversion portion. *Kuboi*, ¶[48]. *Kuboi* also discloses that the pixels and peripheral circuit portion are fabricated on a single substrate. *Kuboi*, ¶¶[70], [78].

103. *Kuboi*'s imaging device is an "integrated structure" because it combines various structures, including for example, pixels with photoelectric conversion portions and peripheral electric circuits. *Kuboi*'s integrated structure is illustrated below:



Kuboi, Fig. 15 (annotated).

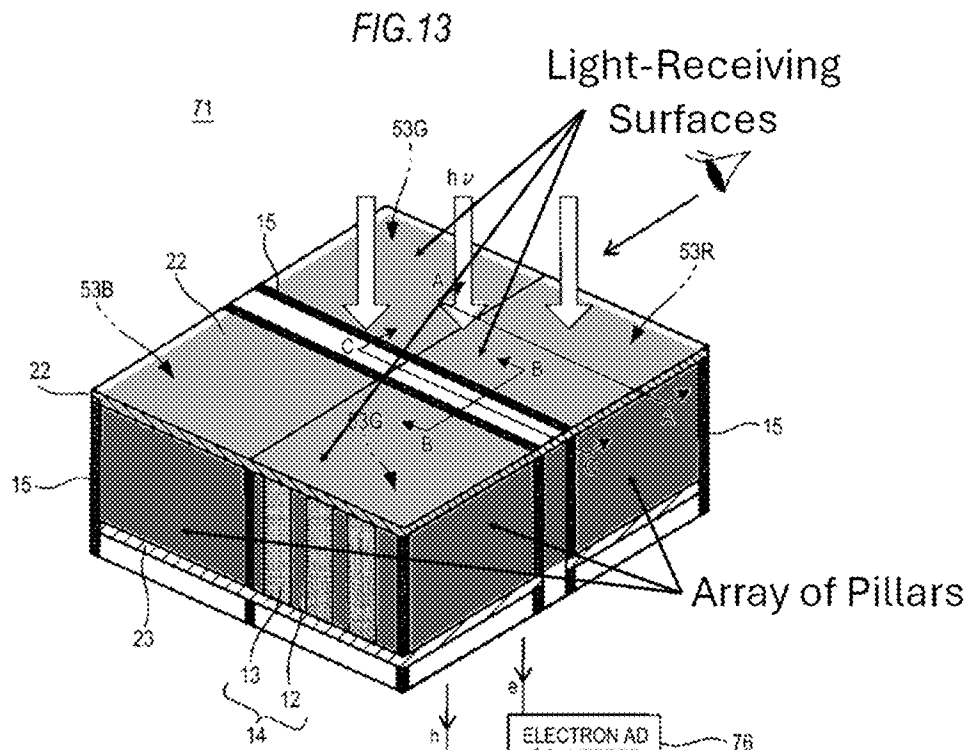
- b. [1a]: "an array of pillars comprising Si, Ge, and/or SiGe alloy semiconductor material wherein at least some of the pillars are configured as photodetectors that have respective light-receiving surfaces and have sides;"

104. In my opinion, *Kuboi* discloses this limitation.

105. For example, *Kuboi* discloses that the pixel region of its imaging device includes "a plurality of pixels 202 which include a photoelectric conversion portion and which are

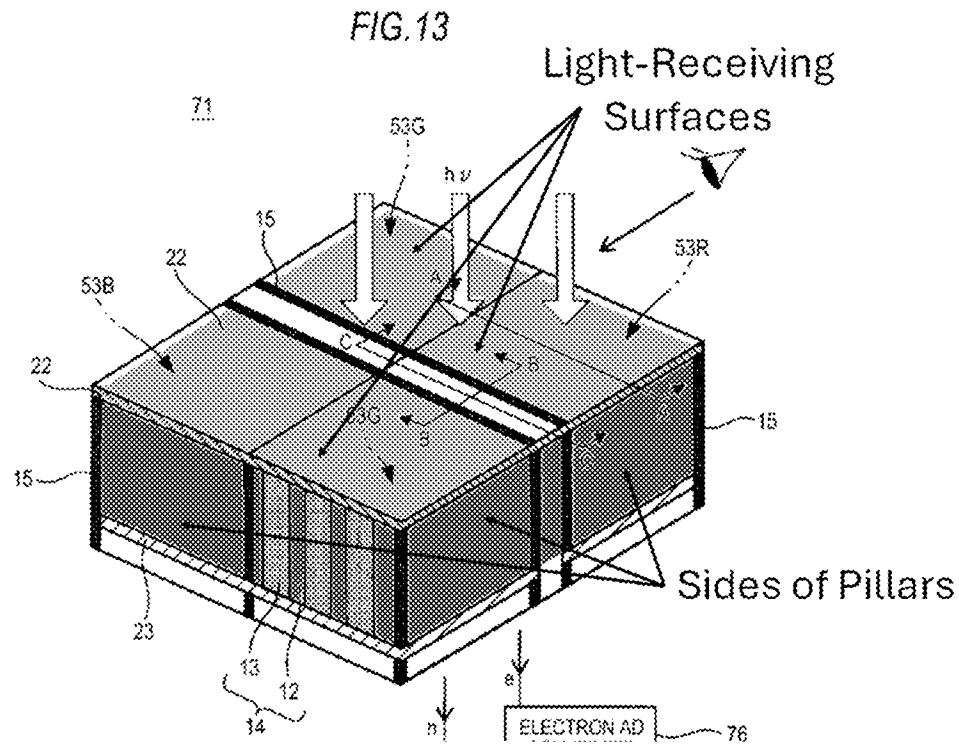
regularly arranged in a two-dimensional array.” *Kuboi*, ¶[48]. *Kuboi* discloses that its imaging device includes “red, blue, green, and green pixels ... arranged in a two-dimensional array.” *Kuboi*, ¶[181], [90]. In my opinion, one skilled in the art would have understood that *Kuboi*’s array of pixels constitutes an array of pillars.

106. *Kuboi* also discloses: “Light $h\nu$ enters the p-type organic photoelectric conversion films 13” of *Kuboi*’s pixels. *Kuboi*, ¶[186], [64]. *Kuboi* discloses that “upper electrode 22 on the light incident side is formed of a transparent electrode.” *Kuboi*, ¶[93]. Because electrode 22 is on the light incident side, one skilled in the art would have understood that the light incident side (i.e., “light-receiving surfaces”) of *Kuboi*’s pixels (i.e., pillars) would be located on the lower surface of upper electrode 22. As illustrated in the figures below, in my opinion, each pixel constitutes a pillar in the two-dimensional array and light $h\nu$ is incident on and enters via each pixel’s light-receiving surface.

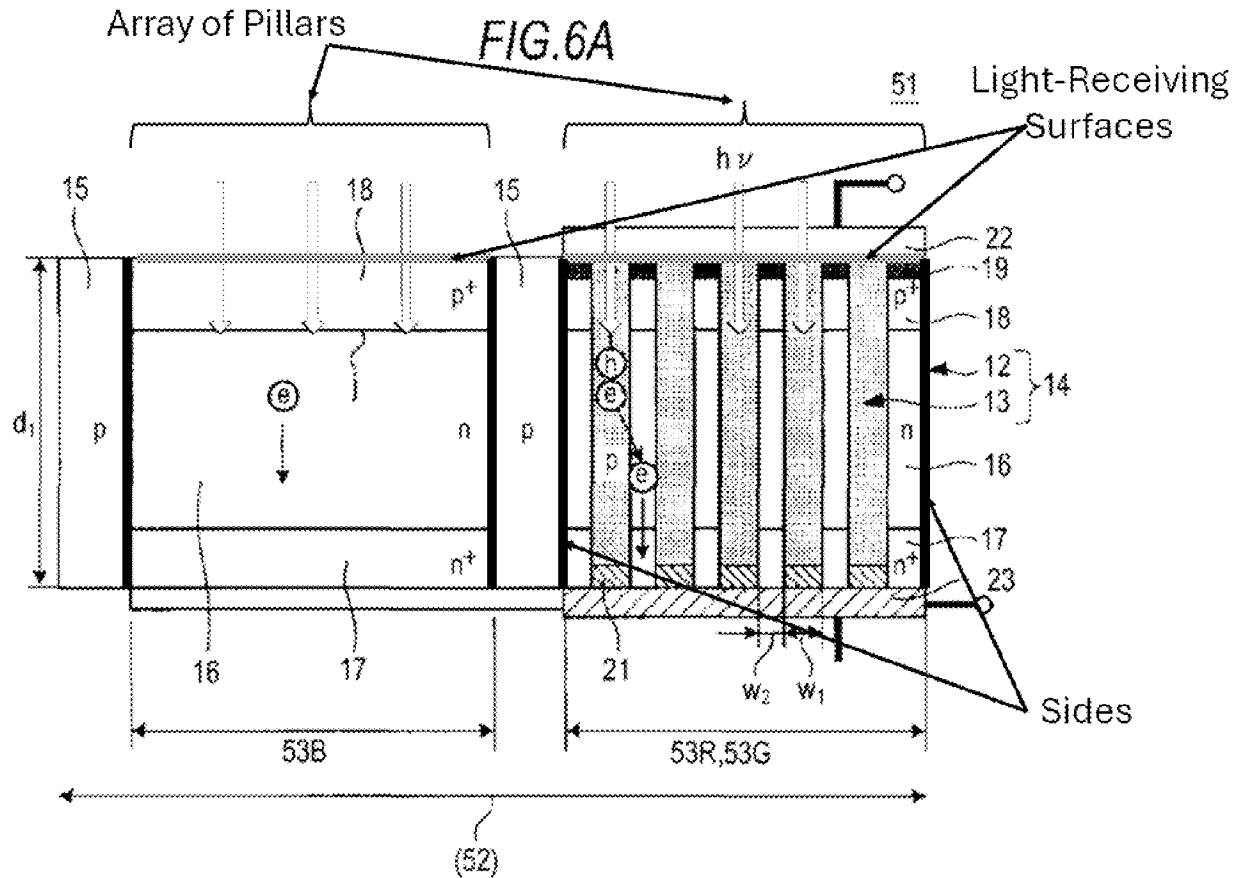


Kuboi, Fig. 13 (annotated).

107. As further illustrated below, *Kuboi*'s pixels (i.e., pillars) have sides.



108. A cross-sectional view of *Kuboi*'s array of pillars illustrating these features is also shown below.



Kuboi, Fig. 6A (annotated).

109. *Kuboi* discloses that “the blue pixel 53B is formed by a photoelectric conversion portion which is formed of a photodiode PD formed in a silicon semiconductor region, and the red pixel 53R, the green pixel 53G, and the green pixel 53G are formed by the hybrid photoelectric conversion portion 14 shown in FIGS. 1A and 1B.” *Kuboi*, ¶[90]; *see also Kuboi*, ¶¶[48], [55], [69]-[71], [79]-[80], [91], [108], [181]. Thus, *Kuboi* discloses that the blue pixel 53B is a photodetector because it includes a photoelectric conversion portion. Further, with regard to the green and red pixels, *Kuboi* discloses “[l]ight hv passes through the on-chip microlens to enter the p-type organic photoelectric conversion film 13, in which the light is subjected to photoelectric conversion, whereby electron-hole pairs are generated.” *Kuboi*, ¶[64]. Thus, *Kuboi* discloses that the red and green pixels 53G and 53R are also photodetectors because

they each include a photoelectric conversion portion that generates charge carriers in response to receiving light. In my opinion, therefore, one skilled in the art would have understood that *Kuboi*'s pixels are photodetectors because its pixels detect light by absorbing light photons and generating electric charge carriers.

110. *Kuboi* also explains that a "silicon semiconductor layer 12" is divided into respective pixels. *Kuboi*, ¶[91]. In my opinion, one skilled in the art would have understood that *Kuboi*'s pixels (i.e., pillars) comprise Si (i.e., silicon) because *Kuboi*'s pixels are formed in a silicon (or Si) semiconductor layer.

- c. **[1b]: "wherein at least some of the photodetectors comprise P-doped and N-doped regions and regions therebetween and are configured to respond to illumination with light in selected visible and infrared wavelength ranges by generating electrical charge carriers;"**

111. In my opinion, *Kuboi* discloses this limitation.

112. As I discussed above, *Kuboi*'s imaging device includes an array of pixels, each of which is a photodetector. *Supra* XI.A.1.b (claim [1a]); *Kuboi*, ¶[90]-[91]. *Kuboi* also discloses that in its blue pixel 53B (i.e., a pillar), "a p⁺-type semiconductor region 18, an n-type semiconductor region 16, and a n⁺-type semiconductor region 17 are formed in that order from the light incident surface of the semiconductor layer 12 toward the opposite surface." *Kuboi*, ¶[91]; *see also Kuboi*, ¶¶[71], [181]. Similarly, *Kuboi* discloses that in its red pixel 53R (i.e., a pillar) and green pixels 53G (i.e., pillars), "the same p⁺-type semiconductor region 18, n-type semiconductor region 16, and n⁺-type semiconductor region 17 are formed." *Kuboi*, ¶[91]. Thus, *Kuboi* discloses that the red, blue, and the green pixels of its imaging device have a p⁺-type region 18, an n-type region 16, and an n⁺-type region 17.

113. *Kuboi* discloses that semiconductor layer 12, which is formed of silicon, is implanted with impurities. *Kuboi*, ¶[56]. In my opinion, one skilled in the art would have understood that the process of implanting impurities into silicon material is known as “doping.” This is supported by other prior art that would have been known to one skilled in the art.

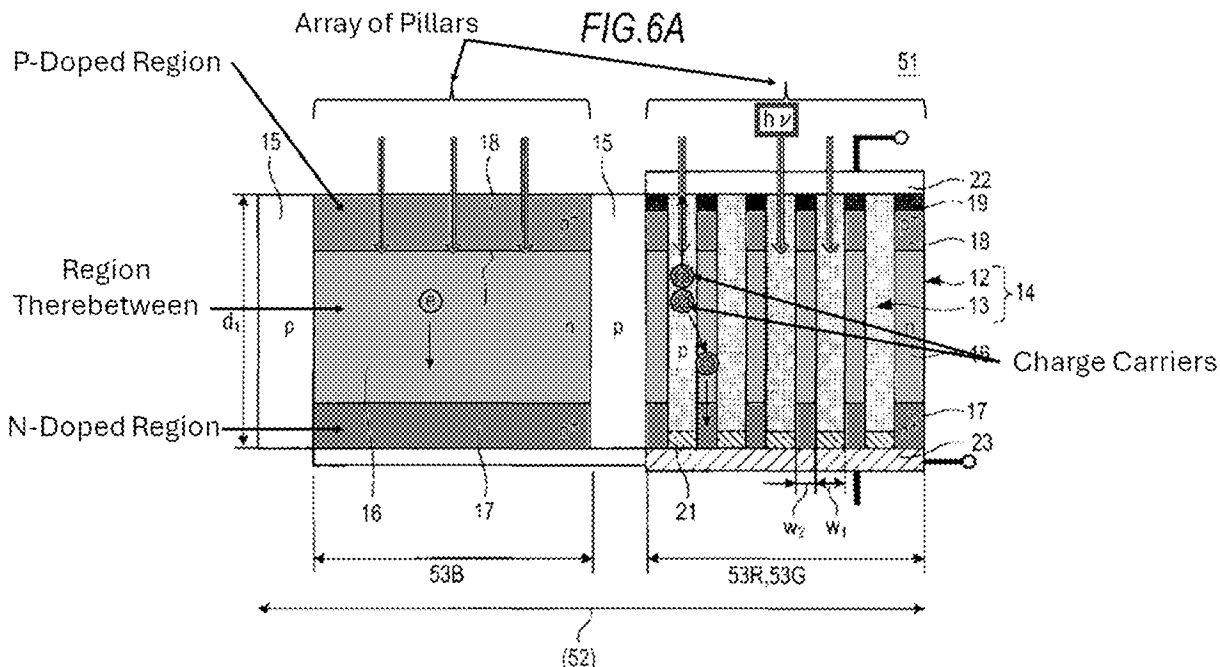
114. For example, doping of semiconductors by implanting impurities has been well known in semiconductor fabrication since at least the early 1960s, and doping has been a major element of semiconductor manufacturing since then and even today. Ex-1018, 4 (noting use of diffusion using diffusion techniques to alter the type of conductivity in silicon patented in 1952, and development of ion implantation for doping semiconductors in 1958). Ex-1001 defines “doping” as “the process of introducing impurity atoms into pure silicon to change its electrical properties.” Ex-1001, 5. Similarly, Ex-1018 discloses: “Impurity doping is the introduction of controlled amounts of impurity dopants into semiconductor materials.” Ex-1018, 37. And Ex-1020 explains: “A doped region is simply a section of the silicon into which impurity atoms have been purposely added to alter the electrical properties.” Ex-1020, 4.

115. *Kuboi* discloses that implanting impurities in *Kuboi*’s semiconductor layer 12 forms “a n⁺-type semiconductor region 17 having higher concentration [of impurities] than the n-type semiconductor region 16.” *Kuboi*, ¶[56]. Similarly, implanting impurities in *Kuboi*’s semiconductor layer 12 forms “a semiconductor region 18 of second conductivity type (for example, p⁺ type) having higher concentration [of impurities] than the n-type semiconductor region 16.” *Kuboi*, ¶[56]; *see also Kuboi*, ¶¶[111], [151], [7]. In my opinion, one skilled in the art would have understood that as a result of implanting impurities (i.e., doping), p⁺-type semiconductor region 18 is a “P-doped” region, and n⁺-type semiconductor region 17 is an

“N-doped” region, as claimed. Further, in my opinion, because *Kuboi*’s region 16 is positioned between region 18 and region 17, *Kuboi*’s region 16 is the “region therebetween,” as claimed.

116. *Kuboi*’s imaging device includes a pixel group composed of blue pixel 53B, red pixel 53R, and green pixels 53G, arranged in a two-dimensional Bayer configuration with corresponding color filters. *Supra* XI.A.1.b (claim [1a]; *Kuboi*, ¶[90]. As I explained above for claim [1a], *Kuboi* discloses that blue pixel 53B is formed by a photoelectric conversion portion comprising a photodiode (PD), while red pixel 53R and green pixels 53G are formed using the photoelectric conversion portion 14. *Kuboi*, ¶[90]; *supra* XI.A.1.b. *Kuboi* discloses that pixel 11 includes a hybrid photoelectric conversion portion 14 that further includes “a plurality of organic material layers 13 embedded in the semiconductor layer 12.” *Kuboi*, ¶¶[55], [91], [181]. *Kuboi* also explains that light $h\nu$ enter the p-type organic photoelectric conversion film 13, in which the light is subjected to photoelectric conversion, which results in generation of electron-hole pairs. *Kuboi*, ¶[64]. In my opinion, *Kuboi*’s photodetector pillars are configured to generate electron-hole pairs (i.e., photo-generated charge carriers) when subjected to illumination with light $h\nu$ (i.e., light photons incident on said array of pillars). *Kuboi*, ¶[107]. *Kuboi* discloses that the silicon photodiode that comprises the blue pixel 53B also generates “charge carriers” when illuminated with light. *Kuboi*, ¶¶[6], [149]. Thus, in my opinion, one skilled in the art would have understood that *Kuboi*’s blue pixel 53B, red pixel 53R, and two green pixels 53G (“pillars”) generate “charge carriers” when illuminated with light ($h\nu$). *Kuboi*, ¶¶[87], [107].

117. *Kuboi*’s photodetector pillars, including the P-doped regions (i.e., region 18), N-doped regions (i.e., region 17), the regions therebetween (i.e., region 16), and the photo-generated charge carriers are illustrated below:



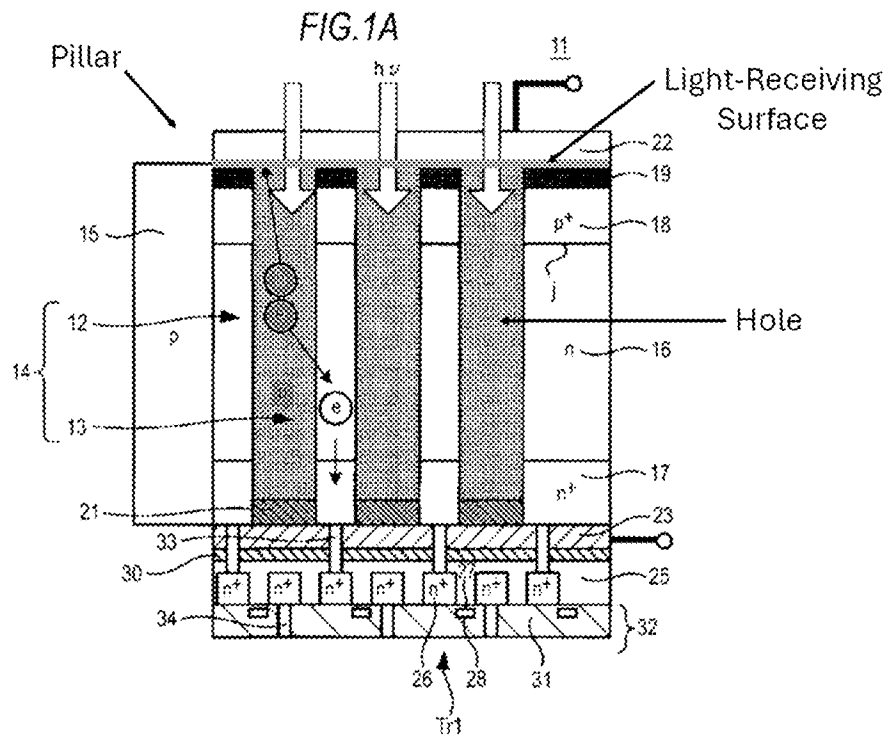
Kuboi, Fig. 6A (annotated).

118. *Kuboi* discloses that its imaging device can be used in the visible light region and in other wavelength bands, for example, infrared. *Kuboi*, ¶[190]. *Kuboi* discloses that its organic material is sensitive to (i.e., generates electric charge carriers in response to) “visible light” but that compounds sensitive to infrared rays can also be used. *Kuboi*, ¶[58]. In my opinion, one skilled in the art would have understood from *Kuboi*’s disclosure that by selecting a suitable organic material, *Kuboi*’s photodetector pillars would be able to respond to light in a wavelength range selected from the visible and/or the infrared light spectrum. One skilled in the art would also have had a reasonable expectation of success in modifying *Kuboi*’s imaging device to respond to light in a wavelength range selected from the visible and/or the infrared light spectrum. This is because *Kuboi* already discloses selecting the material of the organic photoelectric films in its pixels to detect light in selected visible and/or infrared wavelength ranges.

d. [1c]: “one or more holes that are deliberately formed into the light-receiving surfaces, have elongated and/or other shapes at said light-receiving surfaces, extend into the photodetectors to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;”

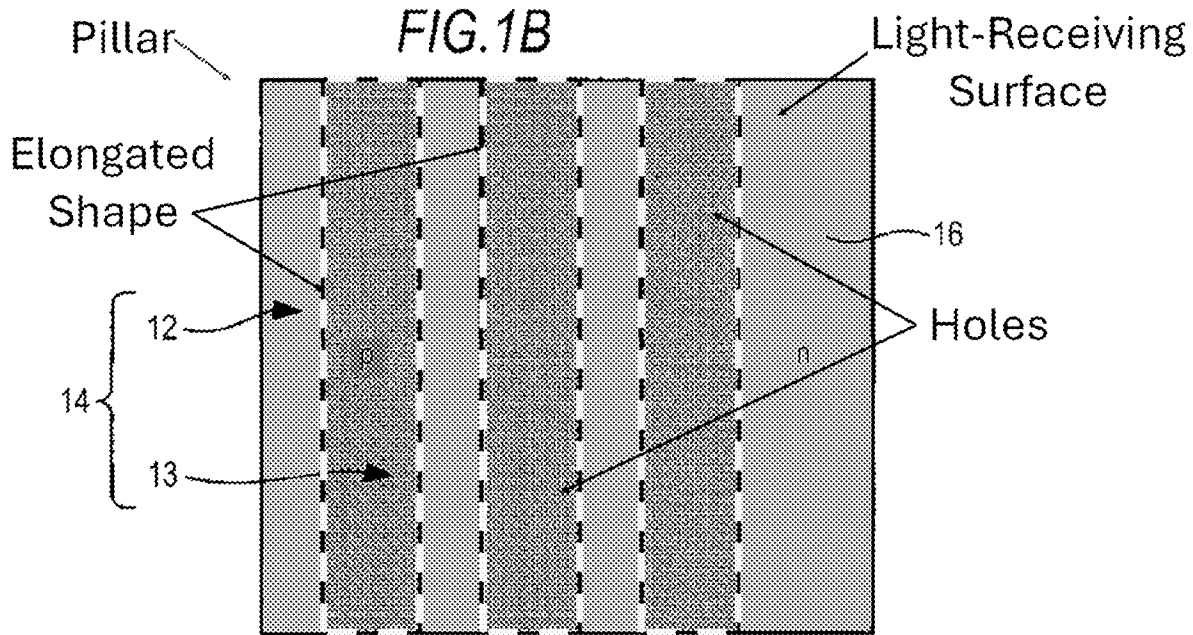
119. In my opinion, *Kuboi* discloses or renders obvious this limitation.

120. *Kuboi* discloses that “hole 38 such as a trench or a via extending from the p⁺-type semiconductor region 18 to the n⁺-type semiconductor region is formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶¶[72], [13]-[14], [67], [95]. *Kuboi* also discloses that a “plurality of vertical holes 38 are formed at necessary intervals.” *Kuboi*, ¶[72]. *Kuboi* describes its vertical holes as “so-called [] trench[es].” *Kuboi*, ¶[67]. *Kuboi* also discloses with reference to its Figure 1A that “the vertical holes 38 are formed in a stripe shape as seen in a planar view.” *Kuboi*, ¶[72]. Figure 1A of *Kuboi* showing the stripe shape of vertical holes 38 in the planar view is illustrated below.



Kuboi, Fig. 1A.

121. *Kuboi* explains that “an organic photoelectric conversion film 13 is deposited so as to be embedded in the vertical holes 38.” *Kuboi*, ¶[73]. As can be seen in the above Figure 1A, vertical holes 38 and films 13 deposited in those holes have elongated shapes in the vertical direction. *Kuboi* also discloses with reference to its Figure 1B that “the plurality of organic photoelectric conversion films 13 are formed in a stripe shape so as to divide the semiconductor layer 12 into a plurality of parts as viewed from the upper surface.” *Kuboi*, ¶[57]. Figure 1B of *Kuboi* showing the stripe shape of films 13 deposited in their associated holes 38 as viewed from the upper surface is illustrated below.



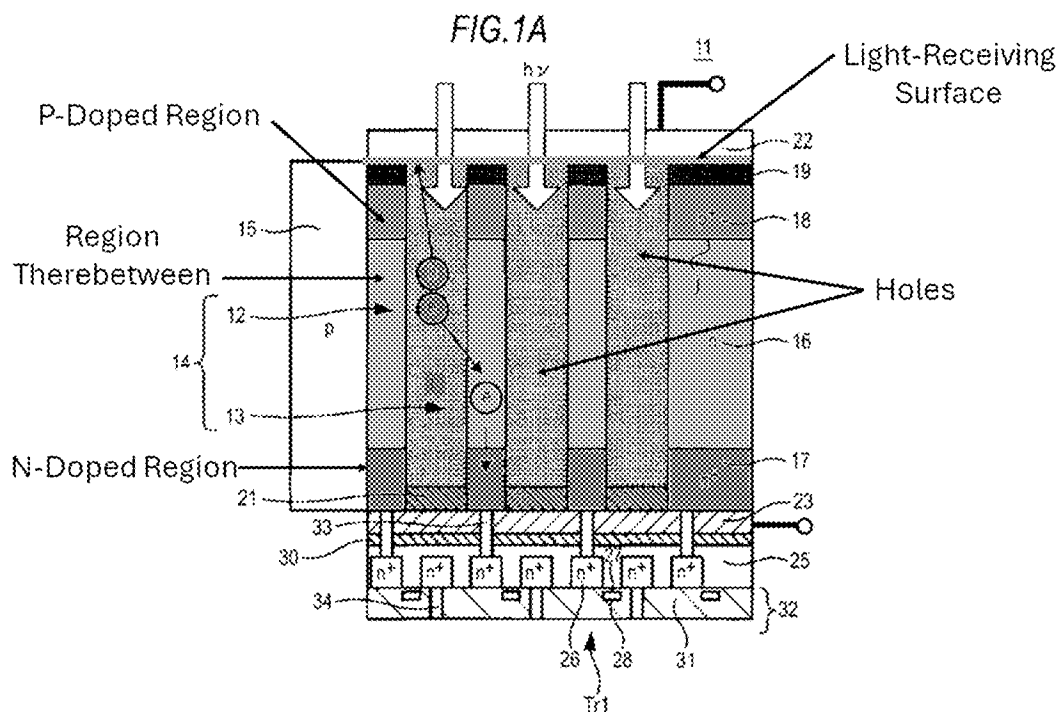
Kuboi, Fig. 1B (annotated).

122. As can be seen in the above Figure 1A, holes 38 and films 31 deposited in those holes have elongated shapes at the light-receiving surfaces of *Kuboi*’s pixels (or pillars), which are photodetectors. *Supra* XI.A.1.b (claim [1a]). In my opinion, one skilled in the art would have understood from these disclosures that *Kuboi*’s stripe shape represents the shape of a trench. One

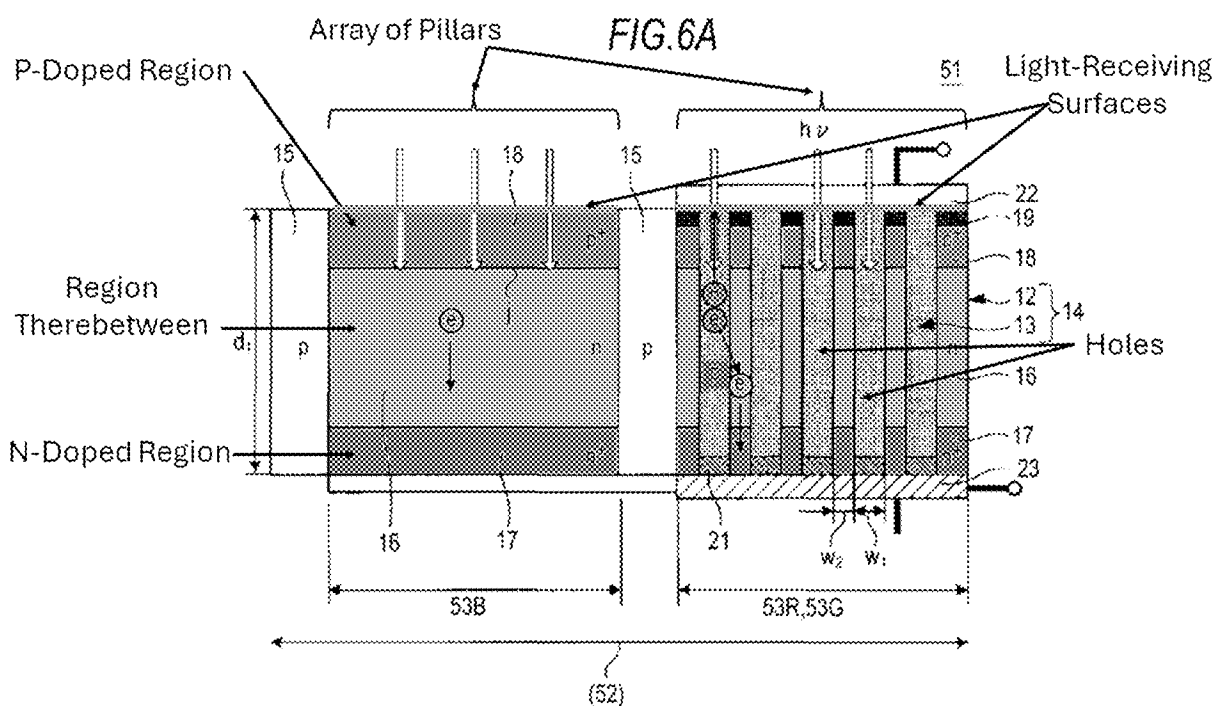
skilled in the art would have further understood from the above figures that a stripe or trench shaped hole would have an elongated or other similar shape.

123. Although Figures 1A/1B illustrate only one pixel (i.e., pillar), as discussed for claim [1a], *Kuboi*'s imaging device includes a plurality of pixels (i.e., 53R and 53G). *Supra* XI.A.1.b. *Kuboi* also discloses that pixels 53R and 53G have structures similar to Figure 1A's pixel. *Kuboi* ¶[90]. Thus, a POSITA would have understood that *Kuboi*'s integrated structure has a plurality of pixels (i.e., pillars), that include one or more holes (i.e., "at least one," "at least some," or "a plurality of holes") having elongated or other shapes (or formed as elongated trenches) at the light-receiving surface of the respective pixel.

124. *Kuboi* also discloses that the holes 38 extending through the PIN regions of its pixels may be dry-etched "using a CCP (Capacitive Coupled Plasma) etching apparatus" or other apparatuses. *Kuboi*, ¶¶[72], [95]. In my opinion, because holes 38 are formed using a CCP apparatus, one skilled in the art would have understood that these holes 38 are deliberately formed in *Kuboi*'s semiconductor layer 12. One skilled in the art would have also understood that because holes 38 extend *from* region 18 (i.e., P-doped region), they are formed in the light-receiving surfaces located between region 18 and electrode 22. *Kuboi*'s holes formed in its light-receiving surfaces are illustrated below.

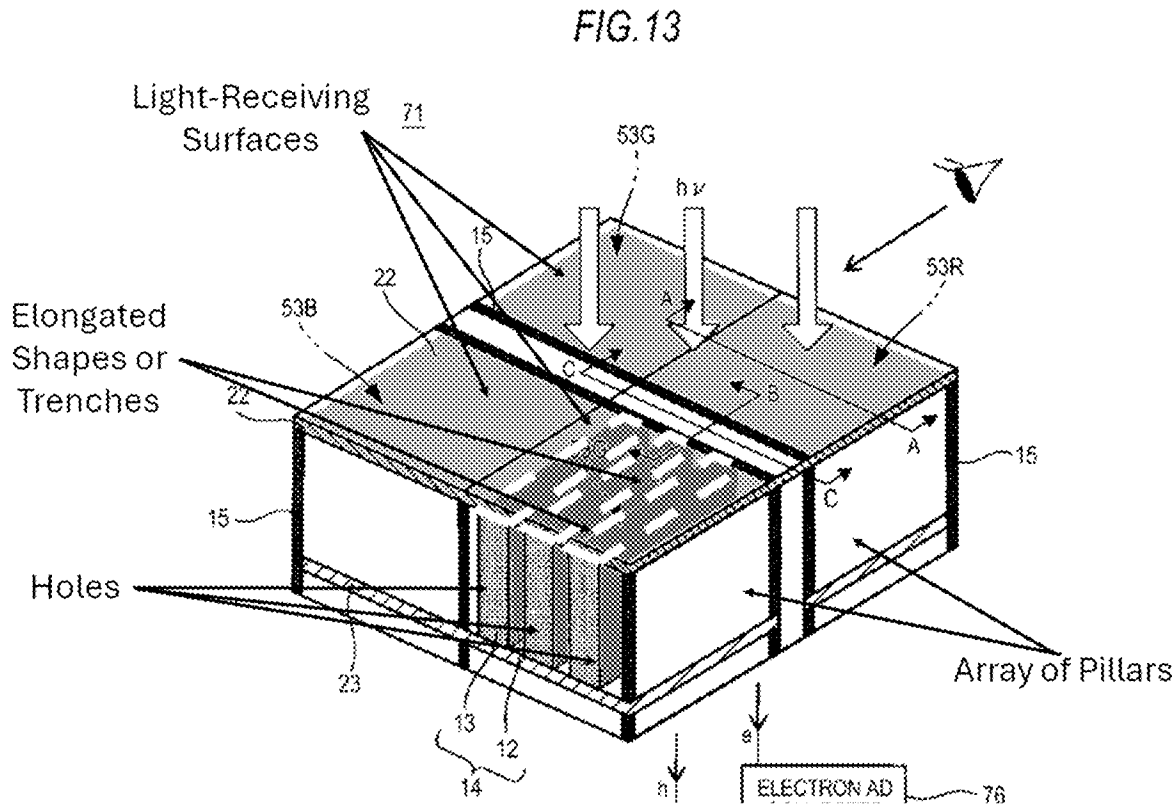


Kuboi, Fig. 1A (annotated).



Kuboi, Fig. 6A (annotated).

125. A perspective view of *Kuboi*'s holes (or trenches) having elongated or other shapes at the light-receiving surface is illustrated below:



Kuboi, Fig. 13 (annotated).

126. *Kuboi* also discloses that “an electron blocking film 21 having a thickness of several tens of nm, for example is formed on the bottom portions of the vertical holes 38.” *Kuboi*, ¶¶[73], [91]. *Kuboi* explains that “film 21 is formed by an insulating film such as, for example, a silicon nitride (Si_3N_4) film [or] a silicon [oxide] (SiO_2) film.” *Kuboi*, ¶[73].

127. In my opinion, a person of ordinary skill in the art would have understood that silicon oxide or silicon nitride films are dielectric materials. This is supported by other prior art that would have been known to one skilled in the art. For example, Ex-1020 discloses: “Classically, silicon dioxide (generically called oxide here) has served as the insulating dielectric.” Ex-1020, 34. Further, Ex-1020 discloses that silicon nitride is “an insulator.”

Ex-1020, 35. As another example, Ex-1018 discloses “[d]ielectric layers such as silicon dioxide and silicon nitride.” Ex-1018, 20.

128. In my opinion, one skilled in the art would have further understood that *Kuboi*’s silicon dioxide or silicon nitride film would be made of solid material. This is because thermal oxides like silicon dioxide are formed during semiconductor fabrication processes by oxidizing the solid silicon material. For example, Ex-1018 discloses the formation of a silicon oxide by a “thermal oxidation” process in which oxygen is supplied for oxidizing solid silicon wafers in a furnace. Ex-1018, 20-21. One skilled in the art would also have understood that an insulating film formed by oxidation of silicon would have an amorphous structure, which is characteristic of a solid material. Ex-1018, 23 (“When silicon is thermally oxidized, the silicon dioxide structure is amorphous.”). In my opinion, one skilled in the art would have recognized that because the thermally oxidized silicon dioxide is amorphous, it would be a solid material.

129. Similarly, a skilled artisan would have recognized that in semiconductor fabrication silicon nitride is deposited via a chemical vapor deposition (CVD) process. Ex-1018, 33. Further, one skilled in the art would have understood that such CVD deposition of silicon nitride would produce a solid layer of silicon nitride. Ex-1018, 30 (“Chemical vapor deposition (CVD) is a method of forming a thin solid film on a substrate.”).

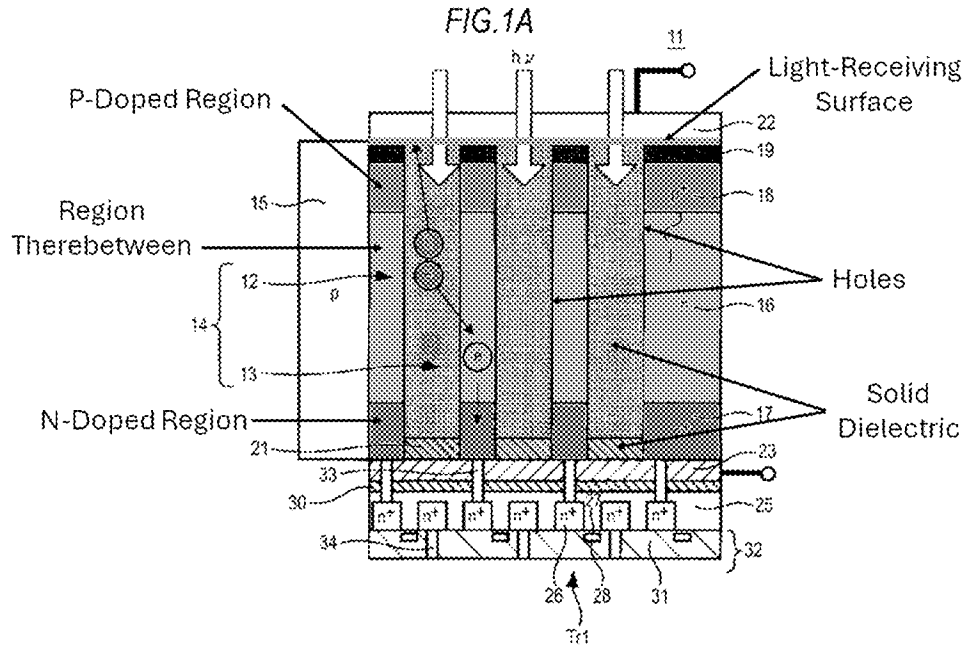
130. In my opinion, therefore, one skilled in the art would have understood that *Kuboi*’s film 21 would be made of a solid dielectric material.

131. *Kuboi* also discloses that an organic material is deposited to fill portions of the holes, thereby forming organic photoelectric conversion films 13 embedded within the hole. *Kuboi*, ¶¶[73], [58], [85], Fig. 4C. *Kuboi* discloses that as the p-type organic material is sensitive to a visible light region, “perylene-based compounds, phthalocyanine compounds, quinacridone

compounds, porphyrin compounds, merocyanine compounds, and the like can be used, for example.” *Kuboi*, ¶[58]. This is consistent with the description in the ’871 Patent indicating that its microstructured pillar and hole arrays can include “polymer, glass, oxides, nitrides, . . . organic conducting and non conducting polymers.” ’871 Patent, 50:7-21.

132. In my opinion, one skilled in the art would have recognized that phthalocyanine compounds, perylene-based compounds, and porphyrin compounds function as dielectric materials. Various prior art references examine their dielectric properties and behavior in optoelectronic devices. For instance, Ex-1021 discusses the dielectric characteristics of phthalocyanine and perylene compounds used in organic solar cells. Ex-1021, 3, 17, 47, 52-56. Additionally, Ex-1022, 1-4, 7, explores the dielectric behavior of phthalocyanine compounds, noting that their dielectric constant decreases with increasing frequency and rises with increasing temperature. Ex-1034, 4-11, presents experimental studies on porphyrin as a dielectric material, while Ex-1035, 1-6, details dielectric investigations of porphyrin compounds used in optical devices. Ex-1036, 1-6, discusses the measurement of photocurrents generated by illuminating a porphyrin compound, alongside its dielectric property evaluations. Ex-1037, 1, explains that the dielectric properties of phthalocyanine compounds increase with temperature and decrease with frequency. Lastly, Ex-1038, 1-5, describes perylene compounds as organic dielectric materials with “high photoluminescence efficiency,” employed in solar cells.

133. Thus, both electron blocking film 21 and photoelectric conversion film 13 together entirely fill the holes of photoelectric conversion portion 14 and are solid dielectric materials. *Kuboi*’s deliberately formed holes filled with solid dielectric material are illustrated below.



Kuboi, Fig. 1A (annotated).

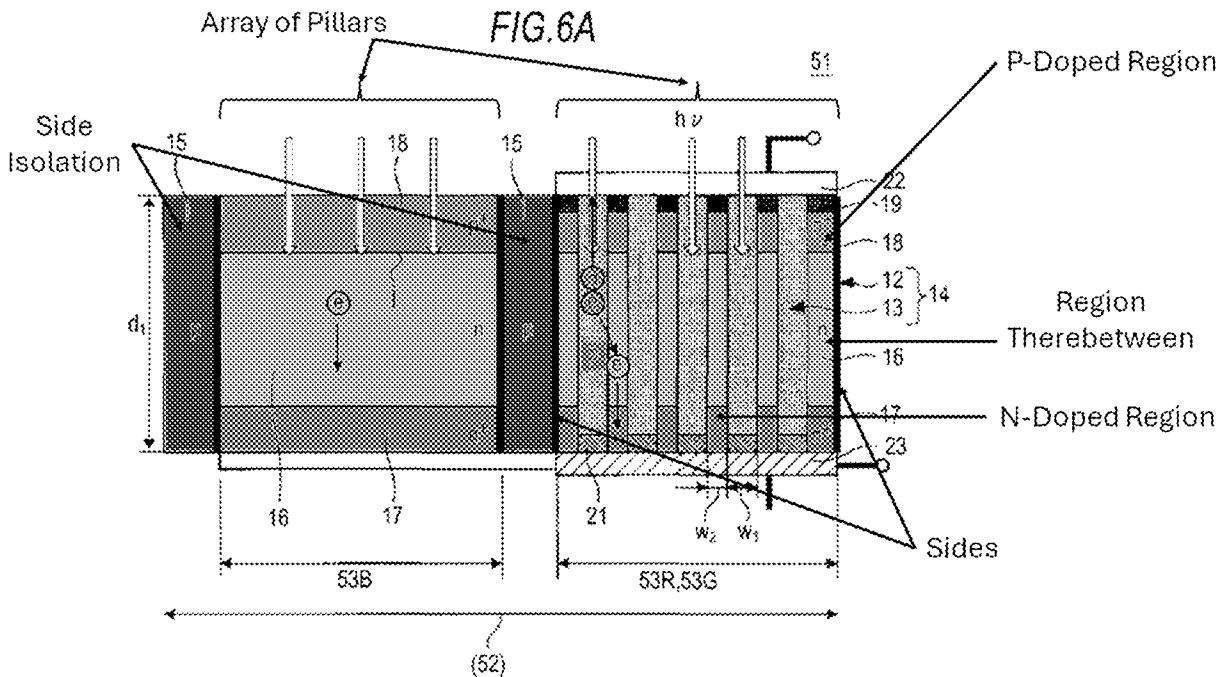
134. *Kuboi* discloses that holes 38 extending from region 18 to region 17 are “formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶¶[72], [13]-[14], [67], [95]. In my opinion, one skilled in the art would have understood that *Kuboi*’s holes extend into its pixels and, therefore, into *Kuboi*’s photodetectors because *Kuboi*’s pixels are photodetectors. *Supra* XI.A.1.b (claim [1a]). Furthermore, referencing Figures 6A/6B, *Kuboi* discloses that the thickness d_1 of semiconductor layer 12 is “set to about 1.4 μm .” *Kuboi*, ¶[94]. *Kuboi*’s holes extending through thickness d_1 of semiconductor layer 12 are illustrated below:



e. [1d]: “side-isolation comprising solid material at said sides of at least some of the photodetectors;”

137. *Kuboi* discloses that its “silicon semiconductor layer 12 is divided into respective pixels by an element separation region 15 which is formed by a p-type semiconductor region.” *Kuboi*, ¶¶[91], [55]-[56], [71], [182]. *Kuboi* also discloses that “pixel 11 is separated by an element separation region 15.” *Kuboi*, ¶[55] (emphasis added). In my opinion, one skilled in the

art would have understood that element separation region 15 provides side-isolation because it separates adjacent pixels. *Kuboi*'s side-isolation made of p-type semiconductor is a solid material because it is formed in *Kuboi*'s silicon semiconductor layer 12, which is a solid material. As illustrated below, *Kuboi*'s side-isolation layer is located at the sides of *Kuboi*'s pixels (which are photodetectors, XI.A.1.b (claim [1a]), *supra*):



Kuboi, Fig. 6A (annotated).

f. [1e]: “a solid dielectric material forming a base dielectric region for said array; and”

138. In my opinion, *Kuboi* discloses or renders obvious this limitation.

139. *Kuboi* discloses a “CMOS solid-state imaging device” in which “pixel transistors constituting one pixel are formed in a semiconductor region 25 formed of silicon which is disposed on the front surface side of the semiconductor layer 12, namely under the lower electrode 23 with an insulating film 30 disposed therebetween.” *Kuboi*, ¶¶[55], [61], [69]. *Kuboi* also discloses a semiconductor substrate on which the semiconductor region 25 having pixel

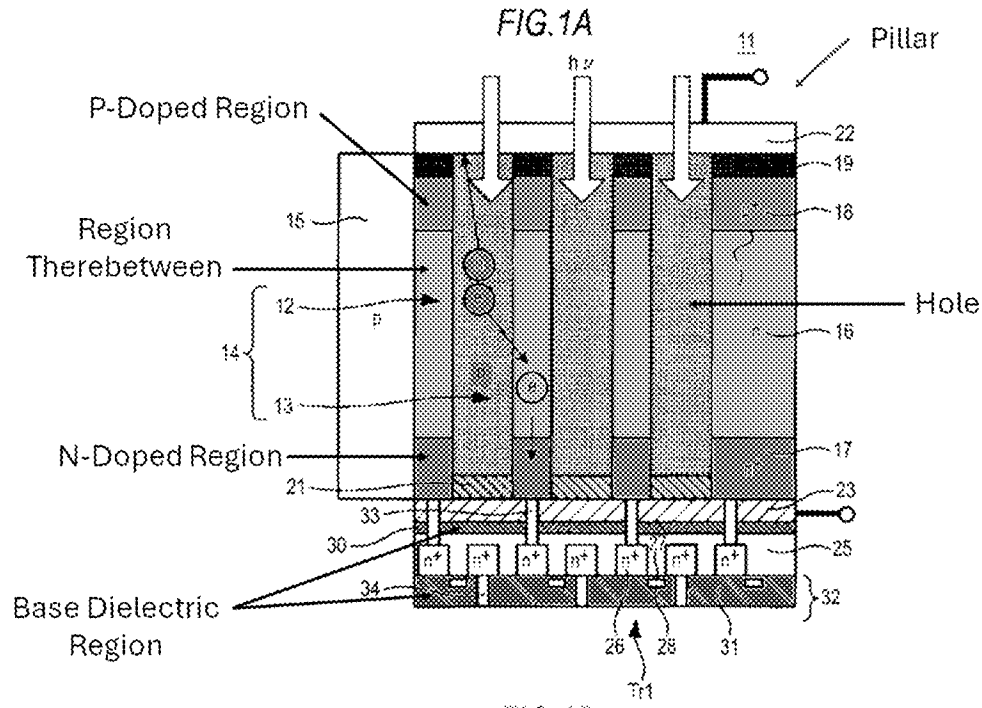
transistors, the multilayer wiring layer 32, and the lower electrode 23 are formed. *Kuboi*, ¶[69]. *Kuboi* explains that multilayer wiring layer 32 includes a plurality of layers of wiring with an interlayer insulating film 31 disposed therebetween. *Kuboi*, ¶[62]. In my opinion, *Kuboi*'s insulating film 30 and/or insulating interlayer film 31 constitutes the claimed base dielectric region. This is because as I explain below, both these layers are made of dielectric material and are located at the base of *Kuboi*'s pillars.

140. *Kuboi* does not disclose the material for its insulating films 30 or 31. However, *Kuboi* discloses “an insulating film such as, for example, a silicon nitride (Si₃N₄) film, a silicon nitride (SiO₂) film, and the like.” *Kuboi*, ¶[73]. Therefore, in my opinion, one skilled in the art would have understood that *Kuboi*'s insulating film 30 that insulates lower electrode 23 from the pixel transistors and is part of a CMOS device would constitute a film of silicon oxide or silicon nitride or at least would have been motivated to use silicon oxide or silicon nitride. This is because silicon oxide or silicon nitride films can be fabricated using standard silicon fabrication processes. Ex-1018, 20 (stating that “thermal oxidation . . . is a key process in modern silicon integrated-circuit technology”). Moreover, silicon oxide or silicon nitride provide good barriers to impurity and moisture diffusion. Ex-1018, 4 (“[A]n oxide layer can prevent most impurity atoms from diffusing through it.”), 5, 34 (“The plasma-deposited nitride provides excellent scratch protection, serves as a moisture barrier, and prevents sodium diffusion.”).

141. Similarly, one skilled in the art would have understood that *Kuboi*'s interlayer insulating film 31 that insulates wiring layers from each other would constitute a film of silicon oxide or silicon nitride, or at least would have found this configuration obvious, there being a motivation for it and a reasonable expectation of success in achieving it. This is supported by other prior art that would have been known to one skilled in the art. Ex-1025, ¶¶[13], [14]

(disclosing “a method of manufacturing a CMOS device” in which “first insulating film 102 may be composed of silicon oxide film (SiO₂) or an aluminum oxide film”); Ex-1020, 34 (“Classically, silicon dioxide (generically called oxide here) has served as the insulating dielectric.”); Ex-1020, 35 (disclosing silicon nitride as “an insulator”); Ex-1024, 26:9-14 (disclosing that “it is preferable that the material of the interlayer insulating film used for the multi-layer wiring of the lower layer is used so as to form the film, from the viewpoint of reliability and manufacturing cost” and that “silicon oxide, silicon nitride, silicon nitride oxide or laminated films thereof are generally used”); Ex-1018, 20 (disclosing that many different kinds of thin films, including thermal oxides, are used to fabricated discrete devices and integrated circuits), 34 (“The plasma-deposited nitride provides excellent scratch protection, serves as a moisture barrier, and prevents sodium diffusion.”). One skilled in the art would have also understood that both silicon dioxide and silicon nitride are solid materials and that both are dielectric or insulating materials. *Supra* XI.A.1.d (claim [1c]).

142. As I explained above, in my opinion, a skilled artisan would have understood that *Kuboi*’s insulating films 30 or 31 made of silicon dioxide or silicon nitride would be made of solid material. *Kuboi*’s insulating films 30 and/or 31 (i.e., base dielectric region) for *Kuboi*’s pixel array (i.e., array of pillar) are illustrated below:



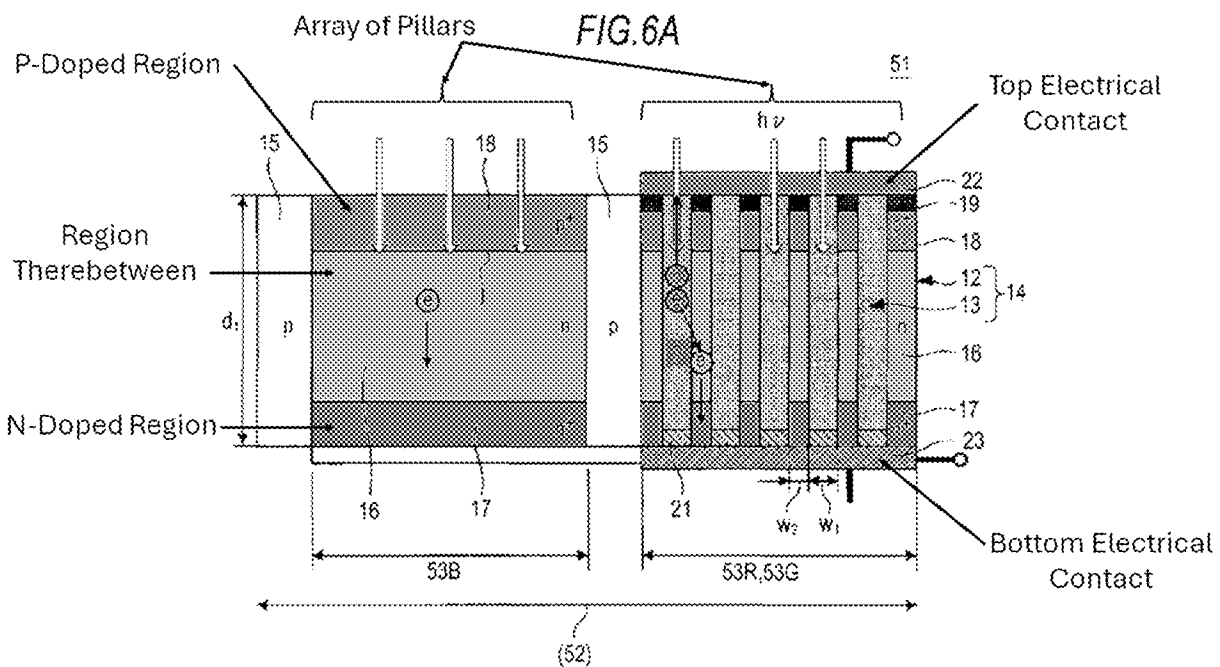
Kuboi, Fig. 1A (annotated).

143. As seen in the above figure, both of *Kuboi*'s insulating films 30 and 31 are disposed below *Kuboi*'s pixel (i.e., pillar). Although Figure 1A illustrates only one pixel, as I discussed for claim [1a], *Kuboi*'s imaging device includes a plurality of pixels (i.e., 53B, 53R, and 53G) arranged as an array of pixels. *Supra* XI.A.1.b. *Kuboi* discloses that pixels 53R and 53G have structures similar to the Figure 1A pixel. *Kuboi* ¶[90]. Moreover, one skilled in the art would have understood that *Kuboi*'s multilayer wiring board with insulating film 31 would be disposed below *Kuboi*'s array of pillars (i.e., below the array of pixels including 53B, 53R, and 53G). *Kuboi*, ¶[70] (“[A] silicon semiconductor substrate for pixels is bonded to the semiconductor substrate on which the semiconductor region 25, the multilayer wiring layer 32, the lower electrode 23, and the like are formed.”). In my opinion, one skilled in the art would therefore have understood that Figure 1A's base dielectric region would be a base dielectric region for *Kuboi*'s array of pixels.

- g. [1f]: “electrical contacts configured to provide electrical pathways to at least some of the photodetectors, including for selected reverse-biasing thereof;”

144. In my opinion, *Kuboi* discloses this limitation.

145. *Kuboi* discloses that a “pair of electrodes 22 and 23 is formed on the entire rear and front surfaces of the semiconductor layer 12.” *Kuboi*, ¶¶[60], [77], [93], [103]. *Kuboi* explains that “upper electrode 22 on the rear surface side is formed by a transparent electrode formed of a transparent conductive film.” *Kuboi*, ¶[60]. *Kuboi* further explains that “lower electrode 23 is formed of metal exhibiting ohmic properties.” *Kuboi*, ¶[60]. *Kuboi*’s electrodes (i.e., “electrical contacts”) are illustrated in the figure below:



Kuboi, Fig. 6A (annotated).

146. *Kuboi* discloses that “an organic photoelectric conversion film 13 is deposited so as to be embedded in the vertical holes 38.” *Kuboi*, ¶¶[73], [91]. *Kuboi* explains that “[l]ight $h\nu$ passes through the on-chip microlens to enter the p-type organic photoelectric conversion film

13, in which the light is subjected to photoelectric conversion, whereby electron-hole pairs are generated.” *Kuboi*, ¶[64].

147. *Kuboi* discloses that a “necessary voltage is applied between the upper electrode 22 and the lower electrode 23.” *Kuboi*, ¶[64]. *Kuboi* discloses that “electrons *e* serving as signal charges move from the organic photoelectric conversion film 13 through the interface toward the semiconductor layer 12 depleted by the applied bias voltage.” *Kuboi*, ¶[64]. *Kuboi* further discloses that “hole *h* moves toward the upper electrode 22 through the organic photoelectric conversion film 13 and is discharged through the upper electrode 22.” *Kuboi*, ¶[64]. In my opinion, one skilled in the art would have understood that *Kuboi*’s electrodes 22 and 23 provide electrical pathways at least to some of *Kuboi*’s pixels (which are photodetectors, *supra* XI.A.1.b). This is because the holes generated in *Kuboi*’s pixels move through electrodes 22, and because electrons *e* generated in *Kuboi*’s pixels move toward semiconductor layer 12 due to a bias voltage applied between electrodes 22 and 23.

148. *Kuboi* also discloses that a necessary voltage is applied between electrodes 22 and 23 so that p^+ -type region 18 is at a negative potential and n^+ -type region 17 is at a positive potential. *Kuboi*, ¶[64]. In my opinion, one skilled in the art would have understood that electrodes 22 and 23 are configured to apply a voltage bias to *Kuboi*’s pixels (which include photodetectors) with a negative potential to p^+ type region 18 and a positive potential to n^+ -type region 17, resulting in a reverse bias for a respective pixel. *Kuboi*, ¶[186]. This is further supported by other prior art that would have been known to one skilled in the art. For example, Ex-1031 explains that reverse bias is “[t]he condition in which a positive voltage is applied to the *n* region with respect to the *p* region of a *pn* junction.” Ex-1031, 3-5, 8. Because *Kuboi* allows for applying the reverse biasing to particular pixels and further allows for selection of the

necessary voltage for reverse biasing, in my opinion, one skilled in the art would have understood that *Kuboi* discloses that its electrical contacts (i.e., electrodes 22 and 23) are configured to provide electrical pathways for selected reverse biasing as claimed. In my opinion, one skilled in the art would have also understood that *Kuboi*'s imaging device selects the bias voltage for the level of reverse biasing needed to maintain performance under changing operating conditions. This is supported by prior art that would have been known to one skilled in the art. Ex-1040 explains that "[i]t is well known that the behavior ... [of photodiodes] are strongly dependent on both bias voltage and temperature." Ex-1040, 4-29. Ex-1009 discloses that "[t]he electric field is proportional to the applied bias voltage in devices." Ex-1009, 1, 4-6 (plotting a "linear dependence of the internal electric field on applied bias"), 10. Ex-1038 demonstrates that the intrinsic frequency response—which determines the upper bandwidth limit of a photodiode—is significantly influenced by both reverse bias voltage and temperature. Ex-1038, 1-6. By applying a physical model and analyzing experimental data, this reference shows that increasing the reverse bias voltage widens the depletion region, thereby reducing junction capacitance and enhancing response speed. This effect is especially beneficial in low-light conditions where fast and sensitive detection is critical. Additionally, this study explores how temperature variations impact carrier mobility and transit time, further affecting the photodiode's dynamic behavior. Together, these findings underscore the importance of carefully tuning bias voltage to optimize photodiode performance across different operating environments. *See* Ex-1039, 4-17. Thus, in my opinion, one skilled in the art would have understood that by selecting the "necessary voltage" based on ambient conditions, *Kuboi* enables stable operation across varied operating conditions. Accordingly, one skilled in the art would have known that since *Kuboi* allows reverse biasing of particular pixels and allows for selection of *necessary*

voltage for reverse biasing, its electrical contacts (electrodes 22 and 23) are configured to provide electrical pathways for selected reverse biasing as claimed

- h. [1g]: “wherein the presence of said one or more holes increases by a factor of 1.1 the absorption of the light by at least some of the photodetectors relative to otherwise like photodetectors lacking said holes.”**

149. In my opinion, *Kuboi* discloses or at least renders this limitation obvious in view of the knowledge of a person of ordinary skill in the art.

150. First, a skilled artisan would have found claim [1g] disclosed in view of the skilled artisan’s knowledge of the state of the art before the priority date of the ’871 patent. In my opinion, the skilled artisan would have understood that the intensity I_d of light at a depth “d” in a material is governed by the Lambert-Beer expression $I_d = I_0 e^{-\alpha d}$, where I_0 is the intensity of incident light and α is the absorption coefficient of the material. Ex-1005, 23. A skilled artisan would have also understood that the amount of incident light entering a material would be $I_0 \times A$, where A is the cross-sectional area available for light to enter the material (i.e., area of light incidence). Ex-1005, 25. Further, the skilled artisan would have understood that the amount of light exiting the material of depth d would be $(I_0 e^{-\alpha d}) \times A$. Ex-1005, 25. A skilled artisan would, therefore, have understood that the amount of incident light absorbed by a material of depth d (P_{abs}) would be $I_0 (1 - e^{-\alpha d}) \times A$, based on the Lambert-Beer expression. Ex-1005, 23-25.

151. *Kuboi* discloses that the organic photoelectric conversion film 13 in the red pixel 53R which is sensitive to the red light wavelength band can include “phthalocyanine compounds.” *Kuboi*, ¶[92]. Red light wavelengths range between about 620 to 750 nm. *Yu*, ¶[23]. Further, *Kuboi* discloses that the organic photoelectric conversion film 13 in the green pixel 53G which is sensitive to the green light wavelength band can include “porphyrin compounds.” *Kuboi*, ¶[92]. Green light wavelengths range between about 495 to 570 nm. *Yu*,

¶[23]. *Kuboi* also discloses “the organic photoelectric conversion film has a greater optical absorption coefficient than silicon.” *Kuboi*, ¶[4], [12], [92]. As I explain below, the higher absorption coefficient of *Kuboi*’s organic photoelectric conversion film provides a greater than 10% increase in light absorption over a comparable photodetector that does not include holes.

152. Ex-1009 provides a graph showing the absorption coefficients for phthalocyanine compounds over a range of wavelengths. Ex-1009, 3, Fig. 1. Ex-1004 similarly provides a graph showing the absorption coefficients for porphyrin compounds over a range of wavelengths. Ex-1004, 3, Fig. 6. I have reproduced these graphs below.

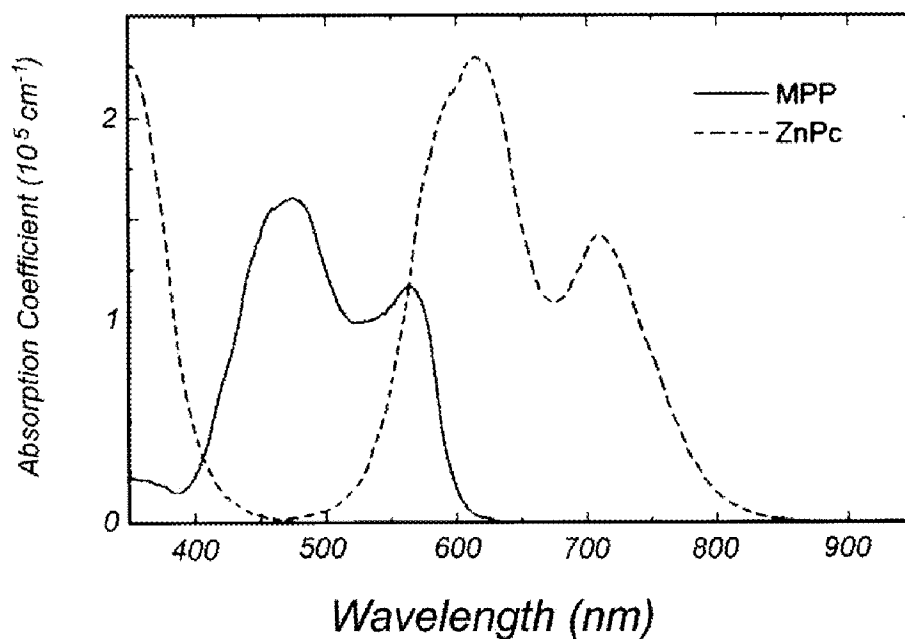


Fig. 1. The absorption spectra of ZnPc (dashed line) and MPP (solid line).

Ex-1008, 3.

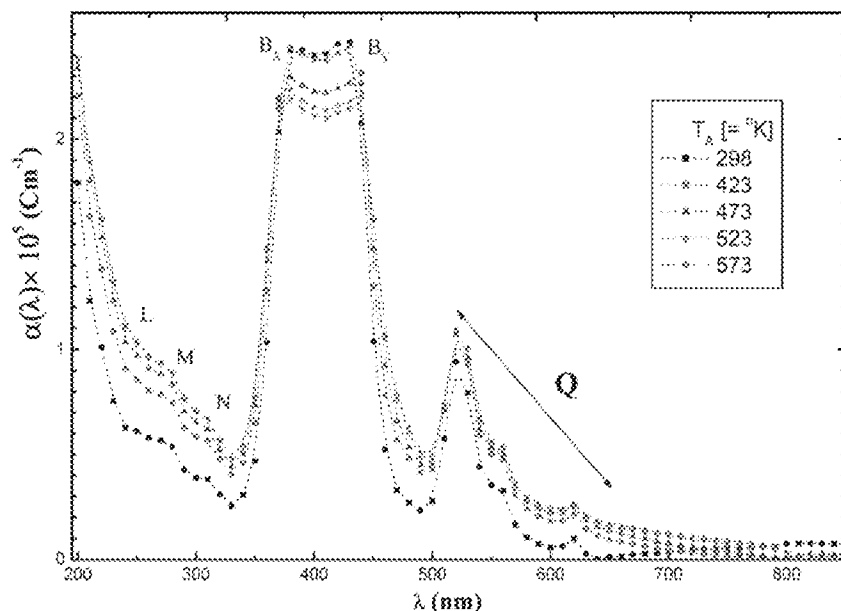


Fig. 6. (Color online) The optical absorption coefficient, $\alpha(\lambda)$, versus wavelength, λ , for as-deposited and annealed NiTPP thin films.

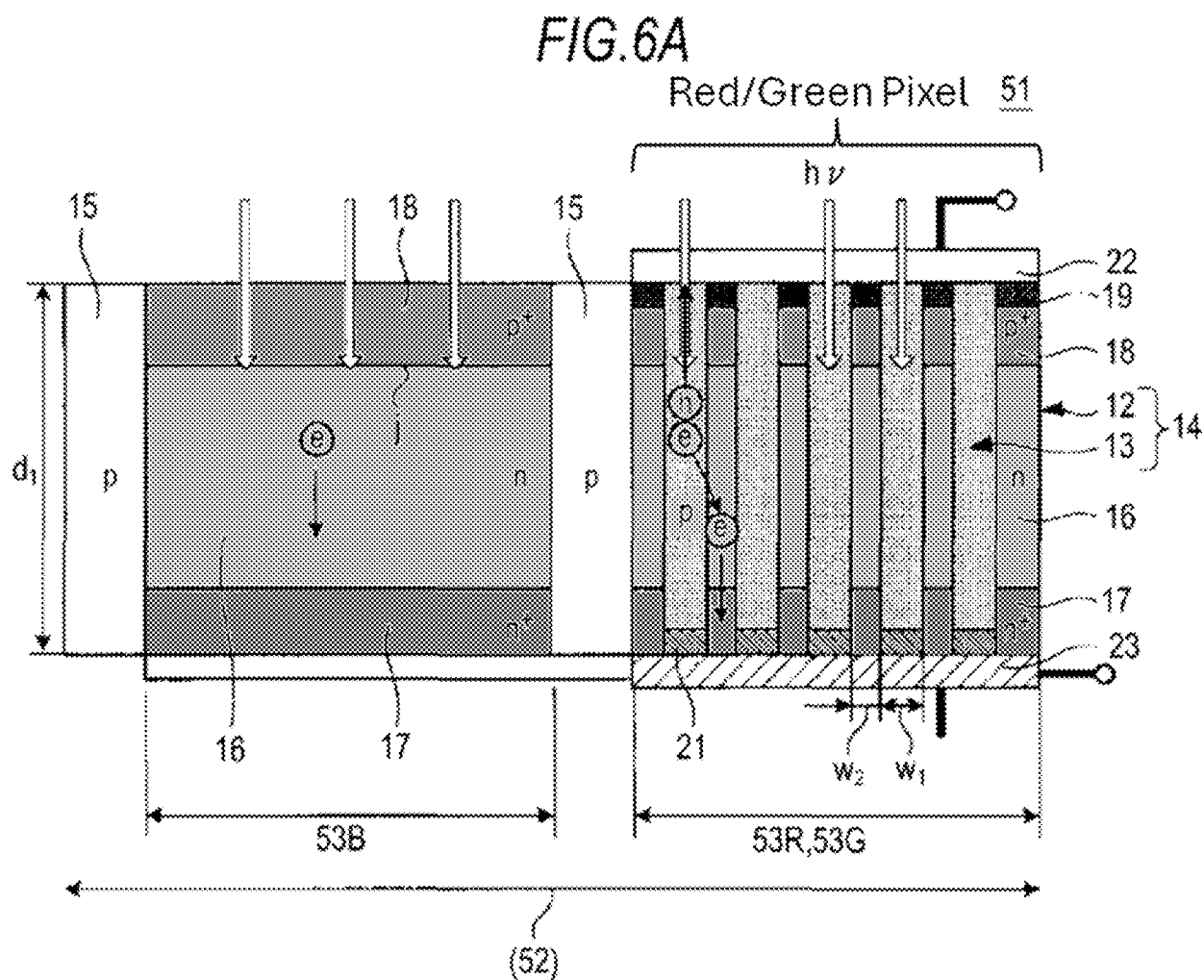
Ex-1003, 5.

153. Ex-1008 provides a table of the absorption coefficients of silicon. In Table A below, I have listed the absorption coefficients for the phthalocyanine and porphyrin organic materials which I extracted from the above figures and compared them with the absorption coefficient for silicon for the green and red light wavelength ranges. As seen from the table below, the absorption coefficient of the porphyrin organic materials is greater than silicon in the green light wavelength range of 510 to 580 nm. Similarly, the absorption coefficient of the phthalocyanine organic materials is ten times greater than silicon for the red light wavelength range of 620 to 750 nm.

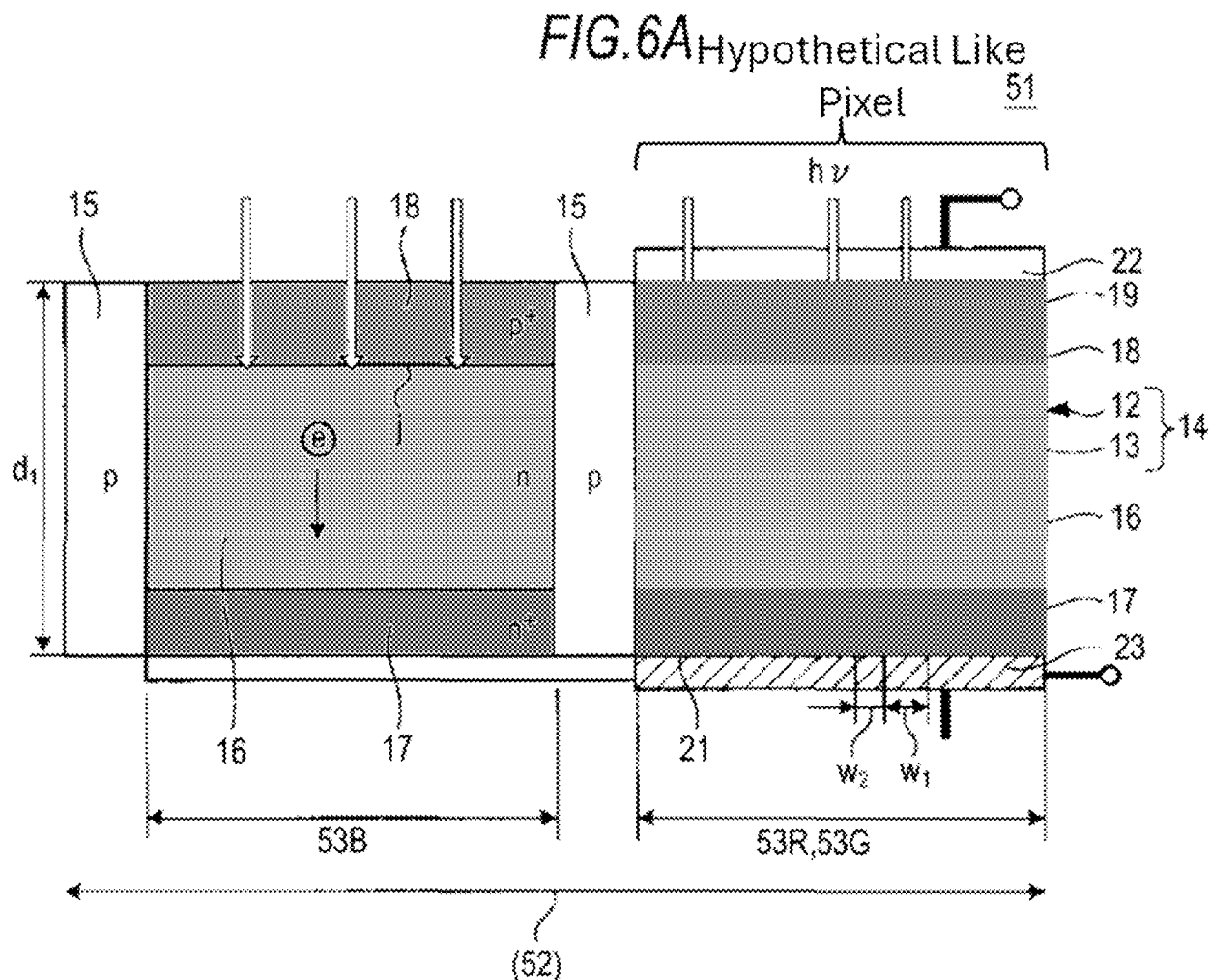
Table A			
Wavelength (nm)	Absorption coefficient α (cm⁻¹)		
	Silicon (Ex-1009)	Porphyrin (Ex-1004)	Phthalocyanine (Ex-1009)
490	12600	22000	
500	11100	27000	
510	9700	57600	
520	8800	93400	
530	7850	79000	
540	7050	44000	
550	6390	35000	
560	5780	31400	
570	5320	15800	
580	4880	10000	
620	3520		228000
630	3280		216000
640	3030		188000
650	2790		147000
660	2570		122000
670	2390		111000
680	2200		110000
690	2040		120000
700	1890		133000
710	1780		142000
720	1680		135000
730	1540		119600
740	1420		101000
750	1310		83000

154. Claim [1g] recites an “increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to otherwise *like* photodetectors lacking said holes” (emphasis added). As I discussed above for claim [1a], *Kuboi*’s pixels are photodetectors. *Supra* XI.A.1.b. Below I have illustrated the structure of *Kuboi*’s red or green pixels (or

photodetectors) 53R or 53G (left) and the structure of a *like* pixel or photodetector (right) that does not have holes. As is apparent from the below figures, a *like* pixel would include silicon in place of the organic film in *Kuboi's* holes. Further, as illustrated in the figures below, both *Kuboi's* 53R or 53G pixel and the *like* pixel would include *Kuboi's* light shielding film 19. Thus, light is incident over the same area, defined by the openings in the light shielding film, at the light-receiving surface for both cases.



Kuboi, Fig. 6A (annotated) (53R/53G pixel with organic material in the in-pillar holes).



Kuboi, Fig. 6A (annotated) (Hypothetical pixel without in-pillar holes and no light shield).

156. *Kuboi* discloses a hole width of 200 nm, at least five holes in its red and green pixels, and a $1.4\ \mu\text{m}$ by $1.4\ \mu\text{m}$ pixel area. *Kuboi*, ¶[94], Fig. 6A. Thus, the area of the organic film on which light is incident in *Kuboi*'s red or green pixels (53R or 53G), as defined by the openings in the light shielding film, is about $1.4\ \mu\text{m}^2$ (i.e., $5 \times 0.2\ \mu\text{m} \times 1.4\ \mu\text{m}$). In contrast, the area on which light would be incident on a *hypothetical like* pixel that does not have the light shielding film is about $1.96\ \mu\text{m}^2$ (i.e., $1.4\ \mu\text{m} \times 1.4\ \mu\text{m}$). Thus, the area on which light is incident in *Kuboi*'s green and red pixels is about 71% of the total pixel area.

157. As I discussed above for claim [1c], *Kuboi* discloses holes filled with the organic material and having a depth of 1.4 μm . *Supra* XI.A.1.d; *Kuboi*, ¶[94]. Table B1 below shows an estimate of the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for a *like* pixel (second column) for the green light wavelength range of 490-580 nm. In Table B1, $P_{\text{abs-organic}}$ is the amount of light absorbed in porphyrin organic material (for green pixel 53G), $P_{\text{abs-silicon}}$ is the amount of light absorbed by a *like* pixel having no holes, and both $P_{\text{abs-organic}}$ and $P_{\text{abs-silicon}}$ are obtained using the Lambert-Beer expression. In my opinion, these are conservative estimates because they assume that light travels over the hole depth d of 1.4 μm without accounting for light reflections in *Kuboi*'s holes. The ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for the *hypothetical like* pixel (Table B, third column) is obtained by scaling the values of $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for the *like* pixel (Table B, second column) by 71% to account for the smaller area of light incidence on the organic material in the green pixel as compared to the area of light incidence on the *hypothetical like* pixel.

Table B1		
Wavelength (nm)	P_{abs-organic} / P_{abs-silicon}	
	<i>Like Pixel</i>	<i>Hypothetical Like Pixel</i> (without light shielding film)
490	1.2	0.8
500	1.2	0.9
510	1.3	1.0
520	1.4	1.0
530	1.5	1.1
540	1.6	1.1
550	1.7	1.2
560	1.8	1.3
570	1.7	1.2
580	1.5	1.1

158. The ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ in Table B1 is illustrated in chart form in Figure A below. As illustrated in Figure A, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 (shown by the dashed black line) for the entire green light wavelength range for the *like* pixel. That is, the amount of light absorbed by *Kuboi's* green pixel with holes filled with porphyrin organic material is at least 1.1 times that absorbed by a *like* pixel without holes. Furthermore, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 (shown by the dashed black line) for the 540-570 nm wavelength range for the *hypothetical like* pixel. That is, the amount of light absorbed by *Kuboi's* green pixel with holes filled with porphyrin organic material is at least 1.1 times that absorbed by a *hypothetical like* pixel without holes and without the light shielding film for the 540-570 nm wavelength range.

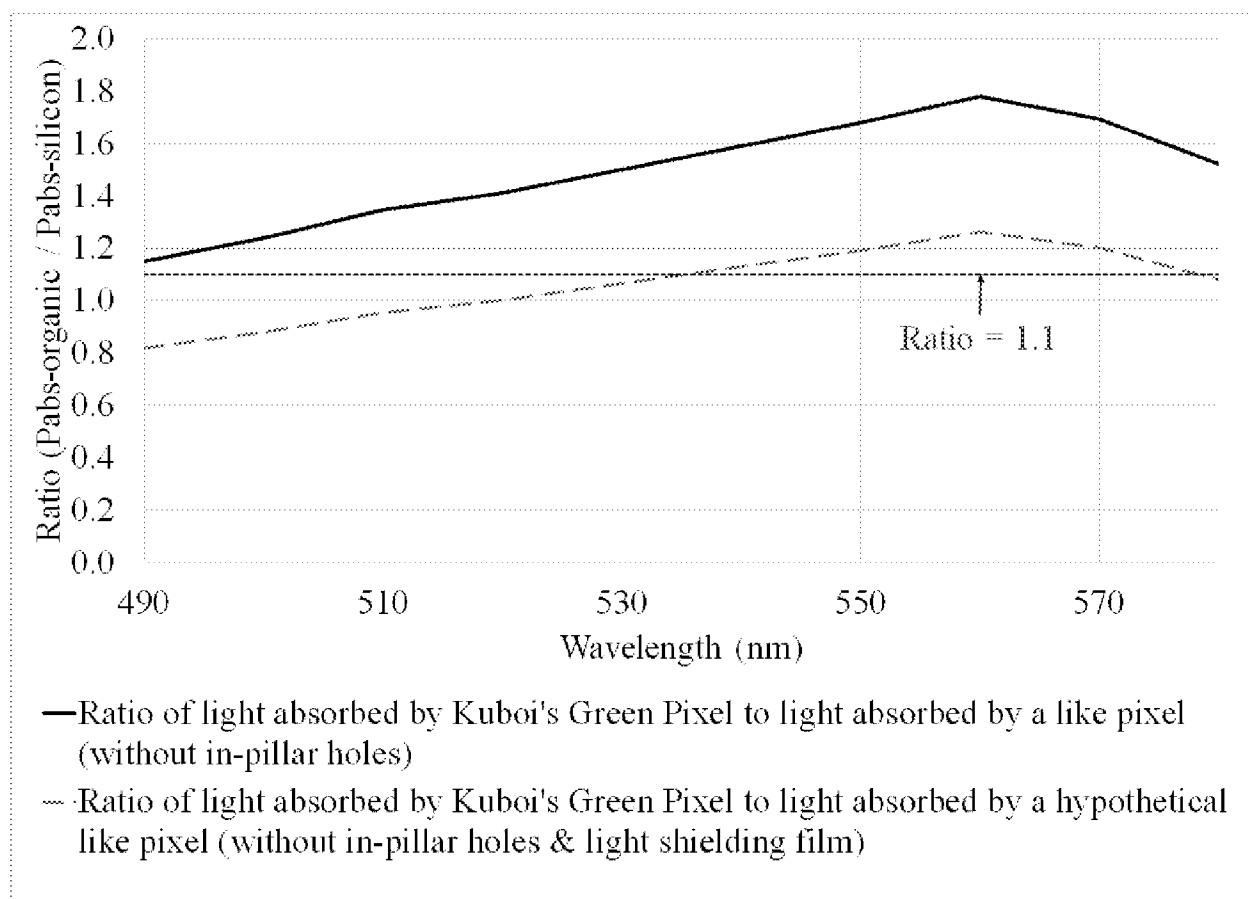


Figure A

I understand that in the related IPR proceeding, Patent Owner argued that the distance 'd' is simply the depth of Kuboi's holes (1.4 μm). I understand that, according to Patent Owner, the light may reflect or scatter as it travels through the non-homogenous materials of Kuboi's hybrid photoelectric portion, and that the distance 'd' traveled by the light may be more than simply the thickness of the material. Even assuming Patent Owner's assertion is true, in my opinion, light reflections in *Kuboi's* holes would increase the distance d traveled by light to a value greater than the hole depth of 1.4 μm . Notably, because of the lack of holes in the *like* pixel or *hypothetical like* pixel, there would be no reflections and as a result the distance d traveled by light in the *like* pixel or *hypothetical like* pixel would remain similar to the hole depth of 1.4 μm assumed in my conservative estimate above. In my opinion, accounting for the increased reflection of light

within *Kuboi*'s holes would yield estimated values for the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ that are similar to or even larger than those shown in Table B1. To illustrate this, I have provided below Table B2 in which I have assumed that light reflection in *Kuboi*'s holes results in an increase in the distance traveled by light of about 5 times the hole depth (e.g., 7.0 μm). I have also assumed that the value of the distance d traveled by light in the *like* pixel and *hypothetical like* pixels remains 1.4 μm because of the lack of any light reflections in the absence of holes in those pixels. As illustrated in Table B2 below, the estimated ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for both the *like* pixel and the *hypothetical like* pixel, including the effect of light reflection in *Kuboi*'s holes, is still greater than 1.1 for most of the green light wavelength range.

Table B2 (assuming light reflection in holes causes 5X increase in d)		
Wavelength (nm)	$P_{\text{abs-organic}} / P_{\text{abs-silicon}}$	
	<i>Like Pixel</i>	<i>Hypothetical Like Pixel</i> (without light shielding film)
490	1.2	0.9
500	1.3	0.9
510	1.3	1.0
520	1.4	1.0
530	1.5	1.1
540	1.6	1.1
550	1.7	1.2
560	1.8	1.3
570	1.9	1.4
580	2.0	1.4

159. Table C1 below shows the estimated ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for a *like* pixel (second column) for the red light wavelength range of 620-780 nm. In Table C1, $P_{\text{abs-organic}}$ is the amount of light absorbed in phthalocyanine organic material (for red pixel 53R) and is obtained using the Lambert-Beer expression. The ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for the *hypothetical like* pixel (Table C, third column) is obtained by scaling the values of $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for the *like* pixel (Table C, second column) by 71% to account for the smaller area of light incidence on the organic material in the red pixel as compared to the area of light incidence on the *hypothetical like* pixel.

Table C1		
Wavelength (nm)	$P_{\text{abs-organic}} / P_{\text{abs-silicon}}$	
	<i>Like Pixel</i>	<i>Hypothetical Like Pixel</i> (without light shielding film)
620	2.6	1.8
630	2.7	1.9
640	2.9	2.1
650	3.1	2.2
660	3.3	2.3
670	3.5	2.5
680	3.8	2.7
690	4.0	2.9
700	4.3	3.1
710	4.5	3.2
720	4.8	3.4
730	5.2	3.7
740	5.5	3.9
750	6.0	4.2
760	6.5	4.6
770	7.0	5.0
780	7.4	5.2

160. The ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ in Table C1 for the *like* pixel is illustrated in chart form in Figure B below. As illustrated in Figure B (and in Table C1, column two), the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 (shown by the dashed black line) for the entire red light wavelength range for the *like* pixel. That is, the amount of light absorbed by *Kuboi's* red pixel with holes filled with phthalocyanine organic material is at least 1.1 times that absorbed by a *like* pixel without holes. Furthermore, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to

1.1 (shown by the dashed black line) for the entire red light wavelength range for the *hypothetical like* pixel. That is, the amount of light absorbed by *Kuboi's* red pixel with holes filled with phthalocyanine organic material is at least 1.1 times that absorbed by a *hypothetical like* pixel without holes and without the light shielding film.

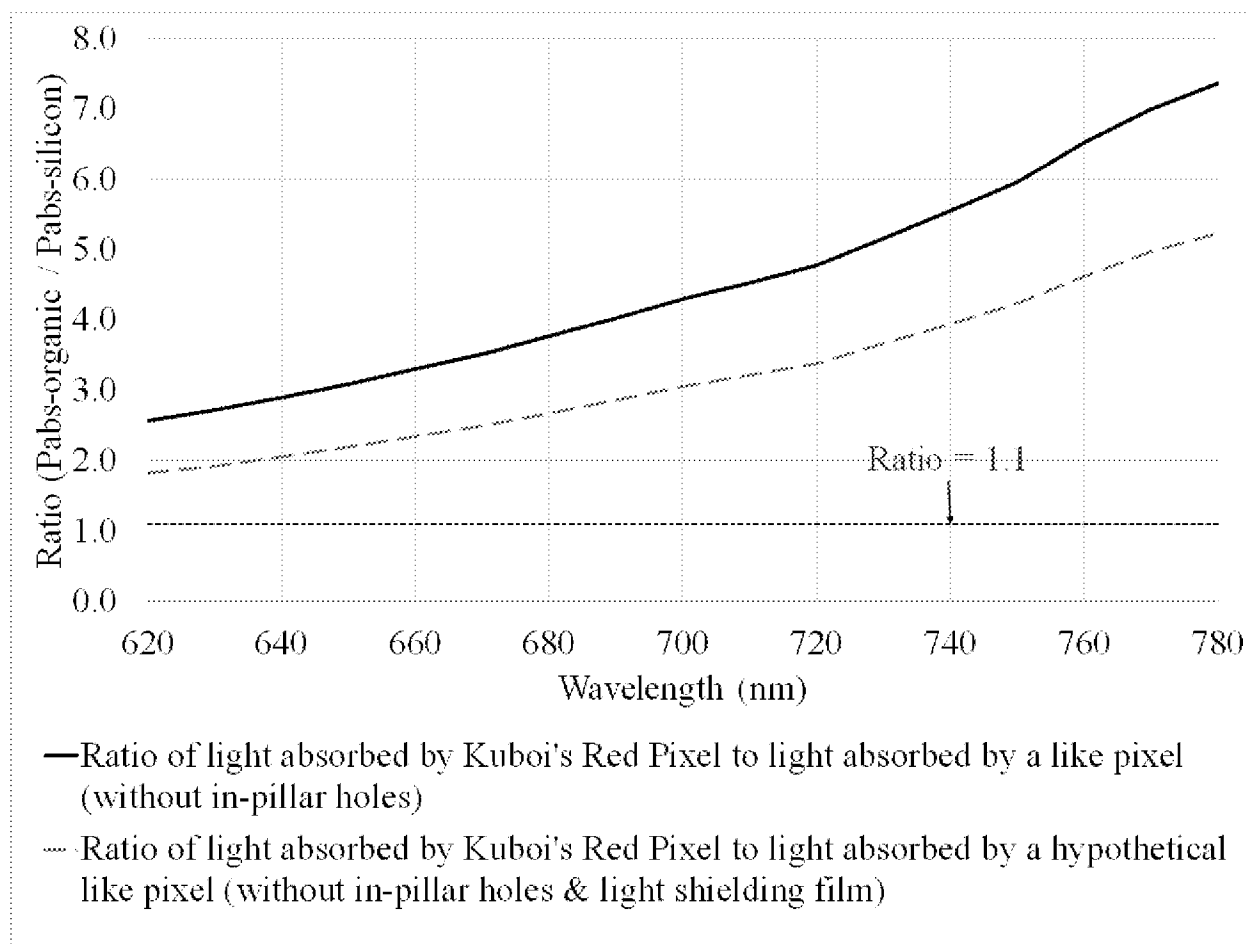


Figure B.

As I did for the green wavelength range, I have also provided below Table C2 in which I have assumed that light reflection in *Kuboi's* holes results in an increase in the distance traveled by light of about 5 times the hole depth (e.g., 7.0 μm). I have also assumed that the value of the distance d traveled by light in the *like* pixel and *hypothetical like* pixels remains 1.4 μm because of the lack of any light reflections in the absence of holes in those pixels. As illustrated in

Table C2 below, the estimated ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for both the *like* pixel and the *hypothetical like* pixel, including the effect of light reflection in *Kuboi*'s holes, is still greater than 1.1 for most of the red light wavelength range.

Table C2 (assuming light reflection in holes causes 5X increase in d)		
Wavelength (nm)	$P_{\text{abs-organic}} / P_{\text{abs-silicon}}$	
	<i>Like Pixel</i>	<i>Hypothetical Like Pixel</i> (without light shielding film)
620	2.6	1.8
630	2.7	1.9
640	2.9	2.1
650	3.1	2.2
660	3.3	2.3
670	3.5	2.5
680	3.8	2.7
690	4.0	2.9
700	4.3	3.1
710	4.5	3.2
720	4.8	3.4
730	5.2	3.7
740	5.5	3.9
750	6.0	4.2
760	6.5	4.6
770	7.0	5.0
780	7.4	5.3

161. In my opinion, therefore, including the effect of light reflections in *Kuboi*'s holes as Patent Owner has asserted still does not change my conclusion. Specifically, the estimated values above illustrate that the amount of light absorbed by *Kuboi*'s green or red pixels with in-

pillar holes filled with organic material is at least 1.1 times the amount of light absorbed by a *hypothetical like* pixel without in-pillar holes and without the light shielding film in selected visible and infrared wavelength ranges as recited in claim [1h]. Further in my opinion, one skilled in the art would have understood that *Kuboi*'s photodetectors with organic material in their holes would increase the absorption of the light (at selected visible and infrared wavelength ranges) in at least some of *Kuboi*'s photodetectors by at least 1.1 times compared to *like* photodetectors lacking said holes.

162. Second, in my opinion, a POSITA would have also found [1g] disclosed based on Patent Owner's statements in the '871 patent. The Patent Owner represents in the '871 patent that an imaging device having the structure disclosed in *Kuboi* would improve photon absorption by at least 10%.

163. The '871 patent details the cause or causes of the enhancement of the absorption coefficient. Specifically, the '871 patent explains:

The cause or causes of the enhancement of the absorption coefficient are believed to include one or more of the following: an increase in optical field concentration, resonance effects, constructive and destructive optical interferences (amplitude and phase) effects, scattering, and *high contrast grating (HCG) effects*. See, e.g. Chang-Hasnain et al, High contrast gratings for integrated optoelectronics, *Advances in Optics and Photonics* 4, 379-440 (2012), hereinafter "Chang-Hasnain." The HCG effects are at the near-wavelength regime (See, Chang-Hasnain) where the optical wavelength in the material of the grating and the optical wavelength in the surrounding material of the grating is the range of the period of the grating.

'871 patent, 11:52-64 (emphasis added). A skilled artisan would have understood from the above-excerpted disclosure that one cause of enhancement of photon absorption is due to effects produced by a high contrast grating (HCG).

164. The '871 patent further explains that "[t]he period of the 3D pillar/hole microstructured array can be seen as a 3D high contrast grating, whose period of the grating Λ can lie between λ/n_1 where n_1 is the optical refractive index of material M_1 and λ/n_2 where n_2 is the optical refractive index of material M_2 ." '871 patent, 12:14-18. Further, "[i]f $n_1 > n_2$, then $\lambda/n_1 < \Lambda < \lambda/n_2$." '871 patent, 12:18-19. A skilled artisan would have understood from this disclosure that a structure that includes holes in the pillars of an imaging device would behave like an HCG if the pitch between the holes satisfies the condition $\lambda/n_1 < \Lambda < \lambda/n_2$, when $n_1 > n_2$.

165. The '871 patent confirms this, explaining that the HCG effect may explain the high absorption coefficient of semiconductors with holes that satisfy the relationship $\lambda/n_1 < \Lambda < \lambda/n_2$. Specifically, the '871 patent states:

The HCG effect that may explain the high enhancement of the absorption coefficient of the bulk material is that a single or multiple HCG layer (or a single microstructured pillar/hole array layer) due to its resonance effects and/or due to a varying of the microstructured pillar/hole period spacing, the optical signal resonating in the HCG/microstructured pillar-hole array can be directed to propagate in the plane of the HCG/microstructured pillar-hole array rather than normal to the surface. Together with resonance and in-plane propagation this can greatly increase the absorption path length in the HCG/microstructured pillar-hole array.

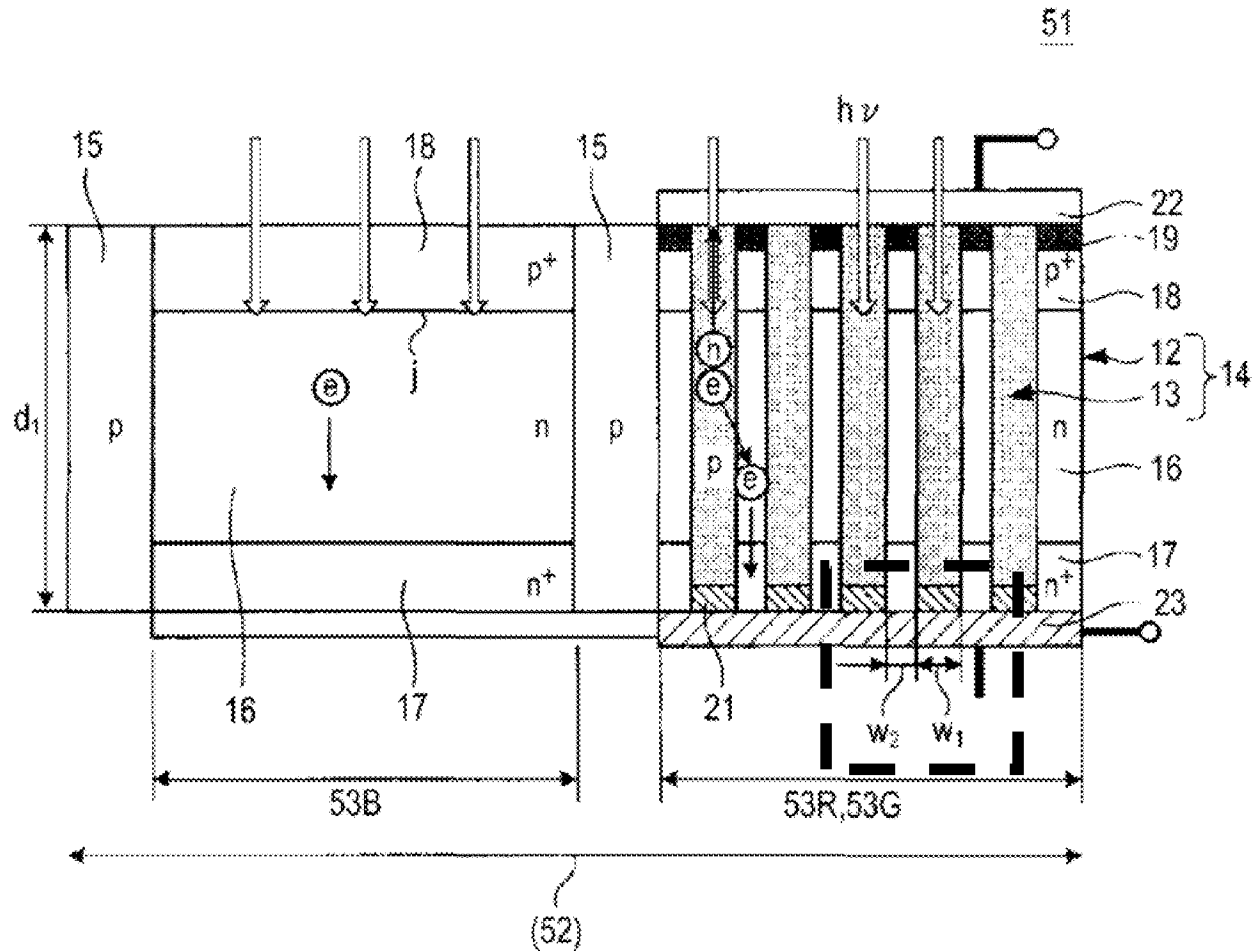
'871 patent, 12:35-45. The '871 patent goes on to say that "[u]sing the phenomenon of near-wavelength and also deep-wavelength where the HCG period is much less than the optical

wavelength, and the diffraction regime where the HCG period is greater than the optical wavelength (See, Chang-Hasnain) the microstructured pillar-hole-void array can have enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100.” ’871 patent, 12:49-55.

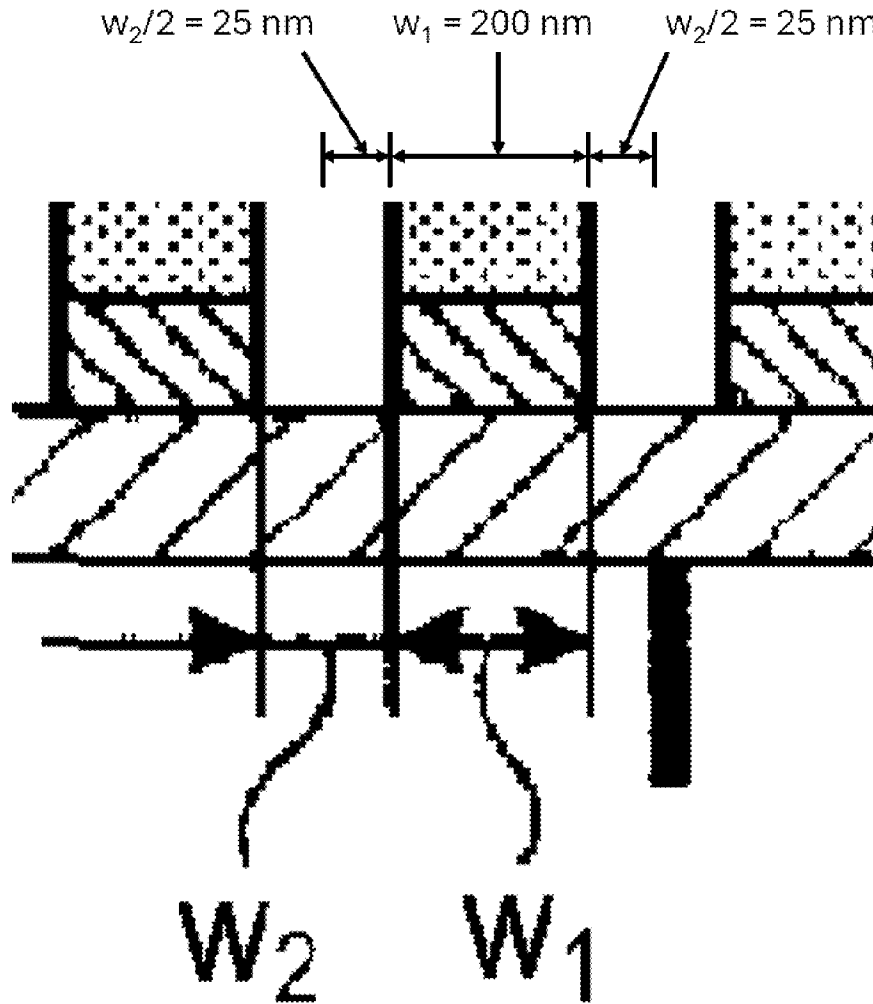
166. One skilled in the art would have understood these disclosures of the ’871 patent as representations made by Patent Owner that a microstructured pillar hole array having microstructure period Λ (i.e., pitch of the holes) and satisfying the relationship $\lambda/n_1 < \Lambda < \lambda/n_2$ forms a high contrast grating (HCG). In my opinion, one skilled in the art would have further understood the Patent Owner as representing that if the microstructured pillar hole array forms an HCG, then the physical phenomenon of near-wavelength and deep-wavelength would result in an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient associated with a structure that does not have the microstructured pillar hole array.

167. As I have discussed, *Kuboi* discloses an imaging device that has an array of pillars with holes. *Supra* XI.A.1.b, XI.A.1.d (claims [1a], [1c]); *infra* XI.A.2 (claims [2], [18]). Furthermore, *Kuboi* discloses a microstructured pillar hole array where the period Λ or center-to-center distance between holes is about 250 nanometers. For example, *Kuboi* discloses that the width w_1 of photoelectric conversion films 13 is 200 nm and width w_2 of semiconductor layer 12 between the photoelectric conversion films is 50 nm. *Kuboi*, ¶[94]. *Kuboi*’s Figure 6A, below, illustrates these dimensions. Additionally, I have provided a magnified view of Figure 6A to illustrate that the period Λ or center-to-center distance between holes in that figure would be 250 nm. Specifically, the period Λ would be $w_2/2 + w_1 + w_2/2 = 25 \text{ nm} + 200 \text{ nm} + 25 \text{ nm} = 250 \text{ nm}$.

FIG. 6A



Kuboi, Fig. 6A (annotated).



Kuboi, Fig. 6A (cropped, magnified, and annotated).

168. One skilled in the art would have understood that visible light has a wavelength range of 400 nm -700 nm and infrared light has a wavelength range of 750 nm to 1,000 μm or even 2,000 μm . Ex-1012, 4 (disclosing wavelengths “typically in the 400-700 nm range of visible light”); *Yu*, ¶[23] (disclosing “IR light (light of wavelengths from about 0.78 to about 1000 microns)”). Further, one skilled in the art would have understood that the refractive index n_1 of silicon ranges between about 3.0 to 5.9 (Ex-1027, 9:43-46, Fig. 4) and varies with wavelength. Ex-1023, 48. For example, the refractive index n_1 of silicon is about 5.8 for light of

wavelength 400 nm, 3.7 for light of wavelength 700-750 nm, and about 3.5 for light of wavelength 1,000 nm. Ex-1023, 48.

169. *Kuboi* discloses the organic photoelectric conversion films in its holes may include materials such as “perylene-based compounds, phthalocyanine compounds, quinacridone compounds, porphyrin compounds, merocyanine compounds.” *Kuboi*, ¶[58]. One skilled in the art would have understood that the refractive index n_2 of such organic materials ranges between 1.5 and 3.0. Ex-1026, 86:35-48 (disclosing porphyrin compounds as photoelectric conversion material), 142:18-25 (disclosing refractive index of photoelectric conversion material); Ex-1004, 6, Fig. 5 (disclosing refractive index of porphyrin compounds ranging from 1.5 to 2.8 for wavelengths of 400-700 nm); Ex-1003, 13, Fig. 7 (disclosing refractive index of phthalocyanine compounds ranging from 1.5 to 2.8 for wavelengths of 400-700 nm); Ex-1002, Abstract (disclosing refractive index of phthalocyanine compounds ranging from 2.03 to 2.48).

170. Below, I have provided Table D showing calculated values of λ/n_1 and λ/n_2 for *Kuboi*'s green pixels with porphyrin for visible light wavelengths 400 nm and 700 nm, and near infrared wavelengths of greater than 700 nm wavelength. I obtained values of λ/n_1 and λ/n_2 in Table D, using values of n_1 of silicon for different wavelengths from Ex-1023, page 48, Table A-1, and values of n_2 of porphyrin compounds at different wavelengths from Ex-1004, Fig. 5. As seen from the values in Table D, *Kuboi*'s hole pitch of 250 nm falls in the range λ/n_1 to λ/n_2 for at least part of the visible light spectrum (400-700 nm wavelengths) and at least part of the near infrared light spectrum (>700 nm wavelengths). For example, for the 550 nm green light wavelength, λ/n_1 ($550/4.5 = 123$) $< \Lambda$ (250 nm) $< \lambda/n_2$ ($550/2.0 = 275$).

Table D				
λ (nm)	n_1 (Silicon)	n_2 (Porphyrin)	λ/n_1(nm)	λ/n_2 (nm)
400	5.8	1.7	68	235
550	4.5	2.0	123	275
700	3.7	1.6	188	438
750	3.7	1.8	203	417

171. Below, I have provided Table E showing calculated values of λ/n_1 and λ/n_2 for *Kuboi*'s red pixels with porphyrin for visible light wavelengths 400 nm and 700 nm, and near infrared wavelengths of greater than 700 nm wavelength. I obtained values of λ/n_1 and λ/n_2 in Table E, using values of n_1 of silicon for different wavelengths from Ex-1023, page 48, Table A-1, and values of n_2 of phthalocyanine compounds at different wavelengths from Ex-1003, page 13, Fig. 7. As seen from the values in Table E, *Kuboi*'s hole pitch of 250 nm falls in the range λ/n_1 to λ/n_2 for at least part of the visible light spectrum (400-700 nm wavelengths) and at least part of the near infrared light spectrum (>700 nm wavelengths). For example, for the 650 nm red light wavelength, λ/n_1 ($650/3.9 = 168$) < Λ (250 nm) < λ/n_2 ($650/2.1 = 302$).

Table E				
λ (nm)	n_1 (Silicon)	n_2 (Phthalocyanine)	λ/n_1(nm)	λ/n_2 (nm)
400	5.8	1.9	68	211
650	3.9	2.1	168	302
700	3.8	1.8	186	389
750	3.7	2.3	203	326

172. In my opinion, therefore, one skilled in the art would have understood that the stated period of *Kuboi*'s hole array falls within the λ/n_1 to λ/n_2 range for light in selected visible and infrared wavelength ranges.

173. Further, one skilled in the art would have understood based on Patent Owner's representations that *Kuboi*'s hole structure would form an HCG. One skilled in the art would have also understood based on Patent Owner's representations that such an HCG would produce an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient based on the near-wavelength and deep-wavelength phenomena. In my opinion, therefore, one skilled in the art would have understood that *Kuboi*'s photodetectors with organic material in their holes would increase the absorption of the light (at selected visible and infrared wavelength ranges) in at least some of *Kuboi*'s photodetectors by at least 1.1 times compared to *like* photodetectors lacking said holes.

174. Third, in my opinion, one skilled in the art would have found that Patent Owner's representations were consistent with those of other prior art teachings. For example, according to *Han* (Ex-1033), "[t]o obtain the same ultimate efficiency as a standard 300 micrometer crystalline silicon wafer, nanohole arrays require less silicon by mass." *Han*, Abstract, 2:4-5. *Han* discloses that "nanoholes can be sized to substantially trap incident light." *Han*, 3:2-3. As shown in Figure 4 of *Han* below, the ultimate efficiency for a device having a semiconductor thickness of about 1.4 μm without nanoholes is approximately 0.12, whereas the ultimate efficiency for a similar device having nanoholes is approximately 0.22. *Han*, Fig. 4. In my opinion, based on a skilled artisan's knowledge of the state of the art before the '871 patent's priority date, the skilled artisan would have understood that nanohole depths of 1.4 μm would increase light absorption by a factor of 1.8 ($0.22/0.12 = 1.8$), which is significantly higher than a factor of 1.1.

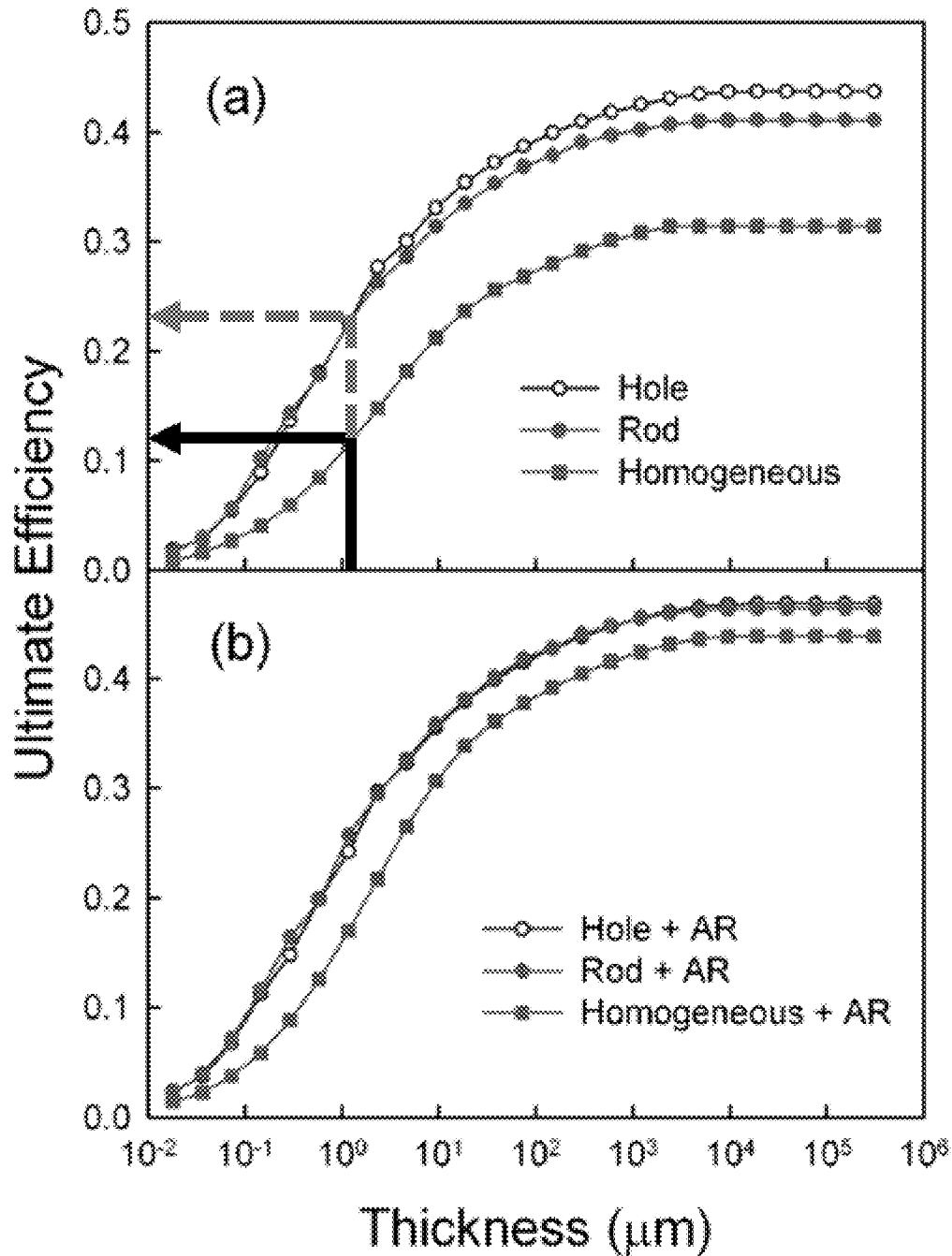


FIG. 4

Han, Fig. 4 (annotated).

175. In my opinion, therefore, based on a skilled artisan's knowledge of the state of the art before the '871 patent's priority date, the skilled artisan would have understood that *Kuboi's*

1.4 μm hole depth would increase by a factor of at least 1.1 the absorption of the light by at least some of *Kuboi*'s photodetectors relative to otherwise like photodetectors lacking said holes, and even if not readily understood, a POSITA would have found such a result not only obvious but also one having a reasonable expectation of success in achieving this increase because *Kuboi* discloses forming nanoholes of 1.4 μm depth.

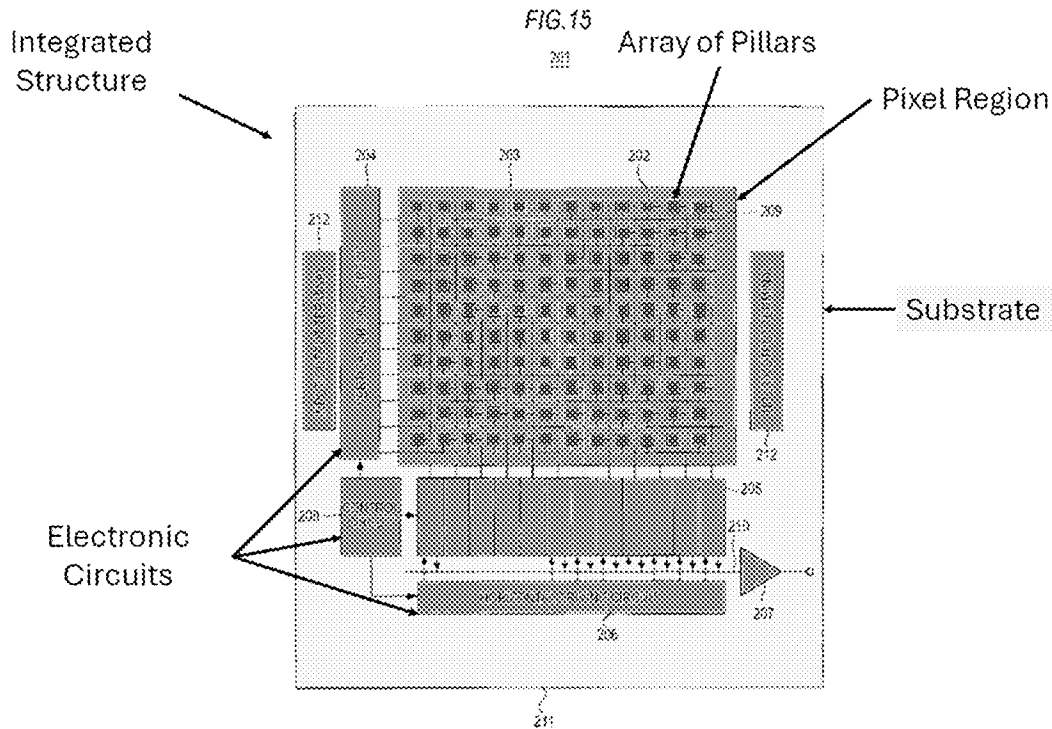
2. Claims 2 and 18:

- a. [2] **"The integrated structure of claim 1, wherein said array of photodetectors is monolithically integrated with SI electronic devices."**
- b. [18] **"The integrate[d] structure of claim 15, in which said array of photodetectors is monolithically integrated with Si electronic devices that include CMOS devices."**

176. In my opinion, *Kuboi* discloses these additional limitations.

177. *Kuboi* discloses "a simplified exemplary configuration of a CMOS solid-state imaging device." *Kuboi*, ¶[48]. *Kuboi*'s imaging device 201 "include[s] a pixel region (so-called ... imaging region) 203 and a peripheral circuit portion which are provided on a semiconductor substrate 211 (i.e., a silicon substrate)." *Kuboi*, ¶[48]. *Kuboi* teaches that "*a pixel and logical circuit portion may be created in advance* and be bonded to the semiconductor substrate on which the semiconductor region 25 having the pixel transistors, the multilayer wiring layer 32, the lower electrode 23, and the like are formed." *Kuboi*, ¶[78] (emphasis added). *Kuboi* also discloses that its logical circuit portion includes vertical driving circuit 204, column signal processing circuits 205, horizontal driving circuit 206, output circuit 207, control circuit 208. *Kuboi*, ¶[49]. One skilled in the art would have understood that each of circuits 204-208 would include electronic devices. Ex-1001, 3 (defining circuit as "a physical device" that may be constructed, for example, by "interconnecting [devices such as] a resistor and a capacitor to a

voltage source”). In my opinion, one skilled in the art would have understood *Kuboi* as teaching that the pixel region (including the array of pillars) is monolithically integrated with the logical circuit portion. *Kuboi*, ¶¶[48]-[49]. *Kuboi*’s monolithically integrated structure is shown below:



Kuboi, Fig. 15 (annotated).

178. *Kuboi* discloses a manufacturing method that forms the pixel region and the logical circuit portion on the same substrate. For example, *Kuboi* discloses a method of forming the pixel region by first forming an element separation region 15 on a silicon semiconductor layer 12. *Kuboi*, ¶[71]. *Kuboi* further discloses that “n⁺-type semiconductor region 17 (corresponding to the front surface side), a n-type semiconductor region 16 (corresponding to an intermediate region), and a p⁺-type semiconductor region 19 (corresponding to the rear surface side) are formed in that order” in the region corresponding to one pixel divided by the element separation region 15. *Kuboi*, ¶[71]. *Kuboi* also discloses that subsequently “a vertical hole 38 such as a trench or a via extending from the p⁺-type semiconductor region 18 to the n⁺-type

semiconductor region is formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶[72]. *Kuboi* explains that a plurality of such holes are formed at necessary intervals. *Kuboi*, ¶[72].

179. *Kuboi* discloses forming electron blocking film 21 on the bottom of the vertical holes 38 and depositing an organic photoelectric conversion film 13 in the vertical holes 38. *Kuboi*, ¶[73]. *Kuboi* discloses forming an upper electrode on the upper surface of semiconductor layer 12 and a lower electrode on its lower surface. *Kuboi*, ¶[77]. Further, *Kuboi* discloses that “the pixel and logical circuit portion may be created in advance” on substrate 12. *Kuboi*, ¶¶[78], [48]-[49]. And as I discussed above, one skilled in the art would have understood *Kuboi*’s logical circuit portion as including a plurality of electronic devices. Ex-1001, 3. In my opinion, because substrate 12 is a silicon substrate, one skilled in the art would have understood that the electronic devices in *Kuboi*’s logical circuit portion would be fabricated in silicon, i.e., they would be Si electronic devices. Further, in my opinion, one skilled in the art would have understood from *Kuboi*’s disclosures that *Kuboi*’s manufacturing method would result in monolithically integrating the array of pillars (i.e., pixel region) with electronic circuits that include active elements for signal processing and transmission (i.e., control circuit 208 and output circuit 207).

180. *Kuboi* also discloses a “CMOS solid-state imaging device” formed on a silicon substrate. *Kuboi*, ¶[48]. In my opinion, one skilled in the art would have understood that because *Kuboi*’s imaging device is a CMOS device, the electronic devices in *Kuboi*’s logical circuit portion would include CMOS devices. This is supported by other prior art that would have been known to one skilled in the art. For example, Ex-1001 defines CMOS as referring “to the process that combines n-channel and p-channel transistors on the same piece of silicon,” where “[t]he transistors are traditionally made of layers of metal, oxide, and semiconductor materials.” Ex-

1001, 4. Thus, one skilled in the art would have understood that the electronic devices in *Kuboi*'s logical circuit portion would include CMOS devices because they are fabricated using the CMOS fabrication process.

181. Further, in my opinion, one skilled in the art would have understood the creating the pixel and logical circuit portion on substrate 12 would include creating the CMOS devices in the logical circuit portion together with the pixel portion on substrate 12. *Kuboi*, ¶¶[78], [48]-[49]. A skilled artisan would have understood that forming the pixel region (including an array of pillars) and logical circuits (including CMOS devices) on the same substrate would result in monolithically integrating *Kuboi*'s array of pillars (i.e., pixel region) with Si electronic devices that include CMOS devices.

3. Claims 3, 4, 7, and 15:

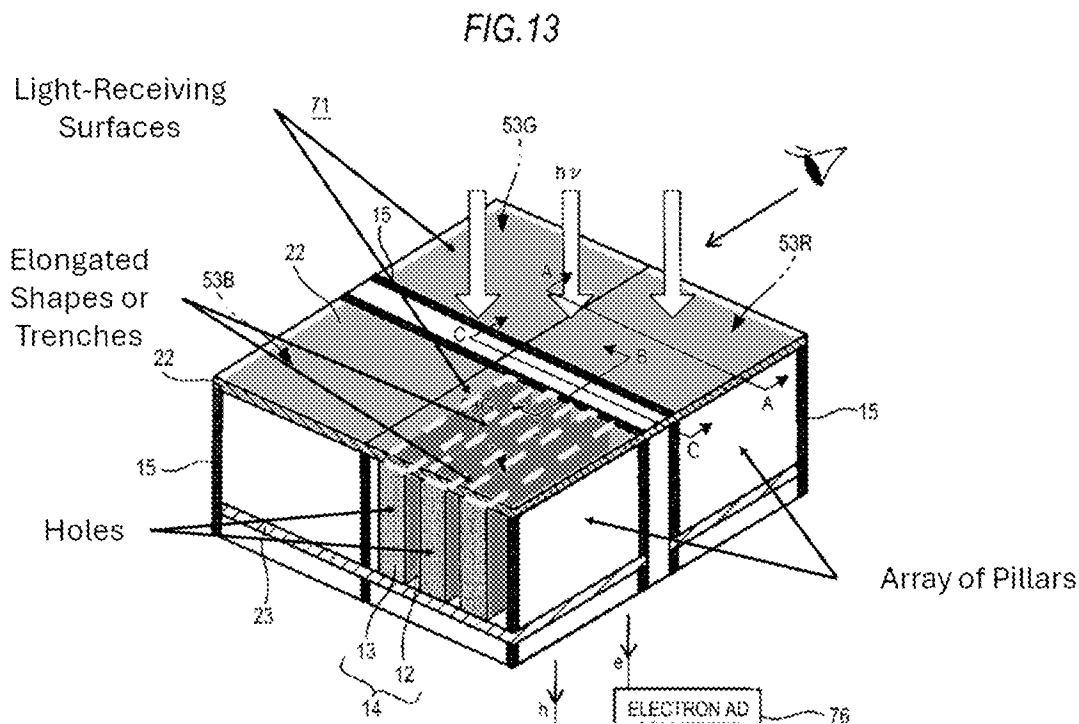
- a. **[3]: “The integrated structure of claim 2, wherein each of at least some of said photodetectors includes at least one of said holes with elongated shapes at the light-receiving surface thereof.**
- b. **[4]: “The integrated structure of claim 2, wherein each of at least some of said photodetectors includes a plurality of said holes with elongated shapes at the light receiving surface thereof.”**
- c. **[7]: “The integrated structure of claim 1, wherein each of at least some of said photodetectors includes at least one of said holes with elongated shapes at the light receiving surface thereof.”**
- d. **[15]: “The integrated structure of claim 1, wherein at least some of said holes are configured as elongated trenches at said light-receiving surfaces.”**

182. In my opinion, *Kuboi* discloses these additional limitations.

183. As I discussed above, each pillar in the array of pillars in *Kuboi*'s integrated structure is a photodetector. *Supra* XI.A.1.b (claim [1a]). Claims 3, 4, and 7 recite “*each of at*

least *some of* said photodetectors includes [at least one/a plurality] of said holes with elongated shapes” (emphases added). And claim 15 recites that “at least some of said holes are configured as elongated trenches.” In my opinion, one skilled in the art would have understood that the term “said photodetectors” in claims 3, 4, and 7 refers to the recitation that “at least *some of* the photodetectors comprise P-doped and N-doped regions and regions therebetween” (emphasis added) of claim 1. As I explain below, at least some of *Kuboi*’s photodetectors (i.e., pixels 53R and 53G) include P-doped and N-doped regions and regions therebetween. And each of those pixels (i.e., pixels 53R and 53G) include a plurality of holes that have elongated shapes.

184. As I discussed for claim [1c], *Kuboi* discloses forming striped shaped holes (or trenches) in the light-receiving surfaces of its pixels (i.e., pixels 53R and 53G). *Supra* XI.A.1.d; *Kuboi*, ¶¶[72], [13]-[14], [67], [95]. *Kuboi*’s holes (or trenches) having elongated shapes are illustrated below:



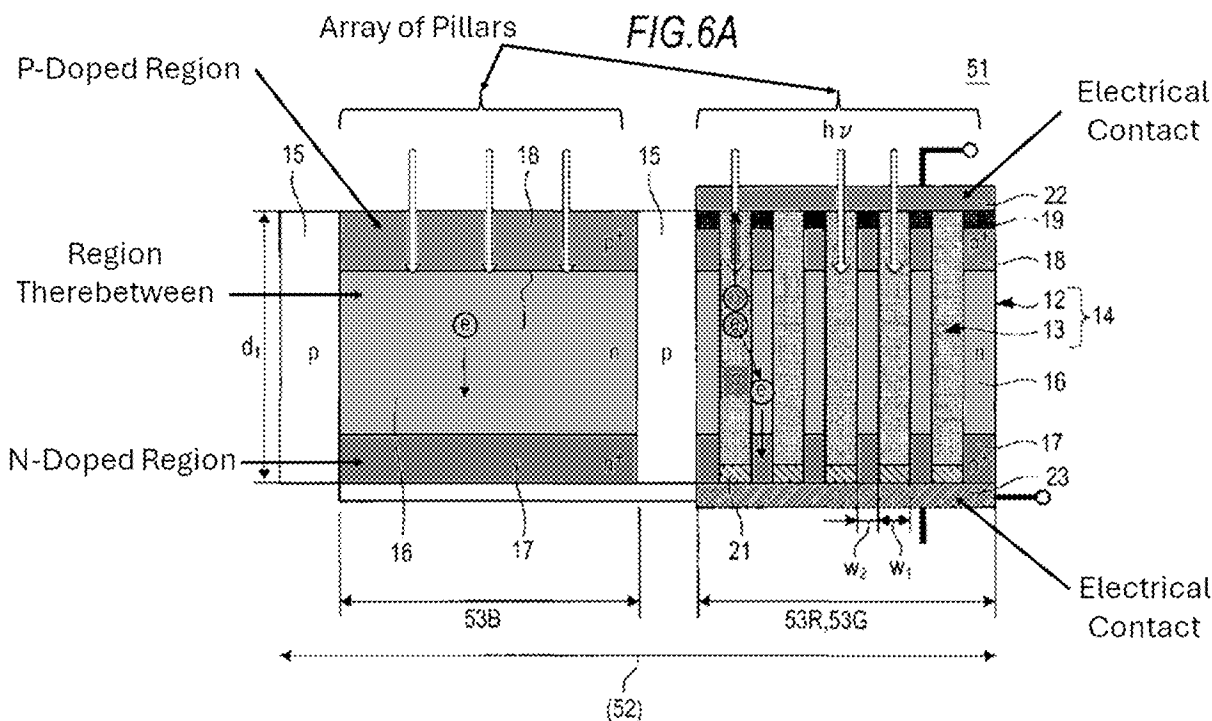
Kuboi, Fig. 13 (annotated).

185. In my opinion, one skilled in the art would have understood from the above disclosures that *Kuboi*'s integrated structure has a plurality of holes (i.e., "at least one," "at least some," or "a plurality of holes"), having an elongated shape (or in the form of elongated trenches) formed at the light-receiving surface, in at least one pillar (i.e., photodetector), as recited in claims 3, 4, 7, or 15. *Supra* XI.A.1.d (claim [1c]).

4. Claim 12: "The integrated structure of claim 1, in which said electrical contacts are configured to provide electrical fields across at least some of said photodetectors."

186. In my opinion, *Kuboi* discloses this additional limitation.

187. As I discussed for claim [1f], *Kuboi*'s electrodes 22 and 23 are "electrical contacts." *Supra* XI.A.1.g. *Kuboi* also discloses that "electrodes 22 and 23 [are] formed on the entire rear and [front] surfaces of the semiconductor layer 12." *Kuboi*, ¶¶[60], [77], [93], [103]. Further, *Kuboi* discloses that a necessary voltage is applied between upper and lower electrodes 22, 23 so that p⁺-type region 18 is at a negative potential and n⁺-type region 17 is at a positive potential. *Kuboi*, ¶¶[64]. The figure below illustrates electrodes 22 and 23.



Kuboi, Fig. 6A (annotated).

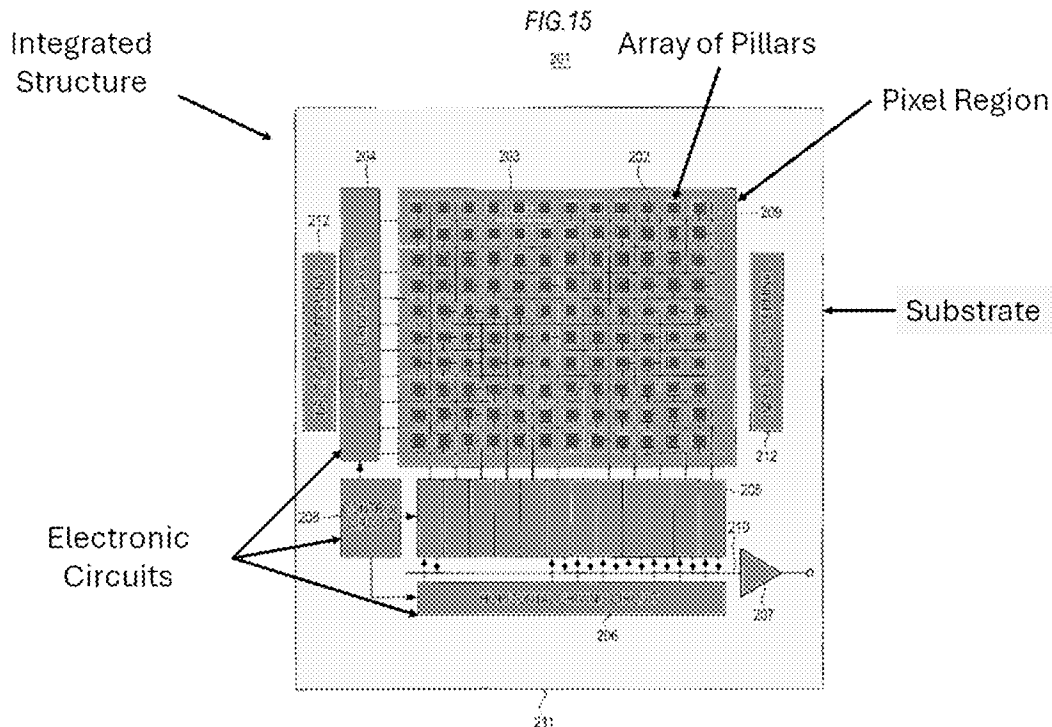
188. As illustrated in the above figure, electrodes 22 and 23 are positioned on opposite sides of pixels (i.e., 53G, 53R). As I also discussed for claim [1a], each of *Kuboi*'s pixels is a photodetector. *Supra* XI.A.1.b. In my opinion, therefore, one skilled in the art would have understood that the voltage applied between electrodes 22, 23 on *Kuboi*'s pixels (i.e., 53G, 53R) provides an electric field across those photodetectors. As a result, one skilled in the art would have also understood that *Kuboi*'s integrated structure includes electrical contacts that provide electrical fields across at least some of *Kuboi*'s photodetectors.

5. Claim 14: “The integrated structure of claim 1, wherein said SI electronic devices include devices for signal processing and transmission.”

189. In my opinion, *Kuboi* discloses this additional limitation.

190. *Kuboi's* discloses that its imaging device 201 includes “a pixel region (so-called an imaging region) 203 and a peripheral circuit portion which are provided on a semiconductor

substrate 211 (e.g., a silicon substrate).” *Kuboi*, ¶[48]. *Kuboi* also discloses that the “peripheral circuit portion is configured to include so-called logical circuits, for example, a vertical driving circuit 204, column signal processing circuits 205, a horizontal driving circuit 206, an output circuit 207, a control circuit 208, and the like,” such as input/output terminal 212. *Kuboi*, ¶[49]. *Kuboi*’s imaging device 201 is illustrated below.



Kuboi, Fig. 15 (annotated).

191. *Kuboi* discloses that “column signal processing circuits 205 are provided, for example, for each column of the pixels 202 and perform signal processing such as noise removal for each pixel column.” *Kuboi*, ¶[52]. As I also discussed above, *Kuboi*’s circuits 204-208 would include electronic devices. Section XI.A.2; Ex-1001, 3. In my opinion, one skilled in the art would have understood that *Kuboi*’s column signal processing circuits would constitute the claimed electronic devices for signal processing. This is supported by other prior art that would have been known to one skilled in the art. For example, Ex-1001 discloses that signal processing

is “a generic term that refers to any technique that manipulates the signal, including but not limited to signal averaging, signal conditioning and signal recognition.” Ex-1001, 10. Thus, because column signal processing circuits 205 include devices that process signals by removing noise, one skilled in the art would have understood that *Kuboi*’s circuits 205 would include devices for signal processing. As I explained above, *Kuboi*’s column signal processing circuits would include Si electronic devices because they are formed on a silicon substrate. *Supra* XI.A.2.

192. *Kuboi* also discloses that output circuit 207 outputs the processed signals and that “input/output terminal 212 exchanges signals with an external device.” As I also discussed above, *Kuboi*’s output circuit 207 would include electronic devices. Section XI.A.2; Ex-1001, 3. In my opinion, one skilled in the art would have understood that *Kuboi*’s output circuit and input/output terminal would include devices for signal transmission. This is supported by other prior art that would have been known to one skilled in the art. For example, Ex-1001 discloses that transmission is “the act of sending information from one location to another.” Ex-1001, 11. Because *Kuboi*’s output circuit and input/output terminal send signals out from *Kuboi*’s imaging device, one skilled in the art would have understood these circuits as including devices for signal transmission. As I explained above, *Kuboi*’s output circuit and input/output terminal would include Si electronic devices because the electronic devices in the output circuit and input/output terminal are formed on a silicon substrate. *Supra* XI.A.2.

B. Claims 1-4, 7, 12, 14, 15, and 18 Are Obvious Over *Kuboi* in View of *Shinohara* (Ground 2)

1. Independent Claim 1

a. [1pre]-[1d], [1f], [1g]

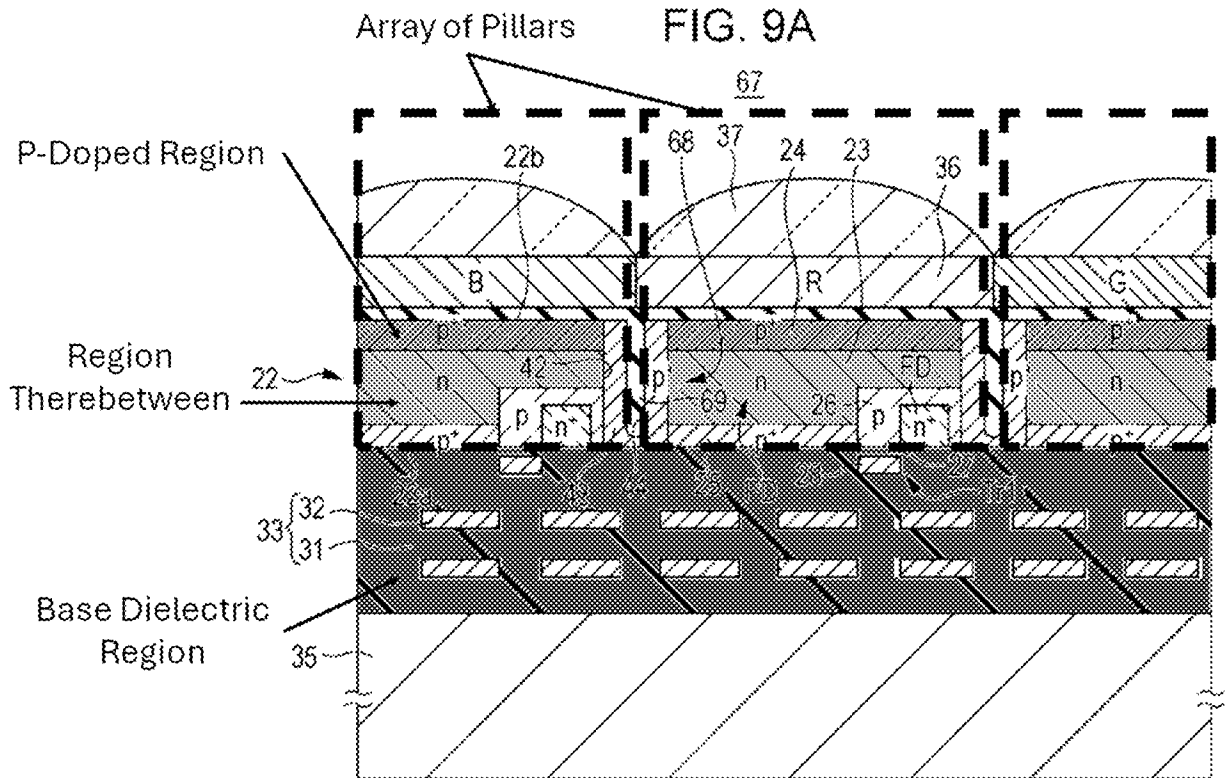
193. In my opinion, *Kuboi* discloses and/or renders obvious these limitations. *Supra* XI.A.1.a-XI.A.1.e (claims [1pre]-[1d]), XI.A.1.g (claim [1f]), XI.A.1.h (claim [1g]).

b. [1e]: “a solid dielectric material forming a base dielectric region for said array;”

194. In my opinion, *Kuboi* in view of *Shinohara* renders obvious this limitation.

195. As I discussed above, *Kuboi* discloses a semiconductor substrate that includes semiconductor region 25 with a multilayer wiring layer 32 that includes a plurality of layers of wirings with interlayer insulating film 31 disposed between the wirings. *Kuboi*, ¶¶[61]-[62], [69]; *supra* XI.A.1.f (claim [1e]). *Kuboi* also discloses bonding the silicon semiconductor substrate with pixels to the semiconductor substrate 25 that includes multilayer wiring layer 32 with interlayer insulating film 31, with insulating film 30 disposed between the substrate with the pixels and semiconductor substrate 25. *Kuboi*, ¶¶[70], [61]-[62], [69]. One skilled in the art would have understood from these disclosures that *Kuboi* discloses bonding a first substrate, including insulating film 31 with a second substrate including *Kuboi*’s image sensor and peripheral circuits to form its imaging device.

196. As I discussed above, *Shinohara* also discloses forming multilayer wiring layer 33, including wires 32 and interlayer insulating film 31, on the same substrate 22 on which pixels B, R, G are formed. *Shinohara*, ¶¶[68]-[89]. In my opinion, *Shinohara*’s interlayer insulating film 31 is a base dielectric region because it is disposed at the base of *Shinohara*’s pixels B, R, G. *Shinohara*’s base dielectric region is illustrated below:



Shinohara, Fig. 9A (annotated).

197. One skilled in the art would have understood that insulating films for separating wires from each other or from an electrical contact, like *Kuboi*'s insulating films 30 or 31, or *Shinohara*'s insulating film 31, are made of silicon oxide or silicon nitride, which are dielectric materials, or at least would have been motivated to use silicon oxide or silicon nitride. As I discussed above, this is because these materials can be fabricated using standard silicon fabrication processes and because these materials provide good barriers to impurity and moisture diffusion. *Supra* XI.A.1.f (claim [1e]); Ex-1020, 34-35; Ex-1025, ¶¶[13]-[14]; Ex-1018, 4-5, 20-21, 23, 34. In my opinion, one skilled in the art would have found it obvious to form *Shinohara*'s insulating film 31 (i.e., base dielectric material) of a solid dielectric material like silicon oxide or silicon nitride. Further, one skilled in the art would also have a reasonable expectation of success

in doing so because methods of formation with such materials in semiconductor fabrication were well known in the art before the '871 patent. Ex-1020, 34-35; Ex-1018, 20-21, 23, 30, 33.

198. Further, as I discuss below with respect to claim 2, a skilled artisan would have found it obvious to modify *Kuboi* in view of *Shinohara* to form the *Kuboi-Shinohara* integrated structure¹ in which *Kuboi*'s array of pillars (i.e., photodetectors) and Si electronic devices are formed on the same substrate (i.e., monolithically integrated). Moreover, one skilled in the art would have understood that in the *Kuboi-Shinohara* integrated structure, *Kuboi*'s insulating film 30 and interlayer insulating film 31 would be formed on the same substrate as *Kuboi*'s array of pillars (i.e., photodetectors). As I also explained for claim [1e] above, one skilled in the art would have further understood that in the *Kuboi-Shinohara* integrated structure, *Kuboi*'s insulating films 30 and 31 would be disposed below *Kuboi*'s array of pillars as illustrated in *Kuboi*'s Figure 1A. *Supra* XI.A.1.f. Further, because *Kuboi*'s insulating films 30 and 31 are made of solid dielectric material, a skilled artisan would have understood that *Kuboi*'s insulating film 30 and/or 31 would form the claimed base dielectric region below *Kuboi*'s array of pillars in the *Kuboi-Shinohara* integrated structure. *Supra* XI.A.1.f.

2. Claim 2: “The integrated structure of claim 1, wherein said array of photodetectors is monolithically integrated with SI electronic devices.”

199. To the extent the Patent Owner argues that *Kuboi* does not disclose monolithic integration, in my opinion, the *Kuboi-Shinohara* combination renders claim 2 obvious.

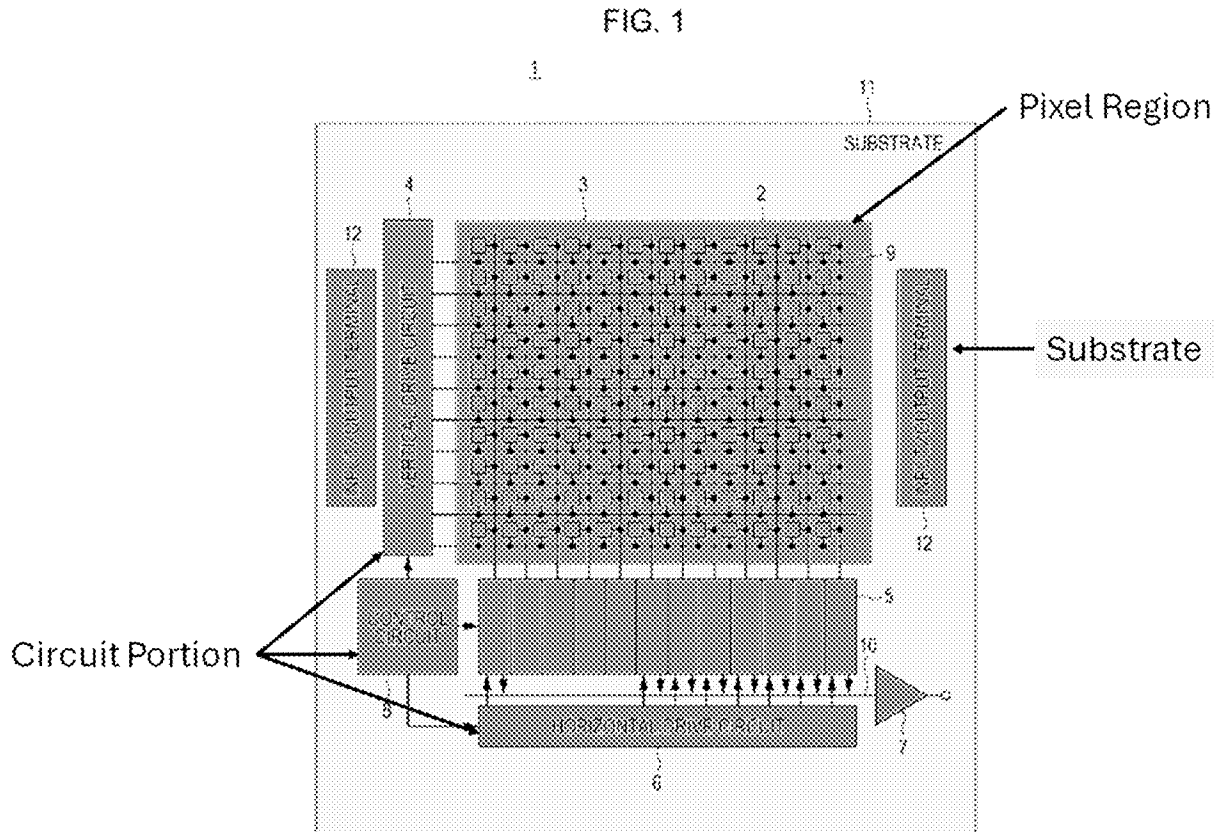
¹ I refer to *Kuboi*'s integrated structure modified by *Shinohara*'s teachings as the *Kuboi-Shinohara* integrated structure in this Declaration.

200. Referring to its Figure 1, *Shinohara* discloses “a MOS solid-state imaging device” that “includes a pixel region (so-called imaging region) 3 in which a plurality of pixels 2 each having a photoelectric conversion portion is regularly arranged in a semiconductor substrate 11, such as a silicon substrate, in a two-dimensional matrix and a peripheral circuit portion.” *Shinohara*, ¶[51]. *Shinohara* also discloses that its “peripheral circuit portion includes so-called logic circuits, such as a vertical drive circuit 4, a column signal processing circuit 5, a horizontal drive circuit 6, an output circuit 7, and a control circuit 8.” *Shinohara*, ¶[52].

201. *Shinohara* discloses a method for manufacturing the imaging device on a “p-type silicon semiconductor substrate 22.” *Shinohara*, ¶[68]. *Shinohara* teaches forming the photodiodes and the separation regions between the photodiodes on the imaging device on a “p-type silicon semiconductor.” *Shinohara*, ¶¶[68]-[82]. According to *Shinohara*, “the floating diffusion portion,” “transfer gate electrode,” “transfer transistor,” “reset transistor,” “amplification transistor,” and “selection transistor” are each “formed in the other part of the p-type semiconductor well region” of the substrate. *Shinohara*, ¶[81]. As a result, “the pixel region in which the pixels are arranged in a two-dimensional matrix is formed.” *Shinohara*, ¶[81]. *Shinohara* discloses that “the peripheral circuit portion (not shown) by CMOS transistors is formed in the periphery of the pixel region.” *Shinohara*, ¶[81]. *Shinohara* also discloses that “the multilayer wiring layer 33 in which a plurality of layers of the wires 32 is disposed with at least one interlayer insulating film 31 provided therebetween is formed on the surface of the semiconductor substrate 22.” *Shinohara*, ¶[82].

202. Thus, *Shinohara* discloses forming the pixel region (i.e., including array of pillars), the peripheral circuit portion, the floating diffusion portion, the transfer gate electrode, transistors (i.e., transfer transistor, reset transistor, amplification transistor, and selection

transistor), and multilayer wiring layer 33 (i.e. electronic circuits) on the same substrate 22. In my opinion, one skilled in the art would have understood that *Shinohara* discloses monolithically integrating its pixel region, and the peripheral circuit portion including various electronic circuits and transistors on the same substrate. *Shinohara*'s integrated structure with these features is illustrated below.



Shinohara, Fig. 1 (annotated).

203. In my opinion, one skilled in the art would have found it obvious to combine *Shinohara*'s teachings with *Kuboi*, resulting in an integrated structure in which *Kuboi*'s array of pillars (i.e., pixel region) is monolithically integrated with electronic circuits (including devices) that include active elements for signal processing and transmission. Ex-1001, 3.

a. Motivation to modify *Kuboi*'s imaging device in view of *Shinohara*'s teaching of monolithic integration

204. Initially, I note that *Kuboi* and *Shinohara* are analogous art to the '871 patent because, like the '871 patent, both *Kuboi* and *Shinohara* aim to improve the light absorption efficiency of their respective imaging devices. The '871 patent is directed to techniques for enhancing photon absorption. '871 patent, Abstract. Similarly, *Kuboi* discloses a solid-state imaging device in which “the light absorption efficiency in the photoelectric conversion portions of the pixels increases, and the charge mobility increases.” *Kuboi*, ¶[16]; *see also Kuboi*, ¶[9]. Likewise, *Shinohara* discloses a solid-state imaging device that improves sensitivity by improving a pixel's light absorption, thereby reducing leakage of charge into an adjacent pixel. *Shinohara*, ¶¶[12]-[13]. Thus, in my opinion, both *Kuboi* and *Shinohara* are analogous art to the '871 patent.

205. As I discussed above, one skilled in the art would have understood from *Shinohara*'s disclosure that the pixel region, the multilayer wiring, and the pixel transistors in *Shinohara*'s imaging device are monolithically formed on a single substrate. *Supra* VIII.B. In my opinion, one skilled in the art would have found it obvious to modify *Kuboi* in view of *Shinohara* to form a monolithically integrated *Kuboi-Shinohara* integrated structure in which *Kuboi*'s array of pillars (i.e., photodetectors) and Si electronic devices are formed on the same substrate.

206. One skilled in the art would have understood that including the pixel region, peripheral circuit portion, pixel transistors, and wiring layer on the same substrate would provide several advantages. For example, monolithically integrating the pixel region and electronic circuits for signal processing and transmission on the same substrate reduces noise and attenuation of the photoelectric signal generated by the pixel region particularly by shortening

the signal travel path in the monolithically integrated imaging device. This is supported by other prior art that would have been known to one skilled in the art.

207. For example, *Hasegawa* (Ex-1028) discloses that “from the viewpoint of curtailing attenuation of the photo-electrical conversion signals and suppressing the superimposition of noise, the length of wiring between the light-receiving parts and the amplifier is configured to be as short as possible.” *Hasegawa*, ¶[9]. *Hasegawa* explains: “Based on this viewpoint, and from the viewpoint of reducing the manufacturing cost of the photodetector, it would be ideal to form the circuits—such as the light-receiving parts, each of which has the PIN photodiode structure, and the amplifier—on the same semiconductor chip.” *Hasegawa*, ¶[9]. Similarly, *Michel* (Ex-1029) discloses that “complete integration of photonic devices into a CMOS process flow will enable low cost photonic functionality within electronic circuits.” *Michel*, Abstract. *Beals* (Ex-1030) discloses that drivers for manufacturing monolithic electronic photonic integrated circuits include “increasing demand for high frequency mixed signal processing, ability to operate at high bandwidths in chip-to-chip as well as within the chip for multicore applications with greater power efficiency and lower manufacturing cost.” *Beals*, 2. And *NXP* teaches that integrating signal processing circuitry and the photodiode on the same substrate “may be more reliable than a discrete solution” and result in a smaller package, which is advantageous for mobile applications. *NXP*, ¶¶[16], [32], [37].

208. In my opinion, one skilled in the art would have been motivated to use *Shinohara*’s monolithic integration method to manufacture and further improve *Kuboi*’s integrated structure to achieve the above-identified benefits such as high bandwidth, low manufacturing cost, and smaller package size. In my opinion, one skilled in the art would have found that using *Shinohara*’s monolithic integration in *Kuboi* would involve nothing more than

the use of a known technique (namely forming the pixel region and all associated electronic circuitry on the same substrate), to improve a similar device (namely *Kuboi*'s integrated structure), in the same way (namely, by improving manufacturing reliability, reducing manufacturing cost and package size, reducing signal attenuation, reducing noise, and improving high-bandwidth performance) of *Kuboi*'s integrated structure.

209. *Kuboi* and *Shinohara* disclose similar integrated structures that include a pixel region and a peripheral circuit portion. Both *Kuboi* and *Shinohara* provide extensive disclosure regarding methods of manufacturing their respective integrated structures. In my opinion, therefore, manufacturing *Kuboi*'s pixel region and associated electronic circuitry, including *Kuboi*'s pixel transistors, using *Shinohara*'s monolithic integration techniques would have been well within the skill level of a person of ordinary skill in the art. Further, in my opinion, a skilled artisan would have had a reasonable expectation of success in implementing *Shinohara*'s teachings for manufacturing *Kuboi*'s integrated structure because it merely requires combining well-known prior elements and manufacturing methods taught by *Shinohara*.

210. It is therefore my opinion that the combination of the teachings of *Kuboi* and *Shinohara* disclose and render obvious the limitations of claim 2.

3. Claims 3, 4, 7, 12, 14, and 15

211. As I have discussed above, *Kuboi* discloses the additional limitations in claims 3, 4, 7, 12, 14, and 15. *Supra* XI.A.3, XI.A.4, XI.A.5. In my opinion, one skilled in the art would have also understood that the *Kuboi-Shinohara* device prepared using *Shinohara*'s monolithic integration would still include the features of *Kuboi* identified above for claims 3, 4, 7, 12, 14, and 15. It is my opinion therefore that the *Kuboi-Shinohara* combination renders obvious claims 3, 4, 7, 12, 14, and 15.

4. Claim 18: “The integrate[d] structure of claim 15, in which said array of photodetectors is monolithically integrated with Si electronic devices that include CMOS devices.”

212. In my opinion, the *Kuboi-Shinohara* combination renders this limitation obvious. In particular, as I discussed above for claim 2, the *Kuboi* and *Shinohara* combination discloses these limitations. *Supra* XI.B.2.

213. Specifically, *Kuboi* discloses a “CMOS solid-state imaging device” formed on a silicon substrate. *Kuboi*, ¶[48]. Similarly, *Shinohara* discloses a “CMOS Solid-State Imaging Device.” *Shinohara*, ¶[50]. As I explained above, in my opinion, one skilled in the art would have understood that because both *Kuboi*’s and *Shinohara*’s imaging devices are CMOS devices, they would include electronic devices that are CMOS devices. Ex-1001, 4. In my opinion, one skilled in the art would have also understood that forming *Kuboi*’s photodetectors and Si electronic devices, as I discussed for claim 2, would yield an imaging device that includes *Kuboi*’s array of photodetectors monolithically integrated with Si electronic devices that include CMOS devices. *Supra* XI.B.2.

C. Claims 1-4, 7, 8, 15, 17, and 18 are Obvious Over *Yu* in view of *Kuboi* and *Shinohara* (Ground 3)

1. Independent Claim 1

a. [1pre]: “An integrated structure comprising:”

214. In my opinion, to the extent the preamble limits the scope of claim 1, *Yu* discloses the preamble.

215. *Yu* discloses an apparatus comprising the image sensor and a control circuit that includes a decoder, a transimpedance amplifier, a multiplexer circuit, and other readout circuitry components. *Yu*, ¶[115]. According to *Yu*, the “image sensor and the control circuit can be formed as an integrated circuit or chip.” *Yu*, ¶[115].

216. *Yu*'s imaging device is an "integrated structure" because it combines various structures, for example, an image sensor and a control circuit. *Yu*'s integrated structure is illustrated below:

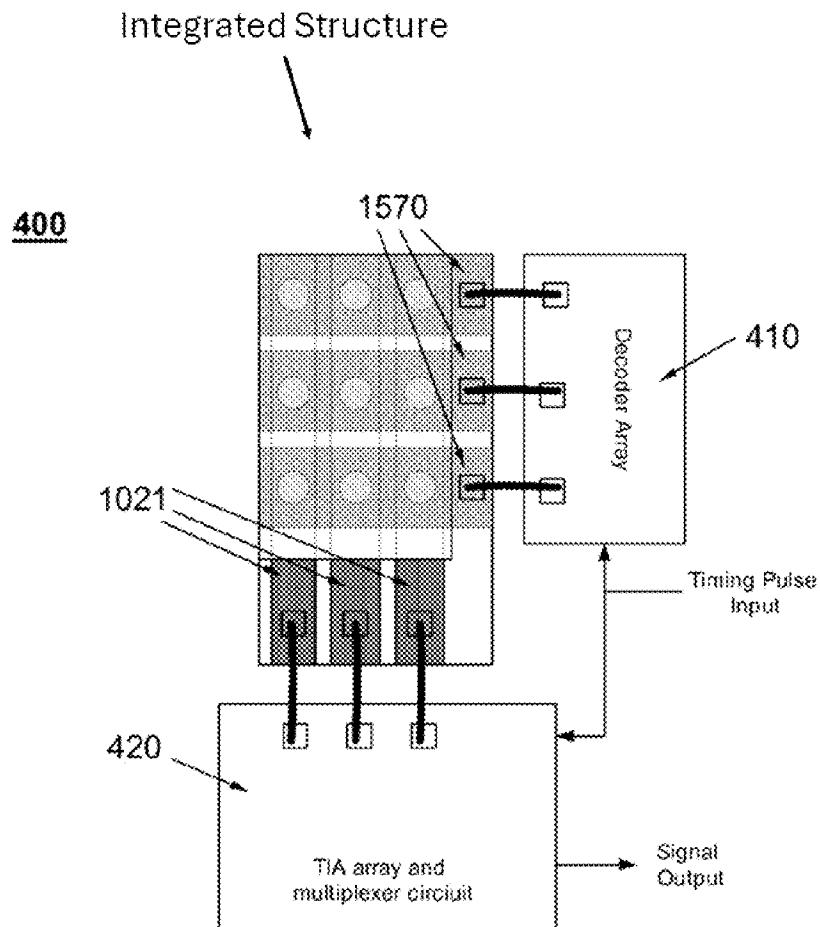


FIG. 4

Yu, Fig. 4 (annotated).

- b. [1a]: “an array of pillars² comprising Si, Ge, and/or SiGe alloy semiconductor material wherein at least some of the pillars are configured as photodetectors that have respective light-receiving surfaces and have sides;”**

217. In my opinion, *Yu* discloses this limitation.

218. *Yu* discloses an image sensor that has a plurality of pixels. *Yu*, ¶¶[7], [17], [25]. *Yu* discloses that the pixels “are organized into a plurality of ‘rows’” and “into a plurality of ‘columns.’” *Yu*, ¶¶[51], [9] (“image sensor can comprise first, second, third[,] and fourth pixels”), [17], [25], [48].

219. *Yu* discloses that each of its pixels “has at least a nanopillar that can convert light impinging thereon to electrical signals (e.g. a nanopillar having a vertical p-n or p-i-n junction).” *Yu*, ¶[48]. *Yu* explains that its pixels are “fabricated to absorb light in the ultraviolet (UV), visible (VIS)[,] or infrared (IR) regions and to generate a detectable electrical signal.” *Yu*, ¶¶[48], [52], [58]-[59], [131]-[132]. In my opinion, one skilled in the art would have understood that *Yu*’s pixels are photodetectors because its pixels absorb light and generate a detectable electrical signal.

220. According to *Yu*, “each pixel has at least one nanopillar, which comprises a p-n or p-i-n junction extending in the length direction of the nanopillar.” *Yu*, ¶[52]. *Yu* explains that each of its pixel can include “three- or four nanopillar[s]” and that “pixels having additional

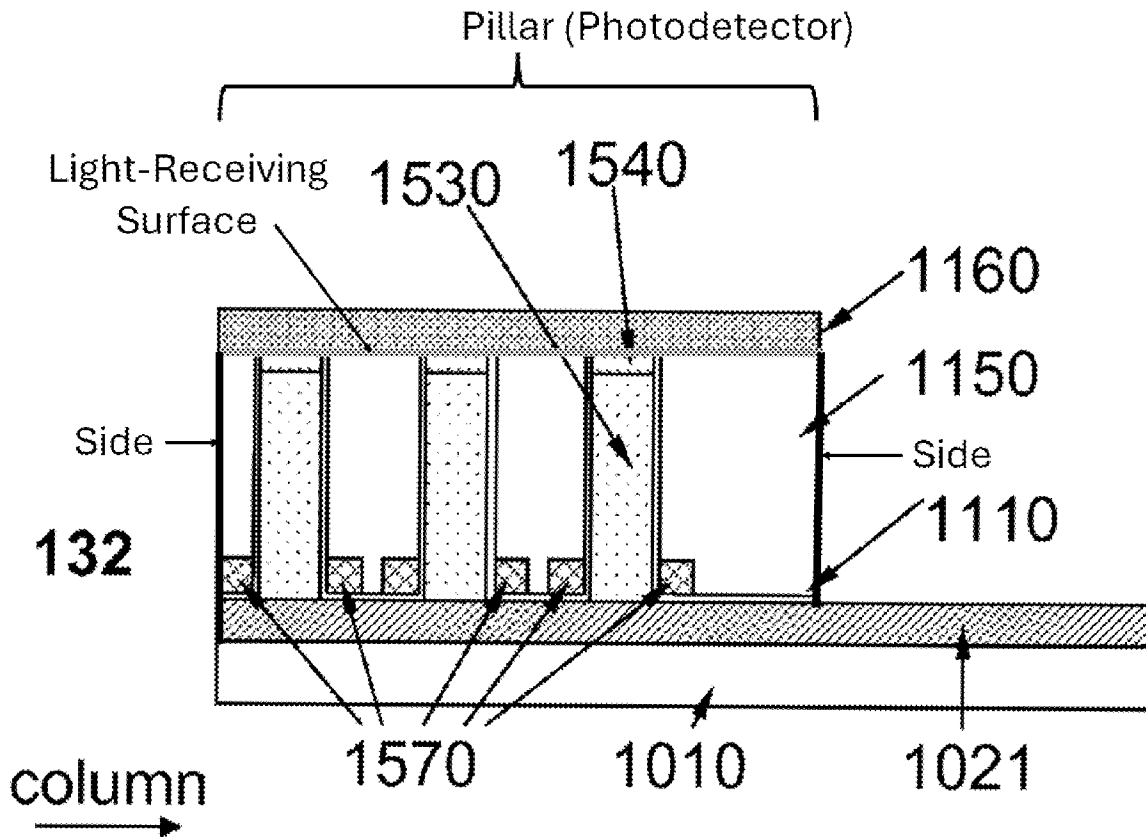
² My mapping of the ’871 patent claims to *Yu*, including the terms “array of pillars” and “elongated trenches [that] crisscross” (claim 17) is consistent with how Patent Owner maps the same claims to Petitioners’ accused products in the parallel litigation. L-1.

pillars are also possible.” *Yu*, ¶[129]. *Yu* also discloses that its nanopillars “extend vertically from the substrate.” *Yu*, ¶[49].

221. In my opinion, *Yu*’s “nanopillars” are not the claimed pillars. Rather, in my opinion, *Yu*’s pixel is the claimed pillar and each such pixel may have more than one nanopillar. Because *Yu*’s pixels can be arranged in rows and columns, in my opinion, *Yu* discloses an array of pixels (i.e., pillars) arranged in an array of rows and columns.

222. *Yu* discloses “nanopillars extending vertically from a substrate.” *Yu*, ¶¶[48]-[49]. *Yu* also discloses that the one or more nanopillars in its pixel and its substrate “can comprise suitable semiconductor materials and/or metals such as Si.” *Yu*, ¶¶[55], [15], [27], [62]. Because the nanopillars in its pixels (i.e., pillars) include Si, one skilled in the art would have understood that *Yu*’s array of pixels (i.e., array of pillars) comprise Si semiconductor material.

223. *Yu* also discloses planarizing an upper surface of oxide or polymer 1150 to expose junction layer 1540 of nanopillars 1500. *Yu*, ¶[88]. *Yu* further discloses that “micro lenses can be fabricated on upper ends of the nanopillars 1500 to enhance light collection.” *Yu*, ¶[95]. A POSITA would have understood this disclosure to mean that the upper ends of the nanopillars 1500 nearer to junction layer 1540 receive light from the micro lenses. *Yu*’s pillar having sides and a light-receiving surface on the top of junction layer 1540 is illustrated below:



Yu, Fig. 1, step 132 (annotated).

224. As another example, *Yu*'s pixel (i.e., pillar), including multiple nanopillars, and having sides and a light-receiving surface is illustrated below:

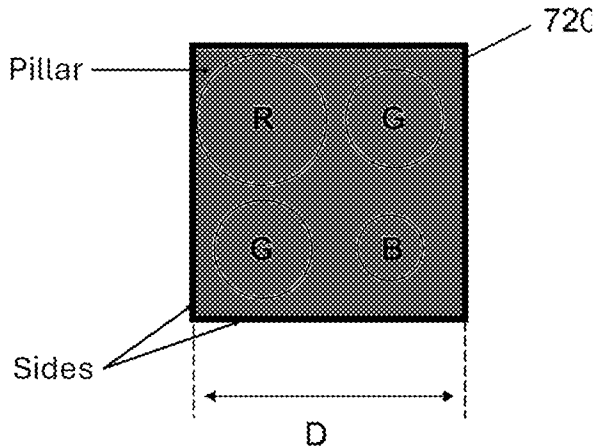


FIG. 7B

Yu, Fig. 7B (annotated)

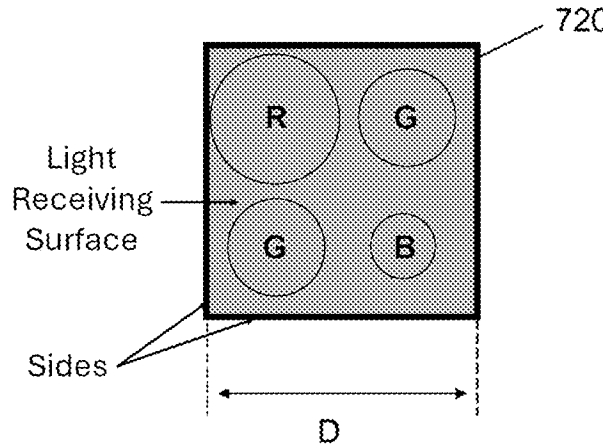


FIG. 7B

Yu, Fig. 7B (annotated)

225. As I discussed above, *Yu* discloses that its image sensor includes a plurality of pixels (i.e., pillars). *Yu*, ¶¶[7],[9], [17], [25], [51]. Therefore, although only one pillar is illustrated above, in my opinion, one skilled in the art would have understood that each of *Yu*'s pillars would have a light-receiving surface and sides similar to that illustrated above.

- c. **[1b]: “wherein at least some of the photodetectors comprise P-doped and N-doped regions and regions therebetween and are configured to respond to illumination with light in selected visible and infrared wavelength ranges by generating electrical charge carriers;”**

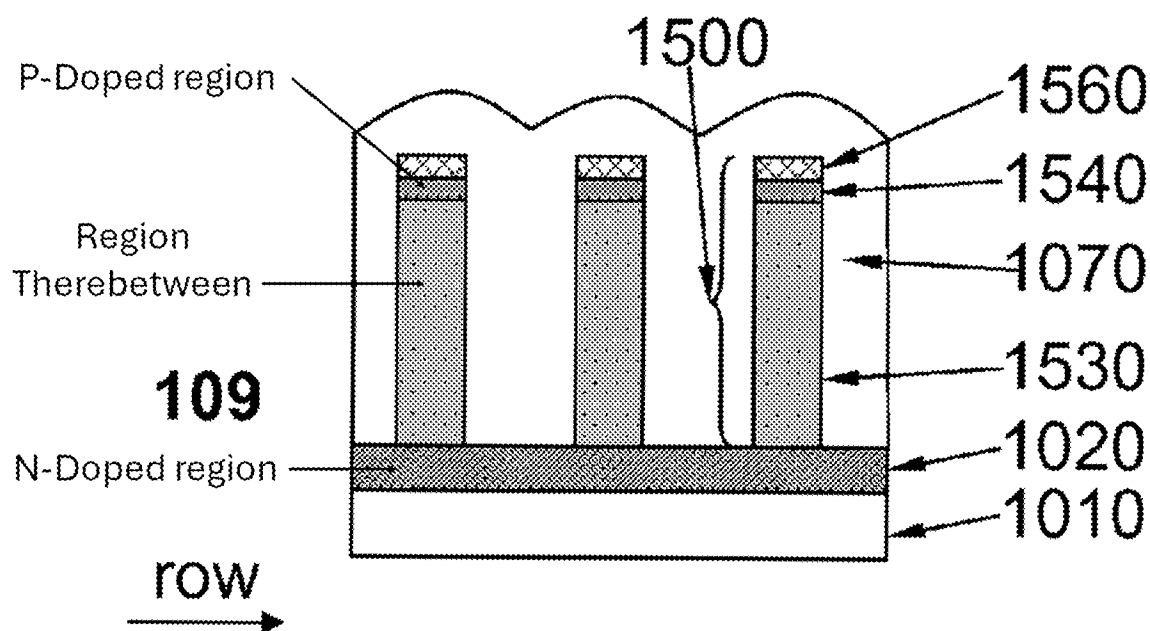
226. In my opinion, *Yu* discloses this limitation.

227. As I discussed for claim [1a], *Yu* discloses an array of pixels (or pillars), each of which is a photodetector and has multiple nanopillars. *Supra* XI.C.1.b.

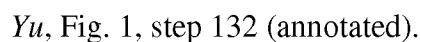
228. As I also discussed for claim [1a], *Yu*'s “nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si.” *Supra* XI.C.1.b; *Yu*, ¶¶[55], [27]. *Yu* discloses that its “substrate has an oxide layer 1010, a heavily doped layer (HDL) 1020 on the layer 1010[,] and an epi layer 1030 on the HDL layer 1020.” *Yu*, ¶[62]. *Yu* also discloses

its substrate can have the following doping profile – “the HDL layer 1020 is n-[and] the epi layer 1030 is i” (i.e. intrinsic). *Yu*, ¶[62]. *Yu* discloses that “junction layer 1040 is formed on the epi layer 1030” and that “if the HDL 1020 is n type, the junction layer 1040 is p type.” *Yu*, ¶[63].

229. As I discussed above, one skilled in the art would have understood that the process of implanting impurities into silicon material is known as “doping.” Ex-1001, 5; Ex-1018, 37; Ex-1020, 4; Ex-1018, 4. Further, in my opinion, one skilled in the art would have understood that *Yu*’s n- doped layer HDL 1020 would constitute the claimed N-doped region and the p type junction layer 1540 which is part of the junction layer 1040 would constitute the claimed P-doped region. One skilled in the art would also have understood that, because the intrinsic epi layer is disposed between P-doped junction layer 1040 and the N-doped HDL 1020, the epi layer would constitute the claimed region therebetween. The figures below illustrate “junction layer 1540 which is part of the junction layer 1040” (*Yu*, ¶[68], i.e., “P-doped region”), intrinsic epi layer (i.e., “region therebetween”), and HDL 1020 (i.e., N-doped region).



Yu, Fig. 1, step 109 (annotated).



230. *Yu* discloses that each pixel of its image sensor “has at least a nanopillar that can convert light impinging thereon to electrical signals.” *Yu*, ¶¶[48], [17]. *Yu* explains that its pixels are “fabricated to absorb light in the ultraviolet (UV), visible (VIS)[,] or infrared (IR) regions and to generate a detectable electrical signal in response thereto.” *Yu*, ¶[48]. Because *Yu*’s pixels are fabricated to absorb visible or infrared light, in my opinion, one skilled in the art would have understood that *Yu*’s pixels (i.e., photodetectors) are configured to convert light in selected visible and infrared wavelength ranges incident on said array of pillars into electrical signals (i.e., “electrical charge carriers”).

- d. **[1c]: “one or more holes that are deliberately formed into the light-receiving surfaces, have elongated and/or other shapes at said light-receiving surfaces, extend into the photodetectors to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;”**

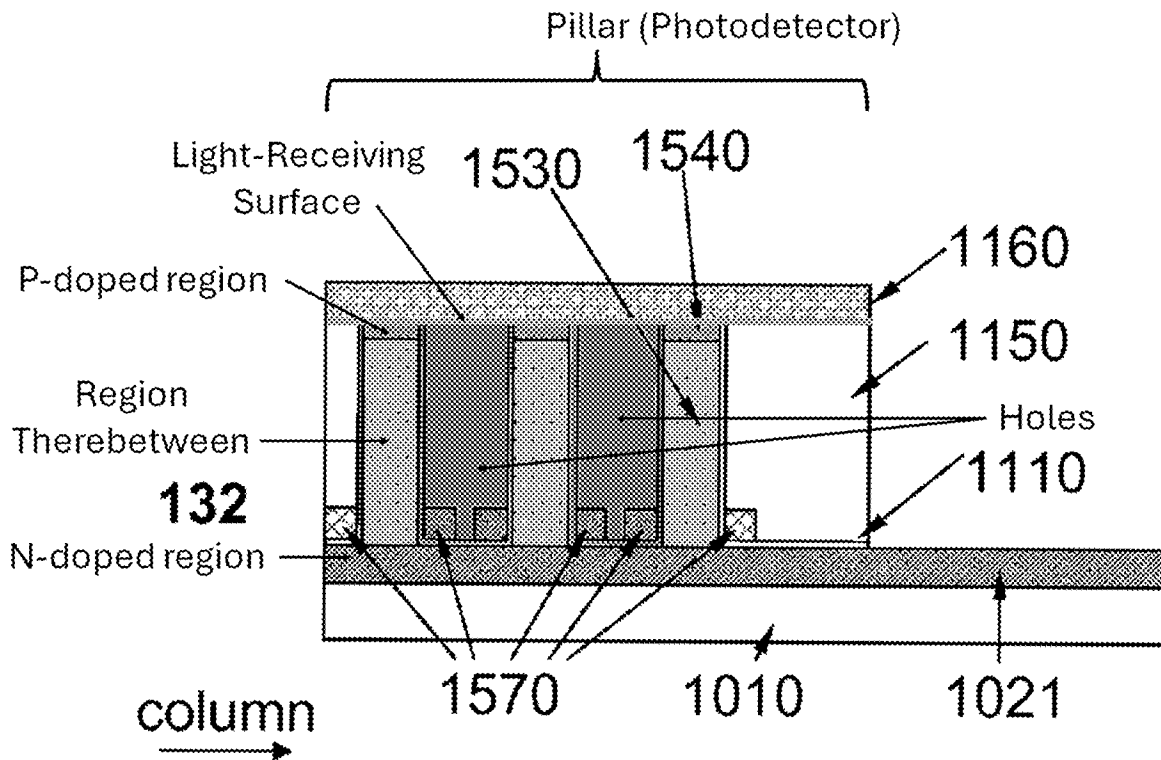
231. In my opinion, *Yu* renders this limitation obvious.

232. *Yu* discloses starting with a substrate and forming an oxide layer, a heavily doped layer (HDL) on the oxide layer, and an epi layer on the HDL layer. *Yu*, ¶[62]. *Yu* also discloses forming a junction layer on the epi layer. *Yu*, ¶[63]. According to *Yu*, “the exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500.” *Yu*, ¶¶[68], [76].

233. In my opinion, the spaces between nanopillars formed by the deep etching process are the holes in *Yu*’s pixel. The deep-etching process removes semiconductor material from *Yu*’s semiconductor layer until the HDL layer 1020 is exposed. In my opinion, one skilled in the art would have understood that removal of semiconductor material from a semiconductor layer in this manner would form indentations or trenches in the semiconductor layer. One skilled in the art would have further understood that such indentations or trenches would constitute holes in *Yu*’s semiconductor layer that constitutes *Yu*’s pillars.

234. Further, one skilled in the art would have understood that because *Yu*’s holes are formed by etching the junction layer, *Yu*’s holes are formed in the light-receiving surfaces of *Yu*’s pillars. This is because *Yu*’s light-receiving surface is located on the upper surface of the junction layer (*supra* XI.A.1.b (claim [1a])), and etching the junction layer would require the etching process to pass through the light-receiving surfaces of *Yu*’s pillars.

235. In my opinion, one skilled in the art would have also understood that the holes in *Yu*'s pillars are deliberately formed because they are formed by a purposeful deep-etch process. *Yu*'s holes are illustrated below. As shown in the figure below, a plurality of (i.e., two) holes are included in each pillar (i.e., pixel).

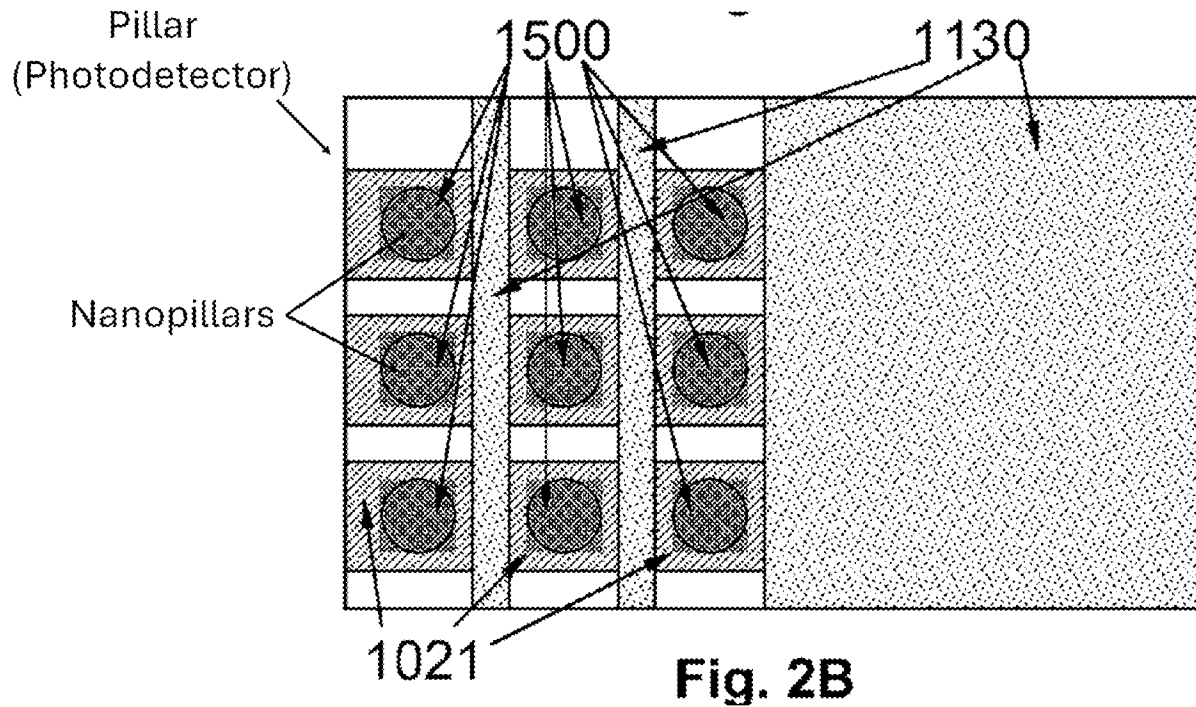


Yu, Fig. 1, step 132 (annotated).

236. *Yu* discloses that its epi layer (i.e., “region therebetween”) can be “about 3000 to 10000 nm thick.” *Yu*, ¶[62]. *Yu* also discloses that “the thickness of the junction layer 1040 [(i.e., ‘P-doped region’)] is from 10 to 200 nm.” *Yu*, ¶[63]. Thus, each hole in *Yu* can have a depth ranging between 3,010-10,200 nm. I note that *Yu*'s disclosed depth range of between 3,010-10,200 nm overlaps with the claimed range of 3,000 to 10,000 nanometers. Further, because *Yu* discloses hole depths of 3,010-10,200 nm, one skilled in the art would have understood that it would be possible to form *Yu*'s device with holes having a depth that falls in the range 3,010-

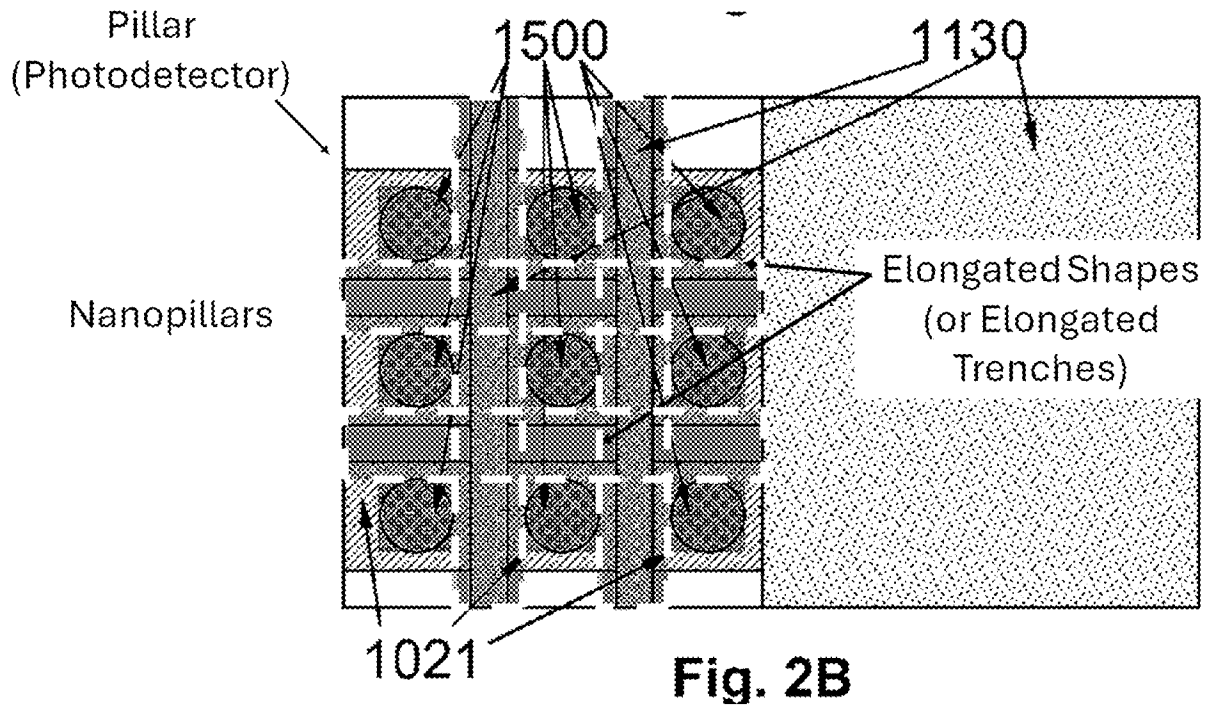
10,000 nm. A skilled artisan would have also understood that such a device would meet the hole depth requirements of claim [1c]. Therefore, because of the substantial overlap in the depth range disclosed by *Yu* and the claimed depth range, in my opinion, one skilled in the art would have found the claimed depth range 3,000 to 10,000 nanometers obvious based on *Yu*'s disclosure. Further, in my opinion, one skilled in the art would have a reasonable expectation of success in forming *Yu*'s device with holes having depths of between 3,000 to 10,000 nanometers, because *Yu* already discloses forming imaging devices that can have holes having depths in the 3,010 to 10,200 nanometer range.

237. *Yu* discloses that its “nanopillars can have any suitable cross-sectional shape such as a circle, a square, [or] a hexagon.” *Yu*, ¶[57]. Figure 2B of *Yu* illustrates a plan view of *Yu*'s pillar where each nanopillar has a generally circular cross-sectional shape. Below, I have provided a modified version of *Yu*'s Figure 2B in which each nanopillar has a generally square or rectangular cross-sectional shape.



Yu, Fig. 2B (annotated).

238. In my opinion, a skilled artisan would have understood that the square- or rectangular-shaped nanopillars illustrated in the above figure would be formed by deep etching a substrate to form trenches oriented generally perpendicular to each other. *Yu*, ¶¶[68], [76]. I have illustrated trenches (or holes) having elongated shapes in the figure below.



Yu, Fig. 2B (annotated).

239. *Yu* discloses that the “space between the nanopillars 1500 is filled by an oxide or a polymer 1150 such as silicon oxide or polyimide.” *Yu*, ¶[87]. As I discussed above, silicon oxide is a solid dielectric material. *Supra* XI.A.1.d; Ex-1020, 34-35; Ex-1018, 20-21, 23. In my opinion, therefore, one skilled in the art would have understood that *Yu*’s holes are filled with solid dielectric material.

e. [1d]: “side-isolation comprising solid material at said sides of at least some of the photodetectors;”

240. In my opinion, *Yu* discloses this limitation.

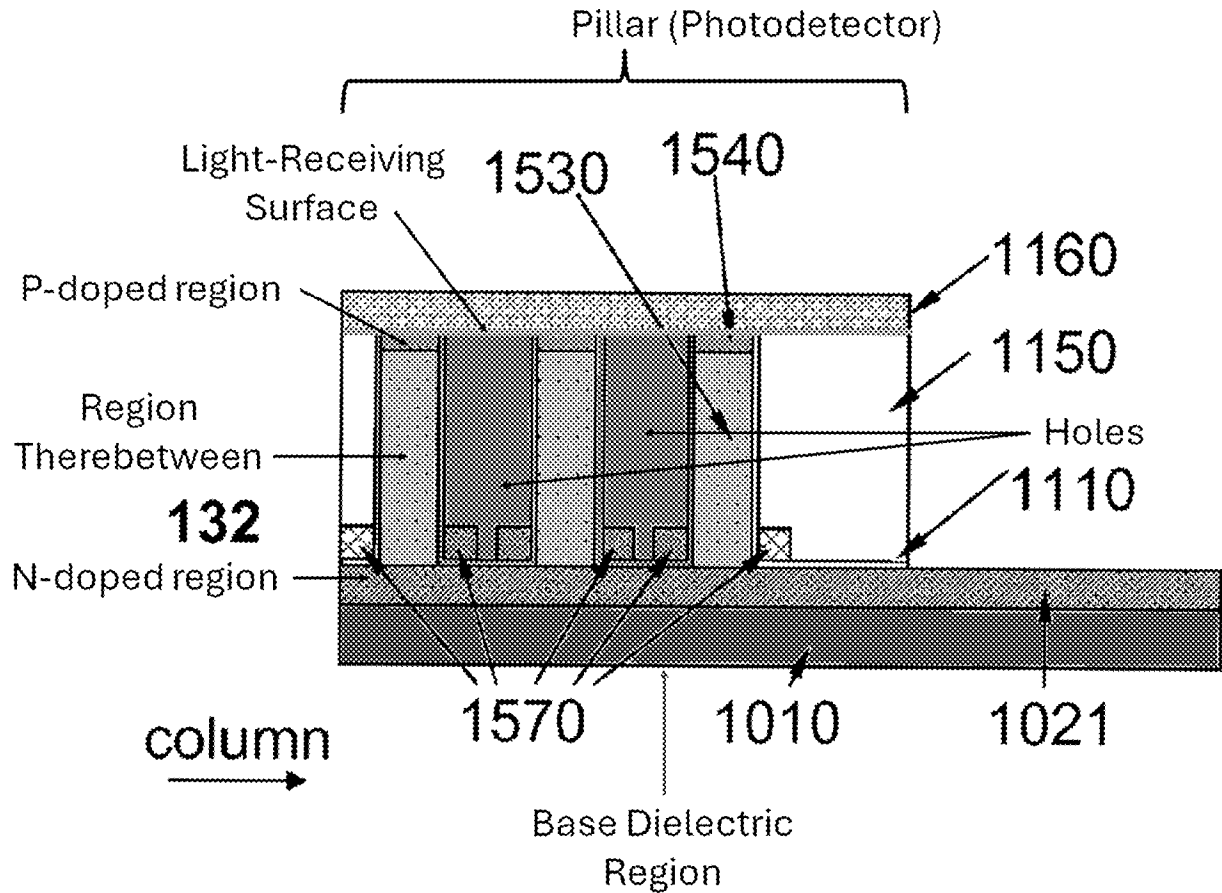
241. As I discussed for claim [1a], *Yu* discloses an array of pixels (or pillars), each of which is a photodetector and has multiple nanopillars. *Supra* XI.C.1.b. *Yu* also discloses that a cladding may surround some or all image sensor pixels, and that the cladding may be formed from silicon nitride. *Yu*, ¶[133]. One skilled in the art would have understood that silicon nitride cladding on the sides of *Yu*’s pixels (i.e., a photodetector) provides side isolation, as claimed,

because such a layer provides insulation or passivation to protect the pixels from impurities, moisture, and scratches. This is supported by other prior art that a skilled artisan would have been aware of. For example, Ex-1018 discloses that in the fabrication of discrete devices and integrated circuits on silicon substrates, “[d]ielectric layers such as silicon dioxide and silicon nitride are used” for various purposes including “passivation to protect devices from impurities, moisture, and scratches.” Ex-1018, 20, 33.

f. [1e]: “a solid dielectric material forming a base dielectric region for said array;”

242. In my opinion, *Yu* discloses or renders obvious this limitation.

243. *Yu* discloses “a silicon-on-insulator (SOI)-type substrate or silicon-on-glass (SG)-type substrate is provided.” *Yu*, ¶¶[62], [15], [102]. *Yu* explains that such a “substrate has an oxide layer 1010.” *Yu*, ¶¶[62], [102]. In my opinion, one skilled in the art would have understood that oxide layer 1010 in *Yu*’s substrate is the base dielectric layer. This is for two reasons. First, as I discussed above, a skilled artisan would have understood or at least found it obvious that *Yu*’s oxide layer 1010 is a solid dielectric material because such oxide layers are fabricated by oxidizing solid silicon material. *Supra* XI.A.1.d; Ex-1020, 34-35; Ex-1018, 20-21, 23. Second, *Yu*’s oxide layer is disposed below (i.e. at the base of) *Yu*’s pillars. In my opinion, therefore, one skilled in the art would have found it obvious that *Yu*’s oxide layer 1010 is formed of a solid dielectric material and constitutes *Yu*’s base dielectric layer. *Yu*’s base dielectric layer is illustrated in the figure below.



Yu , Fig. 1, step 132 (annotated).

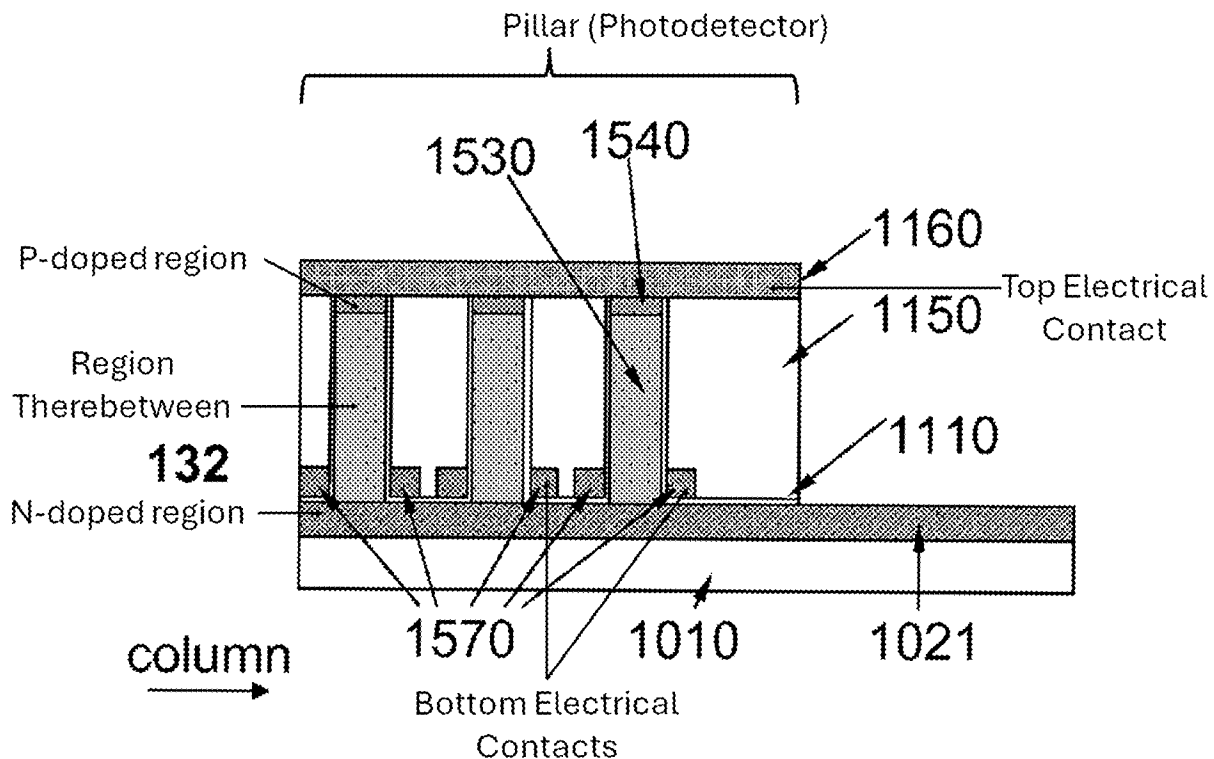
- g. [1f] “electrical contacts configured to provide electrical pathways to at least some of the photodetectors, including for selected reverse-biasing thereof;”**

244. In my opinion, the combination of *Yu* and *Kuboi* renders this limitation obvious.

245. *Yu* discloses that during fabrication of its image sensor, “metal layer 1140 is deposited.” *Yu*, ¶[85]. *Yu* explains that the “portion of the metal layer 1140 deposited around the lower end of the nanopillars 1500 forms the gate electrodes and gate lines 1570.” *Yu*, ¶[85]. *Yu* also discloses applying a gate voltage to one of the gate lines 1570 “to allow electrical current through the nanopillars.” *Yu*, ¶[114]. Because the gate electrodes and gate lines 1570 facilitate flow of electrical current through *Yu*’s nanopillars, one skilled in the art would have understood

that metal layer 1140 forming the gate electrodes and gate lines 1570 constitutes *Yu*'s electrical contacts (i.e., gate electrodes and gate lines).

246. *Yu* further discloses that “a transparent conductive layer (TCL) 1160, such as ITO or aluminum doped zinc oxide (AZO)[.] is deposited.” *Yu*, ¶¶[89], [27], [53]. *Yu* also discloses “applying a bias voltage to the TCL layer 1160.” *Yu*, ¶[114]. Because *Yu*'s TCL 1160 is used to apply a bias voltage, a skilled artisan would have understood that *Yu*'s TCL also constitutes the image sensor's electrical contact. *Yu*'s electrical contacts are illustrated in the figure below.



Yu, Fig. 1, step 132 (annotated).

247. *Yu* also discloses that a method of using the image sensor comprises “applying a bias voltage to the transparent conductive layer[and] applying a first gate voltage to all the gate lines, the first gate voltage being effective to pinch off electrical current through the nanopillars.” *Yu*, ¶¶[28], [114]. Because *Yu*'s transparent conductive layer and gate lines (i.e., “electrical

contacts”) are used to apply voltage across the nanopillars in *Yu*’s pixels (which are photodetectors, *supra* XI.C.1.b) to pinch off electrical current, *Yu*’s transparent conductive layer and gate lines (i.e., “electrical contacts”) provide electrical pathways to *Yu*’s photodetectors.

248. As I discussed above, *Kuboi* discloses applying reverse biasing to improve the response time of an optoelectronic device and induce carrier multiplication. *Supra* XI.A.1.g (claim [1f]). In my opinion, one skilled in the art would have found it obvious to combine *Kuboi*’s teachings with *Yu*, resulting in the *Yu-Kuboi* integrated structure³ in which *Yu*’s electrical contacts provide electrical pathways for reverse biasing as claimed.

i. Motivation to modify *Yu*’s integrated structure in view of *Kuboi*’s teaching of reverse bias

249. Like the ’871 patent, *Yu* discloses an integrated structure having a plurality of pixels and a control circuit. *Yu*, Abstract, ¶¶[7], [17], [48], [52]; *Supra* XI.C.1.a. *Yu* is analogous art to the ’871 patent because, like the ’871 patent, *Yu*’s image sensor also includes features to improve light absorption. *Yu*, ¶[133]. As also discussed above, *Kuboi* is analogous art to the ’871 patent. *Supra* XI.B.2.a.

250. *Kuboi* discloses applying a reverse bias to a PIN photodetector. *Supra* XI.A.1.g. One skilled in the art would have been motivated to implement *Kuboi*’s teaching of applying reverse bias for operating *Yu*’s integrated structure. In my opinion, a skilled artisan would have understood that applying a reverse bias as taught by *Kuboi* would have decreased the response time of the *Yu-Kuboi* integrated structure by more quickly sweeping charge carriers from the

³ I refer to *Yu*’s integrated structure as modified by *Kuboi*’s teachings as the *Yu-Kuboi* integrated structure.

silicon material. This is supported by other prior art that would have been known to a skilled artisan.

251. For example, it was well known in the art that in a “vertically layered P-i-N diode stack under reverse bias, charge carriers photogenerated within the intrinsic region induce carrier multiplication as they are swept to heavily doped layers.” Ex-1017, ¶[2]. Similarly, Ex-1016 discloses that “[i]n high-speed applications, the PIN phase modulator 260 may be reverse biased, which modifies the width of the depletion region, modulating the carrier density overlap with the optical mode, and thus the speed of the optical mode propagating through the PIN phase modulator 260.” Ex-1016, ¶[49]. As another example, Ex-1018 discloses that “[t]o increase the response speed, i.e., to reduce the drift time, we have to increase the reverse bias.” Ex-1018, 13.

252. In my opinion, one skilled in the art, therefore, would have been motivated to apply *Kuboi*’s reverse biasing teaching when operating *Yu*’s integrated structure to induce carrier multiplication and increase *Yu*’s image sensor’s response speed. One skilled in the art would have found that the combination involves the use of a known technique—applying a reverse bias—to improve a similar device—*Yu*’s integrated structure—in the same way, namely, by sweeping charge carriers towards the electrical contacts by applying a reverse bias across the contacts of *Yu*’s integrated structure.

253. In my opinion, one skilled in the art would have had a reasonable expectation of success in implementing *Kuboi*’s teachings in *Yu*’s integrated structure. Given that *Yu* and *Kuboi* disclose similar imaging devices, and both disclose applying bias voltages to the electrical contacts of their respective image sensors, applying *Kuboi*’s reverse biasing to *Yu*’s integrated structure would have been well within the skill of a person of ordinary skill in the art. In my opinion, one skilled in the art would have had a reasonable expectation of success combining *Yu*

with *Kuboi* because it requires combining well-known prior elements already taught by *Yu* and *Kuboi*.

254. In my opinion, in *Yu*'s integrated structure modified by *Kuboi*, *Yu*'s electrical contacts provide electrical pathways for reverse biasing as claimed.

h. [1g]: “wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to otherwise like photodetectors lacking said holes.”

255. In my opinion, *Yu* discloses or at least renders this limitation obvious in view of the knowledge of a person of ordinary skill in the art.

256. As I explain below, one skilled in the art would have found that *Yu* discloses this limitation based on Patent Owner's statements in the '871 patent. The Patent Owner represents in the '871 patent that a photodetector having the structure disclosed in *Yu* would increase by a factor of at least 10% the absorption of the light relative to an otherwise like photodetector lacking said holes.

257. *Yu* discloses minimum feature size of 50 nm when etching the holes. *Yu*, ¶[65]. In my opinion, one skilled in the art would have understood from this disclosure that *Yu* discloses spacing between its nanopillars is of the order of 50 nm. *Yu* also discloses that preferably its nanopillars have dimensions of 90-150 nm. *Yu*, ¶[57]. In my opinion, one skilled in the art would have understood from this disclosure that preferably the period Λ or center-to-center distance between *Yu*'s holes ranges between about 140-200 nm.

258. As I discussed above, one skilled in the art would have understood that visible light has a wavelength range of 400-700 nm and infrared light has a wavelength range of 750 nm to 1,000 μm or even 2,000 μm . *Supra* XI.A.1.h. Further, as I discussed above, one skilled in the art would have understood that the refractive index n_1 of silicon ranges between about 3.0 to 5.9

(Ex-1027, 9:43-46, Fig. 4) and varies with wavelength. Ex-1023, 49; *supra* XI.A.1.h. For example, the refractive index n_1 of silicon is about 5.8 for light of wavelength 400 nm, 3.7 for light of wavelength 700-750 nm, and about 3.5 for light of wavelength 1,000 nm. Ex-1023, 49; *supra* XI.A.1.h. One skilled in the art would also have understood that the refractive index n_2 of silicon dioxide in *Yu*'s nanopillars would be about 1.5 for the wavelength range of 400 nm to 1,000 nm. Ex-1019, 6, Fig. 1; Ex-1027, 9:43-46, Fig. 4.

259. Below, I have provided a table (Table F) showing calculated values of λ/n_1 and λ/n_2 for visible light wavelengths of 400 nm and 700 nm. I obtained values of λ/n_1 and λ/n_2 in Table F, using values of n_1 of silicon for different wavelengths from Ex-1023, page 48, Table A-1, and values of n_2 of 1.5. As seen from the values in Table F, *Yu*'s hole pitch of 140-200 nm falls within the range λ/n_1 to λ/n_2 for at least a portion of the visible light spectrum. For example, for the 550 nm green light wavelength, λ/n_1 ($550/4.5 = 123$) $< \Lambda$ (140-200 nm) $< \lambda/n_2$ ($550/1.5 = 367$). Similarly, for example, for the 650 nm red light wavelength, λ/n_1 ($650/3.9 = 168$) $< \Lambda$ (200 nm) $< \lambda/n_2$ ($650/1.5 = 467$). As seen from the values in Table F, *Yu*'s hole pitch of 140-200 nm falls within the range λ/n_1 to λ/n_2 for at least a portion of the visible light spectrum.

Table F				
λ (nm)	n_1 (Silicon)	n_2 (Dielectric)	λ/n_1(nm)	λ/n_2 (nm)
400	5.8	1.5	68	267
550	4.5	1.5	123	367
650	3.9	1.5	168	433
700	3.8	1.5	184	467

260. Thus, the stated period of *Yu*'s hole array falls within the λ/n_1 to λ/n_2 range for "selected visible and infrared wavelength ranges." Further, in my opinion, based on Patent

Owner's representations, *Yu*'s pillar-hole structure would form an HCG. And, based on those same representations, in my opinion, such an HCG would produce an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient based on the near-wavelength and deep-wavelength phenomena. In my opinion, therefore, one skilled in the art would have understood that consistent with Patent Owner's representations, *Yu*'s holes increase photon absorption in *Yu*'s device by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said holes.

261. As I explain in detail below, one skilled in the art would have found Patent Owner's representations were consistent with those of other prior art teachings.

262. As I discussed above, *Yu* discloses that each of its holes has a depth ranging between 3,010-10,200 nm. *Supra* XI.C.1.d. In my opinion, one skilled in the art would have found it obvious that microstructures like *Yu*'s 3,010-10,000 nm depth holes would increase photon absorption by at least 10% over a similar device lacking the holes.

263. As I discussed above, *Han* discloses that "[t]o obtain the same ultimate efficiency as a standard 300 micrometer crystalline silicon wafer, nanohole arrays require less silicon by mass." *Han*, Abstract, 2:4-5; *supra* XI.A.1.h. *Han* discloses that "nanoholes can be sized to substantially trap incident light." *Han*, 3:2-3; *supra* XI.A.1.h. As shown in Figure 4 of *Han* below the ultimate efficiency for a device having a semiconductor thickness of about 3,010 nm (3.01 μm) without nanoholes is approximately 0.15, whereas the ultimate efficiency for a similar device with nanoholes of 3,010 nm (3.01 μm) depth is approximately 0.27. In my opinion, before the earliest priority date of the '871 patent, one skilled in the art would have understood that *Yu*'s hole depths of 3,010 nm (3.01 μm) would increase light absorption by a factor of 1.8 ($0.27/0.15 = 1.8$), which is significantly higher than a factor of 1.1.

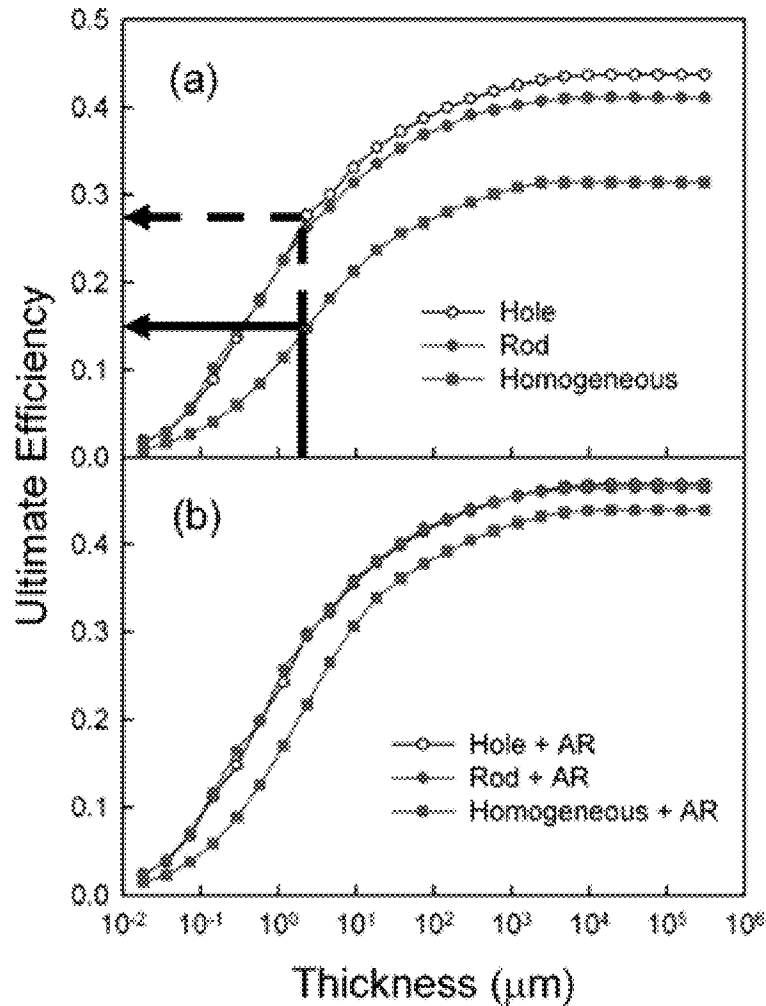


FIG. 4

Han, Fig. 4 (annotated).

264. Similarly, as shown in Figure 4 of *Han* below the ultimate efficiency for a device having a semiconductor thickness of about 10,200 nm (10.2 μm) is approximately 0.22, whereas the ultimate efficiency for a similar device having a semiconductor with nanoholes of 10,200 nm (10.2 μm) depth is approximately 0.33. In my opinion, before the earliest priority date of the '360 Patent, one skilled in the art would have understood that *Yu*'s hole depths of 10,200 nm (10.2 μm) would increase light absorption by a factor of 1.5 ($0.33/0.22 = 1.5$), which is significantly higher than a factor of 1.1.

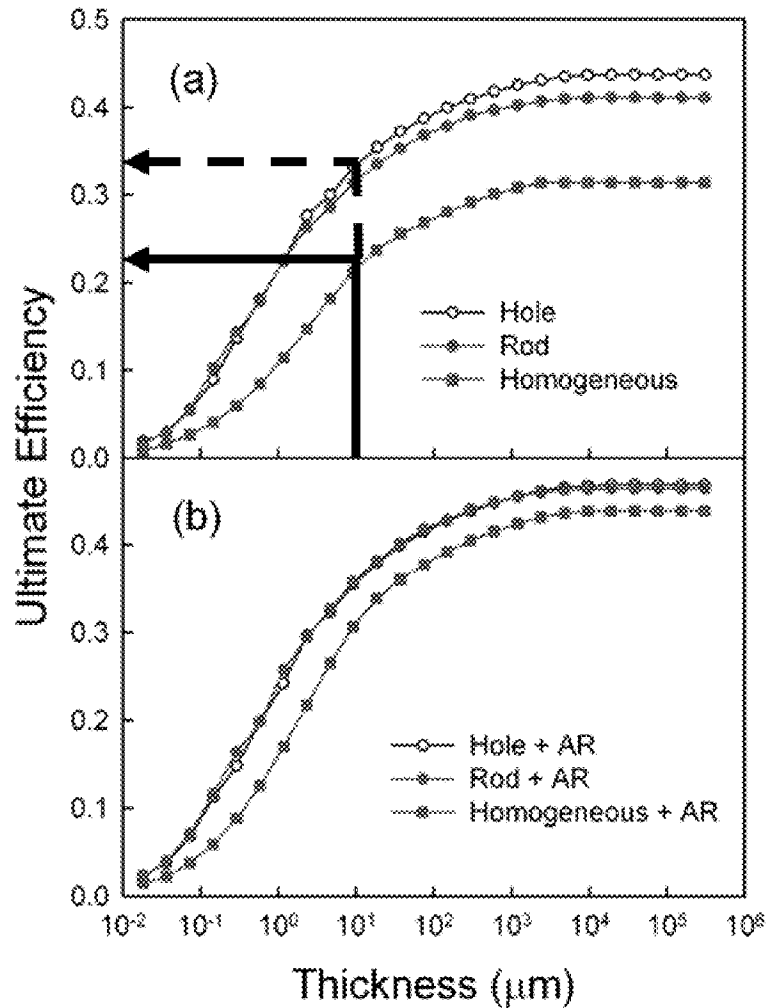


FIG. 4

Han, Fig. 4 (annotated).

265. In my opinion, therefore, based on a skilled artisan's knowledge of the state of the art before the earliest priority date of the '871 patent, the skilled artisan would have understood that *Yu*'s holes of 3,010-10,200 nm would increase by a factor of at least 1.1 the absorption of the light by at least some of *Yu*'s photodetectors relative to otherwise like photodetectors lacking said holes, and even if not readily understood, a POSITA would have found such a result not only obvious but also one having a reasonable expectation of success in achieving this increase because *Yu* discloses forming nanoholes of 3,010-10,200 nm depth.

2. Claims 2 and 18:

- a. [2] “The integrated structure of claim 1, wherein said array of photodetectors is monolithically integrated with Si electronic devices.”**
- b. [18] “The integrate[d] structure of claim 15, in which said array of photodetectors is monolithically integrated with Si electronic devices that include CMOS devices.”**

266. In my opinion, *Yu* discloses these additional limitations. Alternatively, the combination of *Yu*, *Kuboi*, and *Shinohara* renders these additional limitations obvious.

i. *Yu* discloses the additional limitations of claims 2 and 18.

267. *Yu* discloses an apparatus comprising the image sensor and a control circuit that includes a decoder, a transimpedance amplifier, a multiplexer circuit, and other readout circuitry components. *Yu*, ¶[115]. As I discussed above, one skilled in the art would have understood that each of *Yu*’s circuits would include electronic devices. *Supra* XI.A.2; Ex-1001, 3. According to *Yu*, the “image sensor and the control circuit can be formed as an integrated circuit or chip.” *Yu*, ¶[115]. *Yu* discloses that its image sensor includes a plurality of pixels arranged in a two-dimensional array of pillars configured as photodetectors. *Supra* XI.C.1.b. *Yu* also discloses that its “nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si.” *Yu*, ¶¶[55], [15], [27], [62] Because *Yu*’s substrate includes Si, one skilled in the art would have understood that the electronic devices in *Yu*’s control circuit would include Si (i.e., silicon based) electronic devices. *Supra* XI.A.2.

268. In my opinion, one skilled in the art would have understood that forming the image sensor and control circuit as an “integrated circuit” means that *Yu*’s pixels (which are photodetectors) are monolithically integrated with the control circuit (including Si electronic devices) on the same chip or substrate. This is supported by other prior art that would have been

known to one skilled in the art. For example, Ex-1001 defines an integrated circuit as “an *assembly of miniature electronic components* simultaneously produced in batch processing, *on or within a single substrate*, that performs an electronic circuit function,” or alternatively as “many transistors, resistors, capacitors, etc., fabricated and connected together to make a circuit on one monolithic slab of semiconductor material.” Ex-1001, 7 (emphases added).

269. *Yu* also discloses that “[m]ethods of fabrication of the image sensor can include shallow trench isolation (STI), also known as ‘Box Isolation Technique’” that “is generally used on CMOS process technology nodes of 250 nanometers and smaller.” *Yu*, ¶[56]. Because *Yu*’s image sensor is fabricated using CMOS processes, one skilled in the art would have understood that the electronic devices in *Yu*’s control circuit would include CMOS devices. *Supra* XI.A.2; Ex-1001, 4. As I discussed above, one skilled in the art would further have understood that *Yu*’s integrated circuit includes pixels (photodetectors) monolithically integrated with *Yu*’s control circuit. And because *Yu*’s control circuit includes CMOS devices, one skilled in the art would have understood that *Yu*’s integrated circuit monolithically integrates *Yu*’s array of photodetectors with Si electronic devices that include CMOS devices on the same chip or substrate.

ii. The *Yu-Kuboi-Shinohara* combination renders the additional limitations of claims 2 and 18 obvious.

270. To the extent Patent Owner argues that *Yu* does not disclose monolithic integration, the *Yu-Kuboi-Shinohara* combination renders these limitations obvious.

271. As discussed above, *Yu*, *Kuboi*, and *Shinohara* are analogous art to the ’871 patent. *Supra* XI.B.2.a, XI.C.1.g.i. In my opinion, one skilled in the art would have been motivated to implement *Shinohara*’s teaching of monolithic integration of the array of pillars (or

pixels) with Si electronic devices in manufacturing the *Yu-Kuboi* integrated structure (*supra* XI.C.1.g.i).

272. *Shinohara* discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring layer on the same substrate. *Shinohara*, ¶¶[68]-[82]; *supra* XI.B.2.a. As I discussed above, one skilled in the art would have understood that *Shinohara* discloses monolithically integrating its pixel region and the peripheral circuit portion including various electronic circuits and transistors on the same substrate. *Supra* XI.B.2. In my opinion, one skilled in the art would have understood that *Shinohara*'s monolithic integration lowers manufacturing costs, reduces package size, allows high bandwidth operation, improves power efficiency, and enables high-frequency mixed-signal processing. *supra* XI.B.2.a. One skilled in the art, therefore, would have been motivated to use *Shinohara*'s monolithic integration teaching to manufacture the *Yu-Kuboi* integrated structure and achieve the above-identified benefits.

273. In my opinion, a skilled artisan would have also understood that employing *Kuboi*'s reverse biasing capability during use of *Yu*'s integrated structure would not prohibit implementation of *Shinohara*'s monolithic integration teaching to manufacture the *Yu-Kuboi* integrated structure. One skilled in the art would have found that the combination of *Yu*, *Kuboi*, and *Shinohara* involves the use of a known technique—forming the pixel region and all associated electronic circuitry on the same substrate—to improve a similar device—the *Yu-Kuboi* integrated structure—in the same way, namely, by improving manufacturing reliability, reducing manufacturing cost and package size, signal attenuation, and noise, and improving high-bandwidth performance of *Yu-Kuboi* integrated structure.

274. In my opinion, one skilled in the art would have had a reasonable expectation of success in implementing *Shinohara*'s teachings for manufacturing the *Yu-Kuboi* integrated

structure. Given that *Yu*, *Kuboi*, and *Shinohara* disclose similar imaging devices with pixels, manufacturing the pixels in the *Yu-Kuboi* image sensor and associated electronic circuitry using *Shinohara*'s techniques would have been well within the skill level of a person of ordinary skill in the art. In my opinion, one skilled in the art would have had a reasonable expectation of success combining *Shinohara* with the *Yu-Kuboi* integrated structure because it requires combining well-known prior elements and manufacturing methods already taught by *Yu*, *Kuboi*, and *Shinohara*.

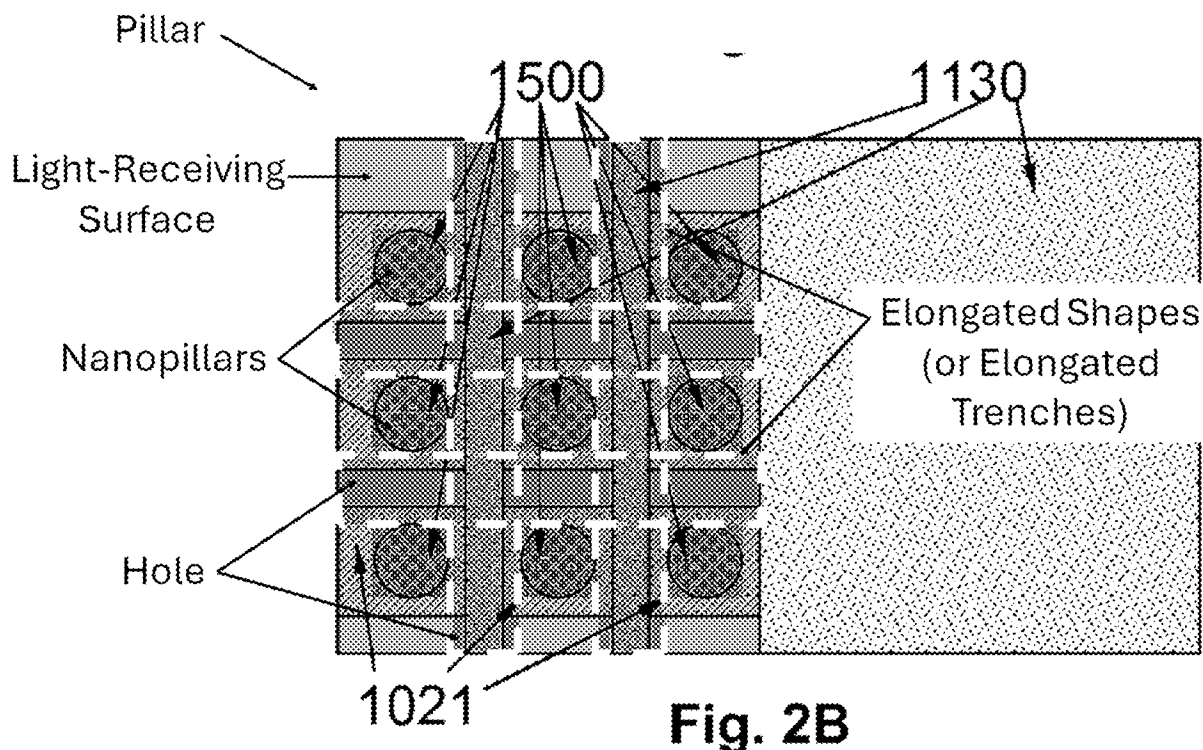
3. Claims 3, 4, 7, and 15

- a. [3]: “The integrated structure of claim 2, wherein each of at least some of said photodetectors includes at least one of said holes with elongated shapes at the light-receiving surface thereof.
- b. [4]: “The integrated structure of claim 2, wherein each of at least some of said photodetectors includes a plurality of said holes with elongated shapes at the light receiving surface thereof.”
- c. [7]: “The integrated structure of claim 1, wherein each of at least some of said photodetectors includes at least one of said holes with elongated shapes at the light receiving surface thereof.”
- d. [15]: “The integrated structure of claim 1, wherein at least some of said holes are configured as elongated trenches at said light-receiving surfaces.”

275. In my opinion, *Yu* discloses or renders obvious these additional limitations.

276. As I discussed for claim [1c], *Yu*'s holes are spaces between respective nanopillars, and those holes are formed in the light receiving surface of *Yu*'s pillar, which is a photodetector. *Supra* XI.C.1.d. *Yu* discloses that its nanopillars can have any suitable cross-sectional shape such as a circle, a square, a hexagon. *Yu*, ¶¶[22], [57]. Figure 2B, below, illustrates a plan view looking down onto *Yu*'s light-receiving surface, and it shows square

shaped nanopillars with holes between the nanopillars. *Supra* XI.C.1.d. As seen below, the holes have elongated shapes and are formed as elongated trenches. *Supra* XI.C.1.d.



Yu, Fig. 2B (annotated).

277. In my opinion, therefore, one skilled in the art would have understood that *Yu*'s integrated structure has a plurality of holes (i.e., "at least one," "at least some," or "a plurality of holes"), having an elongated shape (or in the form of elongated trenches) formed at the light-receiving surface, in at least one pillar (i.e., photodetector). *Supra* XI.C.1.d(claim [1c]).

4. Claim 12: "The integrated structure of claim 1, in which said electrical contacts are configured to provide electrical fields across at least some of said photodetectors."

278. In my opinion, *Yu* discloses these additional limitations.

279. As I discussed above, *Yu*'s metal layer 1140 that forms the gate electrodes and gate lines 1570 constitutes *Yu*'s bottom electrical contacts, and *Yu*'s TCL constitutes *Yu*'s image sensor's top electrical contact. *Supra* XI.C.1.g (claim [1f]). *Yu* discloses a method of using its

image sensor that includes “applying a bias voltage to the transparent conductive layer[and] applying a first gate voltage to all the gate lines, the first gate voltage being effective to pinch off electrical current through the nanopillars.” *Yu*, ¶¶[28], [114]. Because *Yu*’s TCL (i.e., “top electrical contact”) and gate lines (i.e., “bottom electrical contacts”) are used to apply voltage, in my opinion, one skilled in the art would have understood that *Yu*’s electrical contacts provide electrical fields across the nanopillars in *Yu*’s pixels (photodetectors, *supra* XI.C.1.b (claim [1a])).

5. Claim 14: “The integrated structure of claim 1, wherein said SI electronic devices include devices for signal processing and transmission.”

280. In my opinion, *Yu* discloses these additional limitations.

281. *Yu*’s apparatus comprises an image sensor and a control circuit that includes a decoder, a transimpedance amplifier (TIA), a multiplexer circuit, and other readout circuitry components. *Yu*, ¶[115]. As I discussed for claim 2, the control circuit constitutes SI electronic devices. *Supra* XI.C.2. *Yu*’s “TIA and multiplexer circuit 420 can amplify the electrical current from each readout line 1021 and convert it into a voltage signal.” *Yu*, ¶[115]. As I discussed above, in my opinion, one skilled in the art would have understood that because the TIA and multiplexer circuit amplify and convert the electrical current obtained from *Yu*’s pixels, *Yu*’s TIA and multiplexer circuit are SI electronic devices for signal processing. *Supra* XI.C.2; Ex-1001, 3.

282. The figure below illustrates an example of *Yu*’s imaging device. In my opinion, one skilled in the art would have understood the phrase “Signal Output” below as indicating that *Yu*’s TIA array and multiplexer circuit output or transmit a signal external to *Yu*’s imaging device.

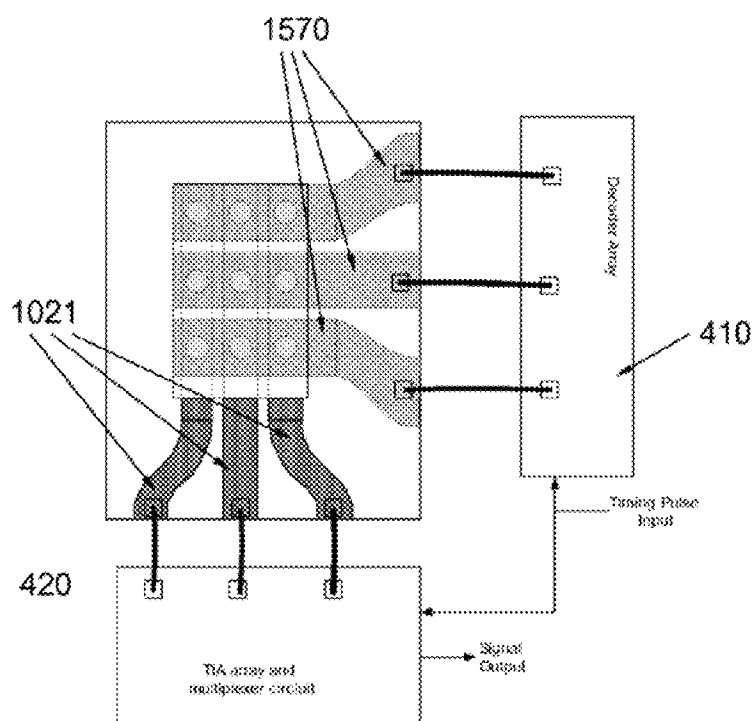
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FIG. 5

Yu, Fig. 5.

XII. CONCLUSION

283. For the reasons set forth above, it is my opinion that one skilled in the art would have found claims 1-4, 7, 12, 14, 15, and 18 of the '871 patent obvious over the prior art. My opinion would remain the same even if the level of skill in the art was slightly lower (e.g., requiring only a bachelor's degree instead of a master's degree).

284. In signing this declaration, I understand that the declaration will be filed as evidence in a request for *ex parte* reexamination before the United States Patent and Trademark Office.

285. I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001.

Date: March 5, 2026

By: _____

A handwritten signature in black ink, appearing to read 'Michael Lebby', is written over a horizontal line. The signature is stylized with loops and flourishes.

Michael Lebby