

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

W&WSENS DEVICES INC.,	)	
	)	
Plaintiff,	)	Case No. 2:24-cv-00854-JRG
	)	
v.	)	
	)	
SAMSUNG ELECTRONICS CO., LTD., and	)	
SAMSUNG ELECTRONICS AMERICA, INC.,	)	
	)	
Defendants.	)	
	)	

JOINT CLAIM CONSTRUCTION CHART

Pursuant to Patent L.R. 4-5(d) and the Court’s Second Amended Docket Control Order (Dkt. No. 54), W&Wsens Devices Inc. (“W&Wsens”) and Defendants Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (“Samsung”) submit the Joint Claim Construction Chart attached as Exhibit A containing the parties’ proposed constructions for the disputed terms of U.S. Patent Nos. 10,446,700 (the “’700 Patent”), 10,468,543 (the “’543 Patent”), 11,621,360 (the “’360 Patent”), 12,087,871 (the “’871 Patent”), and 12,243,948 (the “’948 Patent”) (collectively, the “Asserted Patents”). Exhibit A further directs “the Court’s attention to the patent and claim number(s) where the disputed term(s) appear(s).” See P.R. 4-5(d)(1).

Respectfully submitted,

Dated: January 20, 2026

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EXHIBIT A

	Term for Construction	Patent(s) and Claim(s)	W&Wsens' Proposed Construction	Defendant's Proposed Construction	Court's Construction
1	“hole[s]”	<u>'360</u> : Claims 1, 3, 5, 6 <u>'871</u> : Claims 1, 3, 4, 7 <u>'948</u> : Claims 1, 3, 13, 14 <u>'700</u> : Claims 1, 7, 16, 20 <u>'543</u> : Claims 1, 7, 16, 20	Plain and ordinary meaning	Plain and ordinary meaning (<i>e.g.</i> , not isolation trenches)	

	Term for Construction	Patent(s) and Claim(s)	W&Wsens' Proposed Construction	Defendant's Proposed Construction	Court's Construction
2	“deliberately formed in-pillar holes ... wherein said photodetector device is configured to respond to light photons incident on said array of pillars” “holes that are deliberately formed into the light-receiving surfaces ... extend into the photodetectors” “holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars ... extend[s] into the pillar[s]”	<u>'360</u>: Claim 1 <u>'871</u>: Claim 1 <u>'948</u>: Claims 1, 13	Plain and ordinary meaning	Holes deliberately formed in a pillar of a photodetector for absorbing light that is converted to electricity	

	Term for Construction	Patent(s) and Claim(s)	W&Wsens' Proposed Construction	Defendant's Proposed Construction	Court's Construction
3	“holes intentionally formed therein ... to concurrently receive ... optical input ... [that generates] electrical charges”	<u>'543</u> : Claim 1 <u>'700</u> : Claim 1	Plain and ordinary meaning	Holes designed to absorb an optical input that is converted into an electrical output	
4	“intermediate semiconductor material” “region[] therebetween” “intermediate region”	<u>'360</u> : Claims 1, 6 <u>'871</u> : Claim 1 <u>'543</u> : Claim 1	Plain and ordinary meaning	A region fabricated between the first region and the second region	
5	“intermediate layer”	<u>'700</u> : Claim 1	Plain and ordinary meaning	A layer fabricated between the first layer and the second layer	

Asserted Claims of U.S. Patent No. 10,446,700 With Disputed Terms Highlighted

1. A single-chip device comprising an integrated combination of a microstructure-enhanced photodetector (MSPD) configured for reverse-bias operation and an active electronic circuit, both formed on or in a single substrate and configured to receive an optical input that in cross-section is substantially continuous, convert the optical input to an electrical output, and process the electrical output into a processed output, wherein:

the MSPD on or in said single substrate comprises an **intermediate layer**, a first layer at one side of the **intermediate layer**, and a second layer at an opposite side of the **intermediate layer**, wherein:

each of the layers comprises Silicon, Germanium, or an alloy thereof;

at least one of said layers, or an overlying covering layer that may be present, has **holes intentionally formed therein**, extending in directions transverse to the layers;

each of the first and second layers comprises a doped material;

the **intermediate layer** comprises a material that is less doped than at least one of the first and second layers or is undoped, wherein the degree of doping is the same or different for different positions in the **intermediate layer**;

an input portion configured **to concurrently receive** at a plurality of said **holes** said **optical input** that has said substantially continuous cross-section; and

an output portion configured to provide said electrical output from the MSPD;

the MSPD includes reverse-bias electrodes coupled therewith to establish an electrical field therein when energized to thereby sweep in a selected direction **electrical charges generated** in the MSPD by said optical input;

said reverse-bias electrodes being free of a pattern of openings that matches said **holes**; and

the active electronic circuit on or in said single substrate is configured to process the electrical output from the MSPD by applying thereto:

amplification to form said processed output from the single-chip device;

processing other than or in addition to amplification to form said processed output from the single-chip device; and

routing to one or more selected destinations; and

a communication channel on or in said single-chip device, configured to deliver the electrical output from the MSPD to the active electronic circuit.

7. The single-chip device of claim 1, further including a layer of a dielectric material that covers the **holes** and is in the propagation path of said optical input.
16. The single-chip device of claim 1, in which at least some of said **holes** have sidewalls that slope in planes transverse to said layers.
20. The single-chip device of claim 1, in which the **holes** are at least partly filled with a dielectric material.
24. The single-chip device of claim 1, in which said MSPD further comprises ohmic contacts configured for reverse-biasing the MSPD.

28. The single-chip device of claim 1, further comprising one or more additional MSPD on or in the same substrate, and respective different optical bandpass filters coupled with at least two of the MSPDs on or in said single substrate, whereby at least two of said MSPDs are configured to respond to different wavelength ranges that are within said optical input.

30. The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate.

Asserted Claims of U.S. Patent No. 10,468,543 With Disputed Terms Highlighted

1. A single-chip device comprising an integrated combination of a microstructure-enhanced photodetector (MSPD) configured for reverse-bias operation and an active electronic circuit, both formed on or in a single substrate and configured to receive an optical input that in cross-section is substantially continuous spatially, convert the optical input to an electrical output, and process the electrical output into a processed output, wherein:

the MSPD on or in said single substrate comprises an **intermediate region**, a first region at one side of the **intermediate region**, and a second region at an opposite side of the **intermediate region**, wherein:

each of the regions comprises Silicon, Germanium, or an alloy thereof;

at least one of said regions, and an optional overlying covering region, have **holes intentionally formed therein**

each of the first and second regions comprises a doped material;

the **intermediate region** comprises a material that is less doped than at least one of the first and second regions or is undoped,

wherein the degree of doping is the same or different for different positions in the **intermediate region**;

an input portion configured **to concurrently receive** at a plurality of said **holes** said **optical input** that has said substantially continuous cross-section; and

an output portion configured to provide said electrical output from the MSPD;

the MSPD includes reverse-bias contacts coupled therewith to establish an electrical field therein when energized to thereby sweep in a selected direction **electrical charges generated** in the MSPD by said optical input; and

the active electronic circuit on or in said single substrate is configured to process the electrical output from the MSPD by applying thereto:

amplification to form said processed output from the single-chip device;

processing other than or in addition to amplification to form said processed output from the single-chip device; and

routing to one or more selected destinations; and

a communication channel on or in said single-chip device, configured to deliver the electrical output from the MSPD to the active electronic circuit.

7. The single-chip device of claim 1, further including a region of a dielectric material that covers the **holes** and is in the propagation path of said optical input.

16. The single-chip device of claim 1, in which at least some of said **holes** have sidewalls that slope in planes transverse to said regions.

20. The single-chip device of claim 1, in which the **holes** are at least partly filled with a dielectric material.

24. The single-chip device of claim 1, in which said MSPD further comprises ohmic contacts configured for reverse-biasing the MSPD.

28. The single-chip device of claim 1, further comprising one or more additional MSPD on or in the same substrate, and respective different optical bandpass filters coupled with at least two of the MSPDs on or in said single substrate, whereby at least two of said MSPDs are configured to respond to different wavelength ranges that are within said optical input.

30. The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate.

Asserted Claims of U.S. Patent No. 11,621,360 With Disputed Terms Highlighted

1. A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar **holes** comprising:

a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane;

wherein said array of pillars comprises:

a first doped semiconductor material;

an **intermediate semiconductor material**; and

solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars;

a second doped semiconductor material;

wherein:

the **intermediate semiconductor material** is between said first and second doped semiconductor materials;

the first and second doped semiconductor materials are doped to opposite semiconductor types;

the **intermediate semiconductor material** is less doped than at least one of the first and second doped semiconductor materials and the degree of doping is the same or different for different positions in the **intermediate semiconductor material**; and

each of the first and second doped semiconductor materials and said **intermediate semiconductor material** comprises Si;

one or more **deliberately formed in-pillar holes** with solid dielectric therein;

top and bottom electrical contacts electrically coupled with said array of pillars, **wherein said photodetector device is configured to respond to light photons incident on said array of pillars** by photo-generated charge carriers therein; and a base dielectric region that is below the array of pillars and comprises substantially solid dielectric material; wherein the pillars of said array of pillars:

are laterally spaced center to center by no more than 10,000 nanometers; and

have up-down lengths of said **intermediate semiconductor material** in the range of 100-5000 nanometers;

wherein at least said pillars, in-pillar **holes**, and solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar **holes**;

wherein said array of pillars is monolithically integrated in or on said semiconductor substrate with electronic circuits that include active elements for signal processing and transmission.

3. The photodetector device of claim 1, in which each of said pillars has a plurality of said one or more in-pillar **holes**.
5. The photodetector device of claim 1, in which said one or more in-pillar **holes** extend to a depth in a range of 100-10,000 nanometers.
6. The photodetector device of claim 1, in which said one or more in-pillar **holes** extend into said **intermediate semiconductor material**.

Asserted Claims of U.S. Patent No. 12,087,871 With Disputed Terms Highlighted

1. An integrated structure comprising:

an array of pillars comprising Si, Ge, and/or SiGe alloy semiconductor material wherein at least some of the pillars are configured as photodetectors that have respective light-receiving surfaces and have sides;

wherein at least some of the photodetectors comprise P-doped and N-doped regions and **regions therebetween** and are configured to respond to illumination with light in selected visible and infrared wavelength ranges by generating electrical charge carriers;

one or more **holes that are deliberately formed into the light-receiving surfaces**, have elongated and/or other shapes at said light-receiving surfaces, **extend into the photodetectors** to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;

side-isolation comprising solid material at said sides of at least some of the photodetectors;

a solid dielectric material forming a base dielectric region for said array; and

electrical contacts configured to provide electrical pathways to at least some of the photodetectors, including for selected reverse-biasing thereof;

wherein the presence of said one or more **holes** increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to otherwise like photodetectors lacking said **holes**.

2. The integrated structure of claim 1, wherein said array of photodetectors is monolithically integrated with SI electronic devices.

3. The integrated structure of claim 2, wherein each of at least some of said photodetectors includes a least one of said **holes** with elongated shapes at the light-receiving surface thereof.
4. The integrated structure of claim 2, wherein each of at least some of said photodetectors includes a plurality of said **holes** with elongated shapes at the light receiving surface thereof.
7. The integrated structure of claim 1, wherein each of at least some of said photodetectors includes at least one of said **holes** with elongated shapes at the light receiving surface thereof.
12. The integrated structure of claim 1, in which said electrical contacts are configured to provide electrical fields across at least some of said photodetectors.
14. The integrated structure of claim 1, wherein said SI electronic devices include devices for signal processing and transmission.
18. The integrates structure of claim 15, in which said array of photodetectors is monolithically integrated with Si electronic devices that include CMOS devices.

Asserted Claims of U.S. Patent No. 12,243,948 With Disputed Terms Highlighted

1. An integrated structure comprising:

an array of pillars comprising Si, Ge, and/or SiGe alloy semiconductor material, wherein at least some of the pillars are configured to include photodetectors and have respective light-receiving surfaces and respective sides;

wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;

one or more **holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars**,

have elongated or other shapes at or parallel to the light-receiving surfaces, **extend into the pillars** to a depth of 100 to 10000 nm, and are filled at least partly with solid dielectric material;

wherein at least some of the **holes** are elongated along the respective light-receiving surfaces;

side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;

a solid dielectric material forming a base dielectric region for the array;

electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;

wherein the presence of said one or more **holes** increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said **holes**.

2. The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices.

3. The integrated structure of claim 1, wherein each of at least some of the pillars has a plurality of the elongated **holes**.
7. The integrated structure of claim 1, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors.
13. An integrated structure comprising:
- an array of pillars comprising Si, Ge, and/or alloyed SiGe semiconductor material, wherein at least some of the pillars have respective sides and respective light-receiving surfaces with selected widths and comprise at least one photodetector;
 - wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;
 - one or more **holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars**, wherein each of the **holes** (i) has an elongated shape extending in length over less than the width of the light-receiving surface in which the hole is fabricated, (ii) has at least one closed contour at the light-receiving surface in which the hole is fabricated, (ii) **extends into the pillar** in which the hole is fabricated to a depth of 100 to 10000 nm, and (iv) is filled at least partly with solid dielectric material;
 - side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;
 - a solid dielectric material forming a base dielectric region for the array;
 - electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;

wherein the presence of the one or more **holes** increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the **holes**; and

wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission.

14. The integrated structure of claim 13, in which each of at least some of the pillars has only one of the elongated **holes** fabricated therein.