

Country	Patent/ Application/ Publication No.	Date of Filing	Date of Issue/ Publication	Inventor(s)	Bates Range
JP	2008-311562A	June 18, 2007	December 25, 2008	Obara et al.	SAM-W&W_00026777- SAM-W&W_00026803; SAM-W&W_00026983- SAM-W&W_00027019
JP	2008-544559A	June 28, 2006	December 4, 2008	Morse et al.	SAM-W&W_00035042- SAM-W&W_00035055
JP	2009-130276A	November 27, 2007	June 11, 2009	Tai et al.	SAM-W&W_00026804- SAM-W&W_00026883
JP	2009-206304A	February 28, 2008	September 10, 2009	Ishimura et al.	SAM-W&W_00035056- SAM-W&W_00035066
JP	2010-212347A	March 9, 2009	September 24, 2010	Imai	SAM-W&W_00035067- SAM-W&W_00035086
JP	2010-212469A	March 11, 2009	September 24, 2010	Yokoyama	SAM-W&W_00035087- SAM-W&W_00035120
JP	2010-232264A	March 26, 2009	October 14, 2010	Miura et al.	SAM-W&W_00026884- SAM-W&W_00026940
JP	2011-077370A	September 30, 2009	April 14, 2011	Otsuki	SAM-W&W_00035121- SAM-W&W_00035136
JP	2011-135058A	November 24, 2010	July 7, 2011	Hiruma et al.	SAM-W&W_00035137- SAM-W&W_00035183
JP	2011-139058A	December 15, 2010	July 14, 2011	Wehner et al.	SAM-W&W_00035184- SAM-W&W_00035196
JP	2012-178457A	February 25, 2011	September 13, 2012	Enomoto	SAM-W&W_00035197- SAM-W&W_00035233
JP	2013-033864A	August 2, 2011	February 14, 2013	Sasaki et al.	SAM-W&W_00035234- SAM-W&W_00035268
JP	2013-157567A	January 31, 2012	August 15, 2013	Noda et al.	SAM-W&W_00035310- SAM-W&W_00035332

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JP	05343729A	June 12, 1992	December 24, 1993	Ajisawa et al.	SAM-W&W_00027020- SAM-W&W_00027035
JP	3912024B2	April 9, 2001	May 9, 2007	Harada et al.	SAM-W&W_00026941- SAM-W&W_00026953
JPWO	2009/088071	January 9, 2009	May 26, 2011	Okamoto et al.	SAM-W&W_00027036- SAM-W&W_00027054
KR	100439760B1	June 18, 2002	July 12, 2004	Noh et al.	SAM-W&W_00027064- SAM-W&W_00027079
KR	2004-0036338	October 24, 2002	April 30, 2004	Choi et al.	SAM-W&W_00035336- SAM-W&W_00035341
KR	2004-0076331	February 25, 2003	September 1, 2004	Kim et al.	SAM-W&W_00035342- SAM-W&W_00035360
KR	100851759B1	May 3, 2007	August 11, 2008	Shim	SAM-W&W_00027080- SAM-W&W_00027105
KR	2010-0135548	June 17, 2009	December 27, 2010	Cho et al.	SAM-W&W_00035361- SAM-W&W_00035416
WO	2006/129427	April 18, 2006	December 7, 2006	Katoh et al.	SAM-W&W_00033932- SAM-W&W_00033960
WO	2009/034623	September 12, 2007	March 19, 2009	Masuoka et al.	SAM-W&W_00039487- SAM-W&W_00039539
WO	2008/052067	October 24, 2007	May 2, 2008	Munteanu et al.	SAM-W&W_00039484- SAM-W&W_00039486
WO	2010/037830	October 1, 2009	April 8, 2010	Neuilly	SAM-W&W_00033961- SAM-W&W_00033993
WO	2011/047359	October 15, 2010	April 21, 2011	Lal et al.	SAM-W&W_00039540- SAM-W&W_00039621
WO	2011/083674	December 17, 2010	July 14, 2011	Shigeta et al.	SAM-W&W_00039622- SAM-W&W_00039677

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WO	2011/083694	December 22, 2010	July 14, 2011	Shigeta et al.	SAM-W&W_00039678- SAM-W&W_00039727
WO	2011/085297	May 22, 2014	May 5, 2016	Han et al.	SAM-W&W_00033994- SAM-W&W_00034036
WO	2012/053491	October 17, 2011	April 26, 2012	Hiroaki et al.	SAM-W&W_00034037- SAM-W&W_00034167
WO	2012/056782	July 29, 2011	May 3, 2012	Masuoka, et al.	SAM-W&W_00034168- SAM-W&W_00034281
WO	2012/117469	October 31, 2011	September 7, 2012	Honma	SAM-W&W_00039728- SAM-W&W_00039765
WO	2012/121706	March 8, 2011	September 13, 2012	Oh et al.	SAM-W&W_00034282- SAM-W&W_00034318
WO	2012/160662	May 25, 2011	November 10, 2015	Watanabe et al.	SAM-W&W_00034319- SAM-W&W_00034371
WO	2012/167282	June 4, 2012	December 6, 2012	Pacifici et al.	SAM-W&W_00039760- SAM-W&W_00039807
WO	2013/111173	January 23, 2013	August 1, 2013	Oda et al.	SAM-W&W_00039808- SAM-W&W_00039847
WO	2013/136022	February 27, 2014	September 12, 2014	Simon et al.	SAM-W&W_00034473- SAM-W&W_00034488
WO	2013/189932	June 18, 2013	December 27, 2013	Wilhelm	SAM-W&W_00034372- SAM-W&W_00034423
WO	2013/190646	June 20, 2012	December 27, 2013	Watanabe et al.	SAM-W&W_00039848- SAM-W&W_00039897
WO	2014/136022	February 27, 2014	September 12, 2014	Perraud et al.	SAM-W&W_00034424- SAM-W&W_00034472
WO	2014/190189	May 22, 2014	November 27, 2014	Wang et al.	SAM-W&W_00034489- SAM-W&W_00034627

Table 2: Non-Patent Publications

Title	Publication Date	Author(s)	Publisher	Bates Range
Adhesive Chemistry: Developments and Trends	1984	Lieng-Huang Lee (ed.)	Plenum Press	SAM-W&W_00036266- SAM-W&W_00037111
Integrated Electronic and Photonic Devices	1985	Margalit et al.	Bell Telephone Laboratories, Inc.	SAM-W&W_00026509- SAM-W&W_00026569
Monolithic Optoelectronic Integration: A New Component Technology for Lightwave Communications	December 1985	Forrest	IEEE	SAM-W&W_00027151- SAM-W&W_00027166
CMOS Active Pixel Image Sensor	March 3, 1994	Mendis et al.	IEEE	SAM-W&W_00024533- SAM-W&W_00024534
Mechanisms of recombination in GaN photodetectors	1996	Binet et al.	Applied Physics Letters	SAM-W&W_00027133- SAM-W&W_00027136
Intel Releases 971 PC Camera Kit For Production Of Affordable, Easy-To-Use, Portable PC Cameras	1997	Intel	Intel	SAM-W&W_00034749- SAM-W&W_00034751
CMOS Image Sensors: Electronic Camera-on-a-Chip	October 10, 1997	Fossum	IEEE	SAM-W&W_00024550- SAM-W&W_00024559
CMOS Image Sensors Challenge CCDs	1998	Diefendorff	Microdesign Resources, Microprocessor Report	SAM-W&W_00034681- SAM-W&W_00034685
A 19.8% Efficient Honeycomb Multicrystalline Silicon Solar Cell with Improved Light Trapping	October 10, 1999	Zhao et al.	IEEE	SAM-W&W_00024431- SAM-W&W_00024436

Title	Publication Date	Author(s)	Publisher	Bates Range
Advanced Optoelectronic Devices: Chapter 4 Photodetectors	1999	Dragoman et al.	Springer	SAM-W&W_00024465- SAM-W&W_00024521
Electrical Engineering Dictionary	2000	Laplanche et al.	CRC Press LLC	SAM-W&W_00025575- SAM-W&W_00026348
Performance Analysis of a Color CMOS Photogate Image Sensor	2000	Blanksby et al.	IEEE	SAM-W&W_00037112- SAM-W&W_00037121
IEEE 100 The Authoritative Dictionary of IEEE Standard Terms (7th Edition)	2000	IEEE	IEEE	SAM-W&W_00026454- SAM-W&W_00026457
Signal Processing in CMOS Image Sensors	2000	Nair et al.	IEEE	SAM-W&W_00035508- SAM-W&W_00035517
CMOS Logic Circuit Design	2001	Uyemura	Kluwer Academic Publishers	SAM-W&W_00024660- SAM-W&W_00025208
OMNIVISION Announces 1.3-Megapixel CMOS Image Sensors	2001	OmniVision	OmniVision	SAM-W&W_00037143- SAM-W&W_00037145
OMNIVISION Announces Expanded Image Sensor	2001	OmniVision	OmniVision	SAM-W&W_00037146- SAM-W&W_00037150
OMNIVISION Datasheet OV9610/OV9110 CMOS Image Sensors	2001	OmniVision	OmniVision	SAM-W&W_00037229- SAM-W&W_00037241
The effect of indium tin oxide as an ohmic contact for the 850 nm GaAs oxide-confined VCSELs	February 2002	Jiang et al.	Elsevier Science Ltd.	SAM-W&W_00031762- SAM-W&W_00031765

Title	Publication Date	Author(s)	Publisher	Bates Range
Deeply Etched Grating Structures for Enhanced Absorption in Thin C-Si Solar Cells	2002	Zaidi et al.	IEEE	SAM-W&W_00037139- SAM-W&W_00037142
CMOS Sensor Inc. website describing Contact Image Sensor (CIS)	2002	CMOS Sensor Inc.	CMOS Sensor Inc.	SAM-W&W_00037151- SAM-W&W_00037151
Silicon-on-insulator waveguide photodetector with Ge/Si self-assembled islands	2002	El Kurdi et al.	Journal of Applied Physics	SAM-W&W_00030532- SAM-W&W_00030536
Silicon Substrates with Buried Distributed Bragg Reflectors for Resonant Cavity-Enhanced Optoelectronics	2002	Emsley et al.	IEEE	SAM-W&W_00035518- SAM-W&W_00035525
Semiconductor Physics and Devices Basic Principles (3d Edition)	2003	Neamen	McGraw Hill	SAM-W&W_00029760- SAM-W&W_00029767
Integration of 10Gb/sec Silicon Lateral Trench Photodetector with High-Performance CMOS	2003	Yang et al.	IEEE	SAM-W&W_00026577- SAM-W&W_00026578
Silicon Optoelectronic Integrated Circuits	2004	Zimmermann	Springer	SAM-W&W_00030159- SAM-W&W_00030524
Optical Microscopy Primer: Introduction to CMOS Image Sensors	July 16, 2004	Turchetta et al.	The Florida State University & Michael W. Davidson	SAM-W&W_00027641- SAM-W&W_00027649

Title	Publication Date	Author(s)	Publisher	Bates Range
Characterization of CsI photocathodes at grazing incidence for use in a unit quantum efficiency x-ray streak camera	October 2004	Lowney et al.	American Institute of Physics	SAM-W&W_00024646-SAM-W&W_00024652
A 3.9-mm Pixel Pitch VGA Format 10-b Digital Output CMOS Image Sensor With 1.5 Transistor/Pixel	December 2004	Takahashi et al.	IEEE J. Solid-State Circuits	SAM-W&W_00034660-SAM-W&W_00034668
CMOS Image Sensors	May 2005	El Gamal et al.	IEEE	SAM-W&W_00024535-SAM-W&W_00024549
Aligned Single-Crystalline Si Nanowire Arrays for Photovoltaic Applications	August 18, 2005	Peng et al.	Wiley Online Library	SAM-W&W_00035487-SAM-W&W_00035492
Shared pixels for CMOS image sensor arrays	2005	McGrath et al.	IEEE	SAM-W&W_00035453-SAM-W&W_00035457
Highly Integrated VCSEL-Based 10Gb/s Miniature Optical Sub-Assembly	2005	Bernabe et al.	IEEE	SAM-W&W_00026448-SAM-W&W_00026453
Roadmap for High Efficiency Solid-State Neutron Detectors	October 2005	Nikolic et al.	Digital Commons	SAM-W&W_00029151-SAM-W&W_00029161
Integration of Photonic Detectors in Standard SiGe HBT BiCMOS	2006	Meinhardt et al.	The Electrochemical Society	SAM-W&W_00026579-SAM-W&W_00026593
1/2-inch 7.2MPixel CMOS Image Sensor with 2.25µm Pixels Using 4-Shared Pixel Structure for Pixel-Level Summation	2006	Kim et al.	IEEE – International Solid State Circuits Conference	SAM-W&W_00035424-SAM-W&W_00035433

Title	Publication Date	Author(s)	Publisher	Bates Range
MT9T031 Image Sensor – Product Brief	2006	Micron Technology	Micron Technology	SAM-W&W_00037217- SAM-W&W_00037228
Advances in fully CMOS integrated photonic devices	February 9, 2007	Michel et al.	SPIE	SAM-W&W_00024522- SAM-W&W_00024532
Deep Trench Isolation for Crosstalk Suppression in Active Pixel Sensors with 1.7 m Pixel Pitch	April 24, 2007	Park et al.	Japanese Journal of Applied Physics	SAM-W&W_00035479- SAM-W&W_00035482
High Sensitivity of Dielectric films Structure for Advanced CMOS Image Sensor Technology	June 7-10, 2007	Chang et al.	IEEE	SAM-W&W_00026427- SAM-W&W_00026431
Strong broadband optical absorption in silicon NW films	July 17, 2007	Tsakalakos et al.	Society of Photo-Optical Instrumentation Engineers	SAM-W&W_00035534- SAM-W&W_00035544
Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications	October 10, 2007	Hu et al.	American Chemical Society	SAM-W&W_00034742- SAM-W&W_00034747
Nanophotonic Materials Photonic Crystals, Plasmonics, and Metamaterials	November 2007	Wehrspohn et al.	Wiley-VCH	SAM-W&W_00027190- SAM-W&W_00027638
Gr Gb difference in 3M CMOS Image Sensor with 1.75µm pixel	2007	Kim et al.	International Image Sensors Society (IIS)	SAM-W&W_00035434- SAM-W&W_00035437
Nanoelectrode Lithography: Chemical Nanoimprint that Transfers a Pattern by Electrochemical Reaction	August 2008	Yokoo et al.	NTT Technical Review	SAM-W&W_00027182- SAM-W&W_00027189

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Optical confinement methods for continued scaling of CMOS image sensor pixels	November 25, 2008	Fesenmaier et al.	Optical Society of America	SAM-W&W_00027670- SAM-W&W_00027683
Advanced image sensor technology for pixel scaling down toward 1.0µm	2008	Ahn et al.	IEEE	SAM-W&W_00034672- SAM-W&W_00034675
Process Flow Innovations for Photonic Device Integration in CMOS	2008	Beals et al.	Society of Photo-Optical Instrumentation Engineers (SPIE)	SAM-W&W_00029133- SAM-W&W_00029146
Monolithic Integration of Photonic and Electronic Circuits in a CMOS Process	2008	Mekis et al.	SPIE	SAM-W&W_00027137- SAM-W&W_00027150
Photonic Crystals: Physics and Technology	2008	Sibilia et al.	Springer	SAM-W&W_00028844- SAM-W&W_00029132
Photonic Crystals Molding the Flow of Light 2d Edition	2008	Joannopoulos et al.	Princeton University Press	SAM-W&W_00027684- SAM-W&W_00027988
Through Silicon Vias Technology for CMOS Image Sensors Packaging	2008	Henry et al.	IEEE	SAM-W&W_00037832- SAM-W&W_00037841
Photonic Crystals Towards Nanoscale Photonic Devices 2d Edition	2008	Benisty et al.	Springer	SAM-W&W_00027989- SAM-W&W_00028502
Porous Silicon Carbide and Gallium Nitride	2008	Feenstra et al.	John Wiley & Sons, Ltd.	SAM-W&W_00028503- SAM-W&W_00028843

Title	Publication Date	Author(s)	Publisher	Bates Range
Absorption Enhancement in Thin-Film Silicon Solar Cells in SOI Configuration Using Physical and Geometrical Optics	2008	Prinja et al.	IEEE	SAM-W&W_00024452- SAM-W&W_00024455
CMOS Image Sensor with two-shared pixel and staggered readout architecture	June 26-28, 2009	Bogaerts et al.	International Image Sensor Workshop	SAM-W&W_00034686- SAM-W&W_00034689
Silicon Nanowire-Based Solar Cells on Glass: Synthesis, Optical Properties and Cell Parameters	March 12, 2009	Sivakov et al.	American Chemical Society	SAM-W&W_00034654- SAM-W&W_00034653
Focused ion beam technology and ultimate applications	March 20, 2009	Gierak	Semiconductor Science and Technology	SAM-W&W_00026385- SAM-W&W_00026407
Optical absorption enhancement in silicon nanowire arrays with a large lattice constant for photovoltaic applications	October 26, 2009	Lin et al.	Optical Society of America	SAM-W&W_00035442- SAM-W&W_00035452
Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic application	2010	Lin et al.	IEEE	SAM-W&W_00035477- SAM-W&W_00035478
Optical absorption enhancement in nanopore textured-silicon thin film for photovoltaic application	January 1, 2010	Wang et al.	Optical Society of America	SAM-W&W_00027650- SAM-W&W_00027652
Optical Absorption Enhancement in Silicon Nanohole Arrays for Solar Photovoltaics	February 8, 2010	Han et al.	American Chemical Society	SAM-W&W_00027655- SAM-W&W_00027658

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Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications	February 14, 2010	Kelzenberg et al.	Macmillan Publishers Limited	SAM-W&W_00035417- SAM-W&W_00035423
A grazing incidence x-ray streak camera for ultrafast, single-shot measurements	March 29, 2010	Feng et al.	American Institute of Physics Publishing	SAM-W&W_00024437- SAM-W&W_00024441
High-Performance Silicon Nanohole Solar Cells	May 2010	Peng et al.	American Chemical Society	SAM-W&W_00026445- SAM-W&W_00026447
NREL's Black Silicon Increases Solar Cell Efficiency by Reducing Reflected Sunlight	November 2010	National Renewable Energy Laboratory	National Renewable Energy Laboratory	SAM-W&W_00027180- SAM-W&W_00027181
Light Trapping in Silicon Nanowire Solar Cells	2010	Garnett et al.	American Chemical Society	SAM-W&W_00027117- SAM-W&W_00027122
Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications	2010	Lin et al.	SPIE	SAM-W&W_00027659- SAM-W&W_00027669
Integrated microsystem for blue/ultraviolet detection	2010	Pauchard et al.	MCB University Press	SAM-W&W_00026570- SAM-W&W_00026576
Semiconductor Devices Physics and Technology (3d Edition)	2012	Sze et al.	IEEE	SAM-W&W_00037242- SAM-W&W_00037831
Controlling Light in Optically Induced Photonic Lattices	2011	Terhalle	Springer Theses	SAM-W&W_00025209- SAM-W&W_00025324
Silicon Nanowires for Photovoltaic Solar Energy Conversion	2011	Peng et al.	Advanced Materials	SAM-W&W_00030141- SAM-W&W_00030158

Title	Publication Date	Author(s)	Publisher	Bates Range
Review of the 1.4 μ m Pixel Generation	2011	Fontaine	International Image Sensors Society (IISS)	SAM-W&W_00034719-SAM-W&W_00034722
Pixel-to-Pixel isolation by Deep Trench technology: Application to CMOS Image Sensor	2011	Tournier et al.	International Image Sensors Society (IISS)	SAM-W&W_00035530-SAM-W&W_00035533
A 300mm Wafer-Size CMOS Image Sensor with In-Pixel Voltage-Gain Amplifier and Column-Level Differential Readout Circuitry	2011	Yamashita	IEEE International Solid-State Circuits Conference	SAM-W&W_00034669-SAM-W&W_00034671
A photonic-plasmonic structure for enhancing light absorption in thin film solar cells	September 30, 2011	Bhattacharya et al.	Applied Physics Letters	SAM-W&W_00024442-SAM-W&W_00024445
Optical Absorption Enhancement in Silicon Nanohole Arrays for Photovoltaics	2011	Chen et al.	IEEE	SAM-W&W_00035474-SAM-W&W_00035476
Ge-on-Si optoelectronics	October 29, 2011	Liu et al.	Elsevier	SAM-W&W_00034723-SAM-W&W_00034729
Design and fabrication of photonic crystals in epitaxial free silicon for ultrathin solar cells	November 13-16, 2011	Meng et al.	IEEE	SAM-W&W_00035458-SAM-W&W_00035464
A simple and low-cost technique for silicon nanowire arrays based solar cells	December 7, 2011	Huang et al.	Elsevier B.V.	SAM-W&W_00024446-SAM-W&W_00024451
Light harvesting by planar photonic crystals in solar cells: the case of amorphous silicon	January 12, 2012	Gomard et al.	IOP Publishing Ltd.	SAM-W&W_00034730-SAM-W&W_00034741

Title	Publication Date	Author(s)	Publisher	Bates Range
Black Silicon Antireflection Technology	February 14, 2012	Dennis J. Flood	InterPV	SAM-W&W_00035472- SAM-W&W_00035473; SAM-W&W_00040106- SAM-W&W_00040110
A 1920x1080 3.65 µm-Pixel 2D/3D Image Sensor with Split and Binning Pixel Structure in 0.11 µm Standard CMOS	February 22, 2012	Kim et al.	ISSCC	SAM-W&W_00035493- SAM-W&W_00035495
Electrical Properties of ITO/Crystalline-Silicon Contact at Different Deposition Temperatures	March 2012	De Cesare et al.	IEEE	SAM-W&W_00034716- SAM-W&W_00034718
Experimental Study of Design Parameters in Silicon Micropillar Array Solar Cells Produced by Soft Lithography and Metal-Assisted Chemical Etching	April 2012	Shin et al.	IEEE	SAM-W&W_00026380- SAM-W&W_00026384
Design, fabrication and optical characterization of photonic crystal assisted thin film monocrystalline-silicon solar cells	May 11, 2012	Meng et al.	Optical Society of America (OSA)	SAM-W&W_00034705- SAM-W&W_00034715
Efficient Light Trapping in Inverted Nanopyramid Thin Crystalline Silicon Membranes for Solar Cell Applications	May 21, 2012	Mavrokefalos et al.	Nano Letter	SAM-W&W_00040008- SAM-W&W_00040012

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Efficient Light-Trapping in Inverted Nano-Pyramid Thin Crystalline Silicon Membranes for Solar Cell Applications	June 13, 2012	Mavrokefalos et al.	American Chemical Society	SAM-W&W_00036261-SAM-W&W_00036265
Current-Voltage Characteristics of ITO/p-Si and ITO/n-Si Contact Interfaces	June 2012	Pethuraja et al.	Advances in Materials Physics and Chemistry	SAM-W&W_00037135-SAM-W&W_00037138
Sony develops 'Exmor RS,' the world's first stacked CMOS image sensor	August 20, 2012	Sony	Phys Org	SAM-W&W_00024420-SAM-W&W_00024423
High-contrast gratings for integrated optoelectronics	September 4, 2012	Chang-Hasnain, et al.	Advances in Optics and Photonics	SAM-W&W_00037155-SAM-W&W_00037216
Characteristics of large-scale nanohole arrays for thin-silicon photovoltaics	October 1, 2012	Chen et al.	Wiley Online Library	SAM-W&W_00024636-SAM-W&W_00024645
Natcore Builds World's First Black Silicon Solar Cell Using Scalable Production Process	November 7, 2012	Inhabitat	Inhabitat	SAM-W&W_00027639-SAM-W&W_00027640
A CMOS Image Sensor Based on Unified Pixel Architecture With Time-Division Multiplexing Scheme for Color and Depth Image Acquisition	November 2012	Kim et al.	IEEE	SAM-W&W_00035496-SAM-W&W_00035507
High responsivity MSM black silicon photodetector	December 21, 2012	Su et al.	Elsevier	SAM-W&W_00026438-SAM-W&W_00026444

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Advanced Imaging Research and Development at DARPA	2012	Dhar et al.	SPIE	SAM-W&W_00024456- SAM-W&W_00024464
Suppression of Crosstalk by Using Backside Deep Trench Isolation for 1.12µm Backside Illuminated CMOS Image Sensor	2012	Kitamura et al.	IEEE	SAM-W&W_00035438- SAM-W&W_00035441
Characterization of light absorption in thin-film silicon with periodic nanohole arrays	March 4, 2013	Yahaya et al.	Optical Society of America	SAM-W&W_00024653- SAM-W&W_00024659
Canon develops 35 mm full-frame CMOS sensor for video capture	March 4, 2013	Canon	Canon	SAM-W&W_00024632- SAM-W&W_00024633
Silicon/organic hybrid heterojunction infrared photodetector operating in the telecom regime	March 14, 2013	Bednorz et al.	Elsevier B.V.	SAM-W&W_00030525- SAM-W&W_00030531
Resolution Limits of Electron-Beam Lithography toward the Atomic Scale	March 14, 2013	Manfrinato et al.	American Chemical Society	SAM-W&W_00029147- SAM-W&W_00029150
Optical absorption enhancement in partially aperiodic silicon nanohole structures for photovoltaics	2013	Lin et al.	Optical Society of America	SAM-W&W_00027653- SAM-W&W_00027654
Advances in Infrared Detector Array Technology	2013	Dhar et al.	InTech	SAM-W&W_00026467- SAM-W&W_00026508
SiOnyx Announces First Products	April 4, 2013	Image Sensors World	Image Sensors World	SAM-W&W_00034628- SAM-W&W_00034635

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SNR Metric and Crosstalk in Color Image Sensor of Small Size Pixel	April 22-24, 2013	Ahn et al.	IEEE	SAM-W&W_00034676- SAM-W&W_00034677
DSS 2013: SiOnyx sees digitally with 'black' silicon	May 6, 2013	Optics.org	Optics.org	SAM-W&W_00034652- SAM-W&W_00034653
Canon EOS 70D Specs (New Sensor), to be announced on July 2	June 27, 2013	Cameraegg	Cameraegg	SAM-W&W_00024611- SAM-W&W_00024613
Canon develops new Dual Pixel CMOS AF technology for significantly improved autofocus performance during Live View shooting and when shooting movies	July 2, 2013	Canon	Canon	SAM-W&W_00024634- SAM-W&W_00024635
Monolithic VCSEL-PIN Photodiode Integration for Bidirectional Optical Data Transmission	August 2013	Kern et al.	IEEE	SAM-W&W_00027167- SAM-W&W_00027179
A novel silicon nanostructure with effective light trapping for polycrystalline silicon thin film solar cells by means of metal-assisted wet chemical etching	September 20, 2013	Xue	Wiley Online Library	SAM-W&W_00039898- SAM-W&W_00039901
Natcore Aims To Make Black Silicon Solar Cells Even Cheaper	December 9, 2013	Tina Casey	CleanTechnica	SAM-W&W_00035465- SAM-W&W_00035471
The Evolution of CMOS Image Sensors	2013	Hirayama	IEEE	SAM-W&W_00035526- SAM-W&W_00035529

Title	Publication Date	Author(s)	Publisher	Bates Range
HOT infrared photodetectors	2013	Martyniuk et al.	Opto-Electronics Review	SAM-W&W_00026408- SAM-W&W_00026426
A 1/4-inch 8Mpixel CMOS Image Sensor with 3D Backside-Illuminated 1.12µm Pixel with Front-Side Deep-Trench Isolation and Vertical Transfer Gate	February 9-13, 2014	Ahn et al.	IEEE	SAM-W&W_00034678- SAM-W&W_00034680
Light management for photovoltaics using high-index nanostructures	April 22, 2014	Brongersma et al.	Nature Materials	SAM-W&W_00027123- SAM-W&W_00027132
High quantum efficiency photocathode simulation for the investigation of novel structured designs	Presented June 2, 2014	Opachich et al.	Review of Scientific Instruments	SAM-W&W_00026432- SAM-W&W_00026437
Si Nanostructures based solar cells	2014	Lei	Nanyang Technological University – School of Electrical and Electronic Engineering	SAM-W&W_00029768- SAM-W&W_00029953
Si nanostructures based solar cells	2014	Hong	Nanyang Technological University, School of Electrical and Electronic Engineering	SAM-W&W_00029954- SAM-W&W_00030140
The Art of Electronics (3d Edition)	2016	Horowitz et al.	Cambridge University Press	SAM-W&W_00030537- SAM-W&W_00031761

Title	Publication Date	Author(s)	Publisher	Bates Range
This new phone highlights Samsung's growing photography prowess	December 14, 2016	Deidre R.	SamMobile	SAM-W&W_00040111- SAM-W&W_00040114
High-performance mobile 'Tetracell image sensor' wins Minister's Award at Multimedia Technology Awards!	June 2, 2017	Samsung Semiconductor	Samsung Semiconductor	SAM-W&W_00026349- SAM-W&W_00026355; SAM-W&W_00027107- SAM-W&W_00027113
IR sensitivity enhancement of CMOS Image Sensor with diffractive light trapping pixels	June 19, 2017	Yokogawa et al.	Scientific Reports	SAM-W&W_00026458- SAM-W&W_00026466
Sony Enhances IR Sensitivity by 80% with Pyramidal Structure	June 20, 2017	Image Sensors World	Image Sensors World	SAM-W&W_00024424- SAM-W&W_00024430
Cameras with Black Silicon Sensors Reach the Market	September 22, 2017	Image Sensors World	Image Sensors World	SAM-W&W_00034636- SAM-W&W_00034643
Samsung Electronics Launches Two New Ultra-Compact High-Definition Image Sensors ISOCELL	October 11, 2017	Samsung Semiconductor	Samsung Semiconductor	SAM-W&W_00026356- SAM-W&W_00026359; SAM-W&W_00027114- SAM-W&W_00027116
Samsung's new dual pixel mobile sensor wants to eliminate dual cameras in smartphones	October 12, 2017	John Aldred	DIY Photography	SAM-W&W_00029168- SAM-W&W_00029169
Samsung Honored for Outstanding Design and Engineering with 36 CES 2018 Innovation Awards	November 10, 2017	Yoon Sang-ho	Digital Daily	SAM-W&W_00029162- SAM-W&W_00029167

Title	Publication Date	Author(s)	Publisher	Bates Range
2017 Pixel Technology in Review	December 19, 2017	Image Sensors World	Image Sensors World	SAM-W&W_00034644-SAM-W&W_00034651
An All Pixel PDAF CMOS Image Sensor with $0.64\mu\text{m} \times 1.28\mu\text{m}$ Photodiode Separated by Self-aligned In-pixel Deep Trench Isolation for High AF Performance	2017	Choi et al.	IEEE	SAM-W&W_00034703-SAM-W&W_00034704
Canon Autofocus Series: Dual Pixel CMOS AF Explained	April 27, 2018	Canon	Canon	SAM-W&W_00024601-SAM-W&W_00024610
Pixel Technology for Improving IR Quantum Efficiency of Backsideilluminated CMOS Image Sensor	2019	Park et al.	International Image Sensors Society (IIS)	SAM-W&W_00035483-SAM-W&W_00035486
Canon Technology Explainer: What is Dual Pixel CMOS AF?	December 16, 2022	Canon	Snapshot	SAM-W&W_00024614-SAM-W&W_00024631
CMOS Sensor Inc. About LinkedIn	July 18, 2024	CMOS Sensor Inc.	LinkedIn	SAM-W&W_00037152-SAM-W&W_00037154
Intel 971 PC Camera Kit (1997)	2024	Digitalcamera Museum	Digitalcamera Museum	SAM-W&W_00034748-SAM-W&W_00034748
Intro to Dual Pixel Autofocus (DPAF)	2025	Winston	Canon	SAM-W&W_00026594-SAM-W&W_00026603
DUAL PIXEL CMOS AF	2025	EOS Magazine	EOS Magazine	SAM-W&W_00025478-SAM-W&W_00025484
Everything you wanted to know about autofocus (AF)	2025	Canon	Canon	SAM-W&W_00026360-SAM-W&W_00026379

Defendants further incorporate by reference all “U.S. Patent Documents” and “Other Publications” cited on the face of the Patents-in-Suit. Any citation to one or more of the above prior art references, or other prior art references regarding any method or system, should be construed to constitute not only a citation to the prior art reference itself, but also a reference to the system itself. Discovery has only just begun in this case, and Defendants will supplement if and when more information becomes available from Plaintiff or third parties.

B. Prior Art Disclosures—Known/Use/Sales/Offers for Sale

Defendants believe that there were prior art disclosures in the form of sales, offers for sale, and/or uses by others of products that qualify as prior art under pre-AIA 35 U.S.C. § 102(a) and/or (b) or under AIA 35 U.S.C. § 102(a)(1) against one or more of the Asserted Claims of the Patents-in-Suit. The below-identified prior art products include products Defendants are currently aware of through an on-going diligent and reasonable investigation at this early stage of discovery and/or based on publicly available information. Details regarding such offers for sale and public uses may be within the possession of third parties. As discovery progresses, Defendants intend and reserve the right to promptly supplement and/or amend the lists below to include additional prior art products that anticipate and/or render obvious the asserted claims. To the extent Plaintiff contends that any systems presented below do not qualify as prior art to one or more Patents-in-Suit, Defendants reserve the right to rely on any of such systems as evidence of simultaneous development as an indicia of obviousness.

Table 3: Prior Art Products

System	Sale or Use Date
Intel Corp.'s 971 PC Camera Kit including CMOS Image Sensor for "portable PC cameras for home and business users"	At least as early as November 3, 1997
OMNIVISION Technologies, Inc.'s CMOS Image Sensors, including 1.3-Megapixel CMOS Image Sensors, OV8610 and OV8110 SVGA Sensors, OV5116 TV Sensor, OV6630 and OV6130 CIF Sensors.	At least as early as April 23, 2001
CMOS Image Sensor, Inc.'s CMOS image sensors.	At least as early as May 3, 2002
SiOnyx XQE CMOS sensors, including XQE-1310, XQE-0920, XQE-0570	At least as early as 2013

System	Sale or Use Date
Natcore black silicon solar cells	At least as early as 2012
Solar Cells with Inverted Nanopyramid Thin Crystalline Silicon Membranes for Efficient Light Trapping	At least as early as 2012
Samsung's ISOCELL products with dual-PD or similar PDAF features	At least as early as 2016
Samsung CMOS Image Sensor products with RGB Bayer or similar pixel-binning features	At least as early as 2016
Canon Dual Pixel Autofocus CMOS sensor products	At least as early as 2013
DARPA infrared detector	At least as early as 2012
Sony CMOS Image Sensors	At least as early as 2008

For the public uses identified herein, Defendants are investigating the identities of the individuals who knew about and/or were involved in the making, first public use, offer for sale and/or sale of these products and systems. Defendants are also investigating the exact date that these products and systems were first made, first publicly used, offered for sale and/or sold. In addition, Defendants are currently investigating the dates of conception and reduction to practice of these products and systems and when these products and systems were first known or used by others.

In the course of their investigation, Defendants may identify additional prior art documents describing these products, systems, and/or disclosures that may also anticipate and/or render obvious as invalidating printed publications. Any citation to one or more of prior art references regarding these products, systems, and/or disclosures should be construed to constitute not only a citation to the prior art reference itself, but also a reference to the associated products, systems, and/or disclosures.

3. '543 Patent

**Table 6: Exemplary Anticipatory and Combinations
for the Asserted Claims of the '543 Patent**

Chart	Prior Art References
C1	Kuboi either alone or in combination with one or more of the knowledge of a person of ordinary skill in the art.
C2	NXP either alone or in combination with one or more of Kuboi and Obara.
C3	Wang189 either alone or in combination with one or more of Kuboi, NXP, Obara, and Wang981.
C4	Obara either alone or in combination with one or more of Kuboi and NXP.
C5	Canon Product either alone or in combination with one or more of DARPA Imaging Sensor, Solar Cells, and Kuboi.
C6	Sony CMOS Product either alone or in combination with one or more of DARPA Imaging Sensor, Solar Cells, NXP, Obara, and Kuboi.
C7	Omnivision CMOS Product either alone or in combination with one or more of DARPA Imaging Sensor, Solar Cells, and Kuboi.
C8	Samsung Product under Plaintiff's apparent interpretation of the asserted claims

The prior art identified above, and in the attached '543 charts, individually anticipate and/or can properly be combined in multiple ways to demonstrate the obviousness of the Asserted Claims of the '543 patent. Various combinations of the references would have naturally been considered as part of the exercise of ordinary skill by one skilled in the art. The references disclosed in the attached charts and herein are also directed to the same or similar features as the purported invention claimed in the Asserted Claims of the '543 patent. To the extent Plaintiff contends that any of these features solved a problem in the art, the references cited herein show that that problem was known to those of ordinary skill and had already been solved using obvious solutions.

Dated: May 2, 2025

/s/ Benjamin R. Schlesinger

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Samsung Electronics America, Inc.*

CERTIFICATE OF SERVICE

The undersigned hereby certifies that on May 2, 2025, copies of the foregoing Defendants' Invalidity Contentions and Exhibits have been served to Plaintiff through its counsel of record via email.

/s/ Seth D. Katz
Seth D. Katz
Case Manager



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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
19/036,506

RECEIPT DATE / TIME
09/16/2025 11:52:23 AM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4276	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	72308372	FILING DATE	01/24/2025
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Gerard Wissing

Documents

TOTAL DOCUMENTS: 8

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV2_IDS_Trans_Filed_16Sep2025_w_Exhibits.pdf	47	Transmittal Letter	360 KB
309-0015USCIPDIV2_IDS_Filed_16Sep2025.pdf	5	Information Disclosure Statement (IDS) Form (SB08)	1315 KB
309-0015USCIPDIV2_Resp_NFO A_Mailed_18Mar2025_Final-APP.TEXT.docx	8	Application body structured text document	169 KB

Warning: The claims appear to contain an improper dependency with at least one claim that depends on a missing or canceled claim. Please review and revise if necessary. The automatic document description has been replaced. The claims appear to contain

an improper dependency with at least one claim that depends on a missing or canceled claim. Please review and revise if necessary.

JP2002314116A_orig_certifiedEnglTrans.pdf	9	Foreign Reference	3633 KB
JP2007129024A__orig_certifiedEnglTrans.pdf	29	Foreign Reference	13823 KB
EP2172974A1.pdf	23	Foreign Reference	1486 KB
Yahaya_Characterization of light absorption.pdf	7	Non Patent Literature	2611 KB
309-0015USCIPDIV2_Resp_NFOA_Mailed_18Mar2025_Final.pdf	8	Auxiliary PDF of Application	249 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV2_IDS_Trans_Filed_16Sep2025_w_Exhibits.pdf	02C1DE437530E2BF74EB3F46C5C87F303769013B5348E9D351C1CD9BA1063E45D44529C672099DA5A8F38D20BD1FE59EDBEA3AFFC41D0B0FE0D9DB417DFB778C
309-0015USCIPDIV2_IDS_Filed_16Sep2025.pdf	310D03632AF27097590172C1E4B4BE1C205EFE267C0B26AD49A5B301C550FDFB904DD3F156C98ED161D7FFDC5B9D3DBD46AB7BFD0225C1ABA0588CA08E6F0A65
309-0015USCIPDIV2_Resp_NFOA_Mailed_18Mar2025_Final-APP.TEXT.docx	C2665AE1AA207EEE9D0BAD65CB5E4622670E2DBB37CA5B3B9C9757EB26EFAA4A1D79931B4A2F0B83B7E32C081C9C5C97856AF8F0505455EB98F8BE1D37B09F0B
JP2002314116A_orig_certifiedEnglTrans.pdf	F0E59FF153B8067D7298BB8775D8CC5E80A519FF2697C0494B6639FB3EF1B572649855A962159FFCE1685B9CC3D831A212DBF2AA3885AA17B4BB0103005E0E47
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EP2172974A1.pdf	91348CE85D472E4E7B9A17527FD2D4C5C137283C4D9CAD535A7E4EA85074C4CA01109500EECF8EB0D0AD5C70DBCDB79A79029F1FCE537BBBAB512685E149C052
Yahaya_Characterization of light absorption.pdf	0A81649ADC36BA9F45E8584751F6648298CB6E45ED1F9C09E1C6B780DB451C9A1CB15621E6F56AADCEEE23366E8CDB6089DD26443141AB61391FF41B92C20D22

309-	4866713B6FC11DB9FB43A8E69B7F96B96562B01DFD7E4638D
0015USCIPDIV2_Resp_NFOA	8A303E39173DA8584A542B6BBF8A181ABCF4E2D5C5E4A2AF
_Mailed_18Mar2025_Final.pdf	F293C57420A77559550CEDF4F609F84

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 19/036,506		Filing Date 01/24/2025		☐ To be Mailed	
ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO									
APPLICATION AS FILED - PART I									
FOR		(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A	N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A	N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A	N/A					
TOTAL CLAIMS (37 CFR 1.16(j))		minus 20 =	*	x \$80 =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*	x \$ 240 =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL					
APPLICATION AS AMENDED - PART II									
		(Column 1)		(Column 2)	(Column 3)				
AMENDMENT	09/16/2025	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(j))	* 13	Minus	** 20	= 0	x \$ 80 =		0	
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	x \$ 240 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(j))	*	Minus	**	=	x \$ 0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$ 0 =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						PSS			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/TERRANCE R LAWRENCE/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".									
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
19/036,506	01/24/2025	Shih-Yuan WANG	309-0015USCIPDIV2

CONFIRMATION NO. 4276

PUBLICATION NOTICE



OC00000090095966

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
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Date Mailed: 06/13/2025

Title:MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Publication No.US-2025-0194293-A1

Publication Date:06/12/2025

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be viewed using the USPTO's publicly available Searchable Databases via the Patent Public Search tool at www.uspto.gov. The direct link to access the Patent Public Search tool is currently <https://ppubs.uspto.gov/pubwebapp/static/pages/ppubsbasic.html>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through Patent Center, the USPTO's electronic patent application filing and management system. The direct link to access this status information is currently <https://patentcenter.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of Patent Center.

Further assistance in electronically accessing the publication, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
19/036,506	01/24/2025	Shih-Yuan WANG	309-0015USCIPDIV2	4276
139982	7590	03/18/2025	EXAMINER	
Wissing Miller LLP			RODELA, EDUARDO A	
Industrious at Hudson Yards			ART UNIT	
31 Hudson Yards, 11th Floor			PAPER NUMBER	
New York, NY 10001			2893	
			NOTIFICATION DATE	DELIVERY MODE
			03/18/2025	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

DETAILED ACTION

This correspondence is in response to the communications received March 4, 2025.

Claims 18-36 are pending.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority

Respectfully, Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, 365(c), or 386(c) is acknowledged. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120 Benefit of earlier filing date in the United States as (see MPEP1504.20) follows:

The later-filed application must be an application for a patent for an invention **which is also disclosed in the prior application** (the parent or original nonprovisional application or provisional application). The disclosure of the invention in the parent application and in the later-filed application must be sufficient to comply with the requirements of 35 U.S.C. 112(a) or the first paragraph of pre-AIA 35 U.S.C. 112, except for the best mode requirement. See *Transco Products, Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 32 USPQ2d 1077 (Fed. Cir. 1994).

The disclosure of the prior-filed application, Application No. (18/822,880, 18/385,213, 18/113,474), fails to provide adequate support or enablement in the manner provided by 35

U.S.C. 112(a) or pre-AIA 35 U.S.C. 112, first paragraph for one or more claims of this application. The content which is not supported by the disclosure of any of the parent application disclosures (nor this instant application's disclosure) can be found in **claim 18** as the recitation of, "one or more holes that are fabricated as recesses in each of at least some of the pillars, extend in up-down directions to depths of less than 10000 nm, and are filled at least partly with solid dielectric material" and **claim 32** as the recitation of, "wherein each of at least some of the holes has at least one closed contour at an intermediate area of the light-receiving surface of the pillar in which the hole is fabricated, extends down into the pillar in which the hole is fabricated to a depth of less than 10000 nm, and is filled at least partly with solid dielectric material".

Conversely, Fig. 11A of parent application 17/974,325, appears to support both claims 18 and 32. It is noted that the figures of this '325 patent are not the same figures as that of the instant Application.

Possible status as CIP

This application repeats a substantial portion of prior Application No. (*see all parent applications 18/822,880, 18/385,213, 18/113,474*), filed 9/3/2024, 10/30/2023, 2/23/2023, 10/26/2022, respectively, and adds disclosure not presented in the prior applications. Because this application names the inventor or at least one joint inventor named in the prior application, it may constitute a continuation-in-part of the prior application. Should applicant desire to claim the benefit of the filing date of the prior application, attention is directed to 35 U.S.C. 120, 37

CFR 1.78, and MPEP § 211 *et seq.* The presentation of a benefit claim may result in an additional fee under 37 CFR 1.17(w)(1) or (2) being required, if the earliest filing date for which benefit is claimed under 35 U.S.C. 120, 121, 365(c), or 386(c) and 1.78(d) in the application is more than six years before the actual filing date of the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 18 and 32 and the claims that depend therefrom are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

The content which is not supported by this instant application's disclosure can be found in **claim 18** as the recitation of, "one or more holes that are fabricated as recesses in each of at least some of the pillars, extend in up-down directions to depths of less than 10000 nm, and are

filled at least partly with solid dielectric material” and **claim 32** as the recitation of, “wherein each of at least some of the holes has at least one closed contour at an intermediate area of the light-receiving surface of the pillar in which the hole is fabricated, extends down into the pillar in which the hole is fabricated to a depth of less than 10000 nm, and is filled at least partly with solid dielectric material”.

The claims set forth the requirement for a physical arrangement of an array of:

- 1.) pillars [supported by Fig. 49 and associated description in specification]
- 2.) “one or more holes that are fabricated as recesses into the light receiving surface of each of at least some of the pillars” [supported by Fig. 49 and associated description in specification]
- 3.) [*above unsupported limitations*] “wherein each of at least some of the holes ... extends down into the pillar in which the hole is fabricated to a depth of less than 10000 nm, and (iii) is filled at least partly with solid dielectric material”.

Aspect 3.) does not appear to be supported by the specification for the reason that there is not support for of a 1.) pillar with a 2.) hole formed in the upper surface of the pillar, **and 3.) the hole’s specific depth, and, the holes in the pillars being filled with “solid dielectric material”**. No drawings show this, nor does the disclosure that supports the arrangement of 1.) and 2.) show any details regarding 3.).

Claims 18 and 32 and the claims that depend therefrom are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, because the specification, while being

enabling for “*microstructure enhanced absorption photosensitive devices*”, does not reasonably provide enablement for an “integrated structure comprising an array of pillars”. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make or use the invention commensurate in scope with these claims. Essentially, the disclosure does not support the full breadth of the claims which as presently shown include that the pillars could be sized to be on the order of magnitude of either millimeter or nanometer sized pillars, which is not disclosed and whereas the disclosure specifically centers the pillar dimensions at around 100 micrometers (see ¶ 0091-0093) and micrometers in general.

After consideration of all the wands factors and in particular the relevant factors as shown in the analysis below.

A. Breadth of the claims;

The recitation of the “integrated structure comprising an array of pillars” as claimed is not commensurate with the scope of the enablement and not adequately supported by the written description. Other dimensions like millimeters or nanometers would be included as dimensions for the pillars in the current scope of the claim recitation.

B. The nature of the invention;

Adjusting the dimensions of the group IV material pillars to be able to increase light sensitivity specific to the disclosed wavelengths of interest.

C. The state of the prior art; D. The level of one of ordinary skill; E. The level of predictability in the art;

The Applicant provides no known related prior art of similar structure with the holes in the microstructure pillar array.

F. The amount of direction provided by the inventor;

The inventor does not provide enough direction to support the full scope of the claims.

The following is a quotation of 35 U.S.C. 112(b):

(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 32 and the claims that depend therefrom are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention.

The following content renders the claims indefinite, as they seem to contradict other aspects of the claim.

The **claim 32** recitation, “wherein each of at least some of the holes has at least one *closed contour* at an intermediate area of the light-receiving surface of the pillar in which the hole is fabricated”. The widely held definition of “contour” being, “the outline of a figure, body or mass”. This seems to conflict with the earlier claim 32 limitation of, “one or more holes that are fabricated as *recesses into the light- receiving surface* of each of at least some of the pillars”, as it would seemingly close the light receiving surface as a *closed* contour when viewed from cross sectional view. If thinking of this closed contour from plan view, it is unclear how that represent what is disclosed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 18-36 are rejected under 35 U.S.C. 103 as being unpatentable over Jin et al. (US 2018/0182806) in view of Wang et al. (US 11,830,954).

FIG. 2

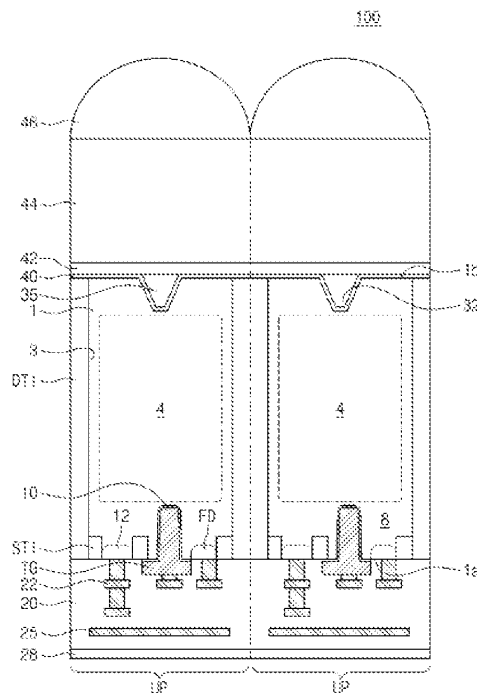
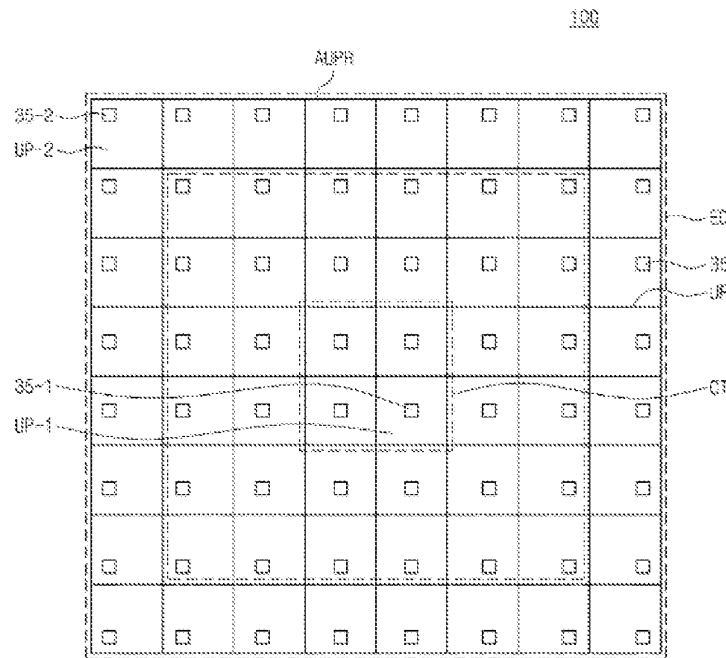


FIG. 5



Regarding claim 18, Jin discloses in Figs. 2 and 5, an integrated structure (structure shown includes the integration of transistors with ‘TG’ and photoconversion elements 4/8) comprising:

an array of pillars in which the pillars (each pixel of 4/8 are considered to be pillars as they are separated by DTI, thus forming separated pillars) extend in up-down directions (as can be seen in Fig. 2) and comprise Si, Ge, and/or alloyed SiGe semiconductor material (see ¶ 0040), wherein at least some of the pillars include photodetectors (¶ 0045, “The first impurity injection region 8 and the second impurity injection region 4 may constitute a photoelectric converter (e.g., a photodiode)”) and have respective light-receiving surfaces (top surface of 8) and respective sides (sides of 8);

wherein at least some of the pillars comprise P-doped and N-doped regions (regions 4 and 8 of oppositely doped conductivity type, ¶ 0045) and are configured to respond to illumination with light in visible and infrared wavelengths by generating electrical charge carriers (definition of a “photoelectric converter”, ¶ 0045);

one or more holes that are fabricated as recesses in each of at least some of the pillars (“recess region 32”, ¶ 0050), extend in up-down directions (32 extends vertically into top surface of portion 8) to depths (shown depths of 32), and are filled at least partly with solid dielectric material (35, “35 may include at least one of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, and a metal oxide layer.”, ¶ 0052);

side-isolation (DTI) comprising solid dielectric material (¶ 0071, “deep trench isolation structure DTI may include at least one of a silicon oxide layer, a silicon nitride layer, and a silicon oxynitride layer”) between at least portions of the sides of at least some of the pillars (DTI between the 4/8 pillars);

electrical contacts (FD and 22) configured to provide electrical pathways coupled to at least some of the photodetectors (shown connected to 4/8).

Jin fails to disclose,

“one or more holes that are fabricated as recesses in each of at least some of the pillars, extend ... to depths of less than 10000 nm;

electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for selected reverse-biasing at least some of the photodetectors;

wherein the presence of the one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes.”

Wang discloses in Fig. 11A,

one or more holes that are fabricated as recesses in each of at least some of the pillars, extend ... to depths of less than 10000 nm (140, depth shown col. 17, lines 16-27);

electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for selected reverse-biasing at least some of the photodetectors (discussed throughout the disclosure including col. 21, lines 39-51);

wherein the presence of the one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes (discussed throughout the disclosure, including col. 22, lines 15-20).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to use the limitations of,

“one or more holes that are fabricated as recesses in each of at least some of the pillars, extend ... to depths of less than 10000 nm;

electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for selected reverse-biasing at least some of the photodetectors;

wherein the presence of the one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes.”, as disclosed by Wang in the system of Jin, for the purpose of improving the performance characteristics of the light sensing array. *G. TSM: Teaching, Suggestion, Motivation Test.*

Regarding claim 19, the prior art of Jin et al. disclose the integrated structure of claim 18, and Wang discloses, in which the array is monolithically integrated with Si electronic devices (Jin discloses transistors shown, which are provided to read out the collected light signals of the 4/8).

Regarding claim 20, the prior art of Jin et al. disclose the integrated structure of claim 18, and Wang discloses, in which each of at least some of the holes is elongated along the light-receiving surface of the pillar in which the hole is fabricated so that the hole is longer in a first than in a second direction that is transverse to the first direction (see col. 26, lines 42-49).

Regarding claim 21, the prior art of Jin et al. disclose the integrated structure of claim 20, and Wang discloses, in which each of at least some of the pillars has a plurality of the elongated holes (see col. 26, lines 42-49).

Regarding claim 22, the prior art of Jin et al. disclose the integrated structure of claim 20, and Wang discloses, in which each of at least some of the pillars has only one of the elongated holes (see col. 30, lines 3-8).

Regarding claim 23, the prior art of Jin et al. disclose the integrated structure of claim 20, and Wang discloses, in which the pillars in which the holes are fabricated have respective widths at the light receiving surfaces thereof and each of at least some of the elongated holes extends in the first direction along less than the width of the pillar in which the hole is fabricated (see col. 26, lines 42-49).

Regarding claim 24, the prior art of Jin et al. disclose the integrated structure of claim 20, and Wang discloses, in which each of at least some of the elongated holes has at least one closed contour remote from side edges of the pillar in which the hole is fabricated (see arrangements in Figs. 1C-1E).

Regarding claim 25, the prior art of Jin et al. disclose the integrated structure of claim 18, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors (see Fig. 11A of Wang, showing 1150/1152 across from 510).

Regarding claim 26, the prior art of Jin et al. disclose the integrated structure of claim 18, in which two or more of the photodetectors are connected electrically in parallel (see Fig. 11A of Wang, showing 1150/1152 across from 510).

Regarding claim 27, the prior art of Jin et al. disclose the integrated structure of claim 18, wherein the array is monolithically integrated with Si electronic devices for signal processing

and transmission (In Jin Fig. 2, transistors shown, which are provided to read out the collected light signals of the 4/8).

Regarding claim 28, the prior art of Jin et al. disclose the integrated structure of claim 18, wherein the array is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors (In Jin Fig. 2, transistors shown, which are provided to read out the collected light signals of the 4/8).

Regarding claim 29, the prior art of Jin et al. disclose the integrated structure of claim 18, in which each of at least some of the holes is shaped as a square or a rectangle or a circle or an oval at the light-receiving surface of the pillar in which the hole is fabricated (Jin shows in Fig. 5 where the 35 fill called 35-1 are square/rectangle shaped, Fig. 9 shows circle shaped).

Regarding claim 30, the prior art of Jin et al. disclose the integrated structure of claim 18, further including solid dielectric material underlying the array of pillars (Jin shows “interlayer insulating layer 20”, ¶ 0048).

Regarding claim 31, the prior art of Jin et al. disclose the integrated structure of claim 29, in which each of at least some of the pillars has two or more of the holes at the light receiving surface of the pillar (see Wang’s Figs. 2A-2C, which show multiple micro holes per photodetector).

Regarding claim 32, Jin discloses in Figs. 2 and 5, an integrated structure comprising:

an array of pillars (each pixel of 4/8 are considered to be pillars as they are separated by DTI, thus forming separated pillars) in which the pillars extend in up-down directions (shown extending vertically) and comprise Si, Ge, and/or alloyed SiGe semiconductor material (see ¶ 0040), wherein each of at least some of the pillars has sides (sides of portion 8) and a light-receiving surface (top surface of portion 8) and comprises at least one photodetector (¶ 0045, “The first impurity injection region 8 and the second impurity injection region 4 may constitute a photoelectric converter (e.g., a photodiode)”);

wherein at least some of the pillars comprise P-doped and N-doped regions (see ¶ 0045 discloses the oppositely doped regions of 4 and 8) and are configured to respond to illumination with light in visible and infrared wavelengths by generating electrical charge carriers (definition of a “photoelectric converter”, ¶ 0045);

one or more holes (32) that are fabricated as recesses into the light-receiving surface of each of at least some of the pillars (32 formed into the top surface of 8),

wherein each of at least some of the holes (i) has at least one closed contour at an intermediate area of the light-receiving surface of the pillar in which the hole is fabricated (Fig. 5 shows a “closed contour” as element 35-1 which represents the fill 35 in hole 32 in Fig. 2), (ii) extends down into the pillar (32 extending into pillar 4/8), and (iii) is filled at least partly with

solid dielectric material (35, “35 may include at least one of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, and a metal oxide layer.”, ¶ 0052);

side-isolation (DTI) comprising solid dielectric material (¶ 0071, “deep trench isolation structure DTI may include at least one of a silicon oxide layer, a silicon nitride layer, and a silicon oxynitride layer”) between at least portions of the sides of at least some of the pillars (DRI between pillars 4/8);

electrical contacts (FD and 22) configured to provide electrical pathways coupled to at least some of the photodetectors (shown connected to 4/8);

wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission (transistors shown, which are provided to read out the collected light signals of the 4/8).

Jin does not disclose,

“wherein each of at least some of the holes (ii) extends down into the pillar in which the hole is fabricated to a depth of less than 10000 nm,

electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for selected reverse-biasing of the photodetectors;

wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the holes”.

Wang discloses in Fig. 11A,

“wherein each of at least some of the holes (ii) extends down into the pillar in which the hole is fabricated to a depth of less than 10000 nm (140, depth shown col. 17, lines 16-27),

electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for *selected reverse-biasing of the photodetectors* (discussed throughout the disclosure including col. 21, lines 39-51);

wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the holes (discussed throughout the disclosure, including col. 22, lines 15-20).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to use the limitations of,

“wherein each of at least some of the holes (ii) extends down into the pillar in which the hole is fabricated to a depth of less than 10000 nm,

electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for *selected reverse-biasing of the photodetectors*;

wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the holes”, as disclosed by Wang in the system of Jin, for the purpose of improving the performance characteristics of the light sensing array. *G. TSM: Teaching, Suggestion, Motivation Test.*

Regarding claim 33, the prior art of Jin et al. disclose the integrated structure of claim 32, in which each of at least some of the pillars has only one of the holes fabricated therein (see Fig. 2 of Jin which shows one 35 per pixel pillar).

Regarding claim 34, the prior art of Jin et al. disclose the integrated structure of claim 32, in which each of at least some of the pillars has at least two of the holes fabricated therein (see Wang's Figs. 2A-2C, which show multiple micro holes per photodetector).

Regarding claim 35, the prior art of Jin et al. disclose the integrated structure of claim 32, in which each of at least some of the pillars includes only a single photodetector (see Fig. 2 of Jin which shows one 35 per pixel pillar).

Regarding claim 36, the prior art of Jin et al. disclose the integrated structure of claim 32, and Wang discloses, in which each of at least some of the holes is elongated along the light-receiving surface of the pillar in which the hole is fabricated (see col. 26, lines 42-49, if "rectangular" shape selected, this limitation is met).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A Rodela whose telephone number is (571)272-8797. The examiner can normally be reached M-F, 8:30-5:00pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yara B Green can be reached on (571) 270-3035. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Primary Examiner, Art Unit 2893

<i>Notice of References Cited</i>	Application/Control No. 19/036,506	Applicant(s)/Patent Under Reexamination WANG et al.	
	Examiner Eduardo A Rodela	Art Unit 2893	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Name	CPC Classification	US Classification
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*	B	US-11037794-B2	2021-06-15	Xu; Xiaobin	H01L21/3083	1/1
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U.S. Patent and Trademark Office
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Notice of References Cited

Part of Paper No. 20250310

Search Notes 	Application/Control No. 19/036,506	Applicant(s)/Patent Under Reexamination WANG et al.
	Examiner Eduardo A Rodela	Art Unit 2893

CPC - Searched*		
Symbol	Date	Examiner
(H10F39/014,024,8027,806,8067; H10F71/121,1212,1215; H10F77/14,147,40,413,488,70,703; H10F77/703; H10F30/223; H10F77/122; H10F77/1226; H10F77/14; H10F77/1437; H10F77/147; H10F77/413	03/11/2025	EAR

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E search - see history for complete details	03/11/2025	EAR
Inventor & Applicant search	03/11/2025	EAR

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	56931	(micrometer OR micro OR (micro NEAR structur\$3)) WITH (pillars OR columns) WITH (plurality OR matrix OR array)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/03/11 10:28 AM
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L4	3763407	(dielectric OR oxide OR nitride OR glass OR insulat\$3) near3 (fill\$3	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY,	OR	ON	ON	2025/03/11 10:49 AM

		OR lin\$3)	CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L5	404	(L1 same3 L3 SAME L4) AND L2	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/03/11 10:49 AM
L6	137	(L1 same3 L3 SAME L4) AND L2	(US-PGPUB; USPAT)	OR	ON	ON	2025/03/11 10:49 AM
L7	49	("4983251" "6316793" "6486502" "6583454" "6682659" "8147704" "8608468" "8993380" "9000584" "9048222" "9048233" "9064879" "9111949" "9209068" "9263511" "9281254" "9299649" "9368460" "9372206" "9425126" "9431368" "9443783" "9461018" "9484482" "9496189" "9564414" "9666502" "9735131" "9899355" "10366962" "20010017370" "20030201459" "20090154871" "20100216294" "20110008484" "20110036396" "20120156321" "20130279844" "20150037044" "20150194337"	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 10:50 AM

L8	15	"20150378095" "20160190093" "20160315452" "20170092626" "20170207600" "20180308834" "20190004247").pn. OR ("11347001").urpn. AND (PGPB USPT USOC).dbnm. ("7189635" "20020133129" "20070049028" "20080061214" "20080067721" "20080217819" "20100203235").pn. OR ("8147704").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 10:51 AM
L9	13	("2010/0203235").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 10:52 AM
L11	7	("2007/0049028").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 10:55 AM
L12	40124	H10F39/014,024,8027, 806,8067.cpc. OR H10F71/121,1212,1215 .cpc. OR H10F77/14,147,40,413, 488,70,703.cpc.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 11:10 AM
L13	15	H10F77/703.cpc. AND L1 AND L3	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 11:11 AM
L14	37	H10F77/703.cpc. AND L1 AND L3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/03/11 11:11 AM
L15	402	L12 AND L1 AND L3	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	OR	ON	ON	2025/03/11 11:11 AM

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L16	132	L12 AND L1 AND L3	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 11:11 AM
L17	0	("2023/0238468").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 12:37 PM
L18	192	("4358851" "4634272" "4676599" "4702600" "4744667" "4851664" "5267016" "5288992" "5760899" "5982552" "6014232" "6133989" "6255133" "6374024" "6414746" "6690019" "6721262" "7091462" "D531525" "7170542" "7295298" "7345271" "7421159" "7433042" "7808706" "7848478" "7969558" "8013983" "8089618" "8130367" "D659030" "8319949" "8330840" "8374405" "8384997" "8494252" "8675181" "8717488" "8742325" "8743176" "8761495" "8767190" "8829406" "8836922" "8848039" "9041915" "9063549" "9071763" "9086273" "9111444" "9157790" "9164511" "9176051" "9229109" "9285464" "9285477" "9299731" "9368936" "9369689" "9383753" "9425654" "9435891" "9470520" "9489601" "9525863" "9529079" "9551791" "9992477" "10063849" "10183541" "10222458" "10222475" "20020072684" "20030006676" "20030047752"	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 12:51 PM

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L19	7	"20160047895" "20160047896" "20160047897" "20160047898" "20160047899" "20160047900" "20160047901" "20160047903" "20160049765" "20160097858" "20160150963" "20160161600" "20160218727" "20160265902" "20160291134" "20160306032" "20160327779" "20160328619" "20170146640" "20170219426" "20170219695" "20170269197" "20170269198" "20170269209" "20170269215" "20170289524" "20170350983" "20180059222" "20180067209" "20180069838" "20180136042" "20180152691" "20180299554" "20180329035" "20180329060" "20180329061" "20180329062" "20180329066" "20180359460" "20190011556" "20190011561" "20190011562" "20190011567" "20190018111" "20190146088" "20190064355").pn. OR ("10739189").urpn. AND (PGPB USPT USOC).dbnm. ("4407695" "6835317" "8501020" "9675790" "9993948" "20080047929" "20170110330").pn. OR ("11037794").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 12:53 PM
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L20	19	("4407695" "7046441" "7483130" "7700520" "20060002656" "20060228722" "20070177647" "20070184204" "20070284570" "20080047929" "20100087723" "20100221866" "20100244079" "20110195201" "20120152353" "20120170033").pn. OR ("8501020").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 12:54 PM
L21	19	("4117506" "4403239" "5211761" "8344241" "20010013362" "20020011263" "20020192441" "20040084080" "20040109666" "20050098205" "20050121068" "20060118166" "20060207647" "20090194152" "20090283139" "20100096013" "20100186802" "20110162706" "20130048070").pn. OR ("9406824").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 01:03 PM
L22	46234	(H10F77/703 OR H10F30/223 OR H10F77/122 OR H10F77/1226 OR H10F77/14 OR H10F77/1437 OR H10F77/147 OR H10F77/413).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/03/11 01:38 PM
L23	42674	L12 OR L22	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2025/03/11 01:39 PM
L24	133	L23 AND L1 AND L3	(US-PGPUB; USPAT;	OR	ON	ON	2025/03/11

L25	31	("4814847" "5266814" "6667528" "7015139" "7132677" "7183127" "20050255581" "20070158661" "20070210349" "20080105296").pn. OR ("8357960").urpn. AND (PGPB USPT USOC).dbnm.	USOCR) (US-PGPUB; USPAT; USOCR)	OR	ON	ON	01:39 PM 2025/03/11 01:40 PM
L26	5	((("W&W") near3 ("SENS") near3 ("DEVICES") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT)	OR	ON	ON	2025/03/11 02:45 PM
L27	865	((("WANG") near3 ("Shih-Yuan")) OR (("WANG") near3 ("Shih-Ping"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2025/03/11 02:45 PM
L28	1	(L26 OR L27) AND ((pillars)(photodetectors)(light NEAR receiving NEAR surfac\$2)(light)(respond)(visible OR infrared)(wavelength\$1)(holes)(recess\$3)(filled)(dielectric NEAR material)(absorption)).clm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2025/03/11 02:48 PM
L29	40	("5315147" "5759292" "6879014" "7276749" "7396696" "7525170" "8129710" "8357960" "8558336" "8946675" "9000492" "9184202" "9263519" "9515218" "10411053" "10522582" "11211419" "11309444" "11728457" "20050145779" "20080083963" "20100320444" "20110156195" "20110297214" "20110309331" "20120012741" "20120153127" "20120153416"	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2025/03/11 02:48 PM

L30	10	"20120196401" "20130125965" "20140016660" "20160240579" "20170141153" "20180012918" "20180102442" "20180182806" "20190001989" "20190166317" "20200006407" "20200006416").pn. OR ("12243948").urpn. AND (PGPB USPT USOC).dbnm. ("20150372034" "20160112614" "20170104020" "20170117309" "20180151759" "20180182806" "20180359434").pn. OR ("11211419").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2025/03/11 02:50 PM
L31	1	"11830594".pn.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2025/03/11 03:30 PM
L32	1	"11830954".pn.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2025/03/11 03:31 PM
L33	9	("9209320" "9331116" "9876045" "11594657" "20100271524" "20140167066" "20180033895" "20200135776" "20210305440").pn. OR ("11830954").urpn. AND (PGPB USPT USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2025/03/11 03:34 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
19/036,506	01/24/2025	Shih-Yuan WANG	309-0015USCIPDIV2

CONFIRMATION NO. 4276

POA ACCEPTANCE LETTER



OC00000085749945

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Date Mailed: 03/13/2025

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/03/2025.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/dtdinh/



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
19/036,506	01/24/2025	2893	1082	309-0015USCIPDIV2	19	2

139982

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

CONFIRMATION NO. 4276

CORRECTED FILING RECEIPT



0000000085/50387

Date Mailed: 03/13/2025

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping Wang, Los Altos, CA;

Applicant(s)

W&WSens Devices, Inc, Los Altos, CA;

Power of Attorney: The patent practitioners associated with Customer Number 139982

Domestic Applications for which benefit is claimed

This application is a DIV of 18/822,880 09/03/2024 PAT 12,243,948
which is a DIV of 18/385,213 10/30/2023 PAT 12,087,871
which is a CIP of 17/974,325 10/26/2022 PAT 11,830,954
and is a CIP of 18/113,474 02/23/2023

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - **None.**
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/28/2025

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 19/036,506**

Projected Publication Date: 06/12/2025

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Preliminary Class

136

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

page 2 of 4

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
19/036,506		Shih-Yuan WANG	309-0015USCIPDIV2	4276
139982	7590	03/04/2025	EXAMINER	
Wissing Miller LLP Industrious at Hudson Yards 31 Hudson Yards, 11th Floor New York, NY 10001			ART UNIT	PAPER NUMBER
			NOTIFICATION DATE	DELIVERY MODE
			03/04/2025	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com



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Commissioner for Patents
United States Patent and Trademark Office
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In re Application of :
WANG et al. :
Application No. 19/036,506 : DECISION ON PETITION
Deposited: January 24, 2025 :
For: MICROSTRUCTURE ENHANCED :
ABSORPTION PHOTSENSITIVE DEVICES :

This is a decision on the petition under 37 CFR 1.102(c)(1), filed January 28, 2025, to make the above-identified application special based on applicant's age as set forth in MPEP § 708.02, Section II.

There is no indication that the petition is signed by a registered patent attorney or patent agent of record. However, in accordance with 37 CFR 1.34, the signature of Ivan S. Kavrukov appearing on the correspondence shall constitute a representation to the United States Patent and Trademark Office that he or she is authorized to represent the particular party on whose behalf he or she acts.

The petition is **GRANTED**.

A grantable petition to make an application special under 37 CFR 1.102(c)(1) and MPEP § 708.02, Section II: Applicant's Age, must be accompanied by evidence showing that the applicant is 65 years of age, or more, such as applicant's statement or a statement from a registered practitioner that he or she has evidence that the applicant is 65 years of age or older. No fee is required.

The instant petition includes a statement from a registered practitioner that he or she has evidence that a joint applicant is 65 years of age or older. Accordingly, the above-identified application has been accorded "special" status.

Telephone inquiries concerning this decision should be directed to Jamice Brantley at 571-272-3814.

/JAMICE T BRANTLEY/

Jamice T Brantley
Paralegal Specialist, Office of Petitions



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
19/036,506	01/24/2025	Shih-Yuan WANG	309-0015USCIPDIV2

CONFIRMATION NO. 4276

IMPROPER CFR REQUEST



OC000000085125812

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Date Mailed: 03/04/2025

RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

Continuity, Priority Claims, Petitions, and Non-Publication Requests

In response to your request for a corrected filing receipt dated 01/24/2025, the Office is unable to comply with your request because:

- One or more of the benefit claims under 35 U.S.C. § 120 cannot be included on the Filing Receipt since applicant did not specify whether the application is a continuation, divisional or continuation-in-part of the prior application. Applicant must submit a new application data sheet (ADS) that sets forth the relationship, and the ADS must be accompanied by a petition under 37 CFR 1.78 if filed after the time period set forth in 37 CFR 1.78.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/ygizaw/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
19/036,506	01/24/2025		1082	309-0015USCIPDIV2	19	2

CONFIRMATION NO. 4276

139982

Wissing Miller LLP

Industrious at Hudson Yards

31 Hudson Yards, 11th Floor

New York, NY 10001

FILING RECEIPT



0000000085126067

Date Mailed: 03/04/2025

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;

Shih-Ping Wang, Los Altos, CA;

Applicant(s)

W&W Sens Devices, Inc, Los Altos, CA;

Power of Attorney: None

Domestic Applications for which benefit is claimed

This application is a DIV of 18/822,880 09/03/2024 PAT 12,243,948

which is a DIV of 18/385,213 10/30/2023 PAT 12,087,871

which is a CIP of 17/974,325 10/26/2022 PAT 11,830,954

and is a CIP of 18/113,474 02/23/2023

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - **None**. Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/28/2025

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 19/036,506**

Projected Publication Date: 06/12/2025

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

page 2 of 4

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

**LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET Substitute for Form PTO-1360 (For use with Form PTO/SB/06)							Application Number 19/036,506		Filing Date				
							Applicant(s) Shih-Yuan WANG						
							* May be used for additional claims or amendments						
CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT			*		*		*	
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PATENT APPLICATION FEE DETERMINATION RECORD						Application or Docket Number 19/036,506			
Substitute for Form PTO-875									
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA		RATE(\$)	FEE(\$)	RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	70	N/A			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A		N/A	308	N/A			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	352	N/A			
TOTAL CLAIMS (37 CFR 1.16(i))	19	minus 20 = *	0	x	= 0	OR			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 = *		x	= 0				
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				180				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					0				
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	910	TOTAL			
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x
	Application Size Fee (37 CFR 1.16(s))							OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x
	Application Size Fee (37 CFR 1.16(s))							OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR	
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE
<p>* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.</p> <p>** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".</p> <p>*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".</p> <p>The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.</p>									

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UNITED STATES
PATENT AND TRADEMARK OFFICE •

Doc Code: R46C.REQ

Document Description: Request under 37 CFR 1.46(c) to correct, update or change the applicant.

PTO/AIA/41 (04-15)
Approved for use through 11/30/2027. OMB 0651-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**REQUEST TO CORRECT OR UPDATE
THE NAME OF THE APPLICANT UNDER
37 CFR 1.46(c)(1), OR CHANGE THE
APPLICANT UNDER 37 CFR 1.46(c)(2)
(FOR USE ONLY IN APPLICATIONS FILED ON OR AFTER
SEPTEMBER 16, 2012)**

Application Number	19/036,506
Filing Date	January 24, 2025
First Named Inventor	Shih-Yuan WANG
Art Unit	OPAP
Examiner Name	DOCKET CENTRAL
Practitioner Docket Number	309-0015USCIPDIV2

To: **Commissioner for Patents**
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant hereby **requests that the name of the applicant be corrected or updated under 37 CFR 1.46(c)(1), or that the applicant be changed under 37 CFR 1.46(c)(2),** in the above-identified application. **Requests under 37 CFR 1.46(c)(1) or (c)(2) cannot be submitted after payment of the issue fee or if the application has been patented.**

Please check the applicable box(es) below.

☒ 1. This request is to **correct or update the name of the applicant (under 37 CFR 1.46(c)(1))** and includes:

☒ An application data sheet (ADS) in accordance with 37 CFR 1.76(c) with the corrected or updated information shown with markings (e.g., underlining for insertions, strikethrough for deletions). A Corrected Web-based ADS may be used.

Note: Requests under 37 CFR 1.46(c)(1) may be filed to correct typographical errors in the name of the § 1.46 applicant, or for updating the name of the § 1.46 applicant (i.e., where there is no change in the applicant itself but just in the applicant's name). See the Manual of Patent Examining Procedure (MPEP) section 605.01.

☐ 2. This request is to **change the applicant (under 37 CFR 1.46(c)(2))** and includes:

☐ An application data sheet (ADS) in accordance with 37 CFR 1.76(c) that identifies the changes with proper markings (underlining for insertions and strikethrough for deletions). A Corrected Web-based ADS may be used.

☐ A Statement Under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent). See MPEP 325.

I am the

☐ applicant*

☒ attorney or agent of record
Registration number 25161

☐ attorney or agent acting under 37 CFR 1.34
Registration number _____

Signature /Ivan S. Kavrukov/

Typed or printed name Ivan S. Karukov

Date March 3, 2025

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. *Juristic entities must be represented by a patent practitioner (See 37 CFR 1.31, applicable to any paper filed on or after September 16, 2012 that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below**.

☒ ** Total of 1 forms are submitted.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0031. Public burden for this form is estimated to average 12 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. If filing this completed form by mail, send to: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013), <https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf>.

Routine uses of the information in this record may include disclosure to: 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law; 2) a federal, state, local, or international agency, in response to its request; 3) a contractor of the USPTO having need for the information in order to perform a contract; 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record; 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record; 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations; 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals; 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)); 9) the Office of Personnel Management (OPM) for personnel research purposes; and 10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: W&WSens Devices, Inc.
Application No./Patent No.: 19/036,506 Filed/Issue Date: January 24, 2025
Titled: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
W&WSens Devices, Inc., a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 070024, Frame 0531, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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5. From: _____ To: _____

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6. From: _____ To: _____

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Ivan S. Kavrukov/

March 3, 2025

Signature

Date

Ivan S. Kavrukov

25161

Printed or Typed Name

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	19/036,506
Filing Date	January 24, 2025
First Named Inventor	Shih-Yuan WANG
Title	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Art Unit	OPAP
Examiner Name	CENTRAL DOCKET
Attorney Docket Number	309-0015USCIPDIV2

SIGNATURE of Applicant or Patent Practitioner			
Signature	/Ivan S. Kavrukov/	Date (Optional)	
Name	Ivan S. Kavrukov	Registration Number	25,161
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			
<p>NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.</p>			
☐ *Total of _____ forms are submitted.			

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82B (07-13)

Approved for use through 03/31/2021, OMB 0651-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

139982

OR



I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:



The address associated with the above-mentioned Customer Number

OR



The address associated with Customer Number:

OR



Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

W&WSens Devices, Inc.



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Title

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV 2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--

Inventor Information:

Inventor 1					Remove		
Legal Name							
Prefix	Given Name		Middle Name		Family Name		Suffix
	Shih-Yuan				WANG		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service							
City	Palo Alto		State/Province	CA	Country of Residence	US	
Mailing Address of Inventor:							
Address 1		766 Encina Grande Drive					
Address 2							
City	Palo Alto		State/Province	CA			
Postal Code	94306		Country	US			
Inventor 2					Remove		
Legal Name							
Prefix	Given Name		Middle Name		Family Name		Suffix
	Shih-Ping				WANG		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service							
City	Los Altos		State/Province	CA	Country of Residence	US	
Mailing Address of Inventor:							
Address 1		38 Third Street, Suite 307					
Address 2							
City	Los Altos		State/Province	CA			
Postal Code	90422		Country	US			
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.							
Add							

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

☐ An Address is being provided for the correspondence information of this application.

Customer Number

Email Address

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Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		
Attorney Docket Number	309-0015USCIPDIV2	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	48	Suggested Figure for Publication (if any)	58

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

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Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	139982		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Division of	18822880	2024-09-03

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0016USCIPDIV2	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18822880	Division of	18385213	2023-10-30	12087871	2024-09-10
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18385213	Continuation in part of	17974325	2022-10-26	11830954	2023-11-28
Prior Application Status		Pending		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
18385213	Continuation in part of	18113474	2023-02-23		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113747	Division of	17707429	2022-03-29	11621360	2023-04-04
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17707429	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-30	10446700	2019-10-15
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113474	Continuation in part of	17707429	2022-03-29	11621360	2023-04-04

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0016USCIPDIV2	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17707429	Division of	17532832	2021-11-22	11309444	2022-04-19
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17532832	Continuation in part of	17182954	2021-02-03	11791432	2023-10-17
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Continuation in part of	PCTUS1667977	2016-12-21		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16042535	2018-07-23	10700225	2020-06-30
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16296985	2019-03-08	10468543	2019-10-16
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113474	Division of	177077429	2022-03-29	11621360	2023-04-04
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
177077429	Division of	17532831	2021-11-22	11309444	2022-04-19
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17532831	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0015USCIPDIV2	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	14947718	2015-11-20	10622498	2020-03-25
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Continuation in part of	PCTUS1667977	2016-12-21		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-20	10446700	2019-09-25
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16042535	2018-07-23	10700225	2020-06-30
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16296985	2019-03-08	10468543	2019-10-16
Prior Application Status		Abandoned		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Continuation in part of	PCTUS1643289	2016-07-23		
Prior Application Status		Abandoned		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Continuation in part of	PCTUS1657963	2016-10-29		
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Claims benefit of provisional	62713455	2018-08-01		
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Claims benefit of provisional	62716310	2018-08-08		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16526958	Claims benefit of provisional	62717750	2018-08-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16526958	Claims benefit of provisional	62719689	2018-08-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16526958	Claims benefit of provisional	62724449	2018-08-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16526958	Claims benefit of provisional	62733476	2018-09-19

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0016USCIPDIV2	Type text here
		Application Number		
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/737062	2018-09-26
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/750016	2018-10-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/770656	2018-09-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/772498	2018-09-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/777157	2018-12-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/779693	2018-12-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/784342	2018-12-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/794330	2019-01-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/797141	2019-01-25

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0016USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/797263	2019-01-26
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/800371	2019-02-01
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/802171	2019-02-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/802718	2019-02-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/805850	2019-02-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/808949	2019-02-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/819604	2019-03-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/819669	2019-03-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/820695	2019-03-19

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		Application Number	
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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/828976	2019-04-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/841798	2019-05-01
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/843206	2019-05-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/846554	2019-05-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/853280	2019-05-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/860115	2019-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/863231	2019-06-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/863852	2019-06-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/867186	2019-06-26

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		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/868911	2019-06-29		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/870533	2019-07-03		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/873891	2019-07-13		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/528958	Claims benefit of provisional	62/874418	2019-07-15		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
PCT/US18/57963	Continuation of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/797821	Continuation in part of	14/947718	2015-11-20	10622498	2020-03-25
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/797821	Continuation in part of	15/309922	2016-11-09	9818893	2017-10-25
Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
15/797821	Continuation in part of	PCT/US16/67977	2016-12-21		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
15/797821	Claims benefit of provisional	62/465734	2017-03-01		

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/474179	2017-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/484474	2017-04-12
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/487606	2017-04-20
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/488998	2017-04-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/500581	2017-05-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/505974	2017-05-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/509093	2017-05-20
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/510249	2017-05-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/514889	2017-06-04

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		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/521504	2017-06-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/522169	2017-06-20
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/527962	2017-06-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/530281	2017-07-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/533078	2017-07-16
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/533603	2017-07-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/542243	2017-08-07

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		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/547728	2017-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/542243	2017-08-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639472	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/628764	2018-02-09

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		Application Number	
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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/643010	2018-03-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/640522	2018-03-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/599246	2017-12-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/645810	2018-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/666005	2018-05-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/607860	2017-12-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/631630	2018-02-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/677609	2018-05-29

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		Application Number	
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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/634692	2018-02-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/652830	2018-04-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/591072	2017-09-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639356	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/615314	2018-01-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/623971	2018-01-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/637945	2018-03-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/651053	2018-03-30

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/682909	2018-06-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/659072	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/659067	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/669194	2018-05-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/675130	2018-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/547728	2017-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/651087	2018-03-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/646871	2018-03-22

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Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/662217	2018-04-24		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/639920	2018-03-07		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/633514	2018-02-21		
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/296985	Continuation of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/042535	Continuation in part of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/635801	2017-07-21		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/540524	2017-08-02		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/542243	2017-08-07		
Prior Application Status	Expired		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/547728	2017-08-18		

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/591072	2017-11-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/599246	2017-12-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/607860	2017-12-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/615314	2018-01-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/623971	2018-01-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/628764	2018-02-09

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/631630	2018-02-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/633514	2018-02-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/634692	2018-02-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/637945	2018-03-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639356	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639472	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639920	2018-03-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/640522	2018-03-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/643010	2018-03-14

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/645810	2018-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/646871	2018-03-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/651053	2018-03-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/651087	2018-03-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/652830	2018-04-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/659067	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/659072	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/662217	2018-04-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/666005	2018-05-02

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/669194	2018-05-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/675130	2018-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/677609	2018-05-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/682909	2018-06-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/270577	2016-12-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/304907	2016-03-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/290391	2016-02-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/334934	2016-05-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/338263	2016-05-18

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/346850	2016-06-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/359349	2017-07-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/366188	2016-07-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/368109	2016-07-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/374828	2016-08-13
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/376869	2016-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/380364	2016-08-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/383391	2016-09-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/383479	2016-09-04

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0016USCIP DIV2	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/394222	2016-09-14		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/398607	2016-09-23		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/401126	2016-09-28		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/406999	2016-10-12		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/414671	2016-10-29		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/415339	2016-10-31		
Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
15/309922	a 371 of international	PCT/US15/61120	2015-11-17		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/309922	Continuation of	14/943898	2015-11-17	9530905	2016-12-27
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/309922	Continuation of	14/945003	2015-11-18	9525084	2016-12-20

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		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/213558	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/199607	2015-07-13
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/175855	2015-06-15

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/090879	2014-12-11

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		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/182602	2015-06-21

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/100025	2015-01-05

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0016USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/188876	2015-07-06

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/174496	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/111582	2015-02-03

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/947718	Continuation of	PCT/US14/39208	2014-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/826446	2013-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/843021	2013-07-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/905109	2013-11-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/834873	2013-06-13
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/892821	a 371 of international	PCT/US14/39208	2014-05-22

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/826446	2013-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/843021	2013-07-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/905109	2013-11-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/834873	2013-06-13

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

☐	This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
	NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h) (1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1			
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
<input type="button" value="Clear"/>			
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117	
		☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor: <input type="text"/>			
If the Applicant is an Organization check here. ☒			
Organization Name		W&W Sens Devices, Inc. W&WSens Devices, Inc.	
Mailing Address Information For Applicant:			
Address 1		38 Third Street, Suite 307	
Address 2			
City		Los Altos	State/Province CA
Country	US	Postal Code	94022
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here.

☐

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		State/Province	
Country ⁱ		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Ivan S. Kavrukov/		Date (YYYY-MM-DD)	2025-01-24 2025-03-03
First Name	Ivan S.	Last Name	Kavrukov	Registration Number 25,161

Additional Signature may be generated within this form by selecting the Add button.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
19/036,506

RECEIPT DATE / TIME
03/03/2025 04:36:44 PM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4276	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	69416074	FILING DATE	01/24/2025
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 4

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV2_RequestTo CorrectApplicant-Final.pdf	2	Request under 37CFR1.46(c) to correct, update, change applicant	571 KB
309-0015USCIPDIV2__Corrected ApplicationDataSheet- Final.pdf	38	Application Data Sheet	6190 KB
Warning: This is not a USPTO supplied ADS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.			
309-0015USCIPDIV2_3.73State ment-Final.pdf	3	Assignee showing of ownership per 37 CFR 3.73	115 KB
309-0015USCIPDIV2_Transmittal	2	Power of Attorney	649 KB

OfPowerOfAttorney-Final.pdf

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV2_RequestToCorrectApplicant-Final.pdf	958952A66E83C09C3B7492FC2FA4F49FAF1C36772649B63CF6CF6E25C12E47BDC0572F6078DFBACF998F1A62FE8D50E351CB38DD2710EF0D3E46C280A2837626
309-0015USCIPDIV2__CorrectedApplicationDataSheet-Final.pdf	0ECC0A57A42C05B3093E15668905008E7CE2A22E882DA35CE261785BF84957918F72CC46F34ECA3A3CECB2A2D835723D1E78981917472B0714C30BF404C67A6E
309-0015USCIPDIV2_3.73Statement-Final.pdf	726518A35A021E4D1F9C4A524EB7B23A996C40F9DD015031E7D44D70DC3CFF7C020E7C8DB8F2C3CC8C608C99FF233416882E06255A02808FF5B70EDD64FF61E0
309-0015USCIPDIV2_TransmittalOfPowerOfAttorney-Final.pdf	C749380C5301F19FB85BBA04750E62E1B48F845920C7E4B4AACF5673E5CE24117CF6323CB222C79102EFB2EB944CB0DB09F4EEBE01B440D7B5B833E904F84CF8

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
19/036,506	01/24/2025	Shih-Yuan WANG	309-0015USCIPDIV2

CONFIRMATION NO. 4276

IMPROPER CPOA LETTER



OC000000085067638

Date Mailed: 03/03/2025

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the power of attorney filed 01/24/2025. The power of attorney in this application is not accepted for the reason(s) listed below:

The power of attorney filed 01/24/2025 has not been accepted because the power of attorney must be signed by the applicant for patent. See 37 CFR 1.32(b)(4).

- The person or entity attempting the change to power of attorney is not the applicant of record in the application. Any request to change the applicant once the applicant has been specified must include (1) an application data sheet (ADS) specifying the new applicant in the Applicant Information section, and (2) a statement under 37 CFR 3.73(c) (USPTO Form PTO/AIA/96 or an equivalent) to show chain of title to the new applicant. The ADS must contain markings to show the information that is being changed, with underlining for insertions and strike-through or brackets for text removed. See 37 CFR 1.76(c)(2).

Because the request to change or update the applicant cannot be accepted, the power of attorney is not properly signed by the applicant and cannot be accepted. The change to applicant must be acceptable before the new applicant can appoint power of attorney.

/jltippett/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001
UNITED STATES



United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :Janice Tippet

Refund Accounting Date:03/03/2025

Effective Date	Sale Item Reference Number	Refund Total
03/03/2025	19036506	\$1,600.00

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method	Account Number
I202533C52258923	2056	FILING AN APPLICATION OR PRESENTATION OF BENEFIT CLAIM MORE	\$1,600.00	DA	600125



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Sale Adjustment Accounting Date:03/03/2025

Effective Date	Sale Accounting Date	Sale Item Reference Number
03/03/2025	03/03/2025	19036506

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I202533C52258923	2056	FILING AN APPLICATION OR PRESENTATION OF BENEFIT CLAIM MORE	\$1,600.00	DA



United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :Tram Vo

Sale Accounting Date:02/28/2025

Sale Item Reference Number	Effective Date
19036506	01/24/2025

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I20252RA50056802	2081	UTILITY APPL SIZE FEE PER 50 SHEETS >100	\$180.00	Deposit Account



United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :Tram Vo

Sale Accounting Date:02/28/2025

Sale Item Reference Number	Effective Date
19036506	01/24/2025

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I20252RB07158347	2054	Non-DOCX Filing Surcharge	\$172.00	Deposit Account



United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :Janice Tippet

Sale Accounting Date:02/27/2025

Sale Item Reference Number	Effective Date
19036506	01/24/2025

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I20252QA15316404	2056	FILING AN APPLICATION OR PRESENTATION OF BENEFIT CLAIM MORE	\$1,600.00	Deposit Account



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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
19/036,506

RECEIPT DATE / TIME
01/28/2025 08:42:47 AM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4276	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68944323	FILING DATE	-
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV2_PetitionToMakeSpecialBasedOnAge-Final.pdf	2	Petition to make special based on Age/Health	180 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV2_PetitionToMakeSpecialBasedOnAge-Final.pdf	BC5F71173E212BACBD80D84072702D98C257308AB76196AA4 F18103C78F73B1FF4424567CFA407569D74EADF532CADA213 E8E16B5C52CF3DCA63A4765561BEE3

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: PET.OP.AGE

Description: Petition to make special based on age/health

PTO/SB/130 (01-19)

Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number

PETITION TO MAKE SPECIAL BASED ON AGE FOR ADVANCEMENT OF EXAMINATION UNDER 37 CFR 1.102(c)(1)					
Application Information					
Application Number	19/036,506	Confirmation Number	4276	Filing Date	January 24, 2025
Attorney Docket Number (optional)	309-0015USCIPDIV2	Art Unit	TBD	Examiner	TBD
First Named Inventor	Shih-Yuan WANG				
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES				
Attention: Office of Petitions An application may be made special for advancement of examination upon filing of a petition showing that the applicant is 65 years of age, or more. No fee is required with such a petition. See 37 CFR 1.102(c)(1) and MPEP 708.02 (II). APPLICANT HEREBY PETITIONS TO MAKE SPECIAL FOR ADVANCEMENT OF EXAMINATION IN THIS APPLICATION UNDER 37 CFR 1.102(c)(1) and MPEP 708.02 (II) ON THE BASIS OF THE APPLICANT'S AGE. A grantable petition requires one of the following items: (1) Statement by one named inventor in the application that he/she is 65 years of age, or more; or (2) Certification by a registered attorney/agent having evidence such as a birth certificate, passport, driver's license, etc. showing one named inventor in the application is 65 years of age, or more.					
Name of inventor who is 65 years of age, or older					
Given Name	Middle Name	Family Name	Suffix		
Shih-Ping		WANG			
A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the format of the signature. Select (1) or (2): ☐ (1) I am an inventor in this application and I am 65 years of age, or more. ☒ (2) I am an attorney or agent registered to practice before the Patent and Trademark Office, and I certify that I am in possession of evidence, and will retain such in the application file record, showing that the inventor listed above is 65 years of age, or more.					
Signature	/Ivan S. Kavrukov/		Date (YYYY-MM-DD)	2025-01-28	
Name	Ivan S. Kavrukov		Registration Number	25,161	

This collection of information is required by 37 CFR 1.102(c)(1). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) a petition to make special based on age for advancement of examination. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETED FORMS TO THE CHIEF INFORMATION OFFICER. Submit completed forms electronically over EFS-Web, or mail to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

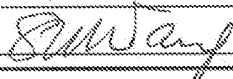
Privacy Act Statement

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES
<p>As the below named inventor, I hereby declare that:</p> <p>This declaration is directed to: ☐ The attached application, or ☒ United States application or PCT international application number <u>18/385,213</u> filed on <u>October 30, 2023</u></p> <p>The above-identified application was made or authorized to be made by me.</p> <p>I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.</p> <p>I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p>WARNING:</p> <p>Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.</p> <p>LEGAL NAME OF INVENTOR</p> <p>Inventor: <u>Shih-Ping Wang</u> Date (Optional): _____</p> <p>Signature: <u></u></p> <p>Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.</p>	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. This information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-0192 and select option 2.



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PATENT AND TRADEMARK OFFICE

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #
19/036,506

RECEIPT DATE / TIME
01/24/2025 01:35:09 PM Z ET

ATTORNEY DOCKET #
309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4276	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68899207	AUTHORIZED BY	Ivan Kavrukov
CUSTOMER #	139982	FILING DATE	-
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Shih-Yuan WANG

Payment Information

PAYMENT METHOD CARD / 2892	PAYMENT TRANSACTION ID E20251ND37055899	PAYMENT AUTHORIZED BY Mary Ellen Finnegan
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PRE-AUTHORIZED ACCOUNT 600125	PRE-AUTHORIZED CATEGORY 37 CFR 1.21 (Miscellaneous fees and charges)
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FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
4011	BASIC FILING FEE- UTILITY	70.00	1	70.00
2111	UTILITY PATENT APPL. SEARCH FEE	308.00	1	308.00
2311	EXAMINATION OF ORIGINAL PATENT APPLICATION	352.00	1	352.00
TOTAL AMOUNT:				\$730.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV 2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Yuan		WANG	
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service				
City	Palo Alto	State/Province	CA	Country of Residence US
Mailing Address of Inventor:				
Address 1	766 Encina Grande Drive			
Address 2				
City	Palo Alto	State/Province	CA	
Postal Code	94306	Country	US	
Inventor 2 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Ping		WANG	
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service				
City	Los Altos	State/Province	CA	Country of Residence US
Mailing Address of Inventor:				
Address 1	38 Third Street, Suite 307			
Address 2				
City	Los Altos	State/Province	CA	
Postal Code	90422	Country	US	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

☐ An Address is being provided for the correspondence information of this application.

Customer Number

Email Address

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Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		
Attorney Docket Number	309-0015USCIPDIV2	Small Entity Status Claimed	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	48	Suggested Figure for Publication (if any)	5B

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

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Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	139982		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Division of	18822880	2024-09-03

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0015USCIPDIV2	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18822880	Division of	18385213	2023-10-30	12087871	2024-09-10
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18385213	Continuation in part of	17974325	2022-10-26	11830954	2023-11-28
Prior Application Status		Pending		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
18385213	Continuation in part of	18113474	2023-02-23		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113747	Division of	17707429	2022-03-29	11621360	2023-04-04
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17707429	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-30	10446700	2019-10-15
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113474	Continuation in part of	17707429	2022-03-29	11621360	2023-04-04
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0015USCIPDIV2	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17707429	Division of	17532832	2021-11-22	11309444	2022-04-19
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17532832	Continuation in part of	17182954	2021-02-03	11791432	2023-10-17
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Continuation in part of	PCTUS1667977	2016-12-21		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16042535	2018-07-23	10700225	2020-06-30
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16296985	2019-03-08	10468543	2019-10-16
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113474	Division of	177077429	2022-03-29	11621360	2023-04-04
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
177077429	Division of	17532831	2021-11-22	11309444	2022-04-19
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17532831	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0015USCIPDIV2	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	14947718	2015-11-20	10622498	2020-03-25
Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958		Continuation in part of		PCTUS1667977	2016-12-21
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-20	10446700	2019-09-25
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16042535	2018-07-23	10700225	2020-06-30
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16296985	2019-03-08	10468543	2019-10-16
Prior Application Status		Abandoned		Remove	
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958		Continuation in part of		PCTUS1843289	2018-07-23
Prior Application Status		Abandoned		Remove	
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958		Continuation in part of		PCTUS1857963	2018-10-29
Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958		Claims benefit of provisional		62713455	2018-08-01
Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958		Claims benefit of provisional		62716310	2018-08-08

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62717750	2018-08-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62719689	2018-08-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62724449	2018-08-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62733476	2018-09-19

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2	Type text here
		Application Number		
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/737062	2018-09-26
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/750016	2018-10-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/770656	2018-09-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/772498	2018-09-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/777157	2018-12-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/779693	2018-12-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/784342	2018-12-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/794330	2019-01-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/797141	2019-01-25

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/797263	2019-01-26
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/800371	2019-02-01
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/802171	2019-02-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/802718	2019-02-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/805850	2019-02-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/808949	2019-02-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/819604	2019-03-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/819669	2019-03-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/820695	2019-03-19

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/828976	2019-04-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/841798	2019-05-01
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/843206	2019-05-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/846554	2019-05-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/853280	2019-05-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/860115	2019-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/863231	2019-06-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/863852	2019-06-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/867186	2019-06-26

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0015USCIPDIV2	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number Filing or 371(c) Date (YYYY-MM-DD)	
16/528958		Claims benefit of provisional		62/868911 2019-06-29	
Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number Filing or 371(c) Date (YYYY-MM-DD)	
16/528958		Claims benefit of provisional		62/870533 2019-07-03	
Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number Filing or 371(c) Date (YYYY-MM-DD)	
16/528958		Claims benefit of provisional		62/873891 2019-07-13	
Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number Filing or 371(c) Date (YYYY-MM-DD)	
16/528958		Claims benefit of provisional		62/874418 2019-07-15	
Prior Application Status		Patented		Remove	
Application Number		Continuity Type		Prior Application Number Filing Date (YYYY-MM-DD) Patent Number Issue Date (YYYY-MM-DD)	
PCT/US18/57963		Continuation of		15/797821 2017-10-30 10446700 2019-10-15	
Prior Application Status		Patented		Remove	
Application Number		Continuity Type		Prior Application Number Filing Date (YYYY-MM-DD) Patent Number Issue Date (YYYY-MM-DD)	
15/797821		Continuation in part of		14/947718 2015-11-20 10622498 2020-03-25	
Prior Application Status		Patented		Remove	
Application Number		Continuity Type		Prior Application Number Filing Date (YYYY-MM-DD) Patent Number Issue Date (YYYY-MM-DD)	
15/797821		Continuation in part of		15/309922 2016-11-09 9818893 2017-10-25	
Prior Application Status		Pending		Remove	
Application Number		Continuity Type		Prior Application Number Filing or 371(c) Date (YYYY-MM-DD)	
15/797821		Continuation in part of		PCT/US16/67977 2016-12-21	
Prior Application Status		Expired		Remove	
Application Number		Continuity Type		Prior Application Number Filing or 371(c) Date (YYYY-MM-DD)	
15/797821		Claims benefit of provisional		62/465734 2017-03-01	

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/474179	2017-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/484474	2017-04-12
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/487606	2017-04-20
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/488998	2017-04-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/500581	2017-05-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/505974	2017-05-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/509093	2017-05-20
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/510249	2017-05-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/514889	2017-06-04

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		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/521504	2017-06-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/522169	2017-06-20
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/527962	2017-06-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/530281	2017-07-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/533078	2017-07-16
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/533603	2017-07-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/542243	2017-08-07

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		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/547728	2017-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/542243	2017-08-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639472	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/628764	2018-02-09

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/643010	2018-03-14
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/640522	2018-03-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/599246	2017-12-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/645810	2018-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/666005	2018-05-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/607860	2017-12-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/631630	2018-02-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/677609	2018-05-29

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/634692	2018-02-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/652830	2018-04-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/591072	2017-09-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639356	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/615314	2018-01-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/623971	2018-01-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/637945	2018-03-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/651053	2018-03-30

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/682909	2018-06-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/659072	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/659067	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/669194	2018-05-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/675130	2018-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/547728	2017-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/651087	2018-03-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/646871	2018-03-22

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0015USCIP DIV2	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/662217	2018-04-24		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/639920	2018-03-07		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US18/43289	Claims benefit of provisional	62/633514	2018-02-21		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/296985	Continuation of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/042535	Continuation in part of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/535801	2017-07-21		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/540524	2017-08-02		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/542243	2017-08-07		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16/042535	Claims benefit of provisional	62/547728	2017-08-18		

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/591072	2017-11-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/599246	2017-12-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/607860	2017-12-19
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/615314	2018-01-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/623971	2018-01-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/628764	2018-02-09

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/631630	2018-02-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/633514	2018-02-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/634692	2018-02-23
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/637945	2018-03-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639356	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639472	2018-03-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639920	2018-03-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/640522	2018-03-08
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/643010	2018-03-14

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/645810	2018-03-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/646871	2018-03-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/651053	2018-03-30
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/651087	2018-03-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/652830	2018-04-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/659067	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/659072	2018-04-17
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/662217	2018-04-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/666005	2018-05-02

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/669194	2018-05-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/675130	2018-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/677609	2018-05-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/682909	2018-06-09
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/270577	2015-12-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/304907	2016-03-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/290391	2016-02-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/334934	2016-05-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/338263	2016-05-18

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Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/346850	2016-06-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/359349	2017-07-07
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/366188	2016-07-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/368109	2016-07-28
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/374828	2016-08-13
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/376869	2016-08-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/380364	2016-08-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/383391	2016-09-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/383479	2016-09-04

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		309-0015USCIP DIV2	
		Application Number			
Title of Invention		MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES			

Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/394222	2016-09-14		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/398607	2016-09-23		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/401126	2016-09-28		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/406999	2016-10-12		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/414671	2016-10-29		
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
PCT/US16/67977	Claims benefit of provisional	62/415339	2016-10-31		
Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
15/309922	a 371 of international	PCT/US15/61120	2015-11-17		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/309922	Continuation of	14/943898	2015-11-17	9530905	2016-12-27
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/309922	Continuation of	14/945003	2015-11-18	9525084	2016-12-20

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/213558	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/199607	2015-07-13
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/175855	2015-06-15

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/090879	2014-12-11

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/182602	2015-06-21

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/100025	2015-01-05

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/188876	2015-07-06

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/111582	2015-02-03

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USC:IPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/947718	Continuation of	PCT/US14/39208	2014-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/826446	2013-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/843021	2013-07-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/905109	2013-11-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/834873	2013-06-13
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/892821	a 371 of international	PCT/US14/39208	2014-05-22

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/826446	2013-05-22
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/843021	2013-07-04
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/905109	2013-11-15
Prior Application Status	Expired	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/834873	2013-06-13
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

☐	This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2 <small>text here</small>
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h) (1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIP DIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1			
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
<input type="button" value="Clear"/>			
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor: <input type="text"/>			
If the Applicant is an Organization check here. ☒			
Organization Name	W&W Sens Devices, Inc.		
Mailing Address Information For Applicant:			
Address 1	38 Third Street, Suite 307		
Address 2			
City	Los Altos	State/Province	CA
Country	US	Postal Code	94022
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country i		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the **INITIAL** filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Ivan S. Kavrukov/		Date (YYYY-MM-DD)	2025-01-24
First Name	Ivan S.	Last Name	Kavrukov	Registration Number 25,161
Additional Signature may be generated within this form by selecting the Add button.				

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	309-0015USCIPDIV2
		Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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APPLICATION #
19/036,506

RECEIPT DATE / TIME
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ATTORNEY DOCKET #
309-0015USCIPDIV2

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4276	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68899207	FILING DATE	-
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 8

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIP_Declaration_Shih-YuanWANG-signed.pdf	2	Oath or Declaration filed	176 KB
309-0015USCIP_Declaration_ShihPingWANG-signed.pdf	1	Oath or Declaration filed	361 KB
309-0015USCIPDIV2_Transmittal OfPowerOfAttorney-Signed.pdf	2	Power of Attorney	649 KB
309-0015USCIPDIV2_Preliminary Amendment-Final.pdf	13	Preliminary Amendment	523 KB
309-	87	Application body structured	148 KB

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on---Final-APP.TEXT.docx

text document

Warning: The document submitted appears to have portions not written in English language. Please review and revise. Bookmarks were found and have been removed. Unable to create PDF for one or more sections. PDF creation skipped and will automatically be retried.

309- 0015USCIP2_Figures_FINAL .pdf	48	Drawings-only black and white line drawings	18638 KB
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309- 0015USCIPDIV2_Application DataSheet__Final.pdf	38	Application Data Sheet	17786 KB
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309- 0015USCIPDIV2_Specificati on---Final.pdf	87	Auxiliary PDF of Application	449 KB
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Digest

DOCUMENT

MESSAGE DIGEST(SHA-512)

309- 0015USCIP_Declaration_Shih- YuanWANG-signed.pdf	085C4DC41556D38647787EC03BE6B1C018335A4BDA768E18E 5FCDD442C0B97B8239C88CA88FABFDCF70AF1B872AC94354 DB30B660BA08E30BDAF9AB254CDF4E2
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309- 0015USCIPDIV2_PreliminaryA mendment-Final.pdf	62604C99C9A85670019A7132C5D8CF00E01D324829F94FCD0 325EDE04217B1DB2AC8F34E69807F137C26C3656E197320F8 DFAC93B266D8F3693F24F80E989772
309- 0015USCIPDIV2_Specification- --Final-APP.TEXT.docx	7DBDD82121C82237501F0506643B6C6CD12B7E60F99F3F99A A226ECE0FB0D178053104BDF34DC5DF0CBE6EFE9E4B5C355 11064AB47A7795401895EBB93905875
309- 0015USCIP2_Figures_FINAL.p df	41C7FA7AA0BC8CC98C4F20BC542C181A15163D1BCD0E9DF 6EDCBE7C37E31FF131777DA01E0EB413751CEB8622A621C7 0AF7E0F9868DBD341A41E166F52B9E4FB

309-0015USCIPDIV2_ApplicationDataSheet_Final.pdf	74B69B63FB87266CC60404B192422D14A9C0D245D28A8EA08 B4F73A952E451BB7EF932D59107081112D5E3D9D9E29F5379 3DB08456292FF58D6ECABA6047847C
309-0015USCIPDIV2_Specification--Final.pdf	CD1EE2A367BD86177552F5AA41FED4E01AC112B17FC19D04 8E851FD0370D26DDAC9F4693B4FD07A672353AED9D99B44E 7C8FB219EB04C1E5022335513F53FC9D

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
<p>As the below named inventor, I hereby declare that:</p> <p>This declaration is directed to: ☐ The attached application, or ☒ United States application or PCT international application number <u>18/385,213</u> filed on <u>October 30, 2023</u>.</p> <p>The above-identified application was made or authorized to be made by me.</p> <p>I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.</p> <p>I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.</p> <p style="text-align: center;">WARNING:</p> <p>Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.</p>	
<p>LEGAL NAME OF INVENTOR</p> <p>Inventor: <u>Shih-Yuan Wang</u> Date (Optional) : _____</p> <p>Signature: <u><i>Shih-Yuan Wang</i></u></p>	
<p>Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.</p>	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Application Number	TBD
Filing Date	TBD
First Named Inventor	Shih-Yuan WANG
Title	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	309-0015USCIPDIV2

SIGNATURE of Applicant or Patent Practitioner			
Signature	/Ivan S. Kavrukov/	Date (Optional)	
Name	Ivan S. Kavrukov	Registration Number	25,161
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			
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PTO/AIA/82B (07-13)

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I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

139982

OR



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Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:



The address associated with the above-mentioned Customer Number

OR



The address associated with Customer Number:

OR



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Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

W&WSens Devices, Inc.



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Title

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of

forms are submitted.

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MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

REFERENCE TO RELATED APPLICATIONS

- 5 **[0001]** This patent application is a continuation in-part of each of U.S. Application 18/113,474 and 17/974,325.
- [0002]** 18/113,474 is a division of 17/707,429, now Pat 11,621,360.
- [0003]** 17/707,429 is a continuation in-part of 17/182,954, now Pat. 11,791,432.
- [0004]** 17/182,954 is a division of 16/528,958, now Pat. 11,121,271, which
- 10 claims priority to U.S. Provisional Patent.
- [0005]** 16/528,958 is a continuation in-part of 15/797,821, now Pat. 10,446,700
- [0006]** 16/528,958 claims priority to U.S. Provisional Pat. Applns. 62/713,455, 62/716,310, 62/717,750, 62/719,689, 62/724,449, 62/733,476, 62/737,062, 62/750,016, 62/770,656, 62/772,498, 62/777,157, 62/779,693, 62/784,342,
- 15 62/794,330, 62/797,141, 62/797,263, 62/800,371, 62/802,171, 62/802,718, 62/805,850, 62/808,949, 62/819,604, 62/819,669, 62/820,695, 62/828,976, 62/841,798, 62/843,206, 62/846,554, 62/853,280, 62/860,115, 62/863,231, 62/863,852, 62/867,186, 62/868,911, 62/870,533, 62/873,891, 62/874,418
- [0007]** 15/797,821 is a continuation in-part of 14/947,718, now Pat. 10,622,498.
- 20 **[0008]** 14/947,718 is a continuation of Int'l Pat. Appln. PCT/US14/39208.
- [0009]** PCT/US14/39208 claim priority to:
- [0010]** U.S. Prov. Ser. No. 61/826,446 filed May 22, 2013;
- [0011]** U.S. Prov. Ser. No. 61/834,873 filed June 13, 2013;
- [0012]** U.S. Prov. Ser. No. 61/843,021 filed July 4, 2013; and
- 25 **[0013]** U.S. Prov. Ser. No. 61/905,109 filed November 15, 2013.
- [0014]** 17/974,325 is a continuation in-part of said 17/182,954.
- [0015]** The chain of parents and siblings of this patent application includes U.S., International, and provisional patent applications that are in addition to those listed above but are identified in the ADS filed concurrently herewith.
- 30 **[0016]** This patent application incorporates by reference the subject matter of each of the patent applications listed above as well as of each of the additional U.S., International, and provisional patent applications listed in the concurrently filed ADS.

[0017] The above-referenced provisional patent applications are collectively referenced herein as “the commonly assigned incorporated applications.”

5

FIELD

[0018] The present invention generally relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.

10

BACKGROUND

[0019] Fiber-optic communication is widely used in applications such as telecommunications and communication within large data centers. Because of attenuation losses associated with using shorter optical wavelengths most fiber-optic communication uses optical wavelengths of 800 nm and longer. Commonly used transmission windows exist between 1260 nm and 1675 nm. A main component of optical receivers used in fiber-optic communication system is the photo detector, usually in the form of a photodiode (PD) or avalanche photodiode (APD).

[0020] High-quality low-noise APDs can be made from silicon. However, while silicon will absorb light in the visible and near infrared range, it becomes more transparent at longer optical wavelengths. Silicon PDs and APDs can be made for optical wavelengths of 800 nm and longer by increasing the thickness of the absorption “I” region of the device. FIG. 2 is a cross section of a conventional PIN photodiode 200, where “d” is the length of the absorption “I” region 220. FIGs. 3A and 3B show bandwidth and quantum efficiency a conventional silicon photodiode with a 30-micron diameter at 850 nm optical wavelength. As can be seen, in order to obtain a quantum efficiency of 90% the thickness “d” of the “I” region is over 30 microns. This leads to a maximum bandwidth of less than 2.5 Gb/s, which is too low for many current and future telecom and data center applications.

[0021] To avoid the inherent problem that silicon PDs and APDs have with longer wavelengths and higher bandwidths, other materials are used. Germanium (Ge) detects infrared out to a wavelength of 1700 nm, but has relatively high multiplication noise. InGaAs can detect out to longer than 1600 nm, and has less

multiplication noise than Ge but still has far greater noise than silicon. InGaAs is known to be used as the absorption region of a heterostructure diode, most typically involving InP as a substrate and as a multiplication layer. This material system is compatible with an absorption window of roughly 900 to 1700 nm.

5 However both InGaAs and Ge devices are relatively expensive and have relatively high multiplication noise when compared with silicon.

[0022] The subject matter claimed herein is not limited to embodiments that solve any specific disadvantages or that operate only in environments such as those described above. Rather, this background is only provided to illustrate one
10 exemplary technology area where some embodiments described herein may be practiced.

SUMMARY

[0023] According to some embodiments, a photodetector with microstructure-
15 enhanced photoabsorption is described. The photodetector (e.g. photodiode or avalanche photodiode) includes: a cathode region; an anode region; reverse biasing circuitry configured to apply a voltage between the cathode and anode regions such that the cathode region is driven to a more positive voltage than the anode region; and a microstructure-enhanced photon absorbing semiconductor
20 region configured to absorb photons from a source signal. The absorbing region includes a plurality of microstructures that are dimensioned and positioned to increase absorption of photons at a range of wavelengths that includes a wavelength of the source signal. According to some embodiments the microstructures have at least one dimension that is equal to or shorter than a
25 longest signal wavelength. According to some embodiments the microstructures are pillars, holes and/or voids. The microstructures can be arranged into a periodically-spaced array, a non-periodically-spaced array, a randomly-spaced array or a multiperiodically-spaced array. According to some embodiments the microstructures have a major longitudinal axis that is normal to the upper surface of
30 the underlying substrate material. According to some other embodiments, the microstructures have major longitudinal axes that are not parallel to one another. According to some embodiments, the microstructures are oriented so as to reduce sensitivity to any single direction of the source signal.

[0024] According to some embodiments, the microstructures increase absorption at least in part by forming an absorbing mode high contrast grating that makes use of resonance effects, scattering effects, near field effects, sub-wavelength effects, and/or interference effects.

5 **[0025]** According to some embodiments, the absorbing region and the microstructures are formed of silicon. According to some embodiments, a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 5 gigabits per second, at wavelengths of 850 nanometers with a quantum efficiency of at least 60%. According to some embodiments, a silicon
10 photodiode is provided that can detect source signals at a data bandwidth of greater than 10 gigabits per second, at signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%. According to some embodiments a silicon avalanche photodiode is provided that can detect source signals at a data bandwidth of greater than 5 gigabits per second, at wavelengths of 850
15 nanometers, while having a gain of greater than 2. According to some embodiments a silicon APD has a multiplication region with microstructures that extend into the P multiplication layer, N multiplication layer and/or charge layer. According to some embodiments a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 1 gigabit per second, at
20 wavelengths of 980 nanometers with a quantum efficiency of at least 40%. According to some embodiments a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 0.5 gigabits per second, at wavelengths of 1000 nanometers with a quantum efficiency of at least 30%. According to some embodiments, the microstructures effectively reduce
25 capacitance of the photodetector when compared to a microstructure-free device having a similar photon absorbing length.

[0026] According to some embodiments, the absorbing semiconductor region and the microstructures are formed of silicon and germanium. According to some embodiments, the microstructures are formed by etching away portions of silicon
30 and using a selective area growth process to grow germanium in the etched away portions. According to some embodiments, the absorbing semiconductor region and the microstructures are formed of germanium. According to some embodiments, the photo detector is configured to receive the source signal from

the substrate-side. The anode region can include a germanium P layer formed by an epitaxial lateral overgrowth process. The device can be configured such that the source signal to passes through the absorbing region a first time, reflects from a surface and thereafter passes through the absorbing region a second time. The
5 device can also be configured to receive the source signal the top-side and the anode region can be made of a silicon P layer. According to some embodiments, a avalanche photodiode is provided that detects source signals at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 1750 nanometers or shorter, and having a gain of greater than 2. According to some
10 embodiments, the absorbing semiconductor region and the microstructures are formed of III-V family material(s) such as InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, AlGaAs, AlGaN, GaP, InSb or InAs.

[0027] According to some embodiments, the microstructures include voids buried within the absorbing semiconductor region. According to some
15 embodiments, voids are buried in a layer of material so as to effectively lower the refractive index at the signal wavelength(s) and as well as lower the capacitance of the layer of material.

[0028] According to some embodiments, a photovoltaic device is described that includes a semiconductor material having a plurality of voids buried therein. The
20 semiconductor material being configured to convert solar radiation into direct current electricity. According to some embodiments, the voids are microstructured voids and are configured to enhance absorption of the semiconductor material thereby increasing conversion efficiency of the device. According to some embodiments, the voids are sized and/or spaced apart by less than 3 microns, and
25 are configured to alter an effective refractive index of the semiconductor material near a surface, for example to reduce reflection of incident sunlight from the device and/or increase internal reflections within the semiconductor material.

[0029] According to some embodiments a glass material is described in which the glass has a plurality of buried voids dimensioned between 0.01 microns to
30 1000 microns. In some examples the glass forms a part of a photovoltaic device. According to some embodiments, the buried voids are filled with a material gel, polymer and gas. The buried voids can provide flexibility of the glass material,

and/or increased resistance of the glass material to physical damage and/or damage propagation.

[0030] According to some embodiments, a microwave transmission line structure is described that includes: a semiconductor substrate material having a plurality of high-density dielectric-filled voids configured to reduce a dielectric constant of the semiconductor substrate material; and a plurality of metallic microwave transmission lines, least one of which is positioned above the semiconductor substrate material. According to some embodiments, the dielectric-filled voids are filled a material such as: nitrogen, argon, vacuum, air, helium, polymer, metal oxides, silicon dioxide, silicon nitride, calcium fluoride, or zinc oxide. According to some embodiments, the voids are further configured to reduce dispersion and reduce loss associated with the microwave transmission lines at least in part by reducing current loop flow and/or eddy currents.

[0031] According to some embodiments, an optical waveguide structure is described that includes: an optical mode region; and a supporting semiconductor material adjacent to the optical mode region. The supporting material includes a plurality of microstructured voids that are configured to alter an effective index of refraction of the supporting material based on the size, shape, density, etc. of the microstructured voids.

[0032] According to some embodiments, a heat exchanger system is described that includes: a heat generating device; a heat sink configured to dissipate heat to a surrounding medium; and an intermediate material mounted between the heat generating device and the heat sink. The intermediate material includes a plurality of buried voids configured to effect thermal conductivity of the intermediate material. According to some embodiments, some of the buried voids are filled with thermally conductive material and others are filled with a thermally isolating material. The two types of voids being positioned to conduct heat from the heat generating device to the heat sink and to reduce thermal cross talk with other heat sensitive devices mounted on the intermediate material.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0033] To further clarify the above and other advantages and features of the subject matter of this patent specification, specific examples of embodiments

thereof are illustrated in the appended drawings. It should be appreciated that these drawings depict only illustrative embodiments and are therefore not to be considered limiting of the scope of this patent specification or the appended claims. The subject matter hereof will be described and explained with additional specificity

5 and detail through the use of the accompanying drawings in which:

[0034] FIG. 1 is schematic side cross section of three dimensional micro structures that enhance bulk absorption coefficient in photo sensitive devices, according to some embodiments;

[0035] FIG. 2 is a cross section diagram showing aspects of a typical structure
10 of a conventional PIN photodiode;

[0036] FIGs. 3A and 3B are plots showing bandwidth and quantum efficiency (QE), respectively, of a bulk conventional silicon photodiode versus "d" in microns;

[0037] FIGs. 4A-4D are graphs showing the enhancement of bulk absorption coefficient vs bandwidth and QE for a microstructured Si photodetector, according
15 to some embodiments;

[0038] FIGs. 5A and 5B are cross sections showing aspects of a top illuminated microstructured PIN silicon photodiode, according to some embodiments;

[0039] FIGs. 6A and 6B are cross sections showing aspects of a bottom
20 illuminated microstructured NIP silicon photodiode, according to some embodiments;

[0040] FIGs. 7A and 7B are cross sections showing aspects of a microstructured avalanche photodiode, according to some embodiments;

[0041] FIG. 8 is a cross section showing a silicon epitaxial structure for a high-
25 speed high-efficiency microstructured APD, according to some embodiments;

[0042] FIGs. 9A-9E are a series of cross sections showing some basic microstructure processing steps, for a high-speed APD, according to some embodiments;

[0043] FIGs. 10A-10B are cross sections showing aspects of a top illuminated
30 microstructured photo diodes, avalanche photo diodes and/or photovoltaics (PV) with microstructured voids in N-Si, according to some embodiments;

[0044] FIGs. 11A and 11B are cross sections showing aspects of an heteroepitaxial APD structure of Ge on Si, according to some embodiments;

[0045] FIG. 12 is a cross section illustrating aspects of a passivation method for Ge surfaces on microstructures, according to some embodiments;

[0046] FIGs. 13A and 13B are graphs showing the effects of microstructure enhancement of Ge bulk absorption coefficient for photodiodes and/or avalanche
5 photodiodes based on Ge on Si, according to some embodiments;

[0047] FIGs. 14A-14B are cross sections showing aspects of a top-illuminated Ge on Si avalanche photodiode having microstructured pillars/holes, according to some embodiments;

[0048] FIGs. 15A-15D are cross sections illustrating aspects of bottom-
10 illuminated Ge on Si avalanche photodiodes having microstructured pillars/holes, according to some embodiments;

[0049] FIGs. 16A and 16B are graphs comparing single pass and double pass photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments;

15 **[0050]** FIGs. 17A-17B are cross sections showing aspects of a top-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 700 to 1800 nm, according to some embodiments;

[0051] FIGs. 18A-18B are cross sections showing aspects of a bottom-
20 illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 1200 to 1800 nm, according to some embodiments;

[0052] FIGs. 19A-19C are diagrams illustrating how microstructures can reduce capacitance of a photodiode such that a larger area photo diode can be fabricated
25 with the same bandwidth and QE, according to some embodiments;

[0053] FIGs. 19D-19E are cross sections showing aspects of fabricating an APD device having a III-V absorbing layer grown on a P-I-N silicon multiplication layer, according to some embodiments;

[0054] FIG. 20 shows bulk layers without a final P-Si layer for devices having
30 microstructured Ge buried or embedded in an Si microstructure, according to some embodiments;

[0055] FIG. 21 is a cross section showing etching of microstructured pillars and/or holes for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments;

[0056] FIG. 22 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after the Ge "I" layer is grown in the etched region and planarized, according to some embodiments;

[0057] FIG. 23 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after I-Ge regrowth and planarization, and a cap layer of P-Si, according to some embodiments;

[0058] FIGs. 24A - 24B are cross sections showing aspects of a microstructured APD with buried/embedded I-Ge absorbing microstructures in I-Si microstructures, according to some embodiments;

[0059] FIGs. 25A - 25C are cross sections showing aspects of a photodiode having buried/embedded Ge microstructures in a Si microstructured pillar and/or hole array, according to some embodiments;

[0060] FIGs. 25D - 25E are cross sections showing aspects of a forward biased device such as a vertical cavity surface emitting laser (VCSEL), according to some embodiments;

[0061] FIG. 26 is a cross section showing starting epitaxial layers in which microstructured voids are fabricated, according to some embodiments;

[0062] FIG. 27 is a cross section showing microstructured holes/pillars etched into the I-Si layer, according to some embodiments;

[0063] FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping P⁺ anode layer 2826, according to some embodiments;

[0064] FIG. 29 is a cross section showing Bragg reflectors formed on the P-Si surface to provide a highly reflective mirror, according to some embodiments;

[0065] FIG. 30 shows an example of a PIN PD/PV structure with microstructured voids to enhance absorption, reduce bulk refractive index, reduce capacitance and increase mechanical flexibility of large sheets of PV on semiconductor material, according to some embodiments;

[0066] Fig. 31 is a cross section showing regrown I-Ge with a buried/embedded voids, according to some embodiments;

[0067] Fig. 32 is a cross section showing a device having buried microstructured voids in I-Si with regrown I-Ge and capped by an epitaxial layer, according to some embodiments;

[0068] FIG. 33 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some embodiments;

[0069] FIG. 34 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some other embodiments;

[0070] Fig. 35 shows the basic epitaxial structure for a conventional Si PV/PD diode on N Si substrate;

[0071] FIG. 36 shows microstructured voids incorporated into an N-Si layer, according to some embodiments;

[0072] FIG. 37 is a cross section showing etched Si microstructured pillars/holes with regrown Ge covering the Si, according to some embodiments;

[0073] FIG. 38 is a cross section showing microstructured Si pillars/holes with Ge regrowth on an N-Si layer having embedded microstructured voids, according to some embodiments;

[0074] FIG. 39 is a cross section showing partial coverage I-Ge on microstructured Si pillars/holes, according to some embodiments;

[0075] FIG. 40 is a cross section showing the basic components for the a microstructured Si-Ge pillar hole array PD/PV and/or APD, according to some embodiments;

[0076] FIGs. 41A-41B are cross sections showing aspects of a microstructured pillar/hole array device above a N-Si layer having buried microstructured voids, according to some embodiments;

[0077] FIGs. 42A-42D are cross sections showing aspects of an APD with microstructured pillar/hole arrays above an N-Si layer having buried microstructured voids, according to some embodiments;

[0078] FIGs. 43-46 are top views illustrating various dimensions, spacings and shapes for microstructured elements, according to some embodiments;

[0079] FIGs. 47-48 are cross sections showing microstructured pillar and hole arrays having varying lengths and depths, according to some embodiments;

[0080] FIG. 49 shows a microstructured surface having a combination of both pillars and holes, according to some embodiments;

[0081] FIG. 50 is a cross section of an optical ridge waveguide, according to some embodiments;

[0082] FIG. 51 is a cross section of a buried optical waveguide in silicon using voids, according to some embodiments;

5 **[0083]** FIGs. 52 and 53 are a cross section and top view, respectively, of a ridge waveguide integrated with a microstructured PD/APD, according to some embodiments;

[0084] FIGs. 54A and 54B show a microwave transmission line on Si with voids, according to some embodiments;

10 **[0085]** FIG. 55 is a cross section of voids for thermal conduction and thermal isolation of heat producing ICs and light emitters, according to some embodiments; and

[0086] FIG. 56 is a cross section showing a distribution of voids to increase lateral path length for increasing lateral electrical resistivity and decrease lateral

15 thermal conduction, according to some embodiments;

[0087] FIGs. 57A and 57B are simplified partial schematic top views of a semiconductor surface having holes configured as trenches, according to some embodiments.

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DETAILED DESCRIPTION

[0088] A detailed description of examples of preferred embodiments is provided below. While several embodiments are described, it should be understood that the new subject matter described in this patent specification is not
25 limited to any one embodiment or combination of embodiments described herein, but instead encompasses numerous alternatives, modifications, and equivalents. In addition, while numerous specific details are set forth in the following description in order to provide a thorough understanding, some embodiments can be practiced without some or all of these details. Moreover, for the purpose of clarity, certain
30 technical material that is known in the related art has not been described in detail in order to avoid unnecessarily obscuring the new subject matter described herein. It should be clear that individual features of one or several of the specific embodiments described herein can be used in combination with features or other

described embodiments. Further, like reference numbers and designations in the various drawings indicate like elements.

[0089] According to some embodiments, microstructures are used to enhance the bulk absorption constant (also referred to as absorption coefficient) to achieve high quantum efficiency (QE) while maintaining an absorption length suitable for high data rate applications. As used herein, "QE" refers to internal quantum efficiency (IQE). IQE is equal to external quantum efficiency (EQE) in cases where reflection and transmission are negligible.

[0090] According to some embodiments, microstructures are used to improve bulk absorption constant at wavelengths in the proximity of the semiconductor material's band gap. This allows for extending the operating optical wavelengths and/or operating spectrum of the photosensor. The enhanced bulk absorption constant (or coefficient) is called the effective absorption constant (or coefficient). The term "effective" is used since absorption constant or coefficient is an inherent material property. However, with resonance effects, plasmonic effects, field enhancement effects, scattering effects, near field and sub wavelength effects, the effective absorption constant or coefficient can be greater than the bulk or material absorption constant or coefficient. As used herein, the following terms are used interchangeably: enhanced absorption constant, enhanced absorption coefficient; enhanced effective absorption constant; enhanced effective absorption coefficient; enhanced absorption; enhanced effective absorption; and effective absorption constant; and effective absorption coefficient.

[0091] According to some embodiments, enhanced absorption can also have drastic effects on path length. In one bulk absorption example, the path length for the photons to be absorbed to 1/e of its original amplitude is, for example 100 micrometers (μm), whereas under enhanced absorption according to some embodiments, the path length is 1 micrometer for the optical amplitude to decay to 1/e of its original amplitude. Equivalently, if path length is kept constant to one micrometer then the enhanced absorption coefficient is 100 times greater than the bulk absorption coefficient.

[0092] This is seen by the relationship $A = A_0 e^{-\alpha L}$ where A is the decaying amplitude of the incident photon flux A_0 and α is the absorption coefficient and L the path length for absorption to take place. So, rather than have L be 100 times

longer, an effective α can be defined such that it is 100 times greater than a non enhanced absorption coefficient such as the bulk absorption coefficient. The resonance/scattering/near field effects of microstructures for example gives the equivalence of the path length that is 100 times longer where the

5 resonant/scattering/near field microstructure is just one micron long. To put it another way, in a very simplistic view, the photons in the resonant structures make 50 round trips before reaching the $1/e$ value of its original amplitude, so the equivalent linear length is 100 times the length of the resonant structure. For simplicity, resonance/scattering/near field effects will collectively be referred to
10 herein as "resonant" which can include, resonant, scattering, near field, plasmonic, nonlinear and linear optical effects.

[0093] As used herein the terms "microstructures" and "microstructured" refer to: pillars, voids, holes and mesas, of various shapes and sizes having at least one dimension in the micrometer scale, submicrometer scale, and/or sub-wavelength
15 scale.

[0094] According to some embodiments, properties of the microstructures can also be explained as the absorption mode of high contrast grating (HCG) being used to enhance the effective absorption constant/coefficient or enhanced absorption. Conventionally, HCG uses material that is transparent at the optical
20 wavelength of interest. In contrast, according to some embodiments, at least one of the microstructures is absorbing or weakly absorbing at the optical wavelength of interest. According to some embodiments a low-Q absorbing mode HCG enhances absorption (e.g. Q values in the range of 2-200).

[0095] According to some embodiments, a low index material is used such as
25 buried oxide (BOX), silicon on insulator (SOI), silicon on sapphire (SOS), low-density semiconductors such as amorphous semiconductor, nanowire semiconductors, voids and holes to lower the effective refractive index. Refractive index is an inherent property of a material. However, according to some embodiments, when structures such as voids, air gaps, and/or holes (which can be
30 filled with low index material, and/or regrowth) have dimensions on the order of the optical wavelength, the optical electromagnetic field will see an average refractive index consisting of the material refractive index and the structures (which can be filled by a low refractive index material). This average is referred to herein as the

effective refractive index. According to some embodiments, a low index or effective low index material need not be used in the microstructures.

[0096] According to some embodiments, the techniques for enhancing effective absorption can be applied to various materials including: silicon, germanium, III-V material such as InP, GaAs, GaN, InGaAs, and any combination of the III-V material family. As used herein, the term "material family" of a III-V material is defined as any material that is lattice matched or approximately lattice matched (within a few percent) to GaAs, InP, GaN, InSb semiconductors. For example, the InP material family can include InGaAs, InGaAsP, InAlAs. According to some embodiments, in the case of microstructures, regrowth such as selective area growth (SAG) of Ge, InGaAs, or other III-V material in silicon microstructures can be carried out without the detrimental effects of lattice mismatch since the dimension of the footprint of the lattice mismatched material on silicon is small (approximately a few micrometers to sub-micrometers). This allows Ge and other III-V materials to be integrated with silicon without the use of a conventional buffer layer (such as amorphous Ge in the case of Ge on Si growth). The heterogeneous integration of materials can be homo or hetero structures, combination of crystalline and microcrystalline and amorphous semiconductor, conductor such as carbon, graphene, insulator, dielectrics, solid, gaseous, liquid such as glass or polymer that can be semiconducting.

[0097] Due to the microstructures, the capacitance can also be represented by an effective capacitance which is a parallel capacitance of (1) the dielectric constant of one semiconductor, and (2) the dielectric constant of another material, which can be a semiconductor, dielectric, gas, vacuum, partial vacuum, liquid such as glass or polymer (polyimide, mylar, or other organic compound). The effective capacitance of the device is the combination of the capacitance of the parallel capacitors, which can be two or more. An advantage of the use of microstructure according to some embodiments, is that the effective capacitance can be significantly lower than the capacitance of a homogeneous material such as a semiconductor. The lower capacitance allows a device to have a larger area while still maintaining suitably high data rate bandwidth, and/or increase the data rate bandwidth by reducing the thickness of the device to reduce the transit time.

[0098] According to some embodiments, the photosensor can be a photodiode (PD), avalanche photodiode (APD), photovoltaic (PV) or solar cell, or any optoelectronic device that converts photons to electrons. According to some
5 electrons/holes to photons can also be implemented using microstructures.

[0099] According to some embodiments, the enhanced absorption allows the APD/PD to: (1) extend the sensitivity of the APD/PD to photons with energies (or wavelength) closer to the material band gap with QE greater than 60% and data
10 Gb/s), due to shorter absorption length therefore shorter transit time; (3) increase quantum efficiency with enhanced absorption; (4) be manufactured of silicon which has superior APD properties with low excess noise; (5) be compatible with Si Photonics and CMOS processes. According to some embodiments, the PD/APD
15 processing, signal amplification, memory, cpu, electrical transmitter, optical waveguides, integrated optics, and other ICs for specific applications. This is advantageous for mass production using CMOS foundries.

[00100] According to some embodiments, microstructures such as voids are used to reduce effective refractive index to create resonant structures to enhance
20 the absorption. In microstructures where selective area growth are used to integrate Ge or III-V material with silicon, voids can be made in the silicon microstructure such that the absorbing region is a resonant structure to enhance the effective absorption coefficient by 2 to over 100 times.

[00101] According to some embodiments, silicon is used for avalanche gain.
25 Silicon has the lowest excess noise for an avalanche photodiode. By integrating Ge and/or III-V material with silicon, the absorption takes place in Ge and/or III-V material and the electronic gain occurs in silicon. Depending on the optical wavelengths, for example shorter than 1100 nm, silicon may be used for both absorption and electronic gain with the use of microstructures.

30 **[00102]** According to some embodiments, microstructures such as buried voids can reduce lateral electrical and thermal conductivity. In situations where directional conductivity of electrical or thermal (phonons) is preferred, voids can be used to confine the flow of electrical current and/or heat.

[00103] According to some embodiments, the absorption of photons in semiconductors is enhanced with the use of microstructures. The microstructures can have effects such as resonance, field enhancement, near field and sub wavelength effects, scattering, plasmonics, photonic crystal, absorption mode in
5 high contrast grating at the near field regime, which are both linear and non linear effects that can effectively increase the effective absorption length resulting in a greater absorption of the photons for a given length.

[00104] According to some embodiments, microstructures used for absorption enhancement for silicon photodiodes and silicon avalanche photodiodes can result
10 in silicon PD and APD with bandwidths in excess of 10 Gb/s (or equivalently 6.75 GHz approximately depending of the digital coding format) at photons with wavelengths of 850 nm approximately (which is the current datacom preferred wavelength) with quantum efficiencies of approximately 90% or more.

[00105] Silicon optical detectors are very robust due to the maturity of the
15 material and processing techniques, the surfaces can be easily passivated to eliminate dangling bonds that can cause surface states and carrier recombination centers, they have excellent carrier lifetimes due to low defects and high material purity, and for APD applications, the noise is low due to the small ionization ratio between holes and electrons (k factor, silicon have the lowest k factor than any III-
20 V material) and such detectors are CMOS compatible for integration with electronics for signal processing and with Si photonics.

[00106] According to some embodiments, other material such as germanium, III-V, a-Si (amorphous silicon) may also be used singly or together with other materials such that a multiple bandgap in parallel can be fabricated with enhanced
25 absorption.

[00107] According to some embodiments, microstructures and voids are used to reduce the effective refractive index and capacitance to achieve the absorption mode high contrast grating effect and to reduce the effective capacitance of the device for lower RC time constants.

30 **[00108]** In addition, according to some embodiments, microstructures buried in the semiconductor can reduce lateral electrical and thermal conduction. Microwave transmission lines are possible for example where high-density voids are buried in Si to reduce the dielectric constant and also eddy currents in the semiconductor

resulting in low loss and dispersion. Voids can also be used for thermal isolation and to improve thermal conductivity by filling the voids with thermal conductors. This is useful in thermal management of components on a silicon substrate.

[00109] The enhancement using nanowires (Garnett et al, Light trapping in
5 silicon nanowire solar cells, Nano Letters, 2010, 10, 1082-1087; Kelzenberg et al, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, Nature Materials, vol. 9, March 2010, 239-244) and nanoholes (Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Proceeding of SPIE, Vol. 7772, 77721G-1, 2010) have
10 been reported. Nanowire is known to be used for light trapping in photovoltaic applications where the photogenerated carriers diffuse to the anode or cathode of a P-N junction with zero external bias operating at DC (direct current).

[00110] According to some embodiments, the photogenerated carriers are swept out with an external reverse bias in the absorbing "i" region of a P-I-N diode (PD) or
15 P-I-P-I-N diode (APD) for high modulation bandwidth (greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain, with gain greater than 3 dB.

[00111] The cause or causes of the enhancement of the absorption coefficient are believed to include one or more of the following: an increase in optical field
20 concentration, resonance effects, constructive and destructive optical interferences (amplitude and phase) effects, scattering, and high contrast grating (HCG) effects. See, e.g. Chang-Hasnain et al, High contrast gratings for integrated optoelectronics, Advances in Optics and Photonics 4, 379-440 (2012), hereinafter "Chang-Hasnain." The HCG effects are at the near-wavelength regime (See,
25 Chang-Hasnain) where the optical wavelength in the material of the grating and the optical wavelength in the surrounding material of the grating is the range of the period of the grating.

[00112] FIG. 1 is schematic side cross section of three dimensional micro structures that enhance bulk absorption coefficient in photo sensitive devices,
30 according to some embodiments. Microstructured pillars 110 and/or holes 120 are etched into the "I" Si layer 100. The optical wavelength in material M_1 is λ/n_1 where n_1 is the refractive index of M_1 and the optical wavelength in material M_2 is given by λ/n_2 where n_2 is the refractive index of material M_2 . The center to center distance L

of the structures 110 can be between λ/n_1 and λ/n_2 or approximately 100-2000 nm, which is referred to as the near-wavelength regime. The diffraction regime is where L (one cycle) is greater than the wavelength, while the subwavelength regime is where L is less than the wavelength. The cross section of FIG. 1 shows the 3D (dimension) microstructured pillar/hole array, which enhances the bulk film absorption coefficient by factors of 1.5 to over 100. The period of the 3D pillar/hole microstructured array can be seen as a 3D high contrast grating, whose period of the grating Λ can lie between λ/n_1 where n_1 is the optical refractive index of material M_1 and λ/n_2 where n_2 is the optical refractive index of material M_2 . If $n_1 > n_2$ then $\lambda/n_1 < \Lambda < \lambda/n_2$ where λ is the optical wavelength of the light to be absorbed by the microstructured pillar/hole array typically in the "I" region of a P-I-N PD or for APD, the absorbing "I" region P-I-P-I-N where the second "I" region is the multiplication region, or the wavelength of the optical signal to be detected by the PD and APD. At this near-wavelength regime of the 3D HCG microstructured pillar/hole array, the resonance Q (quality factor, or proportional to the ratio of the energy stored in the resonator/energy losses per cycle; where it is the optical cycle, the optical frequency impinging on the resonator or in the resonator) can be as high as 10^7 (see, Chang-Hasnain) if the HCG has minimal absorption loss as is known. In addition, in most cases the ratio of the index of the HCG to the surrounding material index need only be approximately 1.1 to observe the effects of the HCG.

[00113] The HCG effect that may explain the high enhancement of the absorption coefficient of the bulk material is that a single or multiple HCG layer (or a single microstructured pillar/hole array layer) due to its resonance effects and/or due to a varying of the microstructured pillar/hole period spacing, the optical signal resonating in the HCG/microstructured pillar-hole array can be directed to propagate in the plane of the HCG/microstructured pillar-hole array rather than normal to the surface. Together with resonance and in-plane propagation this can greatly increase the absorption path length in the HCG/microstructured pillar-hole array. According to some embodiments, the absorbing HCG mode is operated with a reverse voltage bias for PD/APD and a built-in bias (zero applied bias) in photovoltaic devices.

[00114] Using the phenomenon of near-wavelength and also deep-wavelength where the HCG period is much less than the optical wavelength, and the diffraction

regime where the HCG period is greater than the optical wavelength (See, Chang-Hasnain) the microstructured pillar-hole-void array can have enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100.

[00115] According to some embodiments, the HCG effect is also used in the
5 absorbing mode or lossy mode or low Q of 1-10000 (compared with known HCG
that are in the non-absorbing mode or non-lossy mode to achieve high Q of greater
than 1,000,000 and high reflectivity), in both buried/embedded (not fully buried) Ge
microstructures in Si and buried/embedded void microstr Fig. 49: "Pillar with hole
structures in either Ge or Si to improve the quantum efficiency (QE) and operating
10 wavelength range of Si (400-1100 nm) and Ge (400 to 1800 nm) and Ge on Si
photodiodes and avalanche photodiodes operated in a reverse bias mode of the
pn, pin, pinip junctions (p and n can be switched for certain device configurations)
that can be homo or heterojunction, crystalline or amorphous or any combinations
thereof. In addition, the substrate can be on SOI or BOX or voids to reduce the
15 index of refraction or effective index of refraction and the dielectric constant or
effective dielectric constant (a dielectric with many voids can be represented as an
effective dielectric constant, or equivalently effective capacitance).

[00116] Known silicon photodetectors have been limited to wavelength ranges of
200 to 1000 nm due to indirect bandgap of 1.1 eV. In particular, near the band gap
20 wavelengths of 800-1000 nm, the frequency response of the silicon photodetector
to a modulated optical signal at Gb/s rate is limited to 1.5 Gb/s approximately or
less due to the weak absorption constant of Si at those wavelengths which are
approximately 760 cm^{-1} at 850 nm and 67 cm^{-1} and 63 cm^{-1} at 980 and 1000 nm
respectively, resulting in long absorption lengths of material, 30 microns or more,
25 which results in low frequency response for the PD/APD. The wavelengths 850 nm
is of interest since this is the standard wavelength for short distance (few meters to
a few kilometers) multimode fiber optical datacommunication.

[00117] The amount of incident photons absorbed is approximately given by
 $\eta = 1 - e^{-\alpha L}$ where η (also the quantum efficiency if reflection off the surface of the PD
30 is negligible) is the amount absorbed and " α " is α the absorption constant and " L " is
the length length of the absorber. Using this equation and the absorption constant
of Si at 850 nm, 90% of the incident photons are absorbed at a depth of
approximately 30 μm . Known high speed photodetectors typically have an

absorption region of approximately 2 μm in length. The reason for this is that transit time and RC time of the photodiode need to be considered to have a bandwidth of 20 GHz (or approximately 30 Gb/s) or more and still have an external quantum efficiency of 80-90% or better.

5 **[00118]** Efficiency and bandwidth (transit and RC time): At a field strength of 6×10^4 V/cm the electron drift velocity is 1×10^7 cm/s at a temperature of 300 K. The 3 dB bandwidth of the photodetector due to transit time is given by:
 $f(3\text{dB}) = 0.45/t(\text{transit})$ where $t(\text{transit})$ is the transit time for the carriers to cross the depleted high field region. FIG. 2 is a cross section diagram showing aspects of a
10 typical structure of a PIN photodiode structure. Assuming negligible photocarriers generated in the P region 210 of the PIN 200 and mostly generated in the "i" region 220, the transit time is determined by the electron drift velocity and "d" (the high field "i" region). The PIN 200 is reversed biased (e.g. between -4 and -25 V). The "i" region 220 is fully depleted in this case. The RC time of the PIN structure 200 is
15 determined by the capacitance, which is the ratio of the area ($\pi w^2/4$) of the PIN 220 to d.

[00119] According to conventional techniques, a 30 μm thick absorption layer ("i") to achieve 90% absorption for Si at 850 nm wavelength will give a transit time limited 3dB bandwidth of 1.5 GHz (approximately 2.2 Gb/s) which is too low for
20 many current applications. Many current applications are in the 10-20 Gb/s range and in the near future 40 Gb/s. A d of 2 μm or less is desirable for current high-speed photodiodes in optical datacom applications to give over 30 Gb/s bandwidth.

[00120] RC time is another time to consider in photodiodes (applies to both APD and PD). The 3 dB bandwidth due to RC time is given by $f(\text{RC}) = 1/(2\pi RC)$; where
25 C is the capacitance of the photodiode and R is the load resistance which is typically 50 ohms (and occasionally 25 ohms). Capacitance in the case of a conventional PIN structure photodiode with the "i" region fully depleted by the reverse bias, is just a parallel plate capacitance given by $\epsilon A/d$ where ϵ is the dielectric constant of the material (multiplied by vacuum permittivity of 8.854×10^{-14}
30 farads/cm) which is 11.9 for Si, A is the area of the capacitor ($\pi(w/2)^2$), and d is the depleted "i" (i and l are used herein interchangeably). The $f(\text{RC})$ becomes larger as d increases since the capacitance is decreasing with increasing d and a fixed area, where the diode diameter for example is 30 μm (diameters of high frequency

PD/APD range from 5 to 60 μm). Diameter of diode for calculating the RC time is the total capacitive area of the diode that includes the photosensitive area and any metallization that may contribute to the overall capacitance.

[00121] The overall frequency bandwidth of the photodiode is a sum of the squares of the transit time and the RC time. This is given by the equation:

$$f = 1 / (2\pi(RC)^2 + (\tau/2.4)^2)^{1/2}.$$

[00122] FIGs. 3A and 3B are plots showing bandwidth and QE, respectively, of a bulk conventional Silicon photodiode versus “d” in microns. From plots 310 and 312 in FIGs. 3A and 3B, for the combined $f(3\text{dB})$ of the transit time and RC time and the quantum efficiency η (assuming negligible reflection losses) we see that for bulk silicon to reach 10 Gb/s, the quantum efficiency (QE) is less than 40%, for a 30 μm diameter PD, which is too low for most datacom applications.

[00123] According to some embodiments, to overcome the relatively weak absorption of semiconductors with radiation energies near the bandgap and indirect bandgap semiconductors, for example Si at 850-1100 nm, a microstructured array is used that is etched into silicon that is grown by conventional methods epitaxially such as chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE). Note that according to some embodiments, non semiconductors can be used: such as polymers, glass, ceramics, hybrid material such as transition metal oxides, hydrides, chlorides, sulfides embedded with semiconductor, metal, carbon nanoparticles and or atoms, which may or may not have a bandgap. The microstructured array of silicon consists of pillars of Si and/or holes in Si. See, Garnett and Yang, *Light Trapping in Silicon Nanowire Solar Cells*, *Nano Lett.* 2010, 10, 1082–1087 (hereinafter “Garnett et al.”) that experimentally demonstrates that an ordered array of silicon nanowires increased the optical path length of the incident optical radiation by 73 times greater than that of bulk silicon.

[00124] According to some embodiments, as described earlier, the concept of effective absorption coefficient is introduced. The effective absorption coefficient of the ordered array of Si nanowires is 73X that of bulk silicon; bulk α for Si is 760 /cm and nanowire Si α is 5.548×10^4 /cm at 850 nm which is higher than direct bandgap III-V material.

[00125] It should be noted that the microstructures can also be epitaxially grown using methods such as VLS (vapor liquid solid epitaxial grown) nanowires or microwires (some nanowires have the largest dimension, such as the diameter, in the micron range, so that it can be called a microwire) with or without catalysts, or
5 using a dielectric mask for selective area growth (SAG) epitaxy.

[00126] The nanowire array described in Garnett et al. has a diameter of the nanowire of approximately 390 nm using an array of beads of 530 nm as a dry etch mask. Roughly 1/2 of the Si material is etched away; the effective capacitance for the nanowire array is less than that of the bulk. The effective capacitance can be
10 estimated as two parallel capacitors, one with Si and another with polyimide (filler) whose dielectric constants are 11.9 and 3.4 respectively. The area of each capacitor will be 1/2 that of a 30 μm diameter parallel plate.

[00127] With the effective capacitance lower, the overall 3dB bandwidth for a 30 μm diameter device is significantly higher. FIGs. 4A-4D are graphs showing the
15 enhancement of bulk absorption coefficient vs bandwidth and QE for a microstructured Si photodetector, according to some embodiments. FIGs. 4A and 4B shows the bandwidth (plot 410) and quantum efficiency (plot 420) of a microstructured Si photodiode (PD) or avalanche photodiode (APD) at 850 nm wavelength photons impinging on the PD/APD either single or double pass. With
20 an effective absorption coefficient (EAC) of 73X (412), 30X (414) or 15X (416) over bulk absorption coefficient (BAC), the bandwidth and QE are 54 Gb/s, 98%; 49 Gb/s 90%, 28 Gb/s 90% respectively for a 30 micrometer diameter PD/APD for example. At 1100nm, shown in plots 430 and 440 of FIGs. 4C and 4D, with enhancement, for example, of 172X QE of 90% and bandwidths of 26 Gb/s can be
25 attained using Si microstructured PD/APD. Both PD and APD operate at a reverse bias of -2 to -50 volts range. APDs in general will have less bandwidth than PDs for the same geometry due to the added multiplication layer of the APD. In addition, APDs have a gain-bandwidth product. For simplicity, APD and PD are shown to be approximately the same.

30 **[00128]** According to some embodiments, a combination of low capacitance due to the gaps between the microstructured pillars and the enhanced absorption allows the silicon photodiode and avalanche photodiode to operate at bandwidths greater than 10 Gb/s with high quantum efficiencies (> 90%) at 850 nm

wavelength. This has not been demonstrated by conventional silicon PD/APD at these wavelengths. 850 nm is chosen as the nominal wavelength, but according to some embodiments, wavelengths can have values from 700 to 1100 nm.

- 5 [00129] According to some embodiments, the weak absorption in the bulk can be taken advantage of for photodetector applications since this will allow light at 850 nm and longer to pass through Si substrate and epitaxial layers toward the microstructured silicon with minimal optical loss and minimal photocurrent outside of the high field region, which can diffuse to the i-region and can cause the photodetector to have a degradation in frequency response.
- 10 [00130] According to some embodiments, the techniques described herein are applied to other semiconductors, polymers, organic films, glass, dielectrics, hybrid material such as glass, dielectrics, polymers embedded with nanoparticles of metal, semiconductors. According to some embodiments, one or more of the following are used: Ge, III-V material family such as InP, GaAs, GaN, InGaN; II-VI
- 15 material family such as ZnSe, and also heterostructure material such as III-V grown on Si, Ge grown on Si. For example, for Ge on Si, microstructures are fabricated on the Ge to increase absorption which allows a shorter length of Ge to be used resulting in higher speed due to lower effective capacitance and shorter transit time for the carriers.
- 20 [00131] FIGs. 5A and 5B are cross sections showing aspects of a top illuminated microstructured PIN silicon photodiode, according to some embodiments. FIG. 5A shows the starting basic material structure 500. In FIG. 5B, silicon epitaxial structure is shown for a high-speed high efficiency microstructured photodiode 520. The photodiode 520 in FIG. 5B is designed for top
- 25 illumination. According to some embodiments, BOX/SOI layer 504 may not be used. FIGs. 6A-B, *infra* show an example for bottom illumination. Note that with minor modifications the n and p doping can be switched and the direction of illumination may also be affected. According to some embodiments, the illumination can be either perpendicular to the surface of the PD/APD or at an
- 30 angle off perpendicular to the surface. According to some embodiments, in integrated structures where the optical signal is guided in an optical waveguide, the microstructured absorption region can also be illuminated edge wise, directly into the microstructures or evanescently coupled to the microstructured i region.

[00132] FIG. 5B shows a microstructured pillar and or hole PD 520 in silicon with the starting material 500 consisting of a P-I-N Si layer grown on an Si substrate 502 that can be N doped or low doped in which case an extra N⁺ layer is first grown on the substrate to minimize series resistance. The dimensions and doping of the layers can range as follows; N⁺ cathode contact layer 506 (or a thin layer on top of 506, between 506 and 508) with N doping of greater than $5 \cdot 10^{17}/\text{cm}^3$, and thickness ranging approximately from 0.1 to 10 micrometers or more; N layer 506 with N doping greater than $5 \cdot 10^{17}/\text{cm}^3$, and thickness ranging approximately from 0.1 to 10 micrometers or more; I high field absorption region 508 with background doping of less than $5 \times 10^{16}/\text{cm}^3$ and thickness ranging approximately from 0.1 to 5 micrometers depending on applications; and P⁺ anode layer 510 with P doping greater than $5 \cdot 10^{18}/\text{cm}^3$ and thickness ranging approximately from 0.1 to 5 micrometers or more. The PD (and APD) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area) is nominally 30 micrometers (10-80 micrometers in diameter are possible ranges) in diameter for 20 Gb/s or more bandwidth operation. According to some embodiments, the area can be larger for lower bandwidth or smaller for higher bandwidth operation. The Si microstructures of arrays of holes 522 and/or pillars 524 shown in FIG. 5B, which can be random, patterned or pseudo-random, are for enhancing the bulk absorption coefficient of Si to detect photons with wavelengths from 300-1100 nm. In the case of datacom applications, according to some embodiments, the optical signal wavelengths range from 750-1100 nm. A transparent conducting oxide and P-ohmic layer 526 is also provided.

[00133] The PD 520 is operated in a reverse bias mode, with negative voltage on the anode (P⁺ layer 510 via P-ohmic and bond contact metal 528) and positive voltage on the cathode (N⁺ layer 506 with N-ohmic bond contact metal 530) ranging from -1 to -20 volts. According to some embodiments, the PD structure 520 shown in Fig. 5B (and PD structure 620 in FIG. 6B, *infra*) can also be used for photovoltaic (PV) operation without any external bias.

[00134] As shown in FIG. 5B, the optical signal can impinge normal to the surface or at an angle off normal. In certain cases, optical signal coming in at an angle off normal can have a higher QE and can also be at a certain rotation about the axis normal to the surface. This is to avoid the bald spot effect where some

photons travelling normal to the surface can “see” bald spots whereas for photons illuminating at an angle off normal to the surface, the bald spots are hidden by other microstructures. This is not the case in near field optics where the spacing of the microstructures are of the order of the optical wavelength or subwavelength,

5 the bald spots are not a significant issue.

[00135] FIGs. 6A and 6B are cross sections showing aspects of a bottom illuminated microstructured NIP silicon photodiode, according to some embodiments. The optical signal impinges on the photodiode 620 from the substrate side or bottom. The substrate 602 can be thinned to 10 microns or less
10 by etching for example a via and stopping at the P layer or the photodiode can be fabricated on a BOX (buried oxide) or silicon on insulator (SOI) silicon wafer and the etch via can stop at the BOX layer 604 which can also be selectively etched to the silicon layer 606, the via 630 is as wide or wider as the photosensitive area of the photodiode 620. An antireflection layer (not shown) is applied to the silicon
15 remaining layer 606 or the BOX layer 604 (the BOX layer 604 can be designed as a part of the antireflection layer for example) to minimize reflection (the BOX layer 604 can also be selectively etched off such that antireflection layer can be applied to the silicon P layer 606 to minimize multiple reflections). The back illuminated photodiode 620 has the advantage that a reflector 626 can be applied on the N
20 layer 610 to reflect any light not absorbed on the first pass, in effect doubling the length of the “I” layer 608. The QE can be increased due to the extra length. In addition the reflector 626 on the N layer 610 can be smooth or textured to scatter (non-specular or diffused reflection) the light (optical signal) to optimize absorption by the microstructures (arrays of pillars 624 or holes 622). Since the length of the
25 “I” region is effectively doubled, the transit time can effectively be reduced since only half of “I” is needed.

[00136] Bottom illuminated PDs such as PD 620 in FIG. 6B are also sometimes referred to back/substrate illuminated PDs, and top illuminated PDs such as PD 520 in FIG. 5B are also sometimes referred to front/surface illuminated PDs.

30 **[00137]** According to some embodiments, the basic structure of a microstructured Si photodiode such as shown in FIGs. 5A, 5B, 6A and 6B, is fabricated from a bulk thin film epitaxially grown silicon with a P-I-N structure on a

silicon wafer which can be doped N type or not intentionally doped or low doped N type Si substrate with (100) orientation or other orientation such as (111).

[00138] According to some embodiments, the basic layer structures (such as layers 502, 504, 506, 508 and 510 of structure 500 of FIG. 5A, and layers 602, 604, 606, 608 and 610 in structure 600 of FIG. 6A) are all grown epitaxially using one or more of the following methods: chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), plasma enhanced chemical vapor deposition (PECVD), molecular beam epitaxy (MBE), atomic layer deposition (ALD), pulsed laser deposition (PLD) on Si substrate of either P or N or low doped or undoped) or BOX/SOI substrates.

[00139] Processing details have been left out for simplicity. According to some embodiments the following basic steps are carried out: first (for pillars, not necessary for holes), depositing the p ohmic contact metal layer using e-beam, thermal or sputtering deposition; second, photolithographically (or imprint lithography) defining the microstructure pattern either pillars or holes and forming the etch mask for either dry or wet etching; third, etching of microstructure patterns on the P and I layers partially or fully and can extend into the N layer; fourth, passivating the sidewalls of the microstructure patterns (pillars or holes) with thermal oxide to minimize surface recombination of the photogenerated carriers via surface states due to dangling bonds and other surface imperfections (other passivation techniques may also be applied such as ALD (atomic layer deposition) of Si oxides and Si nitrides); fifth, planarization (filler step) using either spin on glass, polyimide, or plasma enhanced chemical vapor deposition (PECVD) of dielectrics such as Si oxides and Si nitrides; sixth, etch back to expose the P layer or P ohmic metal layer (polyimide or spin-on glass may partially fill the holes or space between the pillars/microstructures); and seventh, ohmic and/or bond contacts formed on the P and N layers. In the case of top illuminated photodetectors, where the optical signal enters on the epitaxial surface where the microstructure patterns are fabricated, a transparent conducting oxide is deposited to connect all the P ohmic metal layers (for pillars). In the case where the microstructures are holes or voids the transparent conducting oxide layer is not used, according to some embodiments. A voltage bias is applied between the P layer (anode) and the N layer (cathode) of -1 to -20 V, and the photodiode is

operated in a reverse bias mode to deplete as much as possible the "I" layer, preferably the entire I layer.

[00140] FIGs. 7A and 7B are cross sections showing aspects of a microstructured avalanche photodiode, according to some embodiments. As in the Si microstructured photodiodes shown in FIGs. 5A, 5B, 6A and 6B, the epitaxial layers 700 for the APD 720 are grown first followed by microstructure processing. The microstructured avalanche photodiode 720 can be illuminated (e.g. with 300-1100 nm) from the top with transparent metal oxide P ohmic contact 726, or the P ohmic contact 726 can be a mirror to reflect the photons illuminating from the bottom (e.g. with 950-1100 nm) to have a double pass absorption. The double pass absorption greatly improves the RC time and the Transit time of the APD for a higher frequency response.

[00141] FIG. 8 is a cross section showing a silicon epitaxial structure for a high-speed high-efficiency microstructured APD, according to some embodiments. Layers 800 are shown prior to microstructure processing. With minor modifications, the n and p doping can be switched and the direction of illumination may also be affected. Starting with a N silicon substrate 802 (or low doped or silicon on sapphire or a BOX /SOI wafer depending on the application and packaging considerations), an N⁺ layer 804 (N ohmic contact layer) is formed with doping concentration of greater than 10^{18} cm^{-3} (typically phosphorous) with layer thickness ranging approximately from 0.1 to 10 μm . A non-intentionally doped layer "i" 806 or a P⁻ (very low doping level P layer) has a doping concentration less than $5 \times 10^{16} \text{ cm}^{-3}$ (this is the multiplication or electronic gain layer of the APD) with thickness ranging approximately from 0.1 to 2.0 μm depending on gain and bandwidth of the APD. A P charge layer 808 is grown with an approximate thickness 0.05-0.2 μm and doping concentration of greater than $2 \times 10^{17} \text{ cm}^{-3}$. An absorption layer 810 is grown (P⁻ or "i") ("I" and "i" are used interchangeably herein) with doping less than $5 \times 10^{16} \text{ cm}^{-3}$ with thickness ranging approximately from 0.1 to 5 μm . Finally a P⁺ contact layer 812 is grown with doping greater than $5 \times 10^{19} \text{ cm}^{-3}$ with layer thickness ranging approximately from 0.1 to 1.0 μm . According to some embodiments, all layers 800 are grown epitaxially using CVD or MOCVD reactors. Doping and thickness are approximate and are adjusted depending on applications.

[00142] For best noise performance of the Si APD, photogenerated electrons should dominate in the multiplication process; i.e. holes diffuse/drift toward p (anode) and electrons diffuse/drift toward the n (cathode) with reverse bias. The Si layers 800 are grown epitaxially using chemical vapor deposition, plasma

5 enhanced chemical vapor deposition, molecular beam epitaxy, atomic layer deposition (can be a combination of these methods to generate the optimal layer structure in doping and interface quality) on doped or undoped substrates. The total length for the electrons to transit range from approximately 0.25 to 7.2 microns. This can be, for example, 0.5 μm for absorption, 0.1 μm for charge, 0.5
10 μm for multiplication, with a total of 1.1 μm for the APD layer structure 800 shown. According to some embodiments, for higher QE, the absorption region can be lengthened to one μm for a total transit length of 1.6 μm for example. Other layer thickness and doping concentrations can be adjusted to optimize device characteristics for different wavelength, integration with CMOS, application
15 requirements, operating conditions such as bias voltage, gain and noise.

[00143] Also, the APD can be illuminated with modulated optical signal from the bottom, where using BOX or SOI, the bulk of the substrate can be removed to minimize optical losses and thus can use the double pass of the photons in the enhanced absorbing microstructured layer.

20 **[00144]** FIGs. 9A-9E are a series of cross sections showing some basic microstructure processing steps, for a high-speed APD, according to some embodiments. FIG. 9A shows the high speed APD epi structure 800 as described with respect to FIG. 8. In FIG. 9B, as in the PD process, a P-ohmic metallization or dielectric mask 910 can be deposited first on the P layer 812 for the
25 microstructured pillars. In the case of holes and/or voids this step may not be carried out. Dry etch mask 910 is deposited on the surface using photolithography, metal/dielectric deposition techniques and wet/dry etching. In FIG. 9C, according to some embodiments, reactive ion etching (RIE) or deep reactive ion etching (DRIE), wet etching using chemicals and oxidation of the Si are used to generate
30 the microstructured pillars 914. Native silicon oxide for surface passivation can be provided by thermal oxidation (which is preferred in some cases), electrochemical anodization, and/or plasma enhanced chemical vapor deposition. According to some embodiments, the thermal oxidation of the pillars 914 can also be used to

fine tune the diameter of the pillar since the oxide is created from the Si material. Thermal oxidation also smooths the surface which is favorable for electrical properties. In FIG. 9D a filler 916 is used to fill or partially fill the space between the Si pillars 914 to support subsequent contact layers to be deposited. The filler
5 916 can be spin on glass, polyimide, dielectric such as silicon nitride, or silicon oxide, that can be deposited for example using plasma enhanced chemical vapor deposition. Once the contacts are made the fillers can be left in place or removed by dissolving the filler with an etchant or solvent. Removing the filler has an advantage of further reducing the capacitance of the device since air has a
10 dielectric constant of 1. The reduction of the capacitance allows the device to operate at higher bandwidth due to reduction of the RC time. In FIG. 9E, the anode and cathode ohmic contact metallizations 922, 924 and 926 are made. Depending on the direction of illumination, transparent conducting oxide TCO 932 (such as indium tin oxide ITO) can be used. In the case of top illumination, a dry
15 etch can be used to expose the pillars if they are buried in the filler. The TCO 932 can then be used to contact the P⁺ silicon pillars at the tip or the P ohmic metallization 922. Ohmic contact metallization is then applied to the cathode (N⁺) layer either on the surface (924) or bottom (926) depending on integration topology.

20 **[00145]** In the case of the optical signal coming from the substrate side (the bottom), the wafer is thinned. If the thinning is carried out by etching it can include a buried silicon dioxide layer such as silicon on insulator, SOI/BOX, such that the oxide layer can act as an etch stop layer. The wafer can be thinned first by chemical mechanical polishing to 100 μm followed by a via etch to the oxide layer
25 which can be selectively etched off, such that the optical signal only need to traverse a few micrometers of Si bulk material. Anti-reflection coating 930 is applied to the Si surface to minimize reflection loss. Ohmic metallization is applied to the N⁺ layer followed by bond metal 924. On the microstructured pillars, ohmic metallization is applied to the P⁺ tips (if its not applied already in the preliminary
30 steps), followed by bond metal 922. According to some embodiments, an advantage of the optical signal entering from the substrate surface (i.e. the bottom) is that the light will bounce and travel twice within the pillar structures, thus

increasing the quantum efficiency. According to some other embodiments, the pillars can be made shorter to improve the transit time.

[00146] According to some embodiments, the optical signal can also enter from the edge as shown FIG. 52, *infra*, either in a guided mode or in free space. In the edge application, TCO 932 and solid anode ohmic contacts may not be used and wafer thinning may not be carried out. Cathode ohmic contacts can instead complete the structure. According to some embodiments, in edge approach, the pillars are arranged such that their density is not uniform to optimize the capture of the optical radiation. It can be arranged in a V pattern for example to reduce optical reflection.

[00147] Not shown in FIGS. 9A-9D are mesa etching steps used to define the diameter of the APD 920. According to some embodiments, other methods such as ion implantation may also be used. Note that the microstructures themselves provide good confinement of current in the vertical direction and not in the lateral direction. Other known processing steps that are not shown for sake of simplicity include: thermal oxidation passivation of exposed surfaces; adding guard rings; thinning of the wafer; adding anti-reflection coatings; annealing of ohmic contacts; and creating via holes for removal of filler.

[00148] Taking advantage of low absorption constant of bulk Si. High speed photodiodes made with III-V material often are constructed such that the photocarriers are generated only in the i layer of a PiN structure to minimize the photogenerated carriers outside of the high field region that can cause degradation to the frequency response of the device. This can be done easily in III-V material since there are many ternary and quaternary material such as InGaAsP, InGaAs, InAs, that are lattice matched to InP and the bandgap of these alloys can be changed by altering the composition such that the P⁺ anode 812 and P charge 808 layers are mostly transparent and the i layer is absorbing. However it is not easy for silicon since there are no materials that are lattice matched to silicon. Germanium can be grown on silicon but with the addition of a buffer layer to accommodate for the lattice mismatch.

[00149] According to some embodiments, a method to overcome this issue in silicon is to take advantage of the low absorption constant of silicon at radiation near the bandgap of silicon. According to some embodiments, the wafer can be

thinned to the insulator of an SOI structure and the 850 nm optical signal will only traverse 1-2 μm of bulk silicon losing approximately 10% or less of the incident radiation. The rest of the radiation continues to the microstructured pillar silicon where the absorption is stronger possibly due to resonance effects. According to

5 some embodiments, the shape of the pillars can be circular, oval, rectangle, chevron, hexagon, double-circle, crescent, star, or any shape to optimize absorption and collection efficiency. The pillar diameter range from 50-1200 nm (smallest dimension can be 50 and largest dimension 1200 nm) and can be spaced uniformly or non-uniformly, periodic or aperiodic, chirped, or a pattern either locally
10 or globally to optimize APD/PD performance and applications. The spacing of the pillars can be 20-2000 nm. The microstructured pillars can be 100 to 10000 nm in length that is optimized for bandwidth and efficiency for a particular wavelength near the silicon bandgap for example 850, 880, 980, 1000 nm.

[00150] According to some embodiments, multiple dimensions (both structure
15 and spacing) of the microstructures within a single PD/APD can broaden the resonance bandwidth of the microstructures such that the enhanced absorption coefficient is over a broader optical spectrum.

[00151] The substrate becomes less absorbing as the wavelength approaches 1100 nm (1.1 eV Si indirect bandgap).

20 **[00152]** According to some embodiments, the microstructured pillars/holes/voids can have orientations that are not perpendicular to the surface of the silicon substrate. Other orientations off perpendicular or with multiple orientations or even random or pseudo-random are possible to optimize the QE with respect to the directivity of the optical signal. In multiple and/or random or pseudo random
25 orientations of the microstructures, the device become less sensitive to the direction of light illumination which is beneficial in PV applications. In certain applications, antenna like high directivity of the PD/APD may be desirable to avoid cross talk for example from other optical signal sources or to further improve its QE.

30 **[00153]** According to some embodiments, microstructured hole arrays, instead of pillar arrays, are used as light traps in silicon. Microstructure hole arrays have similar properties as microstructured pillars. See e.g. Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications,

Next Generation (Nano) Photonic and Cell Technologies for Solar Energy Conversion, edited by Loucas Tsakalakos, Proc. of SPIE Vol. 7772, 77721G (2010). According to some embodiments, instead of etching microstructured pillar arrays as described herein, microstructured hole arrays are etched using RIE/DRIE

5 and similar processing for the pillars, including thermal oxidation for surface passivation, deep ion implantation for electrical isolation, confinement of optical fields and reduction of capacitance. In the case of the hole arrays, it is possible that the filler need not extend the entire length of the hole. For example, if the surface tension of the filler is high, only partial filling of the holes with filler will be possible
10 and provide support for subsequent layers of TCO, metal, oxide, silicide, alloys to name a few that may be necessary to complete the device structure. According to some embodiments, in the case of microstructured holes, fillers are not used in the PD/APD/PV devices since the surface is contiguous rather than consisting of islands as in the case of microstructured pillars.

15 **[00154]** According to some embodiments, the microstructured holes can have diameters of 50-3000 nm and can be a square, hexagon, oval, rectangle, chevron, double-hole, with the smallest dimension at 50 nm to the largest dimension of 3000 nm approximately. The spacing between holes (adjacent edges) can be regular or irregular or a pattern at 20-2000 nm. The depth (or length) of the hole can be 100
20 to 10000 nm and can be uniform depth or non-uniform depth. Dimensions are chosen for optimal absorption, quantum efficiency, bandwidth and radiation collection efficiency for a particular wavelength and application.

[00155] As discussed earlier, to optimize High Contrast Grating in the Absorption regime of this invention, it may be desirable to have the microstructured
25 enhanced absorption structures on materials of a lower refractive index such as BOX or SOI where the silicon dioxide refractive index is lower than that of Si, Ge or III-V/II-VI material. According to some embodiments, the effective refractive index can be made lower than the refractive index of the microstructures with the inclusion of voids in the substrate. FIGs. 10A-10B are cross sections showing
30 aspects of a top illuminated microstructured photo diodes, avalanche photo diodes and/or photovoltaics (PV) with microstructured voids in N-Si, according to some embodiments. Voids can be included in the substrate or as a microstructure for enhancing absorption coefficient as will be discussed *infra*. Refractive index in the

optical spectrum of Si, Ge, III-V material typically range from 3-3.6, by using silicon dioxide such as SOI and voids that are 50% of the material in volume, the refractive index or effective refractive index can be reduced to approximately 0.5 that of the bulk semiconductors. By adjusting the ratio of the volume of the voids to the material (Si for example) the effective refractive index can also be adjusted from a few percent to more than 90% that of the bulk material. The voids can be filled with other material such that it is not just air, gas or vacuum, but a dielectric such as glass, polymer, dielectric, oxide, or amorphous semiconductor that can be optically and/or electrically passive and or active with optical and/or electrical gain for example.

[00156] FIG. 10A shows the layers 1000 including N-Si layer 1006 which contains microstructured voids 1008 that effectively reduce the refractive index of the N-Si layer 1006 as described. FIG. 10B shows a top illuminated PD/APD/PV 1020 that includes microstructured pillars 1024 and/or holes 1022, as well as transparent conducting oxide layer 1026. Microstructured voids 1008 can be random or patterned. The microstructured voids 1008 can be used reflect photons back to the absorbing "I" region if the voids 1008 are patterned to have HCG effects at wavelengths where loss is low such as 950-1100 nm. According to some embodiments, BOX or SOI substrates can also be used together with voids or without voids or without BOX/SOI.

[00157] According to some embodiments, the microstructuring techniques described herein are also applied to heteroepitaxial material (III-V on Si, Ge on Si, or II-VI on Si). Ge (bandgap 0.66 eV at 300K) having much smaller bandgap than Si, can be used for detecting optical signals at 850 and 1300 nm. Using the techniques described herein, Ge devices can also be made to detect optical signal with wavelength at 1550-1600 nm which can then replace III-V material based photodetectors. According to some embodiments, microstructures are grown such as nano/microwires or etched from bulk material with or without lithographic masking.

[00158] Ge thin film can be grown epitaxially on Si. See, e.g. Kang et al, Epitaxially-grown Ge/Si avalanche photodiodes for 1.3 μ m light detection, 23 June 2008 / Vol. 16, No. 13 / OPTICS EXPRESS 9365 (hereinafter "Kang et al."), where an APD was fabricated for 1310 nm wavelength operation for a 30 μ m diameter

device. The QE of the device with a 1 μm Ge absorption length is only 56% whereas by using microstructured pillars/holes/voids according to embodiments described herein, QE of approximately 90% or greater can be achieved at 1300-1600 nm wavelength with bandwidths of approximately 30 Gb/s or greater for a 30
5 micrometer diameter PD/APD. Such devices can find useful applications in datacenters, local area networks, and in metro and long distance optical data/telecommunications. According to some embodiments, integration on silicon is used which results in significant cost reduction in manufacturing and packaging. In comparison, in Kang et al. a 30 μm diameter APD was only able to reach
10 approximately 15 Gb/s bandwidth at 1310 nm and cannot extend the wavelength due to low absorption of the bulk material without sacrificing a significant reduction in bandwidth.

[00159] FIGs. 11A and 11B are cross sections showing aspects of a heteroepitaxial APD structure of Ge on Si, according to some embodiments.

15 Layers 1100 and APD device 1120 show a possible heteroepitaxial APD structure of Ge on Si (as opposed to descriptions, *supra*, of homoepitaxial APD/PD structure where only silicon is used with different doping concentrations). Similar processing methods as in the homoepitaxial Si APD are used to fabricate microstructured pillar/hole arrays. According to some embodiments, the absorption constant of
20 bulk Ge is enhanced by greater than 70X, for example 73-172X. According to some embodiments, APDs and PDs with bandwidths in excess of 30 Gb/s can be achieved in devices with an active diameter of 30 μm or less at wavelengths to 1750 nm and QE of approximately 90% or greater. This is a significant improvement over existing Ge on Si APD with illumination normal or off normal to
25 the surface of the substrates.

[00160] According to some embodiments, the microstructured pillar and hole (and variations thereof) arrays can be fabricated in Si, Ge, Ge on Si, SiGe on Si, SiGe on Ge; it can be any combination of Si, Ge and SiGe.

[00161] At longer wavelengths 1200-1800 nm, Ge (germanium) photodiodes are
30 often used since Ge has a bandgap of 0.66 eV (whereas Si has a bandgap of 1.1 eV). However, for high bandwidth applications (greater or equal to 20 Gb/s) Ge photodiodes are only good to 1350 nm due to the fact that for transit times to be approximately 30 picosec (electron saturated drift velocity is 6×10^6 cm/s at 1×10^4

V/cm in order to have a bandwidth of approximately 20 Gb/s ($f(3\text{dB})=0.44/\tau$ where τ is the transit time through the “I” region) the length of the absorption region or the “I” region is limited to approximately 2 microns. At this length, the QE at 1550 and 1600 nm is less than 10%, which is not generally acceptable for optical receivers for datacom and telecom applications. In a waveguide configuration, the length of the absorption region can be 50-100 microns and still achieve 20 Gb/s or higher with QE equal or greater than 90%. The waveguide Ge on Si photodiode structure have been reported by other research groups however such waveguide photodiodes have excess optical losses due to waveguide losses and coupling loss (coupling of optical signal to the optical waveguide) which can be as high as 3 dB or half of the optical signal is lost. The “free-space” coupling (where the optical signal is directed to the PD/APD using elements such as lens, diffraction elements, light pipes, optical waveguides to name a few) of optical signal to the microstructured photodiode and avalanche photodiode have much less optical losses, typically a few percent or less. One of the reason is the large area of the microstructured PD/APD which is 30 microns in diameter as compared to waveguide photodiodes its dimensions are a few microns, typically 1-2 microns. Not only is coupling loss high in waveguide PD/APD, it often uses active alignment which requires that the waveguide PD/APD is turned on to monitor the coupling of the optical signal into the waveguide PD/APD. This active alignment is slow and time consuming which adds cost to the packaging of the waveguide PD/APD in any optical receiver module. In contrast, the large area microstructured PD/APD, according to some embodiments, uses only passive alignment where it is aligned without turning on the microstructured PD/APD. Such alignment is much faster and easier which reduces the cost of a microstructured PD/APD in any optical receiver module. It should be noted that with the effective capacitance of the microstructured PD/APD significantly lower than bulk PD/APD by 10 to 80% or more, the area of the microstructured PD/APD can be correspondingly larger by 10 to 80% or more.

30 **[00162]** In FIG. 11B, a microstructured Ge on Si pillars/holes APD structure 1120 with bottom illumination is shown. Epitaxial layers for an APD Ge on Si are used where the optical absorption to generate electron-hole pairs takes place in Ge and the gain/multiplication of the electrical charged carriers takes place in Si. The

epitaxially grown layers are similar to Ge on Si bulk (thin film) APD with the following layer compositions ranges (shown in FIG. 11A). N is undoped, or low doped (20 ohms-cm) Si substrate 1102, which can also be SOI or BOX, to allow removal of the Si substrate for bottom illumination and/or to reduce the refractive index. If SOI or BOX substrates are used, the N ohmic contact and bond metal will be on the N⁺-Si surface adjacent to the multiplication I region. N⁺ contact layer 1104 which can be 2-8 microns, N⁺ > 5.10¹⁸ cm⁻³. I multiplication layer (or gain layer) 1106 which can be undoped (not intentionally doped), 0.2-1.0 microns thick and I < 1.10¹⁶ cm⁻³. P charge layer 1108 having a thickness of 0.05-0.2 microns and P ~ 1-6. 10¹⁷ cm⁻³. P⁻ low temp Ge buffer layer 1110 having a thickness of ~ 0.01-0.04 microns and P⁻ ~ < 1. 10¹⁶ cm⁻³. I or P⁻ absorption layer 1112 having a thickness of 0.2- 2.0 microns, and I (or P⁻) <1. 10¹⁶ cm⁻³. Finally, P⁺ contact layer 1114 has a thickness of 0.05- 0.2 microns, and P⁺ > 2. 10²⁰ cm⁻³, approximately.

[00163] Starting with a wafer with all the layers 1100 grown for APD operation, the processing details are left out for simplicity. The basic steps involve first, depositing the p ohmic contact metal layer 1126 using e-beam, thermal or sputtering deposition. The microstructure pattern of either pillars or holes is photolithographically, using positive or negative or image reversal photoresist methods depending on pillars or holes, defined to form the etch mask for either dry or wet etching. According to some embodiments imprint lithography can be used. The microstructure patterns are etched on the P⁺ and I (or P⁻) and P Ge layers 1114, 1112 and 1110, respectively, partially or fully to the P Si layer 1108 (e.g. using fluorine, chlorine, bromine based gases such as SF₆, CF₄, BCl₂, Cl₂, for selective dry etching using RIE and DRIE). The selectivity of the etch between Ge and Si can be as high as 70, so as to etch Ge 70 times faster than Si by adjusting gases mixtures, pressure, temperature and bias, and power. The sidewalls of the microstructure patterns (pillars or holes) are passivated with dielectric or SiGe and gradually reducing the Ge content such that Si remains on the surface (using for example atomic layer deposition ALD) and subsequently using thermal oxidation to minimize surface recombination of the photogenerated carriers via surface states due to dangling bonds and other surface imperfections. According to some embodiments, other passivation techniques may also be applied such as ALD of Si oxides and Si nitrides. Planarization is performed using either spin on glass,

polyimide, or PECVD deposition of dielectrics such as Si oxides and Si nitrides. An etch back is performed to expose the P layer. For microstructured holes and pillars, it may not be necessary to planarize completely, by using polyimide or spin-on glass to partially fill the holes and spaces between pillars. Ohmic and/or bond

5 contacts are formed on the P and N layers. For top illuminated photodetectors, where the optical signal enters on the epitaxial surface where the microstructure patterns are fabricated, a transparent conducting oxide 1126 (the transparent conducting oxide may not be used in the case of microstructured holes) is deposited to connect all the P ohmic metal layers (for pillars). A voltage bias is

10 applied between the P⁺ Ge layer 1114 (anode) and the N⁺ Si layer 1104 (cathode) of -2 to -45 V. The APD 1120 is operated in a reverse bias mode to deplete as much as possible both of the "I" layers. Many detailed processing steps are left out such as annealing, surface preparations, deposition of ohmic contacts, bond metal, RIE, DRIE, wet etching, masks for etching, mask removal, antireflection coatings,

15 mirrors such as Bragg reflectors on the microstructured layers, to name a few. Ohmic contact metallization to P and N semiconductors and bond metallizations are well known in the art and details are not mentioned here. Also, holes are used in electron-hole pairs as charged electrical carriers and holes as in a physical void such as the microstructured holes. From context it should be understood if "hole"

20 refers to a charged electrical particle or a physical void.

[00164] According to some embodiments, Ge surfaces of the microstructured pillars or holes and any Ge surfaces exposed to an electric field, where electric current can flow and/or where electric charges are formed are passivated to reduce current leakage, minimize surface states that can be a potential sink or

25 recombination centers for carriers, especially photogenerated carriers of electrons and holes (as in Si, thermal oxide or rapid thermal oxidation, to create SiO₂ and SiO_x used to passivate any silicon surfaces that can cause excessive leakage current or recombination centers for photogenerated carriers, or a carrier sink) and GeO_xN_y which is a native Ge oxynitride that is formed in two stages, where the Ge

30 microstructured pillars and/or holes are first exposed to oxygen and then to ammonia ambient in a rapid thermal annealer to form the Ge oxynitride passivation layer. These passivation methods are well known in the art.

[00165] FIG. 12 is a cross section illustrating aspects of a passivation method for Ge surfaces on microstructures, according to some embodiments. Shown are microstructured Ge pillars 1202 (or holes) for a PD and/or APD. On the Ge surfaces is conformally epitaxially grown SiGe layer 1210. Gradually, the Ge content is reduced within layer 1210 until only Si is exposed on the surface. Thermal oxidation of Si is then used to passivate the exposed Si surfaces, forming SiO₂ layer 1212, to minimize leakage current and surface states that can be a potential sink for carriers, especially photogenerated carriers (electrons and holes) that can degrade QE.

[00166] FIGs. 13A and 13B are graphs showing the effects of microstructure enhancement of Ge bulk absorption coefficient for photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments. According to some embodiments, a 73x enhancement of bulk absorption coefficient is gained in PD/APD devices having microstructured pillars/holes at 1550 and 1600 nm. FIG. 13A shows the bandwidth versus “d” or the length of the “I” layer for 1550 nm (point 1310) and for 1600 nm (point 1312). Note that APDs have both a Ge “I” layer and an Si “I” layer; whereas for PDs have just a Ge “I” layer. FIG. 13B shows QE versus “d” or “I” layer length for 1550 nm (point 1320) and 1600 nm (point 1322). It can be seen that for a 30 micron diameter active region PD/APD bandwidths of 40 and 31 Gb/s can be attained at 1550 nm and 1600 nm optical wavelength respectively with 90% QE. This result was not achievable with bulk Ge photodiodes and avalanche photodiodes of conventional design.

[00167] The separation of using Ge microstructures to absorb the light generating e-h (electron-hole) pairs and using Si for the avalanche multiplication of the carriers, preferably electrons, results in an APD with very low noise due to the fact that the ionization ratio (defined as hole ionization rate/electron ionization rate) for electrons injected into the multiplication region (gain region which is a function of applied reversed bias voltage) is lower than in III-V material family. This result in a low excess noise factor leads advantageously to a high signal to noise ratio (S/N).

[00168] FIGs. 14A-14B are cross sections showing aspects of a top-illuminated Ge on Si avalanche photodiode having microstructured pillars/holes, according to some embodiments. FIG. 14A shows the bulk layers 1400. In FIG. 14B, top

illuminated microstructured Ge on Si APD 1420 is shown with a semitransparent conductive oxide 1426 connecting the P-ohmics on the Ge microstructured pillars 1424 (holes 1422) as described *supra*. Both top and bottom illuminated microstructured Ge on Si share similar epitaxial structures. The processing steps

5 for top and bottom illuminated microstructured APDs are similar. The main differences are that the transparent conductive oxide for top illuminated APD (or PD) is replaced with an opaque ohmic/bond metallization that can act as a mirror to reflect the optical signal back toward the absorption I layer. According to some embodiments, the mirror can also consist of Bragg reflectors either wafer bond to

10 the microstructure or epitaxially or vacuum deposited such as dielectric or conductive metal dielectrics to enhance the reflectivity to greater than 90% of the optical signal. In addition, bottom illuminated PD/APD may require a window or via where most of the Si substrate is removed to reduce optical losses depending on the wavelength of the optical signal.

15 **[00169]** FIGs. 15A-15C are cross sections illustrating aspects of bottom-illuminated Ge on Si avalanche photodiodes having microstructured pillars/holes, according to some embodiments. FIG. 15A shows the bulk layers 1500 prior to forming the microstructures (pillars and/or holes). FIG. 15B shows a Ge on Si microstructured APD 1520 with the optical signal illuminating from the bottom

20 (substrate side) for wavelengths from 1200-1800 nm. Note that Si is basically transparent at these wavelengths. According to some embodiments, to further reduce optical losses, the Si wafer can be thinned just at the area of illumination, for example through a via of 50-500 microns in diameter and thinned to the N⁺ layer of the Si; or the Si substrate 1502 can include a BOX or SOI layer 1502. The Si

25 substrate 1502 can then be thinned selectively to the BOX or insulator layer 1502 which can be etched away selectively. According to some embodiments, an anti reflection layer (not shown) can be added to minimize reflection. The advantage of this arrangement is that the optical signal will have a double bounce, reflecting off the metallization 1526 on the Ge P⁺ layer 1514 and traversing the Ge "I" absorber

30 region 1512 once again. For example, as shown in FIGs. 13A and 13B, keeping the same absorption length, Ge "I" length, the QE for both 1550 and 1600 nm would be approximately 90% or higher for a Si substrate side (bottom) illumination by the optical signal assuming negligible reflection loss. According to some

embodiments, the Ge "I" absorption length can be further shortened to increase the bandwidth and still maintain acceptable QE.

[00170] For Ge epitaxially grown on Si, it is known that the bulk absorption coefficient is greater than that of Ge bulk by itself (not grown on Si); at 1750 nm the
5 Ge on Si absorption coefficient is approximately 100 cm^{-1} . According to some embodiments, this can be enhanced by the microstructured pillars and/or holes by 172 times. The resulting enhanced Ge on Si microstructured pillar and/or holes absorption coefficient can be about $1.72 \cdot 10^4 \text{ cm}^{-1}$.

[00171] FIG. 15C shows an APD 1540 in which the microstructure extends all
10 the way to the N cathode layer 1506 to further reduce capacitance and refractive index. In this case, the absorbing i layer 1512 is microstructured as is the charge layer 1510 and the i multiplication layer 1508. According to some embodiments, the microstructures can also be formed partially into the charge and multiplication layers 1510 and 1508. Additionally, according to some embodiments, the
15 microstructures in the absorbing layer 1512 and the multiplication layer 1508 need not be the same. In FIG. 15D, photons may generate electron hole pairs in the multiplication region which may contribute to added gain but also may contribute to excess noise. According to some embodiments, the absorption and multiplication region using the microstructure APD is combined in one region without the use of
20 the charge layer. This is possible due to enhanced absorption: the length of absorption and multiplication can be of the order of one micron or less allowing reasonable avalanche voltage.

[00172] FIG. 15D shows a microstructured APD 1560 where the absorption and multiplication region are a single region 1566, pillars or holes, according to some
25 embodiments. This is enabled by the microstructure enhancing the absorption coefficient so that less than one micron of the absorbing microstructure length is needed to achieve QE of approximately 90% or more and avalanche multiplication can also occur in this length of material. For example, if $0.5 \text{ }\mu\text{m}$ of microstructured Si shown in Fig.15D is the thickness of layer 1566, a back illuminated APD 1560
30 allows a double bounce of the optical signal reflecting off the N ohmic contact and bond metallization resulting in an effective length of one micron of absorption length. The Si APD 1560 can operate at $0.5 \text{ }\mu\text{m}$ multiplication length resulting in gain of 3 dB or more with a reverse bias ranging from -5 to -50 volts. According to

some embodiments, the structure shown in FIG. 15D can be applied to other material systems such as Ge, Ge on Si, III-V, and III-V on Si or not on Si.

[00173] FIGs. 16A and 16B are graphs comparing single pass and double pass photodiodes and/or avalanche photodiodes based on Ge on Si, according to some

5 embodiments. Points 1610 and 1620 show the bandwidth and QE values for single pass with d of approximately 1.4 microns and points 1612 and 1622 show the bandwidth and QE values for a thinner d of approximately 0.7 microns single pass. For double pass the device will have points 1612 for bandwidth and point 1622 for QE. At 1750 nm optical signal wavelength, using absorption coefficient
10 data of 100/cm for Ge on Si and with, for example, 172 times (172X) enhancement factor due to the microstructured Ge on Si photodiode/avalanche photodiode structures, a bandwidth of 27 Gb/s and a QE of approximately as high as 90% can be attained with an "I" (also "d") length of approximately 1.4 microns for a single pass (top illuminated - where the optical signal illuminates the top Ge
15 microstructured side). As mentioned earlier, for photodiodes the "I" or "d" is the absorption length, whereas for avalanche photodiodes the "I" is the combined absorption length and the multiplication length. For example, for an APD to achieve 27 Gb/s the total "I" length needs to be limited to 1.4 microns. A double pass arrangement can be used such that for example the absorption length is 0.9
20 microns and the multiplication is 0.5 microns, making the absorption length effectively 1.8 microns to achieve QE above 90%. However, if we instead have the optical signal illuminate from the bottom Si substrate side, the Si substrate and Si layers are basically transparent and have minimal optical losses (approximately 1-3 dB/cm) at optical radiation energies that are below the bandgap of Si (1.1 eV or
25 1127 nm wavelength at 300K) for example for radiation from 1200-1800 nm wavelengths. The advantage of illuminating from the Si substrate side (bottom) is that the optical signal can have a double pass at the Ge "I" absorbing region if the metallization on the P^+ contact layer is reflective which it should be since it is metallic composing of Au, Al, Ag, Cr, Zn, Ti, Ta, Ge, or a combination of these
30 metals and semiconductors. Bragg reflectors consisting of material with alternating refractive indices from oxides, nitrides, chlorides, semiconductors, either wafer bonded to the microstructures or deposited on the microstructures can also be incorporated. Reflectivity can be greater than 90%. With double pass, as shown in

FIGs. 16A and 16B, a bandwidth of 40 Gb/s can be attained with a QE approximately as high as 90% or more.

- [00174]** FIGs. 17A-17B are cross sections showing aspects of a top-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 700 to 1800 nm, according to some embodiments. FIG. 17A shows the bulk layers 1700. In FIG. 17B, Ge on Si microstructured pillars 1724 and/or holes 1722 are in a configuration for photodiode 1720. This is essentially a P-I-N structure where the "P" and "I" are Ge with microstructured pillars 1724 and/or holes 1722 to enhance the bulk absorption coefficient of Ge grown on Si. The increase in the absorption coefficient of Ge grown on Si (Ge on Si) could be due to the stress build in the Ge epitaxial layer due to lattice mismatch with the Si host substrate that it is grown on. Optical signal as in the case for Ge on Si APD can be illuminated from either the microstructured side (as in FIG. 17B) or the substrate side (as in FIG. 18B).
- [00175]** FIGs. 18A-18B are cross sections showing aspects of a bottom-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 1200 to 1800 nm, according to some embodiments. FIG. 18A shows the bulk layers 1800. FIG. 18B shows photodiode 1820 configured for signal illumination from the Si substrate side (bottom illumination) with photo energies that are less than the Si bandgap of 1.1 eV at 300K. The corresponding wavelength range is 1200 to 1800 nm. Ohmic contact 1826 can also act as a mirror such that the light makes a double pass of the Ge absorbing microstructures where the metal contact layer on the P Ge can reflect the optical signal back toward the Ge "I" absorbing layer.
- [00176]** It should be noted that in all the discussions of the P-I-N structures, according to some embodiments the P and N are interchanged such as with an N-I-P structure formed on a P substrate or on a low doped P substrate or undoped substrate. According to some embodiments, the N and P for the APD structures are also interchanged and the substrate can be P, low doped P or undoped. However, in an Si multiplication layer, to achieve the lowest noise and the best S/N, electrons are injected into the multiplication region as dominantly as possible since the ionization rate of electrons is higher than the ionization rate of holes in Si; the ionization ratio for Si can range from 0.06 to 0.002 where as compared to Ge

and InGaAs it is 0.9 and 0.45 respectively. This is why in many of the embodiments described herein the enhanced absorption is in Ge microstructures and the gain or multiplication which is dependent on the field strength and therefore on the applied reverse bias voltage which for the described devices can
5 range from -10 to -60 V, is in Si.

[00177] According to some embodiments, the microstructured pillars and or holes for Si and Ge on Si photodiodes (PD) and avalanche photodiodes (APD) are used to replace relatively expensive III-V photodiodes. The Si microstructured pillars and holes PD/APD can operate from 500 to 1100 nm at bandwidths of 20
10 Gb/s or higher and QE of 90% or higher. In particular, the datacom wavelengths of 730-980 nm. The microstructured pillars and or holes on Ge epitaxially grown on Si PD and APD can operate from 500-1800 nm with bandwidths of 20 Gb/s or more and QE of 90% or more. In particular, the telecom wavelengths of 1250-1600 nm and possibly to 1750 nm. The techniques described herein thus extends the
15 wavelengths, bandwidth and QE of conventional Si and Ge on Si free space coupled photodiodes and avalanche photodiodes.

[00178] According to some embodiments, the microstructured pillars can also be fabricated using VLS (vapor-liquid-solid epitaxy) growth of Ge nanowires on an Si substrate. Others have demonstrated the growth of vertical Ge nanowires on Si
20 (111) orientation for example, with Au nanoparticles as catalysts for the VLS epitaxial growth using chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD). Crystal orientations other than (111), or with materials with multiple orientations such as in polycrystalline may be used. Materials such as Si, Ge, III-V, glass, quartz, metal, to name a few can also be used as substrates.
25 According to some embodiments, a thin Ge buffer layer of approximately 2nm on Si (111) substrate is formed together with Au nanoparticles as catalysts for VLS growth in a CVD reactor. The Au catalyst can be deposited using a lithography mask to expose photoresist that is coated on the Si substrate. The Au is evaporated onto the Si substrate with patterned photoresist. Using standard
30 processing methods such as lift-off, the Au pattern is left behind on the Si substrate which is then the catalyst for Ge VLS growth on Si substrates. According to some embodiments, it can also be grown using selective area growth where a dielectric

mask is deposited on the Si substrate with a pattern of voids that allow Ge to grow in the void using CVD.

[00179] The microstructure of pillars and holes on the surface of a bulk photodiode not only enhance the absorption coefficient by factors ranging from 10-
5 200 over the absorption coefficient of bulk material (material without any microstructured features and grown on lattice matched substrates so that stress due to lattice mismatch is minimal) but also significantly reduce the capacitance of devices such as PDs and APDs. The reduction in capacitance allows the PD or APD to have a shorter absorption length, which in turns result in a faster transit
10 time for the photogenerated carriers to be swept out of the high field region. The absorption region typically is depleted as much as possible by the reverse bias voltage that is applied externally with an electric field strength approaching 10,000 V/cm or higher. If the microstructured pillars or holes can result in removing half or more of the semiconductor material, which for silicon has a dielectric constant of
15 11.9 and germanium have a dielectric constant of 16, replacing the removed material with either air (dielectric constant of 1) or polyimide (dielectric constant of 3.5) or other dielectrics with low dielectric constants, then the overall capacitance can be estimated to be the sum of the capacitance due to the total area occupied by the semiconductor and the capacitance due to the area occupied by air or
20 polyimide. $C(\text{total}) = C(\text{semiconductor}) + C(\text{air or polyimide})$ where $C = \epsilon A/d$ where ϵ is the dielectric constant times the free space permittivity (8.854×10^{-14} farads/cm), A is the area occupied by the semiconductor or air/polyimide and d is the length of the "l" region which can be the absorbing region or the absorbing and multiplication region as in the case for APD. From the equation for $C(\text{total})$, the more
25 semiconductor material which has a high dielectric constant removed and replaced by low dielectric material such as air/polyimide/ SiOx/spin on glass the lower the overall capacitance and the faster the RC time. This reduction of capacitance for PD and APD invention can be extended to other PD and APD such as those of III-V material, microstructures can be fabricated on its surfaces and extend into and
30 pass the optical signal absorbing regions to remove half or more of the semiconductor material to reduce its capacitance and can effectively make a larger area PD/APD and have the same bandwidth as before etching microstructures on the device. The larger area allows for easier coupling of the optical signal to the

photodetector. A simple formula for the increase in radius for example by replacing semiconductor material with low dielectric material is: $r = (\epsilon_1 / ((\epsilon_1 - \epsilon_2)x + \epsilon_2))^{1/2} r_0$ where x is the fraction of semiconductor area left, ϵ_1 is the dielectric constant of the semiconductor, ϵ_2 is the low dielectric material such as air or polyimide or spin on glass, and r_0 is the radius of the active area of the PD/APD before etching microstructured pillars and or holes. As an example, for a 20 micron diameter Ge photodiode with $\epsilon_1=16$ and for simplicity $\epsilon_2=1$ (air) and $x=.5$ (half of the semiconductor material is removed in the microstructured pillar or holes), the increase in the new radius with the same capacitance as the non-microstructured Ge PD is 13 microns or a diameter of 26 microns which is significantly larger than 20 microns and can significantly reduce the cost of coupling the optical signal into the microstructured large area photodetector. This reduces the cost of passive packaging of the optical receiver module and increase the yield.

[00180] FIGs. 19A, 19B and 19C are diagrams illustrating how microstructures can reduce capacitance of a photodiode such that a larger area photo diode can be fabricated with the same bandwidth and QE, according to some embodiments.

FIG. 19A shows the bulk layers 1900 in an InP-InGaAs-InP structure. In FIG. 19B, the InP-InGaAs-InP layers with microstructured holes 1922 effectively reduce the capacitance of the photodiode 1920 to allow a larger area photodiode to be

fabricated with the same bandwidth and QE. FIG. 19C is a top view showing PD 1920. The microstructured holes 1922 can be 100-1000 nm in diameter with depth of 0.1 to 3 microns. Also visible in FIG. 19C is contact ring 1930 and bond pad 1932. According to some embodiments, a complementary microstructured pillars can also be fabricated. According to some embodiments, the sidewalls of InP and InGaAs can be passivated with SiO_x, SiN_x (silicon oxide and silicon nitride via ALD or PECVD), polyimide or spin-on-glass that can be spun on using standard processing methods. The absorption coefficient of the bulk material can be enhanced by up to two orders of magnitude or more.

[00181] According to some embodiments, III-V material such as InP, InGaAs, InGaAsP, InAs, InSb, GaSb, InGaSb on Si, Ge on Si, is epitaxially grown in a sub micrometer selective area growth (SAG) or vapor liquid solid (VLS) (See, e.g. Sarkar et al, Heteroepitaxial growth dynamics of InP nanowires on silicon, Journal of Nanophotonics, Vol. 2, 021775 (12 February 2008); Roest, et al, Position-

controlled epitaxial III–V nanowires on silicon, Nanotechnology 17 (2006) S271–S275) heteroepitaxy using metal organic vapor epitaxy with or without catalyst which can consists of Au, Cu, Al, Ti, W, Fe, Cr to name a few. Also for vertical oriented microwires grown on silicon, wafers with surface orientation (111) are

5 selected. It is not necessary that the microwires be normal to the surface, it can be off normal and even have a mixture of orientations.

[00182] In VLS growth, the silicon wafer that has the layer structure for APD or PD just prior to heteroepitaxial growth is photolithographically (or e-beam or nanoimprint lithographically) patterned with aperture ranging from 10-5000 nm, and
10 spaced between 10-3000 nm. An Au deposition (e-beam, or thermal evaporation) follows with thickness of 0.1-10 nm, followed by a lift-off, VLS epitaxial growth in a MOCVD reactor.

[00183] For SAG growth (See, e.g. Chu et al, Wurtzite InP nanowire arrays grown by selective area MOCVD, Phys. Status Solidi C 7, No. 10, 2494 – 2497
15 (2010)), a 50 nm SiN_x is PECVD (or sputtered or ALD) deposited on a (111) oriented Si wafer with the necessary APD or PD epitaxial layers grown on it ready for heteroepitaxial growth. Using lithography (photo, e-beam or nanoimprint) apertures are defined with dimensions ranging from 10-5000 nm and spaced between 10-10000 nm followed by dry etching (RIE) to open a via to the silicon
20 surface. The wafer is then ready for SAG of Ge, III-V microwires in a MOCVD reactor.

[00184] Detailed processes such as surface treatments, surface preparations, annealing, plasma etching, are not described for simplicity. These processes can be found in the literature.

25 **[00185]** FIGs. 19D and 19E are cross sections showing aspects of fabricating an APD device having a III-V absorbing layer grown on a P-I-N silicon multiplication layer, according to some embodiments. In FIG. 19D, a Si APD structure 1940 is etched as shown for v epitaxial growth of the III-V material. In FIG. 19E a III-V absorbing layer is grown on P-I-N silicon multiplication layer for APD device 1960.
30 As in the III-V on Si for a PD device, the III-V nanowires or microwires can be grown on Si using VLS process with or without catalyst. Since the footprint of the nano/microwires on Si is of the order of a micron, defects due to stress from lattice mismatch are not a significant issue and high quality III-V nano/microwires can be

grown on Si. According to some embodiments, SAG is used for fabricating III-V microstructures on Si electronic gain layers.

5 [00186] From FIGs. 19D and 19E it can be seen that the InGaAs on Si APD 1960 starts with a Si APD structure 1940 where microstructures of holes or pillars are etched to the charge layer 1944 or just before the charge layer 1944. According to some embodiments, the microstructure holes and/or pillars can be etched into the multiplication layer 1942. Then using a process, for example SAG, with or without silicon oxide on the Si microstructure's sidewalls, I-InGaAs is grown, ending with P-InGaAs at the surface. Surface growth can use a process such as
10 epitaxial lateral overgrowth (ELOG) to form a continuous P-InGaAs film of high quality. P ohmic alloy and bond metal 1966 are formed and annealed on the P-InGaAs. The back side processing consist of thinning the Si wafer using for example a BOX layer for selective etch stop and removing the BOX layer. Anti reflection can be coated on the backside silicon to reduce reflection. N ohmic 1968
15 is fabricated on the N Si layer. The optical signal is illuminated from the bottom. A reverse bias of -5 to -50 volts is applied to the cathode and anode. As mentioned earlier, the small footprint of the InGaAs on Si microstructure of the order of 10 square microns allows for high quality InGaAs material to be grown where lattice mismatch causing crystal defects are not significant.

20 [00187] According to some embodiments, the integration of Ge, III-V with Si PDs, PVs (See, FIG. 25C, *infra.*) and APDs allow the absorption spectrum of Ge and III-V material on a mature Si electronic platform. It allows integration of III-V with Si CMOS ICs for example for photodetector, optical light source such as light emitting diodes (LED) and laser diodes (LD) and III-V electronics such as
25 transistors.

[00188] Multiple absorbing material and voids as microstructures. According to some embodiments, the microstructured pillars and/or holes are regrown with Ge such that both Si and Ge are microstructured to enhance the bulk absorption coefficient. According to some embodiments, voids can also be buried or
30 embedded to generate a buried/embedded microstructure such that the surface is more planar. The microstructured voids can also enhance the absorption coefficient, by being patterned so as to enhance reflection and also to reduce the effective refractive index of a material (e.g. Si), reduce the weight of the device,

and increase mechanical flexibility. The microstructured voids can be random, pseudo-random or patterned typically with dimension and spacing that are approximately the order of a wavelength or subwavelength. According to some embodiments, instead of combining Ge with Si, others combinations can be used
5 for example III-V with Si or other semiconductor material, polymers, or other non semiconductor absorbers, which can significantly broaden the absorption spectrum over that of a single absorber.

[00189] The enhancement using nanowires (See, e.g. Garnett et al, Light trapping in silicon nanowire solar cells, Nano Letters, 2010, 10, 1082-1087;

10 Kelzenberg et al, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, Nature Materials, vol. 9, March 2010, 239-244) and nanoholes (See, e.g. Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Proceeding of SPIE, Vol. 7772, 77721G-1, 2010) have been reported by various groups. The known use of

15 nanowire for light trapping are for photovoltaic applications where the photogenerated carriers diffuse to the anode or cathode of a P-N junction with zero external bias, operating at DC (direct current). According to many of the embodiments described herein, the photogenerated carriers are swept out with an external reverse bias in the absorbing "i" region of a P-I-N diode (PD) or P-I-P-I-N
20 diode (APD) for high modulation bandwidth (e.g. greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain (e.g. gain greater than 3 dB). In addition, according to some embodiments, multiple absorbing materials can be used to broaden the absorption spectrum. The multiple absorbing materials are connected in parallel as current sources whereas in known
25 technology the absorbing materials are connected in series. In addition, the use of voids as microstructures to enhance the absorption of the material according to many embodiments described herein allows the surface to be more planar and simplify processing since fillers may be avoided. Also, the more planar surface allows the epitaxial growth of semiconductor Bragg reflectors to enhance reflection
30 for double or multiple pass absorption in the I absorption layer of the PD/APD.

According to some embodiments, Dielectric Bragg reflectors can also be used in a more planar surface since the surface can be highly N or P doped and the ohmic contact can be made on the periphery such as a ring ohmic contact and the

dielectric Bragg reflectors deposited on the photosensitive area such as shown in FIG. 29, *infra*. Chemical mechanical polishing (CMP) can be used to smooth the surface of the epitaxial layer with buried voids.

[00190] Further aspects of fabricating devices having microstructured Ge that is buried or embedded in Si microstructure will now be described. FIG. 20 shows bulk layers without a final P-Si layer for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments. The final P-Si layer, according to some embodiment will be the last layer grown in the epitaxial structure where the first layer grown is the layer adjacent to the substrate, followed by the second layer that is adjacent to the first layer, and so forth to the last layer grown. Shown in FIG. 20 is P-I-N PD structure 2000 and a P-I-P-I-N APD structure 2020 both without the final P-Si layer. In many of the embodiments described herein, N can refer to N (mid N type doping of $5 \cdot 10^{16} \text{ cm}^{-3}$ to $8 \cdot 10^{17} \text{ cm}^{-3}$, low N doping less than $1 \cdot 10^{17} \text{ cm}^{-3}$, and high N doping greater than $5 \cdot 10^{17} \text{ cm}^{-3}$, with the same for P doping. I (or i) doping is commonly defined as intrinsic, or not intentionally doped or low doping background doping of less than $5 \cdot 10^{16} \text{ cm}^{-3}$. The "I" region is configured such that the field of a P-I-N junction is developed across the "I" region usually with an external reverse bias. In PD and APD applications, the absorbing material is in the "I" region so that the photogenerated carriers can be quickly sweep to anode (P) and cathode (N) layers. For APDs, the carriers (electrons in most cases shown here, since this gives the lowest noise APD) are swept to the second "I" region for multiplication (current gain) before transiting to the cathode layer). In the Figures herein, P-I-N, P-I-P-I-N structures are shown and the top P layer(s) that are in contact to external circuits are referred to as the anode and the N layer(s) that are in contact to external circuits are referred to as the cathode; the layers can be interchanged from P to N and N to P with P or low dope substrates to also fabricate PD's and APD's.

[00191] FIG. 21 is a cross section showing etching of microstructured pillars and/or holes for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments. The microstructure pillars 2104 and/or holes 2102 are etched into the I-Si layer, partially or entirely or to/into the N (PD structure) or P (APD structure) Si layer. The etching process can be one of the following: wet chemical etching, dry etching using reactive ion etching (RIE), a

deep reactive ion etching (DRIE), ion milling, and/or focused ion beam milling. The etching can be isotropic or anisotropic or a combination of isotropic and anisotropic. As shown in FIGs. 22 and 23, *infra*, Ge is then regrown in the etched region (i.e. the area around the pillars and on the sidewalls of the pillars in the case of pillars, or area in the holes, sidewalls of the holes in the case of holes) isotropically, anisotropically, or by selective area growth (SAG) where a dielectric layer such as SiO_x, SiN_x, cover area where regrowth of Ge is not desired which in some embodiments can include the sidewalls. During etching if a dielectric mask material such as SiO_x, SiN_x, SiC_x is used and left in place during epitaxial growth, the epitaxy layers may not grow on the dielectric mask in a crystalline film and may be amorphous in nature or may not grow on the dielectric layer other than some dendrites. Note that the isotropic or anisotropic growth rate often depends on the crystal plane it is growing on and any etched structures may expose multiple crystal planes resulting in different growth rates at those planes that can lead to anisotropic growth in the etched regions with 3D microstructures.

[00192] Growth of Ge on Si is well documented in the literature where a thin buffer Ge layer is first epitaxially grown at a lower temperature followed by a higher temperature Ge epitaxial growth using chemical vapor deposition (CVD), molecular beam epitaxy (MBE), atomic layer deposition (ALD), low pressure -CVD, and or a combination of growth techniques, for example the thin Ge buffer layer can be grown by MBE and the high quality thicker Ge film grown by CVD. The thin Ge buffer layer is to allow lattice mismatch stress to be accommodated between Si and Ge, (see, e.g. Feng et al, High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide, APPLIED PHYSICS LETTERS 95, 261105 ,2009).

[00193] The Ge regrowth may have voids or non-planarities and, where useful, the surface can be planarized using polishing such as chemical mechanical polishing (CMP) or etching. FIG. 22 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after the Ge "I" layer is grown in the etched region and planarized, according to some embodiments. Note that according to some embodiments, planarization is not needed and is omitted. After the Ge "I" layer 2202 is grown and planarized, a P⁺ Ge capping layer 2204 is grown to complete the P-I-N structure of a PD or P-I-P-I-

N structure of an APD. Optical signal or photons with wavelengths ranging from 400 to 1800 nm can illuminate the PD/APD 2220 from the anode (top) side (P⁺ side) 2202 and optical signal or photons with wavelength ranges 950-1800 from the substrate side (bottom) since Si is mostly non-absorbing at these wavelengths.

5 According to some embodiments, it is advantageous to configure the device 2220 for illumination from the substrate side since this will allow a double bounce of the optical signal or photons within the absorbing Ge microstructures embedded in Si. Shown in these figures are only the basic epitaxial layer structures. Structures and layers not shown for simplicity include: anti-reflection coatings, passivations, ohmic
10 metals, bond metallization, any metal interconnect to CMOS, via's for electrical connectivity, arrays of PD/APD for multichannel optical interconnects, to name a few. Optical signal/photons can illuminate either normal to the surface or at any angle off normal, including rotation angles for optimal PD/APD performances; optimizing QE and bandwidth of the PD/APD.

15 **[00194]** FIG. 23 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after I-Ge regrowth and planarization, and a cap layer of P-Si, according to some embodiments. In the case of FIG. 23, the buried Ge microstructures 2302 are capped with a P⁺ Si layer 2304. The Si P⁺ cap layer (anode) 2304 has low optical loss at optical wavelengths of 950-1800 nm
20 and therefore generates minimal photocarriers that are not in the high field "I" region of the PD/APD 2320 and contribute minimal diffusion photocurrent which can lead to a degradation of the frequency response of the PD/APD 2320 and the QE of the PD/APD.

[00195] Some dimension doping ranges for the buried or embedded Ge and
25 capping layers shown in FIGs. 20-23 will now be provided in greater detail, according to some embodiments. The dimension of the microstructured Ge (e.g. 2202 and/or 2302) can range in depth from 0.1 to 5 micrometers, have a lateral dimension range from 10-5000 nm, and a spacing between adjacent microstructure structures (the structures can be identical or non-identical) in contact (overlapping)
30 to 5000 nm. The "I" doping for both Ge (2202 and/or 2302) and Si (2104) is less than or equal to $5 \cdot 10^{16}/\text{cm}^3$. "I" is often called intrinsic or not intentionally doped and can have either a p or n background doping, the doping level is low enough that a reverse bias voltage of -2 to -45 volts can fully deplete the "I" region of

mobile holes or electrons (carriers). The capping layer, Si (2304) or Ge(2204) thickness can range from 0.1 to 5 μm with doping level greater than or equal to $6 \cdot 10^{17}/\text{cm}^3$. These parameters can be adjusted to other values, but the goals are to increase or optimize the QE and bandwidth of the PD/APD for a given application.

- 5 Series resistance, photogenerated diffusion current, ohmic contacts, capacitance, transit time, depletion of the "I" absorption region all contribute to the performance of the PD/APD. In addition for double/multiple bounce within the "I" region for optical signal illuminating from the bottom substrate side, a reflective metal or dielectric stack such as a Bragg reflector/mirror consisting of alternating dielectric
- 10 layers of different refractive indices or HCG can be used to reflect the optical signal back into the microstructured absorbing region at the top anode side. With the Si cap layer as in FIG. 23, the optical signal can illuminate the Si P⁺ cap layer (anode) 2304 and, since Si has minimal losses at 1100-1800 nm (below bandgap radiation), it can also have double bounce of the optical signal within the
- 15 microstructured buried/embedded Ge 2302 by providing a reflector such as a Bragg reflector epitaxially grown at the Si N⁺ layer or at the Si substrate to reflect the light back into the absorption region.

[00196] According to some embodiments, all the discussions of microstructured layers herein, light can additionally impinge from top and bottom surfaces, as well

20 as on the sides of the microstructures, either directly or from scattering, near field effects, interferences, or resonance, which can vastly improve the QE of the microstructured photosensors since photogenerated carriers are generated directly in the high field absorbing "I" ("I") layer(s).

[00197] According to some embodiments, dopant choices for Si and Ge (group 4

25 elements) include the following: (1) for donors (n-type) from group 5 elements - antimony, phosphorus, and arsenic; and (2) for acceptors (p-type) from group 3 elements - boron, aluminum, and gallium.

[00198] It is also noted that in the structure shown in FIG. 23, the I-Ge microstructures 2302 buried in Si 2104 are completely surrounded by Si which has

30 a lower refractive index than Ge. At 1000-2000 nm wavelength range, the refractive index of Si is approximately 3.49 and for Ge is 4.1. The index ratio of Ge/Si is 1.17 so according to Chang-Hasnain reference, HCG effects will exist. The resonance and field concentration in the absorbing Ge microstructures can further enhance

the absorption coefficient from that of the bulk absorption coefficient value anywhere from greater than 1X to several orders of magnitude. The index difference also causes light to be confined and concentrated in the high index material, in this example, Ge; further improving QE.

5 [00199] The silicon (Si) microstructure can detect photons with wavelength ranging from 300-1100 nm and the germanium (Ge) microstructure can detect photons with wavelengths ranging from 300-1800 nm. According to some embodiments, for high bandwidth and high QE, the shorter wavelengths, 300-600 nm, may generate photocarriers outside the "I" region resulting in a diffusion
10 current that can result in non-optimal bandwidth and or QE. Where bandwidth is not an issue, the degradations may not be very significant.

[00200] FIGs. 24A and 24B are cross sections showing aspects of a microstructured APD with buried/embedded I-Ge absorbing microstructures in I-Si microstructures, according to some embodiments. FIG. 24A shows the bulk layers
15 2400. In FIG. 24B, the etched pillars 2424 and/or holes 2422 are filled with I-Ge (intrinsic-Ge, non-intentionally doped or undoped or low doped Ge) and finished with a capping layer 2426 of P⁺ Ge or Si to complete the anode of the APD 2420. The microstructured Ge 2422 is buried/embedded in Si 2412. Optical signal of wavelength 950-1800 nm (or photons from 300-1800nm where the shorter
20 wavelengths, 300-900 nm, may not have as high a bandwidth) can illuminate the APD 2420 from either top or bottom at various angles to the normal and/or normal to the surface. According to some embodiments, the starting layers prior to the I-Ge regrowth into the etched regions can also include the P⁺ Si layer 2426, such as shown in FIG. 7 with layer 726, *supra*. In the case shown in FIG. 24B, the starting
25 layer was removed to minimize P dopant diffusion during I-Ge regrowth. The buried or embedded Ge microstructure in Si microstructure allows the APD (or PD) 2420 to operate in two regimes. A first regime is at wavelengths where Si is low loss and Ge is absorbing or high loss (950-1800 nm). In this Si low loss regime, the Ge microstructures 2422 with a Si P⁺ anode cap layer 2426 is completely
30 buried in Si which has a lower refractive index than Ge. The Ge microstructure arrays can have HCG low Q with Q ranging from 1 to 3000 approximately (or other resonant, scattering, near field, linear and non-linear optical effects) or high enhancement of the absorption coefficient. A second regime is where both Si and

Ge are absorbing, 300-945 nm, and both Si microstructures 2424 and Ge microstructures 2422 work in parallel (parallel current generators) absorbing the photons with enhancement of the absorption coefficients of both Si and Ge. This is particularly advantageous for examples in photovoltaic applications.

- 5 **[00201]** FIGS. 25A - 25C are cross sections showing aspects of a photodiode having buried/embedded Ge microstructures in a Si microstructured pillar and/or hole array, according to some embodiments. Starting with a Si PD epitaxial layer structure 2500 with or without the P layer 2526, microstructures of holes 2522 and/or pillars 2524 are etched into the Si P layer 2526 and I layer 2512 and can
10 extend into the N layer 2510. Regrowth of Ge 2522 (or III-V material such as InGaAs, InAs, InSb, GaN, InGaN to name a few) using a process such as SAG with or without silicon oxide on the sidewalls of the Si microstructure 2524 or using a process such as VLS with or without catalysts, the I-Ge layer 2522 is grown
15 followed by P Ge 2526 (or a P-Si layer which may be more suitable for top illuminated devices) at the surface where a process such as ELOG can be used to form a continuous P-Ge film. P ohmic alloy, annealed, followed by bond metallization completes the contact 2528 for the anode. The back side processing as discussed earlier is deposited on the silicon surface to reduce reflection. See, e.g. FIGs. 19A-19C, *supra*, where the silicon is thinned and etched to the BOX
20 layer selectively. The BOX layer is etched selectively and an anti reflection N ohmic alloy is formed on the N-Si layer, annealed and followed by bond metallization, which completes the cathode contact. Reverse bias of -2 to -10 volts is applied between the anode and cathode for high bandwidth PD applications. In PV applications, 0 bias is applied.
- 25 **[00202]** According to some embodiments, the dimensions and doping are similar to the Si microstructured PD shown in FIGs. 5A-5B, *supra*, with the I-Ge doping level less than $5 \cdot 10^{16} \text{ cm}^{-3}$, and dimensions ranging in thickness of 0.1 to 5 micrometers, and lateral dimension of the microstructure ranging from 10 to 5000 nm with adjacent structures that can touch/overlap to 5000 nm separation. Optical
30 signal/photons can either illuminate from the anode top side or cathode bottom side with wavelength range of 300-1800 nm and normal to the surface or at an angle to normal which can also include rotation. For bottom side illumination, the Si is thinned down to a few micrometers thickness for illumination at wavelength

ranges of 300-900 nm. Only the basic layers are shown for simplicity. For example, the following structures are not shown: isolation mesa or diffusion or ion implantation, passivation, anti-reflection, ohmic metal, guard rings (e.g. for an APD). Both Si microstructures and Ge microstructures can detect the optical
5 signal/photons in parallel for wavelengths where both are absorbing, 300-1100 nm, and only the Ge microstructure at wavelength ranges 900-1800 nm. The cap layer 2526 and 2546 in FIGs. 25B and 25C respectively can be either P⁺ Si or P⁺ Ge. For broad modulation bandwidth (sometimes just referred to as bandwidth) of greater than 10 Gb/s (gigabits per second), P⁺ Si cap layer is preferred for wavelengths
10 ranges from 950 to 1800 nm, since at these wavelengths Si has low optical losses (also referred to as low loss). According to some embodiments, the structure shown in FIGs. 25B and 25C can also be used for photovoltaic applications where no external bias is purposely applied in the reverse direction.

[00203] According to some embodiments, for all the structures shown, the P and
15 N can be interchanged to form for example N-I-P structures for the PD and PV (photovoltaic) and N-I-N-I-P structures for the APD.

[00204] The regrowth of Ge microstructures in Si also have applications in photovoltaic devices where the device is operated without external reverse bias. The P-I-N PD structure for example with Ge microstructures embedded or buried in
20 Si microstructures effectively have two bandgaps, Si bandgap and Ge bandgap that is exposed to the solar radiation. The combination of two bandgaps widens the absorption spectrum of the photovoltaic device and therefore can collect a broader spectrum of the solar energy. The two bandgaps can have a higher QE and or short circuit current over that of single bandgap photovoltaic devices or multiple
25 devices connected in series. The microstructures also have enhanced absorption that can further improve the QE and or short circuit current of the photovoltaic device. The solar spectrum at AM 0 and AM 1.0, with a photovoltaic device with a spectrum width of 300-1800 nm, at least approximately 90% of the solar spectrum is captured. In addition, in the PV device with Ge and Si microstructures are
30 adjacent laterally to each other (i.e. in parallel) rather than being vertically adjacent (i.e. in series) as in prior art PVs. This allows the Si and Ge to be exposed to solar photons equally and are parallel current generators that are additive; $I_{Si} + I_{Ge} = I_{total}$

where I_s is the photocurrent generated by the Si microstructures and I_{Ge} is the photocurrent generated by the Ge microstructure and I_{total} is the total photocurrent.

[00205] Although according to some embodiments the use of Si and Ge are described, according to some other embodiments, other materials are used.

5 According to some embodiments, Si is used with an InP microstructure embedded or buried. According to some embodiments, more than two materials are used such as Si, Ge, InGaAs, InP, GaAs, GaN, InGaN, InSb, to name a few. The microstructures, in addition to pillars and holes, can be embedded and or buried to use the effects of HCG to enhance the absorption coefficient over that of bulk
10 absorption coefficient to further improve QE and minimize the use of material in order to reduce cost of manufacturing.

[00206] FIG. 25C is a cross section showing grown Ge, InP, InGaAs to name a few, within silicon microstructures. SAG can be used where the sidewalls of the microstructures are oxidized or coated with a conformal dielectric and where the
15 oxide/dielectric is removed at the bottom of the microstructure surface where it is approximately parallel to the silicon substrate where it can provide crystalline information for the growth of Ge, InP, InGaAs microstructures. The area where the Ge, InP, InGaAs will epitaxially grow with or without catalysts using various growth methods such as VLS, MOCVD, CVD to name a few, is approximately 100 square
20 microns or less; more typically around 0.3-3 square microns. Because of the small area, crystalline defects due to lattice mismatch are not significant. The sidewalls with the silicon dioxide that can be thermally grown or deposited using ALD, provide an electrical insulation between the Si and the Ge, InP, InGaAs SAG grown layer. It should be noted that SAG growth can continue until the Ge or InP or
25 InGaAs (to name a few) can merge above the silicon microstructure and with lateral over growth (LOG) epitaxial process, the microstructures of Ge or InP or InGaAs can form a continuous epitaxial thin film layer that can be doped P type for the anode layer.

[00207] FIGs. 25D and 25E are cross sections showing aspects of a forward
30 biased device such as a vertical cavity surface emitting laser (VCSEL), according to some embodiments. VCSEL 2562 can also be fabricated using similar processing as described *supra* for the PDs, PVs and/or APDs. Starting with a Si PIN structure 2562, Si microstructure hole(s) 2564 are etched through I-Si layer

2566 to the N-Si layer 2568. According to some embodiments, the etching of hole 2564 can extend into the N-Si layer 2568. An SAG process is followed with or without silicon oxide on the Si microstructure sidewalls (oxide 2570 is shown).

First, a GaAs/AlGaAs distributed Bragg reflector 2572 (DBR) all N type is grown,
5 follow by N-GaAs 2574, The active layer 2576 is undoped InGaAs/GaAs multiple quantum well (MQW) of 1-5 wells, followed by P-GaAs 2578 to the surface and using ELOG which can form a continuous film at the surface of the I-Si 2566. Dielectric DBR 2582 on the P-GaAs 2580 completes the optical cavity. P ohmic alloy with anneal and bond metal 2584 on P-GaAs 2580 completes the anode
10 contact and N ohmic alloy with anneal and bond metal 2582 on N-Si 2568 completes the cathode contact. Forward bias of 1 to 20 volts to the anode and cathode will result 1200-1300 nm light to be emitted from the VCSEL 2560.

[00208] The design and growth of VCSELs at 1200-1300 nm and other wavelengths are known. See, e.g. "High-performance 1200-nm InGaAs and 1300-
15 nm InGaAsN quantum-well lasers by metalorganic chemical vapor deposition", Tansu et al; Selected Topics in Quantum Electronics, IEEE Journal of (Volume: 9, Issue: 5), 2003.

[00209] According to some embodiments, longer wavelength are selected when embedding InGaAs, InGaAsN and other III-V material, because at wavelengths
20 greater than 1000 nm silicon is mostly transparent and does not introduce excess additional optical losses. Accordingly, Si is a good heat sink for the VCSEL 2560. According to some embodiments, the GaAs/AlGaAs DBR 2572 is replaced with a silicon/air or a dielectric DBR on the bottom by thinning the Si wafer and etching to the BOX layer, removing the BOX layer and depositing a dielectric DBR. Design of
25 DBR, dielectric and semiconductors are well known. The silicon/air DBR will require further processing, using sacrificial layers such as Ge that can later be selectively etched away via etch trenches.

[00210] According to some embodiments, an LED is fabricated by applying minor variations, including removing the DBRs and adding multiple Si
30 microstructures. The LED can use MQW or just a simple heterojunction of P-GaAs/ I-InGaAs/N-GaAs for example. Other semiconductors can also be used such as InGaAsN, InGaAsP, GaAsN, to name a few. The substrate can be another material such as sapphire, SOI, insulator on Si (IOS), ceramic, glass, quartz, GaN,

crystalline or non-crystalline. Additionally, other material for blue/UV LEDs such as GaN, AlGaIn, GaInN, AlN, can be grown using epitaxial reactors and methods of fabrication described above.

[00211] According to some embodiments, voids are formed, that are buried or
5 embedded in Si or Ge on Si or Ge. As used herein “buried” refers to cases when
the void is beneath the surface, and “embedded” refers to cases when the void can
intersect or be slightly above the surface. As described *supra*, during regrowth of
Ge on a microstructured Si with pillar and/or hole arrays, voids can develop due to
the fact that growth rate during epitaxial growth often depends on the crystal
10 orientation of the surface. Since etching microstructured pillars and/or holes in Si
can expose different surface orientation of the side walls, asymmetric growth rate
of Ge on these different Si surface orientation can result in void formation.
According to some embodiments, the void formation is exploited to generate a
buried and/or embedded microstructured void arrays that can behave as HCG and
15 or light trapping structures that concentrate the optical field and/or resonance
through interference of the optical field (amplitude and phase), scattering, near
field, linear and non-linear optical effects to enhance the bulk film absorption
coefficient by one to several orders of magnitude. In addition, the voids can be
used to reduce the effective refractive index of a material (e.g. Si with voids) since
20 the optical field sees an average or effective refractive index. At dimensions on the
order of a wavelength or less, the refractive index of voids and Si, for example, can
be approximated with an effective refractive index which is the average of the
volume occupied by Si and the volume occupied by the void. For example, if Si
occupies 1/2 the volume and voids occupy 1/2 volume, the Si index is 3.49 and the
25 void is 1.0 (for air), then the average effective index is approximately 2.25.

[00212] The voids also reduce capacitance of the device if the voids are
generated in the “I” region, as discussed *supra*; where the space between
microstructured pillars or the microstructured holes can reduce the capacitance of
the P-I-N PD diode or the P-I-P-I-N APD diode. The voids according to some
30 embodiments are either buried (buried holes) or embedded (space between pillars)
and the total capacitance is approximately the capacitance of the total area
occupied by the voids plus the capacitance of the total area occupied by the
semiconductor. In the case where the voids do not occupy the full thickness of the

"I" layer (i.e. only occupy part of the thickness), then the effective dielectric constant can be estimated by taking into account a volume that contains both the void and the semiconductor extending through the thickness of the "I" layer, the volume of the void and the volume of the semiconductor in a given volume; for example if the voids occupy 1/2 of a given volume of the thickness of the "I" layer and the semiconductor material occupies 1/2, and if the semiconductor material is Si with dielectric constant of 11.9, then the average effective dielectric constant is approximately 6.5, where the void is assumed to be air with dielectric constant of 1 for that given volume. The total area occupied by this effective dielectric constant, consisting of both voids and semiconductor material, is used in the capacitance calculation plus the area occupied only by semiconductor in the "I" region to give the total capacitance of the P-I-N or P-I-P-I-N diode. Reduction of capacitance leads to a reduction in RC time constant for the diode which improves the bandwidth of the PD and APD.

[00213] Although buried voids in semiconductor material are known, such voids are conventionally regarded as detrimental and as such are to be avoided. According to some embodiments, such voids are intentionally created and form useful features in the semiconductor material.

[00214] FIG. 26 is a cross section showing starting epitaxial layers in which microstructured voids are fabricated, according to some embodiments. To generate voids in PD, PV and APD structures start with a structure 2600. The starting material can be a Si PD or APD structure with or without the Si P⁺ anode layer. Details of the layers are not shown for simplicity.

[00215] FIG. 27 is a cross section showing microstructured holes/pillars etched into the I-Si layer, according to some embodiments. The microstructured holes (or space around pillars) are etched into the Si "I" layer and can extend pass the "I" layer or can be partially into the "I" layer. Wet and/or dry etching can be used or a combination of wet chemical and dry etching (RIE, DRIE for example) where the wet etching can be used to remove damage due to dry etching or wet etching in combination with dry etching and oxidation to form a certain shape or surface smoothness. As shown in FIG. 27, the etch can be isotropic or anisotropic, the sidewall can have negative or positive slope (slope defined with respect to the plane of the substrate). For anisotropic etching both negative and positive slope

can exist at the same time for an etched feature such as a pillar or hole.

Anisotropic epitaxial growth can result in void formation, with the shape of the void being determined by many factors including: side wall slope, crystal orientations of the side wall, growth conditions, pressure, temperature, flow rate, growth technique
5 (CVD, MBE, ALD or a combination of growth methods), surface preparation, and surface oxidation. According to some embodiments, surface oxide, partial oxide or other dielectric 2726 can be intentionally deposited on the side walls, which can also influence the regrowth of Si or Ge (or any other semiconductor such as InP, GaAs, InGaAs, GaN, InGaN, to name a few) and can be used to form voids.

10 **[00216]** FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping P⁺ anode layer 2826, according to some embodiments. The buried voids 2800 can be uniformly spaced, or with chirped spacing, or any complex patterns with a combination of periodic and aperiodic spacing or it can be random or pseudo-random. The buried voids 2800 can have a
15 length ranging approximately from 0.1 to 10 micrometers and lateral dimension ranging from 10-5000 nm. The voids can also be overlapping one another. Although FIG. 28 shows buried voids in Si, according to some embodiments buried voids can be formed in Ge. For example, in a Ge epitaxial layer on Si, or any other semiconductors, such as InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, and other
20 semiconductors in the III-V material family. The voids can be non-uniform in size and shape within the void and adjacent voids. The voids may also have non-uniform spacing and/or orientation. However, with proper process control uniformity in size and shape, patterning, random and pseudo-random placements of the voids can be attained. For simplicity the voids are shown to be uniform.

25 **[00217]** FIG. 29 is a cross section showing Bragg reflectors formed on the P-Si surface to provide a highly reflective mirror, according to some embodiments. With a more planar surface, high reflectivity Bragg reflectors 2900 may be deposited or grown using dielectrics or semiconductors on the P silicon layer 2826 surface. The ohmic contact and the bond metallization 2902 can be on the
30 peripheral in a ring configuration as shown in FIG. 29. Optical signal illuminating from the bottom will have a double/multiple pass through the absorbing I region thereby improving QE and the bandwidth of the PD/APD. In PV where bandwidth is not an issue, then the QE will be improved. According to some embodiments,

Bragg reflectors 2900 can be configured for wavelength selectivity so as to reflect the optical signal back into the absorbing I region.

[00218] According to some embodiments, voids are not only in the I region but are also formed in the P and/or N region of a PIN PD or PV, in the P charge region, 5 in the I multiplication region and/or the P anode and N cathode region of an APD. According to some embodiments, voids can also be formed in the substrate. The density, shape and material (voids can be filled with different material from vacuum, gas, helium to dielectrics with or without doping with rare earth elements for optical gain for example, carbon/graphene/diamond, copper, ceramics for 10 thermal conductivity for example) of the voids in each layer can be different or the same, or different/same within the same layer.

[00219] According to some embodiments, voids are also used to make the material more mechanically flexible and bend and or conform to different surface contours. For example, in PV applications where large sheets of the device are 15 fabricated, the sheets can conform to contours in for example the roof, or the sheets of semiconductor PV can be rolled for compactness in storage prior to deployment. According to some embodiments, voids sized between 0.01 microns and 1000 microns are introduced into semiconductor and/or glass material for use with photo voltaics for purposes of increasing flexibility and/or resistance to 20 physical damage and/or damage propagation.

[00220] High-density voids in semiconductors are also resistant to crack propagation since the crack will terminate at a boundary, in this case the boundary of the void. This is advantageous for large devices such as solar cells where if an object such as hail or stone strikes the solar cell, only the point of contact will be 25 damaged and perhaps a small adjacent area (5-50% of the diameter of impact for example) where the damages are localized to area of impact and cracks will not propagate across the entire cell. A device may survive such small damage events with minimal degraded performance without taking the entire solar panel down.

[00221] According to some embodiments, the voids are also formed in other 30 materials also such as glass, ceramics, polymers, metal, plastics, to name a few, to avoid crack propagation in case of foreign object impacts since cracks will terminate at a boundary, in this case the boundary at the void.

[00222] FIG. 30 shows an example of a PIN PD/PV structure 3000 with microstructured voids to enhance absorption, reduce bulk refractive index, reduce capacitance and increase mechanical flexibility of large sheets of PV on semiconductor material, according to some embodiments. The Si substrate is removed leaving only the BOX/SOI layers together with the PIN epitaxially grown layers. Ohmic contacts, bond metallizations, antireflection coatings, passivations, are not shown for simplicity. In addition to PV, the techniques are also applicable to PD, APD, light emitters such as light emitting diodes and diode lasers, and to electronic integrated circuits such as CMOS and ASIC (application specific integrated circuits) where voids can not only make the material more flexible and lighter but also as mentioned earlier more resistant to cracking. The voids, according to some embodiments can be filled with a gel that can repair impact damage and seal exposed cracked edges to prevent further deterioration due to moisture for example to the semiconducting surfaces. The gel can be spin on glass for example. According to some embodiments, the voids can be filled with material to enhance thermal conductivity for example, reduction of optical or microwave losses by removing the silicon and replacing with material that is not lossy such as Ar, He, Xe, N₂, Ne gas, or vacuum for example. The voids can have different sizes and shapes and densities and can be random, pseudo random, aperiodic, periodic, chirped, single or multiple patterns. The voids can also be in a single layer or in multiple layers of the device. Fig. 30, for example, shows the voids in P-Si layer 3002, I-Si layer 3004, and N-Si layers 3006 and 3008. According to some embodiments the index of refraction near the uppermost surface can be altered to more effectively index "match" with surrounding air so as to reduce reflections of incident light. For example, in PV applications near surface voids can be used to index match such that less incident sunlight is reflected from the PV surface. According to some embodiments, the index of refraction at lower surfaces can be altered so as to increase internal reflections that may, for examples, increase the number of passes light makes through an absorbing region.

[00223] According to some embodiments, random voids can also be generated by dry etching/electrochemical etching the surface of the semiconductor without any mask. Generating semiconductor nanowires followed by epitaxial regrowth on these random nanowires will result in buried voids. As discussed in Frajtag et al,

Growing thin films that contain embedded voids, 23 June 2011, SPIE Newsroom; DOI: 10.1117/2.1201105.003750, this method can be used in GaN light emitting diodes to minimize defect formation due to lattice mismatch of the GaN epitaxial layer with the substrate which can be sapphire, Si, SOI, IOS to name a few. The random formation of semiconductor nanowires by dry etching of the surface of the semiconductor (which can be Si, Ge, III-V material family such as InP, GaAs, InGaAs, InGaAsP, GaN, InGaN, InSb, to name a few) without any mask and subsequently regrowing on the nanowires epitaxially using CVD for example, to form random buried voids can also be used to reduce the effective refractive index of the semiconductor and reduce the effective capacitance of the P-I-N, P-I-P-I-N diodes if the voids are formed in the "I" absorption layer and/or P, N layers, and/or charge, multiplication layers of the PD, APD, in any combination to optimize the performance of the device in bandwidth, QE, and energy consumption.

[00224] Fig. 31 is a cross section showing regrown I-Ge with a buried/embedded voids, according to some embodiments. The regrowth of Ge 3104 epitaxially on Si microstructured pillars and/or holes results in voids 3102 in the Ge layer that can be intrinsic or non-intentionally doped or low doped using the method shown in FIGs. 27-28, *supra*. In addition, selective masking with dielectric such as SiOx, SiNx for example can be used to generate nanowires only in the selected areas such as the Ge regrowth, for example, and with additional regrowth of Ge, random voids can be buried only in the selected Ge areas. The random voids can be combined with patterned voids to optimize a device performance in terms of bandwidths, quantum efficiencies and power consumption. The microstructures shown in FIG. 31 combine the Ge microstructure and void microstructure to enhance to bulk absorption coefficient and reduce the effective capacitance of the diode.

[00225] Fig. 32 is a cross section showing a device having buried microstructured voids in I-Si with regrown I-Ge and capped by an epitaxial layer, according to some embodiments. As can be seen in FIG. 32, the buried/embedded microstructure voids 3202 can be in I-Si layer 3200 while the Ge microstructure 3104 is also buried/embedded in Si layer 3200 using a few additional processing steps. First the voids 3202 are buried/embedded as in FIG. 28 with or without the P-Si anode layer 3226. Microstructures are then again

etched into the I-Si layer 3200 with the voids and then Ge 3104 is regrown resulting in a microstructure with voids 3202 in the Si layer 3200 and a Ge microstructure 3104 to enhance the bulk absorption coefficient and reduce the capacitance of the diode. Not shown is that the microstructured voids can also be buried/embedded entirely in Ge for Ge on Si layers, such that in Fig. 28, if the I-Si layer 3200 is replaced with I-Ge followed by a P⁺ Ge capping anode layer 3226.

[00226] The buried/embedded microstructure voids is an inverse HCG structure with absorption, or a lossy HCG structure, and can have resonance, constructive and destructive optical interference effects of both phase and amplitude that can result in the enhancement of the bulk absorption coefficient. The period of the microstructure pillar, hole, void, buried/embedded Ge arrays can fall in the near-wavelength regime of the HCG effect or it can fall in the subwavelength regime where the grating period is much less than a wavelength and the diffraction regime where the period is greater than a wavelength. The HCG characteristics of the microstructure array and the input optical signal can be coupled to in-plane optical modes. The microstructured arrays can also behave as a lens to mode match the incoming optical signal. Good coupling efficiency also improves the overall QE of the PD/APD. According to some embodiments, a lossy HCG is provided where the absorbing region is a part of or included in the HCG structure (other effects such as scattering, near field, plasmonic, resonance, linear and non-linear optical effects to name a few, can also play a significant role in absorption enhancements), and where Si can be the HCG for photon energies that are below the Si bandgap and the Ge microstructures are buried or embedded within the Si that is absorbing to the photons with wavelength ranging from 950-1800 nm (where Si has relatively low optical losses).

[00227] According to some embodiments, the microstructures of holes, pillars, and voids can be arranged in any pattern or no pattern in the active area, including any parts of the P-I-N structure of a PD or P-I-P-I-N structure of an APD; the active area includes the absorbing "I" region and the P and N regions. According to some embodiments, to simplify manufacturing and to improve yield, the microstructures can extend outside the active areas of a PD/APD if it does not interfere with the PD/APD operations and performance. FIG. 33 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some

embodiments. The microstructure array 3300 consists of pillars, holes, and/or voids, and buried/embedded Ge in Si or Si in Ge or any combination of multiple semiconductors, can be distributed over the entire active area 3302 of the photodiode or avalanche photodiode or just partially for example in the center

5 where the optical intensity is the highest. The active area can be defined as any area that contributes to the generation of electrical signal upon illumination with optical signal, or in the case of a PV, the generation of electricity upon illumination with photons. In FIG. 33, the active area 3302 is commonly the area within the metal ohmic contact/bond metal ring 3304. The distribution of the array 3300 can
10 be non uniform, non periodic, non uniform is size of the microstructure, or in shape.

[00228] FIG. 34 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some other embodiments. In FIG. 34, the QE is optimized at the center of the active area where the optical intensity is the highest and away from the center, more semiconductor material is
15 removed in the microstructure pattern to reduce the capacitance of the active area in order to decrease the RC (resistance, capacitance) time constant to achieve higher bandwidth for the PD/APD and or to increase the active area to allow passive alignment of the optical signal to the PD/APD thereby reducing the cost of packaging and assembly. Microstructured pillars/holes/buried voids 3400 near the
20 center of the PD/APD optimize QE while the microstructured pillars/holes/buried voids 3410 at the periphery of active area 3402 minimize capacitance while still maintaining good QE.

[00229] Buried voids in the N (or P if P and N are switched) part of the P-I-N or P-I-P-I-N diode structure can reduce the effective refractive index of the

25 semiconductor in the N layer. This is useful in increasing the refractive index contrast for HCG structures (to include other possible optical effects that may be significant in absorption enhancements such as scattering, plasmonic, near field, linear and non-linear optical effects to name a few), for example in Si the refractive index is approximately 3.5 (for wavelengths 950-1800 nm) and if half of the volume
30 of the material is air, then the effective refractive index ($1/2$ air and $1/2$ Si) would be approximately 1.8 for the air-Si composite material. Any semiconductor microstructures of pillars or holes fabricated on top of this composite air-Si material will have a index contrast of, for example Si pillars on the composite air-Si layer,

approximately 2. The high index contrast would enhance the performance of the HCG. According to some embodiments, this is used to enhance the lossy HCG performance (where loss can be as high or higher than - 1 dB/cm) and enhance the absorption coefficient with its resonance, light concentration and in-plane light coupling effects to name a few. There is an advantage in having the voids in the N and or N⁺ layers since it will have a minimal effect on the electrical properties and characteristics of the diode since once electrons are swept into the N and or N⁺ layer, they are majority carriers.

[00230] The microstructured voids in the N and or N⁺ layer can be patterned, non-patterned or random or pseudo-random, and can be defined using lithography, masking and etching or just etching followed by a regrowth of Si, or Ge or any other material. The voids can range in length approximately from 0.01 to 10 micrometers and lateral dimensions can range approximately from 10-5000 nm with spacing between adjacent voids ranging approximately from overlapping to 5000 nm.

[00231] Fig. 35 shows the basic epitaxial structure 3500 for a conventional Si PV/PD diode on N Si substrate. FIG. 36 shows the structure of FIG. 35 with microstructured voids incorporated into the N-Si layer, according to some embodiments. The doping and thickness of the layers are dependent of the applications. For high bandwidth PD applications the "I" Si thickness ranges from 0.1 to 3 micrometers whereas for PV applications the "I" Si thickness ranges from 1 to 20 micrometers with doping range of intrinsic or not intentionally doped, background doping of $< 5 \cdot 10^{16} \text{ cm}^{-3}$. Device size to define the area of the capacitance for high bandwidth PD (for circular apertures) ranges from 5 to 100 micrometer diameter whereas for PV, the lateral dimension can range from 0.1 to > 50 cm (centimeters) limited only by the size of the wafer or substrate. The doping ranges and layer thicknesses for non "I" layers are similar for PV, PD and APD; P or P⁺ layer thickness ranges 0.1 to 3 micrometers P doping $> 5 \cdot 10^{18} \text{ cm}^{-3}$, N or N⁺ layer(s) thickness ranges of 0.1 to 10 micrometers N doping $> 1 \cdot 10^{17} \text{ cm}^{-3}$. The Si substrate can be N doped, low N doped or undoped.

[00232] After growing the N/N⁺ layer(s) on the Si substrate, microstructures of pillars and or holes and or nanowires are etched into the N/N⁺ layer(s) 3604 and followed by a N/N⁺ layer(s) regrowth resulting in buried voids 3622 as shown in Fig.

36. The regrowth surface may or may not need further planarization such as using chemical mechanical polishing (CMP). Some applications may have more optimal performance with a non-planar surface, for example PV that can couple sun light in multiple angles with minimal reflections (a rough surface reflect less light).

- 5 Subsequent "I" Si layer 3606 and P/P⁺ layer 3608 are grown on the N/N⁺ layer(s) 3604 with the buried voids 3622. In addition to reducing the effective refractive index, at wavelengths where Si has low loss (approximately -1 dB/cm or less), 950-1800 nm, the buried voids 3622 can be patterned into a reversed HCG and behave as a very reflective (close to 100% reflectivity) broad spectrum mirror for any
- 10 photons illuminating from the top (P side) and not absorbed in the "I" microstructured pillar/hole region on the first pass, the photons can be reflected back toward the absorbing "I" region. In addition, with the voids, the substrate may be more flexible and lightweight such that it can be more adaptable to contoured surfaces and/or for use where weight is an issue such as a solar panel, or for
- 15 mobility.

[00233] FIG. 37 is a cross section showing etched Si microstructured pillars/holes with regrown Ge covering the Si, according to some embodiments. The starting structure is the same as layers 3500 in FIG. 35. The Si microstructure pillar and/or hole arrays are etched with a depth ranging from 0.1 to 10

20 micrometers and subsequently regrown with a I-Ge layer 3702 of thickness 0.01 to 4 micrometers including according to some embodiments a 1-10 nm low temperature buffer Ge layer to account for lattice mismatch between the Si and Ge. Note that the Ge buffer may not be included for pillar hole lateral dimensions of approximately 1000 nm or less since the lattice mismatch strain at that small area

25 may not be significant to cause extensive defects to form. The lateral dimensions of the microstructured pillars 3704 and holes 3706 range from 10 to 5000 nm and spacing of adjacent elements from overlapping to 5000 nm. The P/P⁺ Si layer 3708 is left on in FIG. 37 as it may be useful in making good P ohmic contact with the ohmic metals of Ti, W, Al silicide that are 1-50 nm thick to be semitransparent or

30 transparent transition metal silicide.

[00234] FIG. 38 is a cross section showing microstructured Si pillars/holes with Ge regrowth on an N-Si layer having embedded microstructured voids, according to some embodiments. The structure shown in FIG. 38 is similar in starting

material as shown in FIG. 36. The buried voids 3822 in the N/N⁺ layer 3804 act to reduce the effective refractive index of layer 3804. The voids spacing and lateral dimensions can be subwavelength ($< \lambda$) or even deep subwavelength ($<< \lambda$) to minimize optical scattering loss such as Rayleigh scattering which is proportional to λ^{-4} where λ is the wavelength. The wavelength of interest range from 300 to 1800 nm.

[00235] FIG. 39 is a cross section showing partial coverage I-Ge on microstructured Si pillars/holes, according to some embodiments. In the variation of the microstructure shown in FIG. 39, instead of regrowing I-Ge over the entire Si microstructured pillars and holes, it is only grown on part of the Si microstructures. Part of the Si microstructure is without I-Ge and the other part has regrown I-Ge. The partial regrowth of Ge can be accomplished by partially covering the Si microstructure with a dielectric such as SiO_x or SiN_x by directional deposition such as electron beam evaporation deposition, or directional laser ablation deposition or other directional methods such as ion milling to remove native oxide of Si selectively or ALD thin layer of oxides/nitrides and removing selectively and directionally with ion beam milling. Once the Si microstructure is partially coated with an oxide or nitride (or other dielectric such as CaF_x, TaO_x, TiO_x, to name a few) Ge epitaxial regrowth will predominantly occur where there is lattice information such as a Si surface. The I-Ge regrowth 3902 thickness can range from 0.1 to 4 micrometers or more. The Si microstructure of pillars 3904 or holes 3906 can have a depth of 0.1 to 10 micrometers and a lateral dimension of 10 to 5000 nm and spacing between adjacent microstructures of overlapping to 5000 nm. Both Si and Ge microstructures are exposed to photons with wavelengths ranging from 300-1800 nm from photons impinging from the anode surface and impinging on the sidewalls of the microstructure directly, scattered, near field, resonance, HCG effect, linear and non-linear optical effects, and with enhanced absorption coefficient. Both Si and Ge will generate photocurrent due to the incident photons. The Si current generator and Ge current generator are in parallel and the total photocurrent generated by this PD/PV is the sum of the Si and Ge photocurrent generators. The buried voids 3922 reduce the refractive index of the N/N⁺ layer 3914 and improve the index contrast of the microstructure and the substrate thus improving the performance of the lossy HCG for enhancing the absorption

coefficient. The voids 3922 in the Si 3914 can also behave as a good reflector to reflect photons back toward the "I" absorbing layer for a double pass (for photons illuminating from the top side). BOX or SOI 3912 can also be used in addition with the buried voids or without the buried voids, as the refractive index of SiO₂ is approximately 1.54, roughly half that of silicon at infrared and near infrared wavelengths.

[00236] FIG. 40 is a cross section showing the basic components for a microstructured Si-Ge pillar hole array PD/PV and/or APD, according to some embodiments. Note that the APD multiplication layers are not shown for simplicity.

Only the very basic parts of the device is shown. After processing steps shown in FIG. 39 are completed, surface passivation is carried out using thermal oxide or ALD or PECVD or CVD deposition of oxide or nitride to passivate or SiGe as a passivation layer on Ge. A filler 4002 is spun on or deposited such as spin-on-glass, or SiO_x, SiN_x by PECVD or CVD. Using RIE to etch back to expose either the Ge or P/P⁺ Si (during i-Ge epitaxial growth, the P dopant in the P/P⁺ Si may diffuse into the Ge layer to also result in a P/P⁺ Ge layer). Ge and or Si P- ohmic material may be Al, W, AuGe, Au, Au/Ti and Al, TiN, Pt, transition metal-silicide respectively; ohmic contacts to P and N semiconductors are well known in the literature and art and these are only a few examples of possible ohmic contacts. A transparent conducting oxide (TCO) 4004 such as indium tin oxide (ITO) may be used to further reduce the series resistance of the anode. For microstructured holes, since the P/P⁺ layers are contiguous, TCO 4004 may not be used and only a perimeter (ring for circular apertured PD/APD/PV) border ohmic contact and metallization 4006 may be used instead to reduce series resistance of the ohmic contact, such as Al, Au/Ti. Cu, to name a few. Anti-reflection layers are not shown for simplicity. N ohmic material can be used on the substrate or on the N/N⁺ layer together with metallization. Al, Pt, transition metal silicide, followed with Al or Au deposition (e-beam, sputter, thermal evaporation) on the ohmic contacts reduce series resistance. Ohmic contacts normally use an annealing process that is well known in the art. Bond and/or connecting metallization 4006 is deposited (using standard processing methods) to complete the PD/APD/PV device. Sunlight/optical signal is illuminated from the top (anode) of the device normal to the surface or at any angle off normal and may be rotated to optimize the QE. At wavelengths where

Si is low loss (950-1800 nm or more) the buried voids can both reduce the effective refractive index of Si and act as a reflector to reflect photons that are not absorbed back toward the absorbing region. The surface of the N/N⁺ layer 3914 can be non-planar to help diffuse the reflected photons to optimize its absorption in the

5 microstructured Si and Ge array. A contact pad 4008 can be provided, for example, on the side of layer 3914 as shown. Although many of the embodiments show the microstructures of Si and Ge, Si, Ge are normal to the surface (vertically aligned) and straight, according to some other embodiments if the N/N⁺ surface is non-planar, subsequent layers may also be non-planar. Etching (wet chemical or
10 dry RIE, DRIE) may result in microstructures that are off normal and not straight (with bends) which may further improve the absorption of photons. Due to the non-planar topology of the surface, the microstructures may have various orientations depending on the orientation of the crystal within the same device. The different orientations of the microstructures are advantageous to capturing photons that may
15 be illuminating the surface of the device at different angles, for example for PV as the sun changes position in the sky and for PD/APD for applications where multiple optical signal may illuminate the PD/APD from different angles/directions.

[00237] Microstructured Si pillar and/or hole arrays/pattern/random PD shown in FIG. 5, *supra*, can also have buried voids in the N/N⁺ layers as shown in FIG. 10 to
20 both reduce the refractive index of Si so that the microstructures of Si pillars/holes are more optimized as lossy HCG by increasing the refractive index contrast and also as a HCG reflector in Si for wavelengths where Si has low loss, 950-1100 nm for this application as a wide bandwidth (> 5 Gb/s) PD or as a PV.

[00238] The Si substrate in all the embodiments described herein can be either
25 Si with doping, not intentionally doped, low doping, or buried oxide (BOX) or silicon on insulator (SOI) where the silicon layers again can be doped, heavily doped, lightly doped or not intentionally doped. The BOX and SOI layers allow the removal of the all or almost all of the Si substrate to reduce optical losses, increase mechanical flexibility and also the refractive index of SiO₂ in BOX and SOI have
30 refractive index of approximately 1.54 in the infrared and near infrared wavelengths which is roughly half of silicon refractive index. The low index of SiO₂ also improves the performance of HCG, or the silicon dioxide layer can be removed for bottom illuminated PD/APD/PV.

[00239] FIGs. 41A-41B are cross sections showing aspects of a microstructured pillar/hole array device above a N-Si layer having buried microstructured voids, according to some embodiments. The bulk layers 4100 shown in FIG. 41A include I-Si layer 4112 and N-Si layer 4110. Microstructured voids 4102 are formed in the N-Si layer 4110 using techniques such as described herein *supra*. The structures in FIGs. 41A and 41B are a version of the PDs/PVs shown in FIGs. 25A-B but with buried voids 4102 in the N/N⁺ layer 4110 to improve the refractive index contrast for lossy HCG (microstructures of Si and Ge) and to provide a reflector low loss HCG for photons. Pillars 4124 and/or holes 4122 arrays are formed in I-Si layer 4112. I-Ge is regrown in the etch region 4122 resulting in a buried/embedded Ge "I" layer with microstructure voids 4102 in the N Si layer 4110 to reduce the effective refractive index of Si and/or to reflect photons entering from the anode surface at wavelength where Si is low loss (950-1800 nm). Cap layer 4126 can be P-GE or P-Si regrowth. In the case of bottom illumination, an anti-reflection coating 4130 may be provided.

[00240] FIGs. 42A-42D are cross sections showing aspects of an APD with microstructured pillar/hole arrays above an N-Si layer having buried microstructured voids, according to some embodiments. The APDs shown in FIGs. 42A-42D are versions of the APD shown in FIGs. 24A and 24B, *supra*, except that buried voids 4202 are included in the N/N⁺ layer 4210 to improve the refractive index contrast for lossy HCG (microstructures of Si and Ge) and to provide a reflector low loss HCG for photons. According to some embodiments, BOX/SOI Si wafers can also be used with or without buried voids to improve refractive index contrast for optimal HCG lossy operation. Only the basic structures are shown for simplicity. Electrical isolation, passivations, ohmic metallization, anneal, anti reflections, bond/interconnect metallization, guard rings, to name a few are not shown. FIG. 42A shows the bulk layers 4200, which include N-Si layer 4206, I-Si layers 4208 and 4212 and P-Si layer 4210. Microstructured voids 4202 are formed in the N-Si layer 4206 using techniques such as described herein *supra*. As in the case of FIG. 41B, I-Ge is regrowth in the etched area 4222. The voids 4202 are to reduce the effective index of the N-Si since the optical field will be an average effective refractive index composing of air and Si. If the voids 4202 are patterned for HCG effect, photons can be reflected that are not absorbed in the first pass

through the "I" absorbing region 4212 for photons illuminating the APD 4220 from the top or anode surface. The APD can also be illuminated from the bottom or cathode side.

[00241] FIGs. 42C and 42D show another variation of an APD 4230 in which
5 voids 4204 are formed in the I-Si multiplication layer 4208 as well as in N⁺ layer 4206 to reduce the effective refractive index and capacitance of those layers. Note that the elongated nature of the microstructured voids will have a minimal effect on charged carrier transport in the semiconductor materials. According to some
10 embodiments, voids of various shapes and densities can be formed in the P anode, N cathode, P charge, and/or I multiplication layers of the APD in addition to the absorbing I layer. The addition of voids in the I multiplication layer 4208 and the I absorption layer 4212 can reduce the effective capacitance resulting in a short RC time constant for the device. The voids 4204 in the multiplication I Si layer 4208
15 also reduce the effective refractive index, which is helpful in enhancing the absorption coefficient in a HCG absorbing mode.

[00242] Epitaxial growth/regrowth/overgrowth/selective area growth/epitaxial lateral over growth of Si, Ge, SiGe, III-V such as InP, GaAs, GaN, InGaN, InGaAs, InGaAsP, InSb, heteroepitaxy, homoepitaxy, heterogeneous epitaxy to name a few, using chemical vapor deposition (CVD), metallic organic chemical vapor
20 deposition (MOCVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE), gas source molecular beam epitaxy (GSMBE) plasma enhanced chemical vapor deposition (PECVD), laser ablation deposition (LAD) to name a few, are well known in the art.

[00243] According to some embodiments, material other than Si and Ge on Si
25 are used. For example, the techniques described herein can be applied to all combinations of Si, Ge, III-V and II-VI material families and substrates.

[00244] FIGs. 43-46 are top views illustrating various dimensions, spacings and shapes for microstructured elements, according to some embodiments. FIG. 43 shows a microstructured pillar and/or hole array 4300 (also applicable to
30 embedded or buried voids) that is uniformly spaced with a fixed diameter ranging from 100-5000 nm and a spacing ranging from 100-10000 nm. The pillars and or holes can be formed in or using: Si, Ge, SiGe, or other materials such as III-V or II-VI material family. Examples includes: GaAs, InP, InGaAs, InGaAsN, InGaAsP,

InAs, GaN, InGaN, ZnTe, CdS, ZnSe, and HgTe. According to some embodiments, the microstructures can also be formed in or using absorbing polymers, glass, and/or ceramics.

[00245] FIG. 44 shows a microstructured pillar and/or hole array 4400 having a fixed diameter but with non-uniform spacing such as aperiodic or a mixture of periodic and aperiodic or random/pseudo random spacing or a mixture of random/pseudo random, periodic and aperiodic. According to some embodiments, the arrays can also be uniformly spaced periodic but with varying diameter. FIG. 45 shows a microstructured pillar and/or hole array 4500 having both variable diameters (ranging from 100 nm to 5000 nm) and variable spacing (ranging from 100 nm to 10000 nm). According to some embodiments, the variations can be random/pseudo random, or a pattern or a mixture of patterns or any combinations thereof. FIG. 46 shows a microstructured pillar and/or hole array 4600 having various shapes such as oval, circular, rectangle, doublets, triplets, and stars. In general, any shape that can be generated using a photolithographic mask, or e-beam direct write or that can be generated with a mold for imprint lithography, can be used. The pillar/hole arrays can also have a combination of different shapes and spacings, as well as variations in the depth of the microstructured holes or lengths of the microstructured pillars/mesas. The variations can be periodic, aperiodic, or random (or a mixture of periodic, aperiodic and random) within a single array.

[00246] According to some embodiments, for some applications an array dimension of Si or Ge or III-V microstructured pillars or holes of length 2 μm approximately (or depth of 2 μm approximately) with diameter of pillar/hole of 390 nm approximately and center to center spacing of 1060 nm approximately has been found to be suitable for enhancement of the absorption coefficient of greater than 50X.

[00247] According to some embodiments, the material can be Si, Ge, SiGe, Ge on Si, III-V, II-VI, III-V on Si, polymer, glass, ceramic and any combination thereof. Examples of III-VI and II-VI are InP, GaAs, AlGaAs, AlAs, AlInAs, InGaAs, InGaAsP, InAs, InGaAsN, InN, GaN, InSb, ZnSe, ZnTe, HgTe, and CdS. Also III-V, II-VI and group IV material such as Ge can be embedded in Si microstructures using SAG, VLS, ELOG growth methods in MOCVD, CVD, MBE, reactors.

[00248] FIGs. 47-48 are cross sections showing microstructured pillar and hole arrays having varying lengths and depths, according to some embodiments. FIG. 47 shows a microstructured pillar array 4700 having different lengths, diameters and spacing. According to some embodiments, the pillar diameters range from 10 nm to 5000 nm and the pillar heights range from 0.1 to 10 microns. FIG. 48 shows a microstructured hole array 4800 having different depths, diameters and spacings. According to some embodiments, the holes have diameters ranging from 10 nm to 5000 nm and depths ranging from 0.1 to 10 microns. The variation in lengths and etched depths can be accomplished by additional lithographic masking steps where regions are masked for longer etch or shorter etch to vary the length of the pillars and the depth of the holes. The lengths and depths can be gradually or sharply varied. A patterned grating effect can be used to further optimize the optical path lengths and increase the enhancement factor for absorption coefficient. Other uses include forming a light trap by using constructive and destructive optical interference, generating a fresnel lens, matching the mode of the optical signal, forming a filter in wavelength selectivity in wavelength division multiplexing for example, or as a wavelength selector for spectroscopy and sensor applications. It should be noted that by varying the dimensions and spacing of the microstructured pillars and holes in an array can also result in constructive and destructive optical interferences that can also increase the enhancement factor of the absorption coefficient, improve light trapping, create fresnel lens, mode matching of radiation patterns of the optical signal.

[00249] FIG. 49 shows shows a microstructured surface having a combination of both pillars and holes, according to some embodiments. Microstructure array 4900 includes pillars and holes co-existing on the same microstructured surface either globally or locally. Both pillars and holes can exist in a single array (such as shown in FIG. 49) for the microstructured photodetector, or holes and pillars can exist on separate arrays for different microstructured photodetectors. In addition, hole(s) can exist in a pillar and pillar(s) can exist within a hole and these also can be global or local. The pillars, holes, hole(s) in pillar and pillar(s) in holes can have any shape, for example a rectangular pillar within a round hole, can have any mixture thereof to optimize enhancement of the absorption coefficient, light trapping, constructive and destructive optical interference, scattering, near field effects,

linear and non-linear optical effects, subwavelengths effects, fresnel lens, wavelength selection, optical mode matching, diffraction, high contrast grating, blazed grating, high Q resonator, highly reflective mirrors using high contrast grating.

- 5 **[00250]** The microstructured pillar and hole (and variations thereof) arrays can be fabricated in Si, Ge, Ge on Si, SiGe on Si, SiGe on Ge. The array structure can be any combination of Si, Ge and SiGe. The array can be entirely Si or Ge or SiGe, or Ge on Si, or Si on Ge, or Ge on Si with SiGe on both. The structure can also include III-V and II-VI material systems together with Si, Ge and SiGe and any
- 10 combination of Si, Ge, and III-V, II-VI material systems. According to some embodiments, the array structure can also include polymer, glass, oxides, nitrides, sulfides and chlorides of transition metals, ceramics, quartz, SOI, IOS, organic conducting and non conducting polymers, carbon based material such as graphene to name a few.
- 15 **[00251]** The microstructures pillars, holes, voids, and any other shapes such as pyramids, microwires, nanowires, multiple materials, SAG microstructures, can have orientations that are not perpendicular to the surface of the substrate. They can have a single or multiple orientations that can be perpendicular and or off perpendicular to the surface. They can be random or pseudo random, single
- 20 pattern or multiple pattern orientations at any angle where angle can range from 0 to 90 degrees with respect to the normal to the silicon substrate, and they can be on sidewalls and on all three dimensions. With the microstructures at certain orientations, the photosensor can have a higher sensitivity to certain direction of illumination. Conversely, with multiple orientations and or random or pseudo
- 25 random orientations the photosensor can be mostly insensitive to direction of illumination.

- [00252]** Reducing the effective refractive index with buried voids in semiconductor has applications beyond PD/APD and PV devices. It also, for example, has applications in optical waveguides. FIG. 50 is a cross section of an
- 30 optical ridge waveguide, according to some embodiments. Waveguide 5000 uses the density of voids to alter the effective refractive index of Si. According to some embodiments materials other than Si are used, for example other semiconductors such as Ge, SiGe, any of the III-V semiconductor family, or other material such as

ceramics, glass, polymer. In Si photonic optical waveguide 5000, the ridge 5002 and slab 5004 are made of Si on a BOX (buried oxide) Si substrate 5006. Due to the high refractive index of Si. 3.49 at 1100-1800 nm wavelengths, the dimensional tolerance of the solid Si waveguide is very critical. Known Si photonic components

5 are difficult to manufacture and have low yield and are temperature sensitive. According to some embodiments, voids are buried in the Si layers. By varying the density of the voids, the refractive index of the composite Si-voids can be adjusted. In the schematic diagram of FIG. 50, a ridge waveguide 5000 has voids 5014 on slab 5004, as well as voids 5012 on ridge 5002. The density of voids 5012 in the

10 ridge 5002 is less than the density of voids 5014 in the slab 5004. The refractive index in the ridge 5002 is therefore higher than the refractive index in the slab 5004 resulting in a ridge optical waveguide. The optical mode of the waveguide 5000 is indicated by the dotted oval 5022. The lower refractive index helps in reducing the dimensional tolerance and the optical waveguide can have a larger dimension.

15 Thus, according to some embodiments, the refractive index can be varied by varying the void density making other components such as couplers easier to manufacture. The dimensions of the voids can be subwavelength ranging from 10nm to 1000nm depending on optical wavelengths.

[00253] According to some embodiments, voids are also buried in a silicon wafer

20 (including BOX/SOI silicon wafers) to adjust the effective refractive index of the Si wafer. The Si wafer with buried voids can then be the starting platform for silicon photonic circuits. It can also be the platform for large area PV cells that allow mechanical flexibility but still retain the high quality of silicon and its electrical characteristics. This can also be the platform for flexible displays and other

25 electronics that require mechanical flexibility and or light weight. According to some embodiments, burying or embedding voids is not limited to just Si, but can include Ge, GeSi, amorphous semiconductors, III-V, II-VI material families, polymers, glass, quartz, metal, alloys, ceramics and any other material that requires flexibility. In some embodiments, the voids can be filled with gas, liquid or solid for specific

30 applications. Gel such as spin on glass that does not require anneal for example can be used for impact/crack situations where the integrity of the device is compromised such as a crack due to impact, to seal surfaces such as semiconductors or any surfaces sensitive to environment such as moisture, water,

oxygen to name a few to prevent further deterioration. Voids are also excellent in preventing crack propagation.

[00254] FIG. 51 is a cross section of a buried optical waveguide in silicon using voids, according to some embodiments. A composite waveguide 5100 is formed in
5 Si substrate 5106 using Si-voids to selectively alter the effective refractive index in certain locations. The effective refractive index of Si can be adjusted precisely by adjusting the total volume of the voids in a given volume of Si. In the example shown in FIG. 51, the higher density voids 5114 surround a central region of lower density voids 5112. The optical mode of the waveguide 5100 is indicated by the
10 dotted oval 5122.

[00255] According to some embodiments, the dimension and spacing of the voids are optimized to reduce scattering losses and to provide ease of manufacturing. Also, the void dimensions and spacing can be adjusted for certain applications. For example, in HCG the dimensions and spacings are selected to
15 satisfy the near field regime where the dimensions and spacing lie approximately between the wavelength in the high refractive index material and the wavelength in the low refractive index material. In most cases, in the applications to reduce the effective refractive index, the void and the surrounding material dimensions and spacing are in the subwavelength regime where the microstructures containing the
20 voids are less or much less than the wavelength in either the high or low index material. For coupling applications, the diffraction regime may be the microstructure (voids and material) dimensions and spacing. It can also be a mixture of two or more regimes to optimize a device performance.

[00256] Array patterns can include microstructure ensembles whose distribution
25 of individual microstructures can be periodic, aperiodic, chirped, random, pseudo-random, uniform, or non-uniform in all three dimensions, orientations and spacings, (including overlapping). According to some embodiments, the patterns can include microstructures within microstructures. The terms "array" and "pattern" are used herein interchangeably.

30 **[00257]** The PD/APD are biased between the anode and cathode, to extract a broadband modulation signal greater than a gigabit per second (Gb/s) at a typical transmission line impedance is 25-50 ohms. According to some embodiments, the external bias is provided with a bias-tee connected to the transmission line to block

the RF signal from reaching the DC power supply and to block the DC from biasing the transmission line away from the PD/APD. The bias-tee basically consists of an inductor and capacitor, the inductor to block the RF and the capacitor to block the DC away from the PD/APD. External bias of -2 to -30 volts is applied depending on
5 the application, PD or APD and performance desired.

[00258] In PV mode, no external bias is applied and the PV is basically a current generator. All the electrical connections are for DC current from the PV which then connects to a converter that converts the DC current/voltage to AC current/voltage.

[00259] PV devices are in DC mode whereas PD/APD for data and tele
10 communication are all RF with modulation bandwidth ranging from 1 to 100 Gb/s. Transit time of carriers and capacitance are critical in PD and APD but not so much for PV.

[00260] The terms "modulation bandwidth" and "bandwidth" are interchangeable as used herein. Both terms refer to the modulation (e.g. of a laser or LED) where
15 an RF signal is impressed on the light. When this modulated light (also referred to as "optical signal") illuminates the PD/APD, the RF modulated signal is extracted and converted from light to electrical signal. For example, a bandwidth or modulation bandwidth of a PD/APD of 20 Gb/s means that an RF signal impressed on the laser light beam at a data rate at 20 Gb/s can be converted by the PD/APD
20 from optical to electrical with good signal integrity or signal replication. The laser/LED is the transmitter and the PD/APD is the receiver where the electrical signal can be further processed by an amplifier such as a transimpedance amplifier and the signal sent for further analysis and processing in application specific integrated circuits (ASIC) computers (CPU central processing unit), routers,
25 memories, to name a few.

[00261] According to some embodiments the applications for the microstructured pillars and or holes in Si and Ge and Si regrowth with Ge, Ge on Si, with and or without buried or embedded voids photodiodes and avalanche photodiodes, are in data and tele communications. According to some
30 embodiments, these applications include: fiber to home, local area network, data center optical interconnects board to board, on the board, rack to rack, and chip to chip, between data centers, metro area network, and optical communication for distances from less than a centimeter to over 10 kilometers or more. The

applications in consumer space also includes: game box, personal computers, tablets, mobile devices such as smart phones, animations studios, and anywhere that benefits from a bandwidth of more than one gigabit per second. Other applications of the microstructured PDs and APDs, according to some

5 embodiments, are in sensors where broadband communication is important, such as sensors for infrastructures, health, environment, oil exploration, where the sensors communicate with a remote receiver that is connected to data centers for data analysis.

[00262] Other applications of the microstructured PD and APD, according to
10 some embodiments, are in analytical instruments and optical tests and measurement instruments where high sensitivity and bandwidth are important.

[00263] According to some embodiments, the microstructured PV have applications in energy harvesting for power generation all the way from gigawatts to watts, to power cities and homes to powering sensors. Since the microstructured
15 PV is lightweight and high efficiency it can be used in mobile applications, space, solar transportation, recycling of photons in home, offices and factories. The PV can also be used on windows and can be semi-transparent.

[00264] The described microstructures in Si, Ge, Si regrowth with Ge, Ge on Si, pillars, holes, and voids can be any shape and form, and are not limited to the
20 schematics shown. According to some embodiments, the dimensions range from 10-10000 nm (nanometers). The microstructures can be within each other such as pillar(s) in hole(s), hole(s) in pillar(s) and void(s) can be in the pillar, and buried and or embedded in any layer of the semiconductor heterogeneous or homogeneous. The material used includes semiconductors such as Si, Ge, GeSi, Ge on Si, and
25 the III-V group material family of InP, GaN, InGaAsP, GaAs, and other semiconductors such as ZnO, CdTe, CuInGaSe (CIGS), amorphous Si, or any amorphous semiconductor and or microcrystalline and crystalline semiconductor. The material can be a combination of amorphous, microcrystalline, crystalline heterogeneous and or homogeneous. The material used is also not limited to
30 semiconductors, but also include polymers, electrically conducting, semiconducting, non conducting polymers, organic and or inorganic polymers, glass, conducting, semiconducting, non conducting glass. Nanoparticles of semiconductors and or metal can also be buried in the polymer and glass.

Semiconductors, polymer and glass can exist within the same microstructure, separately or in any combination.

[00265] According to some embodiments, in silicon photonic circuit applications, optical waveguides such as shown in FIG. 50, *supra*, can be integrated with optical
5 sources and optical detectors such as photodiodes, avalanche photodiodes and photoconductors. FIG. 52 is a cross section of a ridge waveguide integrated with a microstructured PD/APD, according to some embodiments. Device 5200 includes a ridge waveguide that is edge coupled to a microstructured Ge on Si photodiode or avalanche photodiode (with multiplication layers added). In the ridge wave guide
10 portion, as shown in FIG. 50, a ridge 5202 has lower density voids 5212 and slab 5204 has higher density voids 5214. Ion implantation is used to increase the N doping (region 5224) for the PD and a coplanar transmission line is fabricated on the photodiode to extract the electrical signal as shown in FIG. 53, *infra*. Anode contact 5226 is made of P-Ge, according to some embodiments. The cathode
15 contact is made to layer 5224 (cathode contact not shown for simplicity and clarity of drawing.)

[00266] FIG. 53 is a top view the integrated ridge waveguide and microstructured PD/APD shown in FIG. 52, according to some embodiments. The device 5200 is in a coplanar transmission line configuration. Ridge portion 5202 is
20 0.5 to 10 μm wide and 0.1 to 10 μm deep, according to some embodiments. Slab portion 5204 has higher density voids, as shown in FIG. 52, to vary the refractive index as a platform for silicon photonic circuits. Coplanar cathodes 5228 and 5230 are in contact with the N-Si ion implanted region 5224 shown in FIG. 52. According to some embodiments, the optical field can also be coupled evanescently by
25 placing the PD/APD above the optical waveguide such that the optical field overlaps the absorbing I microstructures.

[00267] FIGs. 54A and 54B show a microwave transmission line on Si with voids, according to some embodiments. High bit rate transmission lines on silicon suffers from a multitude of effects, from slow wave to dispersion to loss. However
30 by removing most of the silicon material with the addition of high-density voids according to some embodiments, the dispersion and loss can be alleviated and signal integrity restored. An advantage is that silicon can be the substrate for both microwave transmission line and for ICs without the use of intermediate ceramic

such as alumina for transmission line to connect various IC chips. FIG. 54A is a cross section showing high density voids 5314 buried in silicon 5304 which reduce the effective dielectric constant of the silicon, and disrupt lateral electrical conductivity which in turn can result in lower microwave loss and dispersion which are important as bit rate increases into the multi Gb/s range (e.g. 40-60 Gb/s). Coplanar microwave metallic transmission lines 5310 are provided as means to move the electrical signal to/from electronic devices (e.g. processors, storage devices, input-output devices, ASICs, CPUs, and memories) on the same substrate. FIG. 54B is a top view. Conventional techniques use multi chip carriers that need additional packaging. According to some embodiments, having many devices all on the same silicon substrate greatly reduces the cost since it can be all fabricated at once and requires no additional packaging for each chip. According to some embodiments, the voids 5314 are arranged in a fashion where the path length in silicon laterally is significantly increased in order to increase lateral resistivity. According to some embodiments, Ion implantation of protons and or oxygen can be used to further increase electrical resistivity. Although FIGs. 54A and 54B show a co-planar arrangement, according to some embodiments other microwave transmission line arrangements (e.g. microstrip, slotline, and stripline) are used with a semiconductor substrate having high-density buried voids. According to some embodiments, the positioning and/or other properties (e.g. size, shape, and filling material) of the high-density voids can be selected such that the slow wave effect can be manipulated or "tuned" in a way that is suitable for the application at hand.

[00268] FIG. 55 is a cross section of voids for thermal conduction and thermal isolation of heat producing ICs and light emitters, according to some embodiments. The buried voids in silicon 5404 can be filled with thermal conductors such as helium gas, metal such as copper, aluminum, tungsten, or ceramic such as boron nitride, or carbon, graphene, diamond like carbon, or heterogeneous material/ceramic doped with metal nanoparticles, carbon nanotubes. The voids 5414 underneath the heat producing elements such as ICs and CPUs 5422, and light emitters 5420 such as laser diodes and bipolar drivers, can be filled with enhanced thermal conductors to extract the heat from the hot components and direct it to a heat sink 5402. Voids 5412 between hot elements are kept at a low

thermal conducting state that are either in partial vacuum or filled with a gas such as nitrogen, argon, carbon dioxide, for example to prevent thermal cross talk between the hot components or to any other components where heat is not desirable. According to some embodiments, the voids are arranged in a fashion
5 such that the path length in silicon is vastly increased to maintain low thermal crosstalk. According to some embodiments, the techniques of FIG. 55 are used to keep PVs cool when exposed to the sun. According to some embodiments, thermoelectric devices can be integrated together with the voids to generate electricity from the excess heat.

10 **[00269]** FIG. 56 is a cross section showing a distribution of voids to increase lateral path length for increasing lateral electrical resistivity and decrease lateral thermal conduction, according to some embodiments. The buried voids 5602 configured for microwave transmission lines and/or for thermal management can be arranged in a randomly, pseudo randomly, or in a pattern in areas where lateral
15 electrical and thermal conductance is significantly reduced and vertical electrical and thermal conductance is significantly enhanced. There may be areas where lateral electrical and thermal conductance enhancement is desired, in which case the voids can overlap to form a conducting channel.

[00270] FIGS 57A-B are simplified partial schematic top views of a semiconductor
20 surface having holes configured as trenches, according to some embodiments. The semiconductor 3010' and 3008' can be: Si, Ge, GeSi and/or 111-V material such as InP, GaAs, GaN to name a few. In this case the microstructure "holes" are "connected" to form trenches 3060' and 3062'. The microstructure hole/trenches 3060' and 3062' are further configured to crisscross the surface of the
25 semiconductors 3010' and 3008', respectively. Although the trench-shaped holes in FIGS. 57A-B are shown in straight lines, they could alternatively be formed in curved lines or a combination of straight and curved lines. The width of each trench is approximately one wavelength, and in some cases can be less than a wavelength, and in some cases wide ranging from 600 nm to 1600 nm, and can run the length of
30 of the photosensitive area. The depth of the trench can range from 100 nm to 1000 nm or more, and in some cases 50 nm to 1000 nm or more, and in some cases 100 nm-600 nm.

[00271] This patent application refers to certain theories in explaining the nature and operation of devices, but it should be clear that such theories are based on current understanding and do not affect the actual operation of the disclosed devices even if future developments prove the theories incorrect. This patent
5 specification also refers to numerical ranges of parameters, and it should be understood that insubstantial departures from such ranges are still within the spirit of the disclosed advancements.

[00272] Although the foregoing has been described in some detail for purposes of clarity, it will be apparent that certain changes and modifications may be made
10 without departing from the principles thereof. It should be noted that there are many alternative ways of implementing both the processes and apparatuses described herein. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the body of work described herein is not to be limited to the details given herein, which may be modified within the scope and
15 equivalents of the appended claims.

CLAIMS

What it claimed is:

- 5 1. An integrated, single-chip structure of plural pillars of semiconductor material formed as respective photodetectors configured to generate electrical signals in response to illumination with light including light in the infrared and/or near infrared spectrum, said structure comprising:
- 10 deliberately formed holes into said pillars, filled at least partly with solid dielectric material;
- wherein:
- parts of at least two of the holes overlap such that at a surface of each of said pillars each of the at least two holes has a portion that overlaps with another of said at least two
- 15 holes and a portion that does not;
- said at least two holes that overlap thereby form a depression in said surface that comprises a portion of only one of said two or more holes and a portion at which two of said two or more holes overlap, and
- 20 said two or more holes have:
- depths in the range of 100-10000 nm from said surface, and
- widths in the range of 100-2000 or 100-5000 nm along said surface in at least one direction;
- 25 side-isolation comprising solid material at sides of said pillars; and
- a base dielectric region under the pillars that comprises solid dielectric material;
- wherein said pillars are configured to receive said light directly or through other materials; and
- 30 wherein the presence of said holes and side-isolation increases effective quantum efficiency (EQE) of the pillars to illumination with said light relative to an otherwise same pillars lacking said holes.