

2. The integrated, single-chip structure of claim 1, wherein said at least two holes comprise at least three holes each of which has a portion that overlaps with another of said at least three holes and a portion that does not.
- 5
3. The integrated, single-chip structure of claim 1, in which said pillars comprise semiconductor material that is doped at one portion of the pillar but is less doped or is undoped at a portion of the pillar adjacent the doped portion.
- 10
4. The integrated, single-chip structure of claim 3, in which the pillars are elongated in an up-down direction and the more doped portion of each pillar is over the less doped or undoped portion thereof.
- 15
5. The integrated, single-chip structure of claim 1, further including electrical contacts to said pillars configured to provide an electrical field across said pillars.
- 20
6. The integrated, single-chip structure of claim 5, in which two or more of said pillars share one of said electrical contacts.
7. The integrated, single-chip structure of claim 1, further including active electronic circuits integrated with said pillars.
- 25
8. The integrated, single-chip structure of claim 7, in which said active electronic circuits comprises Si-based active circuits for signal processing of electrical signals generated by said pillars.
- 30
9. The integrated, single-chip structure of claim 1, in which said holes are configured as intersecting elongated trenches.
10. The integrated, single-chip structure of claim 9, in which said elongated trenches have widths no greater than a wavelength of said light at said surface.

35

11. The integrated, single-chip structure of claim 9, in which said elongated trenches run the length of photosensitive areas of said pillars.
 12. The integrated, single-chip structure of claim 9, in which said elongated trenches intersect at right angles.
- 5

ABSTRACT

Techniques for enhancing the absorption of photons in semiconductors with the use of microstructures are described. The microstructures, such as pillars and/or holes, effectively increase the effective absorption length resulting in a greater absorption
5 of the photons. Using microstructures for absorption enhancement for silicon photodiodes and silicon avalanche photodiodes can result in bandwidths in excess of 10 Gb/s at photons with wavelengths of 850 nm, and with quantum efficiencies of approximately 90% or more.

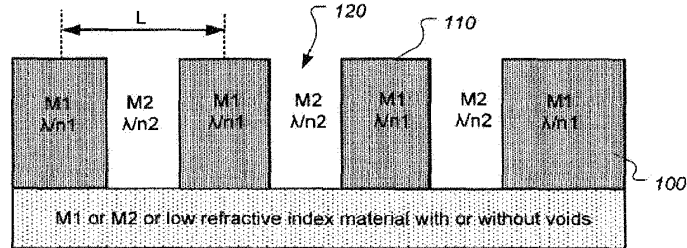
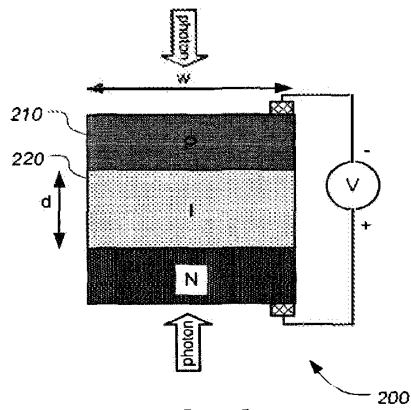


FIG. 1

FIG. 2
(prior art)

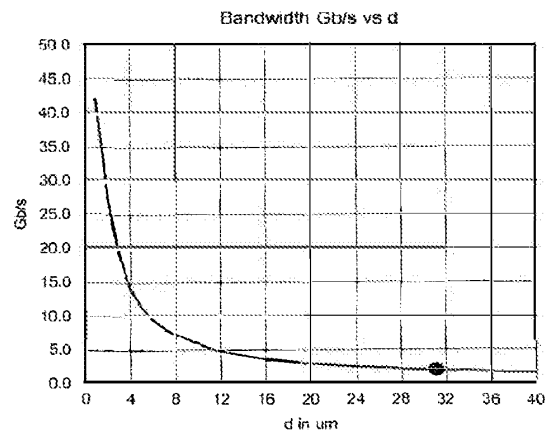


FIG. 3A
(prior art)

310

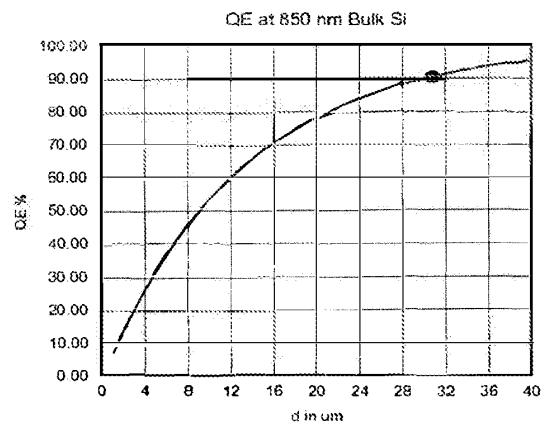
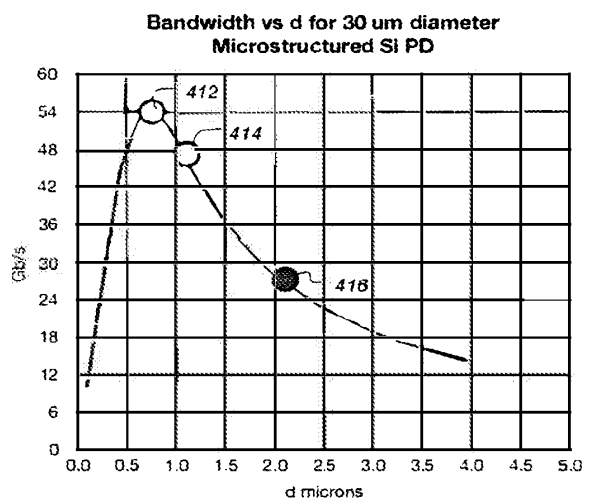
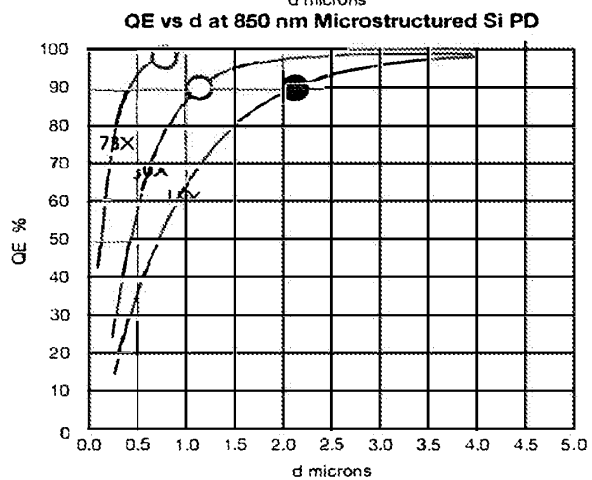
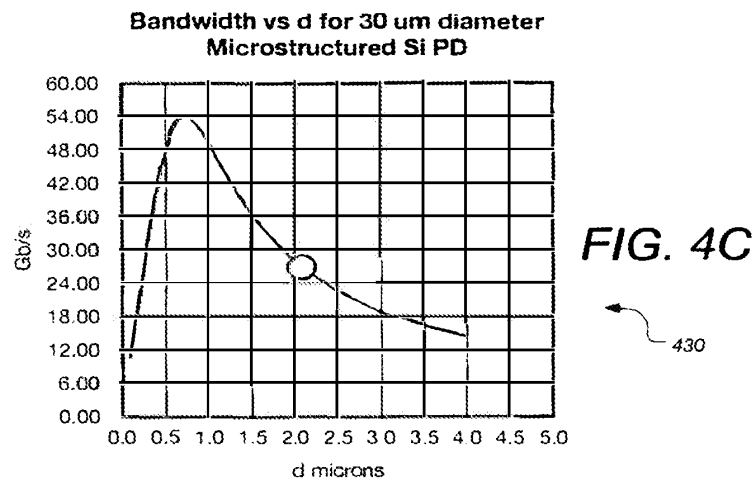
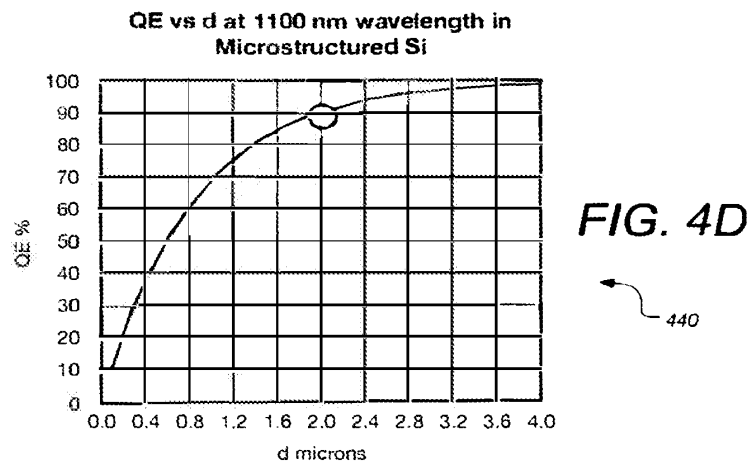


FIG. 3B
(prior art)

312





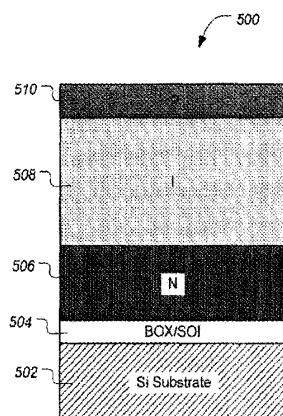


FIG. 5A

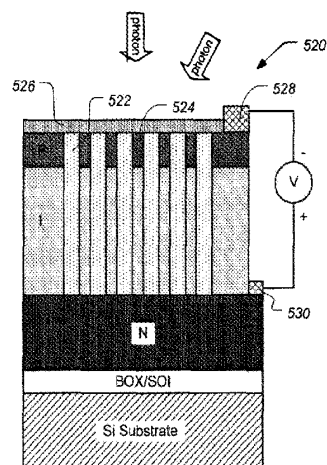


FIG. 5B

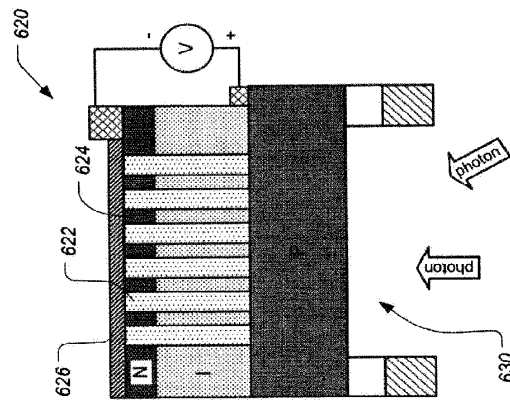


FIG. 6B

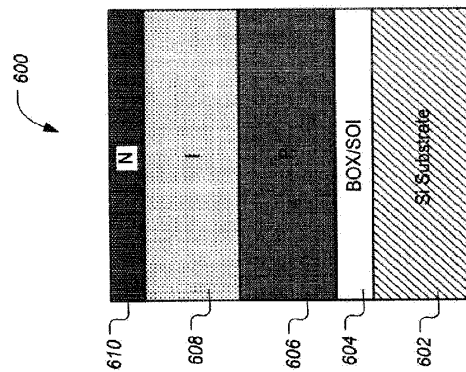


FIG. 6A

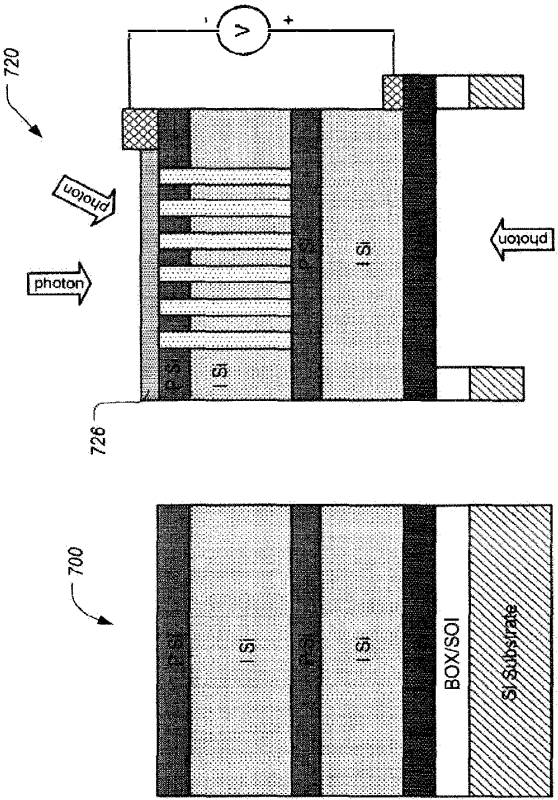


FIG. 7B

FIG. 7A

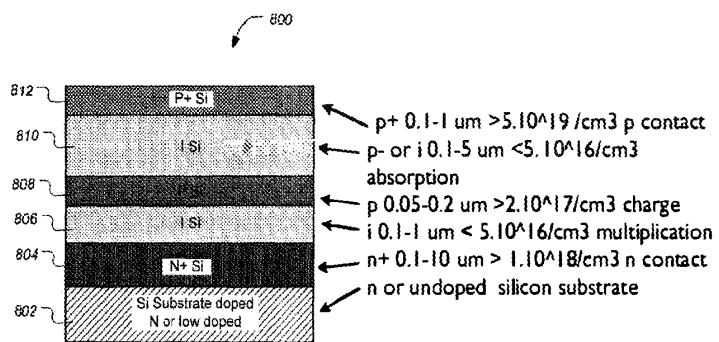
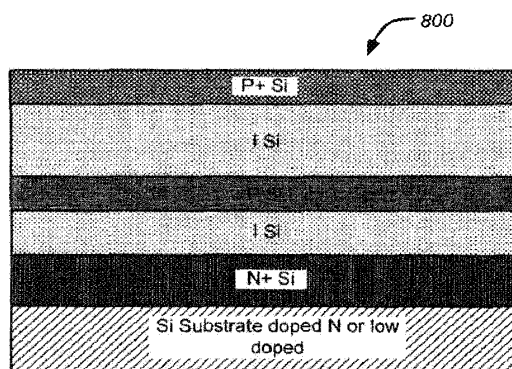
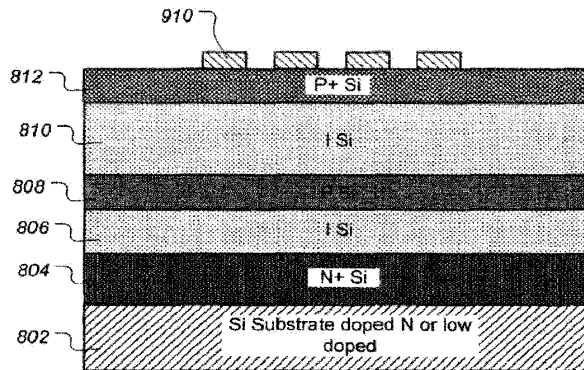
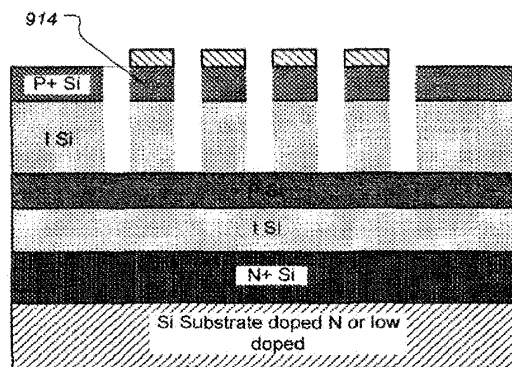
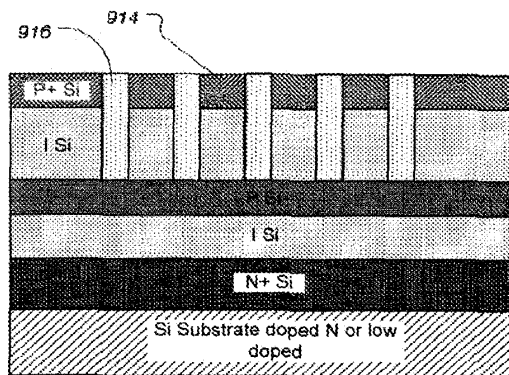


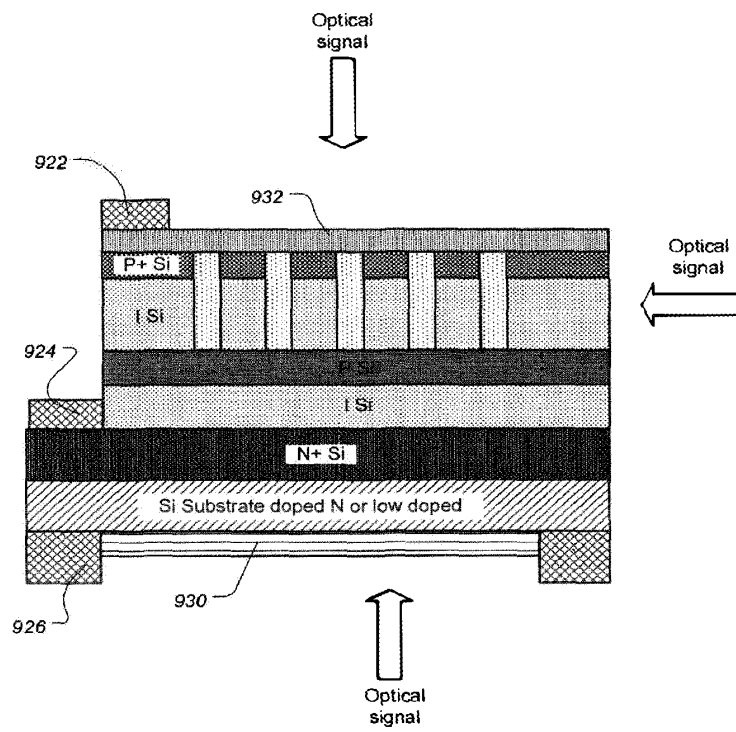
FIG. 8

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**FIG. 9A****FIG. 9B**

**FIG. 9C****FIG. 9D**

**FIG. 9E**

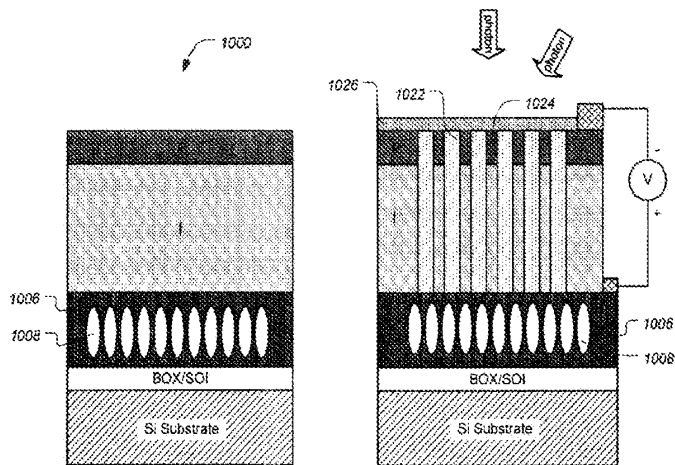


FIG. 10A

FIG. 10B

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309-00150301P

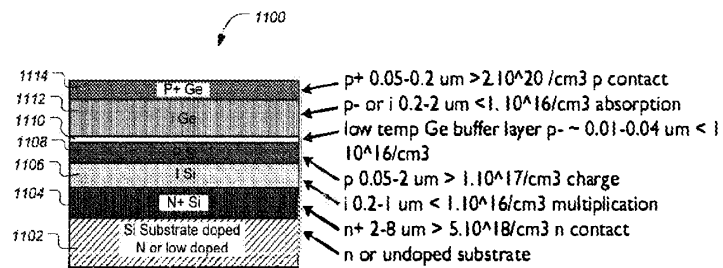


FIG. 11A

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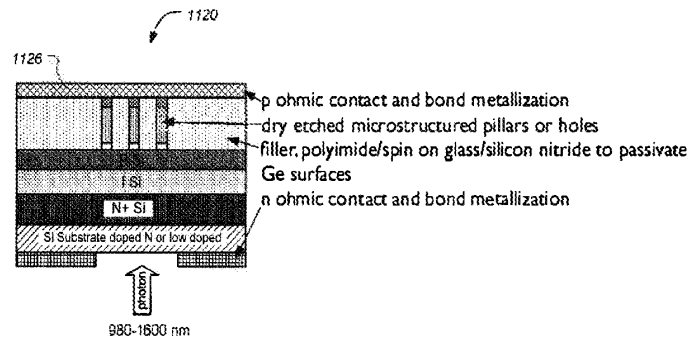


FIG. 11B

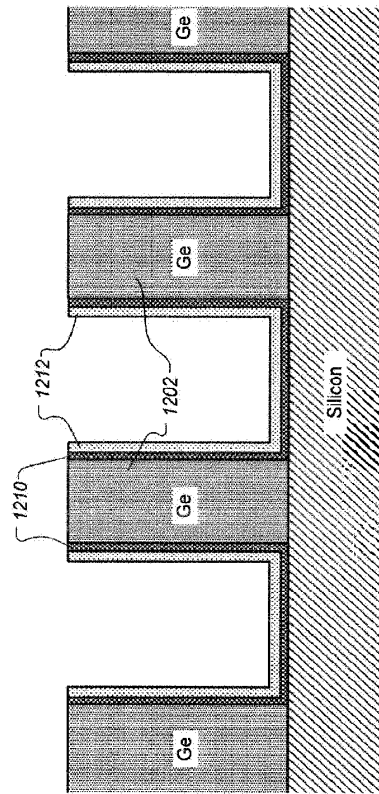
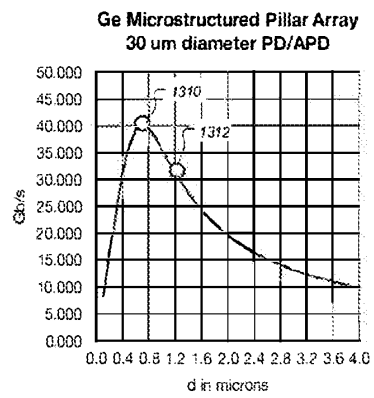
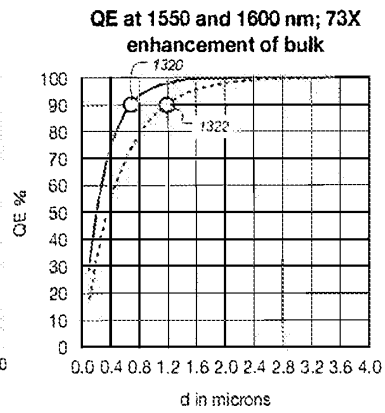


FIG. 12

**FIG. 13A****FIG. 13B**

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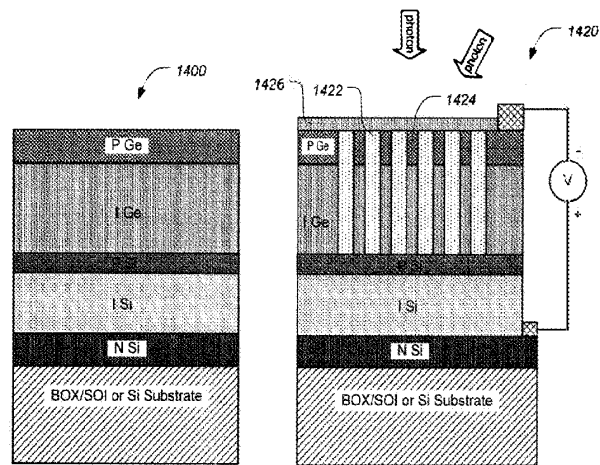


FIG. 14A

FIG. 14B

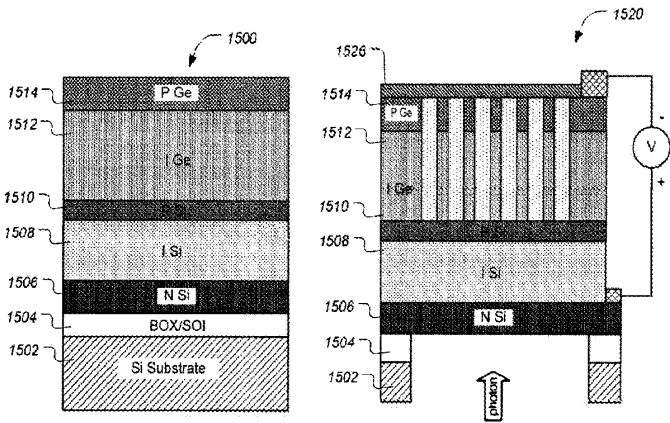


FIG. 15A

FIG. 15B

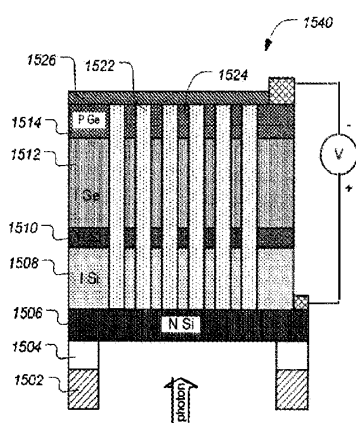


FIG. 15C

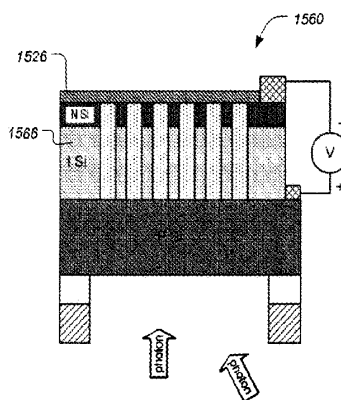


FIG. 15D

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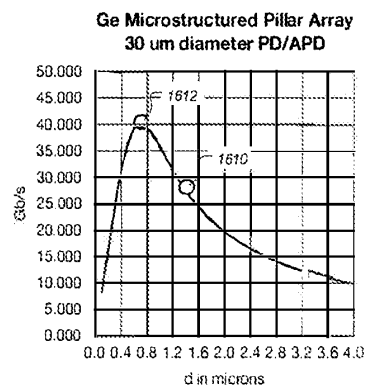


FIG. 16A

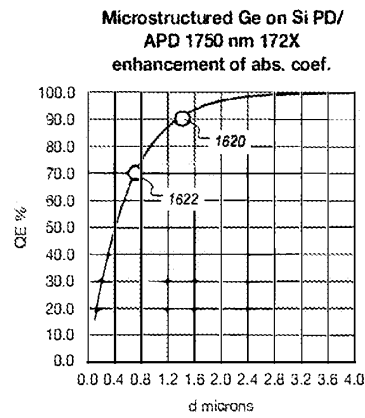


FIG. 16B

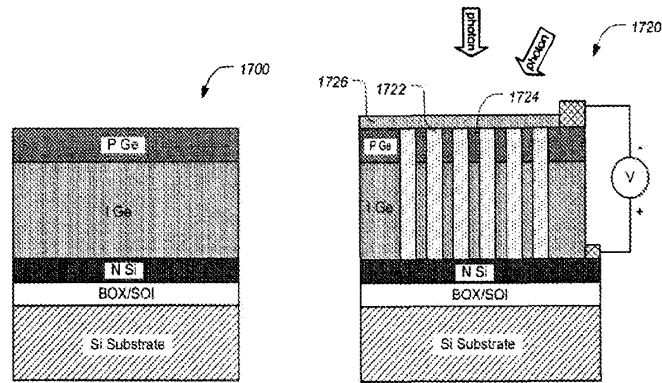


FIG. 17A

FIG. 17B

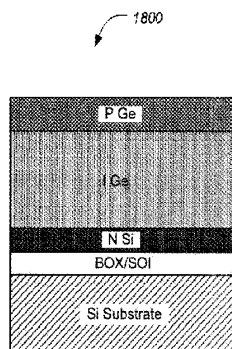


FIG. 18A

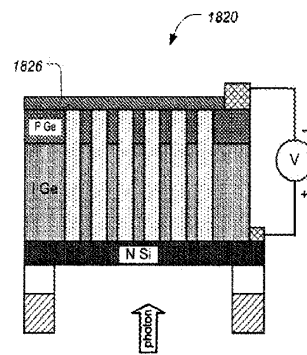
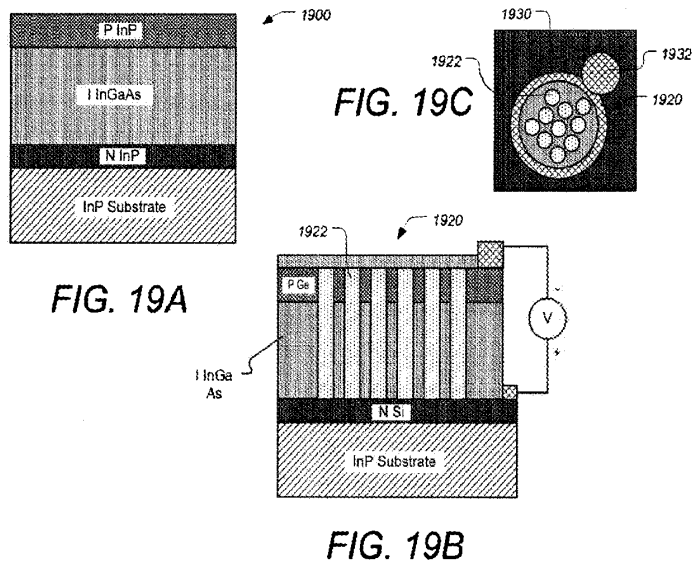


FIG. 18B



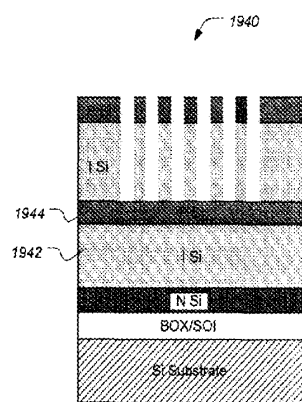


FIG. 19D

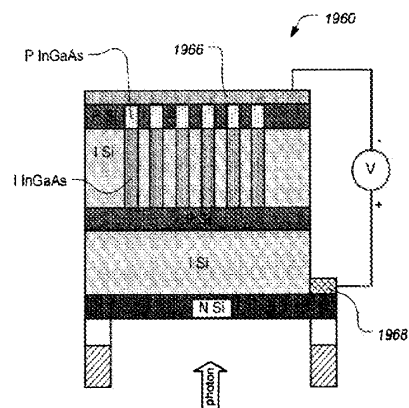
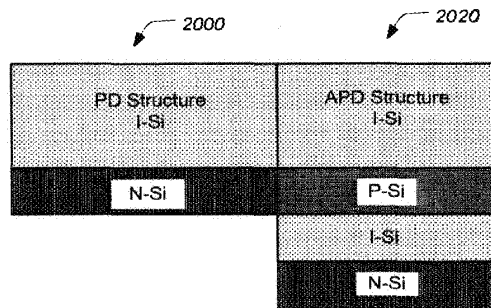
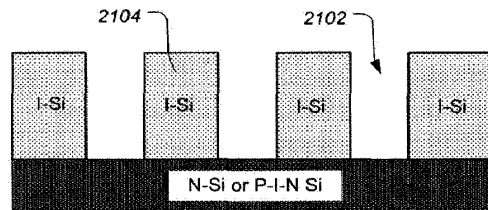
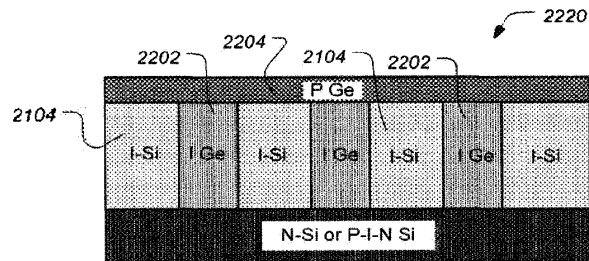
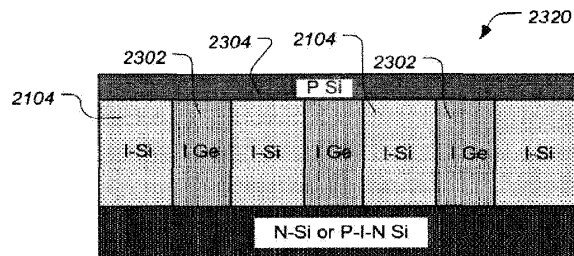


FIG. 19E

**FIG. 20****FIG. 21**

**FIG. 22****FIG. 23**

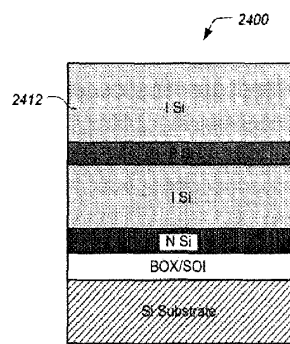


FIG. 24A

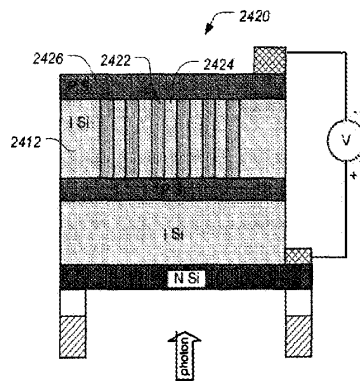


FIG. 24B

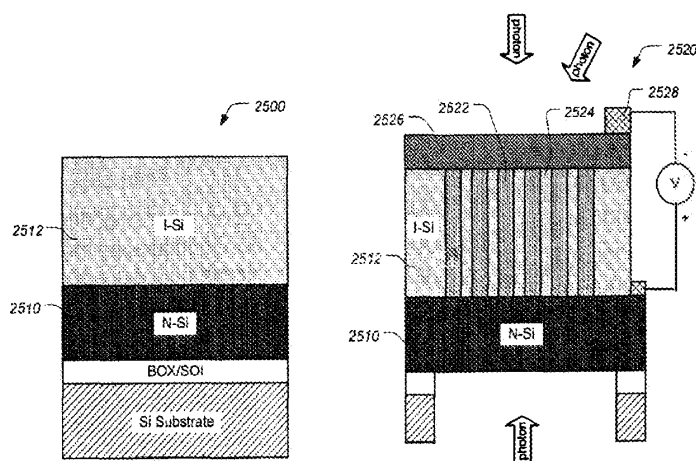


FIG. 25A

FIG. 25B

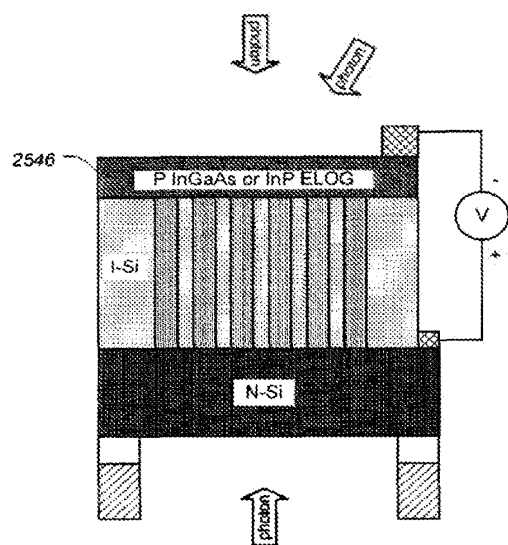


FIG. 25C

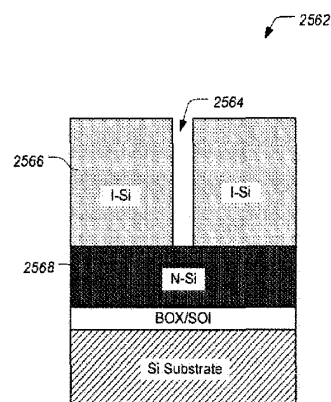


FIG. 25D

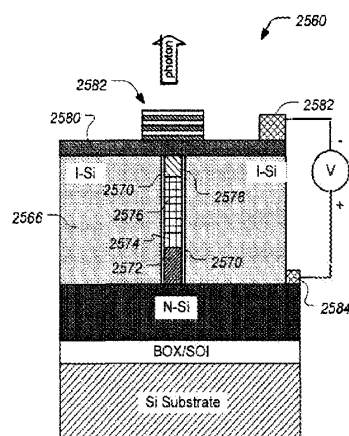
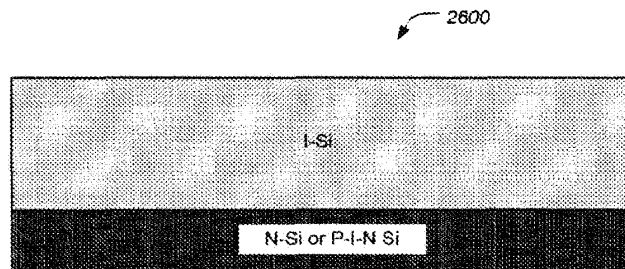
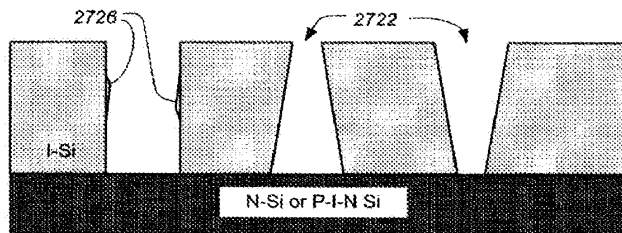
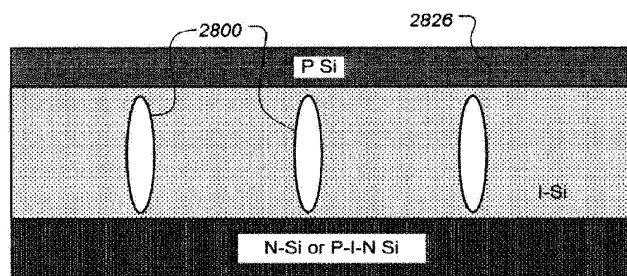
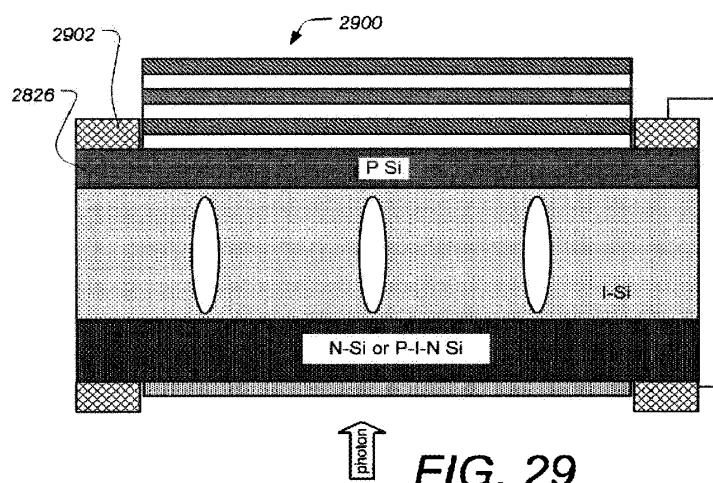


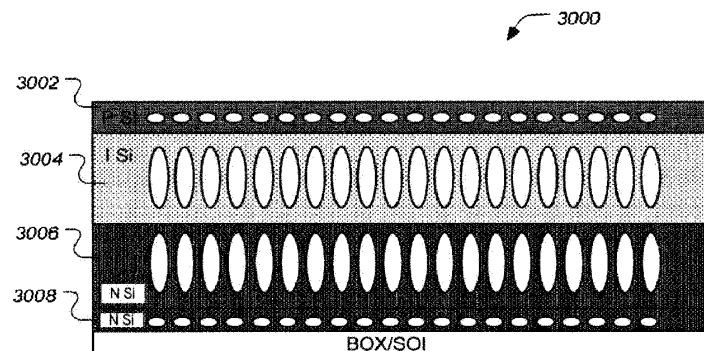
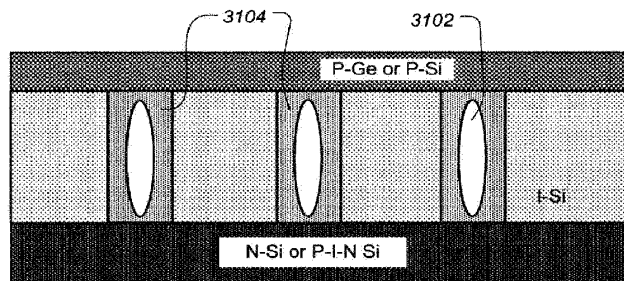
FIG. 25E

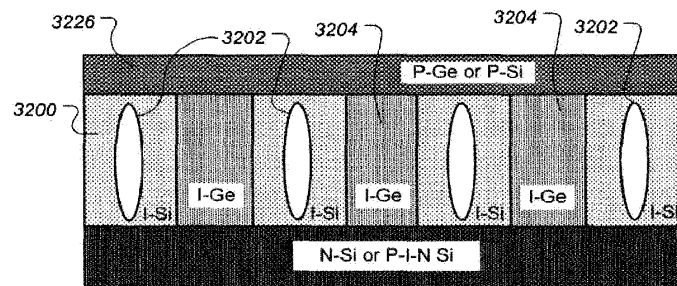
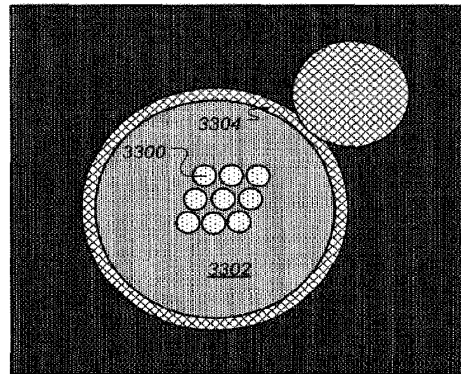
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**FIG. 26****FIG. 27**

**FIG. 28****FIG. 29**

**FIG. 30****FIG. 31**

**FIG. 32****FIG. 33**

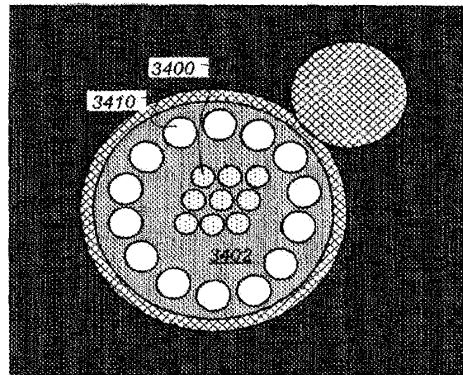


FIG. 34

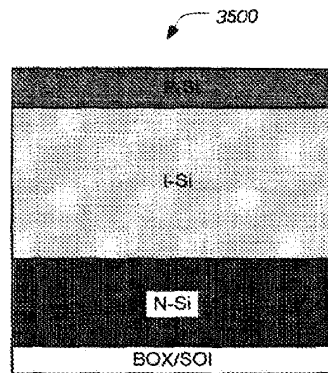


FIG. 35
(prior art)

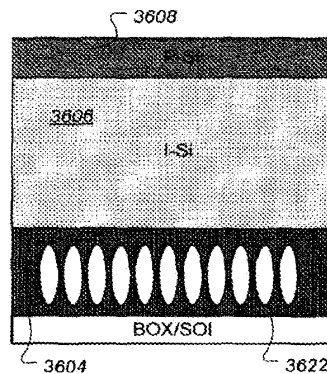
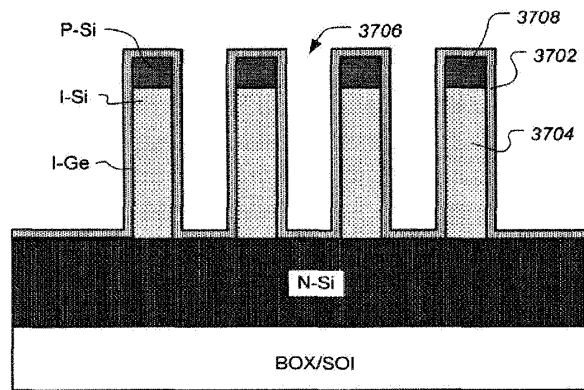
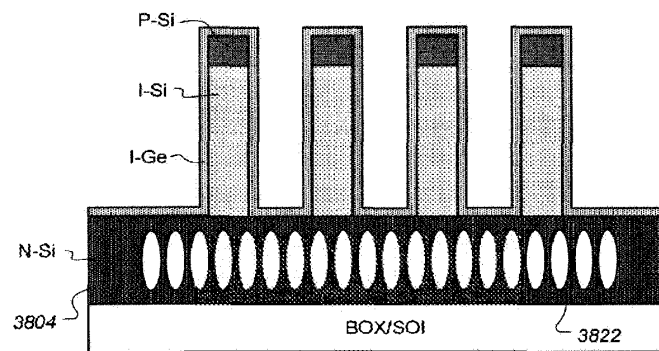


FIG. 36

**FIG. 37****FIG. 38**

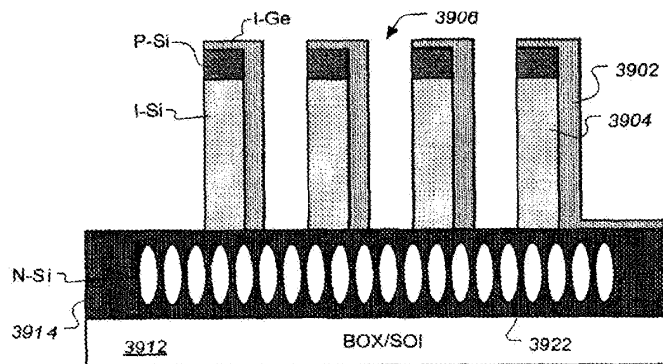


FIG. 39

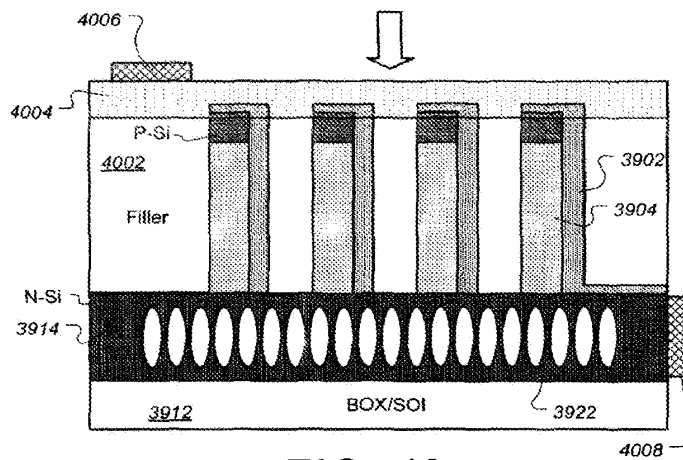


FIG. 40

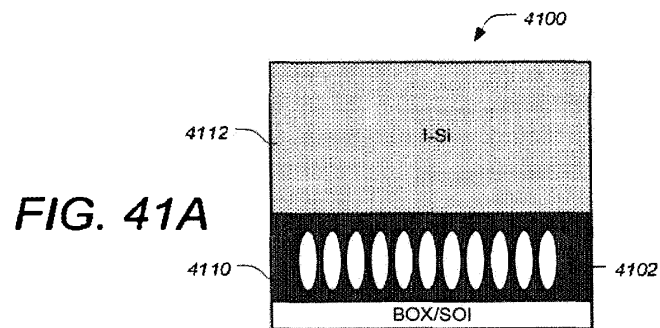
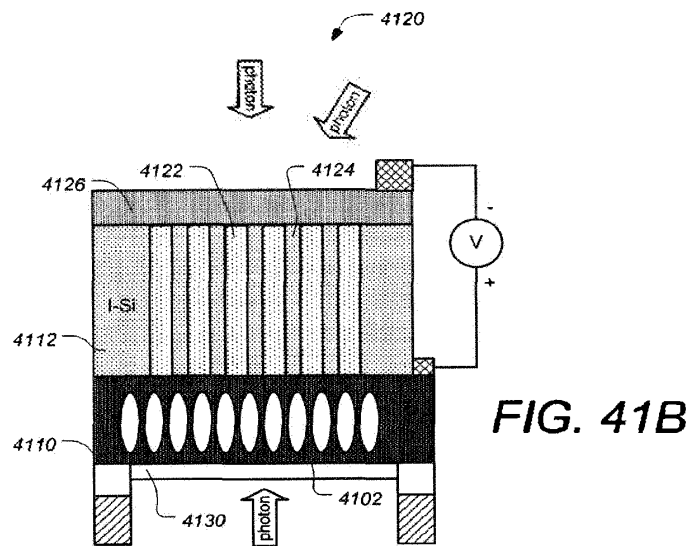


FIG. 42A

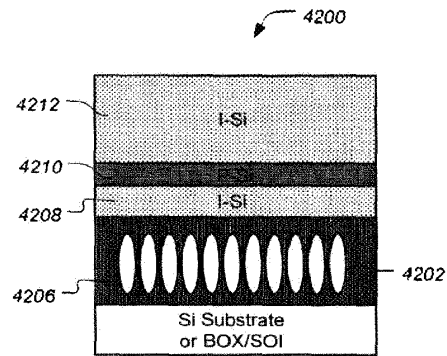
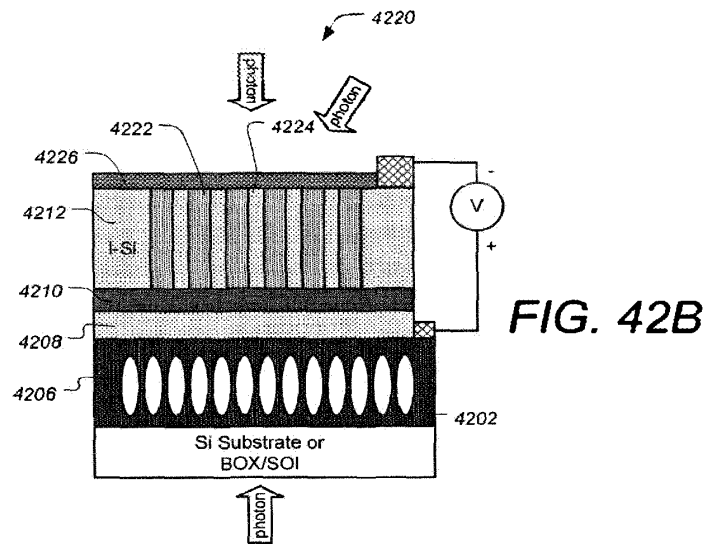
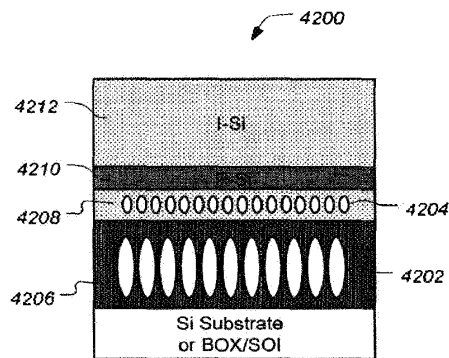
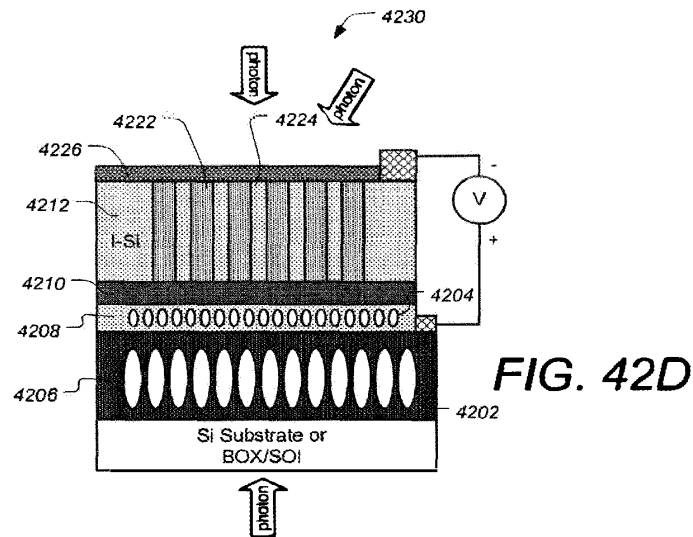
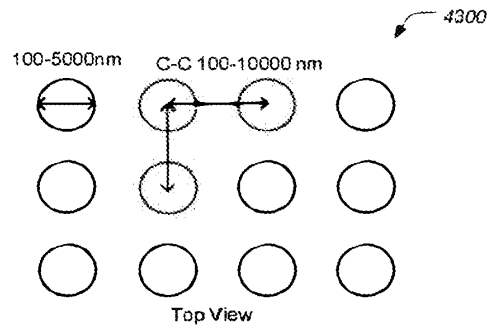
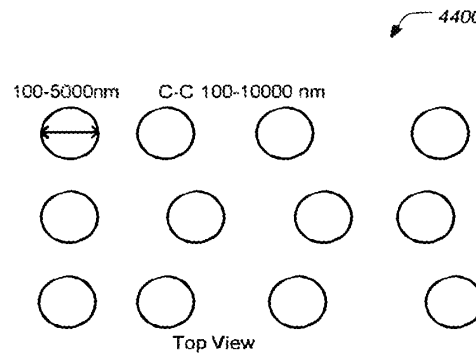
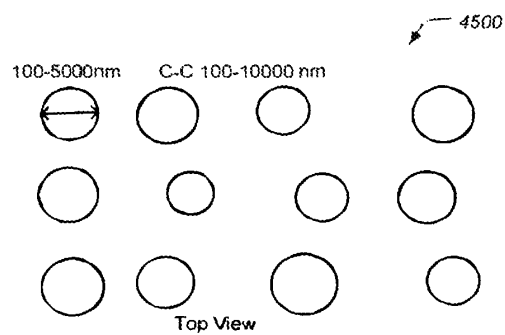
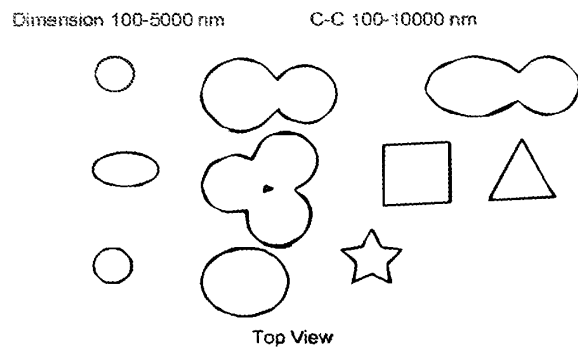
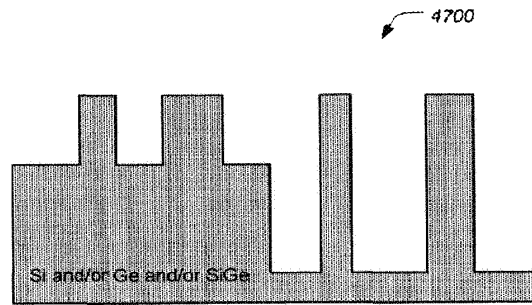
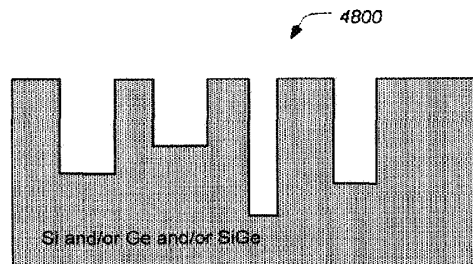


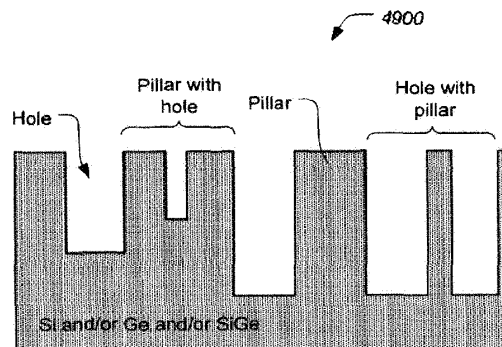
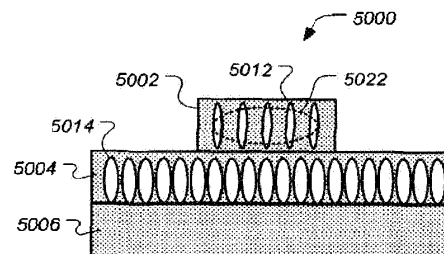
FIG. 42C



**FIG. 43****FIG. 44**

**FIG. 45****FIG. 46**

**FIG. 47****FIG. 48**

**FIG. 49****FIG. 50**

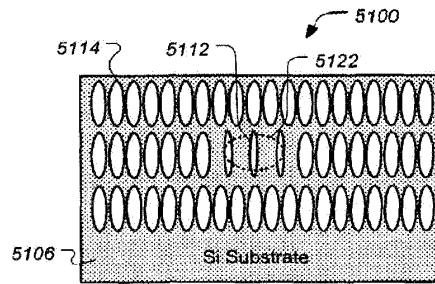


FIG. 51

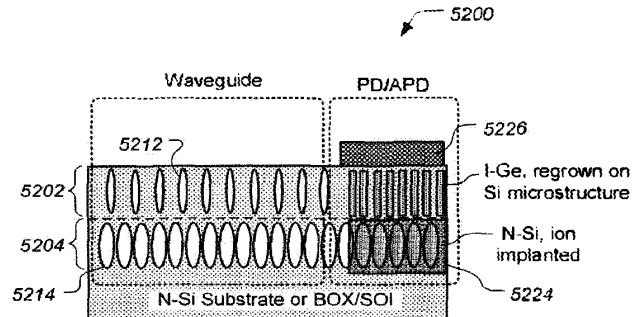


FIG. 52

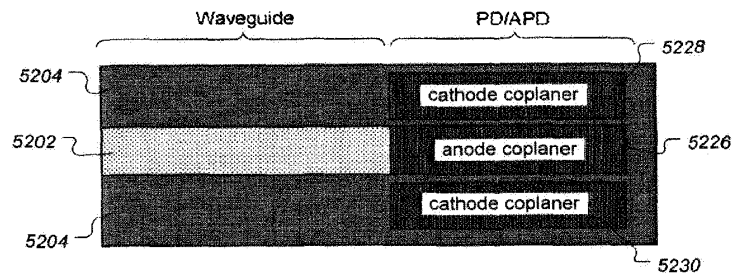


FIG. 53

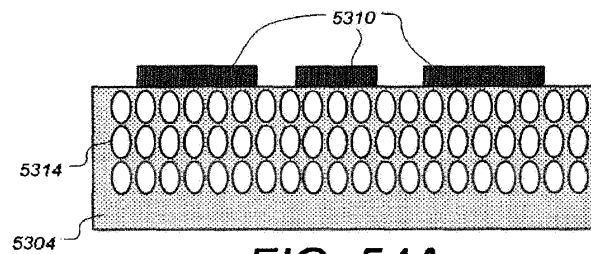


FIG. 54A

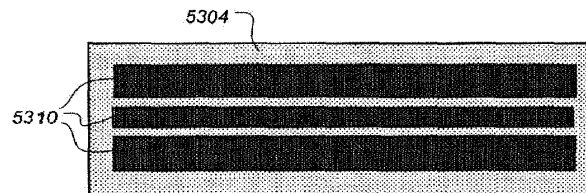
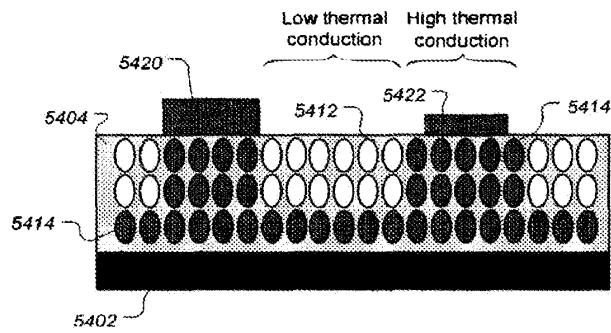
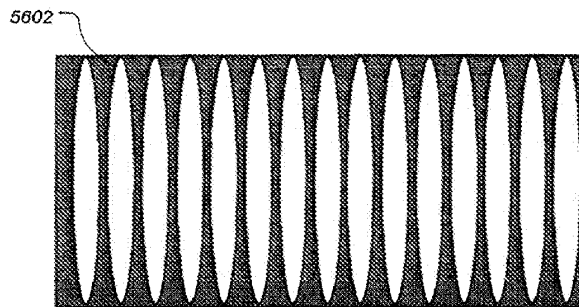


FIG. 54B

*FIG. 55**FIG. 56*

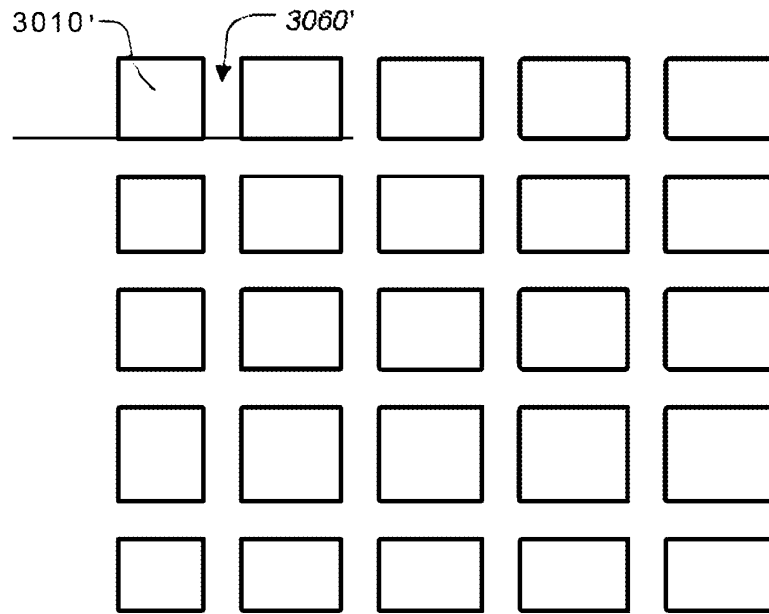


FIG. 57A

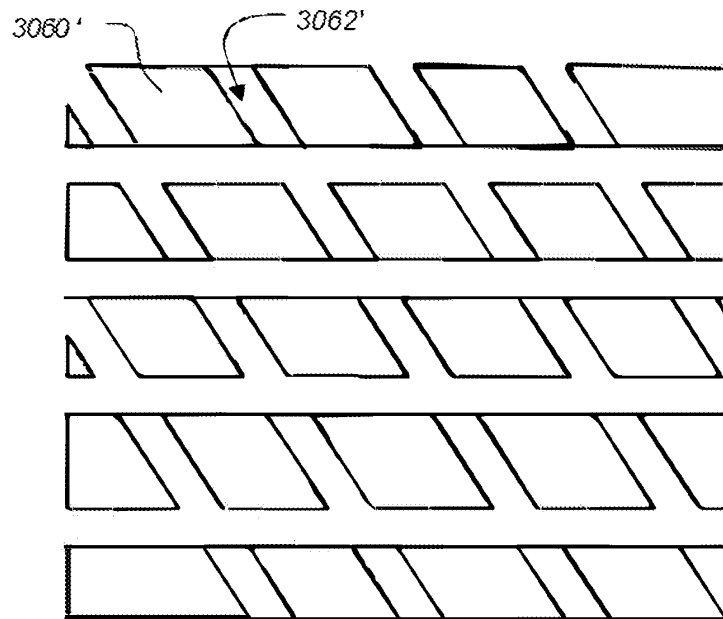


FIG. 57B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Shih-Yuan WANG et al.
Serial No.: Divisional of 18/822,880
Examiner: EDUARDO A RODELA
Group Art Unit 2893
Filing Date: TBD
For: MICROSTRUCTURE ENHANCED ABSORPTION
PHOTOSENSITIVE DEVICES
Conf. No. 5818

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FIRST PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Amendments to the specification start on page 2.

Amendments to the claims start on page 3.

Remarks start on page 8.

Amendments to the Specification:

Please amend paragraph 0001 as follows:

[0001] This patent application is a division of U.S. Ser, No. 18/882,880, which in turn is a divisional of 18/385,213, which in turn is a continuation in-part of each of U.S. Application 18/113,474 and 17/974,325, and through a chain of related U.S., PCT, and provisional patent applications goes back to 2013.

Amendments to the Claims:

Please cancel claims 1-17 and add the following claims 18-36:

18. An integrated structure comprising:

an array of pillars in which the pillars extend in up-down directions and comprise Si, Ge, and/or alloyed SiGe semiconductor material, wherein at least some of the pillars include photodetectors and have respective light-receiving surfaces and respective sides; wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in visible and infrared wavelengths by generating electrical charge carriers;

one or more holes that are fabricated as recesses in each of at least some of the pillars, extend in up-down directions to depths of less than 10000 nm, and are filled at least partly with solid dielectric material;

side-isolation comprising solid dielectric material between at least portions of the sides of at least some of the pillars;

electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for selected reverse-biasing at least some of the photodetectors;

wherein the presence of the one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes.

19. The integrated structure of claim 18, in which the array is monolithically integrated with Si electronic devices.
20. The integrated structure of claim 18, in which each of at least some of the holes is elongated along the light-receiving surface of the pillar in which the hole is fabricated so that the hole is longer in a first than in a second direction that is transverse to the first direction.
21. The integrated structure of claim 20, in which each of at least some of the pillars has a plurality of the elongated holes.
22. The integrated structure of claim 20, in which each of at least some of the pillars has only one of the elongated holes.
23. The integrated structure of claim 20, in which the pillars in which the holes are fabricated have respective widths at the light receiving surfaces thereof and each of at least some of the elongated holes extends in the first direction along less than the width of the pillar in which the hole is fabricated.
24. The integrated structure of claim 20, in which each of at least some of the elongated holes has at least one closed contour remote from side edges of the pillar in which the hole is fabricated.

25. The integrated structure of claim 18, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors.
26. The integrated structure of claim 18, in which two or more of the photodetectors are connected electrically in parallel.
27. The integrated structure of claim 18, wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission.
28. The integrated structure of claim 18, wherein the array is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors.
29. The integrated structure of claim 18, in which each of at least some of the holes is shaped as a square or a rectangle or a circle or an oval at the light-receiving surface of the pillar in which the hole is fabricated.
30. The integrated structure of claim 29, in which each of at least some of the pillars has two or more of the holes at the light receiving surface of the pillar.
31. The integrated structure of claim 18, further including solid dielectric material underlying the array of pillars.

32. An integrated structure comprising:

an array of pillars in which the pillars extend in up-down directions and comprise Si, Ge, and/or alloyed SiGe semiconductor material, wherein each of at least some of the pillars has sides and a light-receiving surface and comprises at least one photodetector;

wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in visible and infrared wavelengths by generating electrical charge carriers;

one or more holes that are fabricated as recesses into the light-receiving surface of each of at least some of the pillars,

wherein each of at least some of the holes (i) has at least one closed contour at an intermediate area of the light-receiving surface of the pillar in which the hole is fabricated, (ii) extends down into the pillar in which the hole is fabricated to a depth of less than 10000 nm, and (iii) is filled at least partly with solid dielectric material;

side-isolation comprising solid dielectric material between at least portions of the sides of at least some of the pillars;

electrical contacts configured to provide electrical pathways coupled to at least some of the photodetectors, including for selected reverse-biasing of the photodetectors;

wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the

photodetectors relative to like photodetectors lacking the holes;
and
wherein the array is monolithically integrated with Si electronic
devices for signal processing and transmission.

33. The integrated structure of claim 32, in which each of at least some of the pillars has only one of the holes fabricated therein.
34. The integrated structure of claim 32, in which each of at least some of the pillars has at least two of the holes fabricated therein.
35. The integrated structure of claim 32, in which each of at least some of the pillars includes only a single photodetector.
36. The integrated structure of claim 32, in which each of at least some of the holes is elongated along the light-receiving surface of the pillar in which the hole is fabricated.

REMARKS

This application is a division of immediate parent application Ser. No. 18/822,880, in which a Notice of Allowance was mailed 01/15/2025. Applicant combined claims 1 and 3 in that immediate parent application to expedite the grant of a patent with the allowable claims.

This divisional application submits claims that applicant believes patentably differ from the references applied in the parent application, **Yu** US 2011/0309331), **Lunev** US2014/001660, **Counil** US 2010/0116332, and **Arimoto** US 5,759,292, and that a fair combination thereof would not have motivated the hypothetical person of ordinary skill the art in 2013-2014 to arrive at the inventions claimed in this divisional application at least for the reasons discussed below.

Yu and Lunev References.

The Notice of Allowability in the immediate parent application comments, in pages 6 and 7, about elements of claims 1 and 14 that **Yu** and **Lunev** fail to disclose. Applicant submits that some of these comments also apply to the subject application.

In addition, Applicant submits that **Yu** is about an SBUV detector, i.e. “a device that detects radiation only in the SBUV region and rejects visible and infrared radiation” (Yu paragraph [0041]; emphasis added). To achieve such effect in SBUV, **Yu** relies on nanowires with 5-30 nm diameters (**Yu** paragraph [0046]). The nanowires are configured to react only to radiation in SBUV region and not to react to radiation outside the SBUV region (**Yu** paragraph [0043]), such as visible and infrared. This is not the structure claimed in the subject application that responds to visible and infrared radiation. There would have been no motivation for any modification of **Yu**’s structure for visible and infrared ranges because it

would defeat the sole purpose of using nanowires in Yu's structure.

Further, **Yu** shows no holes fabricated in pillars as claimed in the subject application. Applicant submits that fabricating holes in **Yu**'s "solar-blind UV detector" nanowires, which have 5-30 nm diameters (**Yu** paragraph [0046]), would have been counterintuitive to the skilled person even if such holes could have been fabricated practically with 2013-2014 technology, as it would have complicated design and manufacturing considerations. Applicant believes that such fabricated holes, even if they could have been made at the time, are likely to have degraded the sensitivity of **Yu**'s device because they would have created an opposite effect of the coupler 140 in Yu's Fig 1C, which directs light to the centers of the nanowires. See **Yu** at [0045] "a coupler 140 disposed on an end of the nanowire 100 away from the substrate 130 (hereafter referred to as the 'receiving end'). The term 'coupler' as used herein means a layer effective to guide light into the nanowires."

Thus, there would have been no motivation to attempt to fabricate holes in the 5-30 nm nanowires as there would have been no expectation that this would improve response to **Yu**'s non-visible SBUV light, much less to light that **Yu**'s device does not respond to.

Regarding **Lunev**, Applicant additionally submits that the reference is about a light-emitting device, i.e. a device that generates light rather than about an array of pillars separated from each other by solid dielectric and comprising photodetectors configured to generate electrical carriers. **Lunev** in paragraph [0042] identifies a "light emitting device such as a light emitting diode (LED), a laser diode (LD), a photodiode, and/or the like." This sentence structure informs that "photodiode" in this context is an example of a device that emits light. The

next **Lunev** sentence confirms this by referring to the wavelength of the light that “the device” emits. Further confirmation is that the metal structure 218 in Lunev’s FIG. 4B is inconsistent with a photodetector as it would block the receiving light from the top surface where the layer 234 is present. **Lunev** in paragraph [0051] can be configured to scatter light, e.g., generated in the semiconductor contact structure 212B.” (Emphasis added.) This again confirms that Lunev is about a light emitting device. The scattering structures serve to scatter light generated in the device rather than light incident on a photodetector. Further, if Lunev’s structure is used as a photodetector, for which it is not designed, the light would enter the structure at the side oppose to layer 218, for a bottom-receiving photodetector. The amount of light blocked by the structure of layer 218 in FIG. 4B would have made this a poor choice for photodetector structure. **Lunev**’s structure is not compatible with Yu’s device, which is a top-receiving photodetector structure. **Yu**’s FIG. 1A.

Accordingly, **Lunev** would not have motivated the skilled person to include roughening structures in **Yu**’s nanowires that detect but do not generate light and thus have no need to scatter light generated in the nanowires.

The skilled person would not have been motivated by **Yu** and **Lunev** to fabricate holes in **Yu**’s 5-30 nm diameter nanowires as neither reference suggests that this would improve light detection performance of a nanowire, even if had been practical in 2013-2014 to fabricate a hole in such a small surface.

Lunev refers to Ohmic contact 218 with metal fingers but they are not “holes that are at least partly filled with solid dielectric material” as the claims of the subject application describe. These metal fingers contact both semiconductor

layers and thus teach away from use in a photodetector in which different electrodes couple to differently doped layers.

Counil Reference.

Counil proposes a continuous, flat and wide solar cell rather than an array of individual pillars with photodetectors and in-pillar holes and with electrodes for reverse-bias as claimed in the subject application. There is no such array in **Counil** and no pillars with holes. While **Counil** refers to increasing solar cell absorption, there is no suggestion of whether and how this might apply to photodetectors in pillars forming the claimed array. Applicant submits that **Counil** would not have motivated the skilled person to arrive at the inventions that the subject application claims because that person would not have expected that Yu's nanowires, which don't respond to visible and infrared light, would respond to such light and further that the individual, nanoscale nanowires could have holes or could have benefited from holes. The skilled person would not have equated roughening of a flat and wide solar cell to fabricating nanoscale holes in Yu's individual nanowires and would not have been motivated to try.

Arimoto Reference.

Last, **Arimoto** also proposes a continuous, flat and wide solar cell rather than an array of individual pillars with photodetectors and in-pillar holes and with electrodes for reverse-bias as claimed in the subject application. Applicant's claims specify a minimum increase in absorption due to the claimed holes, but Arimoto doesn't do that. Arimoto's FIGs. 2, 4, and 5 are not presented as being to scale so they don't quantify an increase. Applicant submits that in 2013-2014 **Arimoto** would not have motivated the skilled person to fabricate holes in Yu's SBUV nanowires as there would have been no expectation that roughening a solar cell

surface would benefit 5-30 nm diameter nanowires to detect visible and infrared light that **Yu** states his nanowires reject

In short, applicant submits that the four references would not have led the skilled person in 2013-2014 to the integrated structure that the claims of the subject application describe as including pillars that comprise photodetectors and include holes fabricated in the pillars, with dielectric material in the holes, at least because (i) **Yu**'s express statement that his proposed device doesn't respond to visible and infrared light would have led the skilled person away from considering **Yu**'s nanowires for structures responding to visible and infrared light, (ii) **Lunev**'s light-generating devices would not have motivated the skilled person to expect benefits for **Yu**'s 5-30 nm nanowires even if the technology at the time provided a practical way to do so, and the skilled person would not have been motivated to expect that scattering light emitted from a device would have improved a device that responds to incident light, and (iii) roughened surfaces of continuous, wide and flat solar cells for visible light as in **Counil** and **Arimoto** would not have motivated the skilled person to expect that fabricating holes in the 5-30 nm surfaces of **Yu** nanowires would make those nanowires better respond to light that **Yu**'s nanowires are specifically designed to reject.

Applicant invites the Examiner to telephone the undersigned if the Examiner finds that a call may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

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