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Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

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PATENT CENTER #	67294168	FILING DATE	01/24/2022
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CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Khaled Shami

Documents

TOTAL DOCUMENTS: 39

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
IDS - 022955-90.pdf	10	Information Disclosure Statement (IDS) Form (SB08)	1366 KB
FOR--EP0744748B1.pdf	30	Foreign Reference	461 KB
FOR--JP2001357669A.pdf	16	Foreign Reference	2378 KB
FOR--EP0908892B1.pdf	129	Foreign Reference	2754 KB
FOR--WO2005066968A1.pdf	70	Foreign Reference	2458 KB
FOR--JP2006268419A.pdf	18	Foreign Reference	4010 KB
FOR--JP09034806A.pdf	27	Foreign Reference	6056 KB
FOR--JP2001318741A.pdf	28	Foreign Reference	4904 KB
FOR--WO2001037090A1.pdf	22	Foreign Reference	796 KB

FOR--KR1020050073902A.pdf	17	Foreign Reference	4217 KB
FOR--JP3707888B2.pdf	52	Foreign Reference	9511 KB
NPL--6__28-MAXIM.pdf	14	Non Patent Literature	328 KB
NPL--1__23-ISL6537.pdf	16	Non Patent Literature	595 KB
NPL--3__25-NXP.pdf	48	Non Patent Literature	768 KB
NPL--4__26-TKDM.pdf	8	Non Patent Literature	440 KB
NPL--2__24-ISL6532.pdf	16	Non Patent Literature	590 KB
NPL--5__27-ISL6534.pdf	29	Non Patent Literature	860 KB
NPL--8__NationalSemiconductor_2006_LP3913.pdf	6	Non Patent Literature	346 KB
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Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application number: JP20000139166
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Priority: JP20000139166 [20000511]
Assignee: IDEC CORP; 和泉電気株式会社; ＩＤＥＣ株式会社
Assignee[std]: IDEC IZUMI CORP
Inventor: 田栗 義輝; 米澤 浩; 菅井 祐平; 錦 朋範; 間宮 勝
Inventor[std]: MAMIYA MASARU; NISHIKI TOMONORI; SUGAI YUHEI; TAKURI YOSHITERU; YONEZAWA HIROSHI
International class[8]: G06F1/00; G06F1/30; G06F12/16; H02J9/00
Title: PROGRAM EXECUTION DEVICE
プログラム実行装置

Abstract:

PROBLEM TO BE SOLVED: To provide a program execution device capable of preventing a processing result from being lost even with a small charging amount of a backup power source. SOLUTION: A detection circuit 20 outputs the detection signal C1 of '0' when a DC voltage Vb is higher than a first threshold voltage and the detection signal C1 of '1' when it is not. An execution circuit 30 is driven by receiving the DC voltage Va at a power source terminal, executes a first kind program at the time of receiving the detection signal C1 of '0' and executes a second kind program for protecting a processing result obtained by executing the first kind program and generates a control signal C2 at the time of receiving the detection signal C1 of '1'. A charging circuit 60 charges the DC voltage Vc. A discharging circuit 50 discharges a charging voltage V2 to the power source terminal of the execution circuit 30 based on the control signal C2.

【課題】 バックアップ電源の少ない充電量でも処理結 果が消失してしまうことを防ぐことができるプログラム 実行装置を得る。 【解決手段】 検出回路２０は、直流電圧Ｖｂが第１閾 値閾電圧より大きいときに"０"の検出信号Ｃ１、そう でないときに"１"の検出信号Ｃ１を出力する。実行回 路３０は、直流電圧Ｖａを電源端子に受けて駆動し、" ０"の検出信号Ｃ１を受けると第１種プログラムを実行し、"１"の検出信号Ｃ１を受けると第１種プログラム を実行することによって得られた処理結果を保護する第 ２種プログラムを実行するとともに制御信号Ｃ２を生成 する。充電回路６０は直流電圧Ｖｃを充電する。放電回 路５０は制御信号Ｃ２に基づいて充電電圧Ｖ２を実行回 路３０の電源端子へ放電する。

Claims:

１．直流電源電圧を受け、当該直流電源電圧が第１閾値閾電圧より大きいときにオン信号、そうで

1. by the DC supply voltage, threshold voltage on signal is larger than the first threshold voltage of

Samsung Electronics Co., Ltd.
Ex. 1002, p. 846

ないときにオフ信号を出力する検出回路と、前記直流電源電圧を電源端子に受けて駆動し、前記オン信号を受けると第１種プログラムを実行し、前記オフ信号を受けると前記第１種プログラムを実行することによって得られた処理結果を保護する第２種プログラムを実行するとともに放電信号を生成する実行回路と、前記直流電源電圧を充電する充電回路と、前記放電信号を受けると、前記充電回路の充電電圧を前記電源端子へ放電する放電回路と、を備えたプログラム実行装置。

２. 前記電源端子の電圧が当該実行回路が動作可能な予め設定された第２閾値電圧になったときに前記放電信号を前記放電回路に出力する出力回路をさらに備えた請求項１記載のプログラム実行装置。

３. 前記第２種プログラムは前記実行回路をリセットする処理を含む請求項１記載のプログラム実行装置。

４. 前記第１種および第２種プログラムは、当該第１種および第２種プログラムの処理結果が所定条件を満たしていなければ、前記実行回路をリセットする処理を含む請求項１記載のプログラム実行装置。

５. 前記充電回路は、前記直流電源電圧を充電するコンデンサを含む請求項１記載のプログラム実行装置。

６. 前記検出回路、前記実行回路、前記充電回路、前記放電回路は１チップ上に形成されている請求項５記載のプログラム実行装置。

said DC power source, and outputs a signal detection circuit turns off when it is not, receiving said DC power supply voltage to the power terminals The drive to run the program on one of said signal is received, along with running a program to protect the processing results of the second kind obtained by running the program and the first species to receive clear signal above run to generate a discharge signal circuit, charging circuit and said DC power supply voltage to charge and discharge signal is received, a discharge circuit for discharging said supply voltage terminal of the charging circuit charges said program execution device with.

2. 1 claim, further comprising an output circuit outputs the signal to the discharge in the discharge circuit when a preset second threshold voltage that can perform such circuit is the voltage of said power supply terminal program execution unit described.

3. program is the second kind of program execution device according to claim 1, including processing said execution circuitry to reset.

4. Species Programme said first and second kind, unless certain conditions are met the result of processing said first kind and second kind program offers, including the process of claim 1 wherein the reset circuit is run program execution unit.

5. charging circuit, said program execution device according to claim 1 comprising a capacitor charging voltage to said DC power supply.

6. detection circuit, said execution circuit, said charging circuit, said discharge circuit program execution apparatus of claim 5 which is formed on one chip.

Description:

[０００１] [発明が属する技術分野]本発明は、コンピュータプログラム（以下、単に「プログラム」と称す）を実行するプログラム実行装置に関する。

[０００２] [従来の技術]従来では、プログラムの実行中に外部からの電源が遮断されたとき、即座にバックアップ電源に切り替えて引き続いて同じプログラムを実行する。

[0001] [technical field to which the invention] The present invention is a computer program (hereinafter referred to simply as "program" referred to as) to run the program execution apparatus.

[0002] [ART] In the past, when external power is interrupted during the execution of the program to run the same program subsequently switched to the backup supply immediately.

[０００３] [発明が解決しようとする課題]しかしながら、バックアップ電源の充電量が少なければ、プログラム実行装置の駆動が不安定になり、それまでのプログラムの実行によって得られた処理結果が消失してしまうという問題点があった。

[０００４]本発明は上記の問題点を解決するためになされたものであり、バックアップ電源の少ない充電量でも処理結果が消失してしまうことを防ぐことができるプログラム実行装置を得ることを目的とする。

[０００５] [課題を解決するための手段]請求項１に記載の課題解決手段は、直流電源電圧を受け、当該直流電源電圧が第１閾値閾電圧より大きいときにオン信号、そうでないときにオフ信号を出力する検出回路と、前記直流電源電圧を電源端子に受けて駆動し、前記オン信号を受けると第１種プログラムを実行し、前記オフ信号を受けると前記第１種プログラムを実行することによって得られた処理結果を保護する第２種プログラムを実行するとともに放電信号を生成する実行回路と、 前記直流電源電圧を充電する充電回路と、前記放電信号を受けると、前記充電回路の充電電圧を前記電源端子へ放電する放電回路とを備える。

[０００６]請求項２に記載の課題解決手段は、前記電源端子の電圧が当該実行回路が動作可能な予め設定された第２閾値電圧になったときに前記放電信号を前記放電回路に出力する出力回路をさらに備える。

[０００７]請求項３に記載の課題解決手段において、前記第２種プログラムは前記実行回路をリセットする処理を含む。

[０００８]請求項４に記載の課題解決手段において、前記第１種および第２種プログラムは、当該第１種および第２種プログラムの処理結果が所定条件を満たしていなければ、前記実行回路をリセットする処理を含む。

[０００９]請求項５に記載の課題解決手段において、前記充電回路は、前記直流電源電圧を充電するコンデンサを含む。

[0003] [PROBLEMS TO BE SOLVED BY THE INVENTION However, the less amount of charge the backup power supply system becomes unstable driving program execution, the results obtained by processing the previous execution of the program there is a problem that disappears.

[0004] The present invention has been made to solve the above problems, to get the program execution apparatus that can prevent you to lose a small amount of charge processing result in backup power for the purpose.

[0005] [Means for Solving the Problem] problem solving method according to claim 1, by the DC supply voltage, threshold voltage on signal is larger than the first threshold voltage of said DC power supply, so detection circuit and outputs a signal when it is not clear, driven by said DC supply voltage to the power terminals, and the first one to run the program receives a signal on said program and said first type wherein the off signal is received Run the discharge circuit for generating a signal to run the program with the second seed treatment to protect the results obtained by running a charging circuit and said DC power supply voltage to charge and discharge signal is received, said charge and a discharge circuit for discharging said charging voltage to the circuit power terminals.

[0006] means for problem solving according to claim 2, wherein the discharge circuit when the voltage signal to discharge a second predefined threshold that can perform such circuit is the voltage of said power supply terminal output circuit further comprises output.

[0007] The problem solving method according to claim 3, wherein the first two programs, including processing said execution circuitry to reset.

[0008] The problem solving method according to claim 4, the program first kind and second kind, unless certain conditions are met the results of two treatment programs per species and said first, said reset the circuit including the processing run.

[0009] The problem solving method according to claim 5, wherein said charging circuit includes a capacitor charging voltage to said DC power supply.

[0010] The problem solving method according to claim 6, wherein the detection circuit, said

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[００１０]請求項６に記載の課題解決手段において、前記検出回路、前記実行回路、前記充電回路、前記放電回路は１チップ上に形成されている。

[００１１] [発明の実施の形態]（実施の形態１）図１は本発明の実施の形態１のプログラム実行装置を示すブロック図である。実施の形態１のプログラム実行装置は、電源回路１０、検出回路２０、実行回路３０、出力回路４０、放電回路５０、充電回路６０、入力部７１、出力部７２、リセット回路８０および電源ライン９０を含む。

[００１２]まず、実施の形態１のプログラム実行装置の構成について説明する。

[００１３]電源回路１０は外部から直流電圧Ｖ０を受け、直流電圧Ｖａ、直流電圧Ｖｂおよび直流電圧Ｖｃを生成して出力する。

[００１４]検出回路２０は直流電圧Ｖｂを受け、検出信号Ｃ１を生成して出力する。検出回路２０は、例えば図２に示すようなインバータ機能を有する回路である。図２において、Ｖｄは電源回路１０が生成する直流電圧、その他の符号は図１に対応している。検出回路２０は、図２のような回路以外であってもよく、直流電圧Ｖｂが閾値電圧ｃより大きいとき"０"の検出信号Ｃ１を出力し、そうでないとき"１"の検出信号Ｃ１を出力するものであればよい。 less than DP N=0003 greater than

[００１５]図１の実行回路３０は、電源端子が電源ライン９０に接続され、検出信号Ｃ１を受け、制御信号Ｃ２を生成して出力する。また、実行回路３０は、入力部７１から入力信号Ｃ４を受け、処理結果Ｃ５を生成して出力部７２に出力する。

[００１６]図３は、実行回路３０の内部構成を示すブロック図である。実行回路３０は割込信号生成回路３１、ＣＰＵ３２および主メモリ３３を含む。割込信号生成回路３１は、検出信号Ｃ１およびＣＰＵ３２からの信号Ｄ１を受け、検出信号Ｃ１および信号Ｄ１の排他的論理和を信号Ｄ２としてＣＰＵ３２に出力する。主メモリ３３およびＣＰＵ３２の動作を図４および図５を用いて説明す

execution circuit, said charging circuit, said discharge circuit being formed on one chip.

[0011] [Embodiment of the Invention (Embodiment 1) Figure 1 is a block diagram showing one embodiment of the program execution apparatus of the present invention. Program execution apparatus of the first embodiment, the power supply circuit 10, detection circuit 20, circuit 30 is executed, the output circuit 40, discharge circuit 50, charging circuit 60, input unit 71, output unit 72, a reset circuit 80 and power line 90 including.

[0012] First, a description of the configuration of a first embodiment of the program execution.

[0013] 10 power supply circuit receives an external DC voltage V0, Va DC voltage, which generates and outputs a DC voltage Vb and Vc of the DC voltage.

[0014] 20 detector receives DC voltage Vb, which generates and outputs a detection signal C1. Detection circuit 20 is a circuit having an inverter function, for example, as shown in Figure 2. In Figure 2, Vd is the DC voltage generated by power supply circuit 10, other symbols that correspond to Figure 1. The detection circuit 20, may be outside the circuit shown in Figure 2, c is greater than the threshold voltage DC voltage Vb to "0" and outputs a detection signal C1, otherwise a "1" detection signal C1 as long as it is output. less than DP N = 0003 greater than

[0015] 30 running the circuit of Figure 1, line 90 is connected to the power supply terminal, receives a detection signal C1 and C2 and generates and outputs a control signal. In addition, the execution circuit 30 receives input signals from the C4 input section 71, section 72 outputs the output to generate the C5 result.

[0016] 3 shows a block diagram showing the internal configuration of the circuit 30 runs. Execution circuit 30 interrupt signal generation circuit 31 includes a main memory 33 and the CPU32. The interrupt signal generating circuit 31 receives a signal from the CPU32 C1 and D1 detection signal is output to the CPU32 as the exclusive signal D2 D1, C1 and signal detection signal. Be described with reference to Figure 4 and Figure 5 the main memory 33 and the operation of the CPU32. As shown in Figure 4, the detection signal C1 is "1" signal at D1 is "0", D2 signal "1" (ta time). In this state, the detection

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る。図４に示すように、検出信号Ｃ１が"１"で信号Ｄ１が"０"のとき、信号Ｄ２は"１"である（時刻ｔａ）。この状態で、検出信号Ｃ１が"０"になると、割込信号生成回路３１は信号Ｄ２を立ち下げる（時刻ｔｂ）。ＣＰＵ３２は信号Ｄ２の立ち下がりを受けると、信号Ｄ１を反転させて"１"にする。これによって、信号Ｄ２は再び"１"になる（時刻ｔｃ）。また、図５に示すように、検出信号Ｃ１が"０"で信号Ｄ１が"１"のとき、信号Ｄ２は"１"である（時刻ｔａ）。この状態で、検出信号Ｃ１が"１"になると、割込信号生成回路３１は信号Ｄ２を立ち下げる（時刻ｔｂ）。ＣＰＵ３２は信号Ｄ２の立ち下がりを受けると、信号Ｄ１を反転させて"０"にする。これによって、信号Ｄ２は再び"１"になる（時刻ｔｃ）。以上のように、検出信号Ｃ１が"０"から"１"あるいは"１"から"０"に変化する度に、ＣＰＵ３２は信号Ｄ２の立ち下がりパルス（割込信号）を受けることになる。

[００１７]また、ＣＰＵ３２は主メモリ３３との間でデータやプログラムを実行することによって得られた処理結果をやりとりしたり、主メモリ３３からプログラムの命令を取り込んだりする。主メモリ３３に格納されているデータやプログラムは入力部７１（図１）から与えられる。

[００１８]出力回路４０は、電源ライン９０に接続され、制御信号Ｃ２を受け、制御信号Ｃ３を出力する。出力回路４０の動作は、制御信号Ｃ２が"１"の場合は制御信号Ｃ３を"０"に固定し、制御信号Ｃ２が"０"の場合は電圧Ｖ３が駆動最低電圧ｄより大きいとき制御信号Ｃ３を"０"にし、電圧Ｖ３が駆動最低電圧ｄ以下のとき制御信号Ｃ３を"１"にする。

[００１９]充電回路６０は直流電圧Ｖｃを受けて充電する。この充電電圧がＶ２である。図６に充電回路６０の内部構成の例を示す。充電回路６０は、充電完了検出回路６１、充電回路本体６２およびコンデンサ６３を含む。図６において、Ｖｅは電源回路１０が生成する基準直流電圧、その他の符号は図１に対応している。充電回路本体６２は直流電圧Ｖｃを受けてコンデンサ６３に充電する。充電完了検出回路６１は、充電電圧Ｖ２が基準電圧Ｖｅに等しくなるように、充電回路本体６

signal C1 is "0" reaches 31, the interrupt signal generator falling edge of the signal D2 (tb time). CPU32 and receive a falling signal D2, D1 signal by inverting the "1". This, D2 again signal "1" to (tc time). Also, as shown in Figure 5, the detection signal C1 is "0" signal at D1 is "1", D2 signal "1" (ta time). In this state, the detection signal C1 is "1" reaches 31, the interrupt signal generator falling edge of the signal D2 (tb time). CPU32 and receive a falling signal D2, D1 by inverting the signal "0" when. This, D2 again signal "1" to (tc time). As mentioned above, the detection signal C1 is "0" to "1" or "1" to "0" time change, CPU32 pulse falling signal D2 (signal interrupt) will be subject to.

[0017] In addition, CPU32 can handle and exchange the results obtained by running the programs and data between main memory 33, which can capture the program instructions from main memory 33. Data and programs stored in memory 33 that the main input unit 71 (Fig. 1) given by the.

[0018] 40 output circuit is connected to a power line 90 receives a control signal C2, and outputs a control signal C3. Operation of the output circuit 40, control signal C2 is "1" is a control signal C3 "0", fixed to the control signal C2 is "0" control signal voltage is greater than the minimum driving voltage V3 d the C3 "0" to the control signal C3 at d less than the minimum voltage at the driving voltage V3 "1".

[0019] 60 by the charging circuit for charging the DC voltage Vc. This is the charging voltage V2. 60 shows an example of internal configuration of the charging circuit in Figure 6. The charging circuit 60, charge completion detection circuit 61 includes a body 62 and a capacitor charging circuit 63. In Figure 6, Ve is the reference DC voltage generated by power supply circuit 10, other symbols that correspond to Figure 1. Body 62 for charging the capacitor charging circuit 63 receives the DC voltage Vc. Charge completion detection circuit 61, so that the voltage V2 is equal to the reference voltage Ve charge, charging circuit that controls the body 62. This charging circuit 60 stops charging automatically when the reference voltage V2 is equal to the charging voltage Ve. The charging circuit 60, may be outside the circuit shown in Figure 6, as long as it can be charged by the DC voltage Vc.

２を制御する。これによって、充電回路６０は充電電圧Ｖ２が基準電圧Ｖｅに等しくなると自動的に充電を停止する。充電回路６０は、図６のような回路以外であってもよく、直流電圧Ｖｃを受けて充電できるものであればよい。

[００２０]図１の放電回路５０は、制御信号Ｃ３および充電電圧Ｖ２を受け、制御信号Ｃ３に応じて充電電圧Ｖ２を電源ライン９０に出力する。なお、放電回路５０は充電電圧Ｖ２を、そのまま電源ライン９０に出力してもよいし、所定の電圧に変換して電源ライン９０に出力してもよい。

[００２１]入力部７１は、例えば、外部の周辺装置からのデータを入力する入力インタフェース、あるいはキーボード、あるいはマウス、あるいはタッチパネルである。

[００２２]出力部７２は、実行回路３０がプログラムを実行することによって得られた処理結果を出力する装置であり、例えば、外部の周辺装置へデータを出力する出力インタフェース、あるいは液晶パネル、あるいはＣＲＴ、あるいはフラッシュメモリ等の不揮発性メモリである。

[００２３]リセット回路８０は押しボタンスイッチを含み、例えばプログラムが暴走したときに操作者が押しボタンスイッチを押すことによって実行回路３０をリセットする。

[００２４]なお、"０"の検出信号Ｃ１がオン信号であり、"１"の検出信号Ｃ１がオフ信号であり、"１"の制御信号Ｃ３および"０"の制御信号Ｃ２が放電信号である。また、直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧Ｖｃ、直流電圧Ｖｄおよび基準電圧Ｖｅは直流電源電圧の概念に含まれる。

[００２５]また、全ての図の各信号において、"０"および"１"の一方が高電位、他方が低電位である。

[００２６]次に、全体の動作を図７を用いて説明する。

[００２７]まず、時刻ｔ０では、直流電圧Ｖ０はＧＮＤ（接地電位）であり、充電回路６０は全く

[0020] 50 discharge circuit of Figure 1 receives a control signal C3 and the charging voltage V2, V2, and outputs the charging voltage supply line 90 in response to the control signal C3. In addition, the discharge voltage V2 charging circuit 50, may be directly output to the power line 90, the output line 90 may be converted to a predetermined voltage power supply.

[0021] 71 input unit, for example, the input interface to input data from an external peripheral device, or keyboard, or mouse, or a touch.

[0022] 72 output unit is a device that outputs the processing result obtained by executing the program execution circuit 30, for example, the output interface for outputting data to external peripherals, LCD panels or, CRT, or a flash memory or other nonvolatile memory.

[0023] 80 The reset circuit includes a push button switch to reset the circuit 30 is performed by pressing the push button switch by the operator when a runaway program, for example.

[0024] The "0" signal is detected on the signal C1, the "1" and the detection signal C1 off signal "1" control signal C3 and the "0" control signal C2 discharge signals. Furthermore, Va DC voltage, Vb DC voltage, Vc dc voltage, Ve DC voltage Vd and the reference voltage is included in the concept of a DC power supply voltage.

[0025] In addition, all figures in each of the signal, "0" and "1" is one of high potential, the other is a low potential.

[0026] Next, an explanation for the overall operation of the FIG.

[0027] First, at time t0, V0 DC voltage to GND (ground potential), and the charging circuit 60 will be charged to GND voltage V2 also because they are not charged at all. Detection signal C1 is not run by driving circuit 30 is "0". The power line 90 voltage V3 GND, C1 detection signal "0", C2 control signal "1", C3 control signal is "0".

[0028] Next, the DC voltage rises at time t1 V0. Accordingly, the power supply circuit 10 is driven, Va DC voltage, Vc DC voltage and DC voltage Vb is varied as well, a1 each voltage, a2 voltage approaches the voltage a3. In addition, a1 voltage, a2 voltage, a3 and the voltage may be a different

充電されていないために充電電圧Ｖ２もＧＮＤであるとする。検出信号Ｃ１は、実行回路３０が駆動しておらず"０"である。電源ライン９０の電圧Ｖ３はＧＮＤ、検出信号Ｃ１は"０"、制御信号Ｃ２は"１"、制御信号Ｃ３は"０"である。

[００２８]次に、時刻ｔ１で直流電圧Ｖ０が立ち上がる。これに従って、電源回路１０は駆動し、直流電圧Ｖａ、直流電圧Ｖｂおよび直流電圧Ｖｃは同様に変化し、それぞれ電圧ａ１、電圧ａ２、電圧ａ３に近づく。なお、電圧ａ１、電圧ａ２、電圧ａ３は互いに異なる大きさであってもよいし、等しくてもよいし、正電圧、負電圧のどちらでもよい。

[００２９]電源ライン９０には、直流電圧Ｖａが与え less than DP N=0004 greater than られるので、電源ライン９０の電圧Ｖ３は直流電圧Ｖａと同様に変化し、実行回路３０の電源端子に印加される。実行回路３０は、電圧Ｖ３が駆動最低電圧ｄ以上になると正常に駆動できる（時刻ｔ２）。

[００３０]直流電圧Ｖ０が定常状態になると、直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧Ｖｃはそれぞれ電圧ａ１、電圧ａ２、電圧ａ３で一定になる。

[００３１]実行回路３０のＣＰＵ３２は、主メモリ３３に格納されている第１種プログラムを実行して主メモリ３３に格納されているデータを処理する。

[００３２]第１種プログラムの実行を詳しく説明する。第１種プログラムには、ＯＳ（オペレーティングシステム）、放電停止処理を行うプログラム、リジューム処理を行うプログラム、アプリケーションプログラムが含まれる。まず、ＯＳが起動した後、放電停止処理を行うプログラムが実行されることで"１"の制御信号Ｃ２が出力される。次に、後述するリジューム処理を行うプログラムが実行される。次に、アプリケーションプログラムが実行される。アプリケーションプログラムは、例えば、入力部７１から入力されたデータを所定の演算式によって処理してその処理結果を主メモリ３３に格納し、必要なときに主メモリ３３

size from each other, may be equal, a positive voltage, negative voltage can be either.

[0029] The supply line 90, it is less than DP N = 0004 greater than the DC applied voltage Va, V3 line voltage power supply 90 varies the voltage Va as well as DC power supply terminal of circuit 30 runs applied to. Execution circuit 30 can be driven normally with the lowest voltage rises above the driving voltage V3 d (t2 time).

[0030] When the steady state DC voltage V0, Va DC voltage, Vb DC voltage, Vc voltage DC voltage respectively a1, a2 voltage at a constant voltage a3.

[0031] CPU32 execution circuit 30 processes the data that is stored in main memory 33 of the first kind to run a program that is stored in main memory 33.

[0032] In more detail the kind of program execution. The program is the first kind, OS (operating system), a program to stop processing the discharge resume processing program that includes an application program. First, after starting the OS, that program is executed to process the discharge stop "1" is output to the control signal C2. Next, the program is run to process later resumed. Then, the application program is executed. Application program, for example, main memory 33 stores the processing result of processing by a predetermined calculation expression data input unit 71 from input to output to the output 72 from the main memory 33 when needed (eg non-volatile memory (output 72) to write to.)

[0033] Meanwhile, the circuit 60 during charging, the charging voltage Vc in response to DC to stop charging automatically when the charging voltage to the Ve reference voltage V2 (t3 time).

[0034] Then, suddenly becomes the GND V0 is the DC voltage is blocked at time t4. V0 is reduced by a DC voltage, Va DC voltage generated by power supply circuit 10, Vb DC voltage, DC voltage Vc is also close to GND. Furthermore, due to parasitics of the power supply circuit 10, Va DC voltage, Vb DC voltage, DC voltage Vc is a gradual change in comparison with dc voltage V0.

[0035] When the threshold voltage Vb c DC voltage detection circuit 20 detects the signal C1 is "0" to "1". This signal is supplied to the CPU32

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から出力部７２へ出力する（例えば、不揮発性メモリ（出力部７２）へ書き込む）。

[００３３]一方、その間に充電回路６０は、直流電圧Ｖｃを受けて充電し、充電電圧Ｖ２が基準電圧Ｖｅになると自動的に充電を停止する（時刻ｔ３）。

[００３４]次に、時刻ｔ４で直流電圧Ｖ０が遮断されて急激にＧＮＤになる。直流電圧Ｖ０が低下したことによって、電源回路１０が生成する直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧ＶｃもＧＮＤに近づく。なお、電源回路１０の寄生容量等が原因で、直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧Ｖｃの変動は直流電圧Ｖ０と比較して緩やかである。

[００３５]直流電圧Ｖｂが閾値電圧ｃになると、検出回路２０は検出信号Ｃ１を"０"から"１"にする。これによって、実行回路３０のＣＰＵ３２に割込信号が与えられ、ＣＰＵ３２は第２種プログラムをスケジューリングして実行する（時刻ｔ５）。

[００３６]第２種プログラムには、サスペンド処理を行うプログラム、放電処理を行うプログラム、所望の処理結果を得るためのプログラムが含まれる。サスペンド処理とは、入力部７１や出力部７２等を省電力モードに制御（個別ハード省電力制御）する処理であり、サスペンド処理が行われた状態をサスペンド状態と称す。まず、サスペンド処理を行うプログラムが実行されることで入力部７１および出力部７２が省電力モードで動作する。次に、放電処理を行うプログラムが実行されることで実行回路３０は制御信号Ｃ２を"０"にする（時刻ｔ６）。なお、この時点では、電圧Ｖ３は駆動最低電圧ｄ以上なので、実行回路３０は正常に動作できる。次に、所望の処理結果を得るためのプログラムが実行される。このプログラムを実行することによって、ここでは例えば、データ書き込み処理が行われ、第１種プログラムを実行することによって得られた処理結果Ｃ５を主メモリ３３から出力部７２の一である不揮発性メモリへの書き込みが開始される。

interrupt execution circuit 30, CPU32 executes the program schedule and Type 2 (t5 time).

[0036] The first two programs, a program to suspend processing, discharge treatment program that includes a program to achieve desired processing results. Suspend processing, such as power-saving mode control unit 72 input and output section 71 (power saving hardware separately) and the process referred to as suspend the suspension which has undergone treatment. First, section 72 operates in a power saving mode input and output unit 71 is performed by suspending the program for processing. Then circuit 30 is accomplished by executing a program to handle the discharge control signal C2 is "0" to (t6 time). Furthermore, at this point, V3 d minimum voltage over-voltage, so the drive circuit 30 can operate normally run. Next, the program is executed to achieve desired processing results. By running this program, where for example, the data write process is performed, the non-volatile memory 72 is output from the memory 33 of the C5 main results obtained by processing the first kind to run the program Writing is started.

[0037] Thereafter, the lowest voltage which drives the voltage V3 d (t7 time). In this case, the control signal C3 to the output circuit 40 '1 ". Discharge circuit 50 is "1" and receive the control signal C3 to discharge circuit 30 to the power terminal lines running through the charging power supply 90 voltage V2. This minimum voltage greater than d drive voltage V3 rises and power line 90, circuit 30 can continue to run a stable drive. Larger than d because the minimum voltage at the driving voltage V3, the output circuit 40 a control signal C3 "0" when. The discharge circuit 50, "0" and receive a control signal C3, stop the discharge line 90 to charge the power supply voltage V2, the lowest voltage that the drive voltage V3 to d. Repeated the above, the charge voltage V2 is supplemented to the power terminal 30 perform circuit, circuit 30 can execute a program to run properly, you can write to the nonvolatile memory to complete the processing result of C5 possible. Thus, it is possible to prevent a loss of protection to non-volatile memory by writing a program to achieve the desired processing results obtained by a C5 processing results of the first kind to run the program.

[0038] Then, each iteration of the discharge circuit 50 discharges stop discharging charge stored in

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[００３７]その後、電圧Ｖ３が駆動最低電圧ｄになる（時刻ｔ７）。このとき、出力回路４０は制御信号Ｃ３を"１"にする。放電回路５０は、"１"の制御信号Ｃ３を受けると、充電電圧Ｖ２を電源ライン９０を介して実行回路３０の電源端子へ放電する。これによって、電源ライン９０の電圧Ｖ３が上昇して駆動最低電圧ｄより大きくなり、実行回路３０は安定した駆動を続けることができる。電圧Ｖ３が駆動最低電圧ｄより大きくなったので、出力回路４０は制御信号Ｃ３を"０"にする。放電回路５０は、"０"の制御信号Ｃ３を受けると、充電電圧Ｖ２を電源ライン９０に放電するのを停止し、電圧Ｖ３が駆動最低電圧ｄになる。以上のことが繰り返され、実行回路３０の電源端子に充電電圧Ｖ２が補われ、実行回路３０はプログラムを正常に実行することができ、処理結果Ｃ５の不揮発性メモリへの書き込みを完了することができる。このように、第１種プログラムを実行することによって得られた処理結果Ｃ５を所望の処理結果を得るためのプログラムによって不揮発性メモリへ書き込んで保護して消失することを防ぐことができる。

[００３８]そして、放電回路５０の放電・放電停止が繰り返されるごとに、充電回路６０に充電された電荷は少なくなっていき、時刻ｔ８では、放電回路５０が放電しても、電圧Ｖ３は駆動最低電圧ｄ以上にならず、実行回路３０は駆動できずに停止する。

[００３９]なお、時刻ｔ８でプログラム実行装置が誤動作すれば、操作者はリセット回路８０の押しボタンを押してリセットすればよい。

[００４０]以上のように、実行回路３０の電源端子には放電回路５０から放電された電圧が補われることで、実行回路３０は時刻ｔ８まで安定して駆動でき、この間に、第１種プログラムを実行することによって得られた処理結果Ｃ５を第２種プログラムの所望の処理結果を得るためのプログラムによって保護して消失することを防ぐことができ、操作者は所望の処理結果Ｃ５を得ることができる。

the charging circuit 60 to go is less, at time t8, even if the discharge circuit 50 discharges, the voltage d not more than the lowest voltage V3 is the driving circuit 30 driving the execution is not stopped.

[0039] Furthermore, if the equipment malfunctions in the program execution time t8, the operator may be reset by pressing the push button reset circuit 80.

[0040] As described above, the supply terminals of circuit 30 compensates the voltage at the execution were discharged from the discharge circuit 50, circuit 30 can drive to run stable until time t8, during which, in You can prevent loss and protect the program for desired processing results of the second kind of program the C5 treatment results obtained by running one program, the operator C5 desired processing results can be obtained.

[0041] Incidentally, during the time from the time t7 t8, again, rises to a DC voltage V0 (t9 time Figure 8). Accordingly, the power supply circuit 10 is driven, Va DC voltage, Vc DC voltage and DC voltage Vb is varied as well, a1 each voltage, a2 voltage approaches the voltage a3.

[0042] c is greater than the threshold voltage Vb is the DC voltage detection circuit 20 detects the signal C1 is "0" to. This is less than DP N = 0005 greater than signal is applied to the CPU32 interrupt execution circuit 30, CPU32 program resume do the first kind of program, a program to stop processing the discharge, the application program in order to schedule running (t10 time). And resume processing, the processing means processing the last return to suspend state, a state referred to as the state resume resume processing was done. Basically, control returns to the state immediately before the suspend process unit 72 and outputs 71 inputs (return control hardware separately) will do, here are 72 and an output unit 71 inputs Va DC voltage, DC voltage Vb, a1-voltage direct-current voltage Vc, a2 voltage returns to its original natural state if the voltage becomes a3. Later time t10, V3 voltage line voltage power supply 90 is sufficiently close to the a1, even without resorting to charging voltage V2, the execution in a state circuit 30 can drive normally. Therefore, the program is run to process the discharge stopped, CPU32 of the control signal C2 from the execution circuit 30 receives an interrupt signal as soon as "1". The output circuit

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[００４１]ところで、時刻ｔ７から時刻ｔ８の間に、再び、直流電圧Ｖ０が立ち上がったとする（図８の時刻ｔ９）。これに従って、電源回路１０は駆動し、直流電圧Ｖａ、直流電圧Ｖｂおよび直流電圧Ｖｃは同様に変化し、それぞれ電圧ａ１、電圧ａ２、電圧ａ３に近づく。

[００４２]直流電圧Ｖｂが閾値電圧ｃより大きくなると、検出回路２０は検出信号Ｃ１を"０"にする。これによって、実行回路３０のＣＰＵ３２に割込信号が与え less than DP N=0005 greater than られ、ＣＰＵ３２は第１種プログラムのリジューム処理を行うプログラム、放電停止処理を行うプログラム、アプリケーションプログラムを順にスケジューリングして実行する（時刻ｔ１０）。リジューム処理とは、サスペンド処理を行う直前の状態に戻す処理を意味し、リジューム処理が行われた状態をリジューム状態と称す。基本的には、入力部７１および出力部７２をサスペンド処理を行う直前の状態に戻す制御（個別ハード復帰制御）を行うが、ここでは、入力部７１および出力部７２は直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧Ｖｃが電圧ａ１、電圧ａ２、電圧ａ３になれば自然に元の状態に戻る。時刻ｔ１０後では、電源ライン９０の電圧Ｖ３は充分に電圧ａ１に近づき、充電電圧Ｖ２に頼らなくても、実行回路３０は正常に駆動できる状態にある。そこで、放電停止処理を行うプログラムが実行され、実行回路３０のＣＰＵ３２は割込信号を受けると直ぐに制御信号Ｃ２を"１"にする。出力回路４０は、"１"の制御信号Ｃ２を受けると制御信号Ｃ３を"０"に固定する。放電回路５０は、"０"の制御信号Ｃ３を受けると、充電電圧Ｖ２を電源ライン９０に放電するのを停止する。その後、アプリケーションプログラムが実行される。

[００４３]つまり、サスペンド処理を行うプログラムを実行することによって、入力部７１、出力部７２等を省電力モードで動作させ、充電回路６０の充電量の消費を抑え、実行回路３０をより長く駆動させ、再び、直流電圧Ｖ０が立ち上がるまで、実行回路３０を待機させることができる。これによって、第１種プログラムを実行することによって得られた処理結果Ｃ５を、サスペンド処理

40 is "1" and receive control signals C2 and C3 control signal "0" fixed. The discharge circuit 50, "0" and receive a control signal C3 to stop the discharge line 90 to supply charging voltage V2. Thereafter, the application program is executed.

[0043] In other words, by executing a program to suspend processing, the input unit 71, is operated in power saving mode, etc. The output unit 72, reduces the amount of charge consumed in charging circuit 60, circuit 30 runs longer is driven again until the rise of the DC voltage V0 is possible to wait for the execution circuit 30. This processing results obtained by a C5 you run the program the first kind, it is possible to prevent a loss of protection circuit 30 will be waiting to suspend the processing performed by the program.

[0044] As described above, the first one to run the program c is greater than the threshold voltage DC voltage Vb. C falls below the threshold voltage DC voltage Vb, the second kind with running the program to protect the processing results obtained by running the program in one terminal, run the power circuit 30 in addition to the direct current voltage Va compensate the charge voltage V2 is discharged from the discharge circuit 50. This circuit 30 can perform stable and longer driving, during which prevents the loss of two programs to protect the processing results obtained by running the program the first kind possible.

[0045] In addition, V0 DC voltage instead of blocked, may have been supplied in time t8 t7 ~ 7 times smaller than a small voltage is the lowest drive voltage Va d dc voltage. In this case, even a slight amount of charge in charging circuit 60, the sum of the voltage V2 from a charging voltage Va and DC charging circuit 60, circuit 30 can drive a stable long run.

[0046] Moreover, by repeatedly stopping the discharge discharge discharge circuit 50 described above, it is supplied from the circuit 50 gradually discharges only enough energy to reach the minimum voltage, d is the drive voltage V3, driving can be stably run even slightly longer battery charge circuit 30 of the charging circuit 60.

[0047] In addition, the less amount of charge in a conventional backup power supply, because that loss of processing results obtained by running the program until it can be applied to charge capacitor 63 as a backup supply small amounts of There

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を行うプログラムによって実行回路３０を待機させて保護して消失することを防ぐことができる。

[００４４]以上のように、直流電圧Ｖｂが閾値電圧ｃより大きければ第１種プログラムを実行する。直流電圧Ｖｂが閾値電圧ｃ以下になると、第１種プログラムを実行することによって得られた処理結果を保護する第２種プログラムを実行するとともに、実行回路３０の電源端子には直流電圧Ｖａに加えて放電回路５０から放電された充電電圧Ｖ２が補われる。これによって、実行回路３０はより長く安定して駆動することができ、その間に、第１種プログラムを実行することによって得られた処理結果を第２種プログラムによって保護して消失することを防ぐことができる。

[００４５]また、直流電圧Ｖ０は遮断されたのではなく、直流電圧Ｖａが駆動最低電圧ｄより小さい僅かな電圧が図７の時刻ｔ７～時刻ｔ８で供給されている場合がある。この場合、充電回路６０の充電量が僅かであっても、直流電圧Ｖａと充電回路６０からの充電電圧Ｖ２との合計により、実行回路３０は長く安定して駆動できる。

[００４６]また、先に説明した放電回路５０の放電・放電停止の繰り返しによって、電圧Ｖ３が駆動最低電圧ｄに達する分だけの電力量が放電回路５０から少しずつ供給されるので、充電回路６０の充電量が僅かでも実行回路３０を長く安定して駆動させることができる。

[００４７]また、従来ではバックアップ電源の充電量が少なければ、それまでのプログラムの実行によって得られた処理結果が消失してしまうので、バックアップ電源として充電容量の少ないコンデンサ６３を適用できなかったが、本発明では充電量が僅かでも上述のように処理結果を保護して消失することを防ぐことができる。したがって、バックアップ電源としてコンデンサ６３を適用することができ、しかも、充電回路６０を寿命のないバックアップ電源として構成でき、充電池のように液漏れがなく、メンテナンスを行う必要がない。

[００４８]また、出力回路４０は、図２のような回路に代えて、制御信号Ｃ２が"１"になったとき

was no in the present invention can prevent loss and protect the results of processing as described above but only charged the amount. Thus, the capacitor 63 can be applied as backup power, yet can be configured as a backup supply of life without charging circuit 60, so there is no leakage of battery, it needs no maintenance.

[0048] In addition, the output circuit 40, in place of the circuit shown in Figure 2, the control signal C2 is "1" when the control signal C3 "0" is held, the control signal C2 " 0 "control signal C3 to less than d when the minimum voltage in the drive voltage V3" 1 "may be held in the latch circuit. And replacing the latch circuit, t8 t7 ~ time 7 time is always "1". Thus, the output circuit 40, a preset threshold voltage circuit 30 can operate the power supply voltage at V3 is running (in the above description is equal to the minimum drive voltage d) when the "0" Controlling discharge circuit 50 outputs the signal C3. This minimum voltage until the drive voltage V3 d circuit 30 is driven by the execution is only a DC voltage Va, the minute circuit 30 can be executed to drive longer stable. In addition, pre-set threshold voltage, minimum voltage may be larger than d drive.

[0049] Moreover, after blocking the DC voltage V0, to maintain the state of the circuit 30 since running in the suspended state, without needing to restart the OS, the program immediately after the dc voltage V0 is turned can be launched.

[0050] Also, if you replace the latch circuit to output circuit 40, to enter into this latch circuit reset signal from the circuit 80, by pressing the push button reset circuit 80 by the operator, C3 control signal "0" may be configured to reset.

[0051] Moreover, by omitting the output circuit 40, circuit 50 may be applied to the discharge control signal C2. In this case, "0" signal of the control signal C2 is discharged, "1" and the discharge stop signal of the control signal C2, in keeping with this, the discharge circuit 50 is "0" and receive a charging voltage control signal C2 The discharge circuit 30 to the power terminal to power line 90 running through the V2, "1" to stop the discharge line 90 to charge the power supply voltage V2 and C2 receive the control signal.

[0052] In addition, the discharge circuit 50, the control signal C3 "0" to "1" in line 90 continues to discharge the power supply voltage V2 to rise if you take charge of the control signal C3 from "1"

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制御信号Ｃ３を"０"に保持し、制御信号Ｃ２が"０"の状態で電圧Ｖ３が駆動最低電圧ｄ以下になったとき制御信号Ｃ３を"１"に保持するラッチ回路でもよい。ラッチ回路に代えると、図７の時刻ｔ７～時刻ｔ８は常に"１"である。このように、出力回路４０は、電源端子の電圧Ｖ３が実行回路３０が動作可能な予め設定された閾値電圧（以上の説明では駆動最低電圧ｄに等しい）になったときに"０"の制御信号Ｃ３を放電回路５０に出力する。これによって、電圧Ｖ３が駆動最低電圧ｄになるまでは実行回路３０は直流電圧Ｖａのみで駆動するので、その分、実行回路３０はさらに長く安定して駆動することができる。なお、予め設定された閾値電圧は、駆動最低電圧ｄより大きくてもよい。

[００４９]また、直流電圧Ｖ０を遮断した後、サスペンド状態で実行回路３０の状態を保持するので、ＯＳを再び起動する必要がなく、直流電圧Ｖ０が投入された直後にプログラムを直ちに立ち上げることができる。

[００５０]また、出力回路４０をラッチ回路に置き換えた場合、リセット回路８０からの信号をこのラッチ回路に入力して、操作者がリセット回路８０の押しボタンを押せば、制御信号Ｃ３を"０"にリセットする構成にしてもよい。

[００５１]また、出力回路４０を省略して、制御信号Ｃ２を放電回路５０に与えても良い。この場合、"０"の制御信号Ｃ２が放電信号、"１"の制御信号Ｃ２が放電停止信号であり、これに合わせて、放電回路５０は、"０"の制御信号Ｃ２を受けると充電電圧Ｖ２を電源ライン９０を介して実行回路３０の電源端子へ放電し、"１"の制御信号Ｃ２を受けると充電電圧Ｖ２を電源ライン９０に放電するのを停止する。

[００５２]また、放電回路５０は、制御信号Ｃ３の"０"から"１"への立ち上がりを受ければ充電電圧Ｖ２を電源ライン９０に放電し続け、制御信号Ｃ３の"１"から"０"への立ち下がりを受ければ放電を停止し続けるラッチ機能を有していてもよい。この場合、リ less than DP N=0006 greater than セット回路８０からの信号を放電回路５０に入力し

"0" may also have a latching feature to stay down if you take the fall for discharge. In this case, enter 50 discharge circuit a signal from the circuit 80 re-less than DP N = 0006 greater than a set, pressing the pushbutton circuit 80 is reset by the operator, even if configured to stop the discharge of the above Good.

[0053] Further, Va DC voltage, Vb DC voltage, Vc may be a DC voltage of the same DC power supply voltage.

[0054] may also charge a capacitor instead of a battery charging circuit 60 63.

[0055] The program of the second kind, other than a program or a program to suspend processing of the above-mentioned data write operation, if it contains a good program to protect the result. For example, programs may be displayed on the LCD panel to make an output unit 72 the C5 result. Alternatively, run by resetting circuit 30, may be a program to restore the initial state as if the reset signal is input to C6. In this case, by resetting to prevent runaway programs driven by the unstable second kind, for example, are destroyed by processing the result is already written in the nonvolatile memory portion 72 of the first kind by the program output it can be prevented.

[0056] In addition, the discharge signal and the discharge stop signal of the control signal C2, in the example above is generated by the CPU32 instruction program includes two of the first kind and the programs, instead of this, run detection circuit 30 is the signal C1 is "1", "0" includes a separate circuit to generate, depending on the stop signal may be generated and discharged by said discharge signal circuit to run the program with Type 2 CPU32.

[0057] The program also includes a program to capture one of the main circuit 30 in memory 33 execute the processing result is written into the nonvolatile memory immediately after the DC voltage V0 rises, the first two programs are described which may include writing a program for processing data. According to this, first, the DC voltage V0 is interrupted at time t4 in Figure 7, as described above, is executed by writing a program to process the data in the first two programs, one of the program be written to nonvolatile memory 72 outputs the main memory 33 from processing the results obtained by C5 run. Then V0 is the DC voltage rises again, the program is executed by

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て、操作者がリセット回路８０の押しボタンを押せば、上記の放電を停止する構成にしてもよい。

[００５３]また、直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧Ｖｃは同一の直流電源電圧であってもよい。

[００５４]また、充電回路６０のコンデンサ６３を充電池に代えてもよい。

[００５５]また、第２種プログラムは、上述のデータ書き込み処理を行うプログラムやサスペンド処理を行うプログラム以外の、処理結果を保護するプログラムを含んでいればよい。例えば、処理結果Ｃ５を出力部７２の一である液晶パネルに表示させるためのプログラムでもよい。あるいは、実行回路３０をリセットすることによって、リセット信号Ｃ６が入力された場合と同じ初期状態に戻すためのプログラムであってもよい。この場合、リセットすることによって、不安定な駆動による第２種プログラムの暴走を防ぎ、例えば、第１種プログラムによって出力部７２の一である不揮発性メモリに既に書き込まれた処理結果が破壊されることを防ぐことができる。

[００５６]また、制御信号Ｃ２の放電信号および放電停止信号は、上述の例では第１種プログラムや第２種プログラムに含まれる命令によってＣＰＵ３２が生成するが、これに代えて、実行回路３０は検出信号Ｃ１の"１"、"０"に応じて生成する別回路を含み、ＣＰＵ３２が第２種プログラムを実行するとともに当該別回路が放電信号および放電停止信号を生成してもよい。

[００５７]また、第１種プログラムは直流電圧Ｖ０が立ち上がった直後に不揮発性メモリに書き込まれた処理結果を実行回路３０の主メモリ３３に取り込むプログラムを含み、第２種プログラムは上述のデータ書き込み処理を行うプログラムを含んでいてもよい。これによれば、まず、図７の時刻ｔ４において直流電圧Ｖ０が遮断されると、上述のように、第２種プログラム内のデータ書き込み処理を行うプログラムが実行されることによって、第１種プログラムを実行することによって得られた処理結果Ｃ５が主メモリ３３から出力部７２の不揮発性メモリに書き込まれる。その後、再

the above process include the result of the first kind in the program is written to main memory 33 from the non-volatile memory and C5 result. This, even below the minimum voltage d is the drive voltage V3 rises before the DC voltage V0, the application program that is included in the program is the first kind, and C5 as the initial treatment results were mainly written in the memory 33, the time can stand up in the same condition as before t4.

[0058] (2 Embodiment) In the first embodiment, a DC voltage V0 is shut off during program execution, resuming from the state when entering a suspended state, or execution of the program is interrupted, the charging circuit 60少Nakattari of charge, for any other reasons, might not work properly program. Does not work correctly in the program and resume it becomes a DC voltage V0 is turned back, it still would be a program does not work correctly.

[0059] In other words, conventional and shut off the power from the outside if it is working properly the program, if the power on again, it is possible to run properly have been started from the beginning of the program. However, the suspended state in the first embodiment described, if a resume condition persists, even if the power shut off the power again from the outside, the program caused a problem that does not work properly.

[0060] In order to solve the above problems, unless the program is working properly, reset the circuit 30 when an operation execution process and suspend resume (suspend reset, resume reset).

[0061] First, described with reference to Figures 9 to 12 to suspend reset. The first kind of program is running, turn on the flags where malfunction-prone. An example of when you turn on the flags where malfunction is likely to occur, are listed in Figures 9 through 11. For example, as shown in Figure 9, CPU32 has just started the OS (step S11), and on the flag (Step S12), and other application programs to run. Then, after a predetermined time has elapsed since the flag on (step S13), to flag off (step S14). Alternatively, as shown in Figure 10, CPU32 executes instructions Furaguon the application program (step S21). This flag is turned on (step S22). Next, CPU32 executes instructions Furaguofu the application program (step S23). This flag is turned off (step

び直流電圧Ｖ０が立ち上がると、第１種プログラム内の上記の処理結果を取り込むプログラムが実行されることによって、処理結果Ｃ５が不揮発性メモリから主メモリ３３に書き込まれる。これによって、直流電圧Ｖ０が立ち上がる前に電圧Ｖ３が駆動最低電圧ｄを下回ったとしても、第１種プログラムに含まれるアプリケーションプログラムは、主メモリ３３に書き込まれた処理結果Ｃ５を初期値として、時刻ｔ４直前と同じ状態で立ち上がることができる。

[００５８]（実施の形態２）実施の形態１において、プログラムの実行中に直流電圧Ｖ０が遮断され、リジューム状態からサスペンド状態に入るとき、プログラムの実行が中断されたり、充電回路６０の充電量が少なかったり、その他の何らかの原因により、プログラムが正常に動作しない可能性がある。プログラムが正常に動作しない状態で、再び直流電圧Ｖ０が投入されてリジューム状態になると、プログラムが正常に動作しない状態が続くことになる。

[００５９]つまり、従来ではプログラムが正常に動作していなければ外部からの電源を遮断して、再び電源を投入すれば、プログラムが始めから起動されて正常に動作させることができる。しかし、実施の形態１で説明したサスペンド状態、レジューム状態が繰り返されれば、外部からの電源を遮断して再び投入しても、プログラムは正常に動作しないという問題点が生じる。

[００６０]そこで、上記問題点を解決するために、プログラムが正常に動作していなければ、サスペンド処理やリジューム処理を行うときに実行回路３０をリセットする（サスペンドリセット、リジュームリセット）。

[００６１]まず、サスペンドリセットを図９～図１２を用いて説明する。第１種プログラムの実行中に、誤動作が生じやすいところにフラグをオンする。誤動作が生じやすいところにフラグをオンする場合の例を、図９～図１１に列挙する。例えば、図９に示すように、ＣＰＵ３２はＯＳを起動した直後（ステップＳ１１）、フラグをオンし（ステップＳ１２）、アプリケーションプログラム等を

S24). Alternatively, as shown in Figure 11, CPU32 will resume the process from the start (step S31), and on the flag (step S32), and other application programs to run. Then, after a predetermined time has elapsed since the flag on (step S33), to flag off (step S34). Flag processing, as shown in Figures 9 through 11 above, the program includes the first kind.

[0062] Next, when the suspend process, and reset if the flag is turned on. In more detail using Figure 12, CPU32, when you start the suspend process (step S41), determines whether the flag is turned off (step S42). If the flag is off, CPU32 will continue to suspend processing (step S43). On the other hand, it is considered sufficiently likely that the program does not work properly if your flag is on, CPU32 to perform the reset circuit 30 (step S44). Treatment as shown in Figure 12 are included in the program over the second kind. less than DP N = 0007 greater than

[0063] above, as described in Figures 9 through 12, CPU32 when an operation is suspended (that is, when receiving a signal from the signal off-on), unless the flag is off (ie, in If the results meet the prescribed treatment program for one) and reset the execution circuit 30. This will resume again when the state can automatically avoid state program is not working properly, or does not have to see if that can be suspended by operation.

[0064] Next, an explanation for the 13 resume reset. First, when you start the process resumed (step S51), display processing is performed, such as messages to the user's shell of the OS. To determine whether the display processing is executed correctly (step S52). How to determine, for example, place a pre-condition contains the shell startup file format in the nonvolatile memory can be determined by comparing the results of this launch condition and render the shell. Depending on how such a decision, reset circuit 30 to execute successfully if the shell is running (step S56), otherwise proceeds to step S53.

[0065] In step S53, to determine whether the state is equal to the number of start resuming a previous application launch number. How to check, for example, by storing in main memory 33 as a launch condition that checks the number of application programs started by the suspend process. Then, resuming after the start of treatment can be confirmed by comparing the number of starts that are stored in main memory

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実行する。そして、フラグをオンしてから所定時間経過後（ステップＳ１３）、フラグをオフする（ステップＳ１４）。あるいは、図１０に示すように、ＣＰＵ３２はアプリケーションプログラムのフラグオン命令を実行する（ステップＳ２１）。これによって、フラグをオンする（ステップＳ２２）。次に、ＣＰＵ３２はアプリケーションプログラムのフラグオフ命令を実行する（ステップＳ２３）。これによって、フラグをオフする（ステップＳ２４）。あるいは、図１１に示すように、ＣＰＵ３２はレジューム処理を開始してから（ステップＳ３１）、フラグをオンし（ステップＳ３２）、アプリケーションプログラム等を実行する。そして、フラグをオンしてから所定時間経過後（ステップＳ３３）、フラグをオフする（ステップＳ３４）。以上の図９～図１１に示したようなフラグを立てる処理は、第１種プログラムに含まれる。

[００６２]次に、サスペンド処理を行うときに、フラグがオンしていればリセットを行う。図１２を用いて詳しく説明すると、ＣＰＵ３２は、サスペンド処理を開始すると（ステップＳ４１）、フラグがオフしているかどうかを判断する（ステップＳ４２）。フラグがオフしていれば、ＣＰＵ３２はサスペンド処理を続行する（ステップＳ４３）。一方、フラグがオンしていればプログラムが正常に動作しない可能性が充分に考えられるので、ＣＰＵ３２は実行回路３０をリセットする（ステップＳ４４）。以上の図１２に示したような処理は第２種プログラムに含まれる。 less than DP N=0007 greater than

[００６３]以上、図９～図１２で説明したように、ＣＰＵ３２はサスペンド処理を行うとき（つまり、オン信号からオフ信号を受けるとき）、フラグがオフしていなければ（つまり、第１種プログラムの処理結果が所定条件を満たしていなければ）、実行回路３０をリセットする。これによって、再びリジューム状態になったときに、プログラムが正常に動作していない状態から自動的に回避することができ、操作者がサスペンド状態にすることができるかどうかを確認しなくて済む。

[００６４]次に、リジュームリセットを図１３を用いて説明する。まず、リジューム処理を開始し

33 and the number of application program starts. The confirmation of such methods, different number of state and resume the previous application launch and run the reset circuit 30 (step S56), otherwise proceeds to step S54.

[0066] In step S54, to determine whether the application program is running correctly. Similar to the decision step S52, for example, place a pre-condition to start the application program stored in the file format in the nonvolatile memory can be determined by comparing the results of this launch conditions and execution of application programs. Depending on how such a decision, reset the circuit 30 if it is running properly executed application program (step S56), otherwise continue processing resumed (step S55).

[0067] Further, steps S52 ~ step S54 may be configured to run selectively.

[0068] above, as described in Figure 13, CPU32 when an operation is suspended (that is, when receiving a signal from the signal on-off), non-volatile memory and the processing results of the OS shell or application program must meet certain criteria that are stored in main memory 33, to reset the execution circuit 30. This will resume again when the state can be avoided automatically when no program is running normally, it does not require an operator to start-up program.

[0069] Furthermore, by performing the reset and suspend resume reset, as the first embodiment, to prevent runaway programs driven by the instability of the second kind, obtained by running the program the first kind The results can be protected or treated.

[0070] (Application of the present invention), the program execution apparatus of the present invention may be any device that runs the program, such as factory automation (FA) control device that controls the machine that make up the production line may be applied to a personal computer. Alternatively, among the components of Figure 1, at least the detection circuit 20, circuit 30 runs, charging circuit 60, formed on a single chip discharge circuit 50, DSP (Digital Signal Processor) 1-chip microprocessor such as those referred may be applied to such computers. In particular, from being shut V0 is the DC voltage of 7 (t4 time), to below the d minimum voltage at the driving voltage V3 (t8 time) between, again, a system that frequently has to stand up V0 is the

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たとき（ステップＳ５１）、ＯＳのシェルのユーザーへのメッセージ等の表示処理が行われる。この表示処理が正しく実行されているかどうかを判断する（ステップＳ５２）。判断方法は、例えば、不揮発性メモリにファイル形式でシェルの起動条件を予め格納しておき、この起動条件とシェルの表示処理の結果とを比較することで判断できる。このような判断方法によって、シェルが正常に実行されていなければ実行回路３０をリセットし（ステップＳ５６）、そうでなければステップＳ５３に進む。

[００６５]ステップＳ５３では、アプリケーションの起動数が前回のリジューム状態の起動数に等しいかどうかを確認する。確認方法は、例えば、サスペンド処理によってアプリケーションプログラムの起動数を調べて起動条件として主メモリ３３に格納しておく。そして、リジューム処理の開始後、アプリケーションプログラムの起動数と主メモリ３３に格納されている起動数とを比較することで確認できる。このような確認方法によって、アプリケーションの起動数が前回のリジューム状態と異なれば、実行回路３０をリセットし（ステップＳ５６）、そうでなければステップＳ５４に進む。

[００６６]ステップＳ５４では、アプリケーションプログラムが正しく実行されているかどうかを判断する。判断方法はステップＳ５２同様、例えば、不揮発性メモリにファイル形式でアプリケーションプログラムの起動条件を予め格納しておき、この起動条件とアプリケーションプログラムの実行結果とを比較することで判断できる。このような判断方法によって、アプリケーションプログラムが正常に実行されていなければ実行回路３０をリセットし（ステップＳ５６）、そうでなければリジューム処理を続行する（ステップＳ５５）。

[００６７]なお、ステップＳ５２～ステップＳ５４は、選択的に実行できるように構成してもよい。

[００６８]以上、図１３で説明したように、ＣＰＵ３２はサスペンド処理を行うとき（つまり、オフ信号からオン信号を受けるとき）、ＯＳのシェル

DC voltage Once applied, effective immediately because it can launch the program immediately after the power has a DC voltage V0.

[0071] [Effects of the Invention According to the invention described in claim 1, the first one to run the program first threshold voltage is greater than the DC voltage. Falls below the first threshold voltage DC voltage to run the program with the second seed treatment to protect the results obtained in the program of the first kind, was discharged from the power supply terminals in addition to the DC voltage discharge circuit The charging voltage is compensated. This circuit can run stable for longer than driving, in the meantime, to prevent the loss of two programs to protect the processing results obtained by running the program the first kind possible.

[0072] According to the invention described in claim 2, the circuit will run until the second threshold voltage is driven by the power supply voltage at DC supply voltage. This circuit can be run longer and stable driving.

[0073] According to the invention described in claim 3, reset the circuit by two runs in the first program, by preventing the runaway of two programs, one program of treatment obtained The results can be protected.

[0074] According to the invention described in claim 4, it is possible to work around the state program is not working properly the first kind and second kind.

[0075] According to the invention described in claim 5, run the program because of the second kind for the desired processing results of the first kind instead of the program, but only the desired amount of the charging circuit charging results can be processed. Thus, a sufficient effect can be obtained even if constructed by using a capacitor charging circuit charging a smaller capacity, moreover, can not be configured as a backup power source less than DP N = 0008 greater than the life of the charging circuit.

[0076] According to the invention described in claim 6, it can be used as backup power capacitors, you can get a program execution device that consists of a single chip for backup.

やアプリケーションプログラムの処理結果が不揮発性メモリや主メモリ３３に格納されている所定条件を満たしていなければ、実行回路３０をリセットする。これによって、再びリジューム状態になったときに、プログラムが正常に動作していない状態から自動的に回避することができ、操作者がプログラムの立上げを行う必要がない。

[００６９]また、サスペンドリセットやリジュームリセットを行うことによって、実施の形態１同様、不安定な駆動による第２種プログラムの暴走を防いで、第１種プログラムを実行することによって得られた処理結果を保護することができる。

[００７０]（本発明の適用例）本発明のプログラム実行装置は、プログラムを実行する装置であればよく、例えば、ファクトリーオートメーション（ＦＡ）の生産ラインを構成する機械を制御する制御機器、パーソナルコンピュータなどに適用してもよい。あるいは、図１の構成要素のうち、少なくとも検出回路２０、実行回路３０、充電回路６０、放電回路５０を１チップ上に形成して、ＤＳＰ（Digital Signal Processor）と称されるような１チップマイクロコンピュータなどに適用してもよい。特に、図７の直流電圧Ｖ０が遮断されてから（時刻ｔ４）、電圧Ｖ３が駆動最低電圧ｄを下回るまで（時刻ｔ８）の間に、再び、直流電圧Ｖ０が立ち上がることが頻繁に起こるシステムに適用すれば、直流電圧Ｖ０が投入された直後にプログラムを直ちに立ち上げることができるので効果的である。

[００７１] [発明の効果]請求項１に記載の発明によれば、直流電圧が第１閾値電圧より大きければ第１種プログラムを実行する。直流電圧が第１閾値電圧以下になると、第１種プログラムで得られた処理結果を保護するための第２種プログラムを実行するとともに、電源端子には直流電圧に加えて放電回路から放電された充電電圧が補われる。これによって、実行回路はより長く安定して駆動することができ、その間に、第１種プログラムを実行することによって得られた処理結果を第２種プログラムによって保護して消失することを防ぐことができる。

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[００７２]請求項２に記載の発明によれば、実行回路は、電源端子の電圧が第２閾値電圧になるまでは直流電源電圧で駆動する。これによって、実行回路はさらに長く安定して駆動することができる。

[００７３]請求項３に記載の発明によれば、第２種プログラムで実行回路をリセットすることで、第２種プログラムの暴走を防ぐことによって、第１種プログラムで得られた処理結果を保護することができる。

[００７４]請求項４に記載の発明によれば、第１種および第２種プログラムが正常に動作していない状態から回避することができる。

[００７５]請求項５に記載の発明によれば、第１種プログラムに代えて所望の処理結果を得るための第２種プログラムを実行するので、充電回路の充電容量が僅かでも所望の処理結果を得ることができる。よって、充電回路を充電容量の小さいコンデンサを用いて構成しても充分な効果を得ることができ、しかも、充電回路を寿命の less than DP N=0008 greater than ないバックアップ電源として構成できる。

[００７６]請求項６に記載の発明によれば、コンデンサをバックアップ電源として用いることができるので、バックアップ機能付きの１チップで構成されたプログラム実行装置を得ることができる。

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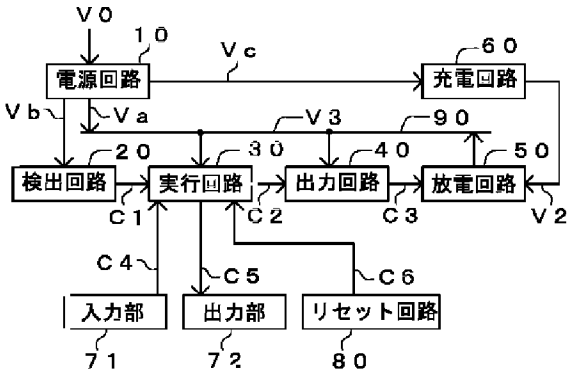
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(54)【発明の名称】　プログラム実行装置

(57)【要約】
【課題】　バックアップ電源の少ない充電量でも処理結果が消失してしまうことを防ぐことができるプログラム実行装置を得る。
【解決手段】　検出回路２０は、直流電圧Ｖｂが第１閾値閾電圧より大きいときに”０”の検出信号Ｃ１、そうでないときに”１”の検出信号Ｃ１を出力する。実行回路３０は、直流電圧Ｖａを電源端子に受けて駆動し、”０”の検出信号Ｃ１を受けると第１種プログラムを実行し、”１”の検出信号Ｃ１を受けると第１種プログラムを実行することによって得られた処理結果を保護する第２種プログラムを実行するとともに制御信号Ｃ２を生成する。充電回路６０は直流電圧Ｖｃを充電する。放電回路５０は制御信号Ｃ２に基づいて充電電圧Ｖ２を実行回路３０の電源端子へ放電する。



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【特許請求の範囲】
【請求項１】　直流電源電圧を受け、当該直流電源電圧が第１閾値閾電圧より大きいときにオン信号、そうでないときにオフ信号を出力する検出回路と、
前記直流電源電圧を電源端子に受けて駆動し、前記オン信号を受けると第１種プログラムを実行し、前記オフ信号を受けると前記第１種プログラムを実行することによって得られた処理結果を保護する第２種プログラムを実行するとともに放電信号を生成する実行回路と、
前記直流電源電圧を充電する充電回路と、
前記放電信号を受けると、前記充電回路の充電電圧を前記電源端子へ放電する放電回路と、を備えたプログラム実行装置。
【請求項２】　前記電源端子の電圧が当該実行回路が動作可能な予め設定された第２閾値電圧になったときに前記放電信号を前記放電回路に出力する出力回路をさらに備えた請求項１記載のプログラム実行装置。
【請求項３】　前記第２種プログラムは前記実行回路をリセットする処理を含む請求項１記載のプログラム実行装置。
【請求項４】　前記第１種および第２種プログラムは、当該第１種および第２種プログラムの処理結果が所定条件を満たしていなければ、前記実行回路をリセットする処理を含む請求項１記載のプログラム実行装置。
【請求項５】　前記充電回路は、前記直流電源電圧を充電するコンデンサを含む請求項１記載のプログラム実行装置。
【請求項６】　前記検出回路、前記実行回路、前記充電回路、前記放電回路は１チップ上に形成されている請求項５記載のプログラム実行装置。
【発明の詳細な説明】
【０００１】
【発明が属する技術分野】本発明は、コンピュータプログラム（以下、単に「プログラム」と称す）を実行するプログラム実行装置に関する。
【０００２】
【従来の技術】従来では、プログラムの実行中に外部からの電源が遮断されたとき、即座にバックアップ電源に切り替えて引き続いて同じプログラムを実行する。
【０００３】
【発明が解決しようとする課題】しかしながら、バックアップ電源の充電量が少なければ、プログラム実行装置の駆動が不安定になり、それまでのプログラムの実行によって得られた処理結果が消失してしまうという問題点があった。
【０００４】本発明は上記の問題点を解決するためになされたものであり、バックアップ電源の少ない充電量でも処理結果が消失してしまうことを防ぐことができるプログラム実行装置を得ることを目的とする。
【０００５】
【課題を解決するための手段】請求項１に記載の課題解決手段は、直流電源電圧を受け、当該直流電源電圧が第１閾値閾電圧より大きいときにオン信号、そうでないときにオフ信号を出力する検出回路と、前記直流電源電圧を電源端子に受けて駆動し、前記オン信号を受けると第１種プログラムを実行し、前記オフ信号を受けると前記第１種プログラムを実行することによって得られた処理結果を保護する第２種プログラムを実行するとともに放電信号を生成する実行回路と、　前記直流電源電圧を充電する充電回路と、前記放電信号を受けると、前記充電回路の充電電圧を前記電源端子へ放電する放電回路とを備える。
【０００６】請求項２に記載の課題解決手段は、前記電源端子の電圧が当該実行回路が動作可能な予め設定された第２閾値電圧になったときに前記放電信号を前記放電回路に出力する出力回路をさらに備える。
【０００７】請求項３に記載の課題解決手段において、前記第２種プログラムは前記実行回路をリセットする処理を含む。
【０００８】請求項４に記載の課題解決手段において、前記第１種および第２種プログラムは、当該第１種および第２種プログラムの処理結果が所定条件を満たしていなければ、前記実行回路をリセットする処理を含む。
【０００９】請求項５に記載の課題解決手段において、前記充電回路は、前記直流電源電圧を充電するコンデンサを含む。
【００１０】請求項６に記載の課題解決手段において、前記検出回路、前記実行回路、前記充電回路、前記放電回路は１チップ上に形成されている。
【００１１】
【発明の実施の形態】（実施の形態１）図１は本発明の実施の形態１のプログラム実行装置を示すブロック図である。実施の形態１のプログラム実行装置は、電源回路１０、検出回路２０、実行回路３０、出力回路４０、放電回路５０、充電回路６０、入力部７１、出力部７２、リセット回路８０および電源ライン９０を含む。
【００１２】まず、実施の形態１のプログラム実行装置の構成について説明する。
【００１３】電源回路１０は外部から直流電圧Ｖ０を受け、直流電圧Ｖａ、直流電圧Ｖｂおよび直流電圧Ｖｃを生成して出力する。
【００１４】検出回路２０は直流電圧Ｖｂを受け、検出信号Ｃ１を生成して出力する。検出回路２０は、例えば図２に示すようなインバータ機能を有する回路である。図２において、Ｖｄは電源回路１０が生成する直流電圧、その他の符号は図１に対応している。検出回路２０は、図２のような回路以外であってもよく、直流電圧Ｖｂが閾値電圧ｃより大きいとき”０”の検出信号Ｃ１を出力し、そうでないとき”１”の検出信号Ｃ１を出力するものであればよい。

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【００１５】図１の実行回路３０は、電源端子が電源ライン９０に接続され、検出信号Ｃ１を受け、制御信号Ｃ２を生成して出力する。また、実行回路３０は、入力部７１から入力信号Ｃ４を受け、処理結果Ｃ５を生成して出力部７２に出力する。

【００１６】図３は、実行回路３０の内部構成を示すブロック図である。実行回路３０は割込信号生成回路３１、ＣＰＵ３２および主メモリ３３を含む。割込信号生成回路３１は、検出信号Ｃ１およびＣＰＵ３２からの信号Ｄ１を受け、検出信号Ｃ１および信号Ｄ１の排他的論理和を信号Ｄ２としてＣＰＵ３２に出力する。主メモリ３３およびＣＰＵ３２の動作を図４および図５を用いて説明する。図４に示すように、検出信号Ｃ１が”１”で信号Ｄ１が”０”のとき、信号Ｄ２は”１”である（時刻ｔａ）。この状態で、検出信号Ｃ１が”０”になると、割込信号生成回路３１は信号Ｄ２を立ち下げる（時刻ｔｂ）。ＣＰＵ３２は信号Ｄ２の立ち下がりを受けると、信号Ｄ１を反転させて”１”にする。これによって、信号Ｄ２は再び”１”になる（時刻ｔｃ）。また、図５に示すように、検出信号Ｃ１が”０”で信号Ｄ１が”１”のとき、信号Ｄ２は”１”である（時刻ｔａ）。この状態で、検出信号Ｃ１が”１”になると、割込信号生成回路３１は信号Ｄ２を立ち下げる（時刻ｔｂ）。ＣＰＵ３２は信号Ｄ２の立ち下がりを受けると、信号Ｄ１を反転させて”０”にする。これによって、信号Ｄ２は再び”１”になる（時刻ｔｃ）。以上のように、検出信号Ｃ１が”０”から”１”あるいは”１”から”０”に変化する度に、ＣＰＵ３２は信号Ｄ２の立ち下がりパルス（割込信号）を受けることになる。

【００１７】また、ＣＰＵ３２は主メモリ３３との間でデータやプログラムを実行することによって得られた処理結果をやりとりしたり、主メモリ３３からプログラムの命令を取り込んだりする。主メモリ３３に格納されているデータやプログラムは入力部７１（図１）から与えられる。

【００１８】出力回路４０は、電源ライン９０に接続され、制御信号Ｃ２を受け、制御信号Ｃ３を出力する。出力回路４０の動作は、制御信号Ｃ２が”１”の場合は制御信号Ｃ３を”０”に固定し、制御信号Ｃ２が”０”の場合は電圧Ｖ３が駆動最低電圧ｄより大きいとき制御信号Ｃ３を”０”にし、電圧Ｖ３が駆動最低電圧ｄ以下のとき制御信号Ｃ３を”１”にする。

【００１９】充電回路６０は直流電圧Ｖｃを受けて充電する。この充電電圧がＶ２である。図６に充電回路６０の内部構成の例を示す。充電回路６０は、充電完了検出回路６１、充電回路本体６２およびコンデンサ６３を含む。図６において、Ｖｅは電源回路１０が生成する基準直流電圧、その他の符号は図１に対応している。充電回路本体６２は直流電圧Ｖｃを受けてコンデンサ６３に充電する。充電完了検出回路６１は、充電電圧Ｖ２が基準電圧Ｖｅに等しくなるように、充電回路本体６２を制御する。これによって、充電回路６０は充電電圧Ｖ２が基準電圧Ｖｅに等しくなると自動的に充電を停止する。充電回路６０は、図６のような回路以外であってもよく、直流電圧Ｖｃを受けて充電できるものであればよい。

【００２０】図１の放電回路５０は、制御信号Ｃ３および充電電圧Ｖ２を受け、制御信号Ｃ３に応じて充電電圧Ｖ２を電源ライン９０に出力する。なお、放電回路５０は充電電圧Ｖ２を、そのまま電源ライン９０に出力してもよいし、所定の電圧に変換して電源ライン９０に出力してもよい。

【００２１】入力部７１は、例えば、外部の周辺装置からのデータを入力する入力インタフェース、あるいはキーボード、あるいはマウス、あるいはタッチパネルである。

【００２２】出力部７２は、実行回路３０がプログラムを実行することによって得られた処理結果を出力する装置であり、例えば、外部の周辺装置へデータを出力する出力インタフェース、あるいは液晶パネル、あるいはＣＲＴ、あるいはフラッシュメモリ等の不揮発性メモリである。

【００２３】リセット回路８０は押しボタンスイッチを含み、例えばプログラムが暴走したときに操作者が押しボタンスイッチを押すことによって実行回路３０をリセットする。

【００２４】なお、”０”の検出信号Ｃ１がオン信号であり、”１”の検出信号Ｃ１がオフ信号であり、”１”の制御信号Ｃ３および”０”の制御信号Ｃ２が放電信号である。また、直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧Ｖｃ、直流電圧Ｖｄおよび基準電圧Ｖｅは直流電源電圧の概念に含まれる。

【００２５】また、全ての図の各信号において、”０”および”１”の一方が高電位、他方が低電位である。

【００２６】次に、全体の動作を図７を用いて説明する。

【００２７】まず、時刻ｔ０では、直流電圧Ｖ０はＧＮＤ（接地電位）であり、充電回路６０は全く充電されていないために充電電圧Ｖ２もＧＮＤであるとする。検出信号Ｃ１は、実行回路３０が駆動しておらず”０”である。電源ライン９０の電圧Ｖ３はＧＮＤ、検出信号Ｃ１は”０”、制御信号Ｃ２は”１”、制御信号Ｃ３は”０”である。

【００２８】次に、時刻ｔ１で直流電圧Ｖ０が立ち上がる。これに従って、電源回路１０は駆動し、直流電圧Ｖａ、直流電圧Ｖｂおよび直流電圧Ｖｃは同様に変化し、それぞれ電圧ａ１、電圧ａ２、電圧ａ３に近づく。なお、電圧ａ１、電圧ａ２、電圧ａ３は互いに異なる大きさであってもよいし、等しくてもよいし、正電圧、負電圧のどちらでもよい。

【００２９】電源ライン９０には、直流電圧Ｖａが与え

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られるので、電源ライン９０の電圧Ｖ３は直流電圧Ｖａと同様に変化し、実行回路３０の電源端子に印加される。実行回路３０は、電圧Ｖ３が駆動最低電圧ｄ以上になると正常に駆動できる（時刻ｔ２）。

【００３０】直流電圧Ｖ０が定常状態になると、直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧Ｖｃはそれぞれ電圧ａ１、電圧ａ２、電圧ａ３で一定になる。

【００３１】実行回路３０のＣＰＵ３２は、主メモリ３３に格納されている第１種プログラムを実行して主メモリ３３に格納されているデータを処理する。

【００３２】第１種プログラムの実行を詳しく説明する。第１種プログラムには、ＯＳ（オペレーティングシステム）、放電停止処理を行うプログラム、リジューム処理を行うプログラム、アプリケーションプログラムが含まれる。まず、ＯＳが起動した後、放電停止処理を行うプログラムが実行されることで”１”の制御信号Ｃ２が出力される。次に、後述するリジューム処理を行うプログラムが実行される。次に、アプリケーションプログラムが実行される。アプリケーションプログラムは、例えば、入力部７１から入力されたデータを所定の演算式によって処理してその処理結果を主メモリ３３に格納し、必要なときに主メモリ３３から出力部７２へ出力する（例えば、不揮発性メモリ（出力部７２）へ書き込む）。

【００３３】一方、その間に充電回路６０は、直流電圧Ｖｃを受けて充電し、充電電圧Ｖ２が基準電圧Ｖｅになると自動的に充電を停止する（時刻ｔ３）。

【００３４】次に、時刻ｔ４で直流電圧Ｖ０が遮断されて急激にＧＮＤになる。直流電圧Ｖ０が低下したことによって、電源回路１０が生成する直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧ＶｃもＧＮＤに近づく。なお、電源回路１０の寄生容量等が原因で、直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧Ｖｃの変動は直流電圧Ｖ０と比較して緩やかである。

【００３５】直流電圧Ｖｂが閾値電圧ｃになると、検出回路２０は検出信号Ｃ１を”０”から”１”にする。これによって、実行回路３０のＣＰＵ３２に割込信号が与えられ、ＣＰＵ３２は第２種プログラムをスケジューリングして実行する（時刻ｔ５）。

【００３６】第２種プログラムには、サスペンド処理を行うプログラム、放電処理を行うプログラム、所望の処理結果を得るためのプログラムが含まれる。サスペンド処理とは、入力部７１や出力部７２等を省電力モードに制御（個別ハード省電力制御）する処理であり、サスペンド処理が行われた状態をサスペンド状態と称す。まず、サスペンド処理を行うプログラムが実行されることで入力部７１および出力部７２が省電力モードで動作する。次に、放電処理を行うプログラムが実行されることで実行回路３０は制御信号Ｃ２を”０”にする（時刻ｔ６）。なお、この時点では、電圧Ｖ３は駆動最低電圧ｄ以上なので、実行回路３０は正常に動作できる。次に、所望の処理結果を得るためのプログラムが実行される。このプログラムを実行することによって、ここでは例えば、データ書き込み処理が行われ、第１種プログラムを実行することによって得られた処理結果Ｃ５を主メモリ３３から出力部７２の一である不揮発性メモリへの書き込みが開始される。

【００３７】その後、電圧Ｖ３が駆動最低電圧ｄになる（時刻ｔ７）。このとき、出力回路４０は制御信号Ｃ３を”１”にする。放電回路５０は、”１”の制御信号Ｃ３を受けると、充電電圧Ｖ２を電源ライン９０を介して実行回路３０の電源端子へ放電する。これによって、電源ライン９０の電圧Ｖ３が上昇して駆動最低電圧ｄより大きくなり、実行回路３０は安定した駆動を続けることができる。電圧Ｖ３が駆動最低電圧ｄより大きくなったので、出力回路４０は制御信号Ｃ３を”０”にする。放電回路５０は、”０”の制御信号Ｃ３を受けると、充電電圧Ｖ２を電源ライン９０に放電するのを停止し、電圧Ｖ３が駆動最低電圧ｄになる。以上のことが繰り返され、実行回路３０の電源端子に充電電圧Ｖ２が補われ、実行回路３０はプログラムを正常に実行することができ、処理結果Ｃ５の不揮発性メモリへの書き込みを完了することができる。このように、第１種プログラムを実行することによって得られた処理結果Ｃ５を所望の処理結果を得るためのプログラムによって不揮発性メモリへ書き込んで保護して消失することを防ぐことができる。

【００３８】そして、放電回路５０の放電・放電停止が繰り返されるごとに、充電回路６０に充電された電荷は少なくなっていき、時刻ｔ８では、放電回路５０が放電しても、電圧Ｖ３は駆動最低電圧ｄ以上にならず、実行回路３０は駆動できずに停止する。

【００３９】なお、時刻ｔ８でプログラム実行装置が誤動作すれば、操作者はリセット回路８０の押しボタンを押してリセットすればよい。

【００４０】以上のように、実行回路３０の電源端子には放電回路５０から放電された電圧が補われることで、実行回路３０は時刻ｔ８まで安定して駆動でき、この間に、第１種プログラムを実行することによって得られた処理結果Ｃ５を第２種プログラムの所望の処理結果を得るためのプログラムによって保護して消失することを防ぐことができ、操作者は所望の処理結果Ｃ５を得ることができる。

【００４１】ところで、時刻ｔ７から時刻ｔ８の間に、再び、直流電圧Ｖ０が立ち上がったとする（図８の時刻ｔ９）。これに従って、電源回路１０は駆動し、直流電圧Ｖａ、直流電圧Ｖｂおよび直流電圧Ｖｃは同様に変化し、それぞれ電圧ａ１、電圧ａ２、電圧ａ３に近づく。

【００４２】直流電圧Ｖｂが閾値電圧ｃより大きくなると、検出回路２０は検出信号Ｃ１を”０”にする。これによって、実行回路３０のＣＰＵ３２に割込信号が与え

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られ、ＣＰＵ３２は第１種プログラムのリジューム処理を行うプログラム、放電停止処理を行うプログラム、アプリケーションプログラムを順にスケジューリングして実行する（時刻ｔ１０）。リジューム処理とは、サスペンド処理を行う直前の状態に戻す処理を意味し、リジューム処理が行われた状態をリジューム状態と称す。基本的には、入力部７１および出力部７２をサスペンド処理を行う直前の状態に戻す制御（個別ハード復帰制御）を行うが、ここでは、入力部７１および出力部７２は直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧Ｖｃが電圧ａ１、電圧ａ２、電圧ａ３になれば自然に元の状態に戻る。時刻ｔ１０後では、電源ライン９０の電圧Ｖ３は充分に電圧ａ１に近づき、充電電圧Ｖ２に頼らなくても、実行回路３０は正常に駆動できる状態にある。そこで、放電停止処理を行うプログラムが実行され、実行回路３０のＣＰＵ３２は割込信号を受けると直ぐに制御信号Ｃ２を”１”にする。出力回路４０は、”１”の制御信号Ｃ２を受けると制御信号Ｃ３を”０”に固定する。放電回路５０は、”０”の制御信号Ｃ３を受けると、充電電圧Ｖ２を電源ライン９０に放電するのを停止する。その後、アプリケーションプログラムが実行される。

【００４３】つまり、サスペンド処理を行うプログラムを実行することによって、入力部７１、出力部７２等を省電力モードで動作させ、充電回路６０の充電量の消費を抑え、実行回路３０をより長く駆動させ、再び、直流電圧Ｖ０が立ち上がるまで、実行回路３０を待機させることができる。これによって、第１種プログラムを実行することによって得られた処理結果Ｃ５を、サスペンド処理を行うプログラムによって実行回路３０を待機させて保護して消失することを防ぐことができる。

【００４４】以上のように、直流電圧Ｖｂが閾値電圧ｃより大きければ第１種プログラムを実行する。直流電圧Ｖｂが閾値電圧ｃ以下になると、第１種プログラムを実行することによって得られた処理結果を保護する第２種プログラムを実行するとともに、実行回路３０の電源端子には直流電圧Ｖａに加えて放電回路５０から放電された充電電圧Ｖ２が補われる。これによって、実行回路３０はより長く安定して駆動することができ、その間に、第１種プログラムを実行することによって得られた処理結果を第２種プログラムによって保護して消失することを防ぐことができる。

【００４５】また、直流電圧Ｖ０は遮断されたのではなく、直流電圧Ｖａが駆動最低電圧ｄより小さい僅かな電圧が図７の時刻ｔ７～時刻ｔ８で供給されている場合がある。この場合、充電回路６０の充電量が僅かであっても、直流電圧Ｖａと充電回路６０からの充電電圧Ｖ２との合計により、実行回路３０は長く安定して駆動できる。

【００４６】また、先に説明した放電回路５０の放電・放電停止の繰り返しによって、電圧Ｖ３が駆動最低電圧ｄに達する分だけの電力量が放電回路５０から少しずつ供給されるので、充電回路６０の充電量が僅かでも実行回路３０を長く安定して駆動させることができる。

【００４７】また、従来ではバックアップ電源の充電量が少なければ、それまでのプログラムの実行によって得られた処理結果が消失してしまうので、バックアップ電源として充電容量の少ないコンデンサ６３を適用できなかったが、本発明では充電量が僅かでも上述のように処理結果を保護して消失することを防ぐことができる。したがって、バックアップ電源としてコンデンサ６３を適用することができ、しかも、充電回路６０を寿命のないバックアップ電源として構成でき、充電池のように液漏れがなく、メンテナンスを行う必要がない。

【００４８】また、出力回路４０は、図2のような回路に代えて、制御信号Ｃ２が”１”になったとき制御信号Ｃ３を”０”に保持し、制御信号Ｃ２が”０”の状態で電圧Ｖ３が駆動最低電圧ｄ以下になったとき制御信号Ｃ３を”１”に保持するラッチ回路でもよい。ラッチ回路に代えると、図7の時刻ｔ７～時刻ｔ８は常に”１”である。このように、出力回路４０は、電源端子の電圧Ｖ３が実行回路３０が動作可能な予め設定された閾値電圧（以上の説明では駆動最低電圧ｄに等しい）になったときに”０”の制御信号Ｃ３を放電回路５０に出力する。これによって、電圧Ｖ３が駆動最低電圧ｄになるまでは実行回路３０は直流電圧Ｖａのみで駆動するので、その分、実行回路３０はさらに長く安定して駆動することができる。なお、予め設定された閾値電圧は、駆動最低電圧ｄより大きくてもよい。

【００４９】また、直流電圧Ｖ０を遮断した後、サスペンド状態で実行回路３０の状態を保持するので、ＯＳを再び起動する必要がなく、直流電圧Ｖ０が投入された直後にプログラムを直ちに立ち上げることができる。

【００５０】また、出力回路４０をラッチ回路に置き換えた場合、リセット回路８０からの信号をこのラッチ回路に入力して、操作者がリセット回路８０の押しボタンを押せば、制御信号Ｃ３を”０”にリセットする構成にしてもよい。

【００５１】また、出力回路４０を省略して、制御信号Ｃ２を放電回路５０に与えても良い。この場合、”０”の制御信号Ｃ２が放電信号、”１”の制御信号Ｃ２が放電停止信号であり、これに合わせて、放電回路５０は、“０”の制御信号Ｃ２を受けると充電電圧Ｖ２を電源ライン９０を介して実行回路３０の電源端子へ放電し、”１”の制御信号Ｃ２を受けると充電電圧Ｖ２を電源ライン９０に放電するのを停止する。

【００５２】また、放電回路５０は、制御信号Ｃ３の“０”から“１”への立ち上がりを受ければ充電電圧Ｖ２を電源ライン９０に放電し続け、制御信号Ｃ３の“１”から“０”への立ち下がりを受ければ放電を停止し続けるラッチ機能を有していてもよい。この場合、リ

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セット回路８０からの信号を放電回路５０に入力して、操作者がリセット回路８０の押しボタンを押せば、上記の放電を停止する構成にしてもよい。

【００５３】また、直流電圧Ｖａ、直流電圧Ｖｂ、直流電圧Ｖｃは同一の直流電源電圧であってもよい。

【００５４】また、充電回路６０のコンデンサ６３を充電池に代えてもよい。

【００５５】また、第２種プログラムは、上述のデータ書き込み処理を行うプログラムやサスペンド処理を行うプログラム以外の、処理結果を保護するプログラムを含んでいればよい。例えば、処理結果Ｃ５を出力部７２の一である液晶パネルに表示させるためのプログラムでもよい。あるいは、実行回路３０をリセットすることによって、リセット信号Ｃ６が入力された場合と同じ初期状態に戻すためのプログラムであってもよい。この場合、リセットすることによって、不安定な駆動による第２種プログラムの暴走を防ぎ、例えば、第１種プログラムによって出力部７２の一である不揮発性メモリに既に書き込まれた処理結果が破壊されることを防ぐことができる。

【００５６】また、制御信号Ｃ２の放電信号および放電停止信号は、上述の例では第１種プログラムや第２種プログラムに含まれる命令によってＣＰＵ３２が生成するが、これに代えて、実行回路３０は検出信号Ｃ１の”１”、”０”に応じて生成する別回路を含み、ＣＰＵ３２が第２種プログラムを実行するとともに当該別回路が放電信号および放電停止信号を生成してもよい。

【００５７】また、第１種プログラムは直流電圧Ｖ０が立ち上がった直後に不揮発性メモリに書き込まれた処理結果を実行回路３０の主メモリ３３に取り込むプログラムを含み、第２種プログラムは上述のデータ書き込み処理を行うプログラムを含んでいてもよい。これによれば、まず、図７の時刻ｔ４において直流電圧Ｖ０が遮断されると、上述のように、第２種プログラム内のデータ書き込み処理を行うプログラムが実行されることによって、第１種プログラムを実行することによって得られた処理結果Ｃ５が主メモリ３３から出力部７２の不揮発性メモリに書き込まれる。その後、再び直流電圧Ｖ０が立ち上がると、第１種プログラム内の上記の処理結果を取り込むプログラムが実行されることによって、処理結果Ｃ５が不揮発性メモリから主メモリ３３に書き込まれる。これによって、直流電圧Ｖ０が立ち上がる前に電圧Ｖ３が駆動最低電圧ｄを下回ったとしても、第１種プログラムに含まれるアプリケーションプログラムは、主メモリ３３に書き込まれた処理結果Ｃ５を初期値として、時刻ｔ４直前と同じ状態で立ち上がることができる。

【００５８】（実施の形態２）実施の形態１において、プログラムの実行中に直流電圧Ｖ０が遮断され、リジューム状態からサスペンド状態に入るとき、プログラムの実行が中断されたり、充電回路６０の充電量が少なかったり、その他の何らかの原因により、プログラムが正常に動作しない可能性がある。プログラムが正常に動作しない状態で、再び直流電圧Ｖ０が投入されてリジューム状態になると、プログラムが正常に動作しない状態が続くことになる。

【００５９】つまり、従来ではプログラムが正常に動作していなければ外部からの電源を遮断して、再び電源を投入すれば、プログラムが始めから起動されて正常に動作させることができる。しかし、実施の形態１で説明したサスペンド状態、レジューム状態が繰り返されれば、外部からの電源を遮断して再び投入しても、プログラムは正常に動作しないという問題点が生じる。

【００６０】そこで、上記問題点を解決するために、プログラムが正常に動作していなければ、サスペンド処理やリジューム処理を行うときに実行回路３０をリセットする（サスペンドリセット、リジュームリセット）。

【００６１】まず、サスペンドリセットを図９～図１２を用いて説明する。第１種プログラムの実行中に、誤動作が生じやすいところにフラグをオンする。誤動作が生じやすいところにフラグをオンする場合の例を、図９～図１１に列挙する。例えば、図９に示すように、ＣＰＵ３２はＯＳを起動した直後（ステップＳ１１）、フラグをオンし（ステップＳ１２）、アプリケーションプログラム等を実行する。そして、フラグをオンしてから所定時間経過後（ステップＳ１３）、フラグをオフする（ステップＳ１４）。あるいは、図１０に示すように、ＣＰＵ３２はアプリケーションプログラムのフラグオン命令を実行する（ステップＳ２１）。これによって、フラグをオンする（ステップＳ２２）。次に、ＣＰＵ３２はアプリケーションプログラムのフラグオフ命令を実行する（ステップＳ２３）。これによって、フラグをオフする（ステップＳ２４）。あるいは、図１１に示すように、ＣＰＵ３２はレジューム処理を開始してから（ステップＳ３１）、フラグをオンし（ステップＳ３２）、アプリケーションプログラム等を実行する。そして、フラグをオンしてから所定時間経過後（ステップＳ３３）、フラグをオフする（ステップＳ３４）。以上の図９～図１１に示したようなフラグを立てる処理は、第１種プログラムに含まれる。

【００６２】次に、サスペンド処理を行うときに、フラグがオンしていればリセットを行う。図１２を用いて詳しく説明すると、ＣＰＵ３２は、サスペンド処理を開始すると（ステップＳ４１）、フラグがオフしているかどうかを判断する（ステップＳ４２）。フラグがオフしていれば、ＣＰＵ３２はサスペンド処理を続行する（ステップＳ４３）。一方、フラグがオンしていればプログラムが正常に動作しない可能性が充分に考えられるので、ＣＰＵ３２は実行回路３０をリセットする（ステップＳ４４）。以上の図１２に示したような処理は第２種プログラムに含まれる。

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【００６３】以上、図９～図１２で説明したように、ＣＰＵ３２はサスペンド処理を行うとき（つまり、オン信号からオフ信号を受けるとき）、フラグがオフしていなければ（つまり、第１種プログラムの処理結果が所定条件を満たしていなければ）、実行回路３０をリセットする。これによって、再びリジューム状態になったときに、プログラムが正常に動作していない状態から自動的に回避することができ、操作者がサスペンド状態にすることができるかどうかを確認しなくて済む。

【００６４】次に、リジュームリセットを図１３を用いて説明する。まず、リジューム処理を開始したとき（ステップＳ５１）、ＯＳのシェルのユーザーへのメッセージ等の表示処理が行われる。この表示処理が正しく実行されているかどうかを判断する（ステップＳ５２）。判断方法は、例えば、不揮発性メモリにファイル形式でシェルの起動条件を予め格納しておき、この起動条件とシェルの表示処理の結果とを比較することで判断できる。このような判断方法によって、シェルが正常に実行されていなければ実行回路３０をリセットし（ステップＳ５６）、そうでなければステップＳ５３に進む。

【００６５】ステップＳ５３では、アプリケーションの起動数が前回のリジューム状態の起動数に等しいかどうかを確認する。確認方法は、例えば、サスペンド処理によってアプリケーションプログラムの起動数を調べて起動条件として主メモリ３３に格納しておく。そして、リジューム処理の開始後、アプリケーションプログラムの起動数と主メモリ３３に格納されている起動数とを比較することで確認できる。このような確認方法によって、アプリケーションの起動数が前回のリジューム状態と異なれば、実行回路３０をリセットし（ステップＳ５６）、そうでなければステップＳ５４に進む。

【００６６】ステップＳ５４では、アプリケーションプログラムが正しく実行されているかどうかを判断する。判断方法はステップＳ５２同様、例えば、不揮発性メモリにファイル形式でアプリケーションプログラムの起動条件を予め格納しておき、この起動条件とアプリケーションプログラムの実行結果とを比較することで判断できる。このような判断方法によって、アプリケーションプログラムが正常に実行されていなければ実行回路３０をリセットし（ステップＳ５６）、そうでなければリジューム処理を続行する（ステップＳ５５）。

【００６７】なお、ステップＳ５２～ステップＳ５４は、選択的に実行できるように構成してもよい。

【００６８】以上、図１３で説明したように、ＣＰＵ３２はサスペンド処理を行うとき（つまり、オフ信号からオン信号を受けるとき）、ＯＳのシェルやアプリケーションプログラムの処理結果が不揮発性メモリや主メモリ３３に格納されている所定条件を満たしていなければ、実行回路３０をリセットする。これによって、再びリジューム状態になったときに、プログラムが正常に動作していない状態から自動的に回避することができ、操作者がプログラムの立上げを行う必要がない。

【００６９】また、サスペンドリセットやリジュームリセットを行うことによって、実施の形態１同様、不安定な駆動による第２種プログラムの暴走を防いで、第１種プログラムを実行することによって得られた処理結果を保護することができる。

【００７０】（本発明の適用例）本発明のプログラム実行装置は、プログラムを実行する装置であればよく、例えば、ファクトリーオートメーション（ＦＡ）の生産ラインを構成する機械を制御する制御機器、パーソナルコンピュータなどに適用してもよい。あるいは、図１の構成要素のうち、少なくとも検出回路２０、実行回路３０、充電回路６０、放電回路５０を１チップ上に形成して、ＤＳＰ（Digital Signal Processor）と称されるような１チップマイクロコンピュータなどに適用してもよい。特に、図７の直流電圧Ｖ０が遮断されてから（時刻ｔ４）、電圧Ｖ３が駆動最低電圧ｄを下回るまで（時刻ｔ８）の間に、再び、直流電圧Ｖ０が立ち上がることが頻繁に起こるシステムに適用すれば、直流電圧Ｖ０が投入された直後にプログラムを直ちに立ち上げることができるので効果的である。

【００７１】

【発明の効果】請求項１に記載の発明によれば、直流電圧が第１閾値電圧より大きければ第１種プログラムを実行する。直流電圧が第１閾値電圧以下になると、第１種プログラムで得られた処理結果を保護するための第２種プログラムを実行するとともに、電源端子には直流電圧に加えて放電回路から放電された充電電圧が補われる。これによって、実行回路はより長く安定して駆動することができ、その間に、第１種プログラムを実行することによって得られた処理結果を第２種プログラムによって保護して消失することを防ぐことができる。

【００７２】請求項２に記載の発明によれば、実行回路は、電源端子の電圧が第２閾値電圧になるまでは直流電源電圧で駆動する。これによって、実行回路はさらに長く安定して駆動することができる。

【００７３】請求項３に記載の発明によれば、第２種プログラムで実行回路をリセットすることで、第２種プログラムの暴走を防ぐことによって、第１種プログラムで得られた処理結果を保護することができる。

【００７４】請求項４に記載の発明によれば、第１種および第２種プログラムが正常に動作していない状態から回避することができる。

【００７５】請求項５に記載の発明によれば、第１種プログラムに代えて所望の処理結果を得るための第２種プログラムを実行するので、充電回路の充電容量が僅かでも所望の処理結果を得ることができる。よって、充電回路を充電容量の小さいコンデンサを用いて構成しても充分な効果を得ることができ、しかも、充電回路を寿命の

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ないバックアップ電源として構成できる。

【００７６】請求項６に記載の発明によれば、コンデンサをバックアップ電源として用いることができるので、バックアップ機能付きの１チップで構成されたプログラム実行装置を得ることができる。

【図面の簡単な説明】

【図１】　本発明の実施の形態１のプログラム実行装置を示すブロック図である。

【図２】　本発明の実施の形態１の検出回路を示す回路図である。

【図３】　本発明の実施の形態１の実行回路を示すブロック図である。

【図４】　本発明の実施の形態１の実行回路の動作を示すタイミングチャートである。

【図５】　本発明の実施の形態１の実行回路の動作を示すタイミングチャートである。

【図６】　本発明の実施の形態１の充電回路を示すブロック図である。

【図７】　本発明の実施の形態１のプログラム実行装置の動作を示すタイミングチャートである。

【図８】　本発明の実施の形態１のプログラム実行装置の動作を示すタイミングチャートである。

【図９】　本発明の実施の形態２のプログラム実行装置の動作を示すフローチャートである。

【図１０】　本発明の実施の形態２のプログラム実行装置の動作を示すフローチャートである。

【図１１】　本発明の実施の形態２のプログラム実行装置の動作を示すフローチャートである。

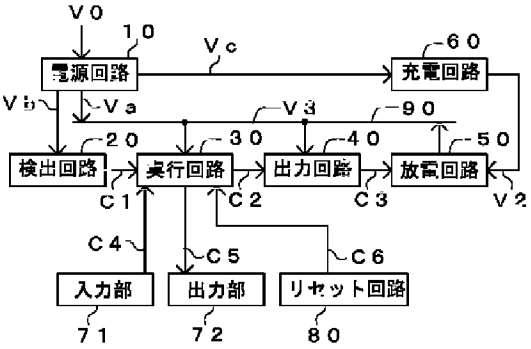
【図１２】　本発明の実施の形態２のプログラム実行装置の動作を示すフローチャートである。

【図１３】　本発明の実施の形態２のプログラム実行装置の動作を示すフローチャートである。

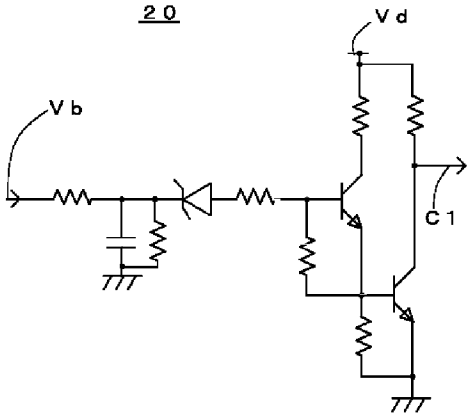
【符号の説明】

１０　電源回路、２０　検出回路、３０　実行回路、４０　出力回路、５０放電回路、６０　充電回路。

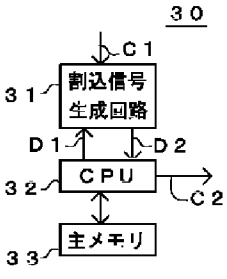
【図１】



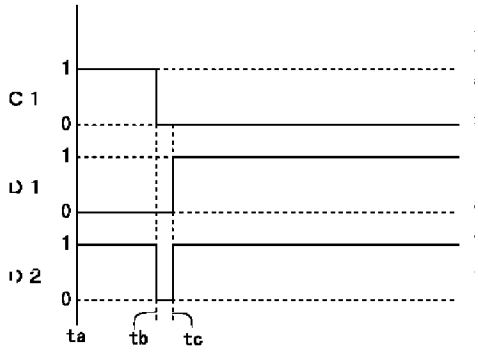
【図２】



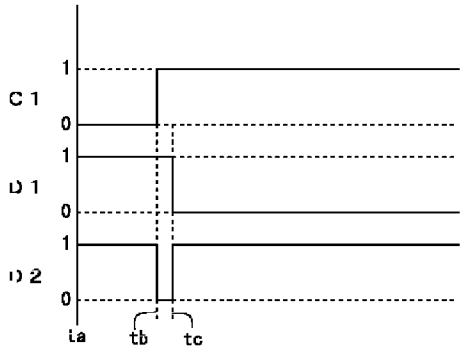
【図３】



【図４】

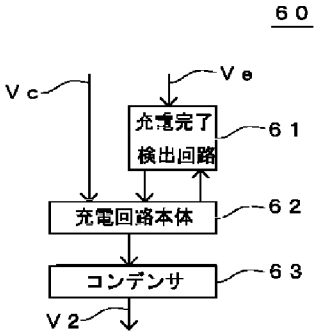


【図５】

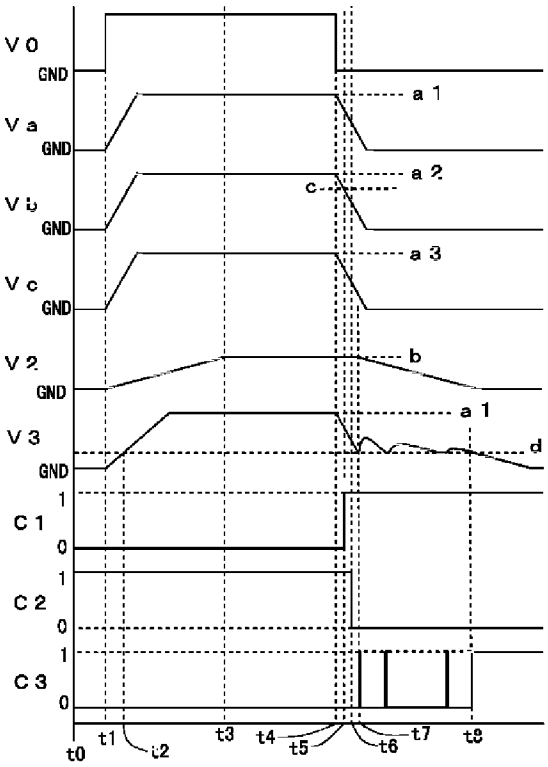


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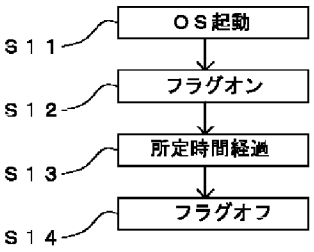
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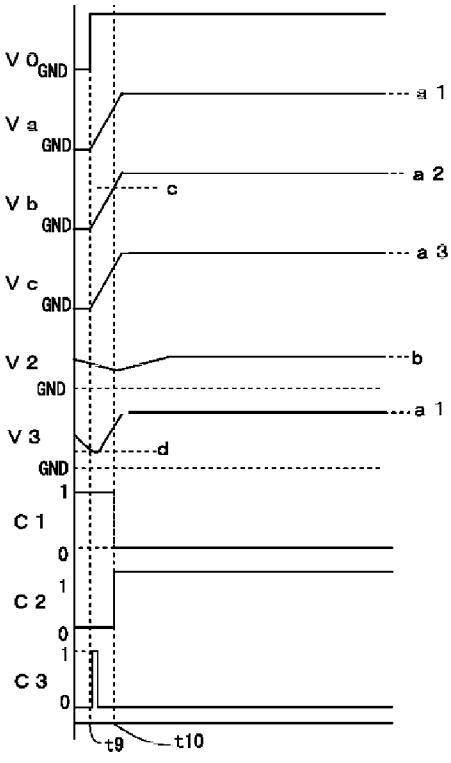
【図7】



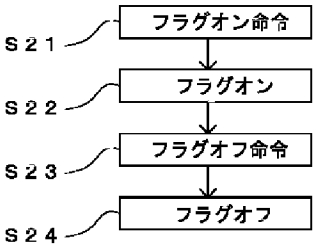
【図9】



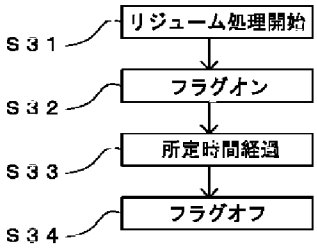
【図8】



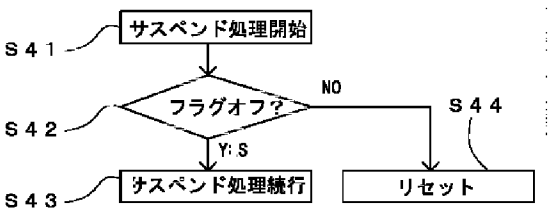
【図10】



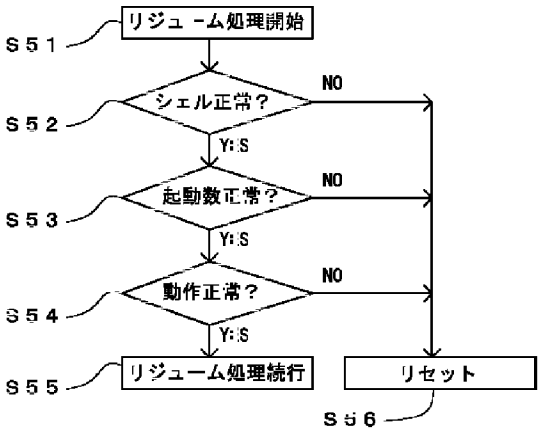
【図11】



【図12】



【図１３】



フロントページの続き

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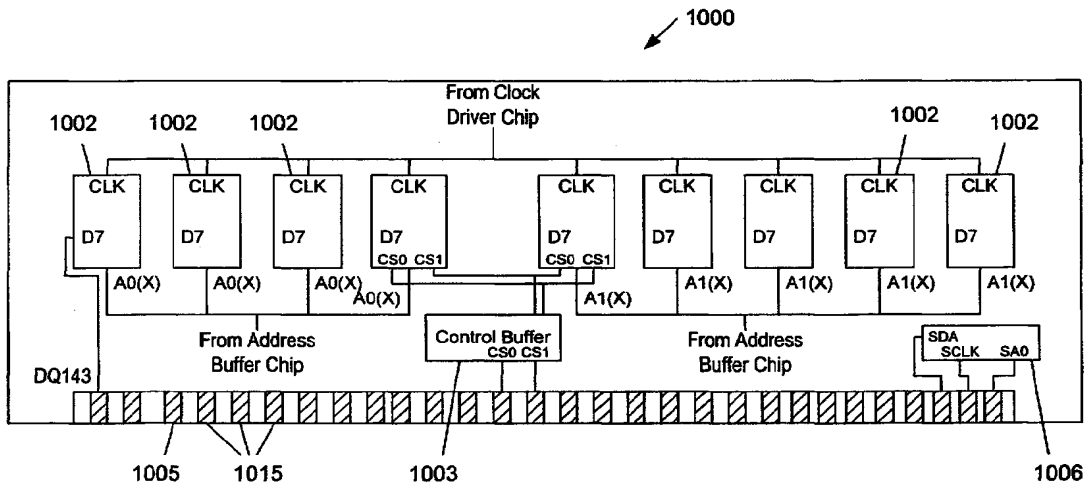
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[Continued on next page]

(54) Title: A MEMORY EXPANSION MODULE WITH STACKED MEMORY PACKAGES



(57) Abstract: A memory expansion module with stacked memory packages. A memory module is implemented using stacked memory packages. Each of the stacked memory packages contains multiple memory chips, typically DRAMs (dynamic random access memory). The memory may be organized into multiple banks, wherein a given memory chip within a stacked memory package is part of one bank, while another memory chip in the same package is part of another bank. The memory module also includes a clock driver chip and a storage unit. The storage unit is configured to store module identification information, such as a serial number. The storage unit is also configured to store information correlating electrical contact pads on the module with individual signal pins on the stacked memory packages. This may allow an error to be quickly traced to a specific pin on a stacked memory package when an error is detected on the memory bus by an error correction subsystem.

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TITLE: A MEMORY EXPANSION MODULE WITH STACKED MEMORY PACKAGES

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention generally relates to memory hardware for computer systems, and more specifically to memory expansion modules for expanding memory in computer systems.

2. Description of the Related Art

Many modern computer systems allow for memory expansion by way of single inline memory modules (SIMMs) and/or dual inline memory modules (DIMMs). SIMMs and DIMMs include small, compact circuit boards that are designed to mount easily into an expansion socket mounted on another circuit board, typically a computer motherboard. The circuit boards used to implement SIMMs and DIMMs include an edge connector comprising a plurality of contact pads, with contact pads typically being present on both sides of the circuit board. On SIMMs, opposing contact pads are connected together (i.e. shorted), and thus carry the same signal, while at least some opposing contact pads on DIMMs are not connected, thus allowing different signals to be carried. Due to this, higher signal density may be accommodated by DIMMs.

Memory elements of SIMMs and DIMMs are typically Dynamic Random Access Memory (DRAM) chips. DRAM chips store information as a charge on a capacitor, with the charge level representing a logic one or logic zero. Since a capacitor charge will dissipate over time, DRAM chips require refresh cycles on a periodic basis.

To access a location in a DRAM, an address must first be applied to the address inputs. This address is then decoded, and data from the given address is accessed. In modern DRAMs, rows and columns are addressed separately using row address strobe (RAS) and column address strobe (CAS) control signals. By using RAS and CAS signals, row and column addresses can be time-multiplexed on common signal lines, contact pads, and pins of the address bus. This allows a greater number of memory locations that can be addressed without a corresponding increase in the number of required signal lines, contact pads, and pins.

To address a memory location in a DRAM as described above, a RAS signal is asserted on the RAS input of the DRAM, and a row address is forwarded to row decode logic on a memory chip. The contents of all locations in the addressed row will then be sent to a column decoder, which is typically a combination multiplexer/demultiplexer. After row addressing is complete, a CAS signal is asserted, and a column address is sent to the column decoder. The multiplexer in the column decoder will then select the corresponding column from the addressed row, and the data from that specific row/column address is placed on the data bus for used by the computer system.

The demand for more memory in computer systems is ever increasing. Advances in software has further driven the demand for greater memory capacity, as complex programs require more memory space with which to operate. Along with the demand for greater memory capacity is the need for greater reliability in computer system operation. As the capacity of memory modules increases so to does the possibility of an error or a failure. Tracking errors to their source on a memory module may sometimes be a difficult and time-consuming process.

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Tracing a signal from a contact on an edge connector to a specific pin on a memory device may be time consuming even when accurate schematics are available. Furthermore, manually tracing a signal from an edge connector contact to a pin on a memory device may be prone to human error.

SUMMARY OF THE INVENTION

The problems outlined above may in large part be solved by a memory expansion module in accordance with the present invention. In one embodiment, a memory module includes a printed circuit board with a connector edge adapted for insertion in an expansion socket of a computer system. Mounted upon the circuit board is a plurality of stacked memory packages. Each stacked memory chip package contains multiple memory chips, or die, within the package. These memory chips are typically Dynamic Random Access Memory (DRAM). In one embodiment, each stacked memory package includes two DRAM die. The printed circuit board of this embodiment includes 18 locations for mounting the stacked memory packages, resulting in a memory module with a total of 36 memory die. Also mounted upon the printed circuit board is at least one buffer (or line driver) chip for driving address and control signals to the plurality of memory die contained within the stacked memory packages. A clock driver chip is also mounted upon the printed circuit board for driving clock signals to the memory chips. Also mounted on the printed circuit board is a storage unit, which provides module identification and signal routing information. In one embodiment, a serial electrically erasable programmable read-only memory (SEEPROM) is used to implement the storage unit. Information which correlates individual contact pads of the edge connector to individual pins of the stacked memory packages may be stored in the storage unit. Using this information, an error detected by in the memory module may be quickly traced to a specific pin of a stacked memory package.

Each memory die within each stacked memory package may be individually accessed by a computer system. Since the memory die within the stacked memory packages may be accessed individually, multiple memory banks may be formed with each die within a given package belonging to a different memory bank. In one embodiment, each memory die is a 32M x 8, resulting in a stacked memory package with a capacity of 64M x 8. The total module capacity in this embodiment is 1 gigabyte. In general, the memory module is scalable and may be implemented with various amounts of memory capacity.

Thus, in various embodiments, the memory expansion module with stacked memory packages and error correction functionality may advantageously allow greater memory capacity. The use of stacked memory packages may allow for greater memory capacity without the need for additional circuit board area. The use of stacked memory packages with no more than two memory die each may advantageously reduce power consumption and thermal output by the memory module.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Figure 1 is a block diagram illustrating an embodiment of a computer system having a CPU, a memory controller, a CPU bus, and a plurality of memory modules;

Figure 2 is a mechanical drawing of one embodiment of a memory module;

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Figure 3A is a block diagram illustrating the electrical connections associated with the top side of an embodiment of the memory module;

Figure 3B is a block diagram illustrating the electrical connections associated with the bottom side of an embodiment of the memory module;

Figure 4 is a functional block diagram of one embodiment of the memory module;

Figure 5 is a pin diagram of one embodiment of a stacked memory package;

Figure 6 is a block diagram of the internal organization of one embodiment of a stacked memory package;

Figure 7 is a drawing of one embodiment the memory module illustrating the electrical interconnections associated with error correction functions; and,

Figure 8 is a table illustrating exemplary entries within the storage unit correlating connector pins to integrated circuit pins.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and description thereto are not intended to limit the invention to the particular form disclosed, but, on the contrary, the invention is to cover all modifications, equivalents, and alternatives falling with the spirit and scope of the present invention as defined be the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to Figure 1, an embodiment of a computer system 100 including a plurality of memory modules 1000, as will be described below, is shown. The computer system includes a CPU 101, coupled to a memory controller 102 through a CPU bus 103. Memory controller 102 is configured to control communications and data transfers between CPU 101 and memory modules 1000.

Memory controller 102 is coupled to each of the memory modules 1000 through a memory bus 104. Memory bus 104 includes a plurality of signal lines, each of which is associated with a single data bit position. The width of memory bus 104 may be any number of bits; typical bus widths include 16 bits, 32 bits, 64 bits, and 128 bits. Some embodiments of memory bus 104 may include extra signal lines for bits that may be used by error correction circuitry. The bits conveyed by the extra signal lines are typically referred to as check bits. For example, one embodiment of a memory bus may be configured to convey 128 data bits and 16 check bits, for a total bus width of 144 bits. Error detection and correction is performed by error correction subsystem 106, located within memory controller 102.

In the embodiment shown, the memory modules are provided to expand main memory of computer system 100, and are electrically coupled to memory bus 104 through a set of expansion sockets 105. An expansion socket 105 of the embodiment shown is configured to receive an edge connector of a printed circuit board of a memory module 1000.

Moving on to Figure 2, a mechanical drawing of one embodiment of the memory module is shown. Memory module 1000 includes a plurality of stacked memory packages 1002 mounted upon both sides of a printed circuit board 500. Memory module 1000 also includes two line driver chips 1003, one mounted on each side of the printed circuit board. In this embodiment, clock driver chip 1004 is mounted on the top side of printed circuit board 500, while a storage unit 1006 is mounted on the bottom side. Edge connector 1005 provides electrical

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contact between the various components of the module and the computer system 100 of Figure 1. In the embodiment shown, edge connector 1005 includes 232 electrical contacts. Furthermore, a majority of opposing electrical contacts of edge connector 1005 are not electrically connected, making this module a DIMM (dual inline memory module).

Figures 3A and 3B are block diagrams illustrating the electrical connections associated with the top and bottom side, respectively, of one embodiment of the memory module. Memory module 1000 includes a plurality of stacked memory packages 1002 mounted upon each side. Memory module 1000 also includes edge connector 1005 for electrically coupling memory module 1000 to the memory bus 104 of Figure 1. Edge connector 1005 includes a plurality of electrical contacts 1015 for conveying electrical signals between memory module 1000 and the memory bus. As in Figure 2, a majority of opposing contacts in the embodiment shown are not electrically connected, making the module a DIMM.

On each side of memory module 1000 is mounted a line driver (or buffer) chip 1003. Line driver chip 1003-A in Figure 3A serves as an address buffer (for address signals), while line driver chip 1003-B in Figure 3B serves as a control buffer (for control signals). Line driver chip 1003-A is configured to receive address signals from a memory bus of a computer system, via electrical contact pads 1015 and interconnecting signal lines. In the embodiment shown, each address signal is split into two separate signals. Those address signals labeled A0(X) are driven to a first memory bank, while those labeled A1(X) are driven to a second memory bank. Line driver chip 1003-B is configured to receive various control signals from a memory bus. These control signals include chip select signals; CS0 and CS1 as shown. Other control signals (not shown) include row address strobe (RAS), column address strobe (CAS), clock enable (CKE), and write enable (WE).

The top side of the module also includes clock driver chip 1004. Clock driver chip 1004 is configured to receive clock signals from a computer system, and to drive these signals to the memory chips of the stacked memory packages 1002. In the embodiment shown, clock driver chip 1004 actually receives two differential PECL (pseudo emitter coupled logic) level signals, designated here as CLK+ and CLK-. These differential signals are used as inputs to a phase-locked loop (PLL) circuit within the clock driver chip. The output of the PLL is a singular clock signal, which is driven to each of the memory chips within the stacked memory packages 1002. Other embodiments configured to receive a singular clock signal (rather than multiple differential clock signals) are possible and contemplated.

A storage unit 1006 is mounted upon the bottom side of the module. In the embodiment shown, storage unit 1006 is a serial EEPROM (electrically erasable read-only memory). Other embodiments may use a flash memory or other type of device to implement storage unit 1006. In the embodiment shown, storage unit 1006 performs two functions. The first of these functions is module identification, as storage unit 1006 may, in one embodiment, be configured to store a unique serial number for memory module 1000. This serial number may be read by a computer system into which the memory module is inserted. Using the unique serial number, the module history may be traced from its time of manufacture, including any failure information.

The second function of storage unit 1006 is the storage of error correction information. In particular, the storage unit 1006 of the embodiment shown is configured to store information correlating pins of the connector edge to individual pins of stacked memory packages 1002. Using this information, an error detected by an error correction subsystem may be quickly traced to a specific pin of a specific stacked memory package 1002.

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Turning now to Figure 4, a functional block diagram of one embodiment of the memory module is shown. Memory module 1000 includes a plurality of memory die1002U and 1002L, wherein each pair of die is part of a stacked memory package 1002 of Figures 2 and 3. Typically, memory die 1002U and 1002L will be dynamic random access memory (DRAM) chips. In the embodiment shown, a first bank and a second bank of memory are present. The first bank of memory includes the shown plurality of memory die 1002U, while the second bank includes the shown plurality of memory chips 1002L. Each memory die has a data width of 8 bits, and is coupled to a data bus of 144 bits.

Two buffers, or line driver chips 1003 are used to drive address and control signals to the memory die 1002U and 1002L. One line driver chip 1003 is used exclusively for address signals. Each address signal received by the line driver chip 1003 is duplicated twice and driven to a stacked memory package 1002. A second line driver chip 1003 is used to drive control signals to the memory die 1002U and 1002L within each stacked memory package in order to control the individual banks of memory. Each stacked memory package 1002 is configured to receive a RAS signal (RAS0 or RAS1), a CAS signal (CAS0 or CAS1), and a WE signal (WE0 or WE1). In addition, each stacked memory package 1002 is configured to receive control signals CS0, CS1, CKE0, and CKE1.

Also shown in Figure 4 is clock driver chip 1004, which is configured to receive two differential PECL clock signals, and drive a singular clock signal to each of the memory chips, as explained above with reference to Figure 3A.

Figure 5 is a pin diagram of one embodiment of a stacked memory package 1002. In the embodiment shown, stacked memory package 1002 includes two memory die. Each stacked memory package is configured to receive 8 data signals (DQ0-DQ7), 15 address signals (A0-A12 and BA0-BA1), and control signals CS0, CS1, CKE0, CKE1, RAS, CAS, and WE. Address signals BA0 and BA1 correspond to address signals A13 and A14 as shown in Figure 4. In general, a limitation of two memory die per stacked memory package is placed upon the various embodiments of the memory module, due to considerations for power consumption and thermal output of the module. Stacked packages with only two memory die may consume less power and generate less heat than those containing three or more memory die, while still allowing additional memory capacity without the need for additional circuit area relative to memory packages having a single memory die.

Figure 6 is a block diagram of the internal organization of one embodiment of a stacked memory package. The embodiment shown consists of memory die 1002U and 1002L. Address signals A0-A14 are coupled to both memory die, as are control signals CAS, RAS, and WE, and data signals DQ0 – DQ7. A clock signal, CLK, is also coupled to both memory die. Control signals CKE0 and CS0 are coupled to memory die 1002U, and are asserted during read and write operations to this memory die. Likewise, control signals CKE1 and CS1 are coupled to memory die 1002L. Memory die 1002U and 1002L are part of a first and a second memory bank, respectively. The memory die in this embodiment are 32M x 8 (i.e. 32 megabytes) each, resulting in a stacked memory package with a capacity of 64 megabytes. Using a total of 18 stacked memory packages of this capacity results in a module capacity of one gigabyte.

Figure 7 is a drawing of one embodiment the memory module illustrating the electrical interconnections associated with error correction functions. Memory module 1000 includes a printed circuit board upon which stacked memory packages 1002 are mounted. Each of these packages has a data width of 8 bits, and includes two memory chips (1002U and 1002L from Figures 4 and 6). Depending on the organization of memory module 1000,

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some of these memory die may be used to store error correction check bits, while others may be used to store data bits. Memory module 1000 also includes an edge connector 1005, with a plurality of electrical contact pads 1015. A plurality of signal lines 1020 couples the electrical contact pads 1015 to the stacked memory packages 1002. Data signals are conveyed along signal lines 1020 between the stacked memory packages 1002 and electrical contact pads 1015. Data pin D0 of each stacked memory package 1002 is shown coupled to electrical contact pads 1015 by signal lines 1020, with the respective position of the bit in the data word (i.e. DQ0, DQ16, etc.) shown. The most significant bit of the data, DQ143, is coupled to pin D7 of a stacked memory package 1002. In this embodiment, 16 check bits are used to protect each data block of 128 bits, with each check word associated with one data block only.

As previously stated, some memory die of the stacked memory packages 1002 may be used exclusively to store check bits in this embodiment. Each of these memory die may store four check bits of each check word. In the embodiment shown, each check word is 16 bits, and protects a data block of 128 bits. These check bits are accessed through a plurality of pins designated CBWX[y:z]. For example, CBW1[3:0] shown in the drawing represents four pins of a stacked memory package 1002 through which check bits 0 through 3 of check word #1 are accessed. Similarly, CBW2[7:4] represents those pins through which check bits 4 through 7 of check word #2 are accessed. Each of these pins is connected to a respective signal line. Representative signal lines are shown in the drawing as CBW1 through CBW4. In general, these signal lines are routed on the printed circuit board in such a manner that physically adjacent memory cells within each memory die store check bits corresponding to different check words.

Figure 8 is a table illustrating exemplary entries within the storage unit correlating connector pins to integrated circuit pins. In the table shown, each connector pad of an edge connector (such as edge connector 1005 of Figures 3A and 3B) is associated with a pin of an integrated circuit package (such as the stacked memory packages 1002 of Figures 3A and 3B). For example, connector pad #1 is associated with integrated circuit U1, pin 5 (U1.5). Similarly, connector pad #5 is associated with integrated circuit U1, pin 9. Most if not all connector pads may be associated with at least one pin of one integrated circuit. In many cases, certain connector pads may be associated with a plurality of integrated circuit pins. Such connector pads may include those that carry address signals and enable signals (e.g. chip enable and write enable signals).

While the present invention has been described with reference to particular embodiments, it will be understood that the embodiments are illustrative and that the invention scope is not so limited. Any variations, modifications, additions, and improvements to the embodiments described are possible. These variations, modifications, additions, and improvements may fall within the scope of the inventions as detailed within the following claims.

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WHAT IS CLAIMED IS:

1. A memory module comprising:
a printed circuit board including a connector edge adapted for insertion within a socket of a computer system;
a plurality of stacked memory packages mounted upon said printed circuit board, each of said stacked memory packages including a first memory die and a second memory die, and wherein said first memory die of each of said stacked memory packages forms a portion of a first bank of memory and said second memory die of each of said stacked memory packages forms a portion of a second bank of memory;
a clock driver chip;
a storage unit for providing module identification and error correction check bit information; and,
at least one line driver chip configured to drive control signals and/or address signals.

2. The memory module as recited in claim 1, wherein said edge connector includes a plurality of electrical contact pads for conveying electrical signals.

3. The memory module as recited in claim 2, wherein said edge connector has 232 of said electrical contact pads.

4. The memory module as recited in claim 2, wherein said connector edge includes contact pads for receiving control signals, said control signals comprising at least one row address strobe (RAS) signal, at least one column address strobe (CAS) signal, at least one write enable (WE) signal, at least one clock enable (CKE) signal, and a least one chip select (CS) signal.

5. The memory module as recited in claim 2, wherein said electrical signals include a plurality of address signals, and wherein said plurality of address signals form an address bus.

6. The memory module as recited in claim 5, wherein said address bus is 14 bits wide.

7. The memory module as recited in claim 2, wherein said electrical signals include a plurality of data signals, and wherein said plurality of data signals form a data path.

8. The memory module as recited in claim 6, wherein said data path is 144 bits wide.

9. The memory module as recited in claim 1, wherein said memory module is configured for use in a system having an error correction subsystem, said error correction subsystem configured to generate a plurality of check words corresponding to a plurality of data blocks.

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10. The memory module as recited in claim 2, wherein said storage unit is configured to store signal line routing information which correlates each of said contact pads of said edge connector to a pin of a said stacked memory package.

11. The memory module as recited in claim 1, wherein said storage unit is configured to store module identification information.

12. The memory module as recited in claim 11, wherein said storage unit is a serial electrically erasable programmable read-only memory (SEEPROM).

13. The memory module as recited in claim 1, wherein said first memory die and said second memory die are dynamic random access memory (DRAM) chips.

14. The memory module as recited in claim 1, wherein said memory module is a dual-inline memory module (DIMM).

15. The memory module as recited in claim 1, wherein said memory module has a memory capacity of one gigabyte.

16. The memory module as recited in claim 1, wherein each of said stacked memory packages includes two memory die.

17. A memory module comprising:
a printed circuit board including a plurality of signal lines for conveying electrical signals and a connector edge adapted for insertion within a socket of a computer system, said edge connector having a plurality of contact pads for conveying said electrical signals between said memory module and a memory bus;
a plurality of stacked memory packages, each having two memory die, mounted upon said printed circuit board, each of said stacked memory packages having a plurality of signal pins;
a clock driver chip;
a storage unit for storing module identification and information which correlates said electrical contact pads to said signal pins; and,
at least one line driver chip for driving electrical signals to said stacked memory packages.

18. The memory module as recited in claim 17, wherein said electrical signals include a plurality of control signals, a plurality of data signals, and a plurality of address signals.

19. The memory module as recited in claim 18, wherein said plurality of data signals form a data path, said data path 144 bits wide.

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20. The memory module as recited in claim 18, wherein said plurality of address signals form an address bus, said address bus 14 bits wide.

21. The memory module as recited in claim 18, wherein said control signals include two column address strobe (CAS) signals, two row address strobe (RAS) signals, two write enable (WE) signals, two chip select (CS) signals, and two clock enable (CKE) signals.

22. The memory module as recited in claim 17, wherein said memory module is a Dual Inline Memory Module (DIMM).

23. The memory module as recited in claim 17, wherein said memory die are synchronous dynamic random access memory (SDRAM) chips.

24. The memory module as recited in claim 17m wherein said memory module has 232 of said contact pads.

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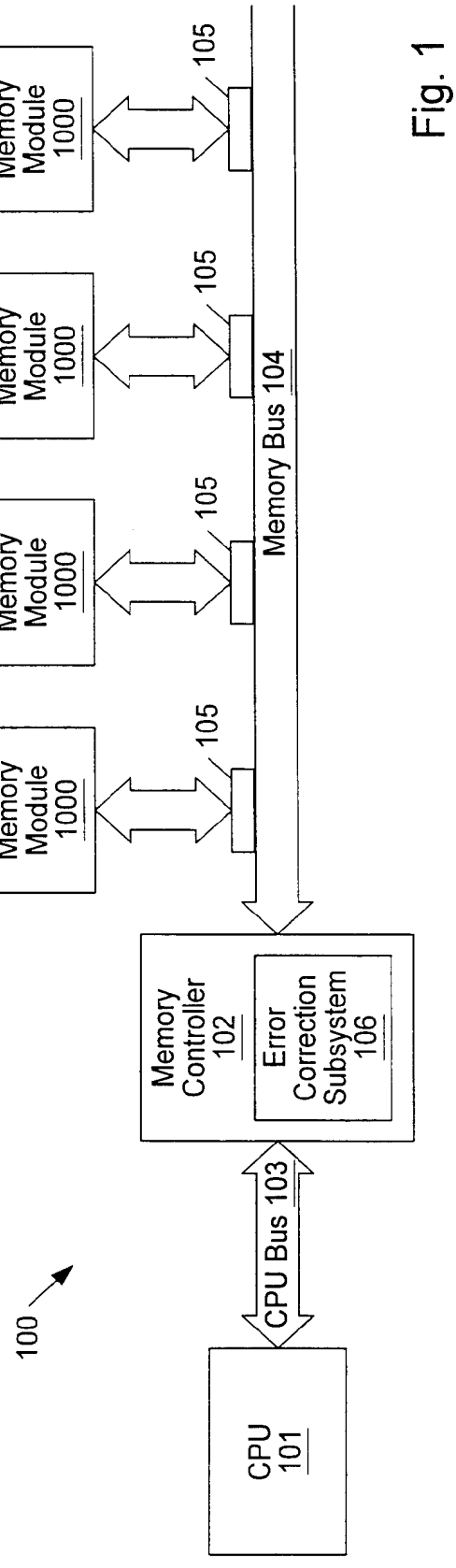


Fig. 1

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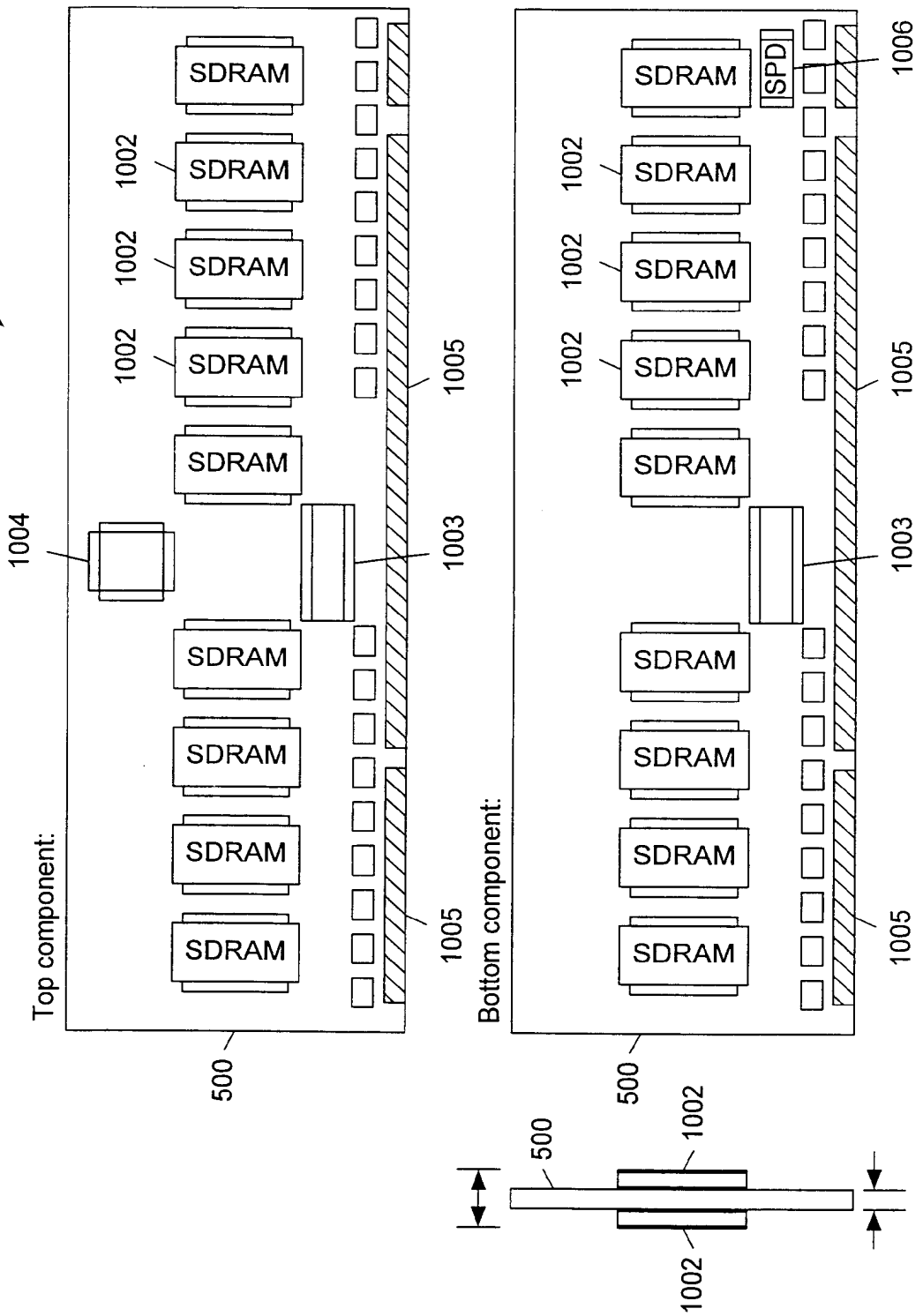


Fig. 2

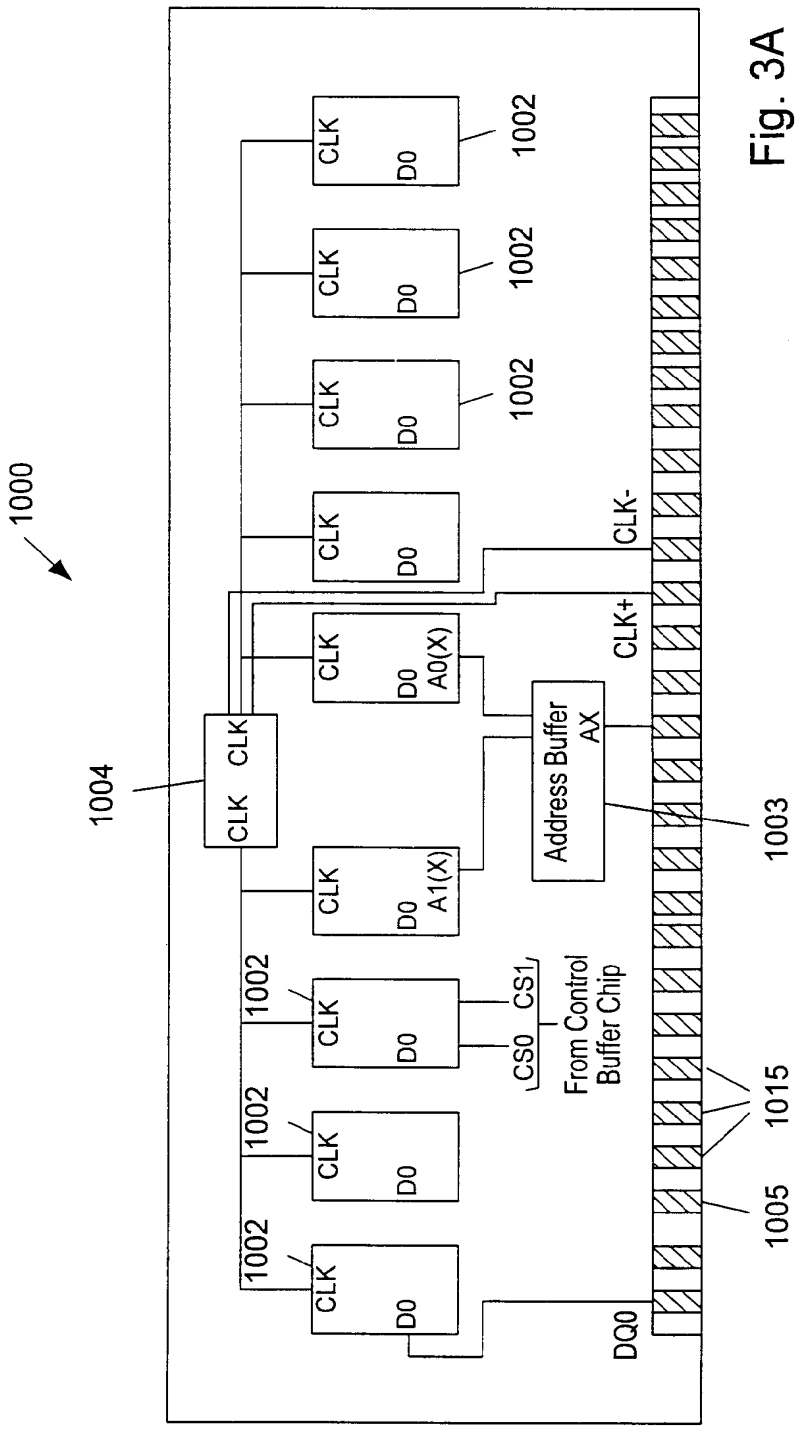


Fig. 3A

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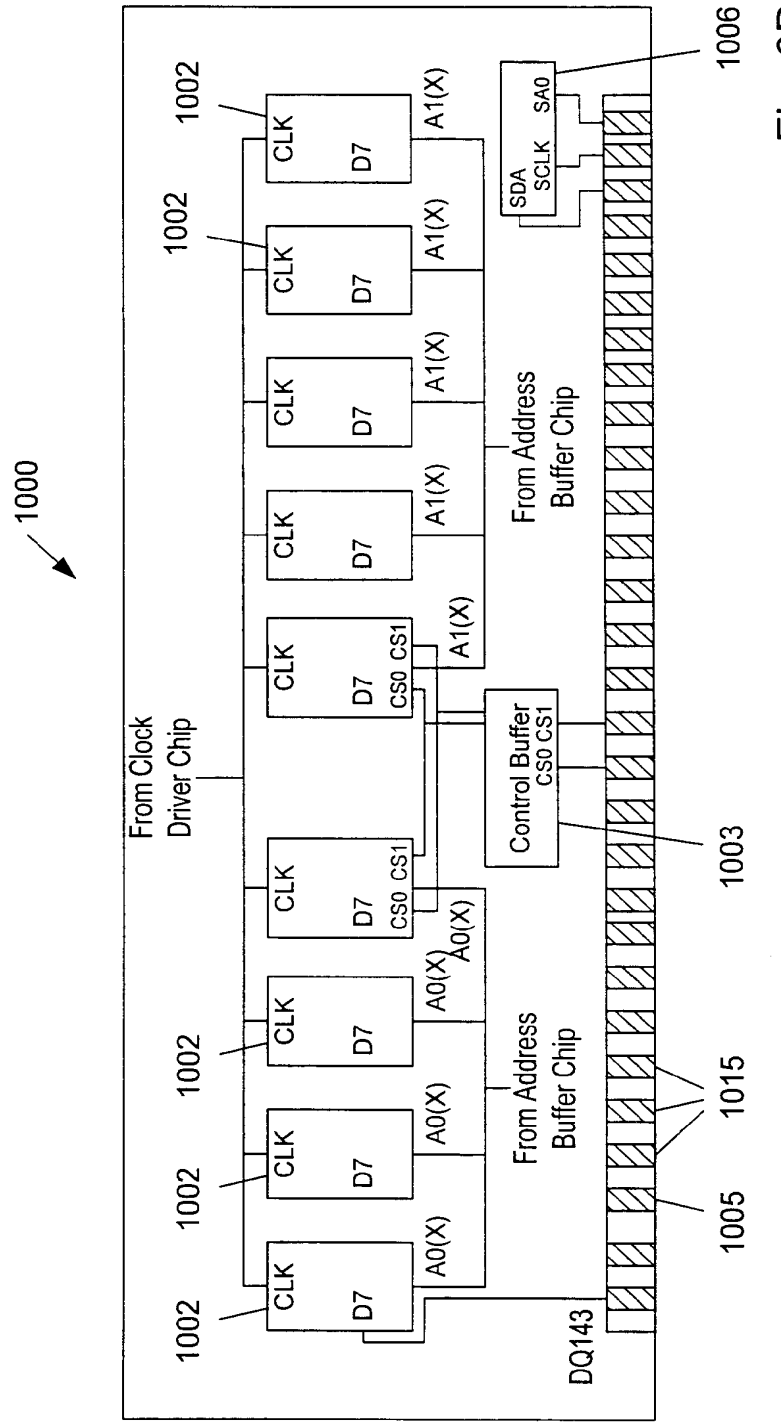


Fig. 3B

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SUBSTITUTE SHEET (RULE 26)

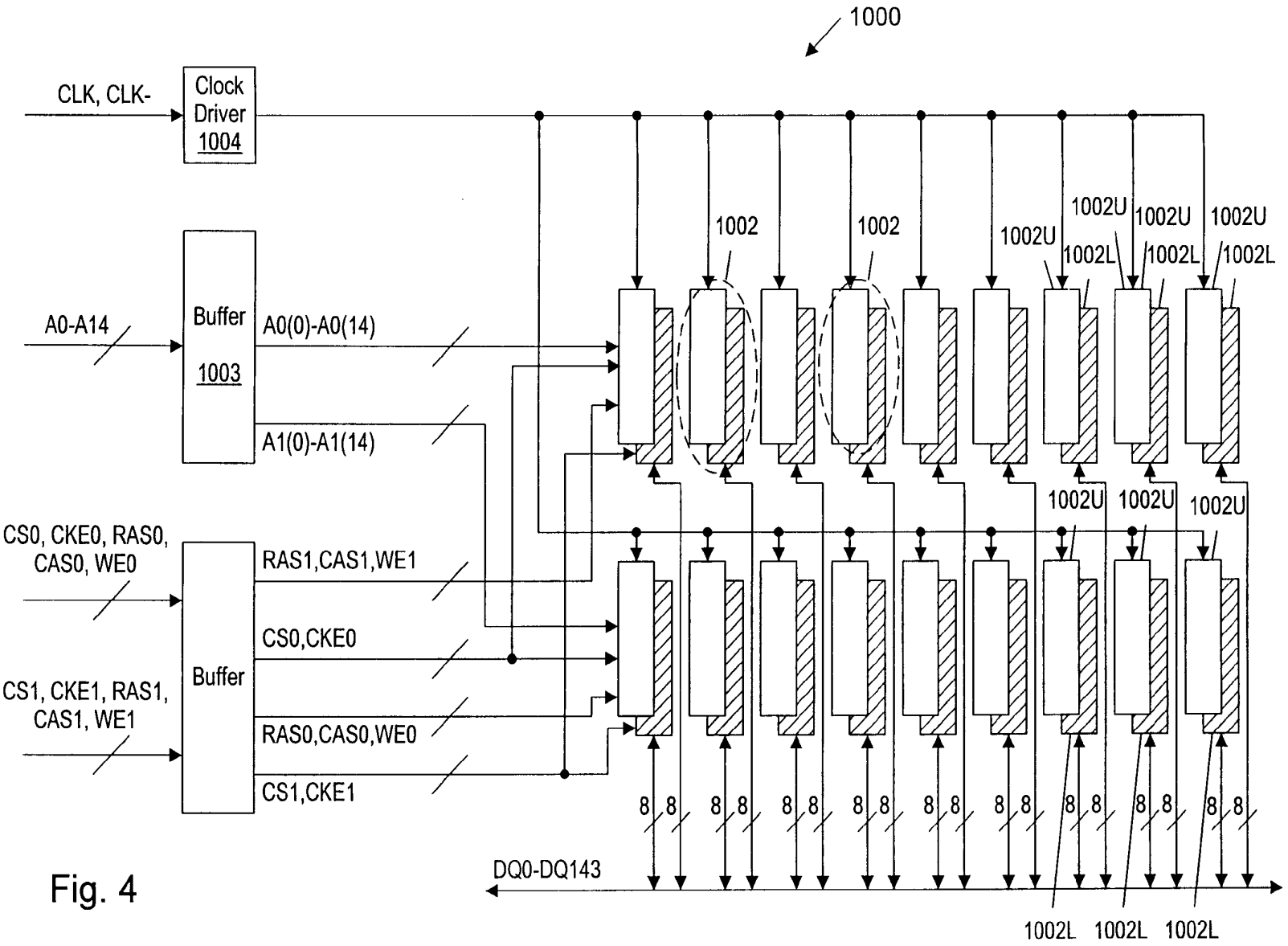


Fig. 4

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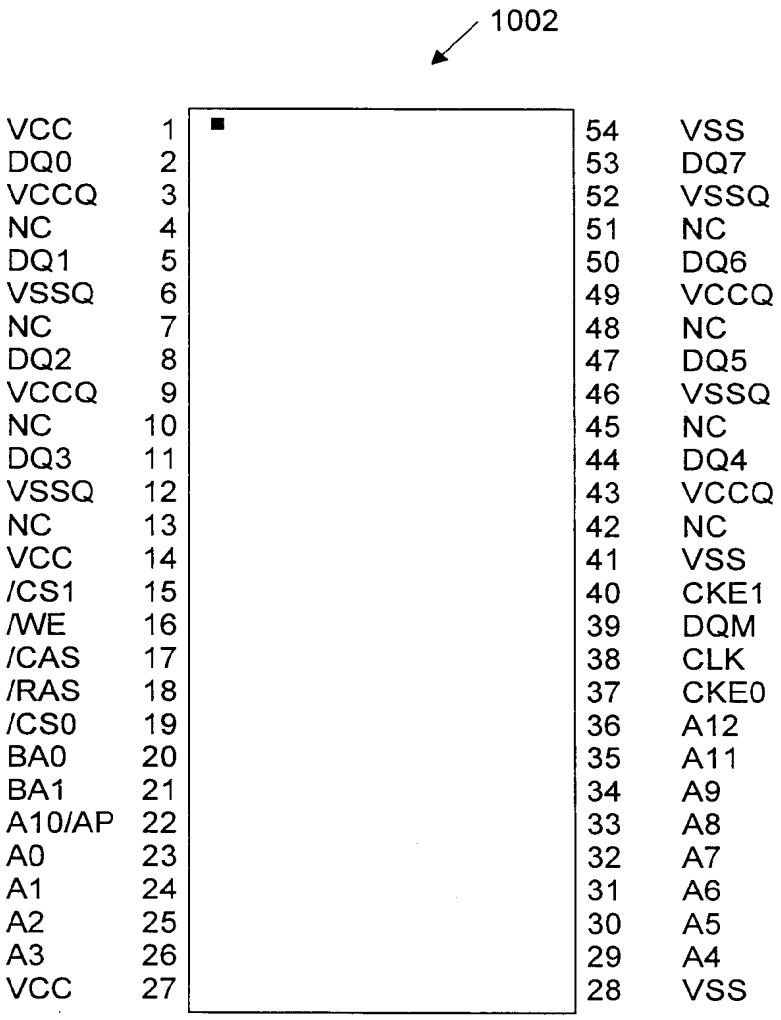


Fig. 5

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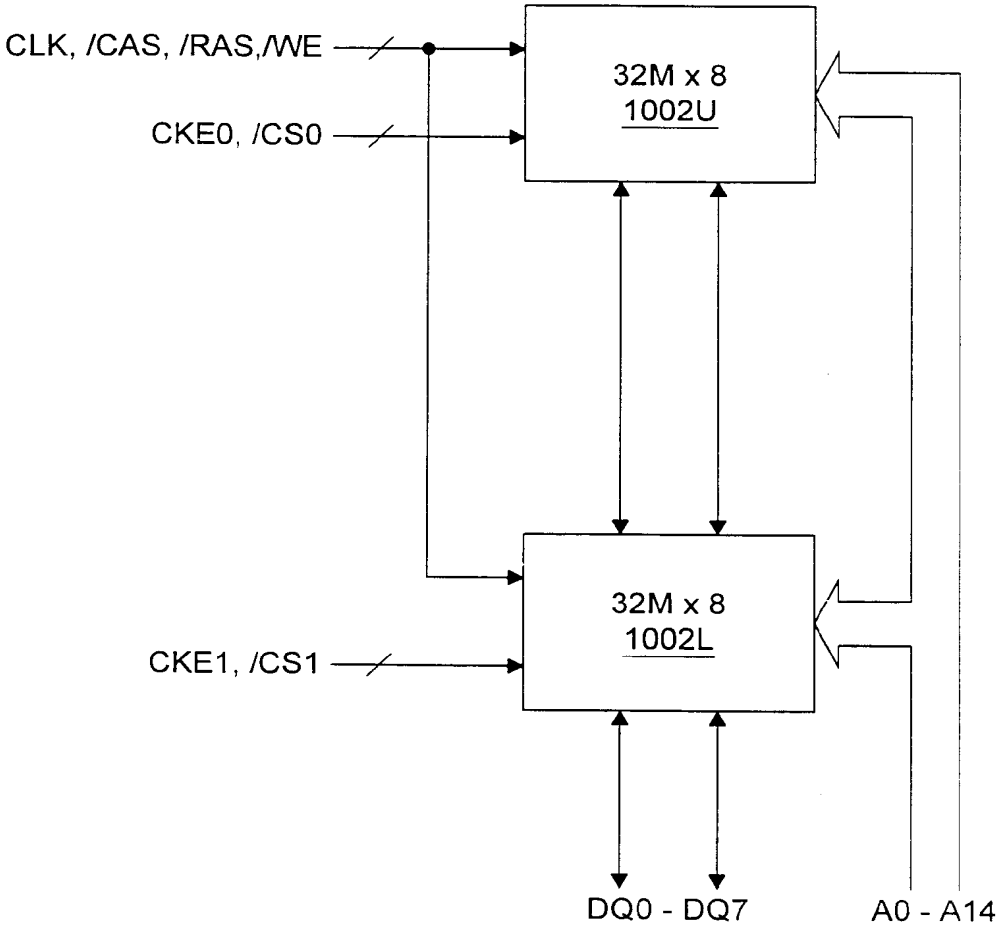


Fig. 6

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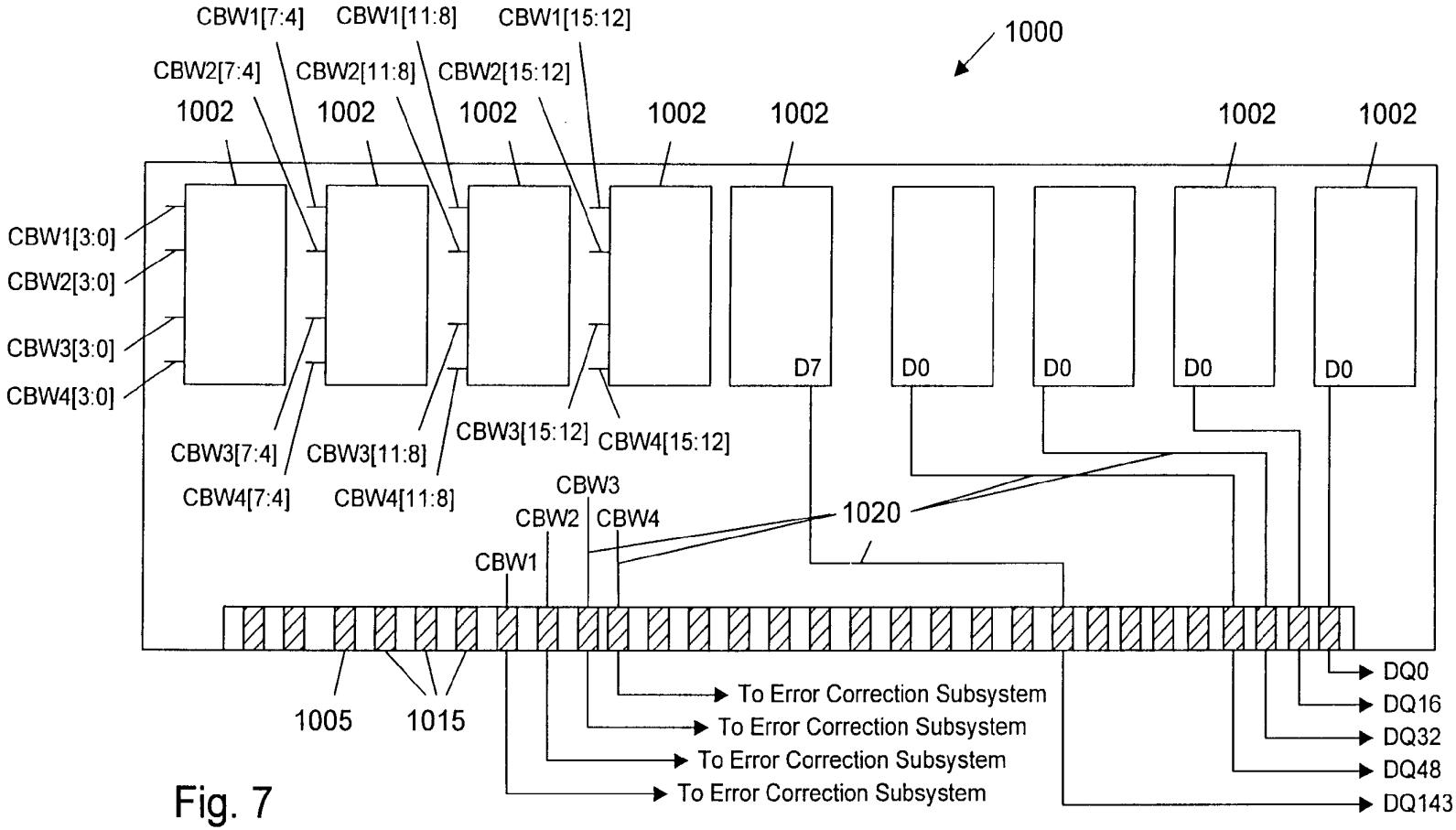


Fig. 7

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Connector Pad	1	2	3	4	5	6
IC and Pin #	U1.5	U1.6	U1.7	U1.8	U1.9	U1.10

Connector Pad	7	8	9	10	11	12
IC and Pin #	U2.15	U2.16	U2.17	U2.18	U2.19	U2.20

Connector Pad	13	14	15	16	17	18
IC and Pin #	U4.2	U4.3	U4.4	U4.5	U4.6	U4.7

Fig. 8

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INTERNATIONAL SEARCH REPORT

Inte ional Application No
PCT/US 00/31439

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F11/00 G06F11/10 G11C5/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 744 748 A (SILICON GRAPHICS INC) 27 November 1996 (1996-11-27) page 5, line 35 -page 6, line 27; figure 3; table 1 page 12, line 40-43	1-9, 11-24
A	US 5 661 677 A (RONDEAU II THOMAS C ET AL) 26 August 1997 (1997-08-26) abstract	1-24
A	EP 0 813 204 A (SUN MICROSYSTEMS INC) 17 December 1997 (1997-12-17) abstract; figure 1A	1-24

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 March 2001	22/03/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Huyghe, E

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte ional Application No
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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/582,797	**09/24/2024 10:04:16 AM Z ET**	**022955-000090**

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3546	FILED BY	LISA MARGARET ELLIOTT
PATENT CENTER #	67294168	AUTHORIZED BY	Khaled Shami
CUSTOMER #	151145	FILING DATE	01/24/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Chi-She Chen

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
DA / 220585	**E20249NA09307303**	**LISA MARGARET ELLIOTT**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	260.00	1	260.00
			TOTAL AMOUNT:	**$260.00**

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If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C.

371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 744 748 B1

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18.10.2000 Bulletin 2000/42

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(21) Application number: **96303385.7**

(22) Date of filing: **14.05.1996**

(54) **High memory capacity DIMM with data and state memory**

DIMM Hochleistungsspeicher mit einem Datenspeicher und einem Zustandsspeicher

Mémoire DIMM à capacité élevée comprenant une mémoire de données et une mémoire d'états

(84) Designated Contracting States:
DE FR GB IT

(30) Priority: **15.05.1995 US 440214**

(43) Date of publication of application:
27.11.1996 Bulletin 1996/48

(60) Divisional application: **00107135.6 / 1 020 864**

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US-A- 5 214 570
US-A- 5 272 664

- **PATENT ABSTRACTS OF JAPAN vol. 8, no. 153 (P-287) [1590] , 17 July 1984 & JP-A-59 052483 (FUJITSU), 27 March 1984,**

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Description

[0001] This application is related to commonly owned, co-pending U.S. Patent Application No. 08/440,967, filed May 15, 1995, entitled "DIMM Pair with Data Memory and State Memory."

[0002] The present invention relates generally to the field of computer memory, and more particularly, to a dynamic random access memory dual in-line memory module.

[0003] Dynamic, random access memory (DRAM) single in-line memory modules (SIMMs) and dual in-line memory modules (DIMMs) are preferred implementations of semiconductor main memory in computer systems of all sizes, including personal computers (PCs), workstations, supercomputers and the like. Both SIMMs and DIMMs include a printed circuit board (PCB) having an edge connector with a plurality of signal pads on opposite sides of the PCB for physical and electrical connection to a connector socket. DRAM or synchronous DRAM integrated circuit chips are mounted on the PCB, and are electrically connected to various connector signal pads. A SIMM has opposing signal pads electrically connected so that each pair carries a single signal. In a DIMM, opposing pads are not connected so that each pad can carry a separate signal. However, the terms SIMM and DIMM are often used synonymously in the memory art. A detailed description of a known DRAM SIMM can be found in commonly owned U.S. Patent No. 5,272,664 to Alexander *et al.*

[0004] In a multiprocessor computer system, main memory may be implemented as distributed shared memory or centralized (i.e., non-distributed) memory. Each processor generally has a local cache. Thus, the processors must maintain cache coherence. Most existing multiprocessors with cache coherence rely on snooping to maintain coherence. To accomplish this, all processors are connected to a common bus. The processors "snoop" the bus. That is, the information about which processors are caching which data items is distributed among all of the caches. Thus, straightforward snooping schemes require that all caches see every memory request from every processor. This inherently limits the scalability of these systems because the common bus and the individual processor caches eventually saturate. With today's high-performance RISC processors, this saturation can occur with just a few processors.

[0005] Directory structures avoid the scalability problems of snoopy schemes by removing the need to broadcast every memory request to all processor caches. The directory maintains pointers to the processor caches holding a copy of each memory block. Only the caches with copies can be affected by an access to the memory block, and only those caches need be notified of the access. Thus, the processor caches and interconnect will not saturate due to coherence requests. Furthermore, directory-based coherence is not dependent on any specific interconnection network like the bus used by most snooping schemes.

[0006] Few DSM multiprocessors that use directory structures have been developed. Examples of such DSM systems include Stanford University's Dash multiprocessor described in Lenoski, Daniel, *et al.,* "The Stanford Dash Multiprocessor," *IEEE,* pp. 63-79, March 1992; Massachusetts Institute of Technology's (MIT) Alewife multiprocessor described in Chaiken, David, *et al.,* "LimitLESS Directories: A Scalable Cache Coherence Scheme," *ACM,* pp. 224-234, 1991; and Convex Computer Corporation's Exemplar multiprocessor described in Brewer, Tony, "A Highly Scalable System Utilizing up to 128 PA-RISC Processors," *IEEE,* pp. 133-140, 1995.

[0007] In the Stanford Dash multiprocessor, the main memory was hardwired for maximum memory capacity.1 In the MIT multiprocessor and the Convex Computer Corporation multiprocessor, directory information was stored in main memory. Thus, the data and the directory information had to be accessed sequentially, limiting memory bandwidth.

[0008] What is needed is a technique for implementing main memory in a DSM multiprocessor computer system in a manner such that directory information is accommodated and such that straightforward memory expansion of both data memory and directory memory are concurrently supported.

[0009] The invention is a dual in-line memory module (DIMM) as indicated in claim 1. It includes a circuit board, and first and second memories mounted on the circuit board. The first memory is configured for storing data and is also called a data memory. The second memory, called a state memory, is configured for storing state information corresponding to at least a portion of the data stored in the data memory. State information includes, for example, cache coherence information (i.e., information on whether and where a block of data is cached, and where the most recent copy of the data resides), information regarding access rights to the data in the data memory, page migration information, and the like. The DIMM of the invention allows the state information in the state memory to be accessed separately from the data in the data memory. By "separately," it is meant that the state information can be read/written independently of and/or in parallel with data stored in the data memory.

[0010] A plurality of the DIMMs of the invention can be used to implement main memory in a distributed, shared memory (DSM) multiprocessor. The DIMM configuration provides a mechanism through which memory can be easily upgraded or replaced. Because the state information is stored on the DIMMs along with the data, an optimal memory management scheme is provided.

[0011] In a first embodiment, each DIMM provides 32 megabytes of data storage capacity and 4 megabytes of ECC (error correcting codes) in the data memory. To achieve this, the DIMM includes two memory bank portions (one per side of the DIMM circuit board) of two megabits deep by 72 bits wide (2M x 72). Of the 72 bits, 64 bits are for data and

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eight bits are for ECC. The state memory includes one megabit by 16 bits wide (1M x 16) of state information capacity. This embodiment can be implemented using a plurality of synchronous, dynamic, random access memory (SDRAM) chips.

[0012] In this embodiment, the circuit board of the DIMM is approximately 1.34 inches high by 6.6 inches long (note that the width dimension is given as a height, since DIMM boards are generally mounted perpendicular to another circuit board via an edge connector) and includes a 122 pad long by 2 pad wide edge connector along one longitudinal edge of the circuit board. The data memory is implemented using eighteen (18) two megabit by eight bit (2M x 8) SDRAM chips. Nine of the SDRAM chips are mounted on a front side of the circuit board, and nine are mounted on a back side of the circuit board. The state memory is implemented using a single one megabit by sixteen bit (1M x 16) SDRAM chip that is mounted on the front side of the circuit board.

[0013] The 244 pads of the edge connector provide separate data and address pads for the data memory and the state memory to allow each memory to be accessed independently and, if desired, in parallel. An address and control buffer is provided on each side of the circuit board. Each address and control buffer provides buffering for all address and control lines to the SDRAM chips for half of the data memory. In addition, a single clock driver is provided for all of the SDRAM chips of the DIMM. The clock driver provides two important functions. First, the clock driver provides sufficient drive current capacity to drive each SDRAM chip without unduly loading the source of the clock signal. Second, the clock driver provides a phase lock loop function to eliminate any skew or delay introduced by the buffering/driving circuitry of the clock driver.

[0014] In a second embodiment, each DIMM provides 64 megabytes of data storage capacity and 8 megabytes of ECC for a total of 72 megabytes of data storage in the data memory. To achieve this, the DIMM includes two memory bank portions of four megabits deep by 72 bits wide (4M x 72). The state memory includes two megabit by 16 bits wide (2M x 16) of state information capacity.

[0015] In this embodiment, the data memory is implemented using thirty-six (36) four megabit by four bit (4M x 4) SDRAM chips. This implementation requires a second circuit board mounted in a piggy-back fashion on the first circuit board. Eighteen of the SDRAM chips of the data memory are mounted on the first circuit board, substantially as set forth in the first embodiment, while the other eighteen SDRAM chips are mounted on the piggy-back board in a similar fashion. The state memory is implemented using two (2) two megabit by eight (2M x 8) bit SDRAM chips. One of the chips is mounted on each side of the first circuit board. Similar to the 36 megabyte embodiment, the first circuit board in the 72 megabyte embodiment includes a single clock driver and two address and control buffers. In addition, the piggy-back board includes its own single clock driver and pair of address and control buffers.

[0016] The invention utilizes the DIMM in a DIMM memory pair. A first DIMM of the pair includes a first data memory having first and second memory bank portions for storing data, and a first state memory configured to store state information corresponding to data stored in a first memory bank. A second DIMM of the pair includes a second data memory having third and fourth memory portions for storing data and a second state memory configured to store state information corresponding to data stored in a second memory bank. The first memory bank is formed from the first memory bank portion of the first DIMM and the third memory bank portion of the second DIMM. The second memory bank is formed from the second memory bank portion of the first DIMM and the fourth memory bank portion of the second DIMM. For example, if the first memory bank portion represents the front side of the first DIMM, the second memory bank portion represents the back side of the first DIMM, the third memory bank portion represents the front side of the second DIMM, and the fourth memory bank portion represents the back side of the second DIMM, then the first memory bank is represented as the front sides of the first and second DIMMs, while the second memory bank portion is represented by the back sides of the first and second DIMMs.

[0017] This DIMM pair configuration optimally provides a very wide dataword DIMM, which is implemented without imposing unwieldy requirements on the physical configuration of the edge connector of the DIMM. For example, each DIMM includes a 244 pad edge connector in the preferred embodiment. Using this connector, each DIMM provides a 72-bit-wide data path. Thus, the DIMM pair provides a 144-bit-wide data word. In the first embodiment described above, the 144-bit data word is provided in a DIMM pair with 64 megabytes of data storage capacity and 8 megabytes for ECC. In the second embodiment described above, the 144-bit data word is provided in a DIMM pair with 128 megabytes of data storage capacity and 16 megabytes for ECC.

[0018] When used in a DSM multiprocessor, the DIMM pairs of the invention are used to implemented main memory. Each processor node of the DSM multiprocessor includes a portion of main memory. In the 36 megabyte and 72 megabyte embodiments of the DIMM, the state memory configurations discussed provide sufficient capacity to accommodate the state information required for a system having a limited number of nodes (e.g., 16 nodes). For example, each state memory described above includes 16 bit wide words of state information.

[0019] When the number of nodes exceeds 16, more processors and caches will be present. Additional state data is required to keep track of the additional caches. Accordingly, more bits are required in the state memory to accommodate the extra nodes. The additional state memory can be provided by a state memory-only DIMM. This DIMM adds 32 bits of additional state memory. The resulting state memory provides 48 bit wide words of state information. With

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the additional state memory, the DSM multiprocessor can accommodate up to 64 nodes using conventional bit-vectors and up to 512 nodes using flexible directory bit vectors.

[0020] Thus, for a DSM multiprocessor having 16 nodes or less, the DIMM of the invention allows a directory-based memory structure to be implemented/upgraded using a single type of DIMM, configured in pairs. For a DSM multiprocessor having 512 nodes or less, the DIMM of the invention allows a directory-based memory structure to be implemented/upgraded using the DIMM pair of the invention and a state memory-only DIMM to expand state memory. In this manner, the DIMM of the invention provides significant advantages. First, when upgrading the number of processors, it is not necessary to replace existing DIMMs. Instead, existing DIMMs are merely supplemented with additional DIMMs and/or state memory-only DIMMs. Second, smaller systems need only one DIMM pair, not a DIMM pair plus a state memory-only DIMM, which reduces the cost of these systems. Third, because a single identical DIMM board, and in some instances a state memory-only DIMM board also, are used to implement main and directory/state memory, it is not necessary to manufacture, stock and distribute many different types of memory assemblies.

[0021] For purposes of illustration, a 36 megabyte embodiment and a 72 megabyte embodiment of the DIMM have been described. It should be understood, however, that the DIMM of the invention may be produced in other data capacities. For example, using 64 megabit (i.e., 8M x 8) SDRAM chips, a single board DIMM may be produced having 128 megabyte data and 16 megabyte ECC (18 chips x 8 megabytes per chip) storage capacity (including data and ECC). This would yield a DIMM pair having 256 megabytes of data storage capacity. If a piggy-back board is used as in the 72 megabyte DIMM embodiment described above, the 64 megabyte SDRAM chips can be used to implement a 256 megabyte data and 32 megabyte ECC DIMM and a 512 megabyte data, 64 megabyte ECC DIMM pair.

[0022] In the preferred embodiment described, a piggy-back board is used to allow the DIMM to accommodate 36 SDRAMs for the data memory. A person skilled in the art will recognize that chip stacking techniques may also be used to accommodate 36 SDRAM chips. If chip stacking techniques are used, the piggy-board may be eliminated.

[0023] The features and advantages of the invention will be apparent from the following, more particular description of several preferred embodiments of the invention, as illustrated in the accompanying drawings.

[0024] The invention will be better understood if reference is made to the accompanying drawings in which:

[0025] FIG. 1 is a representative high level block diagram of a SDRAM DIMM according to the present invention.

[0026] FIG. 2 is a representative schematic block diagram of the front and back of a SDRAM DIMM according to the present invention.

[0027] FIG. 3 is a representative logic diagram of a SDRAM DIMM pair having two banks and the state directory memory for those banks according to the present invention.

[0028] FIG. 4 is a representative schematic diagram of a 36 megabyte SDRAM DIMM according to a first embodiment of the present invention.

[0029] FIG. 5 is a representative schematic diagram of a 72 megabyte SDRAM DIMM according to a second embodiment of the present invention.

[0030] FIG. 6A is front plan view of a SDRAM DIMM according to the present invention.

[0031] FIG. 6B is back plan view of the SDRAM DIMM of FIG. 6A.

[0032] FIG. 7A is front plan view of a SDRAM DIMM piggy-back board according to the present invention.

[0033] FIG. 7B is back plan view of the SDRAM DIMM piggy-back board of FIG. 7A.

[0034] FIG. 8 illustrates a representative data read timing diagram according to the present invention.

[0035] FIG. 9 illustrates a representative data write timing diagram according to the present invention.

[0036] FIG. 10 illustrates a representative read/modify/write timing diagram according to the present invention.

[0037] FIG. 11 illustrates a representative state memory timing diagram for a memory read according to the present invention.

[0038] FIG. 12 illustrates a representative state memory timing diagram for a memory write or read-modify-write according to the present invention.

[0039] FIG. 13 illustrates a representative state memory timing diagram for operation of a state memory-only DIMM according to the present invention.

[0040] FIG. 14 illustrates the organization of DIMM pairs and state memory-only DIMMs in a node of a DSM multiprocessor

[0041] FIG. 15 illustrates a preferred exemplary pad assignment for an entire edge connector.

[0042] In the drawings, like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit of the reference number identifies the drawing in which the reference number first appears.

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I. Overview

[0043] The preferred embodiments of the invention are now described with reference to the figures. While specific steps, configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the relevant art will recognize that other steps, configurations and arrangements can be used without departing from the scope of the invention.

[0044] In a distributed, shared memory (DSM) multiprocessor such as that described in commonly-owned, co-pending U.S. Patent Application No. 08/435,456, filed May 5, 1995, entitled "System and Method For Network Exploration and Access in a Multi-Processor Environment," main computer memory is distributed across a processor network. Each distributed portion (node) of the main memory can be associated with one or more local processors. In such a system, memory management becomes quite complex. The DSM multiprocessor described in the above-identified application implements a directory-based cache coherence scheme that simplifies memory management. The directory-based memory management system is described in the following commonly-owned, co-pending patent applications:

U.S. Patent Application No. 08/435,460, filed May 5, 1995, entitled "Directory-Based Coherence Protocol Allowing Efficient Dropping of Clean-Exclusive Data,"
U.S. Patent Application No. 08/435,462, filed May 5, 1995, entitled "System and Method For a Multiprocessor Partitioning to Support High Availability,"
U.S. Patent Application No. 08/435,464, filed May 5, 1995, entitled "Page Migration In a Non-Uniform Memory Access (NUMA) System,"
U.S. Patent Application No. 08/435,459, filed May 5, 1995, entitled "System and Method For Maintaining Coherency of Virtual-to-Physical Memory Translations in a Multiprocessor Computer," and
U.S. Patent Application No. 08/435,463, filed May 5, 1995, entitled "Cache Coherency Using Flexible Directory Bit Vectors."

[0045] The present invention is a dual in-line memory module (DIMM) for implementing a main memory in a DSM such as that described in the above-referenced patent applications. Advantageously, the invention provides both data memory and state memory on a DIMM. This facilitates installation, replacement, expansion, testing and extension of the distributed main memory.

II. Architecture of the DIMM

[0046] FIG. 1 is a high-level, function block diagram of a DIMM 102 of the invention. DIMM 102 includes a printed circuit board 103, a data memory 104, and a state memory 106. Circuit board 103 is a multilayer (e.g., eight layer) printed circuit board having an edge connector 108. Edge connector 108 typically provides all electrical communications for data memory 104 and state memory 106. Edge connector 108 is configured for being inserted into a connector socket (not shown) such as socket part number ELF244LFCE-4Z50, available from Burndy Corporation, Norwalk, Connecticut.

[0047] Edge connector 108 provides a plurality of data pads 118 that allow data access to data memory 104 via data

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path 110, a plurality of address pads 120 for communicating address and control information to data memory 104 via address and control path 112, a plurality of data pads 122 that allow data access to state memory 106 via data path 114, and a plurality of address pads 124 for communicating address and control information to state memory 106 via address and control path 116. By "access" to a memory, it is meant to read data from or write data to the memory.

[0048] Data memory 104 is configured to store data. The data stored in data memory 104 is generally portioned into data blocks. State memory 106 is configured to store state information corresponding to blocks of data in data memory 104. State information (also known as directory information) includes, for example, cache coherence information (i.e., information on whether and where a block of data is cached, and where the most recent copy of the data resides), information regarding access rights to the data in the data memory, page migration information, and the like. Because connector 108 provides separate address and data pads for state memory 106 and data memory 104, the data and corresponding state information can be separately accessed. By "separately," it is meant that the state information can be read/written independent from and/or in parallel with data being read/written from/to the data memory. This allows the data and state information to be accessed simultaneously.

[0049] FIG. 2 illustrates a more detailed functional block diagram of DIMM 102. In this functional representation, both a front side 202 and a back side 204 are illustrated. Connector 118 is depicted between front side 202 and back side 204. This figure can be best understood by viewing the DIMM like a book that has been opened such that the binding is situated in the center, with both the front and back covers being visible. Connector 118 is analogous to the binding of the book. As illustrated, connector 118 includes a first row of connector pads 206 on front side 202 and a second row of connector pads 208 on back side 204 of circuit board 103.

[0050] As illustrated in this figure, data memory 104 is implemented by a first bank portion 210 on front side 202 and a second bank portion 212 on back side 204. State memory 106 is shown mounted on front side 202. Address and control path 112 is buffered by address and control buffers 214,216. Address and control buffer 214 provides address and control signals (i.e., row address strobe, column address strobe, write enable and data mask) to a left side of first bank portion 210 and a left side of second bank portion 212 via bus 113. In addition, address and control buffer 214 provides a chip select signal and a clock enable signal to both the left and right sides of first bank portion 210 via lines 117.

[0051] Similarly, address and control buffer 216 provides address and control signals (i.e., row address strobe, column address strobe, write enable and data mask) to a right side of first bank portion 210 and a right side of second bank portion 212 via bus 115. In addition, address and control buffer 216 provides a chip select signal and a clock enable signal to both the left and right sides of second bank portion 212 via lines 119. The chip select signals are used to select between first bank portion 210 and second bank portion 212. Buffers 214,216 are arranged to buffer left and right sides of memory bank portions 210,212 to simplify routing of the signal lines on circuit board 103. Alternatively, buffer 214 may be configured to buffer signals only for bank portion 210, and buffer 216 may be configured to buffer signals only for bank portion 212.

[0052] A clock driver 218 is mounted on front side 202 of circuit board 103. Clock driver 218 receives a clock signal from clock signal and control lines 220 and provides sufficient drive current for clock driver 218 to drive a plurality of memory chips that are used to form first and second memory bank portions 210,212 as well as state memory 106. Clock driver 218 also includes a phase-lock loop function that eliminates skew from a clock signal 222, which is being distributed to the various memory chips of the data and state memories on DIMM 102.

[0053] In one embodiment, back side 204 of DIMM 102 includes an SPROM (serial programmable read only memory) 224. SPROM 224 can be used to provide a unique identification number (e.g., a serial number) for DIMM 102. A suitable SPROM is available from Dallas Semiconductor, Dallas, Texas, as Part No. DS2502, which is also known as a NIC (Number In a Can).

III. Implementation of the DIMM in a DIMM Pair

[0054] In a preferred embodiment of the invention, DIMM 102 is used to implement main computer memory only in pairs. Each DIMM of the pair provides half of a data word, such that the pair together is able to provide a very wide data word. This is illustrated in FIG. 3, in which a DIMM 102A and a DIMM 102B form a DIMM pair 302. As illustrated, DIMM 102A includes first memory bank portion 210A, second memory portion 212A, and first state memory 106A. Similarly, DIMM 102B includes first memory bank portion 210B, second memory bank portion 212B, and second state memory 106B.

[0055] In this implementation, first memory bank portion 210A and second memory bank portion 212B form a first memory bank, labeled bank 0. State information for data stored in bank 0 is maintained in state memory 106A. Second memory bank portion 212A and first memory bank portion 210B form a second memory bank, labeled bank 1. State memory 106B is configured to store state information corresponding to data stored in memory bank 1. As discussed in further detail below, a bank select signal is used to select one of bank 0 or bank 1 for data access operations. Memory bank 0 and memory bank 1 share common address and data lines.

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[0056] The DIMM of the invention can be produced with a variety of different data storage capacities. In a first preferred embodiment, DIMM 102 has a thirty-six (36) megabyte data storage capacity (including 32 megabytes of data and 4 megabytes of ECC) and a two (2) megabyte state information storage capacity. This embodiment yields a DIMM pair having sixty-four (64) megabytes of data storage capacity, eight (8) megabytes of ECC, and four (4) megabytes of state information storage capacity. In a second embodiment, DIMM 102 has a seventy-two (72) megabyte data storage capacity (including 64 megabytes of data and 8 megabytes of ECC) and a four (4) megabyte state information storage capacity. This embodiment yields a DIMM pair having one hundred twenty-eight (128) megabytes of data storage capacity, sixteen (16) megabytes of ECC, and eight (8) megabytes of state information storage capacity.

IV. Details of the DIMM Interconnects

[0057] FIG. 4 is a block diagram illustrating interconnection of the components used to implement a DIMM 102 in accordance with the first preferred embodiment of the invention. Data memory 104 is implemented using a plurality of synchronous, dynamic, random access memory (SDRAM) chips D0-D17. SDRAMs D0-D8 represent memory chips of first memory bank portion 210, while SDRAMs D9-D17 represent memory chips of second memory bank portion 212. In this 32 megabyte embodiment of DIMM 102, each SDRAM D0-D17 is a two megabit by eight bit (2M x 8) SDRAM chip. Thus, each memory bank portion 210,212 is two (2) megabits deep by seventy-two (72) bits wide, yielding a total data capacity for data memory 104 of four (4) megabits deep by seventy-two (72) bits wide (i.e., 64 bits for data and 8 bits for ECC). State memory 106 is implemented using a single one megabit by sixteen (1M x 16) bit SDRAM chip.

[0058] Each DRAM chip D0-D17 provides an 8-bit data word. To accommodate communications with each SDRAM, data path 110 provides an 8-bit data path DQ. As indicated, one chip from each of memory bank portions 210,212 is connected to an 8-bit data path DQ. For example, SDRAM D0 and SDRAM D9 are both connected to DQ[7:0]. Which chip is actually active on the data path is determined by an external chip or bank select signal (discussed below).

[0059] Address and control buffers 214,216 receive 20-bits of address and control signals, labeled A[19:0], buffers the address and control signals, and provides the address and control signal to SDRAMs D0-D17 as follows. Address and control buffer 214 provides address and control signals (i.e., row address strobe, column address strobe, write enable and data mask) to left sides of bank portions 210,212 (i.e., SDRAMs D0-D3 and D9-D12) via bus 113. In addition, address and control buffer 214 provides a bank select signal (CS0_) and a clock enable signal (CKE0) to both the left and right sides of first bank portion 210 (i.e., SDRAMS D0-D8) via lines 117.

[0060] Address and control buffer 216 provides address and control signals (i.e., row address strobe, column address strobe, write enable and data mask) to right sides of bank portions 210,212 (i.e., SDRAMs D4-D8 and D13-D17) via bus 115. In addition, address and control buffer 216 provides a bank select signal (CS1_) and a clock enable signal (CKE1) to both the left and right sides of second bank portion 212 (i.e., SDRAMS D9-D17) via lines 119. Address and control signals A[19:0] are described further below in Table 1.

[0061] Clock driver circuit 218 provides clock signal 222 to each of SDRAMs D0-D17 and to the SDRAM of state memory 106. Clock driver circuit 218 generates clock signal 222 based on clock control signals C[5:0]. The clock control signals C[5:0] are described in further detail below. The data path 114 and address and control path 116 of state memory 106 are illustrated by lines DIR_DQ[15:0] and B[17:0], respectively. These signals are also described in further detail below.

[0062] The 72 megabyte embodiment of DIMM 102 is depicted in FIG. 5. In this embodiment, rather than using eighteen two megabit by eight bit (2M x 8) SDRAMs, the DIMM is implemented using thirty-six (36) four megabit by 4 bit (4M x 4) SDRAMs. To accommodate the additional chips, a second circuit board 500 is used. Eighteen of the 4M x 4 SDRAMs (D0-D17) are mounted on a first circuit board 103. The other eighteen 4M x 4 SDRAMs (D18-D35) are mounted on second circuit board 500. Circuit board 500 is mounted on circuit board 103 in a piggy-back fashion. Only circuit board 103 includes edge connector 108 (not shown in Figure 5). All electrical connections to the SDRAM chips of circuit board 500 occur through the edge connector of circuit board 103. Signals are shared by the two boards using a plurality of interconnecting pins. Each end of each pin is located in a plated through hole to provide electrical connections between the boards. These pins also physically attach the second board to the first board. An example of a piggy-back mounted circuit board (not using plated through holes) is provided in U.S. Patent No. 5,200,917 to Shaffer *et al.*

[0063] In this embodiment, first memory bank portion 210 is formed from the front side of each of circuit boards 103,500. For example, SDRAM chips D0-D8 and D27-D35 can be used to implement first memory bank portion 210. Similarly, the back side of each circuit board 103,500 can be used to implement second memory bank portion 212. This includes, for example, SDRAM chips D9-D17 and D18-D26. The chips on each circuit board 103 and 500 include on-board clocking and buffering via clock drivers 218A,218B and address and control buffers 214A,214B,216A,216B. However, in this embodiment, each SDRAM chip is coupled to a 4-bit data path rather than an 8-bit data path. Thus, a corresponding SDRAM chip from each board is used to form the 8-bits provided by a single chip in the 36 megabyte DIMM. As in the 36 megabyte DIMM embodiment of FIG. 4, all SDRAM chips D0-D35 are addressed simultaneously.

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A bank select signal (one of signals A[19:0]) is used to select between memory bank portion 210 and memory bank portion 212.

V. DIMM Chip Layout

[0064] A preferred implementation of the 32 megabyte DIMM embodiment is depicted in FIGS. 6A and 6B. FIG. 6A shows front side 202 of DIMM 102. FIG. 6B shows back side 204 of DIMM 102. In this preferred implementation, circuit board 103 is approximately 1.34 inches high by 6.6 inches long and includes a 122 pad long by 2 pad wide edge connector along one longitudinal edge of the circuit board. SDRAMs D0-D8, SDRAM DIR0 (for state memory 106), data and control buffers 214A and clock driver 218A are mounted on the front side 202 of circuit board 103. SDRAMs D9-D17 and data and control buffer 216A are mounted on the back side 204 of circuit board 103.

[0065] FIGs. 6A and 6B are representative of the 72 megabyte embodiment of the invention as well as the 32 megabyte embodiment with the following differences. First, in the 72 megabyte embodiment, SDRAMs D0-D17 are 4M x 4 devices instead of 2M x 8 bit devices. Second, the directory memory chip (indicated as DIR 0) is a 2M x 8 bit device instead of a 1M x 16 bit device. Third, in the 72 megabyte embodiment, a second 2M x 8 bit SDRAM chip (indicated by dashed lines in FIG. 6B as DIR 1) is used with DIR 0 to implement state memory 106.

[0066] A preferred implementation of the piggy-backed second circuit board 500 of the 72 megabyte DIMM embodiment is depicted in FIGS. 7A and 7B. FIG. 7A shows a front side 702 of second circuit board 500. FIG. 7B shows a back side 704 of second circuit board 500. In this preferred implementation, circuit board 500 is approximately 1.16 inches high by 6.6 inches long and includes 116 interconnecting pins (not shown) providing electrical connections with circuit board 103. SDRAMs D18-D26, data and control buffer 214B and clock driver 218B are mounted on the front side 702 of circuit board 500. SDRAMs D27-D35 and data and control buffer 216B are mounted on the back side 704 of circuit board 500.

VI. The Pad Description

[0067] Table 1 lists the pad name and functions for the edge connector's pads according to a preferred embodiment of the present invention. The left-hand column lists the abbreviated pad names and the right-hand column lists the function of the pads listed in the associated row of the table.

Table 1

Pad Description	
Pad Name	**Function**
A[11:0][A]	Data Memory Address (Row:A[10:0]; Col:A[9:0]; Bank select: A11)
DQ[71:0]	Data I/O Pads for Data Memory
CS1 , CS0 [A]	Chip select for Data Memory SDRAMs
RE [A]	Row address strobe (RAS) command for Data Memory
CE [A]	Column address strobe (CAS) command for Data Memory
WE [A]	Write enable command for Data Memory
DQM[A]	Input/Output mask for Data Memory
CKE1,CKE0[A]	Memory clock enable for CS1 and CS0 SDRAM's respectively
DIR A[11:0][B]	State Memory Address (Row:A[10:0]; Col:A[7:0]; Bank select: A11)
DIR DQ[15:0]	Directory data (i.e., state information) I/O for State Memory
DIR CS[B]	Directory chip select for State Memory
DIR RE[B]	Directory row address strobe command for State Memory
DIR CE[B]	Directory column address strobe command for State Memory
DIR WE[B]	Directory write enable command for State Memory

[A]= These pads are shown collectively on FIGS. 4 and 5 as A[19:0]

[B]= These pads are shown collectively on FIGS. 4 and 5 as B[17:0]

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Table 1 (continued)

Pad Description	
Pad Name	**Function**
DIR DQM[B]	Directory input/output mask for State Memory
DIR CKE[B]	Directory clock enable for State Memory
PCLK, PCLK[c]	Differential LVPECL clock inputs
TCLK[C]	LVTTL clock inputs
TCLK SEL[C]	Selects TCLK when high and PCLK when low
PLL EN[C]	Enables PLL on clock driver
PLL CLR[C]	PLL reset and tri-state clock driver outputs
V3	Power supply (3.3VD.C.)
GND	Ground
SERIAL DAT	Line to read contents of serial prom

[B]= These pads are shown collectively on FIGS. 4 and 5 as B[17:0]

[C]= These pads are shown collectively on FIGS. 4 and 5 as C[5:0]

[0068] The first pad description is for the address pads and is abbreviated A[11:0]. During row addressing the eleven least significant bits are used. During column addressing the nine least significant bits are used in the 36MB DIMM embodiment, and the ten least significant bits are used in the 72MB DIMM embodiment. The most significant bit (A11) is used to select between internal SDRAM banks. (These "internal banks" are different banks than banks zero and bank one of SDRAM DIMM 102 described above. Therefore, banks zero and one will hereafter be referred to as "external" banks that are selected via external back chip select signals CS1 and CS0, to distinguish them from the "internal SDRAM bank select" signal A11. This naming convention applies for SDRAMs used for data, as well as those used to store state information.)

[0069] Data is input to, and output from the data memory of the SDRAM DIMM via 72 data input/output (I/O) paths abbreviated DQ[71:0]. Since the SDRAM DIMMs are used in pairs, a single access of the data memory on a single DIMM provides 72 bits, which when concatenated with 72 bits of the paired DIMM, yields a 144 bit data word that includes 128 bits of data an 16 bits of ECC.

[0070] There are eight remaining paths for the data memory of the SDRAM DIMM. Two external bank chip select pads abbreviated CS1_ and CS0_, a row address strobe command pad abbreviated RE_, a column address strobe command pad abbreviated CE_ and a write-enable command pad abbreviated WE_ are standard signals used for selecting, addressing, and write-enabling SDRAM chips, as would be apparent to a person skilled in the relevant art. Similarly, two pads are provided for memory clock enable for the two banks of SDRAMs, respectively, and are abbreviated CKE1 and CKE0. A single input/output mask path is also provided, and is abbreviated DQM. The function of the DQM mask pad will be described below in connection with the waveform diagrams.

[0071] The pads for the state memory of the SDRAM DIMM will now be described. The collection of directory address pads are abbreviated DIR_A[11:0]. Row addressing for the state memory uses directory address bits A[10:0] and column addressing utilizes directory address bits A[7:0] for a 32MB DIMM and bits A[8:0] for a 72MB DIMM. A twelfth directory address pad (A11) is used for internal SDRAM bank selection.

[0072] Sixteen bits of state information is provided by directory data I/0 pads abbreviated DIR_DQ[15:0]. The next five pads listed in Table 1 have similar functionalities as described above in connection with the analogous paths for the data memory section of the SDRAM DIMM. The directory chip select pad is abbreviated DIR_CS_. A directory row address strobe command pad is abbreviated DIR_RE_. A directory column address strobe command pad is abbreviated DIR_CE_. A directory write-enable command pad is abbreviated DIR_WE_. A directory input/output mask pad is abbreviated DIR_DQM. An additional directory clock-enable pad, abbreviated DIR_CKE, is provided for enabling the state memory clock.

[0073] According to a preferred embodiment of the present invention, a Motorola, Inc., (Phoenix, Arizona) MPC931 PLL chip, is used as a clock driver circuit. Because this specific integrated circuit supports both low voltage transistor-transistor-logic (LVTTL) or low voltage positive emitter coupled logic (LVPECL) respectively, the SDRAM DIMM of the present invention can include pads to facilitate either type of logic level for the clock driver circuit. Therefore, differential LVPECL clock pads abbreviated PCLK and PCLK_ are provided. Additionally, a LVTTL clock pad abbreviated TCLK is also provided. To select between the two possible power pad inputs, a select pad abbreviated TCLK_SEL is provided.

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The logical voltage value applied to the TCLK_SEL pad will select which voltage pads that the clock driver circuit will use. For example, the TCLK can be selected when the TCLK_ SEL pad is a logic high and the PCLK pad can be used for powering the clock driver circuit when the TCLK_SEL pad is at a low logic level. Another pad enables the phase lock loop portion of the clock driver circuit, and is abbreviated PLL_EN. Reset and tri-state clock driver circuit outputs for this manufacturers' chip can be selected via another pad abbreviated PLL_CLR. Other suitable pad arrangements using functionally similar PLL (phase locked loop) chips would be apparent to a person skilled in the relevant art.

[0074] A power supply voltage (*e.g.*, 3.3 V.D.C.) and ground are supplied via pads abbreviated V3 and GND respectively. If implemented, a single additional pad is used to read the contents of the serial programmable read-only memory (PROM), which is labeled SERIAL_DAT.

[0075] FIG. 15 illustrates a preferred exemplary pad assignment for the entire 244 connector pad edge connector 108. This figure is broken-down into 6 columns in order to show all 244 pad assignments on a single page. 14 pads are unassigned. Each column shows the pad number assignment followed by the abbreviation of the pad description corresponding to the pad names listed in Table 1. The pad assignments are made taking trace lengths on the PCB 103 into consideration to minimize signal skew and loading.

VII. Timing Requirements

[0076] Table 2 shows representative timing requirements for an exemplary SDRAM DIMM pair using NEC Corporation (Japan) part numbers uPD4516421GS-A12-TJF (4Mx4), uPD4516421GS-A12-TJF (2Mx8) or uPD45161GS-A12-TJF (1Mx16). The timing requirements listed in Table 2 are for nominal temperatures between 0 and 70°C and a power supply voltage of between 3.3 volts and 3.6 V.D.C., with all clock references to PCLK. The timing requirements of Table 2 include clock jitter and skew of approximately 1.5 nanoseconds.

Table 2

Timing Requirements	
(Ta = 0 to 70C, VDD, VDDQ = 3.15VDC to 3.6 VDC) All clock references (Ref) are to PCLK. The timings include a clock jitter + skew of 1.5ns max	
1.	Clock cycle time = 20ns max
2.	Clock to data in setup = 4.5ns min
3.	Clock to data in hold = 2.5ns min
4.	Set up time input address = 12.0ns min
5.	Hold time input address = 1.0ns min
6.	Set up time input command = 12.0ns min
7.	Hold time input command = 1ns min
8.	Access time from clock (CAS latency = 2) = 15ns max, load 80pf
9.	Hold time output data = 1.5ns min
10.	Clock to data out, high impedance = 16.5ns max, load 80pf
11.	Clock to CKE setup (power down exit) = 12.0ns max
12.	Clock to CKE hold = 1.0ns min
13.	Ref/active to Ref/active command period = 110ns min
14.	Active to precharge command period = 75 ns min - 10000ns max
15.	Active command to column command (same bank) = 38ns min
16.	Precharge to active command period = 38ns min
17.	Last data in to precharge lead time = 18ns min
18.	Refresh period = 64ms max

[0077] The timing parameters shown in Table 2 generally represent time periods as measured at the edge connector,

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ignoring any small effects the connector itself will have on the signals. These times would appear different if measured at a location on the SDRAMs themselves. The row and column addresses are set by a memory system into which the SDRAM DIMMs are connected and as required by the specific SDRAM devices employed on the DIMMs.

VIII. Waveform Diagrams

[0078] The timing diagrams for reading and writing information for the SDRAM DIMM are shown in FIGS. 8-13. FIG. 8 shows a representative "data read" timing diagram according to the present invention. FIG. 9 shows a representative "data write" timing diagram according to the present invention. FIG. 10 shows a representative "read modify write" (RMW) timing diagram according to the present invention. The vertical bars represent clock edges, at which the control and address signals are sampled by the SDRAM parts.

[0079] Turning now to FIG. 8, a total of six timing traces are illustrate, including: chip select (CS_) 802; row address strobe (RE_) 804; column address strobe (CE_) 806; write-enable (WE_) 808; address (A) inputs 810; and, data (DQ) inputs/outputs 812.

[0080] The SDRAM DIMMs data output 812 represents the timing of an output based on application of the row and column addresses and assertion of the RE_, CE_ and WE_ control signals. The data memory is arranged so that a single row access can be followed by four column addresses (C0, C2, C4 and C6) to access a block of data from a DIMM pair. A block of data (not including parity/ECC data) is 8 words by 16 bytes, or a total of 128 bytes (which is 64 bits per DIMM or a total of 128 bits per location access, since the pair is accessed in parallel). So for 4 consecutive location accesses per RA, a total of 8 data words D0-D7 by 16 bytes are output. Similarly, the SDRAM DIMM pair is written to in block writes as illustrated by trace 902 in FIG. 9. Table 3 shows representative cycle latency for various timing parameters of FIGs. 8-10. These parameter latencies are listed in nanosecond and are nominal.

Table 3

Cycle Latency at 50MHZ	
1.	CAS latency = 2(number of clocks between CE_ command and data is available).
2.	tRCD = 2(minimum number of clocks between RE_ and CE_ commands).
3.	RAS latency = 4 (minimum number of clocks between RE_ and data is available).
4.	tRC = 6 (minimum number of clocks between refresh and RE_ command).
5.	tRAS = 4 (minimum number of clocks between RE_ and precharging).
6.	tRRD = 2 (minimum number of clocks between RE_ commands).
7.	tRP = 2 (minimum number of clocks between precharging and RE_ command).
8.	tDPL = 1 (minimum number of clocks between data in and precharging command).
9.	tDAL = 3 (minimum number of clocks between data in and RE_ for auto-precharging).

[0081] Read modify writes can also be done on data, as shown in FIG. 10. A location is accessed by a single RE_ and CE_ (traces 1002 and 1004 respectively) and the data is read at the first D0/D1 pair 1006. After the data is modified it is written back as shown by the second D0/D1 pair (1008) to the DIMM pair by asserting the CE_ and the WE_ (trace 1010) signals.

[0082] As noted above, the state memory is accessed in parallel with the data memory. A state memory comprises two reads and two writes, since each directory entry is 32 bits wide, and each state memory in the preferred embodiment implements SDRAMs that are only 16 bits deep. Also, page migration incrementing requires reading the location that corresponds to the block being accessed for both the node making the request and the home node, and a write to increment the count for the node making the request. The page migration counts keep track of the number of times a node accesses a particular page of memory. Thus, that count must be incremented each time a page is accessed. If the count for some node accessing a given page exceeds either a predetermined threshold or the count for the requestor minus the count for the home node exceeds another threshold, the page is migrated to the memory associated with that node. A more detailed description of page migration is found in the co-pending application (Attorney Docket No. 1452.0690000) noted above. Thus, during the 8 cycle read or write of the data memory, the corresponding state memory is read a total of 4 times and written to a total of 3 times, so that accesses to the data and state information is balanced.

[0083] FIGS. 11, 12 and 13 show three separate waveform diagrams involving data masking, including reads, writes, and revisions, respectively. In FIG. 11 the following signals are shown: chip select (DIR_CS_), row address strobe (DIR_RE_), column address strobe (DIR_CE_), write enable (DIR_WE_), input/output data masks (DIR_DQM), address A inputs and data (DIR_DQ) input/outputs. The directory cycle for a read starts by reading the first half of the directory word (D0), the page migration count for the requesting node (S), the second half of the directory word (D1), the home node's page migration count (H), then after a dead cycle on DIR_DQ, the new page migration count (S) and

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the new directory information (D0 and D1) are written into the state memory. The information is read out in the listed order due to requirements of the memory controller that lead to the quickest memory response time.

[0084] FIG. 12 is a slight permutation of the waveforms shown in FIG. 11. The order of S and D0 are switched in this figure in contrast to FIG. 11.

[0085] FIG. 13 shows the state access for a state revision operation, which is a state-only access and does not require a memory access. To minimize the overhead of these revisions operations only the directory information is accessed.

XI. Expanded State Memory

[0086] When used in a DSM multiprocessor, the DIMM pairs of the invention are used to implement main memory. Each processor node of the DSM multiprocessor includes a portion of main memory. In the 36 megabyte and 72 megabyte embodiments of the DIMM, the state memory configurations discussed provide sufficient capacity to accommodate the state information required for a system having 16 nodes. For example, each state memory described above includes 16 bit wide words of state information.

[0087] When the number of nodes exceeds 16, additional state memory is required at each node to accommodate more state information about caching, because more cache memories are likely added to the system. The additional state memory can be provided by using a state memory-only DIMM. According to a preferred embodiment of this aspect of the present invention, this state memory-only DIMM adds 32 bits of additional state memory. The resulting total state memory provides 48 bit wide words of state information (16 original bits on the SDRAM data/state memory DIMM plus 32 bits from the state memory-only DIMM). With the additional state memory, the DSM multiprocessor can accommodate up to 64 nodes using conventional bit-vectors and up to 512 nodes using flexible directory bit vectors. The specific number of additional state information bits can vary and is extendable, as would be apparent to a person of ordinary skill in the relevant art.

[0088] The organization of DIMM pairs 302 and state memory-only DIMMs 1406 in a main memory portion 1400 of a node of a DSM multiprocessor is illustrated in Figure 14. A memory/directory controller 1402 at the node of the DSM multiprocessor performs all memory management functions for the data and state memory on the DIMMs 302 and 1406. A memory address and control buffer 1410 buffers all address and control lines 1420 going to the data memories of the DIMM pairs 302 from the controller 1402. A state (directory) address and control buffer 1412 buffers all address and control signals on lines 1422 going to the state memories of the state memory-only DIMM pairs 1406 from the controller 1402.

[0089] Each state memory-only DIMM 1406 can be implemented using a single PCB. The PCB can be populated with SDRAM chips of similar or dissimilar capacity chips as the SDRAMs of the DIMMs 302. The SDRAMs of the state memory-only DIMMs 1406 are organized with two banks of state memory so that state information and addressing of the state information is consistent with the directory (DIR)/state memories on the DIMMs 302.

[0090] A bus exchanger 1408 passes the 144 bit data word to/from each DIMM pair 302 via bidirectional buses 1409. The bus exchange 1408 takes 144 bits data at the memory speed and converts it to 72 bits at twice the memory speed. In a preferred embodiment, the bus exchanger 1408 is implemented with a part number SN74ALVC16282 (manufactured by Texas Instruments, Dallas Texas) that converts 144 bits at 50 MHz to 72 bits at 100MHz, and vice versa for bidirectional transfer of the data between the DIMMS 302 and the controller 1402, via bidirectonal bus 1411. Directory data is not buffered, and is transferred between the state memory-only DIMMs 1406 and the controller 1402 via bidirectional bus 1424.

[0091] For purposes of illustration, a 36 megabyte embodiment and a 72 megabyte embodiment of the DIMM have been described. It should be understood, however, that the DIMM of the invention may be produced in other data capacities. For example, using 64 megabit (i.e., 8M x 8) SDRAM chips, a single board DIMM may be produced having 128 megabyte data and 16 megabyte ECC (18 chips x 8 megabytes per chip) storage capacity (including data and ECC). This would yield a DIMM pair having 256 megabytes of data storage capacity. If a piggy-back board is used as in the 72 megabyte DIMM embodiment described above, the 64 megabyte SDRAM chips can be used to implement a 256 megabyte data and 32 megabyte ECC DIMM and a 512 megabyte data, 64 megabyte ECC DIMM pair.

[0092] In the preferred embodiment described, a piggy-back board is used to allow the DIMM to accommodate 36 SDRAMs for the data memory. A person skilled in the art will recognize that chip stacking techniques may also be used to accommodate 36 SDRAM chips. If chip stacking techniques are used, the piggy-board may be eliminated.

[0093] Alternatively, 4 megabit (i.e., 1M x 1) SDRAM chips can be combined to produce DIMMs with lower storage capacity, or the above-described stacking and /or piggy-back techniques can be used for higher storage capacity.

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Claims

1. A dual in-line memory module, short:DIMM, comprising:

   a circuit board (103);
   first memory means (104), mounted on said circuit board, for storing data; and
   second memory means (106), mounted on said circuit board, for storing directory information corresponding to at least a portion of said data.

2. The DIMM of claim 1, comprising:
   further means (108) for permitting said first memory means and said second memory means to be accessed separately.

3. The DIMM of claim 2, wherein said further means comprises a connector (108), said connector having a plurality of pads, said pads including

   a first group of address pads (118),
   a second group of address pads (122),
   a first group of data pads (120), and
   a second group of data pads (124).

4. The DIMM of claim 3, wherein said plurality of pads has the following arrangement:

   said first group of data pads and said first group of address pads are electrically coupled to said first memory means; and
   said second group of data pads and said second group of address pads are electrically coupled to said second memory means,
   wherein said arrangement permits independent addressing of said first and second memory means.

5. The DIMM of claim 4, wherein said plurality of pads further comprises separate control pads for said first and second memory means.

6. The DIMM of claim 4, wherein said connector is an edge connector having two sides and at least 122 pads per side, said first group of address pads includes at least 12 pads, said second group of address pads includes at least 12 pads, said first group of data pads includes at least 72 pads, and said second group of data pads includes at least 16 pads.

7. The DIMM of any of the preceding claims, wherein said first memory means and said second memory means each comprise a plurality of dynamic random access memory (DRAM) chips.

8. The DIMM of any of the preceding claims, further comprising a phase locked loop clock driver coupled to said first and second memory means and a buffer for buffering address and control signals for said first memory means.

9. The DIMM of any of the preceding claims, wherein said first memory means is logically organized into memory blocks, and said second memory means is configured for storing information about where data stored in a group of said memory blocks is cached.

10. The DIMM of any of the preceding claims, wherein said first memory means is logically organized into memory blocks, and said second memory means is configured for storing access rights for the data stored in a group of said memory blocks.

11. The DIMM of any of the preceding claims, wherein said first memory means is logically organized into memory blocks, and said second memory means is configured for storing cache state information about data stored in a group of said memory blocks.

12. The DIMM of claim 4, wherein said first memory means and said second memory means each comprise a plurality of synchronous dynamic random access memory (SDRAM) chips.

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13. The DIMM of claim 12, wherein said first memory means is divided into a first memory bank portion of SDRAM chips and a second memory bank portion of SDRAM chips.

14. The DIMM of claim 13, wherein said first memory bank portion and said second memory bank portion each comprises at least nine SDRAM chips, each of said at least nine SDRAM chips being two megabits deep and eight bits wide, and wherein said second memory means comprises at least one one megabit deep by sixteen bit wide SDRAM chip.

15. The DIMM of claim 13, wherein said first memory bank portion and said second memory bank portion each comprise at least eighteen SDRAM chips, each of said at least eighteen SDRAM chips being four megabits deep and four bits wide, and wherein said second memory means comprises at least two two megabit deep by eight bit wide SDRAM chips.

16. The DIMM of claim 15, wherein said printed circuit board comprises a first circuit board supporting a second circuit board in a parallel, piggy back configuration.

17. The DIMM of claim 13, wherein said first memory bank portion and said second memory bank portion each comprise at least eighteen SDRAM chips, each of said at least eighteen SDRAM chips being sixteen megabits deep and four bits wide; wherein said first group of address pads includes at least 14 pads; and wherein said second memory means comprises at least two eight megabit deep by eight bit wide SDRAM chips.

Patentansprüche

1. Dual-In-Line Speichermodul (kurz: DIMM) mit

   einer Schaltungsplatine (103),

   einer ersten Speichereinrichtung (104), die auf der Schaltungsplatine zum Speichern von Daten befestigt ist, und

   einer zweiten Speichereinrichtung (106), die auf der Schaltungsplatine zum Speichern von Verzeichnisinformationen, die mindestens einem Teil der Daten entsprechen, befestigt ist.

2. DIMM nach Anspruch 1, dadurch gekennzeichnet, daß zusätzliche Einrichtungen (108) vorgesehen sind, um einen separaten Zugriff auf die erste Speichereinrichtung und die zweite Speichereinrichtung zu ermöglichen.

3. DIMM nach Anspruch 2, dadurch gekennzeichnet, daß die zusätzlichen Einrichtungen einen Stecker (108) aufweisen, wobei der Stecker mehrere Anschlüsse besitzt, die folgendes aufweisen:

   eine erste Gruppe von Adressanschlüssen (118),

   eine zweite Gruppe von Adressanschlüssen (122),

   eine erste Gruppe von Datenanschlüssen (120) und

   eine zweite Gruppe von Datenanschlüssen (124).

4. DIMM nach Anspruch 3, dadurch gekennzeichnet, daß die mehreren Anschlüsse folgende Anordnung aufweisen:

   Die erste Gruppe von Datenanschlüssen und die erste Gruppe von Adressanschlüssen sind elektrisch mit der ersten Speichereinrichtung verbunden und

   die zweite Gruppe von Datenanschlüssen und die zweite Gruppe von Adressanschlüssen sind elektrisch mit der zweiten Speichereinrichtung verbunden,

   wobei die Anordnung eine unabhängige Adressierung der ersten und zweiten Speicheranordnung zuläßt.

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5. DIMM nach Anspruch 4, dadurch gekennzeichnet, daß die mehreren Anschlüsse zusätzlich separate Steueranschlüsse für die erste und zweite Speichereinrichtung aufweisen.

6. DIMM nach Anspruch 4, dadurch gekennzeichnet, daß der Stecker eine Steckerleiste ist, die zwei Seiten und mindestens 122 Anschlüsse pro Seite aufweist wobei die erste Gruppe von Adressanschlüssen mindestens zwölf Anschlüsse, die zweite Gruppe von Adressanschlüssen mindestens zwölf Anschlüsse, die erste Gruppe von Datenanschlüssen wenigstens 72 Anschlüsse und die zweite Gruppe von Datenanschlüssen mindestens 16 Anschlüsse aufweist.

7. DIMM nach einem der vorangehenden Ansprüche, dadurch gekennzeichnet, daß die erste Speichereinrichtung und die zweite Speichereinrichtung jeweils mehrere dynamische Direktzugriffsspeicher (DRAM) Chips aufweisen.

8. DIMM nach einem der vorangehenden Ansprüche, dadurch gekennzeichnet, daß ein phasenfester Schleifen-Zeitgeber (phase locked loop clock driver) mit der ersten und zweiten Speichereinrichtung gekoppelt ist und ein Puffer zur Pufferung von Adress- und Steuersignalen für die erste Speichereinrichtung vorgesehen ist.

9. DIMM nach einem der vorangehenden Ansprüche, dadurch gekennzeichnet, daß die erste Speichereinrichtung logisch in Speicherblöcke unterteilt ist und daß die zweite Speichereinrichtung konfiguriert ist, um Informationen darüber zu speichern, wo die Daten in einer Gruppe von Speicherblöcken in einem Cachespeicher gespeichert sind.

10. DIMM nach einem der vorangehenden Ansprüche, dadurch gekennzeichnet, daß die erste Speichereinrichtung logisch in Speicherblöcke organisiert ist und daß die zweite Speichereinrichtung zur Speicherung von Zugriffsrechten für die in einer Gruppe von Speicherblöcken gespeicherten Daten ausgelegt ist.

11. DIMM nach einem der vorangehenden Ansprüche, dadurch gekennzeichnet, daß die erste Speichereinrichtung logisch in Speicherblöcke unterteilt ist und daß die zweite Speichereinrichtung konfiguriert ist, um Cache-Zustandsinformationen über die in einer Gruppe von Speicherblöcken gespeicherten Daten zu speichern.

12. DIMM nach Anspruch 4, dadurch gekennzeichnet, daß die erste Speichereinrichtung und die zweite Speichereinrichtung jeweils mehrere synchrone dynamische Direktzugriffsspeicher (SDRAM) Chips aufweisen.

13. DIMM nach Anspruch 12, dadurch gekennzeichnet, daß die erste Speichereinrichtung in einen ersten Speicherbankabschnitt von SDRAM Chips und in einen zweiten Speicherbankabschnitt von SDRAM Chips unterteilt ist.

14. DIMM nach Anspruch 13, dadurch gekennzeichnet, daß der erste Speicherbankabschnitt und der zweite Speicherbankabschnitt jeweils mindestens 9 SDRAM Chips besitzen, wobei jeder von den mindestens 9 SDRAM Chips zwei Megabit tief und acht Bit breit ist, und daß die zweite Speichereinrichtung mindestens einen ein Megabit tiefen und 16 Bit breiten SDRAM Chip besitzt.

15. DIMM nach Anspruch 13, dadurch gekennzeichnet, daß der erste Speicherbankabschnitt und der zweite Speicherbankabschnitt jeweils mindestens 18 SDRAM Chips aufweisen, wobei jeder von den mindestens 18 SDRAM Chips vier Megabit tief und vier Bit breit ist, und daß die zweite Speichereinrichtung mindestens zwei zwei Megabit tiefe und acht Bit breite SDRAM Chips aufweist.

16. DIMM nach Anspruch 15, dadurch gekennzeichnet, daß die gedruckte Schaltungsplatine eine erste Schaltungsplatine aufweist, die eine zweite Schaltungsplatine in einer parallelen, Hucke-Pack-Anordnung aufweist.

17. DIMM nach Anspruch 13, dadurch gekennzeichnet, daß der erste Speicherbankabschnitt und der zweite Speicherbankabschnitt jeweils mindestens 18 SDRAM Chips aufweisen, wobei jeder von den mindestens 18 SDRAM Chips 16 Megabit tief und 4 Bit breit ist, daß die erste Gruppe von Adressanschlüssen mindestens 14 Anschlüsse aufweist und daß die zweite Speichereinrichtung mindestens zwei acht Megabit tiefe und acht Bit breite SDRAM Chips aufweist.

Revendications

1. Module de mémoires à double rangée de broches (abrégé : DIMM) comprenant :

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une carte de circuit (103);
un premier moyen de mémoire (104), monté sur ladite carte de circuit, pour stocker des données ; et
un second moyen de mémoire (106), monté sur ladite carte de circuit, pour stocker des informations de répertoire correspondant à au moins une partie desdites données.

2. Module DIMM selon la revendication 1, comprenant :
un autre moyen (108) pour permettre d'accéder séparément audit premier moyen de mémoire et audit second moyen de mémoire.

3. Module DIMM selon la revendication 2, dans lequel ledit autre moyen comprend un connecteur (108), ledit connecteur ayant une pluralité de plages, lesdites plages comprenant :

un premier groupe de plages d'adresse (118),
un second groupe de plages d'adresse (122),
un premier groupe de plages de données (120), et
un second groupe de plages de données (124).

4. Module DIMM selon la revendication 3, dans lequel ladite pluralité de plages possède la disposition suivante :

ledit premier groupe de plages de données et ledit premier groupe de plages d'adresse sont électriquement couplés audit premier moyen de mémoire ; et
ledit second groupe de plages de données et ledit second groupe de plages d'adresse sont électriquement couplés audit second moyen de mémoire,
dans lequel ladite disposition permet un adressage indépendant desdits premier et second moyens de mémoire.

5. Module DIMM selon la revendication 4, dans lequel ladite pluralité de plages comprend en outre des plages de commande séparées pour lesdits premier et second moyen de mémoire.

6. Module DIMM selon la revendication 4, dans lequel ledit connecteur est un connecteur de bord ayant deux côtés et au moins 122 plages par côté, ledit premier groupe de plages d'adresse comprend au moins 12 plages, ledit second groupe de plages d'adresse comprend au moins 12 plages, ledit premier groupe de plages de données comprend au moins 72 plages, et ledit second groupe de plages de données comprend au moins 16 plages.

7. Module DIMM selon l'une quelconque des revendications précédentes, dans lequel ledit premier moyen de mémoire et ledit second moyen de mémoire comprennent chacun une pluralité de puces de mémoire vive (DRAM).

8. Module DIMM selon l'une quelconque des revendications précédentes, comprenant en outre un pilote d'horloge à verrouillage de phase couplé audits premier et second moyens de mémoire et un tampon pour tamponner des signaux d'adresse et de commande pour ledit premier moyen de mémoire.

9. Module DIMM selon l'une quelconque des revendications précédentes dans lequel ledit premier moyen de mémoire est logiquement organisé en bloc de mémoire, et ledit second moyen de mémoire est configuré pour stocker des informations concernant l'emplacement où sont mises en antémémoire les données stockées dans un groupe desdits blocs de mémoire.

10. Module DIMM selon l'une quelconque des revendications précédentes, dans lequel ledit premier moyen de mémoire est logiquement organisé en blocs de mémoire, et ledit second moyen de mémoire est configuré pour stocker des droits d'accès pour les données stockées dans un groupe desdits blocs de mémoire.

11. Module DIMM selon l'une quelconque des revendications précédentes, dans lequel ledit premier moyen de mémoire est logiquement organisé en blocs de mémoire, et ledit second moyen de mémoire est configuré pour stocker des informations d'état d'antémémoire concernant des données stockées dans un groupe desdits blocs de mémoire.

12. Module DIMM selon la revendication 4, dans lequel ledit premier moyen de mémoire et ledit second moyen de mémoire comprennent chacun une pluralité de puces de mémoire vive (SDRAM).

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13. Module DIMM selon la revendication 12, dans lequel ledit premier moyen de mémoire est divisé en une première partie de banque de mémoire de puces SDRAM et une seconde partie de banque de mémoire de puces SDRAM.

14. Module DIMM selon la revendication 13, dans lequel ladite première partie de banque de mémoire et ladite seconde partie de banque de mémoire comprennent chacun au moins neuf puces SDRAM, chacune desdites neuf puces SDRAM étant profonde de deux mégabits et large de huit bits, et dans lequel ledit second moyen de mémoire comprend au moins une puce profonde de un mégabit par 16 bits de large.

15. Module DIMM selon la revendication 13, dans lequel ladite première partie de banque de mémoire et ladite seconde partie de banque de mémoire comprennent chacune au moins dix-huit puces SDRAM, chacune des au moins dix-huit puces SDRAM étant profonde de quatre mégabits et large de quatre bits, et dans lequel ledit second moyen de mémoire comprend au moins deux puces profonde de deux mégabits par huit bits de large SDRAM.

16. Module DIMM selon la revendication 15, dans lequel ladite carte de circuit imprimé comprend une configuration rapportée d'une première carte de circuit supportant une seconde carte de circuit en parallèle.

17. Module DIMM selon la revendication 13, dans lequel ladite première partie de banque de mémoire et ladite seconde partie de banque de mémoire comprennent chacune au moins dix-huit puces SDRAM, chacune desdites au moins dix-huit puces SDRAM étant profonde de seize mégabits et large de quatre bits ; dans lequel ledit premier groupe de plages d'adresse comprend au moins 14 plages ; et dans lequel ledit second moyen de mémoire comprend au moins deux puces SDRAM profonde de huit mégabits par 8 bits de large.

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FIG. 1

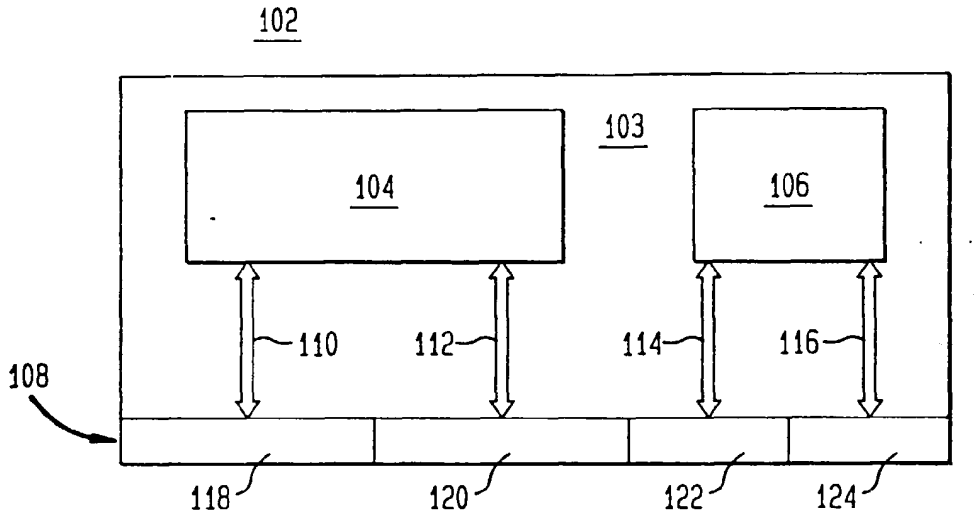
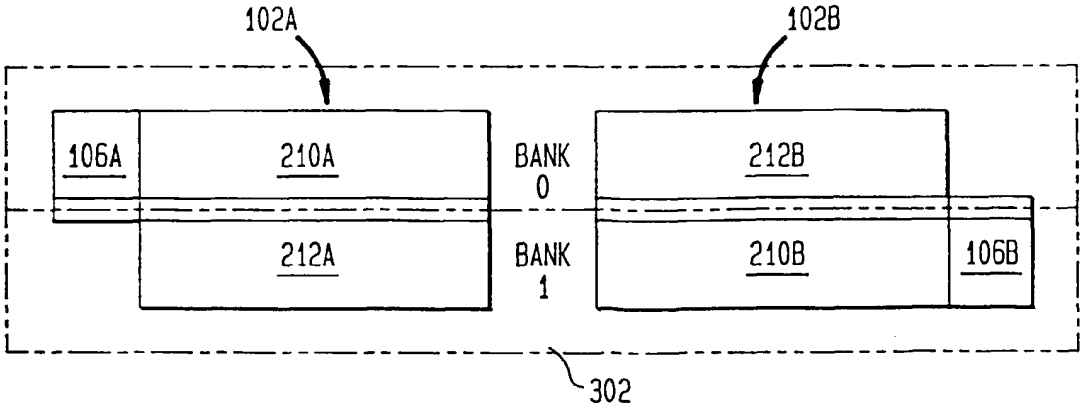
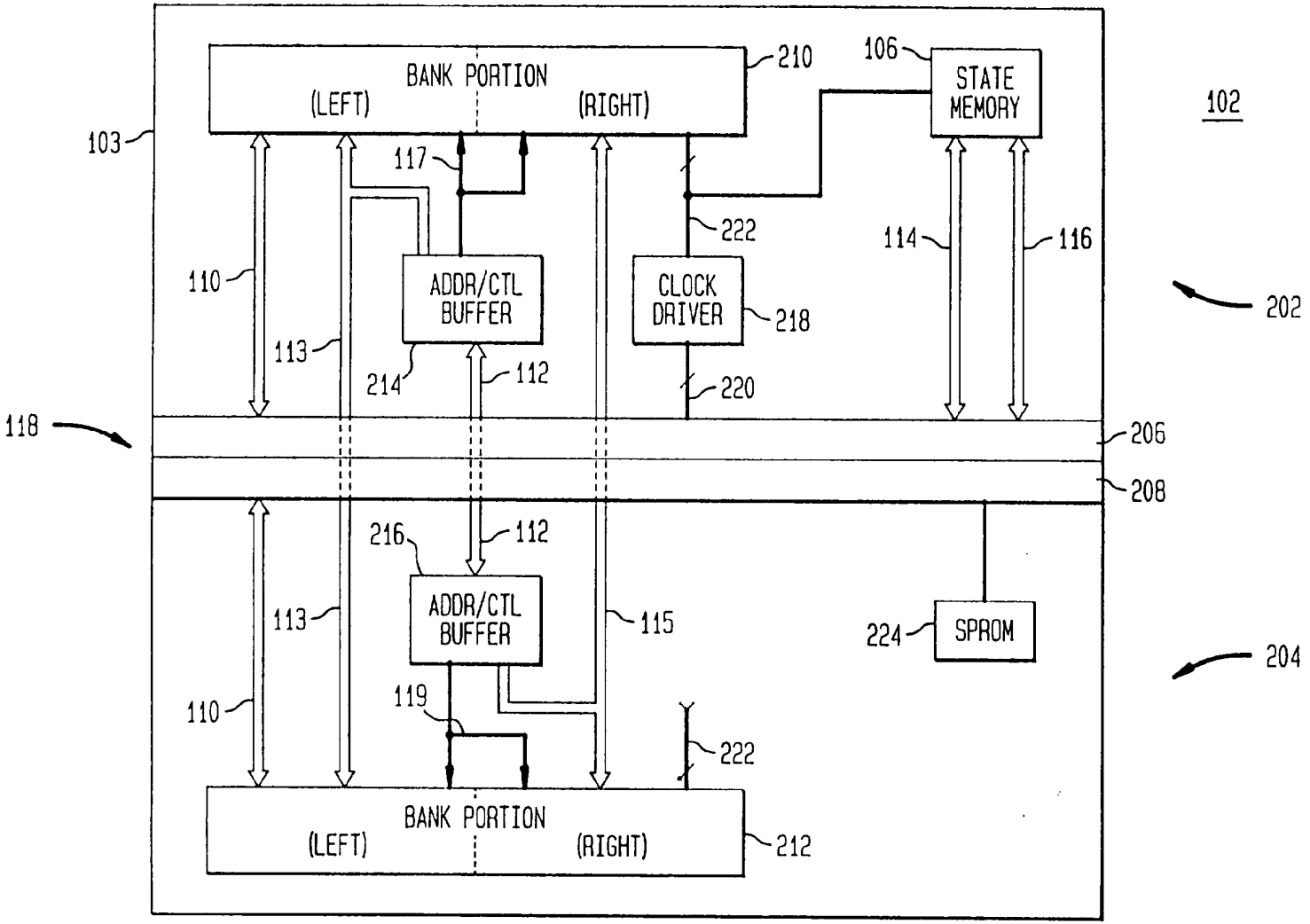


FIG. 3



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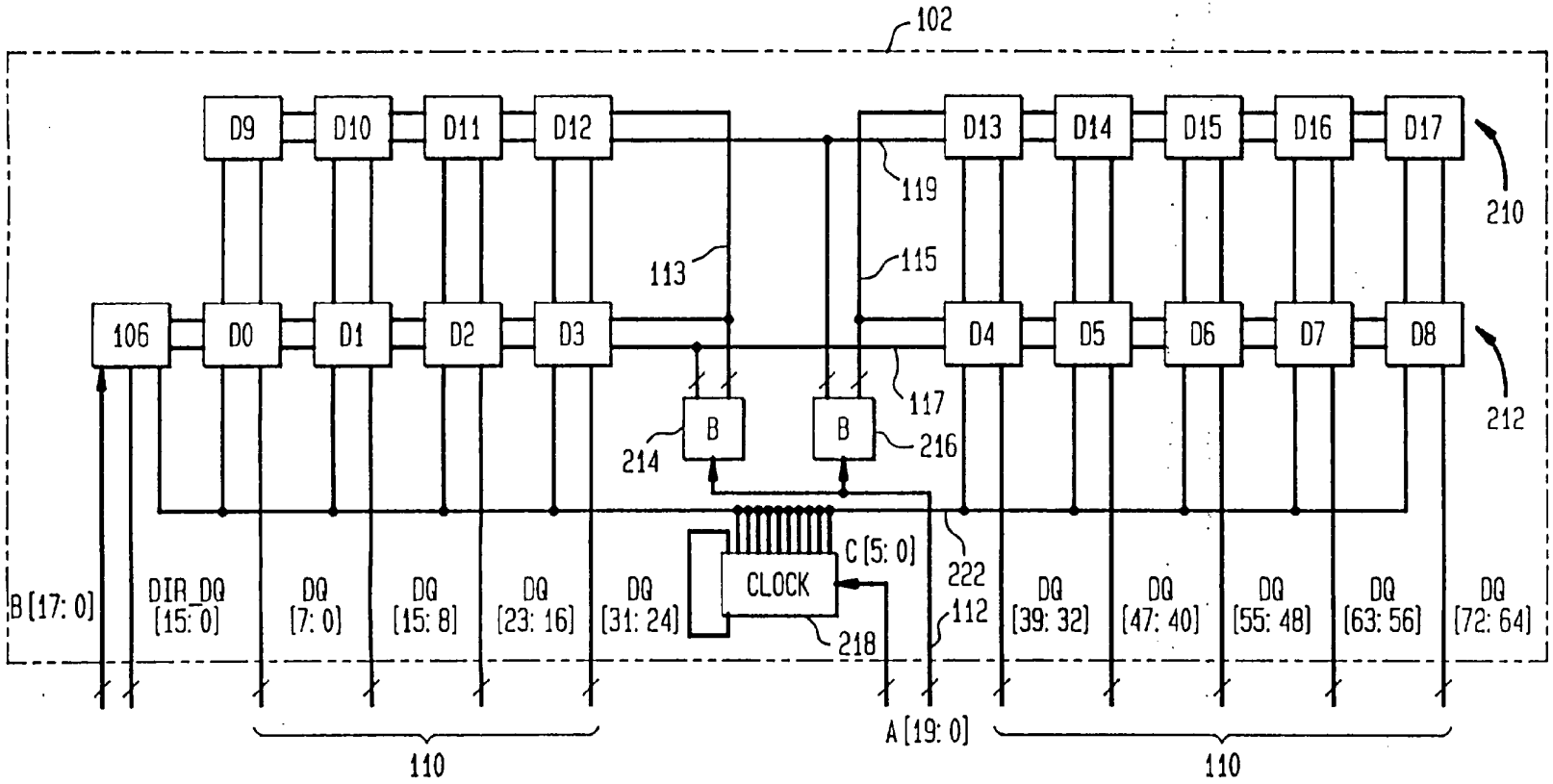
FIG. 2



EP 0 744 748 B1

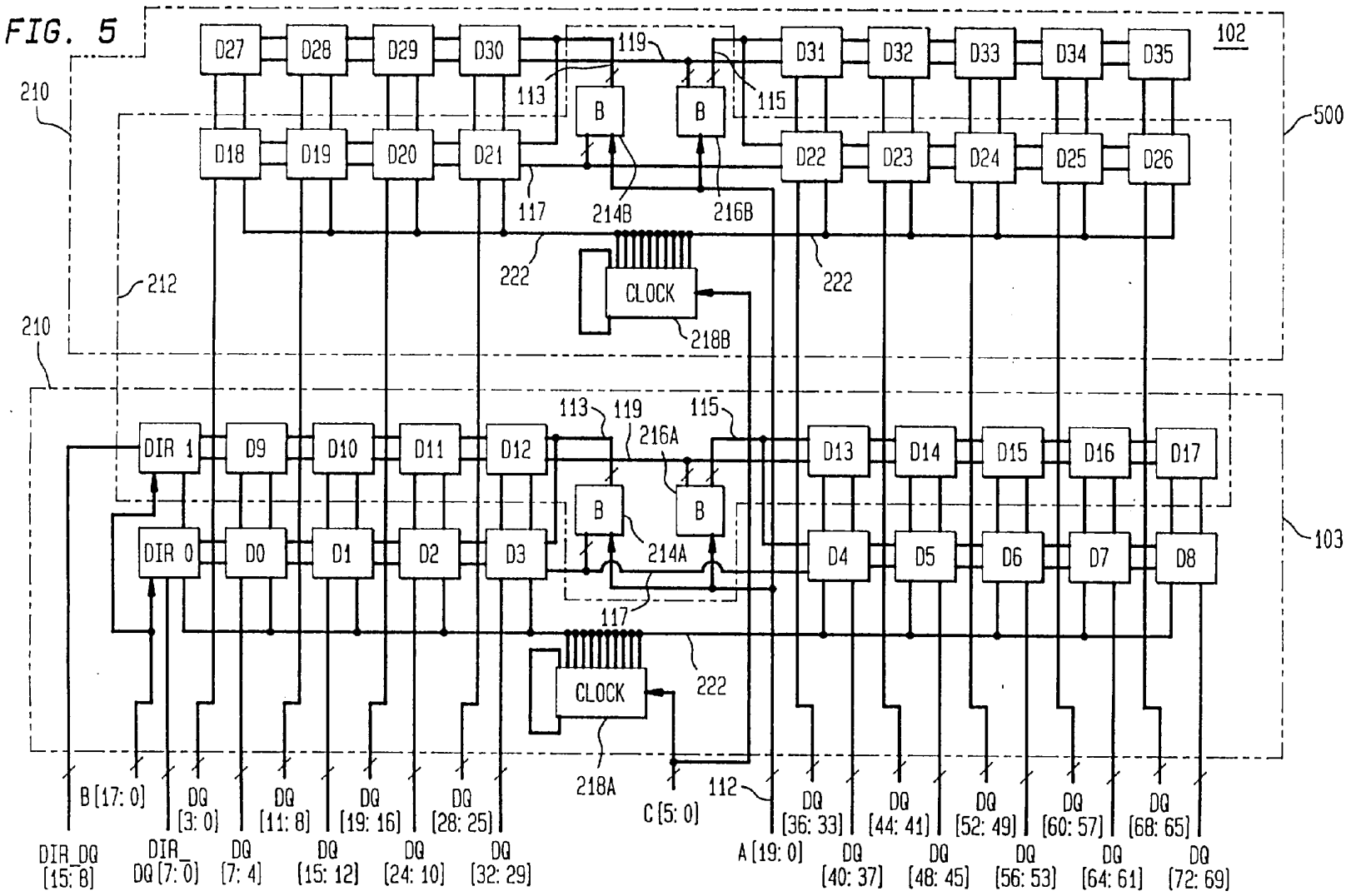
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FIG. 4



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FIG. 5



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FIG. 6A

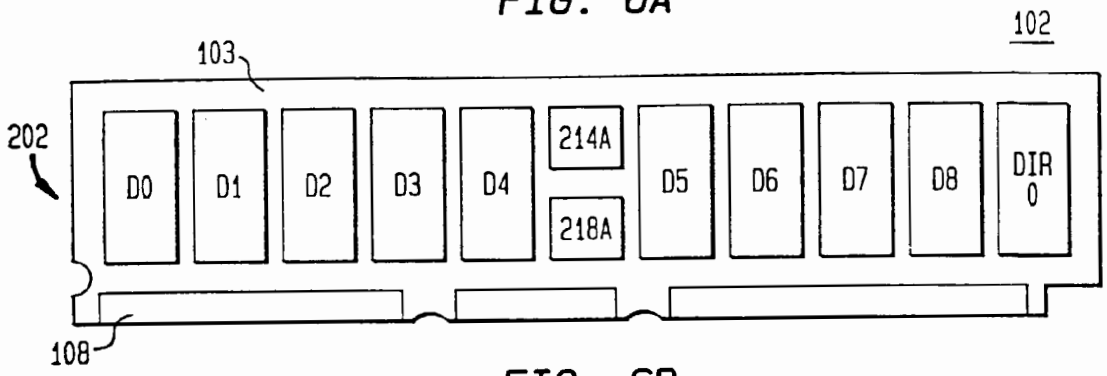


FIG. 6B

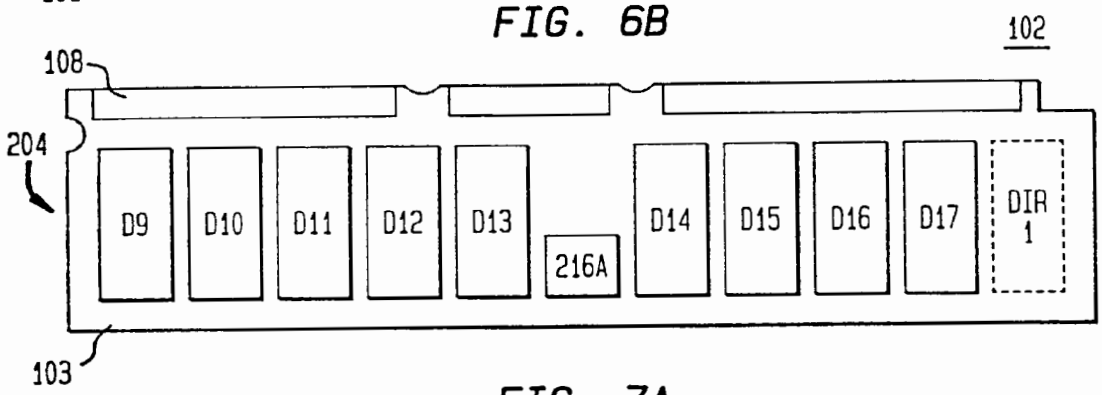


FIG. 7A

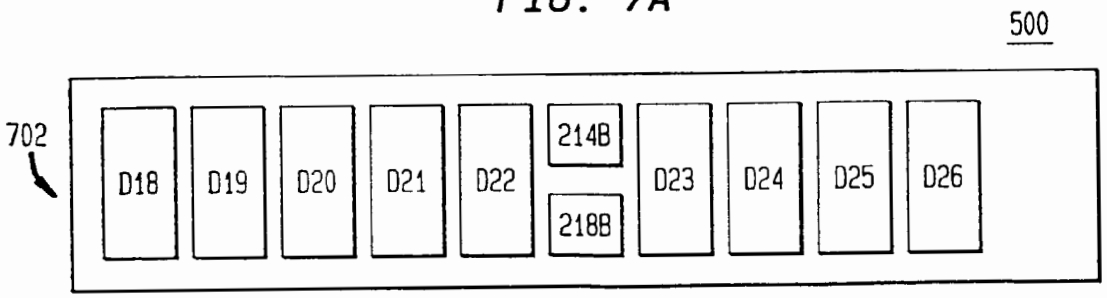
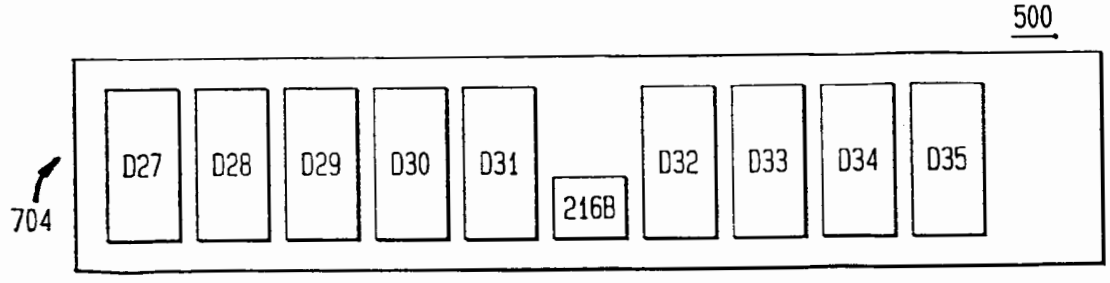


FIG. 7B



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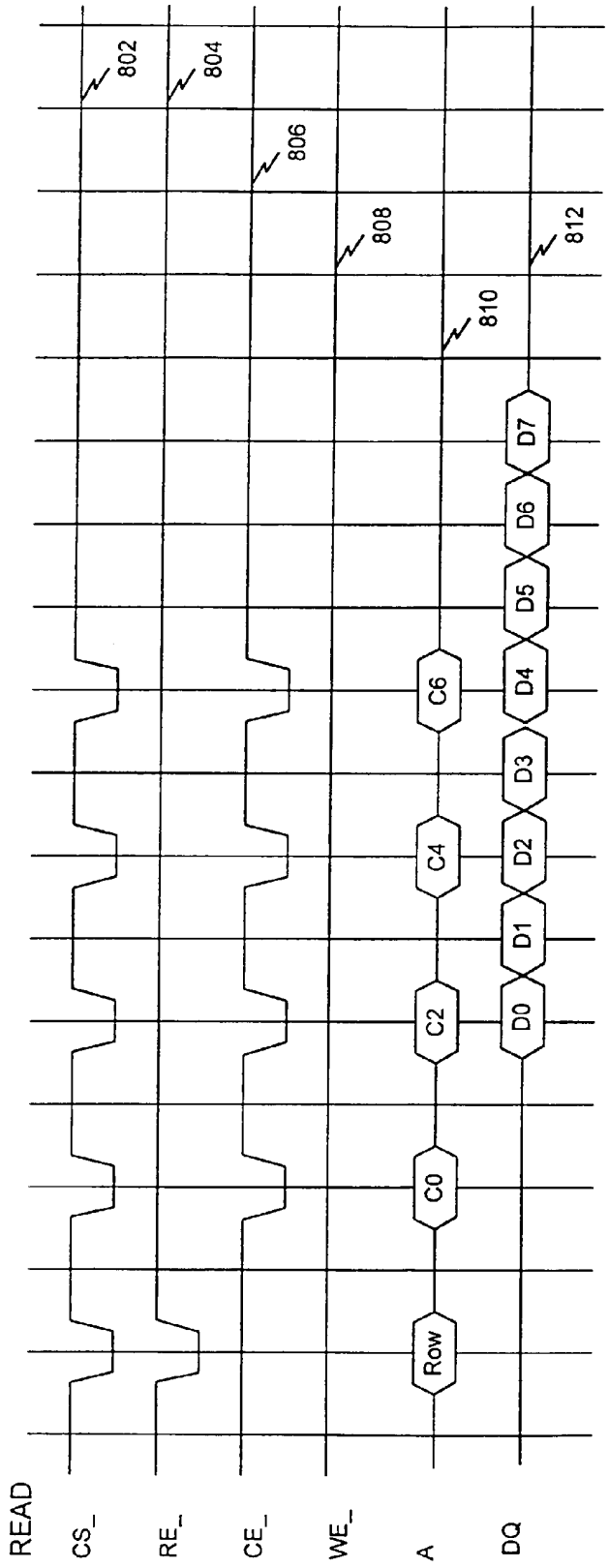


FIG. 8

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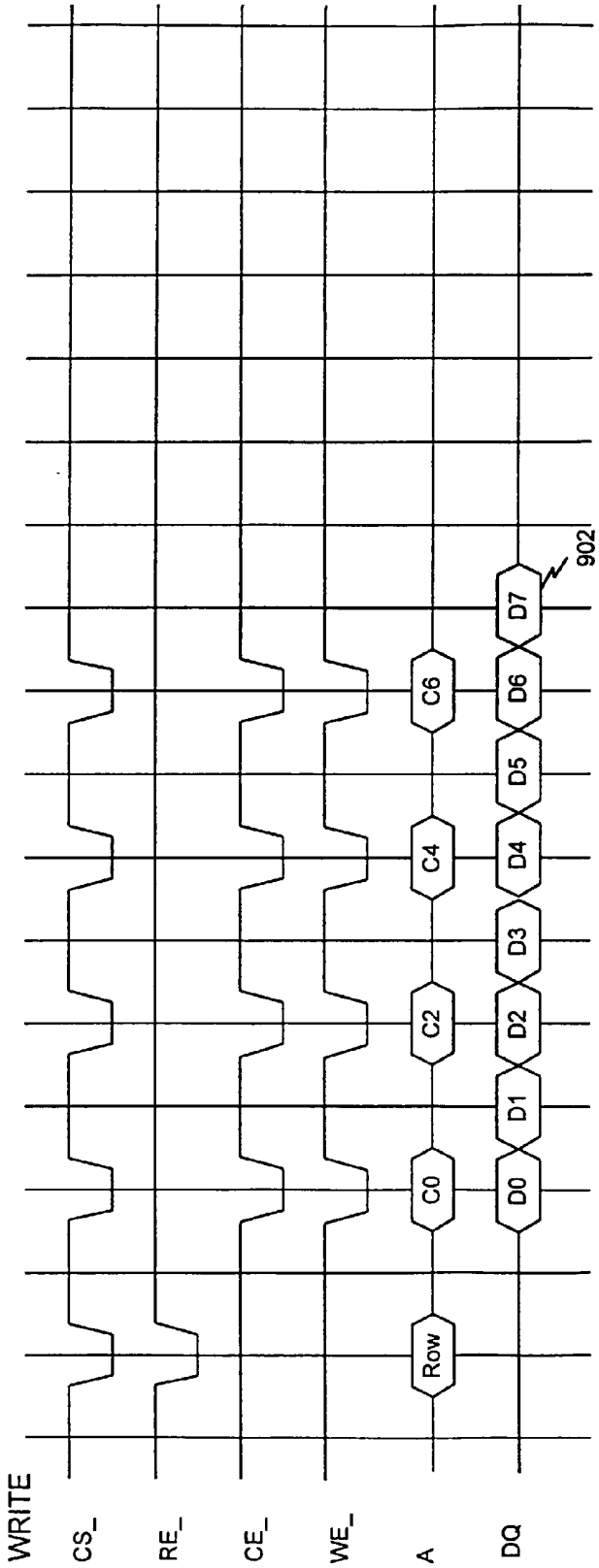


FIG. 9

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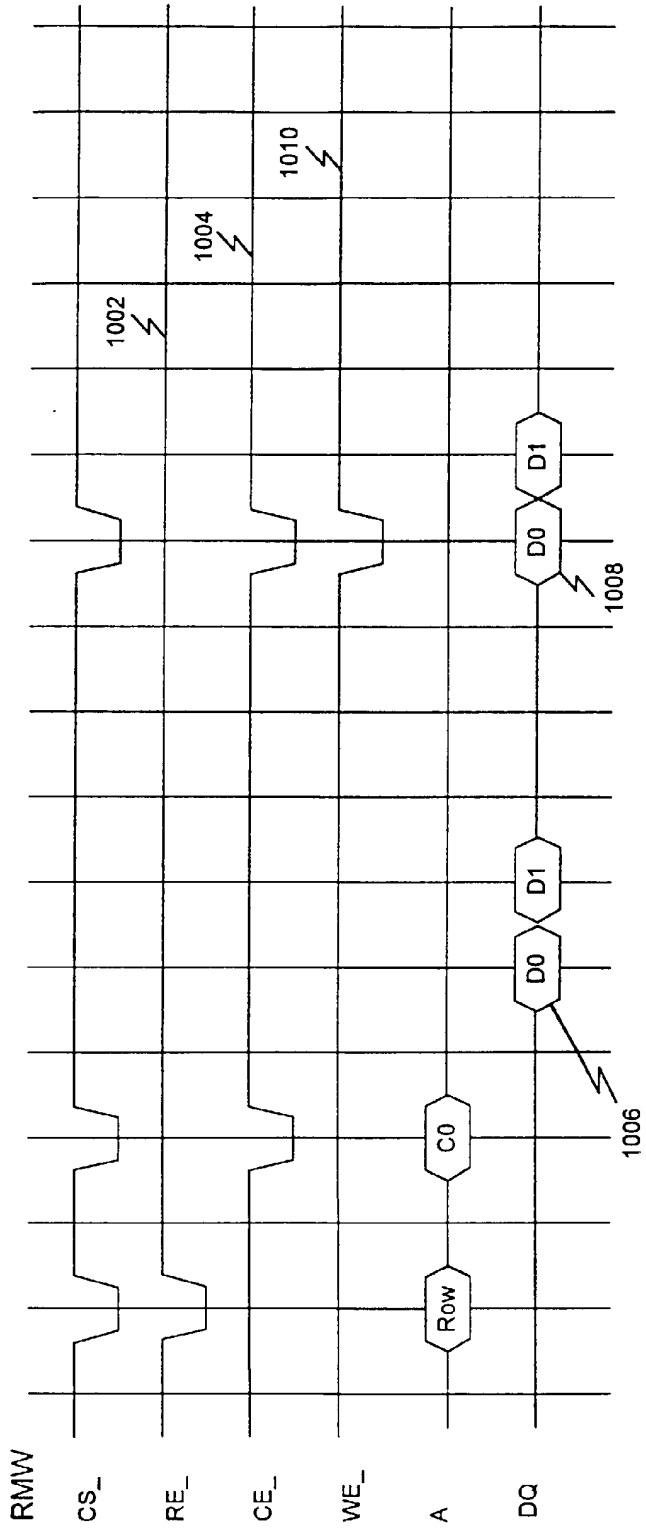


FIG. 10

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Class 1 Directory Access for Reads

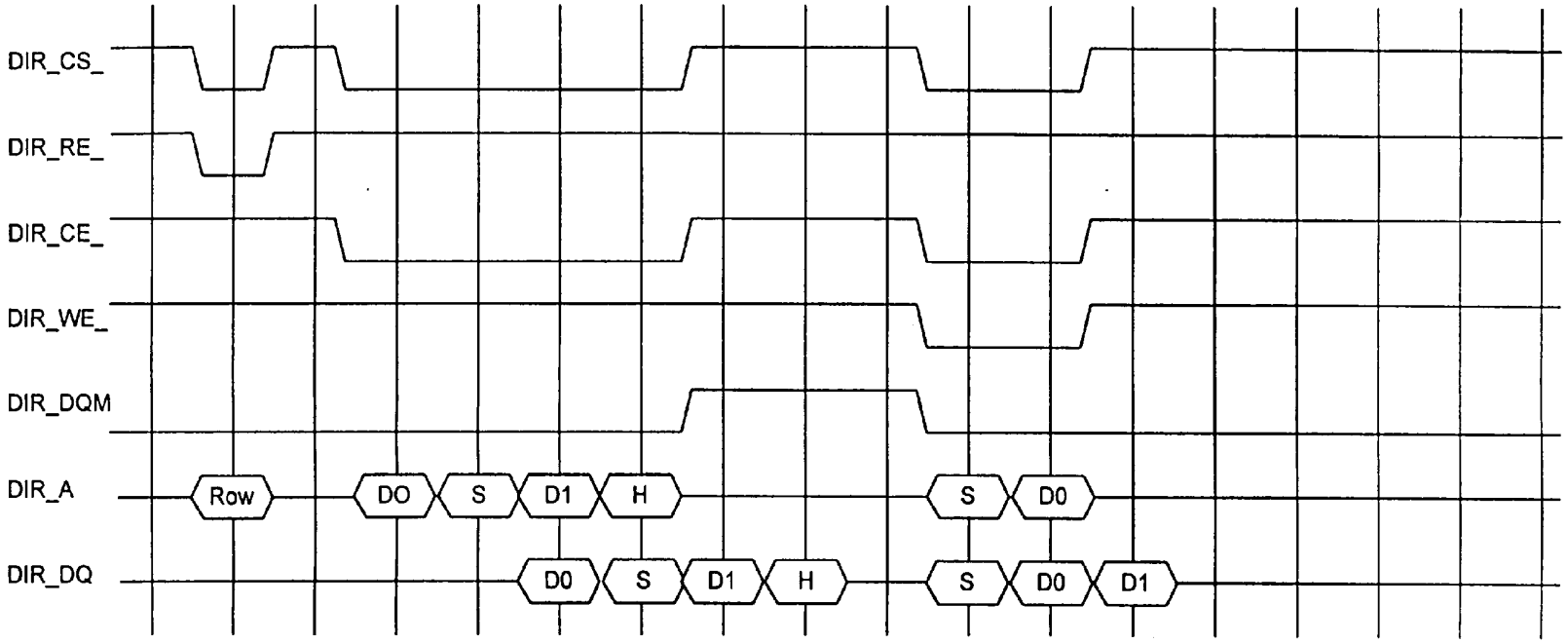


FIG. 11

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Class 2 Directory Access for Writes

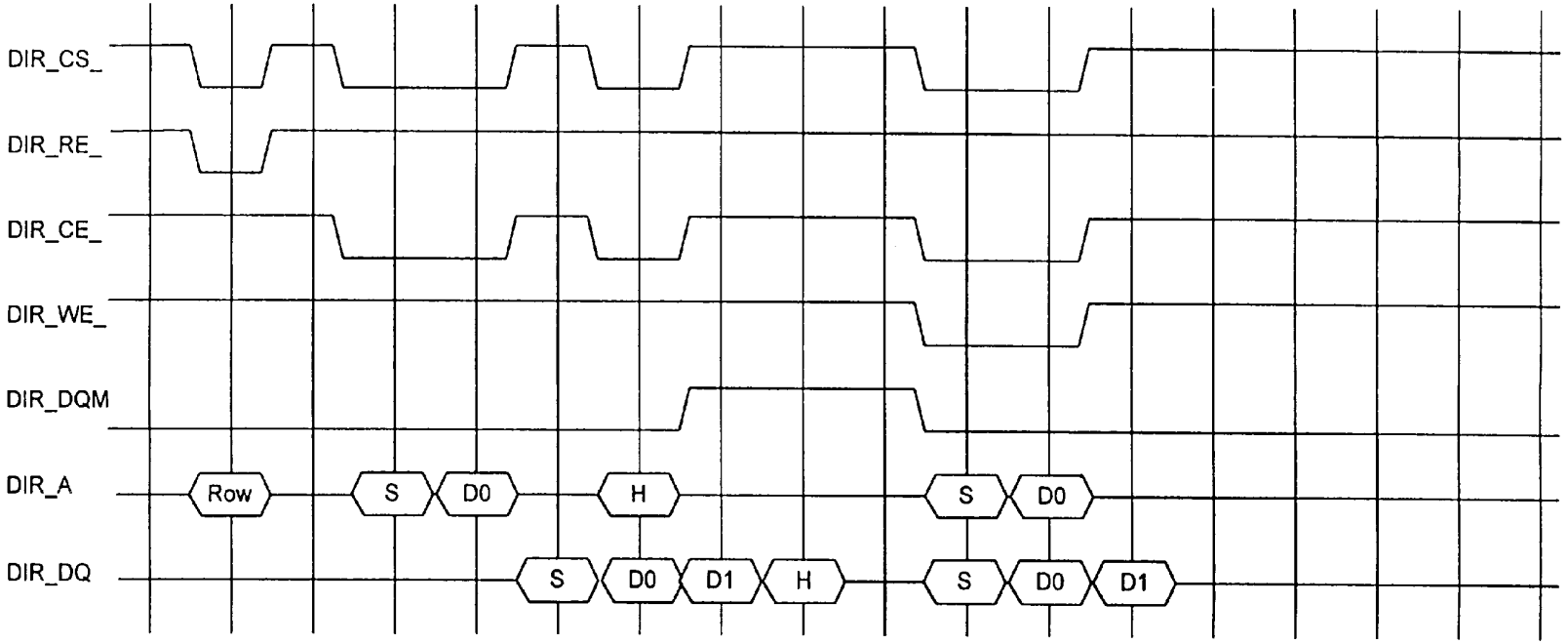


FIG. 12

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Class 3 Directory Access for Revisions

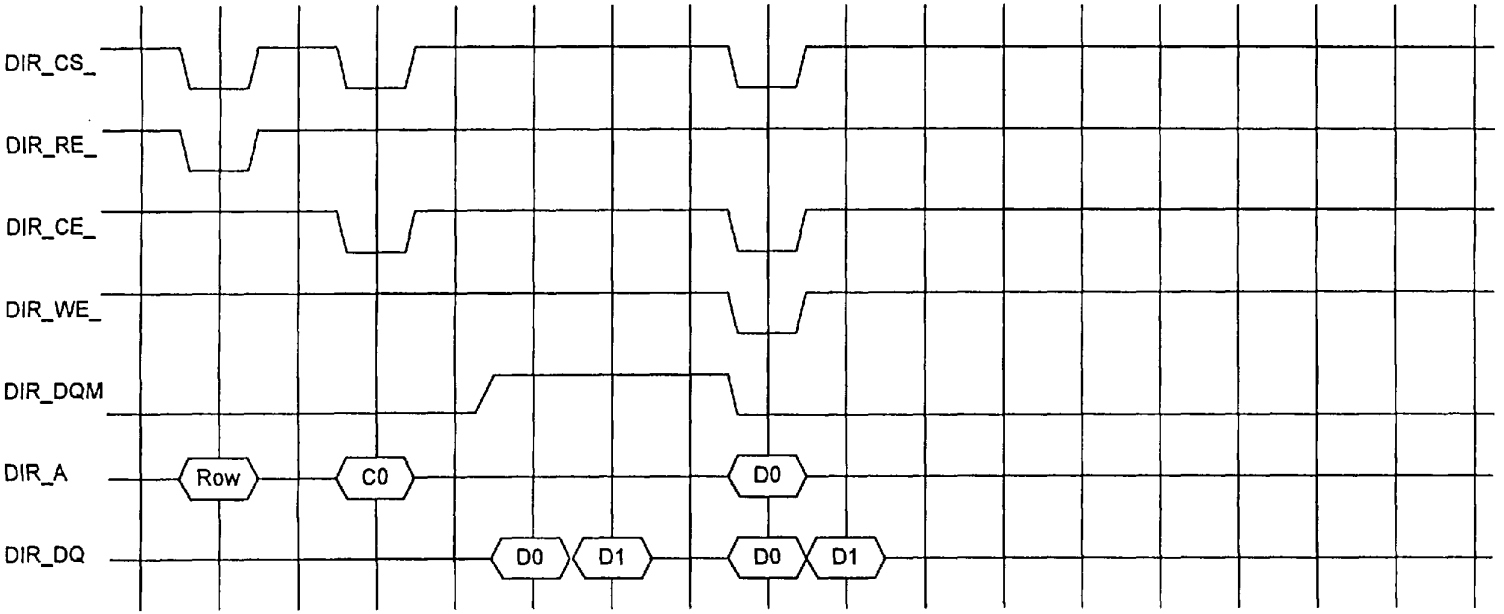
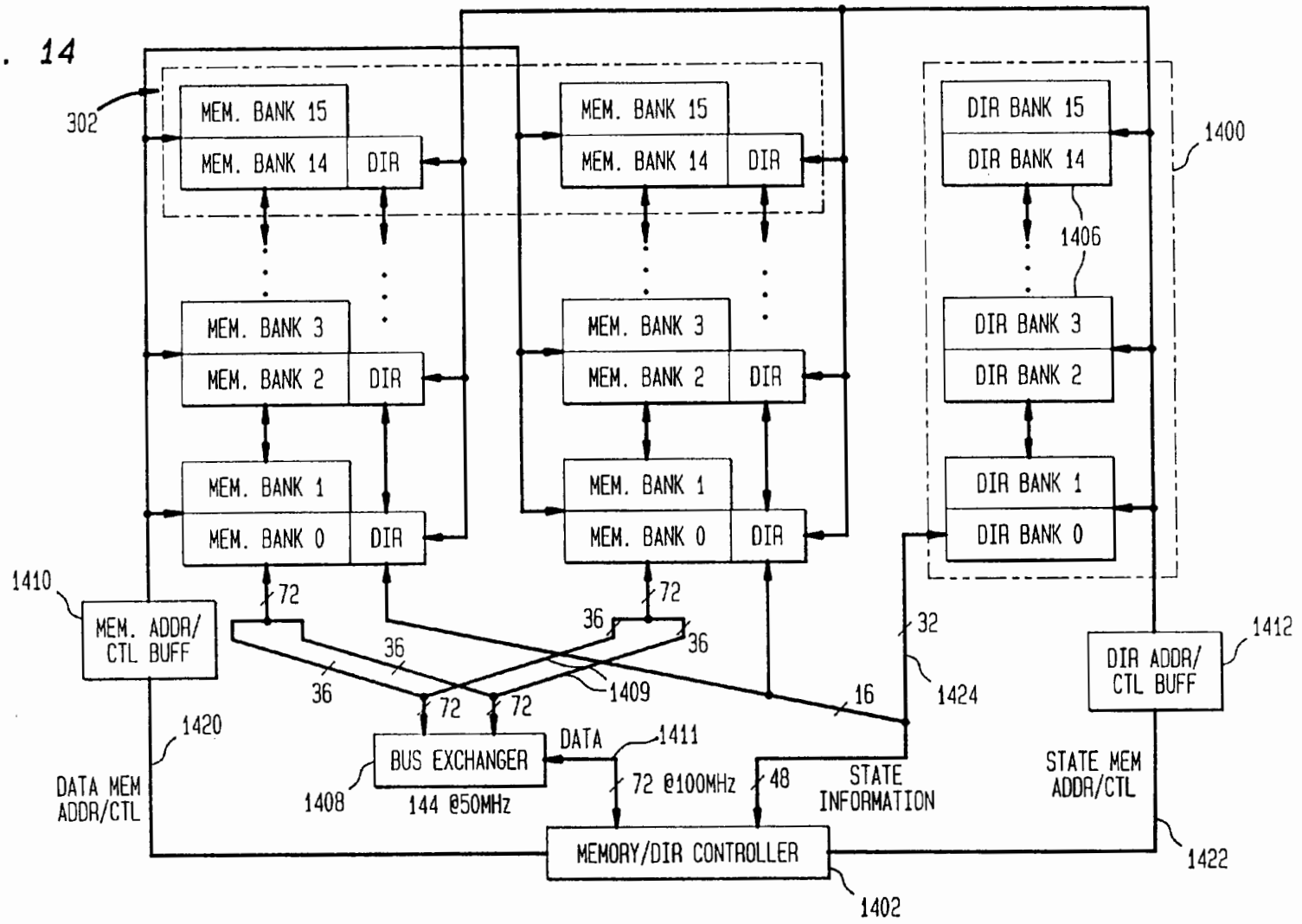


FIG. 13

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FIG. 14



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PAD	NAME	PAD	NAME	PAD	NAME	PAD	NAME	PAD	NAME	PAD	NAME
1	DIR_DQ13	42	DQ49	85	DQ30	131	DIR_A0	174	V3	218	DQ23
2	D	43	DQ50	86	GND	132	V3	175	A11	219	GND
3	DUR_DQ15	44	GND	88	DQ24	133	DIR_A10	177	GND	220	DQ17
4	DIR_DQ11	45	DQ45	89	V3	134	DIR_RE_	178	A8	221	DQ19
5	V3	46	DQ46	90	DQ27	135	GND	179	A6	222	V3
6	DIR_DQ8	47	V3	91	DQ20	136	DIR_DQM	180	V3	224	DQ12
7	DIR_A3	48	DQ41	92	GND	137	DIR_A2	181	CS0_	225	GND
8	GND	49	DQ42	93	GND	138	V3	182	CS1_	226	GND
9	DIR_A11	50	GND	94	DQ22	139	DIR_DQ0	183	GND	227	DQ14
10	DIR_CS_	51	DQ43	95	V3	140	DIR_DQ2	184	CE_	228	V3
11	V3	52	CKE0	96	V3	141	GND	185	P_CLK	229	V3
12	DIR_WE_	53	V3	97	DQ16	142	DIR_DQ5	186	V3	230	DQ8
13	DIR_CE_	54	A10	98	GND	143	DIR_DQ6	187	A5	231	GND
14	GND	55	A9	99	DQ18	144	V3	188	PLL_EN	232	DQ10
15	DIR_A4	56	GND	101	V3	145	DIR_A7	189	GND	234	V3
16	DIR_DQ1	57	A7	103	DQ13	146	DIR_A6	190	DQM	235	DQ4
17	V3	58	CKE1	104	GND	147	GND	191	A4	236	GND
18	DIR_DQ3	59	V3	105	GND	148	DIR_CKE	192	V3	237	GND
19	DIR_DQ4	60	TCLK	106	DQ15	149	DQ68	193	A1	238	DQ6
20	GND	61	PLL_CLR	107	V3	150	V3	194	A2	240	V3
21	DIR_DQ7	62	GND	108	V3	151	DQ71	195	GND	241	DQ1
22	DIR_A5	63	P_CLK_	109	DQ9	152	DQ64	196	DQ37	242	DQ3
23	V3	64	RE_	110	GND	153	GND	197	DQ38	243	GND
24	DIR_A8	65	V3	111	DQ11	154	DQ67	198	V3	244	GND
25	DIR_A9	66	TCLK_SEL	113	V3	155	DQ56	199	DQ32		
26	GND	67	WE_	114	DQ5	156	V3	200	DQ34		
27	DQ69	68	GND	115	GND	157	DQ62	201	GND		
28	DQ70	69	A3	116	GND	158	DQ60	202	GND		
29	V3	70	A0	117	DQ7	159	GND	204	V3		
30	DQ65	71	V3	118	DQ0	160	DQ59	205	V3		
31	DQ66	73	DQ36	119	V3	161	DQ52	206	DQ29		
32	GND	74	GND	120	DQ2	162	V3	207	GND		
33	DQ57	76	DQ39	122	GND	163	DQ55	208	DQ31		
34	DQ63	77	V3	123	GND	164	DQ48	210	V3		
35	V3	78	DQ33	124	DIR_DQ12	165	GND	211	DQ25		
36	DQ61	79	DQ35	125	DIR_DQ14	166	DQ51	212	DQ26		
37	DQ58	80	GND	126	V3	167	DQ44	213	GND		
38	GND	81	GND	127	DIR_DQ10	168	V3	214	GND		
39	DQ53	82	DQ28	128	DIR_DQ9	169	DQ47	215	DQ21		
40	DQ54	83	V3	129	GND	170	DQ40	216	V3		
41	V3	84	V3	130	DIR_A1	171	GND	217	V3		

FIG. 15

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PatentOrder

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Publication country: JAPAN
Publication type: APPLICATION
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Assignee: KABUSHIKI KAISHA TOSHIBA; TOSHIBA KK; TOSHIBA TEC CORP; TOSHIBA TEC KABUSHIKI KAISHA; 東芝テック株式会社; 株式会社東芝
Assignee[std]: TOSHIBA TEC KK
Inventor: 石原 守
Inventor[std]: ISHIHARA MAMORU
International class[8]: G11C11/401; G11C11/403
Title: DRAM MODE CONTROL CIRCUIT
DRAMモード制御回路

Abstract:

PROBLEM TO BE SOLVED: To control the starting of the self-refresh of a DRAM without receiving the supply of power from a battery, so that the backup time of the DRAM can be prolonged. SOLUTION: A DC-DC converter 11 stably outputs the third supply power of a voltage 3.3 V when the voltage of second supply power is not less than 3.3 V based on second supply power (5 V at normal time) which a 5 V power circuit 5 generates. A mode switch circuit 12 changes over a selector circuit 13 to a self-side according to that a voltage monitoring circuit 8 detects that the voltage of second supply power is lower than 4.7 V until the DC-DC converter 11 cannot generate third supply power at the voltage 3.3 V and performs a procedure for starting self-refresh.

【課題】 バッテリからの電力供給を受けることなしにＤＲＡＭのセルフリフレッシュの起動制御を行うことが でき、これによりＤＲＡＭのバックアップ時間の延長を図ることを可能とする。【解決手段】 ＤＣ－ＤＣコンバータ１１は、５Ｖ電源回路５が生成する第２供給電力（平常時５Ｖ）に基づき、この第２供給電力の電圧が３．３Ｖ以上であるならば電圧３．３Ｖの第３供給電力を安定的に出力する。モ ード切換回路１２は、第２供給電力の電圧が４．７Ｖよりも低下したことが電圧監視回路８により検知されたこ とに応じて、それからＤＣ－ＤＣコンバータ１１が第３供給電力を電圧３．３Ｖで生成できなくなるまでの間 に、セレクタ回路１３を自己側に切換えた上でＤＲＡＭ２にセルフリフレッシュを起動させるための手順を実行 する。

Description:

[０００１] [発明の属する技術分野]本発明は、外部からのリフレッシュ制御を受ける第１モードとリフレッシュ動作を自立的に行う第２モードとを有

[0001] [TECHNICAL FIELD OF THE INVENTION The present invention, DRAM mode to switch mode and second mode of the DRAM having the

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したＤＲＡＭのモード切換えを行うＤＲＡＭモード制御回路に関する。

[０００２] [従来の技術]ＤＲＡＭは、データを保持しておくためにリフレッシュを行うことが必要である。通常、ＤＲＡＭのリフレッシュは、アクセスを行う状態ではアクセスを行う側からの制御により、例えばＣＡＳビフォアＲＡＳリフレッシュが行われる。

[０００３]ところでこのような外部制御によるＣＡＳビフォアＲＡＳリフレッシュなどのリフレッシュ動作では、ＤＲＡＭにおける消費電流が比較的大きい。このため、アクセスを行わない状態でＣＡＳビフォアＲＡＳリフレッシュを行うことは、消費電流の無駄が多い。

[０００４]そこでこのようなアクセスを行わない状態でのリフレッシュのために、セルフリフレッシュ機能を有したＤＲＡＭが一般的である。セルフリフレッシュ機能とは、外部からセルフリフレッシュの起動が指定されてからセルフリフレッシュの停止が指定されるまでの間は、ＤＲＡＭが自立的にリフレッシュ動作を行うものである。

[０００５]そこで、停電時などにＤＲＡＭをバッテリバックアップするような場合には、バックアップ時間の延長を図るべくＤＲＡＭにセルフリフレッシュを行わせる技術が例えば特開平7-45066号公報などにより周知である。

[０００６] [発明が解決しようとする課題]ところが上記特開平7-45066号公報の技術では、メイン電源がオフとなった後にＤＲＡＭにセルフリフレッシュの起動を指示するために、そのセルフリフレッシュの起動指示を行うための制御回路（信号発生回路５）はバッテリバックアップしておく構成をとっている。

[０００７]このため、せっかくＤＲＡＭでの消費電流を低減しているのにも拘わらず、制御回路にてバックアップ用のバッテリからの電流消費が発生しているのであり、効率良く消費電流を低減できておらず、バックアップ時間の短縮を招いていた。

refresh operation is performed autonomously under the control the first mode and external refresh on the control circuit.

[0002] [ART] DRAM, the refresh should be performed in order to keep the data. Typically, DRAM refresh is controlled by the state from doing the access to gain access, for example, CAS before RAS refresh is performed.

[0003] In CAS before RAS refresh refresh operations, such as by the way, this kind of external control, power consumption is relatively high in the DRAM. Thus, CAS before RAS refresh to make do with access, wasteful current consumption.

[0004] to refresh with such access to do so, typically a DRAM having self-refresh function. And self-refresh function is stopped until the self-refresh is specified from the start has been given from outside the self-refresh, the refresh operation is conducted autonomously DRAM.

[0005] Thus, when the DRAM such as battery backup during power outages, the well-known due Patent Publication No. 7-45066, for example in DRAM technology that made the self-refresh a view to extend the backup time be.

[0006] [Problems to be Solved by the Invention] The above technical Publication No. Hei 7-45066, however, to indicate the start of the self-refresh DRAM once the main power is off, the self- control circuitry for the launch of the refresh instruction (5 signal generator) is taking to keep battery backup configuration.

[0007] Thus, in spite of the reduced current consumption in the long-awaited DRAM, which are generated from the current consumption control circuits in the battery backup, efficient power consumption You can not reduction, was invited to shorten the backup time.

[0008] The present invention has been made in consideration of the circumstances, we intended to do that to control the DRAM self-refreshing start without receiving power from the battery can, in the control circuit to provide a DRAM mode it is possible to extend the backup time of the DRAM with it.

[0009] [Means for Solving the Problem] The present invention in order to achieve the above

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[０００８]本発明はこのような事情を考慮してなされたものであり、その目的とするところは、バッテリからの電力供給を受けることなしにＤＲＡＭのセルフリフレッシュの起動制御を行うことができ、これによりＤＲＡＭのバックアップ時間の延長を図ることができるＤＲＡＭモード制御回路を提供することにある。

[０００９] [課題を解決するための手段]以上の目的を達成するために本発明は、バッテリバックアップされた例えば３．３Ｖ電源回路などの第１電源からの第１供給電力により動作するもので、外部からのリフレッシュ制御を受ける第１モードとリフレッシュ動作を自立的に行う第２モードとを有したＤＲＡＭと、バッテリバックアップされない例えば５Ｖ電源回路などの第２電源からの第２供給電力により動作し、前記ＤＲＡＭをリフレッシュ制御する例えばリフレッシュ制御回路などのリフレッシュ制御手段と、前記第２供給電力の電圧が正常時における所定の第１電圧（例えば５Ｖ）よりも低い所定の第２電圧（例えば４．７Ｖ）以上であるか否かを監視する例えば電圧監視回路などの電圧監視手段とを備え、前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧以上であることが検知されている場合には前記第１モードで、また前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧以上ではないことが検知されている場合には前記第２モードでそれぞれ前記ＤＲＡＭのリフレッシュを行うシステムに適用されて前記ＤＲＡＭのリフレッ less than DP N=0003 greater than シュモードの切換えを行うＤＲＡＭモード制御回路において、前記第２供給電力により動作し、前記第２供給電力の電圧が前記第２電圧よりも低い所定の第３電圧（例えば３．３Ｖ）以上であるときには前記第２電圧よりも低い所定の第４電圧（例えば３．３Ｖ）の第３供給電力を生成する例えばＤＣ－ＤＣコンバータなどの電圧変換手段と、この電圧変換手段により生成された前記第３供給電力により動作し、前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧よりも低下したことが新たに検知されたことに応じて、前記第３供給電力の電圧が前記第４電圧から低下してしまうまでの間に前記ＤＲＡＭを前記第２状態に設定し、また前記電圧監視手段

objectives, the first operated by power supplied from a 3.3V power supply circuits, etc. For example, the first battery-backed intended to, and having a second mode DRAM and autonomously carry out a refresh operation to receive the first mode and the external refresh control, a second power supply from 5V power supply circuit including a second example, no battery backup works by means of a refresh control circuit and refreshing the DRAM refresh control for example for controlling said first predetermined voltage at power supply voltage is normal, the second (5V for example) a predetermined second voltage lower than (For example, 4.7V) and a voltage monitoring means, such as for example the voltage monitoring circuit that monitors whether or not the least, found to be the second voltage higher than the voltage of the power supply voltage monitoring circuit means wherein said second If you are in the first mode, wherein the at least second voltage voltage of the power supply said second means monitoring the voltage is also when it is detected that there is no DRAM wherein each second mode, wherein The control circuit DRAM mode to switch the refresh rate less than DP N = 0003 greater than flash mode of the DRAM described above have been applied to systems that refresh, and works by electricity supply said second voltage of the power supply second The third predetermined voltage lower than the second voltage (3.3V, for example) when the voltage is greater than the fourth predetermined voltage lower than the second (3.3V, for example) DC power supply for example to generate a third -DC converters such as voltage conversion means, and operated by the third power supply generated by the voltage conversion means, that the second voltage lower than the voltage of the power supply voltage monitoring circuit means wherein said second In response to the sensed a new state of the second set of DRAM between said lowered voltage from the fourth voltage of said third power supply, said first means also monitors the voltage To set the state first DRAM, said in response to sensed a new thing that rises above the second voltage is the voltage of power supply 2, the means for switching modes consisting of the selector 13 and the circuit switching mode, for example with.

[0010] By such measures were taken, when the power supply voltage drops from the second battery backup power is not the second, after the second voltage sensed by the voltage drop to

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により前記第２供給電力の電圧が前記第２電圧以上に上昇したことが新たに検知されたことに応じて前記ＤＲＡＭを前記第１状態に設定する、例えばモード切換回路およびセレクタ１３よりなるモード切換手段とを備えた。

[００１０]このような手段を講じたことにより、バッテリバックアップされない第２電源からの第２供給電力の電圧が低下する際に、その電圧の低下が第２電圧にて検知された後にもその第２電圧よりも低い第３電圧に到達するまでは、第２供給電力に基づいて第４電圧の第３供給電力が安定して生成されて、この第３供給電力によってモード切換手段の動作が維持される。そして第２供給電力の電圧が低下していく過程において第３供給電力が安定して供給される間に、モード切換手段がＤＲＡＭのリフレッシュモードを切換えてセルフリフレッシュを起動する。またセルフリフレッシュを停止させるためのリフレッシュモードの切換えは、第２供給電力の電圧が第２電圧以上まで十分に復帰した後に行われる。従って、ＤＲＡＭのリフレッシュモードの切換えのためにバッテリバックアップされた第１電源からの第１供給電力は全く用いられない。

[００１１] [発明の実施の形態]以下、図面を参照して本発明の一実施形態につき説明する。

[００１２]図１は本実施形態に係るＤＲＡＭモード制御回路の構成を示すブロック図である。

[００１３]この図において、破線で囲い、符号１を付して示す部分がＤＲＡＭモード制御回路である。そしてこのＤＲＡＭモード制御回路１は、ＤＲＡＭ２の動作状態を、リフレッシュ制御回路３からの制御の下にリフレッシュを行う状態とセルフリフレッシュを行う状態とに切換え制御する。

[００１４]ＤＲＡＭ２は、セルフリフレッシュ機能を有したものであって、３．３Ｖ電源回路４から供給される第１供給電力により動作する。

[００１５]リフレッシュ制御回路３は、５Ｖ電源回路５から供給される第２供給電力により動作する。そしてリフレッシュ制御回路３は、ＣＡＳビフォアＲＡＳリフレッシュを行うべくＣＡＳ信号

reach the third voltage lower than the second voltage its is being produced by a stable power supply 3 of the fourth voltage based on the power supply a second means of mode switching by the power supply third The operation is maintained. While the power supply is stable in the process of supplying a third power supply voltage drops to second, and start the self-refresh mode of the DRAM refresh switched mode switching means. Switching to stop the refresh mode of self refresh is also be done after you wake up well over a second voltage power supply voltage of a second. Therefore, the power supplied from the first battery-backed power for the first switching mode, the DRAM refresh is not used at all.

[0011] [Embodiment of the Invention below, will be described an embodiment of the present invention with reference to the drawings.

[0012] 1 is a schematic block diagram showing the configuration of the DRAM mode control circuit according to an embodiment.

[0013] In this figure, enclosed by the dashed line is the DRAM mode control circuit portion of an annotated reference numeral 1 indicates. And the DRAM mode control circuit 1, the operating state of DRAM2, control is switched to perform self-refresh state and do a refresh state under the control of the refresh control circuit 3.

[0014] DRAM2 is a person who had the self-refresh function, to work with the first power supply circuit 4 is supplied from the power supply 3.3V.

[0015] 3 refresh control circuit is operated by a second power supply circuit 5 is supplied from the power supply 5V. The refresh control circuit 3 and supplies appropriate to DRAM2 DRAM mode control circuit via a first signal CAS and RAS signals 行Ubeku the CAS before RAS refresh.

[0016] 4 3.3V supply circuit, power is usually obtained from commercial power supply via a plug 6, to generate a first power supply voltage of 3.3V. 3.3V power supply circuit 4 is also connected to the battery 7 has been, if the commercial power supply is stopped, continue to occur first at 3.3V power supply derives power from the battery 7.

[0017] 5 5V power supply circuit is to obtain power from the utility power via a power plug 6, to generate a second power supply voltage of 5V. This 5V power supply circuit 5 is not connected to

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およびＲＡＳ信号をＤＲＡＭモード制御回路１を介してＤＲＡＭ２へと適宜供給する。

[００１６]３．３Ｖ電源回路４は、通常は電源プラグ６を介して商用電源から電力を得て、電圧３．３Ｖの第１供給電力を発生する。また３．３Ｖ電源回路４にはバッテリ７が接続されていて、商用電源の供給が停止された場合には、バッテリ７から電力を得て電圧３．３Ｖの第１供給電力を発生し続ける。

[００１７]５Ｖ電源回路５は、電源プラグ６を介して商用電源から電力を得て、電圧５Ｖの第２供給電力を発生する。この５Ｖ電源回路５にはバッテリ７が接続されておらず、従って商用電源の供給が停止された場合には第２供給電力の発生を停止する。

[００１８]電圧監視回路８は、５Ｖ電源回路５が発生する第２供給電力の電圧を監視する。そして電圧監視回路８は、第２供給電力の電圧が４．７Ｖ以上である場合に「Ｈ」レベル、第２供給電力の電圧が４．７Ｖよりも小さい場合に「Ｌ」レベルとしたＲＥＳＥＴ信号を発生する。電圧監視回路８が発生するＲＥＳＥＴ信号は、ＤＲＡＭモード制御回路１およびリフレッシュ制御回路３にそれぞれ与えられる。

[００１９]ところでＤＲＡＭモード制御回路１は、ＤＣ－ＤＣコンバータ１１、モード切換回路１２およびセレクタ回路１３を有している。

[００２０]ＤＣ－ＤＣコンバータ１１は、５Ｖ電源回路５が生成する第２供給電力を受けて、電圧３．３Ｖの第３供給電力を生成する。このＤＣ－ＤＣコンバータ１１は、５Ｖ電源回路５が生成する第２供給電力の電圧が本来の５Ｖから低下しても、その電圧が３．３Ｖ以上であるならば電圧３．３Ｖの第３供給電力を安定して生成することが可能である。

[００２１]モード切換回路１２は、ＤＣ－ＤＣコンバータ１１で生成された第３供給電力により動作する。モード切換回路１２には、電圧監視回路８が出力するＲＥＳＥＴ信号が与えられており、このＲＥＳＥＴ信号に応じた後述するタイミング

the battery 7, when the commercial power supply is stopped, therefore the power supply to stop the occurrence of a second.

[0018] 8 voltage monitor circuit monitors the voltage of the power supply circuit 5 causes the second supply 5V. And voltage monitoring circuit 8, when the power supply voltage of 4.7V or higher 2 "H" level, is less than 4.7V power supply voltage of the second "L" level and the RESET signal is generated. RESET signal generated voltage monitoring circuit 8 is fed 1 and 3, respectively refresh control circuit DRAM mode control circuit.

[0019] 1 DRAM mode control circuit is the way, DC-DC converter 11, and selector circuit 13 has a mode switching circuit 12.

[0020] DC-DC converter 11 is supplied by a second power supply circuit 5 generates 5V, generating a third power supply voltage of 3.3V. DC-DC converter 11 is also down from the original 5V power supply voltage generated by the second power supply circuit 5 5V, 3.3V supply voltage if it is the third of its voltage is above 3.3V It is possible to produce stable power.

[0021] 12-mode switching circuits, DC-3 operated by the electricity supply generated by the DC converter 11. Mode switching circuit 12, the RESET signal has been given the output voltage monitoring circuit 8, according to the RESET signal at the timing of this later, RAS and CAS signals for the commands to start and stop the self-refresh DRAM2 The combination of the signal to send. Mode switching circuit 12 is also switched by the selector circuit 13 to be supplied to the SEL signal, if necessary DRAM2 signals sent by the self-CAS and RAS signals.

[0022] 13 is a selector circuit, and RAS signals and CAS signals that are output from the refresh control circuit 3, and RAS signals and CAS signals that are output mode switching circuit 12, according to the SEL signal to select to give DRAM2.

[0023] will be described operation of the DRAM mode control circuit is configured to at least below.

[0024] First, when you are able to successfully get through the plug 6 power from commercial power supply, line 4 less than DP N = 0004 greater than once by the power from a 3.3V supply commercial which generates a first power supply, not using

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で、ＤＲＡＭ２にセルフリフレッシュを起動・停止させるためのコマンドをＣＡＳ信号およびＲＡＳ信号の組み合わせにより送出する。またモード切換回路１２は、自己が送出するＣＡＳ信号およびＲＡＳ信号を必要に応じてＤＲＡＭ２へと供給するようにＳＥＬ信号によりセレクタ回路１３を切換える。

[００２２]セレクタ回路１３は、リフレッシュ制御回路３から出力されるＣＡＳ信号およびＲＡＳ信号と、モード切換回路１２から出力されるＣＡＳ信号およびＲＡＳ信号とを、ＳＥＬ信号に応じて選択してＤＲＡＭ２へと与える。

[００２３]次に以上のように構成されたＤＲＡＭモード制御回路の動作につき説明する。

[００２４]まず、商用電源からの電力が電源プラグ６を介して正常に取得できている時には、３．３Ｖ電源回 less than DP N=0004 greater than 路４は商用電源からの電力により第１供給電力を生成しており、バッテリ７からの電力を使用していない。また、５Ｖ電源回路５が第２供給電力を電圧５Ｖで安定的に発生している。

[００２５]この状態では第２供給電力の電圧が４．７Ｖを上回っているので、電圧監視回路８はＲＥＳＥＴ信号を「H」レベルとしている。そしてこのようにＲＥＳＥＴ信号が「H」レベルであるならば、リフレッシュ制御回路３はＤＲＡＭ２にてＣＡＳビフォアＲＡＳリフレッシュを行うべくＣＡＳ信号およびＲＡＳ信号をそれぞれ出力する。またこのときにモード切換回路１２は、ＳＥＬ信号によりセレクタ回路１３にリフレッシュ制御回路３を選択させる。

[００２６]従ってこのときにＤＲＡＭ２では、リフレッシュ制御回路３の制御の下にＣＡＳビフォアＲＡＳリフレッシュが行われる。

[００２７]この状態から、停電や電源プラグ６の抜けなどにより商用電源からの電力が電源プラグ６を介して正常に取得できなくなったならば、３．３Ｖ電源回路４はバッテリ７からの電力を使い、第１供給電力の生成を継続する。従って、D

power from the battery 7. Also, have occurred in a stable 5V supply voltage to the second power supply circuit 5 5V.

[0025] In this state, because the power supply voltage of 4.7V above the second voltage monitor signal circuit 8 RESET "H" that level. RESET signal in this way is "H" if it is level, and outputs the refresh control circuit 3 and RAS signals 行 Ubeku the CAS signals CAS before RAS refresh at DRAM2. Mode when the switch circuit 12 also is to select a refresh control circuit 3 to 13 by the signal selector circuit SEL.

[0026] In DRAM2 this time, therefore, CAS before RAS refresh is performed under the control of the refresh control circuit 3.

[0027] In this state, if unable to successfully obtain power through the plug 6 power from commercial power due to power failure or disconnection of the plug 6, the 3.3V power supply circuit from the battery 7 4 Use the power of the power supply to continue to produce 1. Therefore, DRAM2 is able to continue operating by the first power supply.

[0028] However, the 5V supply to the circuit 5 is not given so much power from utility power, 5V power supply circuit 5 will not be able to maintain a 5V power supply to the second of the second power supply voltage begins to drop, as shown in Figure 2 (at T1 in Figure 2).

[0029] In the course of the second supply voltage decreases the power in this way, the voltage drops below 4.7V, the RESET signal and voltage monitoring circuit 8 which detects the "L" level changes that (at T2).

[0030] On the other hand, DC-DC converter 11, also began to supply a second power voltage drops, when its voltage falls below 3.3V (at T5) shows the voltage of the power supply until the third 3.3V to keep the two as shown.

[0031] 13 circuit mode selector switch circuit 12 and can therefore continue to work during the voltage drops to 3.3V power supply such a second. Mode switching circuit 12 and during this period, the procedure for starting the self-refresh DRAM2. 12 switching circuit mode, ie, on switching to the self-13 selector circuit, the first "H" signal to CAS had been with "L" level by changing the level (at T3), if the elapsed time TA predetermined it further If the "H" had been with

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ＲＡＭ２はこの第１供給電力により引き続き動作することが可能である。

[００２８]しかしながら５Ｖ電源回路５へは商用電源からの電力しか与えられないので、５Ｖ電源回路５は第２供給電力の電圧を５Ｖに維持することができなくなり、第２供給電力の電圧は図２に示すように低下し始める（図２中のＴ１時点）。

[００２９]このように第２供給電力の電圧が低下する過程において、その電圧が４．７Ｖを下回ると、これを電圧監視回路８が検知してＲＥＳＥＴ信号を「Ｌ」レベルに変化する（Ｔ２時点）。

[００３０]一方、ＤＣ－ＤＣコンバータ１１では、第２供給電力の電圧が低下し始めても、その電圧が３．３Ｖを下回るタイミング（Ｔ５時点）までは第３供給電力の電圧を図２に示すように３．３Ｖに維持する。

[００３１]そこでモード切換回路１２およびセレクタ回路１３はこのような第２供給電力の電圧が３．３Ｖまで低下する期間にも引き続き動作することができる。そしてこの期間にモード切換回路１２は、ＤＲＡＭ２のセルフリフレッシュを起動するための手順を実行する。すなわちモード切換回路１２はセレクタ回路１３を自己側に切換えた上で、まず「Ｈ」レベルとしてあったＣＡＳ信号を「Ｌ」レベルに変化させ（Ｔ３時点）、さらにそれから所定時間ＴＡが経過したならば「Ｈ」レベルとしてあったＲＡＳ信号を「Ｌ」レベルに変化させる（Ｔ４時点）。

[００３２]ＤＲＡＭ２は、このようなＣＡＳ信号およびＲＡＳ信号のレベル変化をセルフリフレッシュの起動指示として捉え、Ｔ４時点にてセルフリフレッシュを開始する。

[００３３]以降、第２供給電力の電圧が３．３Ｖを下回ると、ＤＣ－ＤＣコンバータ１１が第３供給電力の電圧を３．３Ｖに維持できなくなり、ＤＲＡＭモード制御回路１は動作を停止するが、ＤＲＡＭ２はセルフリフレッシュによって自立的にデータ保持を行う。従ってこの状態では、ＤＲＡＭ２によってのみバッテリ７からの電力の消費がなされる。

the RAS signal level "L" to change the level (at T4).

[0032] DRAM2 is regarded as an indication of the self-refresh start signal level changes, such as RAS and CAS signals, the self-refresh to start at point T4.

[0033] Thereafter, the voltage drops below 3.3V the second power supply, DC-can no longer maintain the power supply voltage to 3.3V DC converter 3 11, 1 DRAM mode control circuit operates have to stop, DRAM2 performs autonomous data retention by the self-refresh. In this state, therefore, is made from the battery power consumption by only 7 DRAM2.

[0034] On the other hand, will be able to get through and the power supply plug 6 from the commercial power supply resumes operation circuit 5 5V, the voltage rises on the second power supply. If you get the power supply voltage is 3.3V or more, and second, DC-output stable start to the third power supply voltage of 3.3V DC converter 11 (at T6). In response, the circuit 13 starts to operate switching circuit 12 and mode selector.

[0035] After reaching the 4.7V voltage is further increased by the second power supply, the voltage monitoring circuit 8 RESET signal "H" level is changed (at T7).

[0036] Thus the RESET signal is "H" 3 was the level if the refresh control circuit, the output of the signal to begin the RAS and CAS signals CAS before RAS refresh 行Ubeku DRAM2. But here is still doing well as a self-refresh state DRAM2, so that switching circuit 12 side, select the mode selector circuit 13, CAS before RAS refresh is performed.

[0037] 12 this condition and mode switching circuit, the steps to stop the self-refresh DRAM2. 12 switching circuit mode, ie, "L" RAS signal was as a level "H" is changed to the level (at T8), if the elapsed time TA predetermined that even "L" signal to CAS was as level " H "level to change (at T9).

[0038] DRAM2 is regarded as an indication of the self-refresh stop signal level changes, such as RAS and CAS signals, the time to stop the self-refresh at T9.

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[００３４]一方、商用電源からの電力が電源プラグ６を介して取得できるようになると、５Ｖ電源回路５が動作を再開し、第２供給電力の電圧が上昇して行く。そして第２供給電力の電圧が３．３Ｖ以上となったならば、ＤＣ－ＤＣコンバータ１１が電圧３．３Ｖの第３供給電力を安定的に出力し始める（Ｔ６時点）。これに応じて、モード切換回路１２およびセレクタ回路１３が動作を開始する。

[００３５]第２供給電力の電圧がさらに上昇して４．７Ｖに到達すると、電圧監視回路８がＲＥＳＥＴ信号を「Ｈ」レベルに変化させる（Ｔ７時点）。

[００３６]このようにＲＥＳＥＴ信号が「Ｈ」レベルとなったならばリフレッシュ制御回路３は、ＤＲＡＭ２のＣＡＳビフォアＲＡＳリフレッシュを行うべくＣＡＳ信号およびＲＡＳ信号の出力を開始する。しかしここではまだ、ＤＲＡＭ２がセルフリフレッシュを行う状態であるとともに、セレクタ回路１３がモード切換回路１２側を選択しているので、ＣＡＳビフォアＲＡＳリフレッシュは行われない。

[００３７]そしてこの状態でモード切換回路１２は、ＤＲＡＭ２のセルフリフレッシュを停止するための手順を実行する。すなわちモード切換回路１２は、「Ｌ」レベルとしてあったＲＡＳ信号を「Ｈ」レベルに変化させ（Ｔ８時点）、さらにそれから所定時間ＴＡが経過したならば「Ｌ」レベルとしてあったＣＡＳ信号を「Ｈ」レベルに変化させる（Ｔ９時点）。

[００３８]ＤＲＡＭ２は、このようなＣＡＳ信号およびＲＡＳ信号のレベル変化をセルフリフレッシュの停止指示として捉え、Ｔ９時点にてセルフリフレッシュを停止する。

[００３９]そしてこの後にモード切換回路１２は、ＳＥＬ信号によってセレクタ回路１３をリフレッシュ制御回路３側に切換えて、リフレッシュ制御回路３によるＣＡＳビフォアＲＡＳリフレッシュを有効とする。

[0039] 12 and then switch circuit mode, the control circuit 3 is switched to the refresh circuit 13 by a signal selector SEL, and CAS before RAS refresh is enabled by the refresh control circuit 3.

[0040] According to this embodiment as described above, the DRAM mode control circuit 1 is supplied by a second power generated by operating only at 5 5V power supply circuit of the mains, from the battery 7 to work without being power. Then, place it can operate at standard 3.3V voltage lower than 4.7V power supply voltage drop detection of the second period to take advantage of lowered from 4.7V to 3.3V power supply voltage of the second steps to launch the self-refresh and DRAM2. less than DP N = 0005 greater than

[0041] Thus, the power from the battery 7 in the first DRAM mode control circuit without any result, it becomes possible to maximize the backup time with battery DRAM2 7.

[0042] Furthermore the invention is not limited to the embodiments described above are not. In the above embodiment, for example, 3.3V voltage power supply for their normal first to third, 5V, and 3.3V, and 4.7V reference voltage is the voltage drop is detected a second power supply also that these voltages, the voltage of the second power supply> the reference voltage sensing power supply voltage drops 2> may be any of the power supply if the relationship 電圧Naru 3.

[0043] In the above embodiment also, DC-DC converter 11 is that it is capable of generating a third power supply voltage of 3.3V at 3.3V or more, a second power supply, configurations may not be able to generate a third of the power supplied is higher than 3.3V to 3.3V power supply voltage of a second. That may have to use a power supply, such as those that can generate a third voltage of 3.3V to 3.5V when the voltage of the power supply is greater than the second example. However, DC from the power supply senses the voltage drop in second-period until it can not generate a third power supply voltage of 3.3V DC converter 11 steps possible to launch a self-refresh DRAM2 need to ensure that period.

[0044] In addition, various modifications can be carried out without departing from the scope of the invention.

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[００４０]以上のように本実施形態によれば、ＤＲＡＭモード制御回路１は、商用電源の電力のみで動作する５Ｖ電源回路５で生成される第２供給電力により、バッテリ７からの電力を受けることなく動作する。そして、第２供給電力の電圧低下の検知基準の電圧４．７Ｖよりも低い３．３Ｖにて動作可能としておき、第２供給電力の電圧が４．７Ｖから３．３Ｖまで低下する期間を利用してＤＲＡＭ２にセルフリフレッシュを起動させる手順を実行する。 less than DP N=0005 greater than

[００４１]従って、ＤＲＡＭモード制御回路１ではバッテリ７からの電力消費は全く無く、この結果、バッテリ７によるＤＲＡＭ２のバックアップ時間を最大限に確保することが可能となる。

[００４２]なお本発明は上記実施形態に限定されるものではない。例えば上記実施形態では、第１乃至第３供給電力のそれぞれの通常の電圧を３．３Ｖ、５Ｖ、３．３Ｖとし、また第２供給電力の電圧低下を検知する基準電圧を４．７Ｖとしているが、これらの電圧は、第２供給電力の電圧＞第２供給電力の電圧低下を検知する基準電圧＞第３供給電力の電圧なる関係に有れば任意であって良い。

[００４３]また上記実施形態では、ＤＣ－ＤＣコンバータ１１は第２供給電力の電圧が３．３Ｖ以上であれば電圧３．３Ｖの第３供給電力を生成可能であるとしているが、第２供給電力の電圧が３．３Ｖよりも高いときに３．３Ｖの第３供給電力を生成できなくなる構成であっても良い。すなわち、例えば第２供給電力の電圧が３．５Ｖ以上であるときに電圧３．３Ｖの第３供給電力を生成可能なものなどを用いるようにしても良い。ただし、第２供給電力の電圧低下を検知してからＤＣ－ＤＣコンバータ１１が電圧３．３Ｖの第３供給電力を生成できなくなるまでの期間が、ＤＲＡＭ２にセルフリフレッシュを起動させる手順を実行可能な期間となるようにする必要がある。

[００４４]このほか、本発明の要旨を逸脱しない範囲で種々の変形実施が可能である。

[0045] [Effects of the Invention According to the invention operates by supplying a second power supply from the battery backup is not a second than the first predetermined voltage at power supply voltage is normal, the second When a voltage higher than a predetermined third lower than the second voltage of a predetermined low and means for converting the voltage generated by the power supply a third voltage fourth predetermined lower than the second voltage generation means converts the voltage The power supplied by the third operation was, according to new sensed that the second voltage lower than the voltage of the power supply voltage monitoring means wherein said second, said third power supply The second set of DRAM state between said lowered voltage from the fourth voltage, it rises above the second voltage supply voltage of the second power means also monitors the voltage Since switching mode with the means to set the DRAM to said first state in response to sensed a new power supply from the first battery-backed power for the first switching mode of the DRAM refresh is not used at all, and DRAM mode control circuit it is possible to extend the backup time by which the DRAM.

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[００４５] [発明の効果]本発明によれば、バッテリバックアップされない第２電源からの第２供給電力により動作し、前記第２供給電力の電圧が正常時における所定の第１電圧よりも低い所定の第２電圧よりも低い所定の第３電圧以上であるときには前記第２電圧よりも低い所定の第４電圧の第３供給電力を生成する電圧変換手段と、この電圧変換手段により生成された前記第３供給電力により動作し、前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧よりも低下したことが新たに検知されたことに応じて、前記第３供給電力の電圧が前記第４電圧から低下してしまうまでの間に前記ＤＲＡＭを前記第２状態に設定し、また前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧以上に上昇したことが新たに検知されたことに応じて前記ＤＲＡＭを前記第１状態に設定するモード切換手段とを備えたので、ＤＲＡＭのリフレッシュモードの切換えのためにバッテリバックアップされた第１電源からの第１供給電力は全く用いられず、これによりＤＲＡＭのバックアップ時間の延長を図ることができるＤＲＡＭモード制御回路となる。

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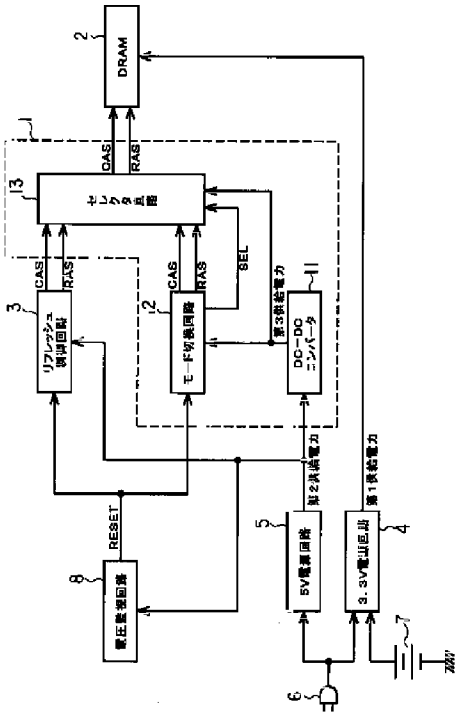
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(54)【発明の名称】　ＤＲＡＭモード制御回路

(57)【要約】
【課題】　バッテリからの電力供給を受けることなしにＤＲＡＭのセルフリフレッシュの起動制御を行うことができ、これによりＤＲＡＭのバックアップ時間の延長を図ることを可能とする。
【解決手段】　ＤＣ－ＤＣコンバータ１１は、５Ｖ電源回路５が生成する第２供給電力（平常時５Ｖ）に基づき、この第２供給電力の電圧が３．３Ｖ以上であるならば電圧３．３Ｖの第３供給電力を安定的に出力する。モード切換回路１２は、第２供給電力の電圧が４．７Ｖよりも低下したことが電圧監視回路８により検知されたことに応じて、それからＤＣ－ＤＣコンバータ１１が第３供給電力を電圧３．３Ｖで生成できなくなるまでの間に、セレクタ回路１３を自己側に切換えた上でＤＲＡＭ２にセルフリフレッシュを起動させるための手順を実行する。



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【特許請求の範囲】
【請求項１】　バッテリバックアップされた第１電源からの第１供給電力により動作するもので、外部からのリフレッシュ制御を受ける第１モードとリフレッシュ動作を自立的に行う第２モードとを有したＤＲＡＭと、
バッテリバックアップされない第２電源からの第２供給電力により動作し、前記ＤＲＡＭをリフレッシュ制御するリフレッシュ制御手段と、
前記第２供給電力の電圧が正常時における所定の第１電圧よりも低い所定の第２電圧以上であるか否かを監視する電圧監視手段とを備え、
前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧以上であることが検知されている場合には前記第１モードで、また前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧以上ではないことが検知されている場合には前記第２モードでそれぞれ前記ＤＲＡＭのリフレッシュを行うシステムに適用されて前記ＤＲＡＭのリフレッシュモードの切換えを行うＤＲＡＭモード制御回路において、
前記第２供給電力により動作し、前記第２供給電力の電圧が前記第２電圧よりも低い所定の第３電圧以上であるときには前記第２電圧よりも低い所定の第４電圧の第３供給電力を生成する電圧変換手段と、
この電圧変換手段により生成された前記第３供給電力により動作し、前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧よりも低下したことが新たに検知されたことに応じて、前記第３供給電力の電圧が前記第４電圧から低下してしまうまでの間に前記ＤＲＡＭを前記第２状態に設定し、また前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧以上に上昇したことが新たに検知されたことに応じて前記ＤＲＡＭを前記第１状態に設定するモード切換手段とを具備したことを特徴とするＤＲＡＭモード制御回路。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、外部からのリフレッシュ制御を受ける第１モードとリフレッシュ動作を自立的に行う第２モードとを有したＤＲＡＭのモード切換えを行うＤＲＡＭモード制御回路に関する。
【０００２】
【従来の技術】ＤＲＡＭは、データを保持しておくためにリフレッシュを行うことが必要である。通常、ＤＲＡＭのリフレッシュは、アクセスを行う状態ではアクセスを行う側からの制御により、例えばＣＡＳビフォアＲＡＳリフレッシュが行われる。
【０００３】ところでこのような外部制御によるＣＡＳビフォアＲＡＳリフレッシュなどのリフレッシュ動作では、ＤＲＡＭにおける消費電流が比較的大きい。このため、アクセスを行わない状態でＣＡＳビフォアＲＡＳリフレッシュを行うことは、消費電流の無駄が多い。
【０００４】そこでこのようなアクセスを行わない状態でのリフレッシュのために、セルフリフレッシュ機能を有したＤＲＡＭが一般的である。セルフリフレッシュ機能とは、外部からセルフリフレッシュの起動が指定されてからセルフリフレッシュの停止が指定されるまでの間は、ＤＲＡＭが自立的にリフレッシュ動作を行うものである。
【０００５】そこで、停電時などにＤＲＡＭをバッテリバックアップするような場合には、バックアップ時間の延長を図るべくＤＲＡＭにセルフリフレッシュを行わせる技術が例えば特開平7-45066号公報などにより周知である。
【０００６】
【発明が解決しようとする課題】ところが上記特開平7-45066号公報の技術では、メイン電源がオフとなった後にＤＲＡＭにセルフリフレッシュの起動を指示するために、そのセルフリフレッシュの起動指示を行うための制御回路（信号発生回路５）はバッテリバックアップしておく構成をとっている。
【０００７】このため、せっかくＤＲＡＭでの消費電流を低減しているのにも拘わらず、制御回路にてバックアップ用のバッテリからの電流消費が発生しているのであり、効率良く消費電流を低減できておらず、バックアップ時間の短縮を招いていた。
【０００８】本発明はこのような事情を考慮してなされたものであり、その目的とするところは、バッテリからの電力供給を受けることなしにＤＲＡＭのセルフリフレッシュの起動制御を行うことができ、これによりＤＲＡＭのバックアップ時間の延長を図ることができるＤＲＡＭモード制御回路を提供することにある。
【０００９】
【課題を解決するための手段】以上の目的を達成するために本発明は、バッテリバックアップされた例えば３．３Ｖ電源回路などの第１電源からの第１供給電力により動作するもので、外部からのリフレッシュ制御を受ける第１モードとリフレッシュ動作を自立的に行う第２モードとを有したＤＲＡＭと、バッテリバックアップされない例えば５Ｖ電源回路などの第２電源からの第２供給電力により動作し、前記ＤＲＡＭをリフレッシュ制御する例えばリフレッシュ制御回路などのリフレッシュ制御手段と、前記第２供給電力の電圧が正常時における所定の第１電圧（例えば５Ｖ）よりも低い所定の第２電圧（例えば４．７Ｖ）以上であるか否かを監視する例えば電圧監視回路などの電圧監視手段とを備え、前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧以上であることが検知されている場合には前記第１モードで、また前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧以上ではないことが検知されている場合には前記第２モードでそれぞれ前記ＤＲＡＭのリフレッシュを行うシステムに適用されて前記ＤＲＡＭのリフレッ

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シュモードの切換えを行うＤＲＡＭモード制御回路において、前記第２供給電力により動作し、前記第２供給電力の電圧が前記第２電圧よりも低い所定の第３電圧（例えば３．３Ｖ）以上であるときには前記第２電圧よりも低い所定の第４電圧（例えば３．３Ｖ）の第３供給電力を生成する例えばＤＣ－ＤＣコンバータなどの電圧変換手段と、この電圧変換手段により生成された前記第３供給電力により動作し、前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧よりも低下したことが新たに検知されたことに応じて、前記第３供給電力の電圧が前記第４電圧から低下してしまうまでの間に前記ＤＲＡＭを前記第２状態に設定し、また前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧以上に上昇したことが新たに検知されたことに応じて前記ＤＲＡＭを前記第１状態に設定する、例えばモード切換回路およびセレクタ１３よりなるモード切換手段とを備えた。

【００１０】このような手段を講じたことにより、バッテリバックアップされない第２電源からの第２供給電力の電圧が低下する際に、その電圧の低下が第２電圧にて検知された後にもその第２電圧よりも低い第３電圧に到達するまでは、第２供給電力に基づいて第４電圧の第３供給電力が安定して生成されて、この第３供給電力によってモード切換手段の動作が維持される。そして第２供給電力の電圧が低下していく過程において第３供給電力が安定して供給される間に、モード切換手段がＤＲＡＭのリフレッシュモードを切換えてセルフリフレッシュを起動する。またセルフリフレッシュを停止させるためのリフレッシュモードの切換えは、第２供給電力の電圧が第２電圧以上まで十分に復帰した後に行われる。従って、ＤＲＡＭのリフレッシュモードの切換えのためにバッテリバックアップされた第１電源からの第１供給電力は全く用いられない。

【００１１】

【発明の実施の形態】以下、図面を参照して本発明の一実施形態につき説明する。

【００１２】図１は本実施形態に係るＤＲＡＭモード制御回路の構成を示すブロック図である。

【００１３】この図において、破線で囲い、符号１を付して示す部分がＤＲＡＭモード制御回路である。そしてこのＤＲＡＭモード制御回路１は、ＤＲＡＭ２の動作状態を、リフレッシュ制御回路３からの制御の下にリフレッシュを行う状態とセルフリフレッシュを行う状態とに切換え制御する。

【００１４】ＤＲＡＭ２は、セルフリフレッシュ機能を有したものであって、３．３Ｖ電源回路４から供給される第１供給電力により動作する。

【００１５】リフレッシュ制御回路３は、５Ｖ電源回路５から供給される第２供給電力により動作する。そしてリフレッシュ制御回路３は、ＣＡＳビフォアＲＡＳリフレッシュを行うべくＣＡＳ信号およびＲＡＳ信号をＤＲＡＭモード制御回路１を介してＤＲＡＭ２へと適宜供給する。

【００１６】３．３Ｖ電源回路４は、通常は電源プラグ６を介して商用電源から電力を得て、電圧３．３Ｖの第１供給電力を発生する。また３．３Ｖ電源回路４にはバッテリ７が接続されていて、商用電源の供給が停止された場合には、バッテリ７から電力を得て電圧３．３Ｖの第１供給電力を発生し続ける。

【００１７】５Ｖ電源回路５は、電源プラグ６を介して商用電源から電力を得て、電圧５Ｖの第２供給電力を発生する。この５Ｖ電源回路５にはバッテリ７が接続されておらず、従って商用電源の供給が停止された場合には第２供給電力の発生を停止する。

【００１８】電圧監視回路８は、５Ｖ電源回路５が発生する第２供給電力の電圧を監視する。そして電圧監視回路８は、第２供給電力の電圧が４．７Ｖ以上である場合に「Ｈ」レベル、第２供給電力の電圧が４．７Ｖよりも小さい場合に「Ｌ」レベルとしたＲＥＳＥＴ信号を発生する。電圧監視回路８が発生するＲＥＳＥＴ信号は、ＤＲＡＭモード制御回路１およびリフレッシュ制御回路３にそれぞれ与えられる。

【００１９】ところでＤＲＡＭモード制御回路１は、ＤＣ－ＤＣコンバータ１１、モード切換回路１２およびセレクタ回路１３を有している。

【００２０】ＤＣ－ＤＣコンバータ１１は、５Ｖ電源回路５が生成する第２供給電力を受けて、電圧３．３Ｖの第３供給電力を生成する。このＤＣ－ＤＣコンバータ１１は、５Ｖ電源回路５が生成する第２供給電力の電圧が本来の５Ｖから低下しても、その電圧が３．３Ｖ以上であるならば電圧３．３Ｖの第３供給電力を安定して生成することが可能である。

【００２１】モード切換回路１２は、ＤＣ－ＤＣコンバータ１１で生成された第３供給電力により動作する。モード切換回路１２には、電圧監視回路８が出力するＲＥＳＥＴ信号が与えられており、このＲＥＳＥＴ信号に応じた後述するタイミングで、ＤＲＡＭ２にセルフリフレッシュを起動・停止させるためのコマンドをＣＡＳ信号およびＲＡＳ信号の組み合わせにより送出する。またモード切換回路１２は、自己が送出するＣＡＳ信号およびＲＡＳ信号を必要に応じてＤＲＡＭ２へと供給するようにＳＥＬ信号によりセレクタ回路１３を切換える。

【００２２】セレクタ回路１３は、リフレッシュ制御回路３から出力されるＣＡＳ信号およびＲＡＳ信号と、モード切換回路１２から出力されるＣＡＳ信号およびＲＡＳ信号とを、ＳＥＬ信号に応じて選択してＤＲＡＭ２へと与える。

【００２３】次に以上のように構成されたＤＲＡＭモード制御回路の動作につき説明する。

【００２４】まず、商用電源からの電力が電源プラグ６を介して正常に取得できている時には、３．３Ｖ電源回

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路4は商用電源からの電力により第1供給電力を生成しており、バッテリ7からの電力を使用していない。また、5V電源回路5が第2供給電力を電圧5Vで安定的に発生している。

【0025】この状態では第2供給電力の電圧が4．7Vを上回っているので、電圧監視回路8はRESET信号を「H」レベルとしている。そしてこのようにRESET信号が「H」レベルであるならば、リフレッシュ制御回路3はDRAM2にてCASビフォアRASリフレッシュを行うべくCAS信号およびRAS信号をそれぞれ出力する。またこのときにモード切換回路12は、SEL信号によりセレクタ回路13にリフレッシュ制御回路3を選択させる。

【0026】従ってこのときにDRAM2では、リフレッシュ制御回路3の制御の下にCASビフォアRASリフレッシュが行われる。

【0027】この状態から、停電や電源プラグ6の抜けなどにより商用電源からの電力が電源プラグ6を介して正常に取得できなくなったならば、3．3V電源回路4はバッテリ7からの電力を使い、第1供給電力の生成を継続する。従って、DRAM2はこの第1供給電力により引き続き動作することが可能である。

【0028】しかしながら5V電源回路5へは商用電源からの電力しか与えられないので、5V電源回路5は第2供給電力の電圧を5Vに維持することができなくなり、第2供給電力の電圧は図2に示すように低下し始める（図2中のT1時点）。

【0029】このように第2供給電力の電圧が低下する過程において、その電圧が4．7Vを下回ると、これを電圧監視回路8が検知してRESET信号を「L」レベルに変化する（T2時点）。

【0030】一方、DC-DCコンバータ11では、第2供給電力の電圧が低下し始めても、その電圧が3．3Vを下回るタイミング（T5時点）までは第3供給電力の電圧を図2に示すように3．3Vに維持する。

【0031】そこでモード切換回路12およびセレクタ回路13はこのような第2供給電力の電圧が3．3Vまで低下する期間にも引き続き動作することができる。そしてこの期間にモード切換回路12は、DRAM2のセルフリフレッシュを起動するための手順を実行する。すなわちモード切換回路12はセレクタ回路13を自己側に切換えた上で、まず「H」レベルとしてあったCAS信号を「L」レベルに変化させ（T3時点）、さらにそれから所定時間TAが経過したならば「H」レベルとしてあったRAS信号を「L」レベルに変化させる（T4時点）。

【0032】DRAM2は、このようなCAS信号およびRAS信号のレベル変化をセルフリフレッシュの起動指示として捉え、T4時点にてセルフリフレッシュを開始する。

【0033】以降、第2供給電力の電圧が3．3Vを下回ると、DC-DCコンバータ11が第3供給電力の電圧を3．3Vに維持できなくなり、DRAMモード制御回路1は動作を停止するが、DRAM2はセルフリフレッシュによって自立的にデータ保持を行う。従ってこの状態では、DRAM2によってのみバッテリ7からの電力の消費がなされる。

【0034】一方、商用電源からの電力が電源プラグ6を介して取得できるようになると、5V電源回路5が動作を再開し、第2供給電力の電圧が上昇して行く。そして第2供給電力の電圧が3．3V以上となったならば、DC-DCコンバータ11が電圧3．3Vの第3供給電力を安定的に出力し始める（T6時点）。これに応じて、モード切換回路12およびセレクタ回路13が動作を開始する。

【0035】第2供給電力の電圧がさらに上昇して4．7Vに到達すると、電圧監視回路8がRESET信号を「H」レベルに変化させる（T7時点）。

【0036】このようにRESET信号が「H」レベルとなったならばリフレッシュ制御回路3は、DRAM2のCASビフォアRASリフレッシュを行うべくCAS信号およびRAS信号の出力を開始する。しかしここではまだ、DRAM2がセルフリフレッシュを行う状態であるとともに、セレクタ回路13がモード切換回路12側を選択しているので、CASビフォアRASリフレッシュは行われない。

【0037】そしてこの状態でモード切換回路12は、DRAM2のセルフリフレッシュを停止するための手順を実行する。すなわちモード切換回路12は、「L」レベルとしてあったRAS信号を「H」レベルに変化させ（T8時点）、さらにそれから所定時間TAが経過したならば「L」レベルとしてあったCAS信号を「H」レベルに変化させる（T9時点）。

【0038】DRAM2は、このようなCAS信号およびRAS信号のレベル変化をセルフリフレッシュの停止指示として捉え、T9時点にてセルフリフレッシュを停止する。

【0039】そしてこの後にモード切換回路12は、SEL信号によってセレクタ回路13をリフレッシュ制御回路3側に切換えて、リフレッシュ制御回路3によるCASビフォアRASリフレッシュを有効とする。

【0040】以上のように本実施形態によれば、DRAMモード制御回路1は、商用電源の電力のみで動作する5V電源回路5で生成される第2供給電力により、バッテリ7からの電力を受けることなく動作する。そして、第2供給電力の電圧低下の検知基準の電圧4．7Vよりも低い3．3Vにて動作可能としておき、第2供給電力の電圧が4．7Vから3．3Vまで低下する期間を利用してDRAM2にセルフリフレッシュを起動させる手順を実行する。

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【００４１】従って、ＤＲＡＭモード制御回路１ではバッテリ７からの電力消費は全く無く、この結果、バッテリ７によるＤＲＡＭ２のバックアップ時間を最大限に確保することが可能となる。

【００４２】なお本発明は上記実施形態に限定されるものではない。例えば上記実施形態では、第１乃至第３供給電力のそれぞれの通常の電圧を３．３Ｖ、５Ｖ、３．３Ｖとし、また第２供給電力の電圧低下を検知する基準電圧を４．７Ｖとしているが、これらの電圧は、第２供給電力の電圧＞第２供給電力の電圧低下を検知する基準電圧＞第３供給電力の電圧なる関係に有れば任意であって良い。

【００４３】また上記実施形態では、ＤＣ－ＤＣコンバータ１１は第２供給電力の電圧が３．３Ｖ以上であれば電圧３．３Ｖの第３供給電力を生成可能であるとしているが、第２供給電力の電圧が３．３Ｖよりも高いときに３．３Ｖの第３供給電力を生成できなくなる構成であっても良い。すなわち、例えば第２供給電力の電圧が３．５Ｖ以上であるときに電圧３．３Ｖの第３供給電力を生成可能なものなどを用いるようにしても良い。ただし、第２供給電力の電圧低下を検知してからＤＣ－ＤＣコンバータ１１が電圧３．３Ｖの第３供給電力を生成できなくなるまでの期間が、ＤＲＡＭ２にセルフリフレッシュを起動させる手順を実行可能な期間となるようにする必要がある。

【００４４】このほか、本発明の要旨を逸脱しない範囲で種々の変形実施が可能である。

【００４５】

【発明の効果】本発明によれば、バッテリバックアップされない第２電源からの第２供給電力により動作し、前記第２供給電力の電圧が正常時における所定の第１電圧よりも低い所定の第２電圧よりも低い所定の第３電圧以上であるときには前記第２電圧よりも低い所定の第４電圧の第３供給電力を生成する電圧変換手段と、この電圧変換手段により生成された前記第３供給電力により動作し、前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧よりも低下したことが新たに検知されたことに応じて、前記第３供給電力の電圧が前記第４電圧から低下してしまうまでの間に前記ＤＲＡＭを前記第２状態に設定し、また前記電圧監視手段により前記第２供給電力の電圧が前記第２電圧以上に上昇したことが新たに検知されたことに応じて前記ＤＲＡＭを前記第１状態に設定するモード切換手段とを備えたので、ＤＲＡＭのリフレッシュモードの切換えのためにバッテリバックアップされた第１電源からの第１供給電力は全く用いられず、これによりＤＲＡＭのバックアップ時間の延長を図ることができるＤＲＡＭモード制御回路となる。

【図面の簡単な説明】

【図１】本発明の一実施形態に係るＤＲＡＭモード制御回路の構成を示すブロック図。

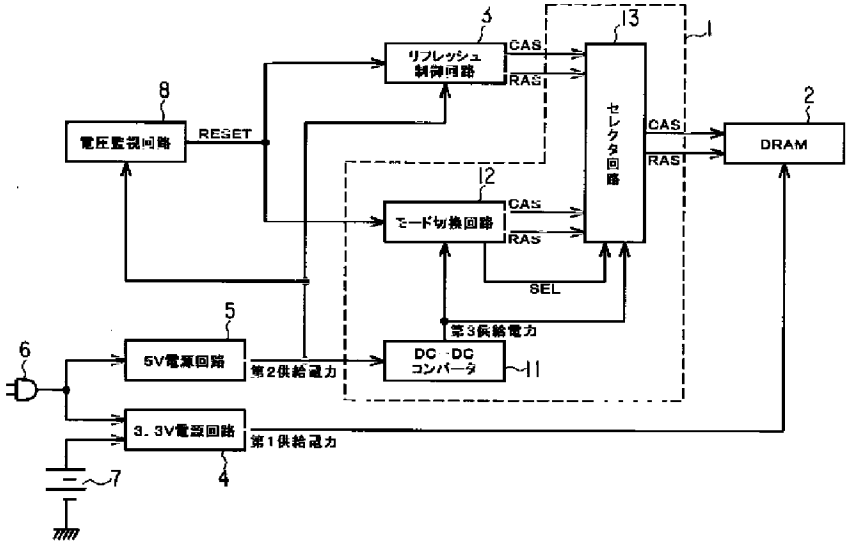
【図２】ＤＲＡＭ２のセルフリフレッシュの起動および停止のための手順の実行タイミングを示す図。

【符号の説明】

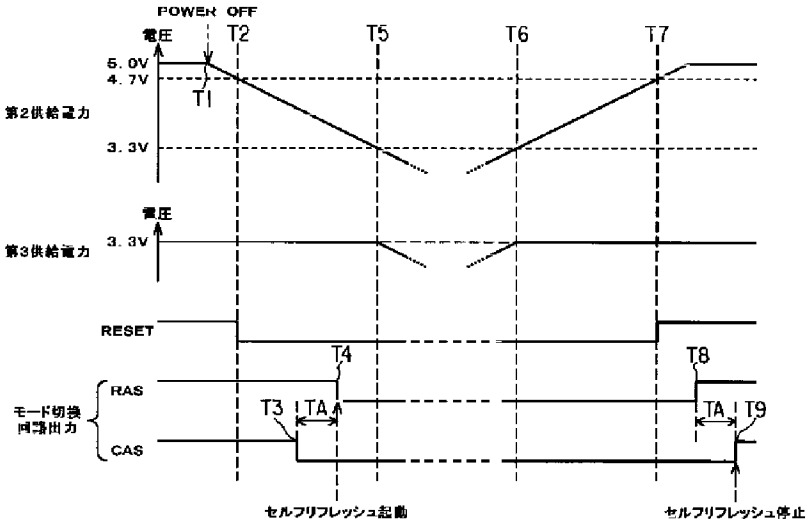
１…モード制御回路
１１…ＤＣ－ＤＣコンバータ
１２…モード切換回路
１３…セレクタ回路
２…ＤＲＡＭ
３…リフレッシュ制御回路
４…３．３Ｖ電源回路
５…５Ｖ電源回路
６…電源プラグ
７…バッテリ
８…電圧監視回路

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【図1】


リフレッシュ制御回路
CAS
RAS
セレクタ回路
CAS
RAS
DRAM
電圧監視回路
RESET
モード切換回路
CAS
RAS
SEL
第3供給電力
5V電源回路
第2供給電力
DC-DC コンバータ
3.3V電源回路
第1供給電力

【図2】


POWER OFF
電圧
5.0V
4.7V
第2供給電力
3.3V
電圧
第3供給電力
3.3V
RESET
モード切換回路出力
RAS
CAS
T1
T2
T3
T4
T5
T6
T7
T8
T9
TA
TA
セルフリフレッシュ起動
セルフリフレッシュ停止

Espacenet

KR20050073902A SEMICONDUCTOR MEMORY MODULE AND METHOD OF TESTING OPERATING MARGIN THEREOF, AND SEMICONDUCTOR MEMORY APPARATUS

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SEMICONDUCTOR MEMORY MODULE AND METHOD OF TESTING OPERATING MARGIN THEREOF, AND SEMICONDUCTOR MEMORY APPARATUS

Abstract

The present invention discloses a semiconductor memory module, a test method thereof, and a semiconductor memory device. The semiconductor memory module of the present invention includes a circuit board having a plurality of external input/output terminals, an interface circuit installed on the circuit board, a plurality of semiconductor memory chips, and a nonvolatile memory chip. The interface circuit interfaces signal transmission between a plurality of external input terminals and an internal circuit. The plurality of semiconductor memory chips are connected to the interface circuit, input an external address signal having mode setting information, decode the input mode setting information, generate a mode setting control signal, provide the mode setting control signal to a normal operation circuit in a normal mode, and provide the mode setting control signal to a test operation circuit in a test mode. The nonvolatile memory chip stores the initial values of the semiconductor memory chips to provide the initial values to the outside through the interface circuit at the time of initial booting of the system. Therefore, in the present invention, various tests can be performed on chips inside the memory module by mode setting, so that test efficiency can be improved during the test process.

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(54) 동작마진 테스트가 가능한 반도체 메모리 모듈 및 테스트방법과 반도체 메모리 장치

요약

본 발명은 반도체 메모리 모듈 및 그 테스트 방법과 반도체 메모리 장치를 개시한다. 본 발명의 반도체 메모리 모듈은 복수의 외부 입출력단자들을 가지는 회로기판과, 회로기판 상에 설치된 인터페이스회로, 복수의 반도체 메모리 칩들, 및 불휘발성 메모리 칩을 포함한다. 인터페이스회로는 복수의 외부 입력단자들과 내부 회로 사이의 신호전송을 인터페이스 한다. 복수의 반도체 메모리 칩들은 인터페이스 회로와 연결되고, 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 입력된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하고, 정상모드에서는 모드세팅 제어신호를 정상동작회로부에 제공하고, 테스트 모드에서는 모드세팅 제어신호를 테스트동작회로부에 제공한다. 불휘발성 메모리 칩은 시스템 초기 부팅시에 상기 인터페이스 회로를 통하여 외부로 상기 반도체 메모리 칩들의 초기값을 제공하기 위하여 상기 초기값을 저장한다. 따라서, 본 발명에서는 메모리 모듈 내부의 칩들을 모드세팅에 의해 다양한 테스트를 수행할 수 있어서, 테스트 과정에서 테스트 효율을 향상시킬 수 있다.

대표도

도 2

명세서

도면의 간단한 설명

도 1은 본 발명에 의한 반도체 메모리 모듈의 구성도.

도 2는 도 1의 내부 메모리 칩의 회로 블록도.

도 3은 도 2의 반도체 메모리 칩의 모드세팅회로의 일예를 나타낸 도면.

도 4는 본 발명에 의한 모드 레지스터 세팅 코드 테이블의 일예를 나타낸 도면.

도 5는 도 1의 반도체 메모리 모듈의 테스트 동작을 설명하기 위한 흐름도.

* 도면의 주요 부분에 대한 간단한 부호설명*

100 : 메모리 모듈 110 : 회로기판

120 : 인터페이스부 130 : 메모리 칩, SDRAM

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140 : 인식부, EEPROM 206 : 모드 레지스터

207 : 모드 세팅회로 MRD : 모드 세팅 디코더

FS1, FS2 : 퓨징회로부 NC : 정상 동작 회로부

TC : 테스트 동작 회로부

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 동작마진 테스트가 가능한 반도체 메모리 모듈 및 테스트 방법과 반도체 메모리 장치에 관한 것으로서, 특히 테스트 동작시 모드 세팅을 프로그램할 수 있도록 함으로써 동작마진을 테스트할 수 있는 반도체 메모리 모듈 및 테스트 방법에 관한 것이다,

컴퓨터 시스템의 중앙처리장치의 성능 향상과 더불어 많은 양의 데이터를 고속으로 처리하기 위하여 고속동작의 대용량 메인 메모리들이 사용되고 있다. 특히 퍼스널 컴퓨터 시스템의 메인 메모리로는 DDR(Double Data Rate) 또는 램버스 디램 칩들을 하나의 패키지로 구성한 메모리 모듈이 상품화되어 제공되고 있다.

이러한 메모리 모듈은 복수의 단위 메모리 칩들을 회로기판 상에 구성하고 구성된 모듈을 마더보드에 장착하여 시스템에 연결한다.

컴퓨터 시스템에서는 시스템 부팅 동작을 고속으로 하기 위하여 메모리 모듈을 초기화하기 위한 초기화 정보를 메모리 모듈 내부에 저장하도록 요구하고 있다.

컴퓨터 시스템이 부팅을 할 때 제대로 작동하기 위해서는 메모리 모듈의 구성형태를 인식할 수 있어야 한다. PPD(Parallel Presence Detect - 병렬 구성 인식장치)는 필요로 하는 정보를 연결시키기 위해 레지스터를 사용하는 일반적인 방법으로 주로 SIMM(Single-In-Line Memory Module)방식의 모듈에서 사용하고, SPD(Serial Presence Detect - 직렬 구성 인식장치)란 DIMM(Dual-In-Line Memory Module)방식의 모듈에서 사용하는 방식으로 모듈에 관한 정보 저장시 EEPROM을 이용하는 것이다.

이와 같은 메모리 모듈의 테스트 범위는 단위 메모리 칩의 구성에 따라 제한된다. 통상적으로 동기형 DRAM의 경우 칩 내부에 모드 레지스터를 구비하고 테스트 모드로 세팅하도록 구성되어 있다. 즉, 단위 칩에서 세팅은 단순히 칩을 테스트 모드로 세팅할 것인지 아니면 노말 모드로 할 것인지를 선택하는 정도의 모드 세팅만 주어진 상태이다.

그러나, 이러한 단위 칩들을 모듈로 구성할 경우 복수의 칩들 간의 데이터 입출력 동작 마진이 서로 차이가 있을 수 있으며, 실장환경이나 모듈에 따라 미세한 동작 파라미터들의 차이가 형성될 우려가 있었다. 그러므로 모듈 실장 후에 이들 파라미터들을 측정하여 모듈 전체의 가장 적합한 마진을 찾아서 모듈 내부의 각 메모리 칩들을 세팅하지 않으면 안되었다. 즉 처음 모듈 생산시에 가장 적당한 마진이 어느 것인지 알 수 없으므로 다양한 동작 마진을 가진 테스트용 샘플 모듈들을 제작한 다음에 실장된 상태에서 테스트하여 최적의 마진을 찾아내는 과정이 요구되었다.

그러나, 각 개별적인 메모리 칩들에는 테스트 모드시 파라미터 값들을 변경하면서 동작 마진을 테스트하기 위한 기능이 없으므로 각 변경값들 마다 각각 별도의 테스트용 모듈을 마련하여 테스트하여야 하기 때문에 많은 비용과 시간이 소요되었다.

이와 같은 작업과정은 시간과 비용을 증가시키므로 모듈 생산 코스트를 상승시킨다.

발명이 이루고자 하는 기술적 과제

본 발명의 목적은 이와 같은 종래 기술의 문제점을 해결하기 위하여 복수의 메모리 칩들 사이의 최적 동작마진을 테스트할 수 있는 반도체 메모리 모듈 및 그 테스트 방법을 제공하는 데 있다.

본 발명의 다른 목적은 복수의 동작마진 테스트를 프로그램할 수 있는 반도체 메모리 장치를 제공하는 데 있다.

발명의 구성 및 작용

상기 목적을 달성하기 위하여 본 발명의 메모리 모듈은 복수의 외부 입출력단자들을 가지는 회로기판과, 회로기판 상에 설치된 인터페이스 회로, 복수의 반도체 메모리 칩들 및 인식부를 포함한다.

인터페이스부는 메모리 칩들과 입출력단자 사이의 신호전송을 인터페이스 한다. 인터페이스부는 타이밍 레지스터를 포함한다. 각 반도체 메모리 칩들은 인터페이스 회로와 연결되고, 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 입력된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하고, 정상모드에서는 상기 모드세팅 제어신호를 정상동작회

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로부에 제공하고, 테스트 모드에서는 모드세팅 제어신호를 테스트동작회로부에 제공한다. 여기서 반도체 메모리 칩들은 각각 DDR SDRAM 또는 램버스 디램으로 구성될 수 있다. 인식부는 시스템 초기 부팅시에 상기 인터페이스 회로를 통하여 외부로 상기 반도체 메모리 칩들의 초기값을 제공하기 위하여 상기 초기값을 저장한다. 여기서 인식부는 직렬 입출력방식의 EEPROM으로 구성한다.

본 발명의 목적을 달성하기 위한 본 발명의 테스트 방법은 다음 단계들을 포함한다.

a) 메모리 테스트 장비에 테스트용 메모리 모듈을 장착하는 단계;

b) 상기 장착된 테스트용 메모리 모듈로부터 초기값 정보를 리드하는 단계;

c) 상기 리드된 초기값 정보에 응답하여 상기 테스트용 메모리 모듈을 초기화 하는 단계;

d) 상기 초기화된 테스트용 메모리 모듈에 테스트 모드 세팅정보를 제공하는 단계;

e) 상기 메모리 모듈 내부에 탑재된 복수의 메모리 칩들을 제공된 테스트 모드 세팅정보에 응답하여 대응하는 테스트 모드로 세팅하는 단계;

f) 상기 세팅된 테스트 모드로 상기 메모리 모듈을 테스트 하는 단계; 및

g) 메모리 모듈에 제공되는 테스트 모드 세팅정보를 변경하면서 상기 d 내지 f단계를 반복하여 최적 동작의 모드 세팅정보를 검출하는 단계.

본 발명에서 테스트용 메모리 모듈은 전기적 퓨징에 의해 내부에 탑재된 복수의 메모리 칩들을 테스트 모드로 프로그램하는 단계를 더 포함한다.

상기 다른 목적을 달성하기 위하여 본 발명의 반도체 메모리 장치는 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 저장하는 모드 레지스터와, 모드 레지스터에 연결되고, 상기 모드 레지스터에 저장된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하는 모드세팅 디코더와, 정상모드에서는 상기 모드세팅 제어신호를 정상동작회로부에 제공하고, 테스트 모드에서는 상기 모드세팅 제어신호를 테스트동작회로부에 제공하기 위해 퓨징되는 퓨즈회로부를 구비한다.

이하, 첨부한 도면을 참조하여 본 발명의 바람직한 실시예를 구체적으로 설명하고자 한다. 이 실시예는 이 기술에 숙련된 자들이 본 발명을 실시할 수 있게 충분히 상세하게 기술한다.

도 1은 본 발명에 의한 반도체 메모리 모듈의 구성도를 나타낸다.

도1에서 본 발명의 메모리 모듈(100)은 회로기판(110) 상에 인터페이스부(120), 복수의 SDRAM(130), 인식부(140)를 설치하여서 된 것이다. 구체적인 예는 본 출원인이 2003년 8월에 공개한 DDR SDRAM Registered Module의 데이터 매뉴얼에 개시되어 있다. 회로기판(110)에는 데이터, 데이터 스트로브신호, 어드레스신호, 타이밍신호, 전원신호 등을 입출력하기 위한 184핀의 입출력단자들(112)이 형성된다.

인터페이스부(120)는 어드레스 및 타이밍 레지스터로 구성한다. 뱅크어드레스 BA0~BA1, 어드레스신호 A0~A12, 타이밍신호들 CS0~CS1, RAS, CAS, CKE0, CKE1, WE 등을 입력하여 내부칩선택신호, 내부 뱅크어드레스신호, 내부 어드레스신호, 내부 타이밍신호 등을 발생한다.

SDRAM(130)은 메모리 용량에 따라 512M, 1G, 2G 등으로 구성할 수 있다.

인식부(140)는 EEPROM으로 구성하고 시리얼 클럭신호에 응답하여 시리얼 데이터를 입출력한다.

도 2는 도 1의 내부 메모리 칩의 회로 블록도를 나타낸다. 도 2에서 본 발명에 의한 SDRAM(Synchronous Dynamic Random Accesses Memory)(130)은 어드레스 레지스터 (202), 타이밍 레지스터(204), 모드 레지스터(206), 모드세팅회로(207), 로우 디코더(208), 컬럼 디코더(210), 메모리 셀어레이(212), 데이터 입력버퍼 및 데이터 입력 레지스터(214), 데이터 출력버퍼(216), 데이터 스트로브 출력버퍼(218), DLL(220) 등을 포함한다.

어드레스 레지스터(202)는 뱅크 어드레스신호 및 어드레스신호(ADD) 등을 입력하여 버퍼링하여 타이밍 제어신호에 응답하여 로우 어드레스, 컬럼 어드레스, 모드세트 어드레스 등을 제공한다.

타이밍 레지스터(204)는 CKE, CS, RAS, CAS, WE 등의 외부 타이밍 제어신호를 입력하여 버퍼링하여 내부 타이밍 제어신호를 발생한다.

모드 레지스터(206)는 타이밍 제어신호, 에컨대 모드 세트 커맨드에 응답하여 모드 세트 어드레스를 래치하여 모드세트 정보를 저장한다.

모드세팅회로(207)는 모드세팅 디코더(MRD), 제1퓨즈회로(FS1), 제2퓨즈회로(FS2), 정상동작 회로부(NC), 테스트동작 회로부(TC)를 포함한다.

도 3을 참조하면, 모드세팅 디코더(MRD)는 MRS 커멘드(MRSCMD)신호와 모드세팅 어드레스 비트(Ai, Aj)를 G1 내지 G4의 게이트를 통하여 디코딩하여 4개의 모드세팅 제어신호(MRS1~MRS4)를 각각 출력한다.

제1 퓨즈회로(FS1) 및 제2 퓨즈회로(FS2)는 과도전류를 흘려서 퓨즈를 절단시킴으로써 '0' 또는 '1'의 상태에서 '1' 또는 '0'의 상태로 출력이 변환되는 통상적인 퓨즈회로로 구성한다.

정상적인 메모리 칩에서는 FS2는 모두 턴오프되고 FS1는 모두 턴온되어 MRS1~MRS4 신호가 정상동작회로에 인가되도록 퓨징된다. 따라서, 정상동작시에는 외부에서 어드레스 비트 Ai, Aj 값을 변경하는 것에 모드세팅 제어신호(MRS1~MRS4)를 발생하고 그 중에 대응하는 모드세팅에 의해 정상동작회로가 프로그램된다.

테스트용 메모리 칩에서는 FS1은 모두 턴오프되고 FS2는 모두 턴온되도록 퓨징된다. 따라서, 테스트 동작시에는 외부에서 어드레스 비트 Ai, Aj 값을 변경하는 것에 모드세팅 제어신호(MRS1~MRS4)를 발생하고 그 중에 대응하는 모드세팅에 의해 테스트 동작회로가 프로그램된다.

도 4는 본 발명에 의한 모드 레지스터 세팅 코드 테이블의 일예를 나타낸다.

즉, 어드레스 비트 Ai, Aj값에 의해 4가지 테스트 모드의 설정이 가능하다. 도시한 바와 같이, 디램의 억세스 타임(tAC) 값을 + 100ps, + 200ps, -100ps, -200ps 등으로 동작마진을 조금씩 변경하면서 설정할 수 있도록 프로그램할 수 있다.

도 5는 도 1의 반도체 메모리 모듈의 테스트 동작을 설명하기 위한 흐름도를 나타낸다.

먼저 모듈 테스트 장비에 테스트용 메모리 모듈(TMM)을 장착한다(S10). 여기서 테스트용 메모리 모듈(TMM)은 상술한 테스트 모드 프로그램이 가능한 메모리 칩들로 구성한 메모리 모듈을 칭하며, 내부 칩들이 테스트모드로 퓨징된 모듈을 말한다.

테스트 장비에서 장착된 메모리 모듈에 SPD 리드명령을 전달하여 모듈의 인식부로부터 읽혀진 SPD 코드 값을 전송받아 장착된 메모리 모듈의 초기값 정보를 해석한다(S12).

해석된 초기값 정보에 따라 TMM을 초기화시킨다(S14).

이어서, 초기화된 TMM에 모드세트 어드레스 정보를 제공하고 MRS 커멘드를 내려서 제1테스트 모드로 모드세팅시킨다(S16).

이어서 주어진 테스트 패턴에 의해 메모리 모듈을 테스트하고, 테스트 결과를 분석한다(S18).

테스트 결과 분석에 의해 최적 동작마진이 아닐 경우에는 모드변경을 수행하여(S20) S16, S18 단계를 반복 수행한다.

상기 테스트에 의해 최적 동작마진이 검출되면 그 테스트 결과를 저장한다(S22).

예컨대 이와 같은 방식에 의해 메모리 칩의 억세스 타임을 초기치에서부터 + 200ps 로부터 -200ps로 4단계로 바꾸어가면서 최적의 억세스 타임을 세팅할 수 있게 된다.

실시예를 참조하여 설명하였지만, 해당 기술 분야의 숙련된 당업자는 하기의 특허 청구의 범위에 기재된 본 발명의 사상 및 영역으로부터 벗어나지 않는 범위 내에서 본 발명을 다양하게 수정 및 변경시킬 수 있음을 이해할 수 있을 것이다.

발명의 효과

상술한 바와 같이 본 발명에서는 메모리 모듈의 테스트시 동작마진을 조금씩 변경하면서 테스트 할 수 있으므로 하나의 테스트 메모리 모듈을 사용하여 최적의 동작마진을 손쉽게 검출할 수 있게 된다. 그러므로, 종래의 4개의 테스트 메모리 모듈을 하나의 테스트 모듈로 모두 테스트 할 수 있으므로 테스트 비용을 절감할 수 있고 테스트 작업 효율을 향상시킬 수 있다.

(57) 청구의 범위

청구항 1.

모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 저장하는 모드 레지스터;

상기 모드 레지스터에 연결되고, 상기 모드 레지스터에 저장된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하는 모드세팅 디코더;

정상모드에서는 상기 모드세팅 제어신호를 정상동작회로부에 제공하고, 테스트 모드에서는 상기 모드세팅 제어신호를 테스트동작회로부에 제공하기 위해 퓨징되는 퓨즈회로부를 구비한 것을 특징으로 하는 반도체 메모리 장치.

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청구항 2.

복수의 외부 입출력단자들을 가지는 회로기판;

상기 회로기판 상에 설치되고, 상기 복수의 외부 입력단자들과 내부 회로 사이의 신호전송을 인터페이스 하기 위한 인터페이스 회로;

상기 회로기판 상에 설치되고, 상기 인터페이스 회로와 연결되고, 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 입력된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하고, 정상모드에서는 상기 모드세팅 제어신호를 정상동작 회로부에 제공하고, 테스트 모드에서는 상기 모드세팅 제어신호를 테스트동작회로부에 제공하는 복수의 반도체 메모리 칩들; 및

상기 회로기판 상에 설치되고, 시스템 초기 부팅시에 상기 인터페이스 회로를 통하여 외부로 상기 반도체 메모리 칩들의 초기값을 제공하기 위하여 상기 초기값을 저장한 인식부를 구비한 것을 특징으로 하는 메모리 모듈.

청구항 3.

a) 메모리 테스트 장비에 테스트용 메모리 모듈을 장착하는 단계;

b) 상기 장착된 테스트용 메모리 모듈로부터 초기값 정보를 리드하는 단계;

c) 상기 리드된 초기값 정보에 응답하여 상기 테스트용 메모리 모듈을 초기화 하는 단계;

d) 상기 초기화된 테스트용 메모리 모듈에 테스트 모드 세팅정보를 제공하는 단계;

e) 상기 메모리 모듈 내부에 탑재된 복수의 메모리 칩들을 제공된 테스트 모드 세팅정보에 응답하여 대응하는 테스트 모드로 세팅하는 단계;

f) 상기 세팅된 테스트 모드로 상기 메모리 모듈을 테스트 하는 단계;

g) 메모리 모듈에 제공되는 테스트 모드 세팅정보를 변경하면서 상기 d 내지 f단계를 반복하여 최적 동작의 모드 세팅정보를 검출하는 단계를 포함하는 것을 특징으로 하는 반도체 메모리 모듈 테스트 방법.

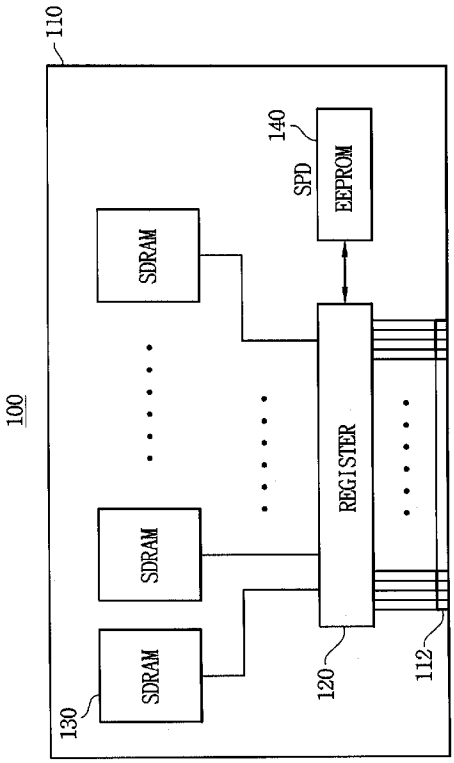
청구항 4.

제3항에 있어서, 상기 테스트용 메모리 모듈은 퓨징에 의해 내부에 탑재된 복수의 메모리 칩들을 테스트 모드로 프로그램하는 단계를 더 포함하는 것을 특징으로 하는 반도체 메모리 모듈 테스트 방법.

도면

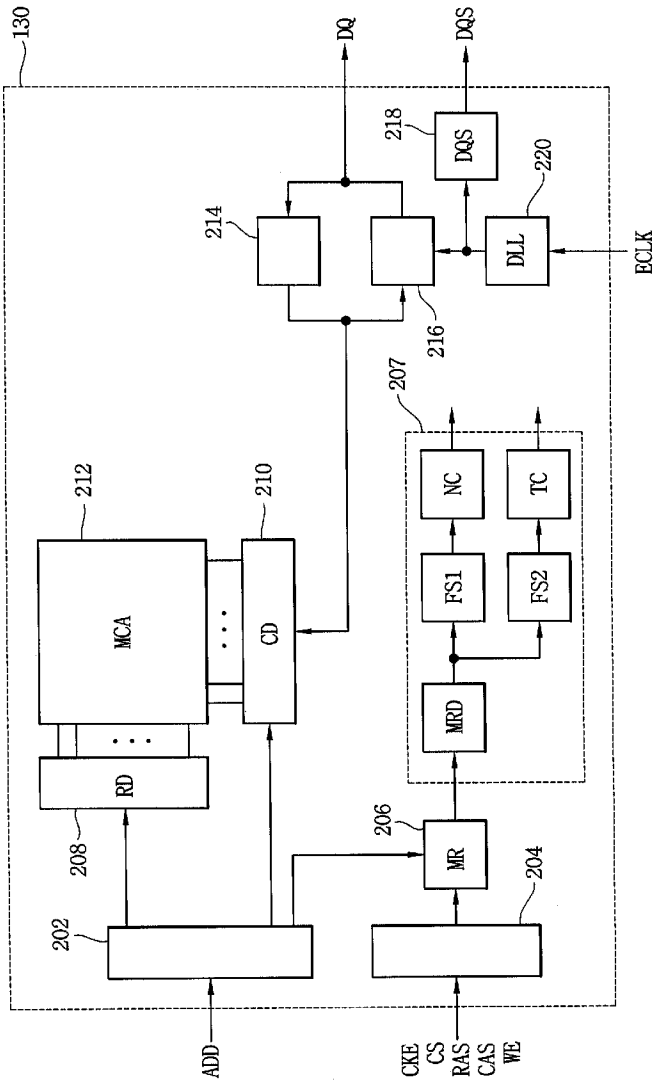
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도면



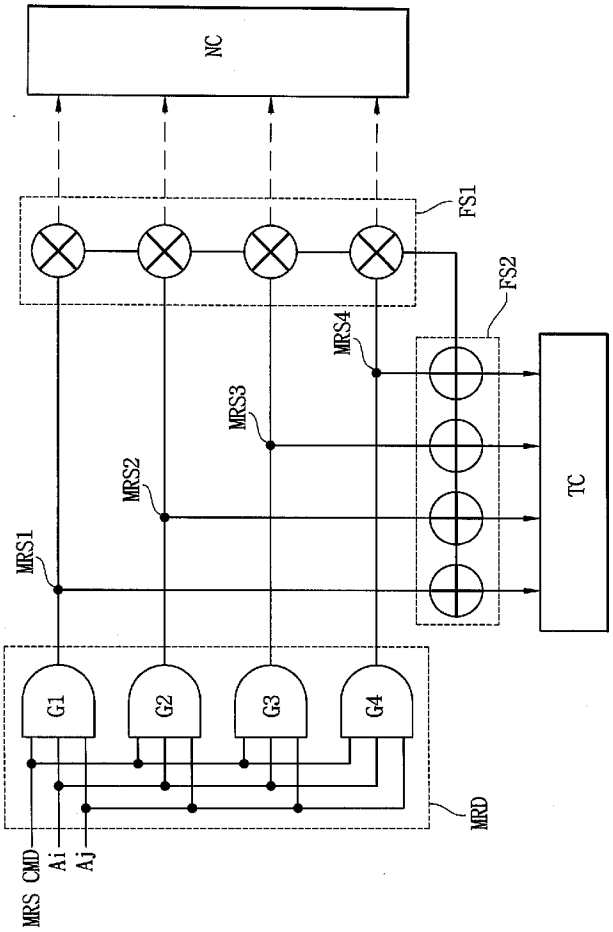
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도면2



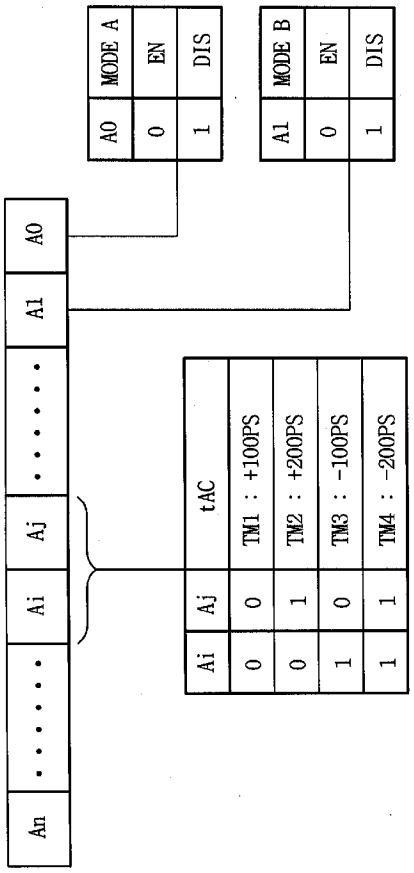
Samsung Electronics Co., Ltd.
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도면3

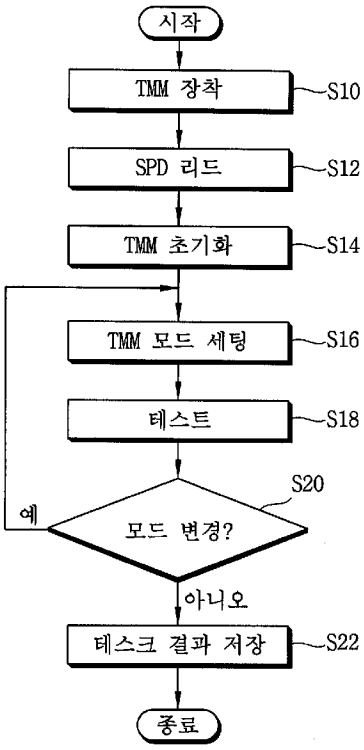


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도면4



도면5



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Title

SEMICONDUCTOR MEMORY MODULE AND METHOD OF TESTING OPERATING MARGIN THEREOF, AND SEMICONDUCTOR MEMORY APPARATUS

Abstract
The present invention relates to a semiconductor memory device with memory modules and how to test for them. In the present invention, a semiconductor memory having a plurality of external input and output terminals formed on the circuit board and the circuit board, a plurality of semiconductor memory chips are installed, the interface circuit, and includes a non-volatile memory chip. The interface circuit includes a plurality of external input terminals is the interface signal transmission between the ink container and the internal circuit. A plurality of semiconductor memory chips are connected to the interface circuit, mode setting information input mode setting signal with an external address decode information, and generating a control signal setting mode in the normal mode, the normal operation mode setting control signal by providing the test mode, the circuit mode and provides the control signal to the test operation for the circuit setting. The non-volatile memory chip in the system via the interface circuit during the initial boot, the initial value of the semiconductor memory chips outside in order to provide the initial value. Therefore, in the present invention, chips inside the memory module tests that can be performed by setting mode, it is possible during the test, the test efficiency can be improved.

Figure 1 is a semiconductor memory according to the present invention [0001] configuration of the module.

[0002] FIG. 2 is a circuit block diagram of the memory chip of Figure 1 shown inside.

[0003] FIG. 3 is circuit of FIG. 2, in the setting mode of the semiconductor memory chips.

[0004] Figure 4 is a code table according to the present invention, showing an example of a mode register setting.

[0005] FIG. 5 is tested semiconductor memory modules of Fig. 1 flow chart for explaining the operation of the.

[0006] * Code Description of the main parts of the drawings *

[0007] 100: memory module 110 simple: Circuit Board

[0008] 120: interface unit 130: Memory chip, SDRAM

, EEPROM 206: mode 140: recognition section [0009] register

[0010] : mode setting decoder 207: mode setting circuit MRD

FS1, FS2: fusing circuitry NC: [0011] Normal operation circuit portion

[0012] TC: Test

theinvention purpose operating circuit. People are object of the invention disclosure by reference to thebackground art and the art of the art
of the present invention prior art [0013] test is possible the operation margin and testing methods and semiconductor memory modules, and more particularly to a semiconductor memory device which can be programd for test operation mode setting can be used to test the operation margin by a semiconductor memory modules, and relates to a method of testing the

performance of a central processing unit of the computer system, [0014] With large amounts of data at high speed in order to handle the large amounts of main memory are used in high-speed operation. In particular personal computer system's main memory using a double data rate (DDR) or Rambus dynamic random access memory chips in a single package has been configured memory modules are being provided.

[0015] This memory module includes a plurality of unit memory chips on a circuit board attached to the configured modules connected to the system motherboard.

[0016] computer systems boot operation at a high speed in order to initialize the memory module, memory module initialization information for required to be stored therein.

[0017] When computer system in order to boot memory module configuration of working properly, should also be recognized. A PPD(PARALLEL presence detect-and-parallel configuration information requiring a recognition device) in order to connect using a Simm(single-in-line) in the normal way use of module mainly, serial presence detect-series configuration method of Dimm(dual-in-line) recognition device) is used in a way that module from the module when it is carried out using the information stored in the EEPROM.

[0018] Testing of such a memory module, depending on the configuration of the multi-unit memory chip is limited. In the case of synchronous DRAM chips typically provided with internal to mode register is configured to set a test mode. In other words, in a unit chip test mode to be set simply setting if you want to select whether the normal mode, the degree of the mode setting a given state.

[0019] However, when such a unit chip module data input/output operations between the plurality of chips may be margin may differ from each other depending on the module of the mounting environment or the difference between the fine there is a fear that the operating parameters. Therefore module by measuring these parameters after the mounting of the entire module, each of the memory modules within the best margin setting and should not unless chips. That is, the first module at the time of production can not know whether one is the most suitable margin to various operating margin manufactured by the following test samples in the mounted state on modules test process to find the optimal margin is required.

[0020] However, when the test mode of each individual memory chips, while changing parameter values because there is no function for testing the operation margin values for each individual change to provide separate test because the test module is costly and time consuming.

[0021] Such a workflow module increases the time and cost increases the production costs.

Abstract problem invention is a technical problem to be solved

[0022] An object of the present invention to solve the problems of the prior art as described above has a plurality of memory chips can be used to test the optimum operating margin between a semiconductor memory module and to provide a method for the test.

[0023] Another object of the present invention can be programd to a plurality of operating margin test is to provide a semiconductor memory device.

Invention configuration configuration and operation of the invention
in order to achieve the above object, the present invention [0024] memory module having a plurality of external input and output terminals formed on the circuit board and the circuit board, a plurality of semiconductor memory chips are installed, the interface circuit and the detection unit.

[0025] Interface unit memory chips and interfaces for signal transmission between the ink container and the input and output terminals. Interface unit timing registers. Each of the semiconductor memory chips are connected to the interface circuit, mode setting information input mode setting signal with an external address decode information, and generating a control signal setting mode in the normal mode, the normal operation control signal setting mode by providing the test mode, the circuit mode and provides the control signal to the test operation for the circuit setting. Each of the semiconductor memory chips that can be configured as a DDR SDRAM or Rambus dynamic random access memory. The interface to the system during the initial boot recognition through the circuit external to the semiconductor memory chip, to provide an initial value of the initial value. In the serial EEPROM of the recognition unit configured system.

[0026] The present invention for achieving the object of the present invention method includes the following steps.

[0027] a memory module for mounting a memory test equipment for testing;

[0028] b) the initial value from the attached test memory module;

[0029] c) to read the information in response to the initial value for the read information; initializing a memory module,

memory module test mode the initialized test [0030] d) providing a setting information;

[0031] e) a plurality of memory chip mounted on the memory module, in response to the test mode, the test mode corresponding to the setting information;

[0032] f) the setting in the setting mode of the memory module to test the test; and

[0033]) is provided to the memory module while changing the test mode setting information to the optimum operation of the repeat steps d to f information, detecting the password setting mode.

[0034] In the present invention, testing the memory module is mounted therein by electrically fused to the plurality of memory chips are further comprises the step of the program the test mode.

[0035] In order to achieve the above another object of the present invention is a semiconductor memory device includes a mode setting information stored in the mode register to enter an external address signal and is connected to the mode register, wherein the mode register setting information stored in the

mode control signal for generating a setting mode, in the normal mode the mode setting mode setting decoder and a normal operating circuitry to provide a control signal, in the test mode, the test mode setting control signal fused to provide operation circuit, the fuse circuit unit.

[0036] Referring now to the drawings with reference to the accompanying drawings a preferred embodiment of the present invention will now be described in detail. This embodiment those skilled in the art to practice the present invention are described in sufficient detail to enable.

[0037] FIG. 1 is a configuration diagram of a semiconductor memory module according to the present invention.

[0038] memory module 100 of the present invention in Figure 1, interface unit 120, a plurality of the circuit board 110 on the hayeoseo install a SDRAM(130), recognition unit 140. Specific examples of the present applicant published in August 2003 manual data of DDR SDRAM registered module is disclosed. Circuit board 110 has data, data strobe signals, address signals, timing signals, power signals, etc. for input and output the input and output terminals 112 are formed in the fin 184.

[0039] Interface unit 120 is configured to address and timing registers. Bank address BA<0 Cs0~cs1, Ba0~ba1, CKE0, A0~a12, timing signals, address signals, RAS, CAS, CKE1, inside the internal chip select signal, the WE, address signals, bank address signals, internal timing signal and the like generated inside.

[0040] In accordance with SDRAM(130) 1G, 2G, such as the memory capacity, it is possible to configure 512M,.

[0041] Composed of recognition unit 140 recognizes the EEPROM and serial clock signal in response to the serial data.

[0042] FIG. 2 is a circuit block diagram of Figure 1 shows the internal memory chip. In Figure 2 the according to the present invention address the dynamic random access memory (SDRAM (202 accesses memory)(130) timing register 204, mode register 206, row decoder 208, column decoder 210, a mode setting circuit 207 of the memory cell array 212, a data input buffer 216 and data input resistor 214, DLL(220) data strobe output buffer 218 data output buffer and the like.

[0043] address register 202 receives input of a bank address signals and address signals ADD) in response to a timing control signal buffers, such as a row address, a column address mode provides a set address.

[0044] Timing of such a CKE, register 204, (, RAS, CAS, we enter the external timing control signal and generates a timing control signal internal keulreokreul.

[0045] A mode register 206 is a timing control signals, such as a mode in response to the set command set address latches a set of modes mode and stores the information.

[0046] Decoder circuit 207 includes (MRD), setting mode the first fuse circuit setting mode second fuse circuit (FS2), (FS1), (NC), normal operation circuit includes a test operation circuit (TC).

[0047] Referring to FIG. 3, mode setting signal and (MRSCMD) MRS command decoder (MRD) address bits ai, AJ) setting mode through the gate of the G1 to G4 by (MRS1~MRS4) four mode setting control signal and outputs, respectively.

[0048] The first fuse circuit FS1 and a second current transient to fuse circuit FS2 by fuse cutting state '1' or '0', '0' or '1 into the state of the output is converted into a conventional fuse circuits.

[0049] Normal memory chips, FS2) are both turned off and Mrs1~mrs4 FS1) are both turned on is applied to the normal circuit operation. Therefore, during normal operation from the outside address bits Ai, Aj in that it changes the value of the mode setting control signal corresponds to a (MRS1~MRS4) and the normal operation circuit is programd by setting mode.

[0050] In test memory chips are all turned off, and FS1) are both turned on so that the FS2. Therefore, in the outside at the time of test operation to change the value of the address bits Ai, Aj in setting mode and generates a control signal corresponding to a (MRS1~MRS4) mode set by the test operation circuit is programd.

[0051] Figure 4 is a code table according to the present invention shows an example of a mode register setting.

[0052] In other words, address bits ai, AJ value it is possible to set the four test mode. As illustrated, the value of the dram -100ps, access time (TAC), such as -200ps +200ps, +100ps, while changing little by little to the operation margin can be programd so that it can be set.

[0053] FIG. 5 is a semiconductor memory module of FIG. 1 shows a flow chart for explaining the operation of the test.

[0054] The first module is equipped with (TMM) test equipment for testing memory module (S10). Here the above test mode for testing memory module capable of (TMM) program configured as memory chips, memory modules into interior chips are refers to the module test mode.

[0055] Test equipment by passing the command to the memory module is mounted on the module of the SPD lead code value read from the recognition unit image receiving the SPD memory modules, analyzes the information of the initial value (S12).

[0056] Interpreted and initializes the information in accordance with the initial value TMM (S14).

[0057] Subsequently, and to provide the mode set address information initialized TMM MRS command, thereby lowering the first test mode settings (S16).

[0058] A memory module by a given test pattern to test and analyze the test result (S18).

[0059] The present invention is best by analyzing test results if not a member performs the operation margin (S20, S16, S18, repeat steps a mode change.

[0060] The optimal operating margin is detected by testing the stores the result of the test (S22).

[0061] e.g. according to this method, the initial value of memory chips by +200ps -200ps from access time to change from Optimal Use of step 4 is capable of setting the access time.

[0062] It has been described with reference to exemplary embodiments, the skilled person of ordinary skill in the art within the scope of the invention as set forth in the claims without departing from the spirit and scope of the present invention vary the invention within the scope not can make various changes and modifications will be appreciated that be.

Advantageous effects of the invention
as described above, the present invention effects [0063] In the testing of a memory module, while changing little by little to the operation margin can be tested using a single test, the optimal operating margin of memory modules can be easily detected. Therefore, in the conventional four test all memory modules in a single test modules can be tested and the test can reduce the cost of the test, it is possible to improve the working efficiency.

1.

Setting mode to enter an external address signal with information stored in the mode register (207) is

connected to the mode register mode setting information stored in the mode register by setting a mode setting mode; generating a control signal

in the normal mode, the normal operation control signal setting mode by providing the test mode, the circuit mode setting control signal and to provide the test operation circuit, the fuse circuit unit for fusing to a semiconductor memory device characterized in that having a.

2.

Circuit having a plurality of external input and output terminals formed on the

circuit board is provided on the substrate; a plurality of external input terminals of the signal transmission between the ink container and the internal circuit; an interface circuit for interfacing to

being installed on the circuit board, wherein the interface circuit is connected to the mode setting information to the setting information input mode to enter an external address signal generates a control signal by decoding setting mode, in the normal mode the mode setting to provide control signals to the normal operation mode, the test circuit, and test operation mode setting control signal provided to the circuit; and the plurality of semiconductor data chips

being installed on the circuit board of the interface circuit during the initial boot the system outside of the semiconductor memory chips through in order to provide an initial value, the initial value storage for recognition memory module characterized in that having a.

3.

A memory module for mounting a memory test equipment for testing of the attached test; b) the initial value from the memory module; c) to read the information in response to the information, the read initial value; d) test memory module to initialize the memory module to the initialized for testing method comprising: providing a test mode setting information; e) a plurality of memory chip mounted on the memory module, in response to the test mode, the test mode corresponding to the setting

information set; f) to test the memory module to set test mode; g) setting information provided by the memory module, while the test mode to change the mode of operation to repeat steps d to f detects the optimal setting information characterized in that it comprises the step of testing a semiconductor memory module.

4.

According to claim 3, wherein the test memory modules are mounted on the inside by fusing a plurality of memory chips are in a test mode, further comprising the step of the program, characterized in that the semiconductor memory module test method.

14.

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Title: 半導体回路
Semiconductor circuit

Claims:

1. 複数のマスク層を用いて製造される半導体回路であって、複数のメモリセルと、複数の出力回路と、複数の周辺回路と、外部プラス電源電圧を受け取るための第１の外部パッドであり、該外部プラス電源電圧のレベルが第１の動作電圧範囲と第２の動作電圧範囲のうちのいずれか１つにあり、該第２の動作電圧範囲が該第１の動作電圧範囲より高いものと、外部接地電源電圧を受け取るための第２の外部パッドと、前記メモリセルのための第１の出力電圧を生成するための第１の電圧レギュレータと、前記周辺回路のための第２の出力電圧を生成するものであり、第１の出力トランジスタと、第２の出力トランジスタと、前記第２の出力電圧の低下に応答して前記第１の出力トランジスタを起動する第１の回路と、前記第１の動作電圧範囲で前記外部プラス電源電圧の前記レベルに応答して前記第２の出力トランジスタを起動する第２回路とを備える第２の電圧レギュレータとを有し、前記外部プラス電源電圧のレベルを前記第１の動作電圧範囲内で動作させようとする場合には、前記第２の電圧レギュレータにおける前記第１および第２の出力トランジスタを短絡させ

1. A semiconductor circuit manufactured using a plurality of mask layers, and a plurality of memory cells, a plurality of output circuits, a plurality of peripheral circuits, is the first external pad for receiving an external positive power supply voltage, is in the level of the external positive power supply voltage one of a first operating voltage range and the second operating voltage range, the second operating voltage range and is higher than the operating voltage range of the first and second external pads for receiving an external ground power supply voltage, the first for generating a first output voltage for said memory cells a voltage regulator, it is intended to produce a second output voltage for the peripheral circuits, a first output transistor, wherein in response to the second output transistor, the decrease of the second output voltage The includes a first circuit for activating the first output transistor, and a second circuit for starting said second output transistors in response to said level of said external positive power supply voltage at the first operating voltage range and a second voltage regulator, the level of the external positive power supply voltage when it is intended to operate in the first operating voltage range, said first and second output of the second voltage regulator The first

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る第１のマスク層が用いられ、前記外部プラス電源電圧のレベルを前記第２の動作電圧範囲内で動作させようとする場合には、第２のマスク層が用いられ、前記外部プラス電源電圧のレベルが前記第１の動作電圧範囲にある場合に、前記外部プラス電圧レベルの変動にもかかわらず前記第１の出力電圧のレベルが略一定であり、前記第２の出力トランジスタが起動されて前記第２の出力電圧が前記第２の出力トランジスタを介して前記外部プラス電源電圧に接続されるようにし、前記外部プラス電源電圧のレベルが前記第２の動作電圧範囲内である時に、前記外部プラス電圧のレベルの変動にもかかわらず前記第１および第２の出力電圧のレベルが略一定であり、前記第２の出力トランジスタがイネーブルされず、前記第２の出力電圧が、前記第２の出力電圧の低下に応答して前記第１の出力トランジスタを介して前記プラス電源電圧に選択的に接続されるようにすることを特徴とする半導体回路。

2. 請求項１記載の半導体回路であって、前記メモリセルの各々がコンデンサを有し、該コンデンサの格納電圧が前記外部接地電源電圧のレベルまたは前記第１の出力電圧のレベルのいずれかであることを特徴とする半導体回路。

3. 請求項１または２記載の半導体回路であって、前記第１および第２のマスク層に関して、前記メモリセルと、前記出力回路と、前記周辺回路とが同一であることを特徴とする半導体回路。

4. 出力電圧と出力電流を生成する半導体回路であって、外部電源に接続され、電圧および電流を供給する第１のプラス電源と、内部電源に接続され、電圧および電流を供給する第２のプラス電源と、振動電圧を受け取る入力端子と、前記振動電圧、前記第１のプラス電源電圧、および、前記第２のプラス電源電圧を受け取り、前記出力電圧を操作する電圧ポンピング回路とを備え、前記出力電圧が前記第１および第２のプラス電源の両方の電圧よりも大きく、かつ前記出力電流が前記第１および第２のプラス電源の電流から供給されることを特徴とする半導体回路。

mask layer is used to short the transistors, when it is intended to operate the level of the external positive power supply voltage in said second operating voltage range, the second mask layer is used, the outer If the level of the positive power supply voltage is in said first operating voltage range, the level of variability despite the first output voltage of the external positive voltage level is a substantially constant, said second output transistor The start has been to as the second output voltage is connected to the external positive power supply voltage through the second output transistor, when the level of the external positive power supply voltage is within the second operating voltage range the level of the level variation despite the first and second output voltages of the external positive voltage is a substantially constant, not the second output transistor is enabled, the second output voltage, the semiconductor circuit is characterized in that to be selectively connected to the positive power supply voltage through the responsive first output transistor to a decrease in the second output voltage.

2. The semiconductor circuit according to claim 1, wherein each memory cell has a capacitor storing a voltage of the capacitor is the external ground Semiconductor circuit, characterized in that it is one of the level of the or the first output voltage of the power supply voltage.

3. The semiconductor circuit according to claim 1, wherein, with respect to the first and second mask layers, and the memory cell, and the output Semiconductor circuit, characterized in that the circuit, and the said peripheral circuits are identical.

4. A semiconductor circuit for generating an output voltage and output current, it is connected to an external power source, the first positive power supply for supplying voltage and current If, connected to the internal power supply, a second positive power supply for supplying voltage and current, an input terminal for receiving an oscillating voltage, said oscillating voltage, said first positive power supply voltage, and the second of the positive power supply voltage The accepts, a voltage pumping circuit for operating the output voltage greater than the voltage of both of the output voltages of the first and second positive power supply and the output current of the first and second plus semiconductor circuit,

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5. 請求項４記載の半導体回路であって、前記出力電流の半分以上が前記第１のプラス電源から供給されることを特徴とする半導体回路。

6. 請求項４または５記載の半導体回路であって、さらに、２つの端子を有する結合コンデンサと、ゲート、ソースおよびドレインを有する第１のＮＭＯＳトランジスタであって、前記ゲートは前記結合コンデンサの第１の端子に接続され、前記ドレインは前記出力電圧を駆動する第１のＮＭＯＳトランジスタとを有し、前記ゲートは前記第２のプラス電源の電圧の３倍の電圧レベルに達し、前記ドレインは、出力電圧を前記第１および前記第２のプラス電源の電圧の和に等しいレベルまで駆動することを特徴とする半導体回路。

7. 請求項６記載の半導体回路路であって、さらに、ゲート、ソースおよびドレインを有する第２のＮＭＯＳトランジスタと、ゲート、ソースおよびドレインを有するＰＭＯＳトランジスタであって、該ＰＭＯＳトランジスタの前記ゲートは前記第２のプラス電源に接続されているＰＭＯＳトランジスタとを有し、前記第２のＮＭＯＳトランジスタおよび前記ＰＭＯＳトランジスタの前記ドレインは前記結合コンデンサの第２の端子に接続され、それにより、前記結合コンデンサの前記第２の端子の電圧レベルが、前記第２のプラス電源電圧レベルの２倍にポンピングされることを特徴とする半導体回路路。

8. 請求項５記載の半導体回路であって、さらに、それぞれがゲートとソースを備えた複数のトランジスタを有し、それにより、各トランジスタのゲートおよびソースにまたがる電圧差が前記第１あるいは前記第２のプラス電源電圧のどちらをも超過しないことを特徴とする半導体回路。

9. メモリセルに対し第１および第２の電圧を供給するための半導体回路であって、該メモリセルは、ビットＨｉｇｈレベル電圧とビットＬｏｗレベル電圧との間で動作するビット線と、前記ビットＨｉｇｈレベル電圧あるいは前記ビットＬｏｗレベル電圧のいずれかを蓄えるためのコンデンサであって前記ビット線に接続可能な第１のプレートと電圧レギュレータの前記第２の電圧に接続さ

characterized in that it is supplied from the power supply current.

5. claim a semiconductor circuit of 4 , wherein the first positive power supply more than half of the output current semiconductor circuit, characterized in that it is supplied from a.

6. The semiconductor circuit of claim 4 or 5 , further comprising of two a coupling capacitor having a terminal, a gate, a first NMOS transistor having a source and a drain, said gate connected to a first terminal of the coupling capacitor, the drain the first of which drives the output voltage and a NMOS transistor, the gate is reached three times the voltage level of the voltage of the second positive power supply, the drain is equal to the output voltage to a sum of said first and said second voltage of the positive power supply Semiconductor circuit according to claim to be driven to the level.

7. claim 6 a semiconductor circuit path, further comprising a gate, the second of which has a source and a drain and an NMOS transistor, a gate, and a PMOS transistor having a source and a drain, the gate of the PMOS transistor and a PMOS transistor connected to the second positive power supply, the second NMOS transistor and the The drain of the PMOS transistor is connected to a second terminal of the coupling capacitor, whereby the voltage level of the second terminal of the coupling capacitor, is pumped to two times the second positive power supply voltage level Semiconductor circuit paths, characterized in that.

8. a semiconductor circuit of claim 5 , further comprising a plurality of transistors, each including a gate and source barbed, thereby a semiconductor circuit of the voltage difference across the gate and source of each transistor is characterized in that not exceed neither of the first or the second positive power supply voltage.

9. The semiconductor circuit for supplying first and second voltages to the memory cell, the memory cell, the bit High-level voltage the bit and the bit line operating between the Low level voltage, the bit High-level voltage or the bit Low level first plate and the voltage in a capacitor connectable to said bit lines for storing any voltage and a capacitor and a second plate connected to the second voltage regulator, the voltage regulator, the first intermediate level between the bit High-level voltage and the bit Low-level voltage

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れた第２のプレートとを備えたコンデンサを有し、該電圧レギュレータは、前記ビットＨｉｇｈレベル電圧と前記ビットＬｏｗレベル電圧との中間のレベルの前記第１の電圧を生成する手段と、前記第１の電圧と前記ビットＬｏｗレベル電圧との中間のレベルの前記第２の電圧を生成する手段とを有することを特徴とする半導体回路。

10. 請求項９記載の半導体回路において、前記第１および第２の回路が、カスケードに接続された第１および第２の半電圧レギュレータをそれぞれ有し、前記第１の半電圧レギュレータが、前記ビットＨｉｇｈレベル電圧および前記ビットＬｏｗレベル電圧により供給されて前記第１の電圧を生成させるようにし、前記第２の半電圧レギュレータが、前記第１の電圧および前記ビットＬｏｗレベル電圧により供給されて前記第２の電圧を生成させるようにすることを特徴とする半導体回路。

11. 請求項１０記載の半導体回路において、前記第１の半電圧レギュレータは前記第１および第２の電圧の両方を供給し、該第２の電圧は前記第２のプレートの電圧を上昇させることを特徴とする半導体回路。

12. 請求項９～１１のいずれか１項に記載の半導体回路であって、さらに、初期動作の間に、前記第２の電圧を生成させる手段を助けるためのプルアップ回路を有することを特徴とする半導体回路。

13. 出力電圧および出力電流を生成する半導体回路であって、外部電源に接続され、電圧および電流を供給する第１のプラス電源と、内部電源に接続され、電圧および電流を供給する第２のプラス電源と、２つの端子を有する結合コンデンサと、前記結合コンデンサの第１の端子に接続されたゲート、および、ソース、および、前記出力電圧を操作するために接続されたドレインを有する第１ＮＭＯＳトランジスタとを備え、前記出力電圧が前記第１および第２のプラス電源電圧より大きく、前記出力電流が前記第１および第２のプラス電源電流から供給され、前記ゲートが、前記第２のプラス電源電圧の３倍の電圧レベルに達し、前記ドレインが、前記第１および第２のプラス電源

semiconductor circuit, characterized by comprising means for generating a voltage, and means for generating the first voltage and the second voltage of the intermediate level between the bit Low-level voltage.

In

10. Claim 9 a semiconductor circuit, wherein said first and second circuits, connected in a cascade and a first and second half-voltage regulator, respectively, the first half voltage regulator, said supplied by the bit High-level voltage and said bit Low-level voltage so as to generate said first voltage, and wherein a semiconductor circuit in which the second half-voltage regulator, characterized in that as supplied to generate the second voltage by the first voltage and the bit Low-level voltage.

11. claim in 10 semiconductor circuit of, wherein the first half voltage regulator is the first and second Semiconductor circuit supplies both voltages, the voltage of the second is characterized by raising the voltage of the second plate.

And met at the

12. claim 9 ~ semiconductor circuit according to any one of 11 Te, In addition, during the initial operation, the semiconductor circuit characterized by having a pull-up circuit to assist means for generating the second voltage.

13. A semiconductor circuit for generating an output voltage and output current are connected to an external power source, a first positive power supply for supplying voltage and current If, connected to the internal power supply, a second positive power supply for supplying voltage and current, a coupling capacitor having two terminals, a first gate connected to a terminal of the coupling capacitor, and, and a source, and a third 1NMOS transistor having a drain connected to manipulate the output voltage, the output voltage is greater than said first and second positive power supply voltage, the output current of the first and second plus is supplied from the supply current, the gate is reached three times the voltage level of the second positive power supply voltage, the drain, operates the output voltage to a level equal to the sum of said first and second positive power supply voltage Semiconductor circuit according to claim to be.

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電圧の合計に等しいレベルまで出力電圧を操作することを特徴とする半導体回路。

14. 請求項１３記載の半導体回路であって、さらに、ゲート、ソース、およびドレインを有するＮＭＯＳトランジスタと、前記第２のプラス電源に接続されたゲート、および、ソース、および、ドレインを有するＰＭＯＳトランジスタとを更に備え、前記第２のＮＭＯＳトランジスタと前記ＰＭＯＳトランジスタとのドレインが、前記結合コンデンサの前記第２の端子に接続され、前記結合コンデンサの前記第２の端子における電圧レベルが、前記第２のプラス電源電圧の２倍にポンピングされるようにすることを特徴とする半導体回路。

14. A semiconductor circuit as claimed in claim 13, further comprising an NMOS transistor having a gate, a source, and a drain said second gate connected to the positive power source, and, a source, and further includes a PMOS transistor having a drain, a drain of said second NMOS transistor and the PMOS transistor, wherein the coupling capacitor first It is connected to the two terminals, the semiconductor circuit of the voltage level at the second terminal of the coupling capacitor, characterized in that to be pumped to twice the second positive power supply voltage.

Description:

【０００１】
【発明の属する技術分野】
本発明は、一般的に半導体設計技術に関し、特に、異なる外部プラス電源電圧レベルで動作できる半導体回路において内部電圧電源を調整するためのシステムおよび方法に適用して有効な技術に関するものである。

[0001]
BACKGROUND OF THE INVENTION
The present invention relates generally to semiconductor design technology, and more particularly to a technique effectively applied to a system and method for adjusting the internal voltage supply in a semiconductor circuit that can operate with different external positive power supply voltage level.

【０００２】
【従来の技術】
多くの技術的進歩によって、集積回路、すなわち「チップ」は単一のモノリシックデバイス上に数百万ものトランジスタを組み込んだものとなっている。それにより、速度の向上およびサイズの減少をはじめとして、多くの利益が得られている。しかし、トランジスタの数が多くなるにつれ、チップ速度、消費電力、信頼性がより関心を引くようになっている。その結果、多くのチップについて外部プラス電源電圧は低下してきている。例えば、従来の１６Ｍビットダイナミックランダムアクセスメモリ（ＤＲＡＭ）は5.０Ｖか3.３Ｖの外部プラス電源を用いているが、２５６ＭビットＤＲＡＭでは3.３Ｖか2.５Ｖの外部プラス電源を用いている。低い外部プラス電源電圧を用いるとＤＲＡＭの速度を遅くさせるかもしれないが、消費電力は減少できる。さらに、薄いトランジスタのゲートや薄いメモリセルの誘電体に非常に高い電界強度を加えることにより引き起こされる破壊等

[0002]
BACKGROUND OF THE INVENTION
By a number of technological advances, integrated circuit, or "chip" has become one incorporating the transistor of millions on a single monolithic device. As a result, including the improvement and reduction in the size of the speed, a lot of profit is obtained. However, as the number of transistors increases, chip rate, power consumption, reliability is adapted to draw more attention. As a result, the external positive power supply voltage for a number of chips has been reduced. For example, a conventional 16M-bit dynamic random access memory (DRAM) but are using an external positive power supply of 5.0V or 3.3V, I'm using an external positive power supply of 3.3V or 2.5V at 256M bit DRAM. Lower external plus the use of a power supply voltage when it may be slow the DRAM speed of, but the power consumption can be reduced. Furthermore, it is possible to reduce the reliability problems of destruction caused by applying a very high electric field strength in the

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の信頼性の問題を減少させることもできる。

【０００３】

ＤＲＡＭの外部プラス電源電圧をユーザーが選択可能とする傾向も１６ＭＤＲＡＭ以来存在している。図１ａおよび図１ｂを参照すると、従来の１６ＭビットＤＲＡＭには、５Ｖの外部プラス電源（ＶＤＤ）に接続された５Ｖバージョンデバイス１０ａと、3.３ＶのＶＤＤに接続された3.３Ｖバージョンデバイス１０ｂが存在する。両方のバージョン１０ａ、１０ｂとも接地電位の外部電源（ＶＳＳ）にも接続されている。多くの部分に関して５Ｖバージョンデバイス１０ａと3.３Ｖバージョンデバイス１０ｂは同一である。しかし、５Ｖバージョンデバイス１０ａにおいては、電圧レギュレータ１２はＶＤＤ電圧を、メモリセルおよび周辺回路１３ａのために約3.３Ｖの内部電圧レベル（ＶＩＮＴ）に調整している。

【０００４】

ＶＩＮＴは、ＤＲＡＭのメモリセルアレイの小さなメモリセル回路を動かすため、また、ＤＲＡＭの消費電力を減少させるために、比較的低電圧でなければならない。しかし、出力回路１３ｂはより高いＶＤＤ電圧で動作する。このようにして、出力回路１３ｂの速度は増強され、出力回路は所望の電圧レベルで動作する。一方、3.３Ｖバージョンデバイス１０ｂの場合は、3.３Ｖは既に外部プラス電源ＶＤＤによって供給されている。従って、3.３Ｖバージョンデバイス１０ａの場合、外部プラス電源電圧が既にＶＩＮＴあるいはそれに近い電圧であるため、メモリセルアレイおよび周辺回路１３ａと出力回路１３ｂは同じＶＤＤ電圧レベルで動作するので、５Ｖバージョンデバイス１０ａのレギュレータ１２のようなレギュレータは存在しない。

【０００５】

外部プラス電源が選択可能なチップに対する要求を満たすために、チップの設計はマスタスライス技術を採用する。チップを設計する際、多くのマスク層からなるマスクセットが作られる。マスク層はチップを製造する際に用いられるフォトマスクのことを示す。例えば、米国特許５，４８９，５０９に記載されているフォトマスクを用いて半導体装置を製造する方法がある。マスタスライス技術では、チップの各バージョンを製造するため

dielectric of the gate and a thin memory cell of a thin transistor.

[0003]

Tend to the external positive power supply voltage of DRAM and user-selectable has also existed since 16MDRAM. Referring to Figures 1a and 1b, the conventional 16M-bit DRAM, and 5V version devices 10a which are connected to an external positive power supply (VDD) of 5V, and 3.3V version device 10b that are connected to the VDD of 3.3V but it exists. Both versions 10a, and is connected to an external power source (VSS) of 10b with ground. 5V version device 10a and the 3.3V version device 10b is the same for many parts. However, in the 5V version device 10a, voltage regulator 12 so as to adjust the VDD voltage, to the internal voltage level of about 3.3V for the memory cell and the peripheral circuit 13a (VINT).

[0004]

VINT is therefore moves the small memory cell circuit of the memory cell array of a DRAM, also, in order to reduce the power consumption of the DRAM, must be a relatively low voltage. However, the output circuit 13b to operate at a higher voltage VDD. Thus, the speed of the output circuit 13b is enhanced, and the output circuit operates at a desired voltage level. On the other hand, in the case of the 3.3V version device 10b, 3.3V has already been supplied by an external positive power supply VDD. Thus, for 3.3V version device 10a, since an external positive power supply voltage is already VINT or voltage close to it, since the memory cell array and the peripheral circuit 13a and the output circuit 13b operates in the same VDD voltage level, 5V version devices 10a the regulator is not present, such as the regulator 12.

[0005]

To external positive power supply to meet the demand for selectable chip, chip design to adopt the master slice technology. When designing a chip, a mask set consisting of a number of the mask layer is made. Mask layer indicates that a photomask used in the production of chips. For example, there is a method of manufacturing a semiconductor device using the photomask described in US patent 5,489,509. In the master-slice technology, the mask layers used to produce the various versions of the chips are all, except only one equivalent. Referring again to Figure 1,

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に用いられるマスク層は１つだけを除いてすべて同じとされている。図１を再び参照すると、５Ｖバージョンデバイス１０ａは、ＶＤＤをレギュレータ１２に向かわせ、調整された電圧を対応する回路に向かわせる配線１２ａを含む第１の配線層が形成されている。一方、3.３Ｖバージョンで１０ｂでは、ＶＤＤ電圧を直接対応する回路に向かわせる配線１２ｂを含む第２の配線層が形成されることになる。

【０００６】

【発明が解決しようとする課題】

ところが、このような単純なマスタスライス技術は２５６ＭビットＤＲＡＭでは同じようには有効でない。２５６ＭビットＤＲＡＭのメモリセルで用いられる誘電体は、誘電漏れ特性とメモリセルの安定性とをバランスさせる非常に小さな内部電圧を必要とするのに対して、周辺回路は、速度と消費電力をバランスさせる他の内部電圧を要求する。さらに、付加的な電圧レギュレータも必要とされるが、その各々はそれぞれに関し多くの設計上の問題を有している。例えば、電圧レギュレータに対する外部プラス電源が非常に低い場合、レギュレータが有効な電流出力を供給することは困難である。また、外部プラス電源が高い場合には、チャージポンプ電圧レギュレータのノードのいくつかが極端に高い電圧に達することがあり、信頼性の問題を引き起こす。最後の点として、従来の電圧レギュレータは、出力電圧を一定のレベルに維持するように出力電圧を充放電することができない。

【０００７】

本発明の目的は、多くの異なる外部プラス電圧に対して出力が一定である電圧レギュレータを複数備えた回路およびそのための方法を提供することにある。

【０００８】

本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

【０００９】

【課題を解決するための手段】

本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、以下のとおりである。

5V version device 10a will directs VDD to the regulator 12, a first wiring layer including a wiring 12a for directing to the corresponding circuit of the regulated voltage is formed. On the other hand, in the 10b at 3.3V version, so that the second wiring layer including a wiring 12b which directs to the circuit corresponding to the VDD voltage directly formed.

[0006]

[Invention Problems to be Solved]

However, such a simple master slice technology is not effective in the same way in the 256M-bit DRAM. 256M-bit DRAM dielectric used in the memory cell body is balanced against to require a very small internal voltage to balance and stability of the dielectric leakage characteristics and memory cell, the peripheral circuit, the power consumption and speed and requests the other internal voltages to be. Furthermore, although additional voltage regulators may be required, each of which has a number of design problems relates respectively. For example, if the external positive power supply for the voltage regulator very low, it is difficult for the regulator is to supply a valid current output. Also, when the external positive power is high, sometimes some nodes of the charge pump voltage regulator reaches extremely high voltage, causing reliability problems. As a final point, conventional voltage regulators can not output voltage is charged and discharged to maintain the output voltage at a constant level.

[0007]

An object of the present invention is to provide a number of circuit outputs to an external positive voltage has a plurality of the voltage regulator is constant different and a method therefor.

[0008]

The above and other objects and novel features of the present invention will be apparent from the description of this specification and the accompanying drawings.

[0009]

In order to solve the problem]

Among the inventions disclosed in the present application will be briefly described an overview of the typical things, it is as follows.

[0010]

That is, in the preferred embodiment of the present invention, by employing a master-slice technology,

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【００１０】
すなわち、本発明の好適な実施形態においては、マスタスライス技術を採用することにより、電圧レギュレータは２つの異なる範囲の外部プラス電源電圧に適応することができる。以下、４種類のレギュレータ技術を開示する。第１の電圧レギュレータの場合、レギュレータの電流供給能力は、外部プラス電源電圧が非常に低い状態下においてもかなり増大されている。第２のチャージポンプ電圧レギュレータの場合には、レギュレータの任意のノードにおける電圧レベルは予め定められた高電圧レベルを超えることはなく、しかも、外部プラス電源からの電流のほとんどを下げる。第３の電圧レギュレータは、その出力電圧を充放電して、出力電圧を一定のレベルに維持することができる。最後に、第４の電圧レギュレータは、誘電漏れを減少させるように最適化されたものである。

【００１１】
【発明の実施の形態】
以下、本発明の実施の形態を図面に基づいて詳細に説明する。

【００１２】
上述したように、図１ａおよび図１ｂは従来の１６Ｍビットダイナミックランダムアクセスメモリ（ＤＲＡＭ）デバイスの５Ｖバージョンデバイス１０ａおよび3.３Ｖバージョンデバイス１０ｂをそれぞれ示すものである。

【００１３】
図２ａおよび図２ｂを参照すると、参照番号２０ａおよび２０ｂは本発明の一実施形態のデバイスの3.３Ｖバージョンおよび2.５Ｖバージョンをそれぞれ全体として示すものである。本発明の好適な実施形態では、3.３Ｖバージョンデバイス２０ａおよび2.５Ｖバージョンデバイス２０ｂは２５６ＭビットＤＲＡＭであるが、本発明はＤＲＡＭへの適用に限定されることはなく、異なる内部電源レベルを必要とする外部プラス電源を選択可能な任意の集積回路デバイス、例えば、プログラマブル論理アレイや他のタイプのランダムアクセスメモリ等に関連して適用することができる。さらに、好適な実施形態において列挙された電圧レベルは例示のためのものであって、本発明を限定するものではない。

the voltage regulator may be adapted to an external positive power supply voltage of the two different ranges. The following, we will disclose the four types of regulator technology. For the first voltage regulator, a current supply capability of the regulator is increased much even under very external positive power supply voltage low. In the case of the second charge pump voltage regulators, voltage level at any node in the regulator does not exceed the high voltage level that is determined in advance, moreover, to reduce the most of the current from the external positive power supply. The third voltage regulator, the output voltage by charging and discharging, can maintain the output voltage at a constant level. Finally, the fourth voltage regulator is one that is optimized to reduce dielectric leakage.

[0011]
DETAILED DESCRIPTION OF THE INVENTION
It will be described in detail with reference to embodiments of the present invention with reference to the drawings.

[0012]
As mentioned above, FIGS. 1a and 1b shows a 5V version devices 10a and 3.3V version device 10b of a conventional 16M-bit dynamic random access memory (DRAM) devices, respectively.

[0013]
Referring to FIGS. 2a and 2b, reference numeral 20a and 20b shows a 3.3V version and 2.5V version of the device of an embodiment of the present invention as a whole, respectively. In a preferred embodiment of the present invention, the 3.3V version devices 20a and 2.5V version device 20b is a 256M bit DRAM, the present invention is not limited to the application to the DRAM, the different internal power supply level It requires an external positive power supply can be selected for any integrated circuit device, for example, can be applied in connection with the random access memory of the programmable logic array or other type. Furthermore, the voltage level listed in the preferred embodiment is for the purpose of illustration and are not intended to limit the present invention.

[0014]
3.3V version device 20a and the 2.5V version device 20b receives the external ground power supply (VSS) of the external positive power supply (VDD) 0V (ground potential), but, VDD voltage

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【００１４】
3.３Ｖバージョンデバイス２０ａおよび2.５Ｖバージョンデバイス２０ｂは外部プラス電源（ＶＤＤ）と０Ｖ（接地電位）の外部接地電源（ＶＳＳ）を受け取るが、ＶＤＤ電圧は3.３Ｖバージョンデバイス２０ａに関しては標準値が3.３Ｖ、2.５Ｖバージョンデバイス２０ｂに関しては標準値が2.５Ｖであり、ＶＳＳ電圧は両方のデバイスに関して０Ｖ（接地電位）である。3.３Ｖバージョンデバイス２０ａと2.５Ｖバージョンデバイス２０ｂはほとんどの部分が同一であり、どちらもそれぞれの周辺回路２１ａ、出力回路２１ｂ、およびメモリセルアレイ２１ｃを有している。さらに、両方のバージョンデバイス２０ａ、２０ｂとも、約2.０Ｖのアレイ電圧（ＶＡＲＹ）をメモリセルアレイ２１ｃに供給する第１の電圧レギュレータ回路２２および第２の電圧レギュレータ回路２４を有している。しかし、3.３Ｖバージョンデバイス２０ａの場合には、第２の電圧レギュレータ２４が約2.５Ｖの内部電圧（ＶＰＥＲＩ）を周辺回路２１ａへ供給している。

【００１５】
電圧レギュレータ２２、２４は様々な目的のために用いられる。まず第１に、メモリセルアレイ２１ｃのメモリセルで用いられる薄い（３－４ｎｍ）誘電体を動作させるためにＶＡＲＹは非常に低く、また、安定していなければならない。ＶＡＲＹをそのように低くすることによりリーク電流特性は最小に保たれ、同時にメモリセルの高い安定性を維持することができる。第２の点として、周辺回路２１ａが含むトランジスタはゲートの厚さ（９－１０ｎｍ）がメモリセルの誘電体の厚さ（３－４ｎｍ）より厚いので、ＶＰＥＲＩはＶＡＲＹより高い電圧をとることが可能である。周辺回路２１ａの回路の数は比較的多いが、ＶＰＥＲＩを中間の電圧（ＶＡＲＹ＜ＶＰＥＲＩ＜ＶＤＤ）とすることにより、それら回路による消費電力をそれほど増大させることなく、周辺回路２１ａの動作速度を向上させることができる。出力回路２１ｂはＶＤＤ電圧で動作する。このようにして、出力回路２１ｂの動作速度は増大し、出力信号の電圧レベルは所望の動作レベルとすることができる。また、出力回路の消費電力はＶＤＤが高い電圧であるために増加するが、出力回路２１ｂ

standard value with respect to 3.3V version device 20a but 3.3V, a standard value is 2.5V with respect to 2.5V version device 20b, VSS voltage is 0V (ground potential) with respect to both devices. 3.3V version device 20a and the 2.5V version device 20b is the same for the most part, I have both each of the peripheral circuit 21a, the output circuit 21b, and the memory cell array 21c. In addition, both versions device 20a, both 20b, it has a first voltage regulator circuit 22 and the second voltage regulator circuit 24 for supplying array voltage of about 2.0V to (VARY) to the memory cell array 21c. However, in the case of 3.3V version device 20a, the second voltage regulator 24 is supplying the internal voltage of about 2.5V to (VPERI) to the peripheral circuit 21a.

[0015]
Voltage regulator 22, 24 are used for a variety of purposes. First 1, VARY in order to operate a thin to be used in the memory cells of the memory cell array 21c (3-4nm) dielectric is very low, also, it must be stable. Leakage current characteristics by so low VARY is kept to a minimum, it is possible to simultaneously maintain a high memory cell stability. As a second point, the transistor the thickness of the gate to the peripheral circuits 21a includes (9-10nm) is larger than the thickness of the dielectric of the memory cells (3-4nm), VPERI is to take a higher voltage than the VARY possible it is. The number of circuits of the peripheral circuit 21a is relatively large, by making the intermediate voltage VPERI (VARY <vperi <vdd), without increasing the power consumption by these circuits too, and increase the operation speed of the peripheral circuit 21a and it can be. output circuit 21b operates in the vdd voltage. thus, the operation speed of the output circuit 21b increases, the voltage level of the output signal can be a desired operating level. in addition, the power consumption of the output circuit is increased to vdd is a high voltage, due to the relatively small number of circuits in the output circuit 21b, a power consumption is acceptable range.

[0016]
On the other hand, in the case of 2.5V version device 20b, since the VDD voltage (2.5V) is equal to VPERI (2.5V), the second voltage regulator 24 of FIG. 2a is not required. Thus, 3.3V version device 20a is to use the first and second voltage regulators 22 and 24 for supplying respectively the VPERI and VARY, die for forming the first wiring

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の回路数が比較的少ないため、その消費電力は許容できる範囲である。

【００１６】

一方、2.５Ｖバージョンデバイス２０ｂの場合には、ＶＤＤ電圧（2.５Ｖ）がＶＰＥＲＩ（2.５Ｖ）に等しいので、図２ａの第２の電圧レギュレータ２４は必要ではない。従って、3.３Ｖバージョンデバイス２０ａが、ＶＰＥＲＩおよびＶＡＲＹをそれぞれ供給するための第１および第２の電圧レギュレータ２２、２４を用いるように、配線２４ａを含む第１の配線層を形成するための第１のマスク層（図示せず）を用いてマスタスライス技術を採用する。第１のマスク層の代わりに配線２４ｂを含む第２の配線層を形成するための第２のマスク層（図示せず）を用いることにより、2.５Ｖバージョンデバイス２０ｂが、やはりＶＡＲＹを供給するための第１の電圧レギュレータ２２を用いるようにすることができる。しかし、2.５Ｖバージョンデバイス２０ｂは第２の電圧レギュレータ２４は用いず、外部電源ＶＤＤが直接ＶＰＥＲＩとして供給される。

【００１７】

図３ａおよび図３ｂを参照すると、3.３Ｖバージョンおよび2.５Ｖバージョンの両方が、内部電圧ＶＡＲＹおよびＶＰＥＲＩの電圧調整に加えて、これとは別の内部電圧ＶＰＰ、ＶＢＢ、ＶＢＬＲおよびＶＰＬＴを生成し、用いている。ＶＰＰは3.６Ｖであってワード線ドライバに用いられ、ＶＢＢは－1.０Ｖで、様々なＮＭＯＳトランジスタのバックバイアスとして用いられ、ＶＢＬＲは1.０Ｖで、ビット線のプリチャージレベルとして用いられ、ＶＰＬＴは0.５Ｖで、メモリセルキャパシタのプレート電圧として用いられる。内部電圧ＶＡＲＹ、ＶＰＥＲＩ、ＶＰＰ、ＶＢＢ、ＶＢＬＲ、およびＶＰＬＴについては後で詳細に説明する。

【００１８】

特に、図３ａのブロック図を参照すると、このブロック図は図２ａの3.３Ｖバージョンデバイス２０ａに対応するものであるが、内部電圧ＶＡＲＹ、ＶＰＥＲＩ、ＶＰＰ、ＶＢＢ、ＶＢＬＲ、およびＶＰＬＴは、様々な電源線および信号線により相互に接続されている６個の電圧レギュレータ２６、２８、３０、３２、３４および３６により

layer including a wiring 24a employing a master-slice technology using one of the mask layer (not shown). By using the second mask layer (not shown) for forming a second wiring layer including a wiring 24b instead of the first mask layer, a 2.5V version device 20b, also supplies the VARY It is possible to make use of the first voltage regulator 22 for. However, 2.5V version device 20b and the second voltage regulator 24 is not used, the external power supply VDD is supplied directly as VPERI.

[0017]

Referring to Figures 3a and 3b, both 3.3V and 2.5V versions version, in addition to the voltage regulation of the internal voltage VARY and VPERI, generate another internal voltages VPP, VBB, VBLR and VPLT to this And we're using. VPP is used for a word line driver and a 3.6V, VBB is at -1.0V, and is used as a back bias for different NMOS transistors, VBLR at 1.0V, is used as a precharge level of the bit line, VPLT is.In 5V, it is used as the plate voltage of the memory cell capacitor. Internal voltage VARY, VPERI, VPP, VBB, VBLR, and I will be described in detail later VPLT.

[0018]

In particular, with reference to the block diagram of Figure 3a, but the block diagram corresponds to the 3.3V version device 20a in FIG. 2a, the internal voltage VARY, VPERI, VPP, VBB, VBLR, and VPLT the various is adjusted by which the six voltage regulators 26,28,30,32,34 and 36 which are interconnected by a power supply line and signal line. Intermediate voltage regulator 26, a first intermediate voltage V1, and the second intermediate voltage V2 generated, V1 voltage is 1.25V, V2 voltage is 1.0V. V1 is supplied to VPERI regulator 28, the regulator generates twice the voltage VPERI = 2.5V at V1, as described in more detail with reference to FIG. VPERI is also supplied to a conventional VBB regulator 34 and the VPP regulator 32, which will be described in detail with reference to Figure 7.

[0019]

Likewise, V2 is supplied to a VARY regulator 30, the regulator generates twice the voltage VARY = 2.0V of V2 as will be described in detail with reference to FIG. VARY is also supplied to the VBLR and VPLT regulator 36, which will be described in detail with reference to Figure 12.

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調整される。中間電圧レギュレータ２６は、第１の中間電圧Ｖ１および第２の中間電圧Ｖ２を生成し、Ｖ１電圧は1.２５Ｖであり、Ｖ２電圧は1.０Ｖである。Ｖ１はＶＰＥＲＩレギュレータ２８に供給され、このレギュレータは図６を参照して詳細に説明されるようにＶ１の２倍の電圧ＶＰＥＲＩ＝2.５Ｖを生成する。ＶＰＥＲＩはまた、従来のＶＢＢレギュレータ３４とＶＰＰレギュレータ３２に供給され、これについては図７を参照して詳細に説明する。

【００１９】

同様に、Ｖ２はＶＡＲＹレギュレータ３０に供給され、このレギュレータは図９を参照して詳細に説明するようにＶ２の２倍の電圧ＶＡＲＹ＝2.０Ｖを生成する。ＶＡＲＹはまた、ＶＢＬＲおよびＶＰＬＴレギュレータ３６に供給され、これについては図１２を参照して詳細に説明する。

【００２０】

図３ｂのブロック図を参照すると、このブロック図は図２ｂの2.５Ｖバージョンデバイス２０ｂに対応するものであり、内部電圧ＶＡＲＹ、ＶＰＥＲＩ、ＶＰＰ、ＶＢＢ、ＶＢＬＲ、およびＶＰＬＴが、図３ａを参照して上述したのと同様の方法で生成されるが、ＶＰＥＲＩが直接ＶＤＤにより供給される点だけが異なっている。

【００２１】

図３ａおよび図３ｂの両方を参照すると、それらの図に示された破線により、この好適な実施形態においてマスタスライス技術がどのように実現されているかが示されている。マスタスライス技術では、3.３Ｖバージョン（図３ａ）と2.５Ｖバージョン（図３ｂ）を製造するために、同一の金属配線層形成行程のための第１および第２のマスク層（図示せず）のどちらかを必要とする。3.３Ｖバージョンのための第１のマスク層は、第１の配線層を形成するために用いられ、2.５Ｖバージョンのための第２のマスク層は、第２の配線層を形成するために用いられる。このようにして、デバイスの目的に対応して、第１のマスク層または第２のマスク層のどちらかを用いる。

【００２２】

第１のマスク層は、3.３Ｖバージョン（図３ａ）で用いられるものであり、外部プラス電源ＶＤＤをＶＰＲＥＩに接続する図３ａに破線として示さ

[0020]
Referring to the block diagram of Figure 3b, the block diagram is intended to correspond to the 2.5V version device 20b in Figure 2b, the internal voltage VARY, VPERI, VPP, VBB, VBLR, and VPLT is, referring to Figure 3a and it is generated in a manner similar to that described above Te, only in that VPERI is fed by direct VDD is different.

[0021]
Referring to both FIGS. 3a and 3b, the broken lines shown in the figures, or the master-slice technology is how to implement is shown in the preferred embodiment. The master-slice technology, in order to produce 3.3V version (Fig. 3a) and 2.5V version (Fig. 3b), the first and second mask layers for the same metal wiring layer forming step (not shown It needs either). The first mask layer for 3.3V version is used to form the first wiring layer, the second mask layer for 2.5V version, in order to form a second wiring layer It used to. Thus, corresponding to the desired device, using either the first mask layer or the second mask layer.

[0022]
The first mask layer, and is intended to be used in 3.3V version (Fig. 3a), and without forming the wiring 40 shown as a dashed line in Figure 3a that connects the external positive power supply VDD to VPREI, the regulator 26, and it is used to form the first wiring layer including a wiring 42, 44 for interconnecting 28,30,32,34,36. Similarly, the second mask layer is intended to be used in 2.5V version (Fig. 3b), and without forming the wires 42 and 44 connecting the VPREI regulator 28, shown as a dashed line in Figure 3b, the regulator and it is used to form the second wiring layer including a wiring 40 interconnecting 26,28,30,32,34,36.

[0023]
Referring to Figure 4a, 3 one internal voltage VPP of 3.3V version (Fig. 3a), the VPERI and VARY is shown as a function of VDD. The first of the normal operating range of VDD 50 is between 3.3V plus or minus 10 percent, that is about 3.0V ~ 3.6V. In the first of the normal operating range 50, the internal voltage VPP, VPERI and VARY is constant at each 3.6V, 2.5V and 2.0V. In the first of the stress range 52 to be used in the VDD is reliability / burn-in test of more than 4.1V, the internal voltage VPP, VPERI and VARY varies with VDD voltage, VPP is equal to VDD, VPERI the VDD-0. equal to 75V, VARY is equal to VDD-1.5V.

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れている配線４０を形成せず、レギュレータ２６、２８、３０、３２、３４、３６を相互接続する配線４２、４４を含む第１の配線層を形成するために用いられる。同様に、第２のマスク層は、2.５Ｖバージョン（図３ｂ）で用いられるものであり、図３ｂに破線として示されているＶＰＲＥＩレギュレータ２８を接続する配線４２および４４を形成せず、レギュレータ２６、２８、３０、３２、３４、３６を相互接続する配線４０を含む第２の配線層を形成するために用いられる。

【００２３】

図４ａを参照すると、3.３Ｖバージョン（図３ａ）の３つの内部電圧ＶＰＰ、ＶＰＥＲＩおよびＶＡＲＹがＶＤＤの関数として示されている。ＶＤＤの第１の通常動作範囲５０は3.３Ｖ±１０％、すなわち約3.０Ｖ～3.６Ｖの間にある。第１の通常動作範囲５０において、内部電圧ＶＰＰ、ＶＰＥＲＩおよびＶＡＲＹはそれぞれ3.６Ｖ、2.５Ｖおよび2.０Ｖで一定である。ＶＤＤが4.１Ｖ以上の信頼性／バーンイン試験で用いられる第１のストレス範囲５２においては、内部電圧ＶＰＰ、ＶＰＥＲＩおよびＶＡＲＹはＶＤＤ電圧と共に変化し、ＶＰＰはＶＤＤに等しく、ＶＰＥＲＩはＶＤＤ－0.７５Ｖに等しく、ＶＡＲＹはＶＤＤ－1.５Ｖに等しい。パワーアップ動作あるいはバッテリバックアップ動作の際に用いられる、ＶＤＤが2.２Ｖ～2.７Ｖの間にある第１の低電圧範囲５３においては、ＶＡＲＹはやはり2.０Ｖであるが、ＶＰＥＲＩはＶＤＤに等しくする。最後に、やはりパワーアップの際に用いられるＶＤＤが2.２Ｖより小さな第２の低電圧範囲５４においては、ＶＡＲＹおよびＶＰＥＲＩの両方がＶＤＤに等しくする。

【００２４】

図４ｂを参照すると、2.５Ｖバージョン（図３ｂ）の３つの内部電圧ＶＰＰ、ＶＰＥＲＩおよびＶＡＲＹがＶＤＤの関数として示されている。ＶＤＤの第２の通常動作範囲５６は2.５Ｖ±１０％、すなわち約2.２５Ｖ～2.７５Ｖの間にある。第２の通常動作範囲５６の全体にわたって、内部電圧ＶＰＰおよびＶＡＲＹはそれぞれ3.６Ｖおよび2.０Ｖで一定であり、3.３Ｖバージョン（図４ａ）の場合と同じ電圧である。しかし、ＶＰＥＲＩはＶＤＤ電圧に等しいままである。ＶＤＤが3.２Ｖ

Used at the time of the power-up operation or battery backup operation, in the first of the low voltage range 53 VDD is between 2.2V ~ 2.7V, but VARY is still 2.0V, VPERI the VDD equal. Finally, still in the low voltage range 54 VDD is small second than 2.2V to be used during power-up, both of VARY and VPERI is equal to VDD.

[0024]

Referring to Figure 4b, 3 one internal voltage VPP of 2.5V version (Fig. 3b), the VPERI and VARY is shown as a function of VDD. The second of the normal operating range of VDD 56 is 2.5V plus or minus 10 percent, ie between about 2.25V ~ 2.75V. Throughout the second normal operating range 56, the internal voltages VPP and VARY are constant respectively 3.6V and 2.0V, which is the same voltage as in the 3.3V version (Fig. 4a). However, VPERI remains equal to the VDD voltage. In the VDD is big second stress range 58 than 3.2V, VPP is a VDD 0.75V, VPERI is equal to the VDD voltage, VARY is equal to VDD-0.75V. Finally, in a small third of the low-voltage range 60 than VDD is 2.2V, both of VARY and VPERI is equal to the VDD voltage.

[0025]

Referring to FIG. 5, in simplified essential part circuit diagram of the 3.3V version device 20a and the 2.5V version device 20b of 256M-bit DRAM, the internal voltage VARY, VPERI, VPP, VBB, VBLR, and VPLT the application of It is shown. Address signals (not shown) passes through an input port INPUT, is applied to the address buffer 62. The address buffer 62 operates in the VDD, the other chips (not shown) to match the interface. Address buffer 62 to drive to the address decoder 64 the address signal. While the address decoder 64 operates in VPERI, it is because VPERI to provide a good balance between the high speed (high voltage) and low power (low voltage). The address decoder 64 applies a decoder signal, the word line driver 66 operating at VPP.

[0026]

The word line driver 66 drives the word line WL, the word line WL for selecting the memory cell (bit) B1. Bit B1 has accumulated a bit voltage VSN located between the VARY (2.0V) and VSS (0V). The bit voltage VSN might be VARY, word line driver 66, plus the threshold voltage of the N-channel metal oxide semiconductor (NMOS) transistor 68 (not shown) to VARY, further, a change in the speed and the voltage and it

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より大きな第２のストレス範囲５８においては、ＶＰＰはＶＤＤ+0.７５Ｖであり、ＶＰＥＲＩはＶＤＤ電圧に等しく、ＶＡＲＹはＶＤＤ−0.７５Ｖに等しい。最後に、ＶＤＤが2.２Ｖより小さな第３の低電圧範囲６０においては、ＶＡＲＹおよびＶＰＥＲＩの両方がＶＤＤ電圧に等しい。

【００２５】

図５を参照すると、２５６ＭビットＤＲＡＭの3.３Ｖバージョンデバイス２０ａおよび2.５Ｖバージョンデバイス２０ｂの単純化された要部回路図において、内部電圧ＶＡＲＹ、ＶＰＥＲＩ、ＶＰＰ、ＶＢＢ、ＶＢＬＲ、およびＶＰＬＴの適用が示されている。アドレス信号（図示せず）は入力ポートＩＮＰＵＴを通過し、アドレスバッファ６２に印加される。アドレスバッファ６２はＶＤＤで動作し、他のチップ（図示せず）とインタフェイスを一致させる。アドレスバッファ６２はアドレス信号をアドレスデコーダ６４へと駆動する。アドレスデコーダ６４はＶＰＥＲＩで動作するが、それはＶＰＥＲＩが高速度（高電圧）と低消費電力（低電圧）との間の良好なバランスを提供するからである。アドレスデコーダ６４は、デコーダ信号を、ＶＰＰで動作するワード線ドライバ６６へ印加する。

【００２６】

ワード線ドライバ６６はワード線ＷＬを駆動し、ワード線ＷＬはメモリセル（ビット）Ｂ１を選択する。ビットＢ１は、ＶＡＲＹ（2.０Ｖ）とＶＳＳ（０Ｖ）との間にあるビット電圧ＶＳＮを蓄えている。ビット電圧ＶＳＮがＶＡＲＹとなるかもしれないので、ワード線ドライバ６６は、ＶＡＲＹにＮチャネル金属酸化物半導体（ＮＭＯＳ）トランジスタ６８の閾値電圧（図示せず）を足し、さらに、速度および電圧の変化を調節するための付加的な電圧を足したものより十分に高い電圧ＶＰＰで動作する。トランジスタ６８はＶＢＢにバイアスされたウェル６８Ｗを有しており、それによりトランジスタ６８のリーク電流（図示されていない）および接合容量（図示せず）が減少される。ビットＢ１はまた、キャパシタＣ１を含んでおり、キャパシタＣ１のプレートはＶＰＬＴに接続されている。ＶＰＬＴのレベルはＶＡＲＹとＶＳＳとの間にあり、キャパシタＣ１のリーク電流を最小にするように最適化されているが、これに

operates at a sufficiently high voltage VPP than those plus additional voltage to regulate. Transistor 68 has a biased wells 68W in VBB, whereby the leak current (not shown) and the junction capacitance of the transistor 68 (not shown) is reduced. Bit B1 also includes a capacitor C1, the plate of the capacitor C1 is connected to the VPLT. Level VPLT is between the VARY and VSS, although the leakage current of the capacitor C1 is optimized to minimize, as will be described in detail with reference to Figure 12 later.

[0027]

Bit B1 is connected to the bit voltage VSN read to the bit line BL, and the sense amplifier circuit 69. The sense amplifier circuit 69 includes an amplifier section 70 for amplifying a bit line signal voltage. Amplifier section 70 by the sense amplifier overdrive circuit 71 is driven via the signal line SDN and SDP. Overdrive circuit 71 receives the three drive signals SAP1, SAP2 and SAN, and drives the signal line SDN to VSS, selectively driven to either the VARY or VDD to SDP. VARY and VSS is the target voltage of High and Low, respectively for the bit line BL. At the time of the sense amplifier amplifying operation, VDD is used to overdrive the bit line BL SAP1 is only a short period of Low. Then SAP1 is High level, SAP2 becomes Low level, the final voltage of the bit line is VARY or zero. The sense amplifier circuit 69 also has an equalizer section 72 for precharging the bit line BL. The equalizer section 72, bit B1 is the bit line BL is controlled by VBLR and so as to signal BLEQ intermediate voltage between VARY and VSS before being selected by the word line WL.

[0028]

The amplified bit line voltage (not shown) is selectively connected to the output line I / O by the column select signal YS. Then, the output line I / O to drive the main amplifier 74. The main amplifier 74, for the same reason as that described above in relation to the address decoder 64 operates in VPERI. Finally, the main amplifier 74 is driving the output buffer 76, output buffer 76 for the same reason as that described above in connection with the input buffer 62 described above, operating at VDD.

[0029]

Referring to Figure 6, there is shown a VPERI regulator which is improved according to the

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ついては後で図１２を参照して詳細に説明する。
【００２７】
ビットＢ１はビット電圧ＶＳＮをビット線ＢＬに読み出し、そしてセンスアンプ回路６９に接続される。センスアンプ回路６９は、ビット線信号電圧を増幅するためのアンプセクション７０を備える。アンプセクション７０はセンスアンプオーバードライブ回路７１により、信号線ＳＤＮおよびＳＤＰを介して駆動されている。オーバードライブ回路７１は３つのドライブ信号ＳＡＰ１、ＳＡＰ２およびＳＡＮを受け取り、信号線ＳＤＮをＶＳＳへと駆動し、ＳＤＰをＶＡＲＹあるいはＶＤＤのどちらかへと選択的に駆動する。ＶＡＲＹおよびＶＳＳは、ビット線ＢＬに対するそれぞれＨｉｇｈおよびＬｏｗの目標電圧である。センスアンプ増幅動作時に、ＶＤＤはビット線ＢＬをＳＡＰ１がＬｏｗの短い期間だけオーバードライブするために用いられる。その後ＳＡＰ１がＨｉｇｈレベル、ＳＡＰ２がＬｏｗレベルになり、ビット線の最終電圧はＶＡＲＹ又はゼロとなる。センスアンプ回路６９はまた、ビット線ＢＬをプリチャージするためのイコライザセクション７２を有している。イコライザセクション７２は、ビットＢ１がワード線ＷＬにより選択される前にビット線ＢＬがＶＡＲＹとＶＳＳとの中間電圧のＶＢＬＲとなるように信号ＢＬＥＱにより制御される。
【００２８】
増幅されたビット線電圧（図示せず）は、列選択信号ＹＳにより選択的に出力線Ｉ／Ｏへと接続される。次いで、出力線Ｉ／Ｏはメインアンプ７４を駆動する。メインアンプ７４は、アドレスデコーダ６４に関連して先に説明したのと同じ理由で、ＶＰＥＲＩで動作する。最後に、メインアンプ７４は出力バッファ７６を駆動するが、出力バッファ７６は、前述の入力バッファ６２に関連して先に説明したのと同じ理由で、ＶＤＤで動作する。
【００２９】
図６を参照すると、3.３Ｖバージョン（図３ａ）において参照番号２８によって本発明による改善されたＶＰＥＲＩレギュレータが示されている。ＶＰＥＲＩレギュレータ２８は中間電圧Ｖ１（図３ａ）、ＶＤＤおよびＶＳＳと、ＡＣＴＶ信号およびＤＥＴＥＣＴ１Ｂ信号とを用いている。ＡＣ

invention by the reference numeral 28 in the 3.3V version (Fig. 3a). VPERI regulator 28 intermediate voltage V1 (Fig. 3a), are used and VDD and VSS, and the ACTV signal and DETECT1B signal. ACTV signal 3.3V version device 20a (Figure 2a) is a High level when the active state, 3.3V version device 20a is a Low level at the time of the stand-by mode. It is described as High level when ACTV signal is not specifically mentioned.

[0030]
Referring to FIGS. 7 and 8, than the reference number 82, the level conversion function with an inverter circuit 82 (FIG. 7), VDD external positive power supply VDD of the dependent DETECT1 signal and DETECT1B signal (Fig. 8) is shown. DETECT1B signal is generated by the level conversion function with the inverter circuit 82. The DETECT1B signal is applied to the gate of the pull-up PMOS transistor 90 of the VPREI regulator circuit 28 (Figure 6). Level conversion function with the inverter circuit 82 external positive power supply (VDD) voltage, are using VBB other to a negative voltage of the external ground power supply (VSS) voltage. Incidentally, VBB is the output voltage of the known back bias voltage generating circuit (not shown). Level conversion function with the inverter circuit 82 as input DETECT1 signal, and outputs the DETECT1B signal. Incidentally, DETECT1 signal is an output signal of the power supply voltage level sensor circuit (not shown). Power supply voltage level sensor circuit can be easily realized by a differential amplifier circuit for comparing the voltage with a constant reference voltage obtained by dividing a predetermined voltage dividing the VDD voltage. Then, it sets the first low-voltage range 53 (FIG. 8) up to the VDD voltage (VDD = 2.7V) divided voltage is the reference voltage at the equal way division ratio or the reference voltage in. Thus, higher if the divided voltage than the maximum VDD voltage of the external positive power supply (VDD) voltage is within a first low-voltage range 53 becomes higher than the reference voltage. It is lower than the VDD voltage maximum VDD voltage of the first low-voltage range 53 divided voltage becomes lower than the reference voltage. As a result of this comparison, the level conversion function with the inverter circuit 82 to convert the DETECT1 signal of the output signal of the differential amplifier circuit to DETECT1B signal. In other words, VDD voltage is normal operating range 50 (FIG. 4a or FIG. 8,3.0-3.6V) when, DETECT1 signal is 0V (ground

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ＴＶ信号は3.３Ｖバージョンデバイス２０ａ（図２ａ）が活性状態のときＨｉｇｈレベルであり、3.３Ｖバージョンデバイス２０ａが待機モードのときにＬｏｗレベルである。ＡＣＴＶ信号は特に言及されない場合にはＨｉｇｈレベルとして説明する。

【００３０】

図７および図８を参照すると、参照番号８２より、レベル変換機能付きインバータ回路８２（図７）と、ＤＥＴＥＣＴ１信号およびＤＥＴＥＣＴ１Ｂ信号のＶＤＤ外部プラス電源ＶＤＤの依存性（図８）が示されている。ＤＥＴＥＣＴ１Ｂ信号はレベル変換機能付きインバータ回路８２により生成される。このＤＥＴＥＣＴ１Ｂ信号は、ＶＰＲＥＩレギュレータ回路２８（図６）のプルアップＰＭＯＳトランジスタ９０のゲートに印加される。レベル変換機能付きインバータ回路８２は外部プラス電源（ＶＤＤ）電圧、外部接地電源（ＶＳＳ）電圧の他に負電圧のＶＢＢを利用している。なお、ＶＢＢは公知のバックバイアス電圧発生回路（図示せず）の出力電圧である。レベル変換機能付きインバータ回路８２はＤＥＴＥＣＴ１信号を入力とし、ＤＥＴＥＣＴ１Ｂ信号を出力とする。なお、ＤＥＴＥＣＴ１信号は電源電圧レベルセンサ回路（図示せず）の出力信号である。電源電圧レベルセンサ回路は，ＶＤＤ電圧の所定の電圧を分圧した電圧と一定の基準電圧とを比較する差動アンプ回路で容易に実現できる。そして、第１の低電圧範囲５３（図８）内の最大ＶＤＤ電圧（ＶＤＤ＝2.７Ｖ）でその分圧電圧が基準電圧と等しくなるように分圧比または基準電圧を設定する。このことから、外部プラス電源（ＶＤＤ）電圧が第１の低電圧範囲５３内の最大ＶＤＤ電圧よりも高ければ分圧電圧は基準電圧より高くなる。ＶＤＤ電圧が第１の低電圧範囲５３の最大ＶＤＤ電圧よりも低ければ分圧電圧は基準電圧より低くなる。この比較結果として、レベル変換機能付きインバータ回路８２は差動アンプ回路の出力信号のＤＥＴＥＣＴ１信号をＤＥＴＥＣＴ１Ｂ信号に変換する。つまり、ＶＤＤ電圧が通常動作範囲５０（図４ａまたは図８、3.０～3.６Ｖ）のとき、ＤＥＴＥＣＴ１信号は０Ｖ（接地電位）である。ＶＤＤ電圧が第１の低電圧範囲５３または第２の低電圧範囲５４（図４ａまたは図８、ＶＤＤ

potential). When the VDD voltage in the first low-voltage range 53 or the second low-voltage range 54 (Fig. 4a or FIG. 8, VDD ≦ 2.7V), DETECT1 signal is at the VDD voltage level. And when DETECT1 signal is 0V to (ground potential), DETECT1B signal is at the VDD voltage level. DETECT1 when the signal is of the VDD voltage level, DETECT1B signal becomes the VBB level. The benefit of such a DETECT1B signal has a low voltage level of VBB level (Fig. 8) will be described later.

[0031]
Referring to Figure 6, VPERI regulators 28 have a differential circuit 84, the voltage dividing circuit 86 and the first and second pull-up P-channel metal oxide semiconductor (PMOS) transistor 88 and a second pull-up PMOS transistor 90 are doing. Voltage divider 86 generates an output voltage 92, but the voltage is one-half of VPERI (typically 2.5V), that is, 1.25V. The half voltage reference method, there is a benefit of increasing the current supply capacity of low-VDD of the transistor 88. The output voltage 92 is compared with (a = 1.25V (Fig. 3a)) the intermediate voltage V1 by the differential circuit 84. VPERI also lowered output voltage 92 and lowered, the differential circuit 84 and further activate the first pull-up PMOS transistor 88, the first PMOS transistor 88 to recover towards the VPERI to 2.5V.

[0032]
Referring to Figure 4a, when the 3.3V version device 20a (FIG. 2a) is in the one of the first low-voltage range 53 and the second low-voltage range 54, the voltage level of the DETECT1B signal is equal to VBB, the 2 of the pull-up transistor 90 is also active. As a result, the second gate of the pull-up transistor 90 - (not shown) source voltage becomes very high, the current supply capability of the second pull-up PMOS transistor 90 can become high. So, over all of the first low-voltage range 53 and the second low-voltage range 54 VPERI is equal to the VDD voltage, this parallel addition of the first pull-up PMOS transistor 88 in parallel with the second pull-up transistor 90 and it is due to a high current driving capability due to the operation.

[0033]
Referring to both FIGS. 6 and 7, by their dashed line or have how been implemented by master-slice technology is shown in the preferred embodiment. The master-slice technology, the first

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≦2.７Ｖ）にあるとき、ＤＥＴＥＣＴ１信号はＶＤＤ電圧レベルである。そして、ＤＥＴＥＣＴ１信号が０Ｖ（接地電位）のとき、ＤＥＴＥＣＴ１Ｂ信号はＶＤＤ電圧レベルである。ＤＥＴＥＣＴ１信号がＶＤＤ電圧レベルのとき、ＤＥＴＥＣＴ１Ｂ信号はＶＢＢレベルとなる。このようにＤＥＴＥＣＴ１Ｂ信号がＶＢＢレベルという低い電圧レベル（図８）を有することの利益については後に説明する。

【００３１】

図６を参照すると、ＶＰＥＲＩレギュレータ２８は差動回路８４、分圧回路８６および第１および第２のプルアップＰチャネル金属酸化物半導体（ＰＭＯＳ）トランジスタ８８および第２のプルアップＰＭＯＳトランジスタ９０を有している。分圧回路８６は出力電圧９２を生成するが、その電圧はＶＰＥＲＩ（通常2.５Ｖ）の２分の１、すなわち1.２５Ｖである。この半電圧基準法は、トランジスタ８８の低ＶＤＤでの電流供給能力を増大させるという利益がある。出力電圧９２は差動回路８４により中間電圧Ｖ１（=1.２５Ｖである（図３ａ））と比較される。ＶＰＥＲＩが下降すると出力電圧９２も下降し、差動回路８４は第１のプルアップＰＭＯＳトランジスタ８８をさらにアクティブとし、第１のＰＭＯＳトランジスタ８８はＶＰＥＲＩを2.５Ｖに向けて回復させる。

【００３２】

図４ａを参照すると、3.３Ｖバージョンデバイス２０ａ（図２ａ）が第１の低電圧範囲５３および第２の低電圧範囲５４の１つにあるとき、ＤＥＴＥＣＴ１Ｂ信号の電圧レベルはＶＢＢに等しく、第２のプルアップトランジスタ９０もアクティブとされる。その結果、第２のプルアップトランジスタ９０のゲートーソース間電圧（図示せず）は非常に高くなり、第２のプルアップＰＭＯＳトランジスタ９０の電流供給能力は高いものとなり得る。それで、第１の低電圧範囲５３および第２の低電圧範囲５４のすべてにわたってＶＰＥＲＩはＶＤＤ電圧に等しく、これは第１のプルアップＰＭＯＳトランジスタ８８と並列な第２のプルアップトランジスタ９０の並列加算動作による高電流駆動能力によるものである。

【００３３】

図６および図７の両方を参照すると、それらの破

mask layer for 3.3V version (not shown) is used to form the first wiring layer excluding the wires, shown in dashed lines. The second mask layer for 2.5V version (not shown) is used to form the second wiring layer including a wiring indicated by the broken line.

[0034]
For 3.3V version, the first mask layer as VPREI regulator 28 can output a VPREI from the intermediate voltage V1, the wiring 28a, 28b (Fig. 6) shown by the broken line, and excluding 82a (FIG. 7) and it is used to form the first wiring layer. In the case of 2.5V version, the VPREI regulator second mask layer so as not to output VPREI from the intermediate voltage V1 includes wires 28a indicated by a dashed line, 28b (FIG. 6) and 82a (Fig. 7) and it is used to form the second wiring layer. As a result, it wants to be able to output a VDD (= 2.5V) voltage.

[0035]
To further improve the performance of VPERI regulator 28 in a relatively large size chip (Fig. 19), multi-regulator (19) is arranged in a different position around the tip. Thus, voltage drop caused by the wiring resistance of the long VPERI power line (not shown) is significantly reduced.

[0036]
Referring to Figure 9, a conventional VPP regulator is indicated by reference number 94. VPP regulator 94 is a power supply voltage 96 (which is connected to either VDD or VPERI), it uses the output voltage VOSC from VPP level sensor. Voltage regulator 94 generates a higher voltage VPP than the power supply voltage 96 by the external positive power supply VDD voltage 96 doubles. Supply voltage is doubled in principle by pumping the VOSC which oscillates between the VDD and VSS. Pumping by VOSC is controlled by the VPP level sensor 98 to adjust to 3.6V steady voltage level (VARY (2.0V) 1.6V). Thus VPP is, up to two times the VDD level is constrained by the VPP level sensor 98 but does not reach, it will maintain a sufficiently strong state.

[0037]
If the power supply voltage 96 is first in the form of a conventional VPP regulator is connected to VDD, the voltage regulator circuit 94 reliability problems. This is because when the 4.0V VDD voltage rises, the internal node voltage (not shown) may exceed the 8.0V (VDD VDD), in order

線により、この好適な実施形態においてマスタスライス技術でどのように実現されているかが示されている。マスタスライス技術では、3.３Ｖバージョンのための第１のマスク層（図示せず）は、破線で示される配線を除いた第１の配線層を形成するために用いられる。また、2.５Ｖバージョンのための第２のマスク層（図示せず）は、破線で示される配線を含む第２の配線層を形成するために用いられる。

【００３４】

3.３Ｖバージョンの場合、ＶＰＲＥＩレギュレータ２８が中間電圧Ｖ１からＶＰＲＥＩを出力できるように第１のマスク層は、破線で示される配線２８ａ、２８ｂ（図６）、および８２ａ（図７）を除いた第１の配線層を形成するために用いられる。また、2.５Ｖバージョンの場合、ＶＰＲＥＩレギュレータが中間電圧Ｖ１からＶＰＲＥＩを出力できないように第２のマスク層は、破線で示される配線２８ａ、２８ｂ（図６）および８２ａ（図７）を含む第２の配線層を形成するために用いられる。その結果、ＶＤＤ（=2.５Ｖ）電圧を出力できるようにする。

【００３５】

比較的サイズの大きなチップ（図１９）におけるＶＰＥＲＩレギュレータ２８の性能をさらに向上させるために、チップの周りの様々な位置に多重レギュレータ（図１９）が複数配置される。このようにして、長いＶＰＥＲＩ電源線（図示せず）の配線抵抗によって引き起こされる電圧下降はかなり減少させられる。

【００３６】

図９を参照すると、参照番号９４により従来のＶＰＰレギュレータが示されている。ＶＰＰレギュレータ９４は電源電圧９６（これはＶＤＤあるいはＶＰＥＲＩのどちらかに接続される）と、ＶＰＰレベルセンサからの出力電圧ＶＯＳＣとを用いている。電圧レギュレータ９４は、外部プラス電源ＶＤＤ電圧９６を２倍にすることにより電源電圧９６よりも高い電圧ＶＰＰを生成する。電源電圧は、ＶＤＤとＶＳＳとの間を振動するＶＯＳＣによりポンピングすることにより原理的には２倍にされる。ＶＯＳＣによるポンピングは、3.６Ｖの定常電圧レベル（ＶＡＲＹ（2.０Ｖ）＋1.６Ｖ）に調整するためＶＰＰレベルセンサ９８によ

to continue keeping the reliability, the conventional VPP regulator 94 It exceeds 8.0V This is because must ensure no internal nodes. If the supply voltage 96 of the second embodiment of the prior art connected to VPERI, when VDD is 4.0V, which internal node voltage is not to exceed 8.0V, another problem arises. For example, conventional VPP regulator 94, the ratio of output current to input current (current efficiency) is 50 percent. That is, the conventional VPP regulator supplies an output current of 10mA for each swallowing the supply current of 20mA. Therefore, in the conventional second embodiment, the voltage regulator 94 consumes extremely current at VPERI voltage regulator (Fig. 6) becomes overloaded.

[0038]

Referring to Figure 10, VPP regulator is improved according to the present invention by reference numeral 32 is shown. VPP regulator 32 is used in both the 3.3V version device 20a (FIG. 2a) and 2.5V version device 20b (Fig. 2b). VPP regulator 32 by using the output voltage VOSC from both the oscillator VDD and VPERI. By using both VDD and VPERI, if the VDD voltage is higher than 4.0V also does not exceed the voltage of 8.0V is also an internal node of the VPP regulator 32 throat including a node N2. In other words, the low voltage level of VPERI, the voltage of the node N2 is reduced VDD VPERI, that is, 6.5V. Furthermore, VPP regulator 32 is the input current - but is about 50 percent the output current ratio is also, VPP regulator 32 is designed to swallow a large part of the input current (not shown) from an external positive power supply VDD, whereby the consumption of current in VPERI regulator 28 (FIG. 6) is reduced.

[0039]

Referring to Figure 11, the reference numeral 32, VPP regulator is improved according to the invention in Figure 10 is shown. Both VDD and VPERI in order to generate the VPP in VPP regulator 32 is used. VPP regulator 32, a plurality of NMOS transistors 99a, 99b, 99c, 99d, 99e, 99f, 99g, 99h, and 99i, a PMOS transistor 100, a plurality of capacitors C2, C3, C4, C5, C6, a plurality of inverters 101a, 101b, 101c, 101d, and has a 101e, 101d, each inverter, with the exception of 101e operating in the VDD voltage level. These transistors and inverters are grouped by their applied voltage. VDD applied to NMOS transistor 99b, 99c, 99d and the inverter 101a,

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り制御されている。こうしてＶＰＰは、２倍のＶＤＤレベルまで到達しないもののＶＰＰレベルセンサ９８により制約され、十分に強い状態を維持する。

【００３７】

電源電圧９６がＶＤＤに接続される従来のＶＰＰレギュレータの第１の形態の場合、電圧レギュレータ回路９４は信頼性の問題が生じる。これは、ＶＤＤ電圧が上昇し4.０Ｖのとき、内部ノード電圧（図示せず）は8.０Ｖ（ＶＤＤ＋ＶＤＤ）を超えることがあり、信頼性を保ち続けるためには、従来のＶＰＰレギュレータ９４は8.０Ｖを超える内部ノードを持たないようにしなければならないからである。電源電圧９６がＶＰＥＲＩに接続される従来の第２の形態の場合には、ＶＤＤが4.０Ｖのとき、どの内部ノード電圧も8.０Ｖを超えることはないが、他の問題が生じる。例えば、従来のＶＰＰレギュレータ９４は、入力電流に対する出力電流の比（電流効率）が５０％である。すなわち、従来のＶＰＰレギュレータは、２０ｍＡの電源電流を飲み込むごとに１０ｍＡの出力電流を供給する。従って、従来の第２の形態の場合、電圧レギュレータ９４はＶＰＥＲＩ電圧レギュレータ（図６）において極端に電流を消費し過負荷となってしまう。

【００３８】

図１０を参照すると、参照番号３２によって本発明による改善されたＶＰＰレギュレータが示されている。ＶＰＰレギュレータ３２は、3.３Ｖバージョンデバイス２０ａ（図２ａ）および2.５Ｖバージョンデバイス２０ｂ（図２ｂ）の両方で用いられる。ＶＰＰレギュレータ３２は、ＶＤＤおよびＶＰＥＲＩの両方と発振器からの出力電圧ＶＯＳＣとを用いている。ＶＤＤおよびＶＰＥＲＩの両方を用いることにより、ＶＤＤ電圧が4.０Ｖより高い場合にも、ノードＮ２を含めＶＰＰレギュレータ３２のどの内部ノードも8.０Ｖの電圧を超えることはない。すなわち、ＶＰＥＲＩの低電圧レベルにより、ノードＮ２の電圧はＶＤＤ＋ＶＰＥＲＩ、すなわち6.５Ｖに減少されている。さらに、ＶＰＰレギュレータ３２はその入力電流ー出力電流比がやはり約５０％であるものの、ＶＰＰレギュレータ３２は入力電流（図示せず）の大部分を外部プラス電源ＶＤＤから飲み込むように設

101b, it is a 101c. On the other hand, VPERI applied to the NMOS transistor 99e, an inverter 101d, it is 101e. Operation of VPP regulator 32 is further explained by considering the signal at node N1, N2, N3, N4, N5, N6, N7, N8 and N9.

[0040]

Referring also to Figure 12, the signal waveforms at the nodes N8 and N9 are those reversed signals and VOSC waveforms at node N7. Signal waveforms at the node N1 is generated by pumping the VDD amplitude signal of VPERI which is pre-charged to the capacitor C2 at the node N7 by 99a. Signal waveforms at the node N2 is generated by pumping the VDD amplitude signal to the capacitor C3 at node N8 the VPERI which is precharged by 99h. Signal waveform at node N5 is generated by combining the signals at VOSC and the node N9, N4 and N6. Signal waveform at node N3 is generated by pumping the double VPERI amplitude of the signal to the capacitor C4 and VPERI which is pre-charged at the node N5 by 99f. As a result, High level at the node N2 is equal to the sum for the VDD voltage and VPERI (2.5V). In addition, High voltage of N3 is three times of VPERI. 99i is a rectifier transistor. Capacitor C6 is a large decoupling capacitor, and has helped to prevent fluctuation of the VPP voltage.

[0041]

Advantageous Other points VPP regulator 32 in Figure 11, the gate - a transistor source voltage exceeds the confidence limits is that the VPP level is generated without even one. Also, 99b, 99c, 99d, 99e and 101c is a circuit that was devised for the voltage relaxation. In the above embodiment, stationary gate of the PMOS transistor 100 - source voltage is VPERI (2.5V). If the node N9 is equal to VDD (3.3V or 2.5V), node N5 is twice the VPERI (5.0V), and therefore NMOS transistor 99b is the maximum gate of 2.5V - a voltage between the source. If the node N3 is equal to three times the VPERI (7.5V), the node N2 is VPERI VDD (5.0V or 5.8V), and therefore NMOS transistor 99i is the maximum gate of 2.5V - a voltage between the source. Similarly, the remaining transistors, the gate - source voltage is relatively low.

[0042]

Referring to Figure 13, VARY regulator is indicated by reference number 30. As shown in the figure, VARY regulator 30 is driven to set the signal line SDP1, SDP2, SDP3 etc., these signal lines, the first is referred to as SDP as a whole with

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計されており、それによりＶＰＥＲＩレギュレータ２８（図６）における電流の消費は減少される。

【００３９】

図１１を参照すると、参照番号３２によって、図１０の本発明による改善されたＶＰＰレギュレータが示されている。ＶＰＰレギュレータ３２ではＶＰＰを生成するためにＶＤＤおよびＶＰＥＲＩの両方が用いられている。ＶＰＰレギュレータ３２は、複数のＮＭＯＳトランジスタ９９ａ、９９ｂ、９９ｃ、９９ｄ、９９ｅ、９９ｆ、９９ｇ、９９ｈ、９９ｉと、ＰＭＯＳトランジスタ１００と、複数のコンデンサＣ２、Ｃ３、Ｃ４、Ｃ５、Ｃ６と、複数のインバータ１０１ａ、１０１ｂ、１０１ｃ、１０１ｄ、１０１ｅとを有しており、１０１ｄ、１０１ｅを除く各インバータはＶＤＤ電圧レベルで動作する。これらトランジスタおよびインバータは、それらの印加電圧によりグループ分けされる。ＶＤＤ印加はＮＭＯＳトランジスタ９９ｂ、９９ｃ、９９ｄとインバータ１０１ａ、１０１ｂ、１０１ｃである。一方、ＶＰＥＲＩ印加はＮＭＯＳトランジスタ９９ｅと、インバータ１０１ｄ、１０１ｅである。ＶＰＰレギュレータ３２の動作は、さらに、ノードＮ１、Ｎ２、Ｎ３、Ｎ４、Ｎ５、Ｎ６、Ｎ７、Ｎ８およびＮ９における信号を検討することにより説明される。

【００４０】

図１２をも参照すると、ノードＮ８およびＮ９における信号の波形は、ノードＮ７における信号およびＶＯＳＣの波形を逆転したものである。ノードＮ１における信号の波形は、９９ａによりプリチャージされたＶＰＥＲＩをノードＮ７におけるコンデンサＣ２へのＶＤＤ振幅信号によりポンピングすることにより生成されている。ノードＮ２における信号の波形は、９９ｈによりプリチャージされたＶＰＥＲＩをノードＮ８におけるコンデンサＣ３へのＶＤＤ振幅信号によりポンピングすることにより生成されている。ノードＮ５における信号の波形は、ＶＯＳＣとノードＮ９、Ｎ４およびＮ６における信号とを組み合わせることにより生成されている。ノードＮ３における信号の波形は、９９ｆによりプリチャージされたＶＰＥＲＩをノードＮ５におけるコンデンサＣ４への２倍のＶＰＥＲＩ振幅の信号によりポンピングするこ

reference to Figure 5, it is one that has been described. Since the overdrive sense amplifier operation VDD also drive the signal line SDP, by two of the drive signal SAP1 and SAP2 (see also Figure 5), which of the two voltage VDD voltage and VARY at any one time is a signal line SDP do you want to drive is controlled.

[0043]

VARY regulator 30 includes a first differential circuit 102, a divider 104, and in that it has first and second pull-up PMOS transistors 106 and 108, similar to VPERI regulator 28 of FIG. 6 there. VARY regulator 30 also has a second differential circuit 110, the PMOS transistor 112, it also has a pull-down NMOS transistor 114. VARY regulator 30 intermediate voltage V2 (1.And 0V), it receives and ACTV signal, and the sense enable signal SAE, and DETECT2B. DETECT2B signal is applied to the gate of the pull-up PMOS transistor 108. Method of generating the DETECT2B signal and DETECT2 signal is the same as the DETECT1 signal, DETECT1B signal. In other words, by setting the division ratio or the reference voltage, it is set so DETECT2B signal changes at a lower VDD voltage (VDD = 2.2V). The VDD voltage second low voltage range 54 (FIG. 4a, VDD ≦ 2.2V) or a third of the low-voltage range 60 (FIG. 4b, VDD ≦ 2.2V), DETECT2B signal becomes VBB level.

[0044]

Referring also to Figure 14, the operation occurs in the active period 116, this period will always ACTV signal is determined by the High level. In this period 116, when the VARY is low, VARY regulator 30 functions so as to restore the original voltage of the VARY like the VPERI regulator 28. However, in the case VARY high reversed, and the SAE signal, a second differential circuit 110, a pull-down NMOS transistor 114 is VARY level is discharged working. As mentioned above, both the VARY and VDD voltage is driving the SDP signal line. Period of overdrive, becomes the signal line SDP is VDD voltage or the level close to it, then when the SAP2 to Low level, VARY temporarily rises toward the VDD voltage. By discharging the VARY level, in order to lower it into Again 2.0V, SAE signals (which becomes the High level after the VARY is connected to the SDP signal) to the second differential circuit 110, To compare the output with a reference voltage divider 104 V2. As a result, the second differential circuit 110 to the voltage level from the voltage dividing circuit 104 is equal to V2

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とにより生成されている。その結果、ノードＮ２におけるＨｉｇｈレベルはＶＤＤ電圧とＶＰＥＲＩ（2.５Ｖ）のに和に等しい。また、Ｎ３のＨｉｇｈ電圧は３倍のＶＰＥＲＩである。９９ｉは整流用トランジスタである。コンデンサＣ６は大きなデカップリングコンデンサであって、ＶＰＰ電圧の変動を防止するのに助けとなっている。

【００４１】

図１１のＶＰＰレギュレータ３２の有利な他の点は、ゲートーソース間電圧が信頼性限界を超えるトランジスタは１つも用いずにＶＰＰレベルが生成されていることである。また、９９ｂ、９９ｃ、９９ｄ、９９ｅと１０１ｃは電圧緩和のために工夫した回路である。上述の実施形態においては、ＰＭＯＳトランジスタ１００の定常的なゲートーソース間電圧はＶＰＥＲＩ（2.５Ｖ）である。ノードＮ９がＶＤＤ（3.３Ｖあるいは2.５Ｖ）に等しい場合、ノードＮ５はＶＰＥＲＩの２倍（5.０Ｖ）であり、そのためＮＭＯＳトランジスタ９９ｂは2.５Ｖの最大ゲートーソース間電圧となる。ノードＮ３がＶＰＥＲＩの３倍（7.５Ｖ）に等しい場合、ノードＮ２はＶＰＥＲＩ＋ＶＤＤ（5.０Ｖあるいは5.８Ｖ）であり、そのためＮＭＯＳトランジスタ９９ｉは2.５Ｖの最大ゲートーソース間電圧となる。同様に、残りのトランジスタについても、ゲートーソース間電圧は比較的低いものとなる。

【００４２】

図１３を参照すると、参照番号３０によりＶＡＲＹレギュレータが示されている。その図に示されているように、ＶＡＲＹレギュレータ３０は一連の信号線ＳＤＰ１、ＳＤＰ２、ＳＤＰ３等を駆動しており、これら信号線は、先に、図５を参照して全体としてＳＤＰとして参照され、説明されたものである。オーバードライブセンスアンプ動作によりＶＤＤも信号線ＳＤＰを駆動するので、２つのドライブ信号ＳＡＰ１およびＳＡＰ２（図５をも参照）により、任意の１時点において２つの電圧ＶＤＤ電圧およびＶＡＲＹのどちらが信号線ＳＤＰを駆動するのかが制御される。

【００４３】

ＶＡＲＹレギュレータ３０は、第１の差動回路１０２と、分圧器１０４と、第１および第２のプルアップＰＭＯＳトランジスタ１０６および１０８

(1.0V), while the pull-down transistor 114 and activated, which VARY equals 2.0V it is meant to become.

[0045]
In Figure 5 reference again to the bit B1 has a capacitor C1, the plate of C1 is connected to the VPLT, the counter electrode of the capacitor is stored bit voltage VSN of VSS or VARY. Referring also to Figure 15, the voltage level of VPLT is set midway, that is, 1.0V for as in the conventional VSS and (0V) and VARY (2.0V). This works well with respect to SiO_2 and Si_3N and $_4$ of such a dielectric. However, the use of small to take a large capacitor capacitance in the memory cell high dielectric Ta_2O_5, a leakage current characteristic is asymmetric. For example, when the bit voltage VSN is equal to VSS, dielectric Ta_2O_5 there is a positive leakage current I1 to the, when the bit voltage VSN is equal to VARY minus of leakage current I2 exists. In this prior art embodiment, the leakage currents I1 and I2 is asymmetric, that is, the leakage current I1 is large and disproportionately compared to the leakage current I2. Thus, since the leakage current I1 is too large, so that it would not lose the data stored in the capacitor C1.

[0046]
Referring to FIG. 16, according to the present invention, has been adjusted level of VPLT so that the leakage current becomes more symmetric dielectric Ta_2O_5. This in order to achieve the result, the voltage level of the VPLT is 0.5V, ie, has been adjusted to the level of 1/4 of VARY. As a result, when the bit voltage VSN is equal to VSS is positive leakage current I3 is generated, when the bit voltage VSN is equal to VARY is, minus the leakage current I4 is generated, these leakage current I3, I4 rather symmetrical, both are relatively small.

[0047]
Referring to Figure 17, there is shown a VBLR and VPLT regulator is improved according to the present invention by reference numeral 36. VBLR and VPLT regulator 36, is generating a bit line pre-charge voltage VBLR and plate voltage VPLT. Although VBLR (1.0V) is generated by the first subcircuit 118a, a first sub-circuit 118a generates exactly one voltage half of the VARY (2.0V) and VSS (0V) It is. The first sub-circuit 118a, for example Satoet al. US patent 4, 839, as described

を有している点で、図６のＶＰＥＲＩレギュレータ２８と類似している。ＶＡＲＹレギュレータ３０はまた、第２の差動回路１１０と、ＰＭＯＳトランジスタ１１２と、プルダウンＮＭＯＳトランジスタ１１４をも有している。ＶＡＲＹレギュレータ３０は中間電圧Ｖ２（1.0Ｖ）と、ＡＣＴＶ信号と、センスイネーブル信号ＳＡＥと、ＤＥＴＥＣＴ２Ｂとを受け取る。ＤＥＴＥＣＴ２Ｂ信号はプルアップＰＭＯＳトランジスタ１０８のゲートに印加されている。ＤＥＴＥＣＴ２Ｂ信号とＤＥＴＥＣＴ２信号の生成方法はＤＥＴＥＣＴ１信号、ＤＥＴＥＣＴ１Ｂ信号と同様である。つまり、分圧比または基準電圧の設定により、より低いＶＤＤ電圧（ＶＤＤ=2.２Ｖ）でＤＥＴＥＣＴ２Ｂ信号が変化するように設定する。ＶＤＤ電圧が第２の低電圧範囲５４（図４ａ、ＶＤＤ≦2.２Ｖ）または第３の低電圧範囲６０（図４ｂ、ＶＤＤ≦2.２Ｖ）、ＤＥＴＥＣＴ２Ｂ信号はＶＢＢレベルになる。

【００４４】

図１４をも参照すると、動作はアクティブ期間１１６において発生し、この期間はいつもＡＣＴＶ信号がＨｉｇｈレベルとなることにより決定されている。この期間１１６において、ＶＡＲＹが低いときには、ＶＡＲＹレギュレータ３０はＶＰＥＲＩレギュレータ２８と同様にＶＡＲＹの本来の電圧に回復させるように機能する。しかし、ＶＡＲＹが逆に高い場合には、ＳＡＥ信号と、第２の差動回路１１０と、プルダウンＮＭＯＳトランジスタ１１４が働いてＶＡＲＹレベルが放電される。上述のように、ＶＡＲＹおよびＶＤＤ電圧の両方がＳＤＰ信号線を駆動している。オーバードライブの期間、信号線ＳＤＰはＶＤＤ電圧あるいはそれに近いレベルとなり、その後ＳＡＰ２をＬｏｗレベルにすると、ＶＡＲＹは一時的にＶＤＤ電圧に向かって上昇する。ＶＡＲＹレベルを放電して、それを再び2.０Ｖへと引き下げるために、ＳＡＥ信号（これはＶＡＲＹがＳＤＰ信号に接続された後にＨｉｇｈレベルとなる）は第２の差動回路１１０をして、分圧器１０４の出力と基準電圧Ｖ２とを比較させる。その結果、第２の差動回路１１０は、分圧回路１０４からの電圧レベルがＶ２（1.０Ｖ）に等しくなるまで、プルダウントランジスタ１１４をアクティブとするが、これは

in 865 issue, it is a semi-voltage regulator, the current consumption is very low. The invention also includes a second sub-circuit 118b coupled between the VBLR and (1.0V) and VSS (0V).

[0048]
Referring to Figure 18, the second subcircuit 118b to produce the desired voltage level VPLT (0.5V). However, the circuit is the load current supply capacity as raise the VPLT marked with a large parasitic capacitance when VDD power up quickly from 0V is not strong. Load capacity of VPLT is the sum of all of the memory cell capacitor, it is because extremely large. Thus, if or VDD is the first power-up VDD, the second and third low voltage range 53,54,60 (FIG. 4a, Fig. 4b) in the case of the connection to a large VBLR more current supply capability of VPLT By, it becomes possible to raise quickly VPLT through the circuit 120. NMOS diode in the circuit 120 for that is what makes the level difference between VBLR and VPLT. VBLR level is pulled through the bit line BL, the charge-discharge operation of the sense amplifier circuit 69 (Figure 5). Finally, the VDD reaches a normal operating level at time t1, the pull-up circuit 120 is set to the disabled by the detector voltage VUPB transitions Low, the second subcircuit 118b is to VPLT through the transistor 122 and it is connected to. In this case, VBLR and VPLT is different voltage.

[0049]
Referring to Figure 19, the chip overall view of a 64M-bit or 256M bit DRAM in which a plurality of voltage regulators by reference number 123 is shown. Among the memory chip 123, the word lines are horizontal, the bit lines in the vertical direction. Region 127 extending in the longitudinal direction is the peripheral circuits and the bonding pad region, the region 132 extending in the short side direction is between the memory cell array region. Various voltage regulator of the present invention (VPERI, VARY, VPP, VBB, VBLRV, VPLT regulator) peripheral circuits and or bonding pad region 127, are preferably arranged in the memory cell array region between 132. Because the voltage regulator has a large circuit element dimensions, and because the occupied area to the memory chip 123 is large, because it is difficult to place on the periphery of the memory cell array 128. Then, VPREI regulator, a large circuit of the load current as a VARY regulators are arranged in a dispersed manner in the memory chip 123, to reduce the drop in voltage due to load current.

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ＶＡＲＹが2.０Ｖに等しくなることを意味している。

【００４５】

図５を再び参照すると、ビットＢ１はキャパシタＣ１を有しており、Ｃ１のプレートはＶＰＬＴに接続され、キャパシタの対向電極がＶＳＳ又はＶＡＲＹのビット電圧ＶＳＮを蓄えている。図１５をも参照すると、ＶＰＬＴの電圧レベルは従来のようにＶＳＳ（０Ｖ）とＶＡＲＹ（2.０Ｖ）との中間、すなわち1.０Ｖに設定されている。これはSiO_2やSi_3N_4のような誘電体に関してうまく機能する。しかし、小さなメモリセルで大きなキャパシタ容量をとるため高誘電体Ta_2O_5を用いると、そのリーク電流特性は非対称である。例えば、ビット電圧ＶＳＮがＶＳＳに等しい場合、誘電体Ta_2O_5にはプラスのリーク電流Ｉ１が存在し、ビット電圧ＶＳＮがＶＡＲＹに等しい場合にはマイナスのリーク電流Ｉ２が存在する。この従来の形態の場合、リーク電流Ｉ１およびＩ２は非対称であり、すなわち、リーク電流Ｉ１はリーク電流Ｉ２に比較して不釣合いに大きい。こうして、リーク電流Ｉ１が大きすぎるため、キャパシタＣ１に蓄えられたデータを失わせてしまうことになる。

【００４６】

図１６を参照すると、本発明により、誘電体Ta_2O_5のリーク電流がより対称的となるようにＶＰＬＴのレベルが調節されている。この結果を達成するために、ＶＰＬＴの電圧レベルは0.５Ｖ、すなわち、ＶＡＲＹの４分の１というレベルに調節されている。それにより、ビット電圧ＶＳＮがＶＳＳに等しい場合には、プラスのリーク電流Ｉ３が生成され、ビット電圧ＶＳＮがＶＡＲＹに等しい場合には、マイナスのリーク電流Ｉ４が生成され、これらリーク電流Ｉ３、Ｉ４はかなり対称的で、どちらも比較的小さいものである。

【００４７】

図１７を参照すると、参照番号３６によって本発明による改善されたＶＢＬＲおよびＶＰＬＴレギュレータが示されている。ＶＢＬＲおよびＶＰＬＴレギュレータ３６は、ビット線プリチャージ電圧ＶＢＬＲおよびプレート電圧ＶＰＬＴを生成している。ＶＢＬＲ（1.０Ｖ）は第１の副回路１１８ａにより生成されるが、その第１の副回路１１

[0050]
Above, and it is the invention made by the inventors has been concretely described based on the embodiments, the present invention is not limited to the above embodiments, and various modifications within a scope not departing from the gist thereof it is needless to say is.

[0051]
For example, may incorporate features of a voltage regulator to another regulator, on the other hand, it may be omitted and other features. Furthermore, without departing from the spirit of the present invention, it is also possible to add an additional or alternative elements or other circuitry. Accordingly, the appended claims are appropriate to broadly construed in a manner consistent with the spirit of the invention.

[0052]
It has been described the case of applying the invention made by the present inventors in a semiconductor circuit which is a Field in the above description, and are not limited thereto.

[0053]
Effect of the Invention]
Among the inventions disclosed in the present application, a brief description of effects obtained by the typical ones, it is as follows.

[0054]
(1) By using the master slice technology, the voltage regulator may be adapted to an external voltage of two different ranges.

[0055]
It is possible to significantly increase in the state of very low external voltage the current supply capacity of (2) voltage regulator.

[0056]
(3) charge pump voltage regulators is to not exceed the high voltage level the voltage level predetermined in that any node, moreover, can be as little consumes current from the external power source.

[0057]
(4) by charging and discharging the output voltage of the voltage regulator, it is possible to maintain the output voltage at a constant level.

[0058]
(5) a voltage regulator, it can be assumed that is

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８ａはＶＡＲＹ（2.０Ｖ）とＶＳＳ（０Ｖ）との丁度２分の１の電圧を生成するものである。第１の副回路１１８ａは、例えばＳａｔｏｅｔａｌ．の米国特許４，８３９，８６５号に記載されているような、半電圧レギュレータであり、消費電流は非常に少ない。本発明はまた、ＶＢＬＲ（1.０Ｖ）とＶＳＳ（０Ｖ）との間に結合された第２の副回路１１８ｂをも含んでいる。

【００４８】

図１８を参照すると、第２の副回路１１８ｂは所望の電圧レベルＶＰＬＴ（0.５Ｖ）を生成する。しかし、その回路はＶＤＤパワーアップ時に大きな寄生容量の付いたＶＰＬＴをすばやく０Ｖから引き上げるほど負荷電流供給能力は強力ではない。ＶＰＬＴの負荷容量はすべてのメモリセルキャパシタの総和であり、極端に大きいからである。従って、ＶＤＤパワーアップの場合あるいはＶＤＤが第１、第２および第３の低電圧範囲５３、５４、６０（図４ａ、図４ｂ）の場合には、ＶＰＬＴをより電流供給能力の大きなＶＢＬＲに接続することにより、回路１２０を介してＶＰＬＴをすばやく引き上げることが可能となる。そのために回路１２０内のＮＭＯＳダイオードはＶＢＬＲとＶＰＬＴのレベル差を作るものである。ＶＢＬＲレベルはセンスアンプ回路６９のビット線ＢＬ、充放電動作（図５）を介して引き上げられる。最後に、ＶＤＤが時刻ｔ１において通常の動作レベルに到達すると、ディテクタ電圧ＶＵＰＢがＬｏｗに遷移することによりプルアップ回路１２０がディスエーブルとされ、第２の副回路１１８ｂがトランジスタ１２２を介してＶＰＬＴへと接続される。この時、ＶＢＬＲとＶＰＬＴは異なった電圧となる。

【００４９】

図１９を参照すると、参照番号１２３により複数の電圧レギュレータを配置した６４Ｍビットまたは２５６ＭビットＤＲＡＭのチップ全体図が示されている。メモリチップ１２３の中で、ワード線は水平方向、ビット線は垂直方向としている。長辺方向に延びる領域１２７は周辺回路およびボンディングパッド領域であり、短辺方向に延びる領域１３２はメモリセルアレイ間領域である。本発明の各種の電圧レギュレータ（ＶＰＥＲＩ、ＶＡＲＹ、ＶＰＰ、ＶＢＢ、ＶＢＬＲＶ、ＶＰＬＴレ

optimized to reduce dielectric leakage.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1a is a block diagram of a 5V version of the conventional 16M-bit DRAM.

FIG. 1b is a block diagram of the 3.3V version of the conventional 16M-bit DRAM.

2a is a block diagram of the 3.3V version of 256M-bit DRAM according to an embodiment of the present invention.

[Figure 2b] 2. 256M bit DRAM according to an embodiment of the present inventionIs a block diagram of a 5V version.

Is a block diagram of a voltage regulator used in the DRAM of FIG. 3a Figure 2a.

It is a block diagram of a voltage regulator used in the DRAM of FIG. 3b Figure 2b.

[Figure 4a] operating voltage corresponding to the DRAM of Figure 2a - is a graph of the internal voltage.

[Figure 4b] operating voltage corresponding to the DRAM of Figure 2b - is a graph of the internal voltage.

5 is a circuit diagram of a DRAM which is simplified, which is an embodiment of the present invention.

6 is a circuit diagram of a first voltage regulator which is an embodiment of the present invention.

FIG. 7 is a circuit diagram of an inverter circuit according to an embodiment of the present invention.

FIG. 8 is a curve showing the dependence of the power supply voltage of the input signal and the output signal of the level conversion function with inverter.

FIG. 9 is a block diagram of a conventional second voltage regulator.

FIG. 10 is a block diagram of a second voltage regulator of the present invention.

11 is a circuit diagram of a second voltage regulator which is an embodiment of the present invention.

FIG. 12 is a timing diagram of the signals shown in Figure 11.

[13] The third voltage regulator according to an embodiment of the present invention, is a circuit diagram showing with a number of circuits of the simplified DRAM of FIG.

FIG. 14 is a timing diagram of the signals shown in Figure 13.

[15] the voltage of the conventional fourth voltage regulators - is a current graph, and illustrates the leakage currents.

[16] The fourth voltage regulator of a voltage of the present invention - is a current graph, and

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ギュレータ）は周辺回路およびボンディングパッド領域１２７または、メモリセルアレイ間領域１３２に配置されるのが好ましい。なぜなら、電圧レギュレータは回路素子寸法が大きく、またメモリチップ１２３に対する占有面積が大きいため、メモリセルアレイ１２８の周辺に配置するのが困難であるからである。そして、ＶＰＲＥＩレギュレータ、ＶＡＲＹレギュレータのような負荷電流の大きい回路はメモリチップ１２３中に分散して配置し、負荷電流による電圧の低下を減少させる。

【００５０】

以上、本発明者によってなされた発明を実施の形態に基づき具体的に説明したが、本発明は前記実施の形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

【００５１】

たとえば、ある電圧レギュレータの特徴を他のレギュレータに組み入れてもよく、一方、他の特徴を省いてもよい。さらに、本発明の趣旨を逸脱することなく、付加的あるいは代替的な素子や他の回路を追加することもできる。従って、添付の特許請求の範囲は本発明の趣旨と整合する仕方で広く解釈するのは適切である。

【００５２】

以上の説明では主として本発明者によってなされた発明をその利用分野である半導体回路に適用した場合について説明したが、これに限定されるものではない。

【００５３】

【発明の効果】

本願において開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば、以下のとおりである。

【００５４】

（１）マスタスライス技術を用いることにより、電圧レギュレータは２つの異なる範囲の外部電圧に適応することができる。

【００５５】

（２）電圧レギュレータの電流供給能力を非常に低い外部電圧の状態においてかなり増大することができる。

【００５６】

illustrates the leakage currents.
17 is a circuit diagram of a fourth voltage regulator of an embodiment of the present invention.
FIG. 18 is a timing diagram of the signals shown in Figure 17.
19 is a diagram showing the entire chip as one embodiment of the present invention.
Description of the code]
10a 5V version device
10b 3.3V version device
12 voltage regulator
12a wiring
12b wiring
13a memory cell and the peripheral circuit
13b output circuit
20a 3.3V version device
20b 2.5V version device
21a peripheral circuit
21b output circuit
21c memory cell array
22 voltage regulator
24 voltage regulator
24a wiring
24b wiring
26 voltage regulator (intermediate voltage regulator)
28 voltage regulator (VPERI regulator)
28a wiring
28b wiring
30 voltage regulator (VARY regulator)
32 voltage regulator (VPP regulator)
34 voltage regulator (VBB regulator)
36 voltage regulator (VBLR and VPLT regulator)
40 wiring
42 wiring
44 wiring
50 The first of the normal operating range
52 first stress range
53 first low voltage range
54 second low voltage range
56 second normal operating range
58 second stress range
60 third low voltage range
62 address buffer
64 address decoder
66 word line driver
68 MOS transistor
68W well
69 sense amplifier circuit
70 amplifier action
71 sense amplifier overdrive circuit
72 equalizer
74 main amplifier
76 output buffer

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（３）チャージポンプ電圧レギュレータは、その任意のノードにおける電圧レベルが予め定められた高電圧レベルを超えないようにし、しかも、ほとんど外部電源からの電流を消費するようにすることができる。

【００５７】

（４）電圧レギュレータの出力電圧を充放電して、出力電圧を一定のレベルに維持することができる。

【００５８】

（５）電圧レギュレータを、誘電漏れを減少させるように最適化されたものとすることができる。

【図面の簡単な説明】

【図１ａ】従来の１６ＭビットＤＲＡＭの５Ｖバージョンのブロック図である。

【図１ｂ】従来の１６ＭビットＤＲＡＭの3.３Ｖバージョンのブロック図である。

【図２ａ】本発明の一実施形態である２５６ＭビットＤＲＡＭの3.３Ｖバージョンのブロック図である。

【図２ｂ】本発明の一実施形態である２５６ＭビットＤＲＡＭの2.５Ｖバージョンのブロック図である。

【図３ａ】図２ａのＤＲＡＭで用いられる電圧レギュレータのブロック図である。

【図３ｂ】図２ｂのＤＲＡＭで用いられる電圧レギュレータのブロック図である。

【図４ａ】図２ａのＤＲＡＭに対応する動作電圧－内部電圧のグラフである。

【図４ｂ】図２ｂのＤＲＡＭに対応する動作電圧ー内部電圧のグラフである。

【図５】本発明の一実施形態である単純化されたＤＲＡＭの回路図である。

【図６】本発明の一実施形態である第１の電圧レギュレータの回路図である。

【図７】本発明の一実施形態であるインバータ回路の回路図である。

【図８】レベル変換機能付きインバータの入力信号および出力信号の電源電圧の依存性を示す曲線である。

【図９】従来の第２の電圧レギュレータのブロック図である。

【図１０】本発明の第２の電圧レギュレータのブロック図である。

82 level conversion function with inverter circuit
82a wiring
84 differential circuit
86 voltage driver
88 first pull-up PMOS transistor
90 second pull-up PMOS transistor
92 output voltage
94 VPP regulator
96 power supply voltage
98 VPP level sensor
99a NMOS transistor
99b NMOS transistor
99c NMOS transistor
99d NMOS transistor
99e NMOS transistor
99f NMOS transistor
99g NMOS transistor
99h NMOS transistor
99i NMOS transistor
100 PMOS transistor
101a inverter
101b inverter
101c inverter
101d inverter
101e inverter
102 first differential circuit
104 minutes divider
106 first pull-up PMOS transistor
108 second pull-up PMOS transistor
110 and the second differential circuit
112 PMOS transistor
114 pull-down MOS transistor
116 active period
118a first sub-circuit
118b second sub-circuit
120 pull-up circuit
122 transistor
123 memory chips
124 main row decoder area
125 main word driver area
126 column decoder area
127 peripheral circuit and the bonding pad region
128 memory cell array
129 sense amplifier area
130 sub-word driver area
131 intersection area
132 memory cell array region
B1 bit
VSN bit voltage
BL bit line
Bar / BL bit line
SDN signal line
SDP signal line
SAP1 drive signal

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【図１１】本発明の一実施形態である第２の電圧レギュレータの回路図である。
【図１２】図１１に示された信号のタイミング図である。
【図１３】本発明の一実施形態としての第３の電圧レギュレータを、図５の単純化されたＤＲＡＭの幾つかの回路と共に示した回路図である。
【図１４】図１３に示された信号のタイミング図である。
【図１５】従来の第４の電圧レギュレータの電圧－電流グラフであり、そのリーク電流を示すものである。
【図１６】本発明の第４の電圧レギュレータの電圧－電流グラフであり、そのリーク電流を示すものである。
【図１７】本発明の一実施形態の第４の電圧レギュレータの回路図である。
【図１８】図１７に示された信号のタイミング図である。
【図１９】本発明の一実施形態であるチップ全体を示す図である。
【符号の説明】
１０ａ ５Ｖバージョンデバイス
１０ｂ 3.3Ｖバージョンデバイス
１２ 電圧レギュレータ
１２ａ 配線
１２ｂ 配線
１３ａ メモリセルおよび周辺回路
１３ｂ 出力回路
２０ａ 3.3Ｖバージョンデバイス
２０ｂ 2.5Ｖバージョンデバイス
２１ａ 周辺回路
２１ｂ 出力回路
２１ｃ メモリセルアレイ
２２ 電圧レギュレータ
２４ 電圧レギュレータ
２４ａ 配線
２４ｂ 配線
２６ 電圧レギュレータ（中間電圧レギュレータ）
２８ 電圧レギュレータ（ＶＰＥＲＩレギュレータ）
２８ａ 配線
２８ｂ 配線
３０ 電圧レギュレータ（ＶＡＲＹレギュレータ）

SAP2 drive signal
SAN drive signal
WL word line
BLEQ signal
YS column selection signal
I / O input-output line
ACTV signal
Output signal
of DETECT1B level conversion function with inverter Output signal
of DETECT2B level conversion function with inverter DETECT1 output signal
of the power supply voltage level sensor circuit ID current
Output voltage
from VOSC oscillator C1 capacitor
C2 capacitor
C3 capacitor
C4 capacitor
C5 capacitor
C6 capacitor
N1 node
N2 node
N3 node
N4 node
N5 node
N6 node
N7 node
N8 node
N9 node
SDP1 signal line
SDP2 signal line
SDP3 signal line
SAE sense enable signal
VSN bit voltage
I1 plus of leakage current
I2 negative leakage current
I3 plus the leakage current
I4 negative leakage current
VDD external plus power
VSS external ground power
VARY array voltage
VPERI internal voltage
VPP internal voltage
VBB internal voltage
VBLR internal voltage
VPLT internal voltage
V1 the first intermediate voltage
V2 second intermediate voltage
Input port of INPUT address

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３２ 電圧レギュレータ（ＶＰＰレギュレータ）
３４ 電圧レギュレータ（ＶＢＢレギュレータ）
３６ 電圧レギュレータ（ＶＢＬＲおよびＶＰＬＴレギュレータ）
４０ 配線
４２ 配線
４４ 配線
５０ 第１の通常動作範囲
５２ 第１のストレス範囲
５３ 第１の低電圧範囲
５４ 第２の低電圧範囲
５６ 第２の通常動作範囲
５８ 第２のストレス範囲
６０ 第３の低電圧範囲
６２ アドレスバッファ
６４ アドレスデコーダ
６６ ワード線ドライバ
６８ ＭＯＳトランジスタ
６８Ｗ ウエル
６９ センスアンプ回路
７０ アンプアクション
７１ センスアンプオーバードライブ回路
７２ イコライザ
７４ メインアンプ
７６ 出力バッファ
８２ レベル変換機能付きインバータ回路
８２ａ 配線
８４ 差動回路
８６ 電圧ドライバ
８８ 第１のプルアップＰＭＯＳトランジスタ
９０ 第２のプルアップＰＭＯＳトランジスタ
９２ 出力電圧
９４ ＶＰＰレギュレータ
９６ 電源電圧
９８ ＶＰＰレベルセンサ
９９ａ ＮＭＯＳトランジスタ
９９ｂ ＮＭＯＳトランジスタ
９９ｃ ＮＭＯＳトランジスタ
９９ｄ ＮＭＯＳトランジスタ
９９ｅ ＮＭＯＳトランジスタ
９９ｆ ＮＭＯＳトランジスタ
９９ｇ ＮＭＯＳトランジスタ
９９ｈ ＮＭＯＳトランジスタ
９９ｉ ＮＭＯＳトランジスタ

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１００ ＰＭＯＳトランジスタ
１０１ａ インバータ
１０１ｂ インバータ
１０１ｃ インバータ
１０１ｄ インバータ
１０１ｅ インバータ
１０２ 第１の差動回路
１０４ 分圧器
１０６ 第１のプルアップＰＭＯＳトランジスタ
１０８ 第２のプルアップＰＭＯＳトランジスタ
１１０ 第２の差動回路
１１２ ＰＭＯＳトランジスタ
１１４ プルダウンＭＯＳトランジスタ
１１６ アクティブ期間
１１８ａ 第１の副回路
１１８ｂ 第２の副回路
１２０ プルアップ回路
１２２ トランジスタ
１２３ メモリチップ
１２４ メインローデコーダ領域
１２５ メインワードドライバ領域
１２６ カラムデコーダ領域
１２７ 周辺回路およびボンディングパッド領域
１２８ メモリセルアレイ
１２９ センスアンプ領域
１３０ サブワードドライバ領域
１３１ 交差領域
１３２ メモリセルアレイ領域
Ｂ１ ビット
ＶＳＮ ビット電圧
ＢＬ ビット線
バー／ＢＬ ビット線
ＳＤＮ 信号線
ＳＤＰ 信号線
ＳＡＰ１ ドライブ信号
ＳＡＰ２ ドライブ信号
ＳＡＮ ドライブ信号
ＷＬ ワード線
ＢＬＥＱ 信号
ＹＳ 列選択信号
Ｉ／Ｏ 入出力線
ＡＣＴＶ 信号
ＤＥＴＥＣＴ１Ｂ レベル変換機能付きインバータの出力信号

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ＤＥＴＥＣＴ２Ｂ レベル変換機能付きインバータの出力信号
ＤＥＴＥＣＴ１ 電源電圧レベルセンサ回路の出力信号
ＩＤ 電流
ＶＯＳＣ 発振器からの出力電圧
Ｃ１ キャパシタ
Ｃ２ コンデンサ
Ｃ３ コンデンサ
Ｃ４ コンデンサ
Ｃ５ コンデンサ
Ｃ６ コンデンサ
Ｎ１ ノード
Ｎ２ ノード
Ｎ３ ノード
Ｎ４ ノード
Ｎ５ ノード
Ｎ６ ノード
Ｎ７ ノード
Ｎ８ ノード
Ｎ９ ノード
ＳＤＰ１ 信号線
ＳＤＰ２ 信号線
ＳＤＰ３ 信号線
ＳＡＥ センスイネーブル信号
ＶＳＮ ビット電圧
Ｉ１ プラスのリーク電流
Ｉ２ マイナスのリーク電流
Ｉ３ プラスのリーク電流
Ｉ４ マイナスのリーク電流
ＶＤＤ 外部プラス電源
ＶＳＳ 外部接地電源
ＶＡＲＹ アレイ電圧
ＶＰＥＲＩ 内部電圧
ＶＰＰ 内部電圧
ＶＢＢ 内部電圧
ＶＢＬＲ 内部電圧
ＶＰＬＴ 内部電圧
Ｖ１ 第１の中間電圧
Ｖ２ 第２の中間電圧
ＩＮＰＵＴ アドレスの入力ポート

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最終頁に続く

(54)【発明の名称】半導体回路

(57)【特許請求の範囲】

【請求項１】

複数のマスク層を用いて製造される半導体回路であって、

複数のメモリセルと、

複数の出力回路と、

複数の周辺回路と、

外部プラス電源電圧を受け取るための第１の外部パッドであり、該外部プラス電源電圧のレベルが第１の動作電圧範囲と第２の動作電圧範囲のうちのいずれか１つにあり、該第２の動作電圧範囲が該第１の動作電圧範囲より高いものと、

外部接地電源電圧を受け取るための第２の外部パッドと、

前記メモリセルのための第１の出力電圧を生成するための第１の電圧レギュレータと、

前記周辺回路のための第２の出力電圧を生成するものであり、第１の出力トランジスタと、第２の出力トランジスタと、前記第２の出力電圧の低下に応答して前記第１の出力トランジスタを起動する第１の回路と、前記第１の動作電圧範囲で前記外部プラス電源電圧の前記レベルに応答して前記第２の出力トランジスタを起動する第２回路とを備える第２の電圧レギュレータとを有し、

前記外部プラス電源電圧のレベルを前記第１の動作電圧範囲内で動作させようとする場合には、前記第２の電圧レギュレータにおける前記第１および第２の出力トランジスタを短絡させる第１のマスク層が用いられ、

前記外部プラス電源電圧のレベルを前記第２の動作電圧範囲内で動作させようとする場

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合には、第２のマスク層が用いられ、
前記外部プラス電源電圧のレベルが前記第１の動作電圧範囲にある場合に、前記外部プラス電圧レベルの変動にもかかわらず前記第１の出力電圧のレベルが略一定であり、前記第２の出力トランジスタが起動されて前記第２の出力電圧が前記第２の出力トランジスタを介して前記外部プラス電源電圧に接続されるようにし、
前記外部プラス電源電圧のレベルが前記第２の動作電圧範囲内である時に、前記外部プラス電圧のレベルの変動にもかかわらず前記第１および第２の出力電圧のレベルが略一定であり、前記第２の出力トランジスタがイネーブルされず、前記第２の出力電圧が、前記第２の出力電圧の低下に応答して前記第１の出力トランジスタを介して前記プラス電源電圧に選択的に接続されるようにすることを特徴とする半導体回路。

【請求項２】
請求項１記載の半導体回路であって、前記メモリセルの各々がコンデンサを有し、該コンデンサの格納電圧が前記外部接地電源電圧のレベルまたは前記第１の出力電圧のレベルのいずれかであることを特徴とする半導体回路。

【請求項３】
請求項１または２記載の半導体回路であって、前記第１および第２のマスク層に関して、前記メモリセルと、前記出力回路と、前記周辺回路とが同一であることを特徴とする半導体回路。

【請求項４】
出力電圧と出力電流を生成する半導体回路であって、
外部電源に接続され、電圧および電流を供給する第１のプラス電源と、
内部電源に接続され、電圧および電流を供給する第２のプラス電源と、
振動電圧を受け取る入力端子と、
前記振動電圧、前記第１のプラス電源電圧、および、前記第２のプラス電源電圧を受け取り、前記出力電圧を操作する電圧ポンピング回路とを備え、
前記出力電圧が前記第１および第２のプラス電源の両方の電圧よりも大きく、かつ前記出力電流が前記第１および第２のプラス電源の電流から供給されることを特徴とする半導体回路。

【請求項５】
請求項４記載の半導体回路であって、前記出力電流の半分以上が前記第１のプラス電源から供給されることを特徴とする半導体回路。

【請求項６】
請求項４または５記載の半導体回路であって、さらに、
２つの端子を有する結合コンデンサと、
ゲート、ソースおよびドレインを有する第１のＮＭＯＳトランジスタであって、前記ゲートは前記結合コンデンサの第１の端子に接続され、前記ドレインは前記出力電圧を駆動する第１のＮＭＯＳトランジスタとを有し、
前記ゲートは前記第２のプラス電源の電圧の３倍の電圧レベルに達し、
前記ドレインは、出力電圧を前記第１および前記第２のプラス電源の電圧の和に等しいレベルまで駆動することを特徴とする半導体回路。

【請求項７】
請求項６記載の半導体回路路であって、さらに、ゲート、ソースおよびドレインを有する第２のＮＭＯＳトランジスタと、
ゲート、ソースおよびドレインを有するＰＭＯＳトランジスタであって、該ＰＭＯＳトランジスタの前記ゲートは前記第２のプラス電源に接続されているＰＭＯＳトランジスタとを有し、
前記第２のＮＭＯＳトランジスタおよび前記ＰＭＯＳトランジスタの前記ドレインは前記結合コンデンサの第２の端子に接続され、それにより、前記結合コンデンサの前記第２の端子の電圧レベルが、前記第２のプラス電源電圧レベルの２倍にポンピングされることを特徴とする半導体回路路。

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【請求項８】
請求項５記載の半導体回路であって、さらに、それぞれがゲートとソースを備えた複数のトランジスタを有し、それにより、各トランジスタのゲートおよびソースにまたがる電圧差が前記第１あるいは前記第２のプラス電源電圧のどちらをも超過しないことを特徴とする半導体回路。
【請求項９】
メモリセルに対し第１および第２の電圧を供給するための半導体回路であって、
該メモリセルは、ビットＨｉｇｈレベル電圧とビットＬｏｗレベル電圧との間で動作するビット線と、前記ビットＨｉｇｈレベル電圧あるいは前記ビットＬｏｗレベル電圧のいずれかを蓄えるためのコンデンサであって前記ビット線に接続可能な第１のプレートと電圧レギュレータの前記第２の電圧に接続された第２のプレートとを備えたコンデンサを有し、
該電圧レギュレータは、
前記ビットＨｉｇｈレベル電圧と前記ビットＬｏｗレベル電圧との中間のレベルの前記第１の電圧を生成する手段と、
前記第１の電圧と前記ビットＬｏｗレベル電圧との中間のレベルの前記第２の電圧を生成する手段とを有することを特徴とする半導体回路。
【請求項１０】
請求項９記載の半導体回路において、
前記第１および第２の回路が、カスケードに接続された第１および第２の半電圧レギュレータをそれぞれ有し、前記第１の半電圧レギュレータが、前記ビットＨｉｇｈレベル電圧および前記ビットＬｏｗレベル電圧により供給されて前記第１の電圧を生成させるようにし、前記第２の半電圧レギュレータが、前記第１の電圧および前記ビットＬｏｗレベル電圧により供給されて前記第２の電圧を生成させるようにすることを特徴とする半導体回路。
【請求項１１】
請求項１０記載の半導体回路において、前記第１の半電圧レギュレータは前記第１および第２の電圧の両方を供給し、該第２の電圧は前記第２のプレートの電圧を上昇させることを特徴とする半導体回路。
【請求項１２】
請求項９～１１のいずれか１項に記載の半導体回路であって、さらに、初期動作の間に、前記第２の電圧を生成させる手段を助けるためのプルアップ回路を有することを特徴とする半導体回路。
【請求項１３】
出力電圧および出力電流を生成する半導体回路であって、
外部電源に接続され、電圧および電流を供給する第１のプラス電源と、
内部電源に接続され、電圧および電流を供給する第２のプラス電源と、
２つの端子を有する結合コンデンサと、
前記結合コンデンサの第１の端子に接続されたゲート、および、ソース、および、前記出力電圧を操作するために接続されたドレインを有する第１ＮＭＯＳトランジスタとを備え、
前記出力電圧が前記第１および第２のプラス電源電圧より大きく、前記出力電流が前記第１および第２のプラス電源電流から供給され、
前記ゲートが、前記第２のプラス電源電圧の３倍の電圧レベルに達し、
前記ドレインが、前記第１および第２のプラス電源電圧の合計に等しいレベルまで出力電圧を操作することを特徴とする半導体回路。
【請求項１４】
請求項１３記載の半導体回路であって、さらに、ゲート、ソース、およびドレインを有するＮＭＯＳトランジスタと、
前記第２のプラス電源に接続されたゲート、および、ソース、および、ドレインを有す

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るＰＭＯＳトランジスタとを更に備え、
　前記第２のＮＭＯＳトランジスタと前記ＰＭＯＳトランジスタとのドレインが、前記結合コンデンサの前記第２の端子に接続され、前記結合コンデンサの前記第２の端子における電圧レベルが、前記第２のプラス電源電圧の２倍にポンピングされるようにすることを特徴とする半導体回路。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】
本発明は、一般的に半導体設計技術に関し、特に、異なる外部プラス電源電圧レベルで動作できる半導体回路において内部電圧電源を調整するためのシステムおよび方法に適用して有効な技術に関するものである。
【０００２】
【従来の技術】
多くの技術的進歩によって、集積回路、すなわち「チップ」は単一のモノリシックデバイス上に数百万ものトランジスタを組み込んだものとなっている。それにより、速度の向上およびサイズの減少をはじめとして、多くの利益が得られている。しかし、トランジスタの数が多くなるにつれ、チップ速度、消費電力、信頼性がより関心を引くようになっている。その結果、多くのチップについて外部プラス電源電圧は低下してきている。例えば、従来の１６Ｍビットダイナミックランダムアクセスメモリ（ＤＲＡＭ）は5.０Ｖか3.３Ｖの外部プラス電源を用いているが、２５６ＭビットＤＲＡＭでは3.３Ｖか2.５Ｖの外部プラス電源を用いている。低い外部プラス電源電圧を用いるとＤＲＡＭの速度を遅くさせるかもしれないが、消費電力は減少できる。さらに、薄いトランジスタのゲートや薄いメモリセルの誘電体に非常に高い電界強度を加えることにより引き起こされる破壊等の信頼性の問題を減少させることもできる。
【０００３】
ＤＲＡＭの外部プラス電源電圧をユーザーが選択可能とする傾向も１６ＭＤＲＡＭ以来存在している。図１ａおよび図１ｂを参照すると、従来の１６ＭビットＤＲＡＭには、５Ｖの外部プラス電源（ＶＤＤ）に接続された５Ｖバージョンデバイス１０ａと、3.３ＶのＶＤＤに接続された3.３Ｖバージョンデバイス１０ｂが存在する。両方のバージョン１０ａ、１０ｂとも接地電位の外部電源（ＶＳＳ）にも接続されている。多くの部分に関して５Ｖバージョンデバイス１０ａと3.３Ｖバージョンデバイス１０ｂは同一である。しかし、５Ｖバージョンデバイス１０ａにおいては、電圧レギュレータ１２はＶＤＤ電圧を、メモリセルおよび周辺回路１３ａのために約3.３Ｖの内部電圧レベル（ＶＩＮＴ）に調整している。
【０００４】
ＶＩＮＴは、ＤＲＡＭのメモリセルアレイの小さなメモリセル回路を動かすため、また、ＤＲＡＭの消費電力を減少させるために、比較的低電圧でなければならない。しかし、出力回路１３ｂはより高いＶＤＤ電圧で動作する。このようにして、出力回路１３ｂの速度は増強され、出力回路は所望の電圧レベルで動作する。一方、3.３Ｖバージョンデバイス１０ｂの場合は、3.３Ｖは既に外部プラス電源ＶＤＤによって供給されている。従って、3.３Ｖバージョンデバイス１０ａの場合、外部プラス電源電圧が既にＶＩＮＴあるいはそれに近い電圧であるため、メモリセルアレイおよび周辺回路１３ａと出力回路１３ｂは同じＶＤＤ電圧レベルで動作するので、５Ｖバージョンデバイス１０ａのレギュレータ１２のようなレギュレータは存在しない。
【０００５】
外部プラス電源が選択可能なチップに対する要求を満たすために、チップの設計はマスタスライス技術を採用する。チップを設計する際、多くのマスク層からなるマスクセットが作られる。マスク層はチップを製造する際に用いられるフォトマスクのことを示す。例えば、米国特許５，４８９，５０９に記載されているフォトマスクを用いて半導体装置を製造する方法がある。マスタスライス技術では、チップの各バージョンを製造するために用

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いられるマスク層は１つだけを除いてすべて同じとされている。図１を再び参照すると、５Ｖバージョンデバイス１０ａは、ＶＤＤをレギュレータ１２に向かわせ、調整された電圧を対応する回路に向かわせる配線１２ａを含む第１の配線層が形成されている。一方、3.３Ｖバージョンで１０ｂでは、ＶＤＤ電圧を直接対応する回路に向かわせる配線１２ｂを含む第２の配線層が形成されることになる。

【０００６】

【発明が解決しようとする課題】

ところが、このような単純なマスタスライス技術は２５６ＭビットＤＲＡＭでは同じようには有効でない。２５６ＭビットＤＲＡＭのメモリセルで用いられる誘電体は、誘電漏れ特性とメモリセルの安定性とをバランスさせる非常に小さな内部電圧を必要とするのに対して、周辺回路は、速度と消費電力をバランスさせる他の内部電圧を要求する。さらに、付加的な電圧レギュレータも必要とされるが、その各々はそれぞれに関し多くの設計上の問題を有している。例えば、電圧レギュレータに対する外部プラス電源が非常に低い場合、レギュレータが有効な電流出力を供給することは困難である。また、外部プラス電源が高い場合には、チャージポンプ電圧レギュレータのノードのいくつかが極端に高い電圧に達することがあり、信頼性の問題を引き起こす。最後の点として、従来の電圧レギュレータは、出力電圧を一定のレベルに維持するように出力電圧を充放電することができない。

【０００７】

本発明の目的は、多くの異なる外部プラス電圧に対して出力が一定である電圧レギュレータを複数備えた回路およびそのための方法を提供することにある。

【０００８】

本発明の前記ならびにその他の目的と新規な特徴は、本明細書の記述および添付図面から明らかになるであろう。

【０００９】

【課題を解決するための手段】

本願において開示される発明のうち、代表的なものの概要を簡単に説明すれば、以下のとおりである。

【００１０】

すなわち、本発明の好適な実施形態においては、マスタスライス技術を採用することにより、電圧レギュレータは２つの異なる範囲の外部プラス電源電圧に適応することができる。以下、４種類のレギュレータ技術を開示する。第１の電圧レギュレータの場合、レギュレータの電流供給能力は、外部プラス電源電圧が非常に低い状態下においてもかなり増大されている。第２のチャージポンプ電圧レギュレータの場合には、レギュレータの任意のノードにおける電圧レベルは予め定められた高電圧レベルを超えることはなく、しかも、外部プラス電源からの電流のほとんどを下げる。第３の電圧レギュレータは、その出力電圧を充放電して、出力電圧を一定のレベルに維持することができる。最後に、第４の電圧レギュレータは、誘電漏れを減少させるように最適化されたものである。

【００１１】

【発明の実施の形態】

以下、本発明の実施の形態を図面に基づいて詳細に説明する。

【００１２】

上述したように、図１ａおよび図１ｂは従来の１６Ｍビットダイナミックランダムアクセスメモリ（ＤＲＡＭ）デバイスの５Ｖバージョンデバイス１０ａおよび3.３Ｖバージョンデバイス１０ｂをそれぞれ示すものである。

【００１３】

図２ａおよび図２ｂを参照すると、参照番号２０ａおよび２０ｂは本発明の一実施形態のデバイスの3.３Ｖバージョンおよび2.５Ｖバージョンをそれぞれ全体として示すものである。本発明の好適な実施形態では、3.３Ｖバージョンデバイス２０ａおよび2.５Ｖバージョンデバイス２０ｂは２５６ＭビットＤＲＡＭであるが、本発明はＤＲＡＭへの適用に限定されることはなく、異なる内部電源レベルを必要とする外部プラス電源を選択可能な任

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意の集積回路デバイス、例えば、プログラマブル論理アレイや他のタイプのランダムアクセスメモリ等に関連して適用することができる。さらに、好適な実施形態において列挙された電圧レベルは例示のためのものであって、本発明を限定するものではない。

【００１４】

3.３Ｖバージョンデバイス２０ａおよび2.５Ｖバージョンデバイス２０ｂは外部プラス電源（ＶＤＤ）と０Ｖ（接地電位）の外部接地電源（ＶＳＳ）を受け取るが、ＶＤＤ電圧は3.３Ｖバージョンデバイス２０ａに関しては標準値が3.３Ｖ、2.５Ｖバージョンデバイス２０ｂに関しては標準値が2.５Ｖであり、ＶＳＳ電圧は両方のデバイスに関して０Ｖ（接地電位）である。3.３Ｖバージョンデバイス２０ａと2.５Ｖバージョンデバイス２０ｂはほとんどの部分が同一であり、どちらもそれぞれの周辺回路２１ａ、出力回路２１ｂ、およびメモリセルアレイ２１ｃを有している。さらに、両方のバージョンデバイス２０ａ、２０ｂとも、約2.０Ｖのアレイ電圧（ＶＡＲＹ）をメモリセルアレイ２１ｃに供給する第１の電圧レギュレータ回路２２および第２の電圧レギュレータ回路２４を有している。しかし、3.３Ｖバージョンデバイス２０ａの場合には、第２の電圧レギュレータ２４が約2.５Ｖの内部電圧（ＶＰＥＲＩ）を周辺回路２１ａへ供給している。

【００１５】

電圧レギュレータ２２、２４は様々な目的のために用いられる。まず第１に、メモリセルアレイ２１ｃのメモリセルで用いられる薄い（３－４ｎｍ）誘電体を動作させるためにＶＡＲＹは非常に低く、また、安定していなければならない。ＶＡＲＹをそのように低くすることによりリーク電流特性は最小に保たれ、同時にメモリセルの高い安定性を維持することができる。第２の点として、周辺回路２１ａが含むトランジスタはゲートの厚さ（９－１０ｎｍ）がメモリセルの誘電体の厚さ（３－４ｎｍ）より厚いので、ＶＰＥＲＩはＶＡＲＹより高い電圧をとることが可能である。周辺回路２１ａの回路の数は比較的多いが、ＶＰＥＲＩを中間の電圧（ＶＡＲＹ＜ＶＰＥＲＩ＜ＶＤＤ）とすることにより、それら回路による消費電力をそれほど増大させることなく、周辺回路２１ａの動作速度を向上させることができる。出力回路２１ｂはＶＤＤ電圧で動作する。このようにして、出力回路２１ｂの動作速度は増大し、出力信号の電圧レベルは所望の動作レベルとすることができる。また、出力回路の消費電力はＶＤＤが高い電圧であるために増加するが、出力回路２１ｂの回路数が比較的少ないため、その消費電力は許容できる範囲である。

【００１６】

一方、2.５Ｖバージョンデバイス２０ｂの場合には、ＶＤＤ電圧（2.５Ｖ）がＶＰＥＲＩ（2.５Ｖ）に等しいので、図２ａの第２の電圧レギュレータ２４は必要ではない。従って、3.３Ｖバージョンデバイス２０ａが、ＶＰＥＲＩおよびＶＡＲＹをそれぞれ供給するための第１および第２の電圧レギュレータ２２、２４を用いるように、配線２４ａを含む第１の配線層を形成するための第１のマスク層（図示せず）を用いてマスタスライス技術を採用する。第１のマスク層の代わりに配線２４ｂを含む第２の配線層を形成するための第２のマスク層（図示せず）を用いることにより、2.５Ｖバージョンデバイス２０ｂが、やはりＶＡＲＹを供給するための第１の電圧レギュレータ２２を用いるようにすることができる。しかし、2.５Ｖバージョンデバイス２０ｂは第２の電圧レギュレータ２４は用いず、外部電源ＶＤＤが直接ＶＰＥＲＩとして供給される。

【００１７】

図３ａおよび図３ｂを参照すると、3.３Ｖバージョンおよび2.５Ｖバージョンの両方が、内部電圧ＶＡＲＹおよびＶＰＥＲＩの電圧調整に加えて、これとは別の内部電圧ＶＰＰ、ＶＢＢ、ＶＢＬＲおよびＶＰＬＴを生成し、用いている。ＶＰＰは3.６Ｖであってワード線ドライバに用いられ、ＶＢＢは－1.０Ｖで、様々なＮＭＯＳトランジスタのバックバイアスとして用いられ、ＶＢＬＲは1.０Ｖで、ビット線のプリチャージレベルとして用いられ、ＶＰＬＴは0.５Ｖで、メモリセルキャパシタのプレート電圧として用いられる。内部電圧ＶＡＲＹ、ＶＰＥＲＩ、ＶＰＰ、ＶＢＢ、ＶＢＬＲ、およびＶＰＬＴについては後で詳細に説明する。

【００１８】

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特に、図３ａのブロック図を参照すると、このブロック図は図２ａの3.３Ｖバージョンデバイス２０ａに対応するものであるが、内部電圧ＶＡＲＹ、ＶＰＥＲＩ、ＶＰＰ、ＶＢＢ、ＶＢＬＲ、およびＶＰＬＴは、様々な電源線および信号線により相互に接続されている６個の電圧レギュレータ２６、２８、３０、３２、３４および３６により調整される。中間電圧レギュレータ２６は、第１の中間電圧Ｖ１および第２の中間電圧Ｖ２を生成し、Ｖ１電圧は1.２５Ｖであり、Ｖ２電圧は1.０Ｖである。Ｖ１はＶＰＥＲＩレギュレータ２８に供給され、このレギュレータは図６を参照して詳細に説明されるようにＶ１の２倍の電圧ＶＰＥＲＩ＝2.５Ｖを生成する。ＶＰＥＲＩはまた、従来のＶＢＢレギュレータ３４とＶＰＰレギュレータ３２に供給され、これについては図７を参照して詳細に説明する。

【００１９】

同様に、Ｖ２はＶＡＲＹレギュレータ３０に供給され、このレギュレータは図９を参照して詳細に説明するようにＶ２の２倍の電圧ＶＡＲＹ＝2.０Ｖを生成する。ＶＡＲＹはまた、ＶＢＬＲおよびＶＰＬＴレギュレータ３６に供給され、これについては図１２を参照して詳細に説明する。

【００２０】

図３ｂのブロック図を参照すると、このブロック図は図２ｂの2.５Ｖバージョンデバイス２０ｂに対応するものであり、内部電圧ＶＡＲＹ、ＶＰＥＲＩ、ＶＰＰ、ＶＢＢ、ＶＢＬＲ、およびＶＰＬＴが、図３ａを参照して上述したのと同様の方法で生成されるが、ＶＰＥＲＩが直接ＶＤＤにより供給される点だけが異なっている。

【００２１】

図３ａおよび図３ｂの両方を参照すると、それらの図に示された破線により、この好適な実施形態においてマスタスライス技術がどのように実現されているかが示されている。マスタスライス技術では、3.３Ｖバージョン（図３ａ）と2.５Ｖバージョン（図３ｂ）を製造するために、同一の金属配線層形成行程のための第１および第２のマスク層（図示せず）のどちらかを必要とする。3.３Ｖバージョンのための第１のマスク層は、第１の配線層を形成するために用いられ、2.５Ｖバージョンのための第２のマスク層は、第２の配線層を形成するために用いられる。このようにして、デバイスの目的に対応して、第１のマスク層または第２のマスク層のどちらかを用いる。

【００２２】

第１のマスク層は、3.３Ｖバージョン（図３ａ）で用いられるものであり、外部プラス電源ＶＤＤをＶＰＲＥＩに接続する図３ａに破線として示されている配線４０を形成せず、レギュレータ２６、２８、３０、３２、３４、３６を相互接続する配線４２、４４を含む第１の配線層を形成するために用いられる。同様に、第２のマスク層は、2.５Ｖバージョン（図３ｂ）で用いられるものであり、図３ｂに破線として示されているＶＰＲＥＩレギュレータ２８を接続する配線４２および４４を形成せず、レギュレータ２６、２８、３０、３２、３４、３６を相互接続する配線４０を含む第２の配線層を形成するために用いられる。

【００２３】

図４ａを参照すると、3.３Ｖバージョン（図３ａ）の３つの内部電圧ＶＰＰ、ＶＰＥＲＩおよびＶＡＲＹがＶＤＤの関数として示されている。ＶＤＤの第１の通常動作範囲５０は3.３Ｖ±１０％、すなわち約3.０Ｖ～3.６Ｖの間にある。第１の通常動作範囲５０において、内部電圧ＶＰＰ、ＶＰＥＲＩおよびＶＡＲＹはそれぞれ3.６Ｖ、2.５Ｖおよび2.０Ｖで一定である。ＶＤＤが4.１Ｖ以上の信頼性／バーンイン試験で用いられる第１のストレス範囲５２においては、内部電圧ＶＰＰ、ＶＰＥＲＩおよびＶＡＲＹはＶＤＤ電圧と共に変化し、ＶＰＰはＶＤＤに等しく、ＶＰＥＲＩはＶＤＤ－0.７５Ｖに等しく、ＶＡＲＹはＶＤＤ－1.５Ｖに等しい。パワーアップ動作あるいはバッテリバックアップ動作の際に用いられる、ＶＤＤが2.２Ｖ～2.７Ｖの間にある第１の低電圧範囲５３においては、ＶＡＲＹはやはり2.０Ｖであるが、ＶＰＥＲＩはＶＤＤに等しくする。最後に、やはりパワーアップの際に用いられるＶＤＤが2.２Ｖより小さな第２の低電圧範囲５４においては、ＶＡＲＹおよびＶＰＥＲＩの両方がＶＤＤに等しくする。

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【００２４】
図４ｂを参照すると、2.５Ｖバージョン（図３ｂ）の３つの内部電圧ＶＰＰ、ＶＰＥＲＩおよびＶＡＲＹがＶＤＤの関数として示されている。ＶＤＤの第２の通常動作範囲５６は2.５Ｖ±１０％、すなわち約2.２５Ｖ～2.７５Ｖの間にある。第２の通常動作範囲５６の全体にわたって、内部電圧ＶＰＰおよびＶＡＲＹはそれぞれ3.６Ｖおよび2.０Ｖで一定であり、3.３Ｖバージョン（図４ａ）の場合と同じ電圧である。しかし、ＶＰＥＲＩはＶＤＤ電圧に等しいままである。ＶＤＤが3.２Ｖより大きな第２のストレス範囲５８においては、ＶＰＰはＶＤＤ＋0.７５Ｖであり、ＶＰＥＲＩはＶＤＤ電圧に等しく、ＶＡＲＹはＶＤＤ－0.７５Ｖに等しい。最後に、ＶＤＤが2.２Ｖより小さな第３の低電圧範囲６０においては、ＶＡＲＹおよびＶＰＥＲＩの両方がＶＤＤ電圧に等しい。

【００２５】
図５を参照すると、２５６ＭビットＤＲＡＭの3.３Ｖバージョンデバイス２０ａおよび2.５Ｖバージョンデバイス２０ｂの単純化された要部回路図において、内部電圧ＶＡＲＹ、ＶＰＥＲＩ、ＶＰＰ、ＶＢＢ、ＶＢＬＲ、およびＶＰＬＴの適用が示されている。アドレス信号（図示せず）は入力ポートＩＮＰＵＴを通過し、アドレスバッファ６２に印加される。アドレスバッファ６２はＶＤＤで動作し、他のチップ（図示せず）とインタフェイスを一致させる。アドレスバッファ６２はアドレス信号をアドレスデコーダ６４へと駆動する。アドレスデコーダ６４はＶＰＥＲＩで動作するが、それはＶＰＥＲＩが高速度（高電圧）と低消費電力（低電圧）との間の良好なバランスを提供するからである。アドレスデコーダ６４は、デコーダ信号を、ＶＰＰで動作するワード線ドライバ６６へ印加する。

【００２６】
ワード線ドライバ６６はワード線ＷＬを駆動し、ワード線ＷＬはメモリセル（ビット）Ｂ１を選択する。ビットＢ１は、ＶＡＲＹ（2.０Ｖ）とＶＳＳ（０Ｖ）との間にあるビット電圧ＶＳＮを蓄えている。ビット電圧ＶＳＮがＶＡＲＹとなるかもしれないので、ワード線ドライバ６６は、ＶＡＲＹにＮチャネル金属酸化物半導体（ＮＭＯＳ）トランジスタ６８の閾値電圧（図示せず）を足し、さらに、速度および電圧の変化を調節するための付加的な電圧を足したものより十分に高い電圧ＶＰＰで動作する。トランジスタ６８はＶＢＢにバイアスされたウェル６８Ｗを有しており、それによりトランジスタ６８のリーク電流（図示されていない）および接合容量（図示せず）が減少される。ビットＢ１はまた、キャパシタＣ１を含んでおり、キャパシタＣ１のプレートはＶＰＬＴに接続されている。ＶＰＬＴのレベルはＶＡＲＹとＶＳＳとの間にあり、キャパシタＣ１のリーク電流を最小にするように最適化されているが、これについては後で図１２を参照して詳細に説明する。

【００２７】
ビットＢ１はビット電圧ＶＳＮをビット線ＢＬに読み出し、そしてセンスアンプ回路６９に接続される。センスアンプ回路６９は、ビット線信号電圧を増幅するためのアンプセクション７０を備える。アンプセクション７０はセンスアンプオーバードライブ回路７１により、信号線ＳＤＮおよびＳＤＰを介して駆動されている。オーバードライブ回路７１は３つのドライブ信号ＳＡＰ１、ＳＡＰ２およびＳＡＮを受け取り、信号線ＳＤＮをＶＳＳへと駆動し、ＳＤＰをＶＡＲＹあるいはＶＤＤのどちらかへと選択的に駆動する。ＶＡＲＹおよびＶＳＳは、ビット線ＢＬに対するそれぞれＨｉｇｈおよびＬｏｗの目標電圧である。センスアンプ増幅動作時に、ＶＤＤはビット線ＢＬをＳＡＰ１がＬｏｗの短い期間だけオーバードライブするために用いられる。その後ＳＡＰ１がＨｉｇｈレベル、ＳＡＰ２がＬｏｗレベルになり、ビット線の最終電圧はＶＡＲＹ又はゼロとなる。センスアンプ回路６９はまた、ビット線ＢＬをプリチャージするためのイコライザセクション７２を有している。イコライザセクション７２は、ビットＢ１がワード線ＷＬにより選択される前にビット線ＢＬがＶＡＲＹとＶＳＳとの中間電圧のＶＢＬＲとなるように信号ＢＬＥＱにより制御される。

【００２８】
増幅されたビット線電圧（図示せず）は、列選択信号ＹＳにより選択的に出力線Ｉ／Ｏへと接続される。次いで、出力線Ｉ／Ｏはメインアンプ７４を駆動する。メインアンプ７４

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は、アドレスデコーダ６４に関連して先に説明したのと同じ理由で、ＶＰＥＲＩで動作する。最後に、メインアンプ７４は出力バッファ７６を駆動するが、出力バッファ７６は、前述の入力バッファ６２に関連して先に説明したのと同じ理由で、ＶＤＤで動作する。

【００２９】

図６を参照すると、3.３Ｖバージョン（図３ａ）において参照番号２８によって本発明による改善されたＶＰＥＲＩレギュレータが示されている。ＶＰＥＲＩレギュレータ２８は中間電圧Ｖ１（図３ａ）、ＶＤＤおよびＶＳＳと、ＡＣＴＶ信号およびＤＥＴＥＣＴ１Ｂ信号とを用いている。ＡＣＴＶ信号は3.３Ｖバージョンデバイス２０ａ（図２ａ）が活性状態のときＨｉｇｈレベルであり、3.３Ｖバージョンデバイス２０ａが待機モードのときにＬｏｗレベルである。ＡＣＴＶ信号は特に言及されない場合にはＨｉｇｈレベルとして説明する。

【００３０】

図７および図８を参照すると、参照番号８２より、レベル変換機能付きインバータ回路８２（図７）と、ＤＥＴＥＣＴ１信号およびＤＥＴＥＣＴ１Ｂ信号のＶＤＤ外部プラス電源ＶＤＤの依存性（図８）が示されている。ＤＥＴＥＣＴ１Ｂ信号はレベル変換機能付きインバータ回路８２により生成される。このＤＥＴＥＣＴ１Ｂ信号は、ＶＰＲＥＩレギュレータ回路２８（図６）のプルアップＰＭＯＳトランジスタ９０のゲートに印加される。レベル変換機能付きインバータ回路８２は外部プラス電源（ＶＤＤ）電圧、外部接地電源（ＶＳＳ）電圧の他に負電圧のＶＢＢを利用している。なお、ＶＢＢは公知のバックバイアス電圧発生回路（図示せず）の出力電圧である。レベル変換機能付きインバータ回路８２はＤＥＴＥＣＴ１信号を入力とし、ＤＥＴＥＣＴ１Ｂ信号を出力とする。なお、ＤＥＴＥＣＴ１信号は電源電圧レベルセンサ回路（図示せず）の出力信号である。電源電圧レベルセンサ回路は，ＶＤＤ電圧の所定の電圧を分圧した電圧と一定の基準電圧とを比較する差動アンプ回路で容易に実現できる。そして、第１の低電圧範囲５３（図８）内の最大ＶＤＤ電圧（ＶＤＤ＝2.７Ｖ）でその分圧電圧が基準電圧と等しくなるように分圧比または基準電圧を設定する。このことから、外部プラス電源（ＶＤＤ）電圧が第１の低電圧範囲５３内の最大ＶＤＤ電圧よりも高ければ分圧電圧は基準電圧より高くなる。ＶＤＤ電圧が第１の低電圧範囲５３の最大ＶＤＤ電圧よりも低ければ分圧電圧は基準電圧より低くなる。この比較結果として、レベル変換機能付きインバータ回路８２は差動アンプ回路の出力信号のＤＥＴＥＣＴ１信号をＤＥＴＥＣＴ１Ｂ信号に変換する。つまり、ＶＤＤ電圧が通常動作範囲５０（図４ａまたは図８、3.０～3.６Ｖ）のとき、ＤＥＴＥＣＴ１信号は０Ｖ（接地電位）である。ＶＤＤ電圧が第１の低電圧範囲５３または第２の低電圧範囲５４（図４ａまたは図８、ＶＤＤ≦2.７Ｖ）にあるとき、ＤＥＴＥＣＴ１信号はＶＤＤ電圧レベルである。そして、ＤＥＴＥＣＴ１信号が０Ｖ（接地電位）のとき、ＤＥＴＥＣＴ１Ｂ信号はＶＤＤ電圧レベルである。ＤＥＴＥＣＴ１信号がＶＤＤ電圧レベルのとき、ＤＥＴＥＣＴ１Ｂ信号はＶＢＢレベルとなる。このようにＤＥＴＥＣＴ１Ｂ信号がＶＢＢレベルという低い電圧レベル（図８）を有することの利益については後に説明する。

【００３１】

図６を参照すると、ＶＰＥＲＩレギュレータ２８は差動回路８４、分圧回路８６および第１および第２のプルアップＰチャネル金属酸化物半導体（ＰＭＯＳ）トランジスタ８８および第２のプルアップＰＭＯＳトランジスタ９０を有している。分圧回路８６は出力電圧９２を生成するが、その電圧はＶＰＥＲＩ（通常2.５Ｖ）の２分の１、すなわち1.２５Ｖである。この半電圧基準法は、トランジスタ８８の低ＶＤＤでの電流供給能力を増大させるという利益がある。出力電圧９２は差動回路８４により中間電圧Ｖ１（＝1.２５Ｖである（図３ａ））と比較される。ＶＰＥＲＩが下降すると出力電圧９２も下降し、差動回路８４は第１のプルアップＰＭＯＳトランジスタ８８をさらにアクティブとし、第１のＰＭＯＳトランジスタ８８はＶＰＥＲＩを2.５Ｖに向けて回復させる。

【００３２】

図４ａを参照すると、3.３Ｖバージョンデバイス２０ａ（図２ａ）が第１の低電圧範囲５３および第２の低電圧範囲５４の１つにあるとき、ＤＥＴＥＣＴ１Ｂ信号の電圧レベルは

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ＶＢＢに等しく、第２のプルアップトランジスタ９０もアクティブとされる。その結果、第２のプルアップトランジスタ９０のゲート－ソース間電圧（図示せず）は非常に高くなり、第２のプルアップＰＭＯＳトランジスタ９０の電流供給能力は高いものとなり得る。それで、第１の低電圧範囲５３および第２の低電圧範囲５４のすべてにわたってＶＰＥＲＩはＶＤＤ電圧に等しく、これは第１のプルアップＰＭＯＳトランジスタ８８と並列な第２のプルアップトランジスタ９０の並列加算動作による高電流駆動能力によるものである。

【００３３】

図６および図７の両方を参照すると、それらの破線により、この好適な実施形態においてマスタスライス技術でどのように実現されているかが示されている。マスタスライス技術では、3.３Ｖバージョンのための第１のマスク層（図示せず）は、破線で示される配線を除いた第１の配線層を形成するために用いられる。また、2.５Ｖバージョンのための第２のマスク層（図示せず）は、破線で示される配線を含む第２の配線層を形成するために用いられる。

【００３４】

3.３Ｖバージョンの場合、ＶＰＲＥＩレギュレータ２８が中間電圧Ｖ１からＶＰＲＥＩを出力できるように第１のマスク層は、破線で示される配線２８ａ、２８ｂ（図６）、および８２ａ（図７）を除いた第１の配線層を形成するために用いられる。また、2.５Ｖバージョンの場合、ＶＰＲＥＩレギュレータが中間電圧Ｖ１からＶＰＲＥＩを出力できないように第２のマスク層は、破線で示される配線２８ａ、２８ｂ（図６）および８２ａ（図７）を含む第２の配線層を形成するために用いられる。その結果、ＶＤＤ（＝2.５Ｖ）電圧を出力できるようにする。

【００３５】

比較的サイズの大きなチップ（図１９）におけるＶＰＥＲＩレギュレータ２８の性能をさらに向上させるために、チップの周りの様々な位置に多重レギュレータ（図１９）が複数配置される。このようにして、長いＶＰＥＲＩ電源線（図示せず）の配線抵抗によって引き起こされる電圧下降はかなり減少させられる。

【００３６】

図９を参照すると、参照番号９４により従来のＶＰＰレギュレータが示されている。ＶＰＰレギュレータ９４は電源電圧９６（これはＶＤＤあるいはＶＰＥＲＩのどちらかに接続される）と、ＶＰＰレベルセンサからの出力電圧ＶＯＳＣとを用いている。電圧レギュレータ９４は、外部プラス電源ＶＤＤ電圧９６を２倍にすることにより電源電圧９６よりも高い電圧ＶＰＰを生成する。電源電圧は、ＶＤＤとＶＳＳとの間を振動するＶＯＳＣによりポンピングすることにより原理的には２倍にされる。ＶＯＳＣによるポンピングは、3.６Ｖの定常電圧レベル（ＶＡＲＹ（2.０Ｖ）＋1.６Ｖ）に調整するためＶＰＰレベルセンサ９８により制御されている。こうしてＶＰＰは、２倍のＶＤＤレベルまで到達しないもののＶＰＰレベルセンサ９８により制約され、十分に強い状態を維持する。

【００３７】

電源電圧９６がＶＤＤに接続される従来のＶＰＰレギュレータの第１の形態の場合、電圧レギュレータ回路９４は信頼性の問題が生じる。これは、ＶＤＤ電圧が上昇し4.０Ｖのとき、内部ノード電圧（図示せず）は8.０Ｖ（ＶＤＤ＋ＶＤＤ）を超えることがあり、信頼性を保ち続けるためには、従来のＶＰＰレギュレータ９４は8.０Ｖを超える内部ノードを持たないようにしなければならないからである。電源電圧９６がＶＰＥＲＩに接続される従来の第２の形態の場合には、ＶＤＤが4.０Ｖのとき、どの内部ノード電圧も8.０Ｖを超えることはないが、他の問題が生じる。例えば、従来のＶＰＰレギュレータ９４は、入力電流に対する出力電流の比（電流効率）が５０％である。すなわち、従来のＶＰＰレギュレータは、２０ｍＡの電源電流を飲み込むごとに１０ｍＡの出力電流を供給する。従って、従来の第２の形態の場合、電圧レギュレータ９４はＶＰＥＲＩ電圧レギュレータ（図６）において極端に電流を消費し過負荷となってしまう。

【００３８】

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図１０を参照すると、参照番号３２によって本発明による改善されたＶＰＰレギュレータが示されている。ＶＰＰレギュレータ３２は、3.３Ｖバージョンデバイス２０ａ（図２ａ）および2.５Ｖバージョンデバイス２０ｂ（図２ｂ）の両方で用いられる。ＶＰＰレギュレータ３２は、ＶＤＤおよびＶＰＥＲＩの両方と発振器からの出力電圧ＶＯＳＣとを用いている。ＶＤＤおよびＶＰＥＲＩの両方を用いることにより、ＶＤＤ電圧が4.０Ｖより高い場合にも、ノードＮ２を含めＶＰＰレギュレータ３２のどの内部ノードも8.０Ｖの電圧を超えることはない。すなわち、ＶＰＥＲＩの低電圧レベルにより、ノードＮ２の電圧はＶＤＤ＋ＶＰＥＲＩ、すなわち6.５Ｖに減少されている。さらに、ＶＰＰレギュレータ３２はその入力電流－出力電流比がやはり約５０％であるものの、ＶＰＰレギュレータ３２は入力電流（図示せず）の大部分を外部プラス電源ＶＤＤから飲み込むように設計されており、それによりＶＰＥＲＩレギュレータ２８（図６）における電流の消費は減少される。

【００３９】

図１１を参照すると、参照番号３２によって、図１０の本発明による改善されたＶＰＰレギュレータが示されている。ＶＰＰレギュレータ３２ではＶＰＰを生成するためにＶＤＤおよびＶＰＥＲＩの両方が用いられている。ＶＰＰレギュレータ３２は、複数のＮＭＯＳトランジスタ９９ａ、９９ｂ、９９ｃ、９９ｄ、９９ｅ、９９ｆ、９９ｇ、９９ｈ、９９ｉと、ＰＭＯＳトランジスタ１００と、複数のコンデンサＣ２、Ｃ３、Ｃ４、Ｃ５、Ｃ６と、複数のインバータ１０１ａ、１０１ｂ、１０１ｃ、１０１ｄ、１０１ｅとを有しており、１０１ｄ、１０１ｅを除く各インバータはＶＤＤ電圧レベルで動作する。これらトランジスタおよびインバータは、それらの印加電圧によりグループ分けされる。ＶＤＤ印加はＮＭＯＳトランジスタ９９ｂ、９９ｃ、９９ｄとインバータ１０１ａ、１０１ｂ、１０１ｃである。一方、ＶＰＥＲＩ印加はＮＭＯＳトランジスタ９９ｅと、インバータ１０１ｄ、１０１ｅである。ＶＰＰレギュレータ３２の動作は、さらに、ノードＮ１、Ｎ２、Ｎ３、Ｎ４、Ｎ５、Ｎ６、Ｎ７、Ｎ８およびＮ９における信号を検討することにより説明される。

【００４０】

図１２をも参照すると、ノードＮ８およびＮ９における信号の波形は、ノードＮ７における信号およびＶＯＳＣの波形を逆転したものである。ノードＮ１における信号の波形は、９９ａによりプリチャージされたＶＰＥＲＩをノードＮ７におけるコンデンサＣ２へのＶＤＤ振幅信号によりポンピングすることにより生成されている。ノードＮ２における信号の波形は、９９ｈによりプリチャージされたＶＰＥＲＩをノードＮ８におけるコンデンサＣ３へのＶＤＤ振幅信号によりポンピングすることにより生成されている。ノードＮ５における信号の波形は、ＶＯＳＣとノードＮ９、Ｎ４およびＮ６における信号とを組み合わせることにより生成されている。ノードＮ３における信号の波形は、９９ｆによりプリチャージされたＶＰＥＲＩをノードＮ５におけるコンデンサＣ４への２倍のＶＰＥＲＩ振幅の信号によりポンピングすることにより生成されている。その結果、ノードＮ２におけるＨｉｇｈレベルはＶＤＤ電圧とＶＰＥＲＩ（2.５Ｖ）のに和に等しい。また、Ｎ３のＨｉｇｈ電圧は３倍のＶＰＥＲＩである。９９ｉは整流用トランジスタである。コンデンサＣ６は大きなデカップリングコンデンサであって、ＶＰＰ電圧の変動を防止するのに助けとなっている。

【００４１】

図１１のＶＰＰレギュレータ３２の有利な他の点は、ゲート－ソース間電圧が信頼性限界を超えるトランジスタは１つも用いずにＶＰＰレベルが生成されていることである。また、９９ｂ、９９ｃ、９９ｄ、９９ｅと１０１ｃは電圧緩和のために工夫した回路である。上述の実施形態においては、ＰＭＯＳトランジスタ１００の定常的なゲート－ソース間電圧はＶＰＥＲＩ（2.５Ｖ）である。ノードＮ９がＶＤＤ（3.３Ｖあるいは2.５Ｖ）に等しい場合、ノードＮ５はＶＰＥＲＩの２倍（5.０Ｖ）であり、そのためＮＭＯＳトランジスタ９９ｂは2.５Ｖの最大ゲート－ソース間電圧となる。ノードＮ３がＶＰＥＲＩの３倍（7.５Ｖ）に等しい場合、ノードＮ２はＶＰＥＲＩ＋ＶＤＤ（5.０Ｖあるいは5.８Ｖ）であ

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り、そのためＮＭＯＳトランジスタ９９ｉは2.５Ｖの最大ゲート－ソース間電圧となる。同様に、残りのトランジスタについても、ゲート－ソース間電圧は比較的低いものとなる。

【００４２】

図１３を参照すると、参照番号３０によりＶＡＲＹレギュレータが示されている。その図に示されているように、ＶＡＲＹレギュレータ３０は一連の信号線ＳＤＰ１、ＳＤＰ２、ＳＤＰ３等を駆動しており、これら信号線は、先に、図５を参照して全体としてＳＤＰとして参照され、説明されたものである。オーバードライブセンスアンプ動作によりＶＤＤも信号線ＳＤＰを駆動するので、２つのドライブ信号ＳＡＰ１およびＳＡＰ２（図５をも参照）により、任意の１時点において２つの電圧ＶＤＤ電圧およびＶＡＲＹのどちらが信号線ＳＤＰを駆動するのかが制御される。

【００４３】

ＶＡＲＹレギュレータ３０は、第１の差動回路１０２と、分圧器１０４と、第１および第２のプルアップＰＭＯＳトランジスタ１０６および１０８を有している点で、図６のＶＰＥＲＩレギュレータ２８と類似している。ＶＡＲＹレギュレータ３０はまた、第２の差動回路１１０と、ＰＭＯＳトランジスタ１１２と、プルダウンＮＭＯＳトランジスタ１１４をも有している。ＶＡＲＹレギュレータ３０は中間電圧Ｖ２（1.０Ｖ）と、ＡＣＴＶ信号と、センスイネーブル信号ＳＡＥと、ＤＥＴＥＣＴ２Ｂとを受け取る。ＤＥＴＥＣＴ２Ｂ信号はプルアップＰＭＯＳトランジスタ１０８のゲートに印加されている。ＤＥＴＥＣＴ２Ｂ信号とＤＥＴＥＣＴ２信号の生成方法はＤＥＴＥＣＴ１信号、ＤＥＴＥＣＴ１Ｂ信号と同様である。つまり、分圧比または基準電圧の設定により、より低いＶＤＤ電圧（ＶＤＤ＝2.２Ｖ）でＤＥＴＥＣＴ２Ｂ信号が変化するように設定する。ＶＤＤ電圧が第２の低電圧範囲５４（図４ａ、ＶＤＤ≦2.２Ｖ）または第３の低電圧範囲６０（図４ｂ、ＶＤＤ≦2.２Ｖ）、ＤＥＴＥＣＴ２Ｂ信号はＶＢＢレベルになる。

【００４４】

図１４をも参照すると、動作はアクティブ期間１１６において発生し、この期間はいつもＡＣＴＶ信号がＨｉｇｈレベルとなることにより決定されている。この期間１１６において、ＶＡＲＹが低いときには、ＶＡＲＹレギュレータ３０はＶＰＥＲＩレギュレータ２８と同様にＶＡＲＹの本来の電圧に回復させるように機能する。しかし、ＶＡＲＹが逆に高い場合には、ＳＡＥ信号と、第２の差動回路１１０と、プルダウンＮＭＯＳトランジスタ１１４が働いてＶＡＲＹレベルが放電される。上述のように、ＶＡＲＹおよびＶＤＤ電圧の両方がＳＤＰ信号線を駆動している。オーバードライブの期間、信号線ＳＤＰはＶＤＤ電圧あるいはそれに近いレベルとなり、その後ＳＡＰ２をＬｏｗレベルにすると、ＶＡＲＹは一時的にＶＤＤ電圧に向かって上昇する。ＶＡＲＹレベルを放電して、それを再び2.０Ｖへと引き下げるために、ＳＡＥ信号（これはＶＡＲＹがＳＤＰ信号に接続された後にＨｉｇｈレベルとなる）は第２の差動回路１１０をして、分圧器１０４の出力と基準電圧Ｖ２とを比較させる。その結果、第２の差動回路１１０は、分圧回路１０４からの電圧レベルがＶ２（1.０Ｖ）に等しくなるまで、プルダウントランジスタ１１４をアクティブとするが、これはＶＡＲＹが2.０Ｖに等しくなることを意味している。

【００４５】

図５を再び参照すると、ビットＢ１はキャパシタＣ１を有しており、Ｃ１のプレートは ＶＰＬＴに接続され、キャパシタの対向電極がＶＳＳ又はＶＡＲＹのビット電圧ＶＳＮを蓄えている。図１５をも参照すると、ＶＰＬＴの電圧レベルは従来のようにＶＳＳ（０Ｖ）とＶＡＲＹ（2.０Ｖ）との中間、すなわち1.０Ｖに設定されている。これはSiO_2やSi_3N_4のような誘電体に関してうまく機能する。しかし、小さなメモリセルで大きなキャパシタ容量をとるため高誘電体Ta_2O_5を用いると、そのリーク電流特性は非対称である。例えば、ビット電圧ＶＳＮがＶＳＳに等しい場合、誘電体Ta_2O_5にはプラスのリーク電流Ｉ１が存在し、ビット電圧ＶＳＮがＶＡＲＹに等しい場合にはマイナスのリーク電流Ｉ２が存在する。この従来の形態の場合、リーク電流Ｉ１およびＩ２は非対称であり、すなわち、リーク電流Ｉ１はリーク電流Ｉ２に比較して不釣合いに大きい。こうして

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、リーク電流Ｉ１が大きすぎるため、キャパシタＣ１に蓄えられたデータを失わせてしまうことになる。

【００４６】

図１６を参照すると、本発明により、誘電体Ta_2O_5のリーク電流がより対称的となるようにＶＰＬＴのレベルが調節されている。この結果を達成するために、ＶＰＬＴの電圧レベルは0.５Ｖ、すなわち、ＶＡＲＹの４分の１というレベルに調節されている。それにより、ビット電圧ＶＳＮがＶＳＳに等しい場合には、プラスのリーク電流Ｉ３が生成され、ビット電圧ＶＳＮがＶＡＲＹに等しい場合には、マイナスのリーク電流Ｉ４が生成され、これらリーク電流Ｉ３、Ｉ４はかなり対称的で、どちらも比較的小さいものである。

【００４７】

図１７を参照すると、参照番号３６によって本発明による改善されたＶＢＬＲおよびＶＰＬＴレギュレータが示されている。ＶＢＬＲおよびＶＰＬＴレギュレータ３６は、ビット線プリチャージ電圧ＶＢＬＲおよびプレート電圧ＶＰＬＴを生成している。ＶＢＬＲ（1.０Ｖ）は第１の副回路１１８ａにより生成されるが、その第１の副回路１１８ａはＶＡＲＹ（2.０Ｖ）とＶＳＳ（０Ｖ）との丁度２分の１の電圧を生成するものである。第１の副回路１１８ａは、例えばＳａｔｏｅｔ　ａｌ．の米国特許４，８３９，８６５号に記載されているような、半電圧レギュレータであり、消費電流は非常に少ない。本発明はまた、ＶＢＬＲ（1.０Ｖ）とＶＳＳ（０Ｖ）との間に結合された第２の副回路１１８ｂをも含んでいる。

【００４８】

図１８を参照すると、第２の副回路１１８ｂは所望の電圧レベルＶＰＬＴ（0.５Ｖ）を生成する。しかし、その回路はＶＤＤパワーアップ時に大きな寄生容量の付いたＶＰＬＴをすばやく０Ｖから引き上げるほど負荷電流供給能力は強力ではない。ＶＰＬＴの負荷容量はすべてのメモリセルキャパシタの総和であり、極端に大きいからである。従って、ＶＤＤパワーアップの場合あるいはＶＤＤが第１、第２および第３の低電圧範囲５３、５４、６０（図４ａ、図４ｂ）の場合には、ＶＰＬＴをより電流供給能力の大きなＶＢＬＲに接続することにより、回路１２０を介してＶＰＬＴをすばやく引き上げることが可能となる。そのために回路１２０内のＮＭＯＳダイオードはＶＢＬＲとＶＰＬＴのレベル差を作るものである。ＶＢＬＲレベルはセンスアンプ回路６９のビット線ＢＬ、充放電動作（図５）を介して引き上げられる。最後に、ＶＤＤが時刻ｔ１において通常の動作レベルに到達すると、ディテクタ電圧ＶＵＰＢがＬｏｗに遷移することによりプルアップ回路１２０がディスエーブルとされ、第２の副回路１１８ｂがトランジスタ１２２を介してＶＰＬＴへと接続される。この時、ＶＢＬＲとＶＰＬＴは異なった電圧となる。

【００４９】

図１９を参照すると、参照番号１２３により複数の電圧レギュレータを配置した６４ＭビットまたはＭビットＤＲＡＭのチップ全体図が示されている。メモリチップ１２３の中で、ワード線は水平方向、ビット線は垂直方向としている。長辺方向に延びる領域１２７は周辺回路およびボンディングパッド領域であり、短辺方向に延びる領域１３２はメモリセルアレイ間領域である。本発明の各種の電圧レギュレータ（ＶＰＥＲＩ、ＶＡＲＹ、ＶＰＰ、ＶＢＢ、ＶＢＬＲＶ、ＶＰＬＴレギュレータ）は周辺回路およびボンディングパッド領域１２７または、メモリセルアレイ間領域１３２に配置されるのが好ましい。なぜなら、電圧レギュレータは回路素子寸法が大きく、またメモリチップ１２３に対する占有面積が大きいため、メモリセルアレイ１２８の周辺に配置するのが困難であるからである。そして、ＶＰＲＥＩレギュレータ、ＶＡＲＹレギュレータのような負荷電流の大きい回路はメモリチップ１２３中に分散して配置し、負荷電流による電圧の低下を減少させる。

【００５０】

以上、本発明者によってなされた発明を実施の形態に基づき具体的に説明したが、本発明は前記実施の形態に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。

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【００５１】
たとえば、ある電圧レギュレータの特徴を他のレギュレータに組み入れてもよく、一方、他の特徴を省いてもよい。さらに、本発明の趣旨を逸脱することなく、付加的あるいは代替的な素子や他の回路を追加することもできる。従って、添付の特許請求の範囲は本発明の趣旨と整合する仕方で広く解釈するのは適切である。
【００５２】
以上の説明では主として本発明者によってなされた発明をその利用分野である半導体回路に適用した場合について説明したが、これに限定されるものではない。
【００５３】
【発明の効果】
本願において開示される発明のうち、代表的なものによって得られる効果を簡単に説明すれば、以下のとおりである。
【００５４】
（１）マスタスライス技術を用いることにより、電圧レギュレータは２つの異なる範囲の外部電圧に適応することができる。
【００５５】
（２）電圧レギュレータの電流供給能力を非常に低い外部電圧の状態においてかなり増大することができる。
【００５６】
（３）チャージポンプ電圧レギュレータは、その任意のノードにおける電圧レベルが予め定められた高電圧レベルを超えないようにし、しかも、ほとんど外部電源からの電流を消費するようにすることができる。
【００５７】
（４）電圧レギュレータの出力電圧を充放電して、出力電圧を一定のレベルに維持することができる。
【００５８】
（５）電圧レギュレータを、誘電漏れを減少させるように最適化されたものとすることができる。
【図面の簡単な説明】
【図１ａ】従来の１６ＭビットＤＲＡＭの５Ｖバージョンのブロック図である。
【図１ｂ】従来の１６ＭビットＤＲＡＭの3.３Ｖバージョンのブロック図である。
【図２ａ】本発明の一実施形態である２５６ＭビットＤＲＡＭの3.３Ｖバージョンのブロック図である。
【図２ｂ】本発明の一実施形態である２５６ＭビットＤＲＡＭの2.５Ｖバージョンのブロック図である。
【図３ａ】図２ａのＤＲＡＭで用いられる電圧レギュレータのブロック図である。
【図３ｂ】図２ｂのＤＲＡＭで用いられる電圧レギュレータのブロック図である。
【図４ａ】図２ａのＤＲＡＭに対応する動作電圧－内部電圧のグラフである。
【図４ｂ】図２ｂのＤＲＡＭに対応する動作電圧－内部電圧のグラフである。
【図５】本発明の一実施形態である単純化されたＤＲＡＭの回路図である。
【図６】本発明の一実施形態である第１の電圧レギュレータの回路図である。
【図７】本発明の一実施形態であるインバータ回路の回路図である。
【図８】レベル変換機能付きインバータの入力信号および出力信号の電源電圧の依存性を示す曲線である。
【図９】従来の第２の電圧レギュレータのブロック図である。
【図１０】本発明の第２の電圧レギュレータのブロック図である。
【図１１】本発明の一実施形態である第２の電圧レギュレータの回路図である。
【図１２】図１１に示された信号のタイミング図である。
【図１３】本発明の一実施形態としての第３の電圧レギュレータを、図５の単純化されたＤＲＡＭの幾つかの回路と共に示した回路図である。

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【図１４】図１３に示された信号のタイミング図である。
【図１５】従来の第４の電圧レギュレータの電圧－電流グラフであり、そのリーク電流を示すものである。
【図１６】本発明の第４の電圧レギュレータの電圧－電流グラフであり、そのリーク電流を示すものである。
【図１７】本発明の一実施形態の第４の電圧レギュレータの回路図である。
【図１８】図１７に示された信号のタイミング図である。
【図１９】本発明の一実施形態であるチップ全体を示す図である。
【符号の説明】

１０ａ	５Ｖバージョンデバイス
１０ｂ	3.３Ｖバージョンデバイス
１２	電圧レギュレータ
１２ａ	配線
１２ｂ	配線
１３ａ	メモリセルおよび周辺回路
１３ｂ	出力回路
２０ａ	3.３Ｖバージョンデバイス
２０ｂ	2.５Ｖバージョンデバイス
２１ａ	周辺回路
２１ｂ	出力回路
２１ｃ	メモリセルアレイ
２２	電圧レギュレータ
２４	電圧レギュレータ
２４ａ	配線
２４ｂ	配線
２６	電圧レギュレータ（中間電圧レギュレータ）
２８	電圧レギュレータ（ＶＰＥＲＩレギュレータ）
２８ａ	配線
２８ｂ	配線
３０	電圧レギュレータ（ＶＡＲＹレギュレータ）
３２	電圧レギュレータ（ＶＰＰレギュレータ）
３４	電圧レギュレータ（ＶＢＢレギュレータ）
３６	電圧レギュレータ（ＶＢＬＲおよびＶＰＬＴレギュレータ）
４０	配線
４２	配線
４４	配線
５０	第１の通常動作範囲
５２	第１のストレス範囲
５３	第１の低電圧範囲
５４	第２の低電圧範囲
５６	第２の通常動作範囲
５８	第２のストレス範囲
６０	第３の低電圧範囲
６２	アドレスバッファ
６４	アドレスデコーダ
６６	ワード線ドライバ
６８	ＭＯＳトランジスタ
６８Ｗ	ウエル
６９	センスアンプ回路
７０	アンプアクション

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７１　センスアンプオーバードライブ回路
７２　イコライザ
７４　メインアンプ
７６　出力バッファ
８２　レベル変換機能付きインバータ回路
８２ａ　配線
８４　差動回路
８６　電圧ドライバ
８８　第１のプルアップＰＭＯＳトランジスタ
９０　第２のプルアップＰＭＯＳトランジスタ
９２　出力電圧
９４　ＶＰＰレギュレータ
９６　電源電圧
９８　ＶＰＰレベルセンサ
９９ａ　ＮＭＯＳトランジスタ
９９ｂ　ＮＭＯＳトランジスタ
９９ｃ　ＮＭＯＳトランジスタ
９９ｄ　ＮＭＯＳトランジスタ
９９ｅ　ＮＭＯＳトランジスタ
９９ｆ　ＮＭＯＳトランジスタ
９９ｇ　ＮＭＯＳトランジスタ
９９ｈ　ＮＭＯＳトランジスタ
９９ｉ　ＮＭＯＳトランジスタ
１００　ＰＭＯＳトランジスタ
１０１ａ　インバータ
１０１ｂ　インバータ
１０１ｃ　インバータ
１０１ｄ　インバータ
１０１ｅ　インバータ
１０２　第１の差動回路
１０４　分圧器
１０６　第１のプルアップＰＭＯＳトランジスタ
１０８　第２のプルアップＰＭＯＳトランジスタ
１１０　第２の差動回路
１１２　ＰＭＯＳトランジスタ
１１４　プルダウンＭＯＳトランジスタ
１１６　アクティブ期間
１１８ａ　第１の副回路
１１８ｂ　第２の副回路
１２０　プルアップ回路
１２２　トランジスタ
１２３　メモリチップ
１２４　メインローデコーダ領域
１２５　メインワードドライバ領域
１２６　カラムデコーダ領域
１２７　周辺回路およびボンディングパッド領域
１２８　メモリセルアレイ
１２９　センスアンプ領域
１３０　サブワードドライバ領域
１３１　交差領域

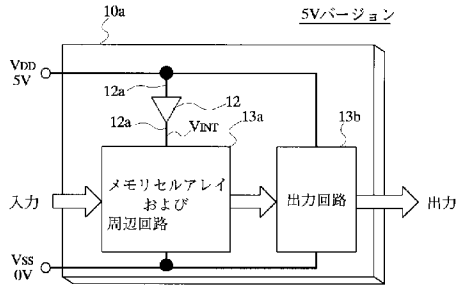
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１３２　メモリセルアレイ領域
Ｂ１　ビット
ＶＳＮ　ビット電圧
ＢＬ　ビット線
バー／ＢＬ　ビット線
ＳＤＮ　信号線
ＳＤＰ　信号線
ＳＡＰ１　ドライブ信号
ＳＡＰ２　ドライブ信号
ＳＡＮ　ドライブ信号
ＷＬ　ワード線
ＢＬＥＱ　信号
ＹＳ　列選択信号
Ｉ／Ｏ　入出力線
ＡＣＴＶ　信号
ＤＥＴＥＣＴ１Ｂ　レベル変換機能付きインバータの出力信号
ＤＥＴＥＣＴ２Ｂ　レベル変換機能付きインバータの出力信号
ＤＥＴＥＣＴ１　電源電圧レベルセンサ回路の出力信号
ＩＤ　電流
ＶＯＳＣ　発振器からの出力電圧
Ｃ１　キャパシタ
Ｃ２　コンデンサ
Ｃ３　コンデンサ
Ｃ４　コンデンサ
Ｃ５　コンデンサ
Ｃ６　コンデンサ
Ｎ１　ノード
Ｎ２　ノード
Ｎ３　ノード
Ｎ４　ノード
Ｎ５　ノード
Ｎ６　ノード
Ｎ７　ノード
Ｎ８　ノード
Ｎ９　ノード
ＳＤＰ１　信号線
ＳＤＰ２　信号線
ＳＤＰ３　信号線
ＳＡＥ　センスイネーブル信号
ＶＳＮ　ビット電圧
Ｉ１　プラスのリーク電流
Ｉ２　マイナスのリーク電流
Ｉ３　プラスのリーク電流
Ｉ４　マイナスのリーク電流
ＶＤＤ　外部プラス電源
ＶＳＳ　外部接地電源
ＶＡＲＹ　アレイ電圧
ＶＰＥＲＩ　内部電圧
ＶＰＰ　内部電圧
ＶＢＢ　内部電圧

ＶＢＬＲ　内部電圧
ＶＰＬＴ　内部電圧
Ｖ１　第１の中間電圧
Ｖ２　第２の中間電圧
ＩＮＰＵＴ　アドレスの入力ポート

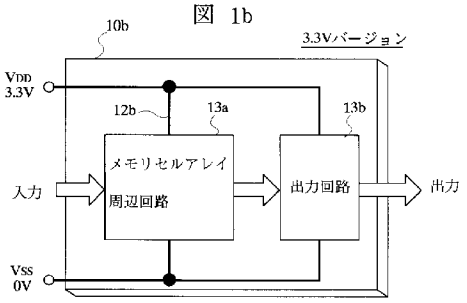
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図 1a



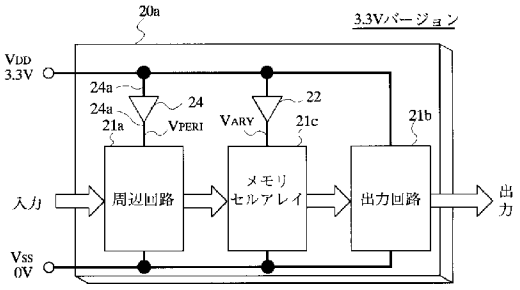
【図１ｂ】

図 1b



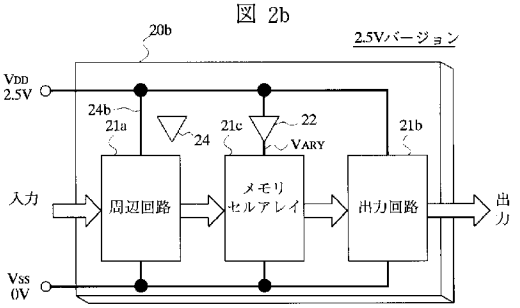
【図２ａ】

図 2a



【図２ｂ】

図 2b



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【図３ａ】

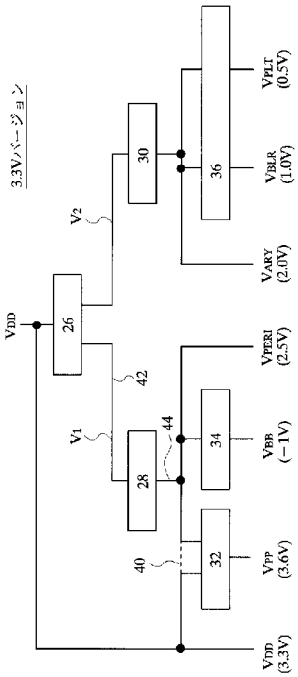


図 3a

【図３ｂ】

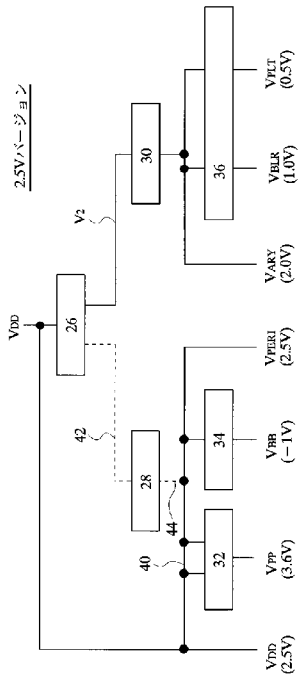
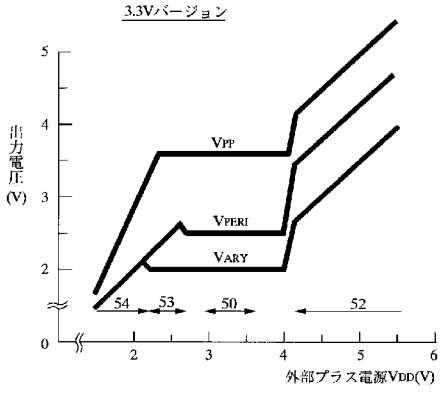


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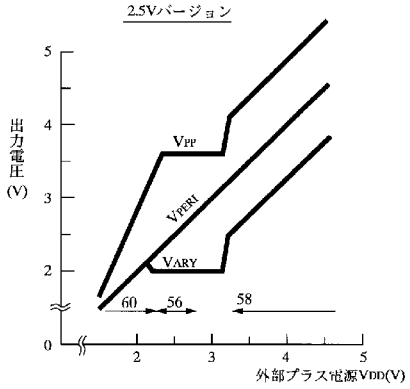
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図 4a



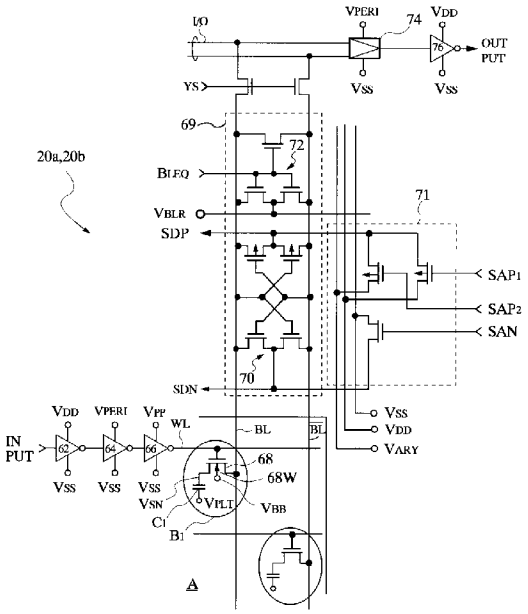
【図４ｂ】

図 4b



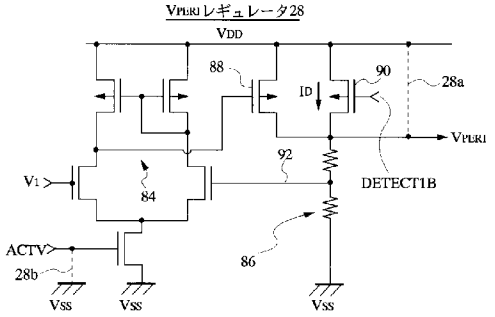
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図 5



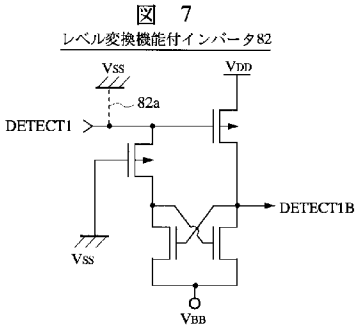
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図 6



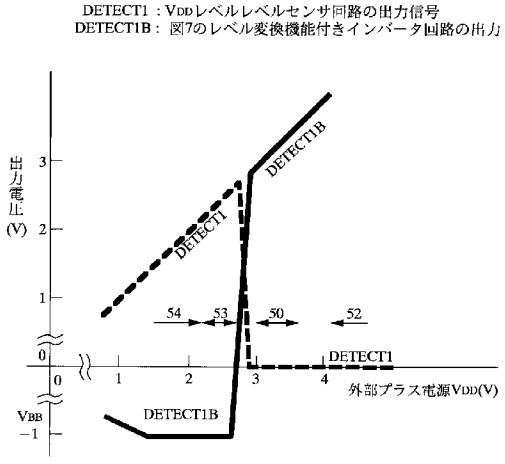
【図７】

図 7



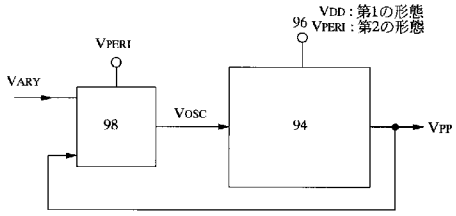
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図 8



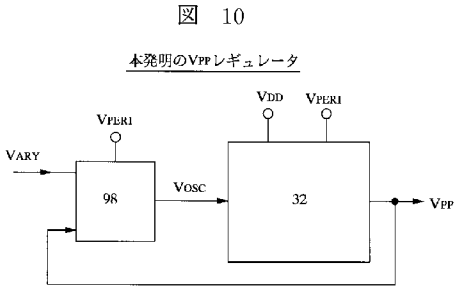
【図９】

図 9



【図１０】

図 10



【図１１】

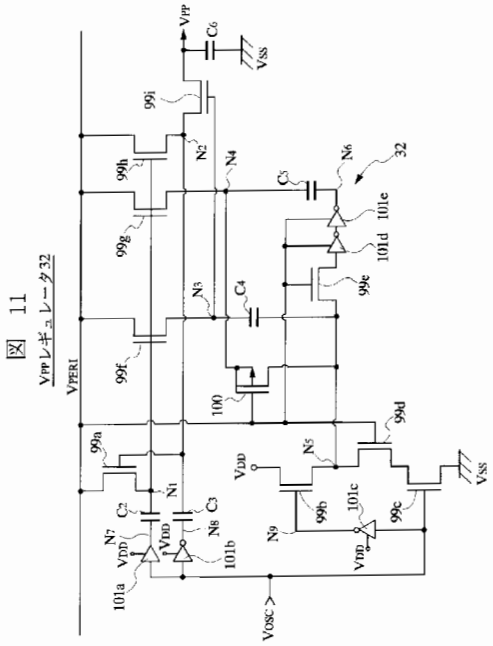
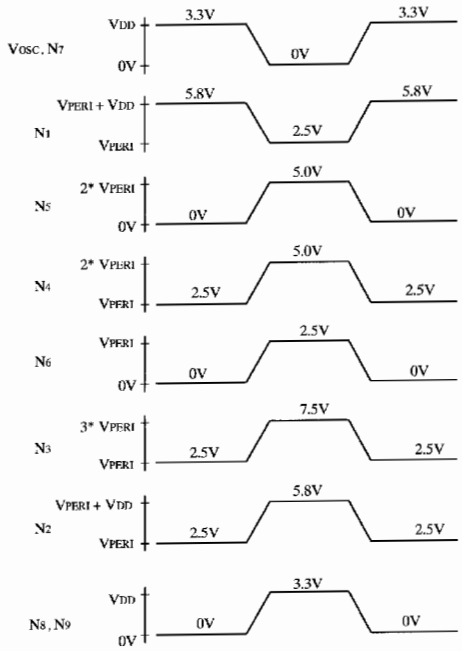


図 11
VPPレギュレータ32

【図１２】

図 12



【図１３】

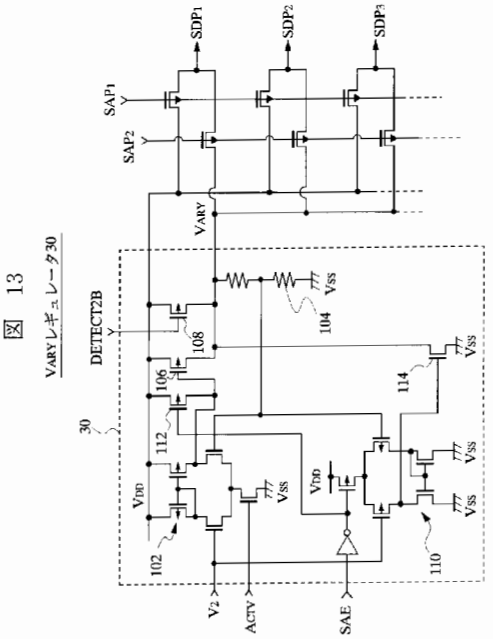
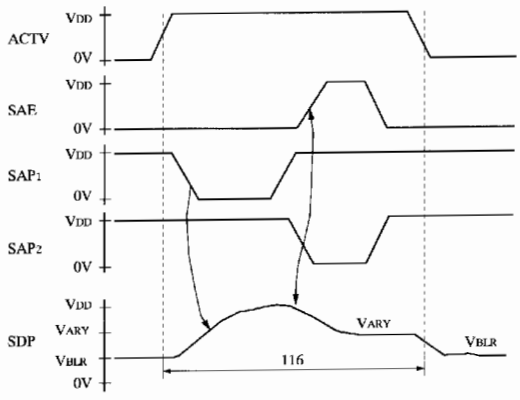


図 13
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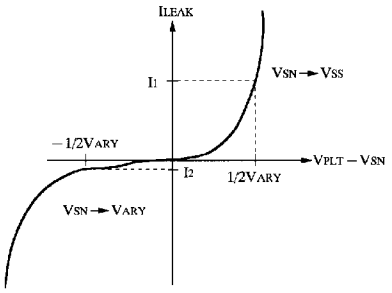
【図１４】

図 14



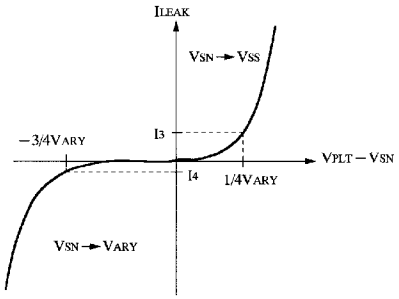
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図 15



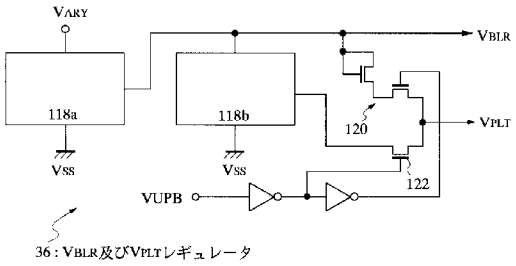
【図１６】

図 16



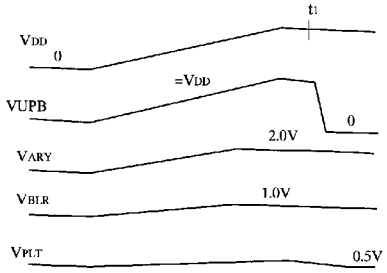
【図１７】

図 17



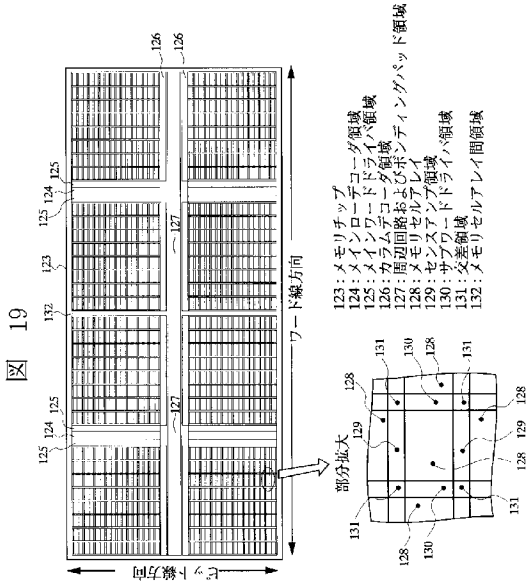
【図１８】

図 18



【図１９】

図 19



フロントページの続き

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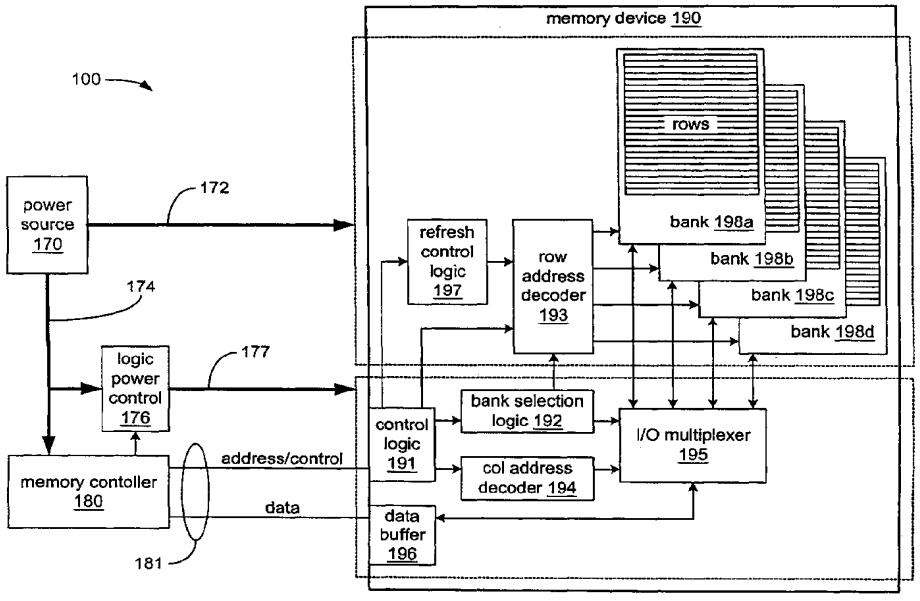
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[Continued on next page]

(54) Title: MEMORY SYSTEM SEGEMENTED POWER SUPPLY AND CONTROL



(57) Abstract: A memory device having memory cells supplied with a separate higher voltage power than the separate power supplied to memory logic, and a lower power state that entails removing power from at least some of the logic such that refresh operations to preserve the contents of the memory cells continue to take place, but at least some of the interface to the memory device is powered down to reduce power consumption.

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MEMORY SYSTEM SEGMENTED POWER SUPPLY AND CONTROL

BACKGROUND

[0001] Computer systems continue to be designed to meet the two often opposing goals of increased performance and decreased power consumption (sometimes manifesting in trying to maintain a level of power consumption while increasing performance). The struggle to meet both goals becomes quite evident in the case of electronic devices such as portable computer systems (including notebook and handheld computers), networking appliances (including firewall appliances and intelligent routers), and banks of servers (including blade and telco servers), all of which employ memory systems having considerable quantities of DRAM (dynamic random access memory). As ever more uses for such electronic devices are found, there is a need for faster processors, greater quantities of memory, etc. However, as ever more uses for such devices are found, there is a need to consume lesser amounts of power to increase battery life in portable application and to allow for greater densities of electronic devices to be assembled together in centralized facilities.

[0002] This struggle has resulted in efforts to find ways to decrease the amount of power required by each of the components of such electronic devices, including memory devices. Known approaches include creating reduced power modes (commonly referred to as "sleep modes" or "hibernation modes") for such electronic devices to enter into when not actively being used. Specifically, DRAM devices have been created with lower power modes, including what is

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commonly referred to in the DRAM device industry as "self refresh" mode where interactions between DRAM devices and other components are minimized. Self refresh modes entail using a minimal amount of logic built into a DRAM device to allow the DRAM device to autonomously carry out maintenance functions such as refreshing the DRAM device's memory cells.

[0003] However, such approaches to reducing DRAM device power consumption have not addressed the problem of power wasted as a result of the growing disparity in the voltage level at which the memory cells within DRAM devices must operate to acquire and preserve a charge indicating bit values within memory cells, and the ever lower voltage levels required by processors and other logic that are often coupled to DRAM devices. As a result of this disparity, inefficient I/O interface and memory controller logic designs must be employed, and opportunities to decrease power consumption and/or to increase the speeds at which memory is accessed by making use of lower voltage interfaces are lost.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The objects, features, and advantages of the present invention will be apparent to one skilled in the art in view of the following detailed description in which:

[0005] **Figure 1** is a block diagram of an embodiment employing a memory system.

[0006] **Figure 2** is a block diagram of another embodiment employing a memory system.

[0007] **Figure 3** is a block diagram of an embodiment employing a memory device.

[0008] **Figure 4** is a block diagram of another embodiment employing a memory device.

[0009] **Figure 5** is a block diagram of still another embodiment employing a memory device.

[0010] **Figure 6** is a block diagram of yet another embodiment employing a memory device.

[0011] **Figure 7** is a block diagram of an embodiment employing a memory device having a point-to-point interface.

[0012] **Figure 8** is a block diagram of another embodiment employing a memory device having a point-to-point interface.

[0013] **Figure 9** is a block diagram of another embodiment employing a computer system.

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DETAILED DESCRIPTION

[0014] In the following description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of embodiments of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention as hereinafter claimed.

[0015] Embodiments of the present invention concern segmenting the power supply used for memory devices such that different power supplies are used to supply power at differing voltage levels for DRAM memory cells and at least a portion of DRAM interface logic, thereby reducing the overall amount of power required by DRAM devices. Although the following discussion centers on DRAM devices, it will be understood by those skilled in the art that the present invention as hereinafter claimed may be practiced in support of other memory devices. Also, although at least part of the following discussion centers on memory within computer systems, it will be understood by those skilled in the art that the present invention as hereinafter claimed may be practiced in connection with other electronic devices or systems having memory devices. It will also be understood by those skilled in the art that although the following discussion centers on memory devices in which memory cells are organized in two dimensional arrays of rows and columns, the memory cells may be organized in any of a number of ways, including into banks and with or without interleaving, arrays of more than two dimensions, content-addressable, etc.

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[0016] **Figure 1** is a block diagram of one embodiment employing a memory system. Memory system 100 is made up, at least in part, of memory controller 180 and memory device 190 coupled together via memory bus 181. Those skilled in the art of the design of memory systems will readily recognize that **Figure 1** depicts one form of a relatively simple memory system, and that alternate embodiments are possible in which the exact arrangement and configuration of components may be reduced, augmented or otherwise altered without departing from the spirit and scope of the present invention as hereinafter claimed. For example, although memory system 100 is depicted as having only one memory bus 181 and only one memory device 190 for the sake of simplicity in the discussion that follows, it will be readily understood by those skilled in the art that other possible embodiments of memory system 100 may be made up of multiple memory buses and/or devices without departing from the spirit and scope of the claimed invention.

[0017] Memory controller 180 controls the functions carried out by memory device 190 as part of providing access to memory device 190 to external devices (not shown) coupled to memory controller 180, such as a processor, bus mastering I/O controller, etc. Specifically, an external device coupled to memory controller 180 issues commands to memory controller 180 either to store data within memory device 190, or to retrieve stored data from memory device 190. Memory controller 180 receives these commands and relays them to memory device 190 in a format having timing and protocols compatible with memory bus 181 and/or the combination of control logic 191 and data buffer 196 that make up

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the interface between memory device 190 and memory bus 181. In effect, memory controller 180 coordinates accesses made to memory cells within memory device 190 in answer to read and write commands from external devices. In support of these functions in various embodiments, memory controller 180 also coordinates various maintenance operations that must be performed to ensure that data stored within memory device 190 is preserved, including the initiation of regular refresh operations and the occurrence of precharge operations as needed between accesses.

[0018] Memory bus 181 is made up of various control, address and data signal lines coupling together memory controller 180 and memory device 190. The exact quantity and characteristics of the various signal lines making up various possible embodiments of memory bus 181 may be configured to be interoperable with any of a number of possible memory interfaces, including those meant to be compatible with known types of memory devices, among them being DRAM (dynamic random access memory) devices such as FPM (fast page mode) memory devices, EDO (extended data out), dual-port VRAM (video random access memory), window RAM, SDR (single data rate), DDR (double data rate), RAMBUS™ DRAM, etc. In some embodiments, where activity on various signal lines is meant to be coordinated with a clock signal, one or more of the signal lines, perhaps the control signal lines, serves to transmit a clock signal between memory controller 180 and memory device 190. In some embodiments, one or more control signals and address signals may be multiplexed onto common signal lines such that control signals and address signals are transmitted

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at different times on common conductors for carrying signals between memory controller 180 and memory device 190. Also, in some embodiments, one or more address signals and data signals may be multiplexed onto common signal lines.

[0019] Memory device 190 is a DRAM memory device with an interface made up of control logic 191 and data buffer 196 configured to be interoperable with memory bus 181. In some embodiments, memory device 190 is a single integrated circuit. In other embodiments, memory device 190 is made up of multiple integrated circuits of a removable memory module, such as a SIMM (single inline memory module), SIPP (single inline pin package), DIMM (dual inline memory module), etc.

[0020] The memory cells of memory device 190 are grouped into multiple banks, such as banks 198a-d, with each bank being organized into a two dimensional array of memory cells having rows and columns. However, those skilled in the art will readily recognize that the memory cells within memory device may be organized in any of a number of possible ways. In some embodiments, control logic 191 receives at least some commands and addresses from memory controller 180 through memory bus 181, and uses bank selection logic 192 and row address decoder 193 to gain access to the appropriate rows, while using column address decoder 194, I/O multiplexer 195 and/or data buffer 196 to carry out the appropriate actions, at least for read and write commands. Control logic 191 further coordinates the carrying out of commands received from memory controller 180 with the refreshing of memory cells within banks 198a-d by refresh control logic 197.

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[0021] In various embodiments as depicted in **Figure 1**, memory controller 180 and memory device 190 receive power from power source 170. Memory controller 180 is supplied with logic level power through logic level power line 174. In some embodiments, this same logic level power received by memory controller 180 is selectively supplied to a portion of memory device 190 through logic power control 176 under the control of memory controller 180. In alternate embodiments, this same logic level power received by memory controller 180 is supplied to a portion of memory device 190 directly from logic level power line 174 without intervening logic power control 176. This portion of memory device 190 supplied with logic level power (outlined with a dotted rectangle) is made up, at least in part, of control logic 191, bank selection logic 192, column address decoder 194, I/O multiplexer 195 and data buffer 196. However, another portion of memory device 190 receives storage level power through storage level power line 172 (also outlined with a dotted rectangle). This portion of memory device 190 supplied with storage level power is made up, at least in part, of refresh control logic 197, row address decoder 193 and banks 198a-d.

[0022] As those skilled in the art will recognize, the exact choice of which of control logic 191, bank selection logic 192, row address decoder 193, column address decoder 194, I/O multiplexer 195, data buffer 196 and refresh control logic 197 are supplied with one or the other of logic level power via logic level power line 177 or storage level power via storage level power line 172 may depart in various embodiments from what is depicted in **Figure 1** without departing from the spirit and scope of the claimed invention. Like memory

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controller 180, control logic 191, bank selection logic 192, row address decoder 193, column address decoder 194, I/O multiplexer 195, data buffer 196, and refresh control logic 197 are logic circuit devices, and as logic circuit devices, are able to be designed to make use of recent improvements in transistors and other technologies that have become available for logic circuit design, including the use of ever smaller transistors. Such smaller transistors in logic circuits do not require as high a voltage level to distinguish between 0 and 1 bit values as do larger transistors, and so such smaller transistors can be operated more efficiently at lower voltage levels. This makes the use of higher voltage levels as would be required by larger transistors with smaller transistors unnecessary, and in many logic circuits employing such smaller transistors, the use of such a higher voltage provides excess electrical energy that cannot be used by such smaller transistors and which, therefore, much be wastefully converted to and dissipated as heat. However, in contrast to such logic circuits, the memory cells of a DRAM device still require a higher voltage level to reliably distinguish between 0 and 1 bit values as a result of the use of charges that are dynamically stored and maintained in the capacitor-like design of those memory cells where a stored charge always decays over time and has to be repeatedly refreshed (recharged) to be maintained. The fact of this decay over time requires a higher voltage level to be used in storing the charge to provide some "extra" separation in voltage levels signifying 0 and 1 bit values so that voltage levels between partly decayed 0 and 1 bit values are still distinguishable after that partial decay has occurred. For these and related reasons, DRAM memory cells require a somewhat higher voltage level

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from a power source despite the fact that the size of the transistors used in the memory cells has been decreasing just as the transistors of logic circuits have.

[0023] The provision of two different portions of memory device 190 with two different power sources affords an opportunity to save power in situations when the electronic system of which memory system 100 is placed in a lower power state such that accesses to store data within memory device 190 or retrieve data from memory device 190 are suspended. In such a lower power state, it may be desirable to provide memory device 190 with power only to the degree necessary to preserve data stored within banks 198a-d, and this may be accomplished in some embodiments by allowing the logic level power provided via logic level power line 177 to be selectively turned off via logic power control 176. In such embodiments, row address decoder 193 and refresh control logic 197 may use the storage level power supplied via storage level power line 172 such that refresh control logic 197 is able to continue to initiate refresh cycles on rows within banks 198a-d possibly selected at intervals via a counter within refresh control logic 197, and row address decoder 193 is able to continue selecting the rows specified by refresh control logic 197 to be put through a refresh operation.

[0024] Depending on specific details of implementation of banks 198a-d, the provision of storage level power to at least row address decoder 193 may be necessary for row address decoder 193 to properly drive word lines within banks 198a-d with sufficient voltage levels. Likewise, the provision of other components within memory device 190 that are directly coupled to banks 198a-d,

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such as I/O multiplexer 195, with storage level power may also be necessary, again to support signaling with sufficient voltage levels.

[0025] Supplying the same logic level power to control logic 191 and data buffer 196 as is supplied to memory controller 180 permits control logic 191 and data buffer 196 to operate at a more efficient voltage level that does not waste electrical energy. Sharing this same lower voltage also provides the opportunity to use a lower voltage level in signaling across memory bus 181 between memory controller 180 and memory device 190, and the resulting opportunity to make use of lower voltage swings to convey control, address, data and/or other signals affords the further opportunity to increase the rate at which such signals are transmitted across memory bus 181, which in turn, provides the further opportunity to increase the performance of memory bus 181. Furthermore, sharing this same lower voltage level may also alleviate the need to design the interface within memory controller 180 to couple memory controller 180 to memory bus 181 to accommodate higher voltage levels, thereby potentially simplifying the design of that interface within memory controller 180 and/or potentially allowing a faster interface to be more easily provided. Furthermore, the reduction in power consumed by having memory bus 181 and the interfaces to memory bus 181 within both memory controller 180 and memory device 190 (such as control logic 191 and/or data buffer 196) can become significant, especially where multiple ones of memory device 190 make up memory system 100.

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[0026] **Figure 2** is a block diagram of another embodiment employing a memory system. Not unlike memory system 100 of **Figure 1**, memory system 200 is made up, at least in part, of memory controller 280 and memory device 290 coupled together via memory bus 281. Those skilled in the art of the design of memory systems will readily recognize that **Figure 2** depicts one form of a relatively simple memory system, and that alternate embodiments are possible in which the exact arrangement and configuration of components may be reduced, augmented or otherwise altered without departing from the spirit and scope of the present invention as hereinafter claimed.

[0027] Memory controller 280 controls the functions carried out by memory device 290 as part of providing access to memory device 290 to external devices (not shown) coupled to memory controller 280, such as a processor, bus mastering I/O controller, etc. Memory controller 280 coordinates accesses made to memory cells within memory device 290 in answer to read and write commands from external devices. Memory controller 280 also coordinates various maintenance operations that must be performed to ensure that data stored within memory device 290 is preserved, including the initiation of regular refresh operations and the occurrence of precharge operations as needed between accesses. Memory bus 281 is made up of various control, address and data signal lines coupling together memory controller 280 and memory device 290. The exact quantity and characteristics of the various signal lines making up various possible embodiments of memory bus 281 may be configured to be interoperable with any of a number of possible memory interfaces. In some embodiments,

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activity on various signal lines of memory bus 281 may be meant to be coordinated with a clock signal. Memory device 290 is a DRAM memory device with an interface made up of control logic 291 and data buffer 296 configured to be interoperable with memory bus 281. In some embodiments, memory device 290 is a single integrated circuit, and in other embodiments, memory device 290 is made up of multiple integrated circuits of a removable memory module. The memory cells of memory device 290 are grouped into multiple banks, such as banks 298a-d, with each bank being organized into a two dimensional array of memory cells having rows and columns.

[0028] In various embodiments, memory controller 280 is supplied with logic level power through logic level power line 274. This same logic level power is selectively supplied to a portion of memory device 290 through logic power control 276 under the control of memory controller 280, namely a portion encompassing control logic 291, banks selection logic 292, column address decoder 294, I/O multiplexer 295 and data buffer 296. This same logic level power is also supplied to another portion of memory device 290 directly from logic level power line 274 without intervening logic power control 276, namely a portion encompassing row address decoder 293 and refresh control logic 297. Another portion of memory device 290 receives storage level power through storage level power line 272, namely a portion encompassing banks 298a-d. As those skilled in the art will recognize, the exact choice of which of control logic 291, bank selection logic 292, row address decoder 293, column address decoder 294, I/O multiplexer 295, data buffer 296 and refresh control logic 297 are

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supplied with one or the other of logic level power or storage level power, as well as the choice as to whether logic level power is selectively supplied through logic power control 276, or not, may depart in various embodiments from what is depicted in **Figure 2** without departing from the spirit and scope of the claimed invention.

[0029] The provision of three different portions of memory device 290 with two different power sources, with one of the three portions being supplied one of the two power sources in a selective manner, affords an opportunity to save power in situations when the electronic system of which memory system 200 is placed in a lower power state where, as was the case with memory system 200 of **Figure 1**, it may be desirable to provide memory device 290 with power only to the degree necessary to preserve data stored within banks 298a-d. This may be accomplished in some embodiments by allowing the logic level power provided via logic level power line 277 to be selectively turned off to a portion of memory device 290 via logic power control 276, while the same logic level power continues to be provided to another portion of memory device 290 via logic power line 274. In such embodiments, banks 298a-d continue to be supplied with storage level power to preserve the contents of the memory cells within banks 298a-d. Furthermore, row address decoder 293 and refresh control logic 297 may use logic level power supplied via logic level power line 274 such that refresh control logic 297 is able to continue to initiate refresh cycles on rows within banks 298a-d possibly selected at intervals via a counter within refresh control

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logic 297, and row address decoder 293 is able to continue selecting the rows specified by refresh control logic 297 to be put through a refresh operation.

[0030] Depending on specific details of implementation of banks 298a-d, the provision of storage level power to at least row address decoder 293 may be necessary for row address decoder 293 to properly drive word lines within banks 298a-d with sufficient voltage levels. Likewise, the provision of other components within memory device 290 that are directly coupled to banks 298a-d, such as I/O multiplexer 295, with storage level power may also be necessary, again to support signaling with sufficient voltage levels.

[0031] In a manner not unlike memory system 100 of **Figure 1**, supplying the same logic level power to control logic 291 and data buffer 296 as is supplied to memory controller 280 permits control logic 291 and data buffer 296 to operate at a more efficient voltage level that does not waste electrical energy. Sharing this same lower voltage also provides the opportunity to use a lower voltage level in signaling across memory bus 281 between memory controller 280 and memory device 290, and the resulting opportunity to make use of lower voltage swings to convey control, address, data and/or other signals affords the further opportunity to increase the rate at which such signals are transmitted across memory bus 281, which in turn, provides the further opportunity to increase the performance of memory bus 281.

[0032] **Figure 3** is a block diagram of one embodiment employing a memory device. In various possible embodiments, memory device 390 is made up, at least in part, of memory circuits 398a-i assembled together as ICs on a substrate

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(such as a circuitboard) or as dies within a multiple die package. More specifically, in some embodiments, memory device 390 is an unbuffered DIMM (dual inline memory module). Each of memory circuits 398a-i is made up, at least in part, of memory cell arrays 399a-i, higher power logic 397a-i and lower power logic 396a-i, respectively. Each of lower power logic 396a-i is coupled to memory bus 381, and together with corresponding ones of higher power logic 397a-i, couples corresponding ones of memory arrays 399a-i within memory device 390 to a memory controller and/or other devices (not shown) also coupled to memory bus 381 outside of memory device 390. Lower power logic 396a-i are all supplied with logic level power from logic level power line 377, and both higher power logic 397a-i and memory cells 399a-i are all supplied with storage level power from storage level power line 372.

[0033] Each of memory cell arrays 399a-i is made up of numerous memory cells organized into at least a single two-dimensional array. To ensure the reliable retention of the data stored in these memory cells, the storage level power supplied to each of memory cell arrays 399a-i is of sufficient voltage to allow reliable distinguishing between 0 and 1 bit values of charges stored in memory cells of a capacitor-like configuration, as discussed at length, earlier. Each one of lower power logic 396a-i, together with corresponding ones of higher power logic 397a-i, provides the interface logic that carries out commands received from memory bus 381 to either store data within or retrieve data from corresponding ones of memory cell arrays 399a-i, as well as carrying out other various functions. The splitting of this interface logic between lower power and higher

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power logic may, in some embodiments, allow the portions of this interface logic within each of higher power logic 397a-i that are more closely coupled to memory cell arrays 399a-i to use the storage level power supplied via storage level power line 372 to interact with corresponding ones of memory cell arrays 399a-i with signaling voltage levels that may be more easily compatible with memory cell arrays 399a-i. At the same time, this same splitting of interface logic may, in some embodiments, allow the portions of this interface logic within each of lower power logic 396a-i that are more closely coupled to memory bus 381 to use the logic level power supplied via logic level power line 377 to interact with memory bus 381 with signaling voltage levels that may be more easily compatible with other devices coupled to memory bus 381. In various implementations, the voltage level of the logic level power supplied via logic level power line 377 is lower than the voltage level of the storage level power supplied via storage level power line 372 in recognition of the possible advantages of using lower voltage signaling across memory bus 381, including lower overall power consumption and shorter signal rise and fall times leading to opportunities to increase the transfer rate of addresses, commands and/or data across memory bus 381.

[0034] Also, in some embodiments, the separation of this interface logic between lower power logic 396a-i and higher power logic 397a-i may allow power supplied to at least those portions of the interface logic that are more closely coupled to memory bus 381 (i.e., portions within lower power logic 396a-i) to be powered down by turning off the logic level power supplied via logic

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level power line 377 at times when some or all of the signal lines making up memory bus 381 are powered down. At such times when logic level power line 377 is powered down, storage level power line 372 remains turned on to continue supplying storage level power to both higher power logic 397a-i and memory cell arrays 399a-i. Also, in some embodiments, the turning off of logic level power supplied via logic level power line 377 coincides with memory device 390 being placed in a lower power state such as self-refresh mode where at least a portion of higher power logic 397a-i uses the storage level power that continues to be supplied via storage level power line 372 to initiate and/or carry out refresh operations on portions (e.g., pages or rows of memory cells) of corresponding ones of memory cell arrays 399a-i.

[0035] As those skilled in the art will recognize, the exact decision of which portions of interface logic are to make up each of lower power logic 396a-i and which portions are to make up each of higher power logic 397a-i may be varied between specific embodiments without departing from the spirit and scope of the claimed invention. In some embodiments, the portions of interface logic making up each of higher power logic 397a-i may be limited to logic needed to carry out refresh operations, possibly including a row address decoder, so that these limited portions of interface logic continue to be supplied with power from storage level power line 372 at times when logic level power line 377 is turned off as part of memory device 390 entering a lower power state. In other embodiments, the design of each of memory cell arrays 399a-i may be such that any portions of

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interface logic directly coupled to the memory cells must be among those portions making up each of higher power logic 397a-i.

[0036] **Figure 4** is a block diagram of another embodiment employing a memory device, with memory device 490 being somewhat similar to memory device 390 of **Figure 3**. In various possible embodiments, memory device 490 is made up, at least in part, of memory circuits 498a-i assembled together as ICs on a substrate or as dies within a multiple die package. Also, in some embodiments, memory device 490 is an unbuffered DIMM. Each of memory circuits 498a-i is made up, at least in part, of memory cell arrays 499a-i, unswitched power logic 497a-i and lower power logic 496a-i, respectively. Each of lower power logic 496a-i is coupled to memory bus 481, and together with corresponding ones of unswitched power logic 497a-i, couples corresponding ones of memory arrays 499a-i within memory device 490 to a memory controller and/or other devices (not shown) also coupled to memory bus 481 outside of memory device 390. Lower power logic 496a-i are all supplied with logic level power from logic level power line 477, constant power logic 497a-i are all supplied with unswitched power from unswitched power line 474, and memory cells 499a-i are all supplied with storage level power from storage level power line 472.

[0037] Each of memory cell arrays 499a-i is made up of numerous memory cells organized into at least a single two-dimensional array. To ensure the reliable retention of the data stored in these memory cells, the storage level power supplied to each of memory cell arrays 499a-i is of sufficient voltage to allow reliable distinguishing between 0 and 1 bit values of charges stored in memory

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cells of a capacitor-like configuration, as discussed at length, earlier. Each one of lower power logic 496a-i, together with corresponding ones of unswitched power logic 497a-i, provides the interface logic that carries out commands received from memory bus 481 to either store data within or retrieve data from corresponding ones of memory cell arrays 499a-i, as well as carrying out other various functions. The splitting of this interface logic between lower power and unswitched power logic may, in some embodiments, allow the portions of this interface logic within each of unswitched power logic 497a-i that are more closely coupled to memory cell arrays 499a-i to use a form of unswitched power supplied via unswitched power line 474 having a voltage high enough to interact with corresponding ones of memory cell arrays 499a-i with signaling voltage levels that may be more easily compatible with memory cell arrays 499a-i. At the same time, this same splitting of interface logic may, in some embodiments, allow the portions of this interface logic within each of lower power logic 496a-i that are more closely coupled to memory bus 481 to use the logic level power supplied via logic level power line 477 to interact with memory bus 481 with signaling voltage levels that may be more easily compatible with other devices coupled to memory bus 481. In various implementations, the voltage level of the logic level power supplied via logic level power line 477 is lower than the voltage level of the storage level power supplied via storage level power line 472 in recognition of the possible advantages of using lower voltage signaling across memory bus 481, including lower overall power consumption and shorter signal

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rise and fall times leading to opportunities to increase the transfer rate of addresses, commands and/or data across memory bus 481.

[0038] Also, in some embodiments, the separation of this interface logic between lower power logic 496a-i and unswitched power logic 497a-i may allow power supplied to at least those portions of the interface logic that are more closely coupled to memory bus 481 (i.e., portions within lower power logic 496a-i) to be powered down by turning off the logic level power supplied via logic level power line 477 at times when some or all of the signal lines making up memory bus 481 are powered down. At such times when logic level power line 477 is powered down, both unswitched power line 474 and storage level power line 472 remain turned on to continue supplying unswitched power and storage level power to both unswitched power logic 497a-i and memory cell arrays 499a-i, respectively. Also, in some embodiments, the turning off of logic level power supplied via logic level power line 477 coincides with memory device 490 being placed in a lower power state such as self-refresh mode where at least a portion of unswitched power logic 497a-i uses the unswitched power that continues to be supplied via unswitched power line 474 to initiate and/or carry out refresh operations on portions (e.g., pages or rows of memory cells) of corresponding ones of memory cell arrays 499a-i.

[0039] In some embodiments, the voltage level of the unswitched power supplied via unswitched power line 474 is similar to the voltage level of the logic level power supplied via logic level power line 477. In such embodiments, although lower power logic 496a-i and unswitched power logic 497a-i are

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supplied with power at similar voltage levels such that efficiencies of lower voltage operation of logic circuits may be realized (as described at length, above) the supplying of separate unswitched power and logic level power may be done to allow for the switching off of the logic level power, as described above, while the unswitched power at a similar voltage level continues to be supplied. In other embodiments, the voltage level of the unswitched power supplied via unswitched power line 474 may be chosen to be somewhere between the voltage levels of the logic level power and storage level power so as to allow unswitched power logic 497a-i to operate with signaling levels chosen to be more easily compatible with both lower power logic 496a-i and memory cell arrays 499a-i, respectively.

[0040] As those skilled in the art will recognize, the exact decision of which portions of interface logic are to make up each of lower power logic 496a-i and which portions are to make up each of unswitched power logic 497a-i may be varied between specific embodiments without departing from the spirit and scope of the claimed invention. In some embodiments, the portions of interface logic making up each of unswitched power logic 497a-i may be limited to logic needed to carry out refresh operations, possibly including a row address decoder, so that these limited portions of interface logic continue to be supplied with power from unswitched power line 474 at times when logic level power line 477 is turned off as part of memory device 490 entering a lower power state.

[0041] **Figure 5** is a block diagram of still another embodiment employing a memory device, with memory device 590 being largely identical to memory device 390 of **Figure 3** except for the addition of buffer logic 592 separating

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some of the signals of memory bus 581 from other portions of memory device 590, effectively creating two memory buses 581 and 594 where some of the signals are buffered and/or latched between memory buses 581 and 594, while other signals are directly connected between memory buses 581 and 594. In some embodiments, memory device 590 is a registered DIMM where address and/or command signals are buffered and/or latched through buffer logic 592, while data signals are directly connected between memory buses 581 and 594. Like memory device 390 of **Figure 3**, in various embodiments, memory device 590 is made up, at least in part, of memory circuits 598a-i assembled together as ICs on a substrate or as dies within a multiple die package, and buffer logic 592. Each of memory circuits 598a-i is made up, at least in part, of memory cell arrays 599a-i, higher power logic 597a-i and lower power logic 596a-i, respectively. Both buffer logic 592 and lower power logic 596a-i are all supplied with logic level power from logic level power line 577, and both higher power logic 597a-i and memory cells 599a-i are all supplied with storage level power from storage level power line 572.

[0042] To ensure the reliable retention of the data stored in these memory cells, the storage level power supplied to each of memory cell arrays 599a-i is of sufficient voltage to allow reliable distinguishing between 0 and 1 bit values of charges stored in memory cells of a capacitor-like configuration, as discussed at length, earlier. Each one of lower power logic 596a-i, together with corresponding ones of higher power logic 597a-i, provides the interface logic that carries out commands received through memory buses 581 and 594 to either store

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data within or retrieve data from corresponding ones of memory cell arrays 599a-i, as well as carrying out other various functions. The splitting of this interface logic between lower power and higher power logic may, in some embodiments, allow the portions of this interface logic within each of higher power logic 597a-i that are more closely coupled to memory cell arrays 599a-i to use the storage level power supplied via storage level power line 572 to interact with corresponding ones of memory cell arrays 599a-i with signaling voltage levels that may be more easily compatible with memory cell arrays 599a-i. At the same time, this same splitting of interface logic may, in some embodiments, allow the portions of this interface logic within each of lower power logic 596a-i that are more closely coupled to buffer logic 592 and/or memory buses 581 and/or 594 to use the logic level power supplied via logic level power line 577 to interact with buffer logic 592 and/or memory buses 581 and/or 594 with signaling voltage levels that may be more easily compatible with buffer logic 592 and/or other devices coupled to memory bus 581 and/or 594. In various implementations, the voltage level of the logic level power supplied via logic level power line 577 is lower than the voltage level of the storage level power supplied via storage level power line 572 in recognition of the possible advantages of using lower voltage signaling with buffer logic 592 and/or across memory bus 581 and/or 594, including lower overall power consumption and shorter signal rise and fall times leading to opportunities to increase the transfer rate of addresses, commands and/or data across memory buses 581 and/or 594.

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[0043] Also, in some embodiments, the separation of this interface logic between lower power logic 596a-i and higher power logic 597a-i may allow power supplied to at least those portions of the interface logic that are more closely coupled to buffer logic 592 and/or memory buses 581 and/or 594 (i.e., portions within lower power logic 596a-i) to be powered down by turning off the logic level power supplied via logic level power line 577 at times when some or all of the signal lines making up memory bus 581 are powered down. At such times when logic level power line 577 is powered down, storage level power line 572 remains turned on to continue supplying storage level power to both higher power logic 597a-i and memory cell arrays 599a-i. Also, in some embodiments, the turning off of logic level power supplied via logic level power line 577 coincides with memory device 590 being placed in a lower power state such as self-refresh mode where at least a portion of higher power logic 597a-i uses the storage level power that continues to be supplied via storage level power line 572 to initiate and/or carry out refresh operations on portions (e.g., pages or rows of memory cells) of corresponding ones of memory cell arrays 599a-i.

[0044] As was the case with memory device 390 of **Figure 3**, those skilled in the art will recognize that the exact decision of which portions of interface logic are to make up each of lower power logic 596a-i and which portions are to make up each of higher power logic 597a-i may be varied between specific embodiments without departing from the spirit and scope of the claimed invention. In some embodiments, the portions of interface logic making up each of higher power logic 597a-i may be limited to logic needed to carry out refresh

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operations, possibly including a row address decoder, so that these limited portions of interface logic continue to be supplied with power from storage level power line 572 at times when logic level power line 577 is turned off as part of memory device 590 entering a lower power state. In other embodiments, the design of each of memory cell arrays 599a-i may be such that any portions of interface logic directly coupled to the memory cells must be among those portions making up each of higher power logic 597a-i.

[0045] **Figure 6** is a block diagram of yet another embodiment employing a memory device, with memory device 690 being largely identical to memory device 490 of **Figure 4** except for the addition of buffer logic 692 separating some of the signals of memory bus 681 from other portions of memory device 690, effectively creating two memory buses 681 and 694 where some of the signals are buffered and/or latched between memory buses 681 and 694, while other signals are directly connected between memory buses 681 and 694. In some embodiments, memory device 690 is a registered DIMM where address and/or command signals are buffered and/or latched through buffer logic 692, while data signals are directly connected between memory buses 681 and 694. Like memory device 490 of **Figure 4**, in various embodiments, memory device 690 is made up, at least in part, of memory circuits 698a-i assembled together as ICs on a substrate or as dies within a multiple die package, and buffer logic 692. Each of memory circuits 698a-i is made up, at least in part, of memory cell arrays 699a-i, unswitched power logic 697a-i and lower power logic 696a-i, respectively. Both buffer logic 692 and lower power logic 696a-i are all supplied

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with logic level power from logic level power line 677, constant power logic 697a-i are all supplied with unswitched power from unswitched power line 674, and memory cells 699a-i are all supplied with storage level power from storage level power line 672.

[0046] To ensure the reliable retention of the data stored in these memory cells, the storage level power supplied to each of memory cell arrays 699a-i is of sufficient voltage to allow reliable distinguishing between 0 and 1 bit values of charges stored in memory cells of a capacitor-like configuration, as discussed at length, earlier. Each one of lower power logic 696a-i, together with corresponding ones of unswitched power logic 697a-i, provides the interface logic that carries out commands received through memory buses 681 and 694 to either store data within or retrieve data from corresponding ones of memory cell arrays 699a-i, as well as carrying out other various functions. The splitting of this interface logic between lower power and unswitched power logic may, in some embodiments, allow the portions of this interface logic within each of unswitched power logic 697a-i that are more closely coupled to memory cell arrays 699a-i to use a form of unswitched power supplied via unswitched power line 674 having a voltage high enough to interact with corresponding ones of memory cell arrays 699a-i with signaling voltage levels that may be more easily compatible with memory cell arrays 699a-i. At the same time, this same splitting of interface logic may, in some embodiments, allow the portions of this interface logic within each of lower power logic 696a-i that are more closely coupled to buffer logic 692 and/or memory buses 681 and/or 694 to use the logic level power supplied

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via logic level power line 677 to interact with buffer logic 692 and/or memory buses 681 and/or 694 with signaling voltage levels that may be more easily compatible with buffer logic 692 and/or other devices coupled to memory bus 681 and/or 694. In various implementations, the voltage level of the logic level power supplied via logic level power line 677 is lower than the voltage level of the storage level power supplied via storage level power line 672 in recognition of the possible advantages of using lower voltage signaling across memory buses 681 and/or 694, including lower overall power consumption and shorter signal rise and fall times leading to opportunities to increase the transfer rate of addresses, commands and/or data across memory buses 681 and/or 694.

[0047] Also, in some embodiments, the separation of this interface logic between lower power logic 696a-i and unswitched power logic 697a-i may allow power supplied to at least those portions of the interface logic that are more closely coupled to buffer logic 692 and/or memory bus 681 and/or 694 (i.e., portions within lower power logic 696a-i) to be powered down by turning off the logic level power supplied via logic level power line 677 at times when some or all of the signal lines making up memory bus 681 are powered down. At such times when logic level power line 677 is powered down, both unswitched power line 674 and storage level power line 672 remain turned on to continue supplying unswitched power and storage level power to both unswitched power logic 697a-i and memory cell arrays 699a-i, respectively. Also, in some embodiments, the turning off of logic level power supplied via logic level power line 677 coincides with memory device 690 being placed in a lower power state such as self-refresh

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mode where at least a portion of unswitched power logic 697a-i uses the unswitched power that continues to be supplied via unswitched power line 674 to initiate and/or carry out refresh operations on portions (e.g., pages or rows of memory cells) of corresponding ones of memory cell arrays 699a-i.

[0048] In some embodiments, the voltage level of the unswitched power supplied via unswitched power line 674 is similar to the voltage level of the logic level power supplied via logic level power line 677. In such embodiments, although lower power logic 696a-i and unswitched power logic 697a-i are supplied with power at similar voltage levels such that efficiencies of lower voltage operation of logic circuits may be realized (as described at length, above) the supplying of separate unswitched power and logic level power may be done to allow for the switching off of the logic level power, as described above, while the unswitched power at a similar voltage level continues to be supplied. In other embodiments, the voltage level of the unswitched power supplied via unswitched power line 674 may be chosen to be somewhere between the voltage levels of the logic level power and storage level power so as to allow unswitched power logic 697a-i to operate with signaling levels chosen to be more easily compatible with both lower power logic 696a-i and memory cell arrays 699a-i, respectively.

[0049] As those skilled in the art will recognize, the exact decision of which portions of interface logic are to make up each of lower power logic 696a-i and which portions are to make up each of unswitched power logic 697a-i may be varied between specific embodiments without departing from the spirit and scope of the claimed invention. In some embodiments, the portions of interface logic

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making up each of unswitched power logic 697a-i may be limited to logic needed to carry out refresh operations, possibly including a row address decoder, so that these limited portions of interface logic continue to be supplied with power from unswitched power line 674 at times when logic level power line 677 is turned off as part of memory device 690 entering a lower power state.

[0050] **Figure 7** is a block diagram of still another embodiment employing a memory device, with memory device 790 being largely identical to memory device 590 of **Figure 5** except for the replacement of buffer logic 592 in memory device 590 with buffer logic 792 having a pair of point-to-point interfaces in memory device 790. The point-to-point interfaces of buffer logic 792 couple memory bus 794 of memory device 790 with memory busses 781 and 782, allowing memory device 790 to be coupled to one or two other devices making up a memory system, including memory controllers and/or other memory devices. Such point-to-point interfaces may be made up of sets of unidirectional signal lines (perhaps matched sets in opposite directions) and/or at least one set of bidirectional signal lines. In various embodiments, memory device 790 is made up, at least in part, of memory circuits 798a-i assembled together as ICs on a substrate or as dies within a multiple die package, and buffer logic 792. In some embodiments, memory device 790 is a fully buffered DIMM. Like memory device 590 of **Figure 5**, each of memory circuits 798a-i is made up, at least in part, of memory cell arrays 799a-i, higher power logic 797a-i and lower power logic 796a-i, respectively. Each of lower power logic 796a-i is coupled to memory buses 781 and 782 through buffer logic 792 and memory bus 794 for

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access to at least the majority of the signal lines making up memory buses 781 and 782, although there may be a smaller number of signals making memory buses 781 and/or 782 to which each of lower power logic 796a-i may be directly coupled. Both buffer logic 792 and lower power logic 796a-i are all supplied with logic level power from logic level power line 777, and both higher power logic 797a-i and memory cells 799a-i are all supplied with storage level power from storage level power line 772.

[0051] To ensure the reliable retention of the data stored in these memory cells, the storage level power supplied to each of memory cell arrays 799a-i is of sufficient voltage to allow reliable distinguishing between 0 and 1 bit values of charges stored in memory cells of a capacitor-like configuration, as discussed at length, earlier. Each one of lower power logic 796a-i, together with corresponding ones of higher power logic 797a-i, provides the interface logic that carries out commands received through memory buses 781, 782 and/or 794 to either store data within or retrieve data from corresponding ones of memory cell arrays 799a-i, as well as carrying out other various functions. The splitting of this interface logic between lower power and higher power logic may, in some embodiments, allow the portions of this interface logic within each of higher power logic 797a-i that are more closely coupled to memory cell arrays 799a-i to use the storage level power supplied via storage level power line 772 to interact with corresponding ones of memory cell arrays 799a-i with signaling voltage levels that may be more easily compatible with memory cell arrays 799a-i. At the same time, this same splitting of interface logic may, in some embodiments,

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allow the portions of this interface logic within each of lower power logic 796a-i that are more closely coupled to buffer logic 792 and/or memory buses 781, 782 and/or 794 to use the logic level power supplied via logic level power line 777 to interact with buffer logic 792 and/or memory buses 781, 782 and/or 794 with signaling voltage levels that may be more easily compatible with buffer logic 792 and/or other devices coupled to memory buses 781, 782 and/or 794. In various implementations, the voltage level of the logic level power supplied via logic level power line 777 is lower than the voltage level of the storage level power supplied via storage level power line 772 in recognition of the possible advantages of using lower voltage signaling with buffer logic 792 and/or across memory buses 781 and/or 782, including lower overall power consumption and shorter signal rise and fall times leading to opportunities to increase the transfer rate of addresses, commands and/or data across memory buses 781, 782 and/or 794.

[0052] Also, in some embodiments, the separation of this interface logic between lower power logic 796a-i and higher power logic 797a-i may allow power supplied to at least those portions of the interface logic that are more closely coupled to buffer logic 792 and/or memory buses 781, 782 and/or 794 (i.e., portions within lower power logic 796a-i) to be powered down by turning off the logic level power supplied via logic level power line 777 at times when some or all of the signal lines making up memory buses 781 and/or 782 are powered down. At such times when logic level power line 777 is powered down, storage level power line 772 remains turned on to continue supplying storage

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level power to both higher power logic 797a-i and memory cell arrays 799a-i. Also, in some embodiments, the turning off of logic level power supplied via logic level power line 777 coincides with memory device 790 being placed in a lower power state such as self-refresh mode where at least a portion of higher power logic 797a-i uses the storage level power that continues to be supplied via storage level power line 772 to initiate and/or carry out refresh operations on portions (e.g., pages or rows of memory cells) of corresponding ones of memory cell arrays 799a-i.

[0053] As was the case with memory device 590 of **Figure 5**, those skilled in the art will recognize that the exact decision of which portions of interface logic are to make up each of lower power logic 796a-i and which portions are to make up each of higher power logic 797a-i may be varied between specific embodiments without departing from the spirit and scope of the claimed invention. In some embodiments, the portions of interface logic making up each of higher power logic 797a-i may be limited to logic needed to carry out refresh operations, possibly including a row address decoder, so that these limited portions of interface logic continue to be supplied with power from storage level power line 772 at times when logic level power line 777 is turned off as part of memory device 790 entering a lower power state. In other embodiments, the design of each of memory cell arrays 799a-i may be such that any portions of interface logic directly coupled to the memory cells must be among those portions making up each of higher power logic 797a-i.

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[0054] **Figure 8** is a block diagram of yet another embodiment employing a memory device, with memory device 890 being largely identical to memory device 690 of **Figure 6** except for the replacement of buffer logic 692 in memory device 690 with buffer logic 892 having a pair of point-to-point interfaces in memory device 890. The point-to-point interfaces of buffer logic 892 couple memory bus 894 of memory device 890 with memory busses 881 and 882, allowing memory device 890 to be coupled to one or two other devices making up a memory system, including memory controllers and/or other memory devices. Such point-to-point interfaces may be made up of sets of unidirectional signal lines (perhaps matched sets in opposite directions) and/or at least one set of bidirectional signal lines. In various embodiments, memory device 890 is made up, at least in part, of memory circuits 898a-i assembled together as ICs on a substrate or as dies within a multiple die package, and buffer logic 892. In some embodiments, memory device 890 is a fully buffered DIMM. Like memory device 690 of **Figure 6**, each of memory circuits 898a-i is made up, at least in part, of memory cell arrays 899a-i, unswitched power logic 897a-i and lower power logic 896a-i, respectively. Each of lower power logic 896a-i is coupled to memory buses 881 and 882 through buffer logic 892 and memory bus 894 for access to at least the majority of the signal lines making up memory buses 881 and 882, although there may be a smaller number of signals making up memory buses 881 and/or 882 to which each of lower power logic 896a-i may be directly coupled. Both buffer logic 892 and lower power logic 896a-i are all supplied with logic level power from logic level power line 877, constant power logic

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897a-i are all supplied with unswitched power from unswitched power line 874, and memory cells 899a-i are all supplied with storage level power from storage level power line 872.

[0055] To ensure the reliable retention of the data stored in these memory cells, the storage level power supplied to each of memory cell arrays 899a-i is of sufficient voltage to allow reliable distinguishing between 0 and 1 bit values of charges stored in memory cells of a capacitor-like configuration, as discussed at length, earlier. Each one of lower power logic 896a-i, together with corresponding ones of unswitched power logic 897a-i, provides the interface logic that carries out commands received through memory buses 881, 882 and/or 894 to either store data within or retrieve data from corresponding ones of memory cell arrays 899a-i, as well as carrying out other various functions. The splitting of this interface logic between lower power and unswitched power logic may, in some embodiments, allow the portions of this interface logic within each of unswitched power logic 897a-i that are more closely coupled to memory cell arrays 899a-i to use a form of unswitched power supplied via unswitched power line 874 having a voltage high enough to interact with corresponding ones of memory cell arrays 899a-i with signaling voltage levels that may be more easily compatible with memory cell arrays 899a-i. At the same time, this same splitting of interface logic may, in some embodiments, allow the portions of this interface logic within each of lower power logic 896a-i that are more closely coupled to buffer logic 892 and/or memory buses 881, 882 and/or memory bus 894 to use the logic level power supplied via logic level power line 877 to interact with

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buffer logic 892 and/or memory buses 881, 882 and/or 894 with signaling voltage levels that may be more easily compatible with buffer logic 892 and/or other devices coupled to memory buses 881 and/or 882. In various implementations, the voltage level of the logic level power supplied via logic level power line 877 is lower than the voltage level of the storage level power supplied via storage level power line 872 in recognition of the possible advantages of using lower voltage signaling across memory buses 881, 882 and/or 894, including lower overall power consumption and shorter signal rise and fall times leading to opportunities to increase the transfer rate of addresses, commands and/or data across memory buses 881, 882 and/or 894.

[0056] Also, in some embodiments, the separation of this interface logic between lower power logic 896a-i and unswitched power logic 897a-i may allow power supplied to at least those portions of the interface logic that are more closely coupled to buffer logic 892 and/or memory buses 881, 882 and/or 894 (i.e., portions within lower power logic 696a-i) to be powered down by turning off the logic level power supplied via logic level power line 877 at times when some or all of the signal lines making up memory buses 881 and/or 882 are powered down. At such times when logic level power line 877 is powered down, both unswitched power line 874 and storage level power line 872 remain turned on to continue supplying unswitched power and storage level power to both unswitched power logic 897a-i and memory cell arrays 899a-i, respectively. Also, in some embodiments, the turning off of logic level power supplied via logic level power line 877 coincides with memory device 890 being placed in a

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lower power state such as self-refresh mode where at least a portion of unswitched power logic 897a-i uses the unswitched power that continues to be supplied via unswitched power line 874 to initiate and/or carry out refresh operations on portions (e.g., pages or rows of memory cells) of corresponding ones of memory cell arrays 899a-i.

[0057] In some embodiments, the voltage level of the unswitched power supplied via unswitched power line 874 is similar to the voltage level of the logic level power supplied via logic level power line 877. In such embodiments, although lower power logic 896a-i and unswitched power logic 897a-i are supplied with power at similar voltage levels such that efficiencies of lower voltage operation of logic circuits may be realized (as described at length, above) the supplying of separate unswitched power and logic level power may be done to allow for the switching off of the logic level power, as described above, while the unswitched power at a similar voltage level continues to be supplied. In other embodiments, the voltage level of the unswitched power supplied via unswitched power line 874 may be chosen to be somewhere between the voltage levels of the logic level power and storage level power so as to allow unswitched power logic 897a-i to operate with signaling levels chosen to be more easily compatible with both lower power logic 896a-i and memory cell arrays 899a-i, respectively.

[0058] As those skilled in the art will recognize, the exact decision of which portions of interface logic are to make up each of lower power logic 896a-i and which portions are to make up each of unswitched power logic 897a-i may be varied between specific embodiments without departing from the spirit and scope

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of the claimed invention. In some embodiments, the portions of interface logic making up each of unswitched power logic 897a-i may be limited to logic needed to carry out refresh operations, possibly including a row address decoder, so that these limited portions of interface logic continue to be supplied with power from unswitched power line 874 at times when logic level power line 877 is turned off as part of memory device 890 entering a lower power state.

[0059] It should be noted that as those skilled in the art of the design of memory devices, including DRAM devices, will readily recognize, **Figures 3 through 8** provide a relatively simple depiction of components making up a DRAM device, and that the exact arrangement and configuration of components within a DRAM device may be reduced, augmented or otherwise altered in comparison to what is depicted within those figures without departing from the spirit and scope of the present invention as hereinafter claimed. Specifically, as those skilled in the art will readily recognize, a quantity of memory circuits other than what is depicted in **Figures 3 through 8** is certainly possible without departing from the spirit and scope of the claimed invention. Also, specifically, although embodiments specifically employing 2 and 3 power connections/sources have been depicted and discussed, it will be understood by those skilled in the art that 4 or more power connections/sources may be employed to provide power to various subparts of a memory device without departing from the spirit and scope of the claimed invention.

[0060] **Figure 9** is a block diagram of an embodiment employing a computer system. Computer system 900 is, at least in part, made up of processor 910,

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system logic 920, and memory device 990. System logic 920 is coupled to processor 910 and performs various functions in support of processor 910 including providing processor 910 with access to memory device 990 to which system logic 920 is also coupled, using memory controller 980 within system logic 920. Processor 910, system logic 920 and memory device 990 make up a form of core for computer system 900 that is capable of supporting the execution of machine readable instructions by processor 910 and the storage of data and instructions within memory device 990. Alternatively, in other embodiments, memory controller 980 may be either partially or entirely integrated within processor 910, with the possible result of processor 910 being directly coupled to and having direct access to memory device 990.

[0061] In various embodiments, processor 910 could be any of a variety of types of processor including a processor capable of executing at least a portion of the widely known and used "x86" instruction set, and in other various embodiments, there could be more than one processor. In various embodiments, memory device 990 could be any of a variety of types of dynamic random access memory (RAM) including fast page mode (FPM), extended data out (EDO), single data rate (SDR) or double data rate (DDR) forms of synchronous dynamic RAM (SDRAM), RAM of various technologies employing a RAMBUS™ interface, etc., and memory controller 980 provides logic 920 with an appropriate interface for the type of memory. At least a portion of the memory cells of memory device 990 are divided into banks 999a-d, each of which are made up of memory cells organized into rows and columns in a two dimensional memory

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array. To access a portion of the memory cells within memory device 990, that portion must be addressed by memory controller 980 with a combination of bank, row and column addresses. As those skilled in the art will recognize, the depiction of a single memory device 990 with four banks of memory cells, namely banks 999a-999d, is but an example of a memory system that could be a part of a computer system, and that a larger number of memory devices and/or a differing number of banks within memory devices could be used without departing from the spirit and scope of the present invention as hereinafter claimed.

[0062] In some embodiments, system logic 920 is coupled to and provides processor 910 with access to storage device 960 by which data and/or instructions carried by storage media 961 may be accessed. Storage media 961 may be of any of a wide variety of types and technologies as those skilled in the art will understand, including CD or DVD ROM, magnetic or optical diskette, magneto-optical disk, tape, semiconductor memory, characters or perforations on paper or other material, etc. In some embodiments, nonvolatile memory device 930 is coupled to system logic 920 (or other part of computer system 900) and provides storage for an initial series of instructions executed at a time when computer system 900 is either "reset" or initialized (for example, when computer system 900 is "turned on" or "powered up") to perform tasks needed to prepare computer system 900 for normal use. In some variations of such embodiments, upon initialization or resetting of computer system 900, processor 910 accesses nonvolatile memory device 930 to retrieve instructions to be executed to prepare

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memory controller 970 for normal use in providing access for CPU 910 to memory device 990. It may be that these same retrieved instructions are executed to prepare system logic 920 for normal use in providing access to storage device 960 and whatever form of storage media 961 that may be used by storage device 960.

[0063] In some embodiments, computer system 900 is further made up of power source 970 supplying logic level power through power line 974, power control 976 and power line 977 to a portion of memory device 990, and supplying storage level power through power line 972 to another portion of memory device 990. In some variants of such embodiments, power control 976 may be operated by logic making up a portion of memory controller 980, and in other variants, power control 976 may be operated by another portion within a memory system making up computer system 900 or elsewhere within computer system 900, such as logic dedicated to the function of controlling the distribution of power.

[0064] In some embodiments, storage media 961 carries machine-accessible instructions to be executed by processor 910 to cause processor 910 to carry out one or more tests of memory device 990 to determine what type of DRAM device memory device 990 may be, and/or to determine what functions memory device 990 may support. Such tests may include a series of attempted accesses to portions of memory device 990 and observation of the nature of the responses, received. Alternatively, such tests may include interrogating a code identifying the type of memory device or identifying the presence of one or more features, or such tests may entail reading data stored in a portion of nonvolatile memory

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within memory device 990 identifying the type of memory device, various parameters, and/or the presence or absence of various features. If it is determined that memory device 990 supports the use of a segmented power supply, as described at length above, then processor 910 may be caused to program or otherwise configure memory controller 980 and/or other logic within computer system 900 to operate power control 976 to make use of such a capability.

[0065] In other embodiments, a characteristic of the design of computer system 900, such as the physical design of a connector by which memory device 990 is coupled to the rest of computer system 900, may preclude the use of memory devices that do not support the use of a segmented power supply. In such embodiments, it may then be presumed that any memory device, such as memory device 990, that could be connected to the rest of computer system 900 would, therefore, necessarily support a segmented power system, and so processor 910 may be caused to execute instructions to prepare the use of power control 976 to selectively supply a portion of memory device 990 with power without having carried out a test to confirm that memory device 990 supports a segmented power supply.

[0066] The invention has been described in conjunction with various possible embodiments. It is evident that numerous alternatives, modifications, variations and uses will be apparent to those skilled in the art in light of the foregoing description. It will be understood by those skilled in the art that the present invention may be practiced in support of various types of electronic devices with various possible memory devices in which the memory cells repeatedly require

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some form of "refreshing" or other regular maintenance activity in order to prevent the loss of data. It will also be understood by those skilled in the art that the present invention may be practiced in support of electronic devices other than computer systems such as audio/video entertainment devices, controller devices in vehicles, appliances controlled by electronic circuitry, etc.

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CLAIMS

What is claimed is:

1. A DRAM IC comprising:

a first external connection to receive a first power supply voltage;

a second external connection to receive a second power supply voltage that is lower in voltage than the first power supply voltage;

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage; and

a second logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both received data to store within and output data retrieve from the selected memory cells, wherein the second logic is powered by the second power supply voltage.

2. The DRAM IC of claim 1, wherein the first logic is coupled to the plurality of bit lines, and both transmits data across the plurality bit lines to the plurality of memory cells and receives data from across the plurality of bit lines from the memory cells.

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3. The DRAM IC of claim 1, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

4. The DRAM IC of claim 3, wherein the first logic is comprised of refresh logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the DRAM IC is placed in a lower power state in which the second logic is deprived of power as a result of the second power supply voltage being removed.

5. A DRAM IC comprising:

a first external connection to receive a first power supply voltage;

a second external connection to receive a second power supply voltage that is lower in voltage than the first power supply voltage;

a third external connection to receive a third power supply voltage that is lower in voltage than the first power supply voltage;

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage;

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a second logic coupled to the first logic to control at least a portion of the first logic, wherein the second logic is powered by the second power supply voltage; and

a third logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both receive data to store within and output data retrieved from the selected memory cells, wherein the third logic is powered by the third power supply voltage.

6. The DRAM IC of claim 5, wherein the first logic is coupled to the plurality of bit lines, and both transmits data across the plurality bit lines to the plurality of memory cells and receives data from across the plurality of bit lines from the memory cells.

7. The DRAM IC of claim 5, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

8. The DRAM IC of claim 7, wherein the second logic is comprised of refresh logic control the at least a portion of the first logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the DRAM IC is placed in a lower power state in which the third logic is deprived of power as a result of the third power supply voltage being removed.

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9. A memory device comprising:

a circuitboard;

a plurality of electrical contacts carried by the circuitboard to couple the circuitboard to a memory bus and to at least a first power supply voltage and a second power supply voltage; and

at least one DRAM IC comprising:

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage; and

a second logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both receive data to store within and output data retrieved from the selected memory cells, wherein the second logic is powered by the second power supply voltage.

10. The memory device of claim 9 wherein the external interface of the at least one DRAM IC is directly coupled to at least a subset of the electrical contacts carried by the circuitboard to further couple the external interface of the at least one DRAM IC to the memory bus.

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11. The memory device of claim 9, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

12. The memory device of claim 11, wherein the first logic is comprised of refresh logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the second logic is deprived of power as a result of the second power supply voltage being removed.

13. The memory device of claim 12, further comprising at least one interposed IC coupled to at least a subset of the electrical contacts carried by the circuitboard and to the external interface of the at least one DRAM IC to at least buffer at least a subset of the signals communicated between the at least one DRAM IC and the memory bus, wherein the at least one interposed IC is powered by the second power supply voltage, and the at least DRAM IC carries out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the at least one interposed IC is deprived of power as a result of the second power supply voltage being removed.

14. A memory device comprising:

a circuitboard;

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a plurality of electrical contacts carried by the circuitboard to couple the circuitboard to a memory bus and to at least a first power supply voltage, a second power supply voltage, and a third power supply voltage; and

at least one DRAM IC comprising:

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage;

a second logic coupled to the first logic to control at least a portion of the first logic, wherein the second logic is powered by the second power supply voltage; and

a third logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both receive data to store within and output data retrieved from the selected memory cells, wherein the third logic is powered by the third power supply voltage.

15. The memory device of claim 14 wherein the external interface of the at least one DRAM IC is directly coupled to at least a subset of the electrical contacts carried by the circuitboard to further couple the external interface of the at least one DRAM IC to the memory bus.

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16. The memory device of claim 14, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

17. The memory device of claim 16, wherein the second logic is comprised of refresh logic control the at least a portion of the first logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the third logic is deprived of power as a result of the third power supply voltage being removed.

18. The memory device of claim 17, further comprising at least one interposed IC coupled to at least a subset of the electrical contacts carried by the circuitboard and to the external interface of the at least one DRAM IC to at least buffer at least a subset of the signals communicated between the at least one DRAM IC and the memory bus, wherein the at least one interposed IC is powered by the third power supply voltage, and the at least DRAM IC carries out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the at least one interposed IC is deprived of power as a result of the third power supply voltage being removed.

19. An apparatus comprising:

a processor;

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a core logic providing a memory controller coupled to the processor to provide a memory bus;

a first power source providing a first power supply voltage;

a second power source providing a second power supply voltage;

a power control circuit coupled to the core logic to selectively enable provision of the second power supply voltage; and

at least one DRAM IC comprising:

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage; and

a second logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both received data to store within and output data retrieve from the selected memory cells, wherein the second logic is powered by the second power supply voltage.

20. The apparatus of claim 19, wherein the external interface of the at least one DRAM IC is directly coupled to the memory bus.

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21. The apparatus of claim 19, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

22. The apparatus of claim 21, wherein the first logic is comprised of refresh logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the second logic is deprived of power as a result of the second power supply voltage being removed by the power control circuit.

23. The apparatus of claim 22, further comprising at least one interposed IC coupled to at least a subset of the memory bus and to the external interface of the at least one DRAM IC to at least buffer at least a subset of the signals communicated between the at least one DRAM IC and the memory bus, wherein the at least one interposed IC is powered by the second power supply voltage, and the at least DRAM IC carries out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the at least one interposed IC is deprived of power as a result of the second power supply voltage being removed by the power control circuit.

24. An apparatus comprising:

a processor;

a core logic providing a memory controller coupled to the processor to provide a memory bus;

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a first power source providing a first power supply voltage;

a second power source providing a second power supply voltage;

a third power source providing a third power supply voltage;

a power control circuit coupled to the core logic to selectively enable provision of the third power supply voltage; and

at least one DRAM IC comprising:

a plurality of memory cells organized into a two-dimensional array to store data, wherein the memory cells are powered by the first power supply voltage, receive and output data through a plurality of bit lines coupled to the plurality of memory cells, and are controlled through a plurality of word lines coupled to the plurality of memory cells;

a first logic directly coupled to the memory cells to at least transmit signals to the memory cells, wherein the first logic is powered by the first power supply voltage;

a second logic coupled to the first logic to control at least a portion of the first logic, wherein the second logic is powered by the second power supply voltage; and

a third logic coupled to the first logic to provide an external interface to receive commands and addresses to select memory cells from among the plurality of memory cells for access, and to both receive data to store within and output data retrieved from the selected memory cells, wherein the third logic is powered by the third power supply voltage.

25. The apparatus of claim 24, wherein the external interface of the at least one DRAM IC is directly coupled to the memory bus.

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26. The apparatus of claim 24, wherein the first logic is coupled to the plurality of word lines and transmits row activation signals across the plurality of word lines to the plurality of memory cells.

27. The apparatus of claim 26, wherein the second logic is comprised of refresh logic control the at least a portion of the first logic to operate the plurality of word lines to carry out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the third logic is deprived of power as a result of the third power supply voltage being removed by the power control circuit.

28. The apparatus of claim 27, further comprising at least one interposed IC coupled to at least a subset of the electrical contacts carried by the circuitboard and to the external interface of the at least one DRAM IC to at least buffer at least a subset of the signals communicated between the at least one DRAM IC and the memory bus, wherein the at least one interposed IC is powered by the third power supply voltage, and the at least DRAM IC carries out refresh operations to preserve data stored within the plurality of memory cells while the memory device is placed in a lower power state in which the at least one interposed IC is deprived of power as a result of the third power supply voltage being removed by the power control circuit.

29. A method comprising:

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signaling a memory device to enter into a lower power state, wherein the memory device is comprised of a plurality of memory cells organized into at least one two-dimensional array of rows and columns, a first logic to at least transmit signals to the memory cells and second logic to provide an external interface, wherein the memory cells and the first logic are powered by the first power supply voltage, and wherein the second logic is powered by the second power supply voltage;

depriving the second logic of power by removing the second power supply voltage;

carrying out at least one refresh operation wherein the first logic signals a row of the plurality of the memory cells through a word line to which the row of the plurality of memory cells and the first logic are coupled;

restoring the second power supply voltage to the second logic by providing the second power supply voltage; and

signaling the memory device to exit the lower power state.

30. The method of claim 29, further comprising:

depriving an interposed IC of power by removing the second power supply voltage at substantially the same time that power is removed from the second logic, wherein the interposed IC is coupled to the external memory interface of the memory device and is powered by the second power supply voltage; and

restoring power to the interposed IC by providing the second power supply voltage.

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31. A machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to:

signal a memory device to enter into a lower power state, wherein the memory device is comprised of a plurality of memory cells organized into at least one two-dimensional array of rows and columns, a first logic to at least transmit signals to the memory cells and second logic to provide an external interface, wherein the memory cells and the first logic are powered by the first power supply voltage, and wherein the second logic is powered by the second power supply voltage;

deprive the second logic of power by removing the second power supply voltage;

signal the first logic to carry out at least one refresh operation wherein the first logic signals a row of the plurality of the memory cells through a word line to which the row of the plurality of memory cells and the first logic are coupled;

restore the second power supply voltage to the second logic by providing the second power supply voltage; and

signaling the memory device to exit the lower power state.

32. The machine-accessible medium of claim 31, further causing the processor to:

deprive an interposed IC of power by removing the second power supply voltage at substantially the same time that power is removed from the second logic, wherein the interposed IC is coupled to the external memory interface of the memory device and is powered by the second power supply voltage; and

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restore power to the interposed IC by providing the second power supply voltage.

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FIGURE 1

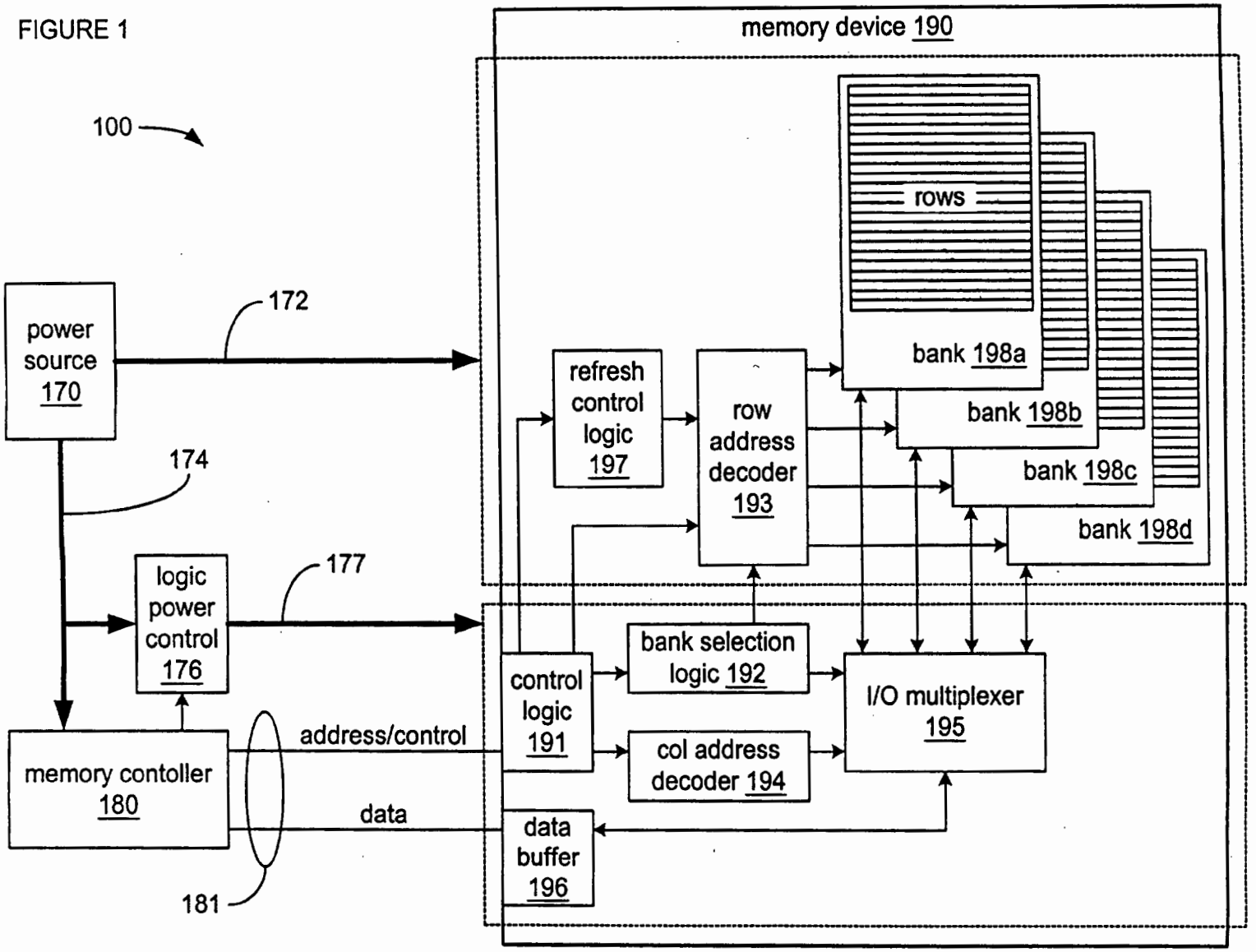
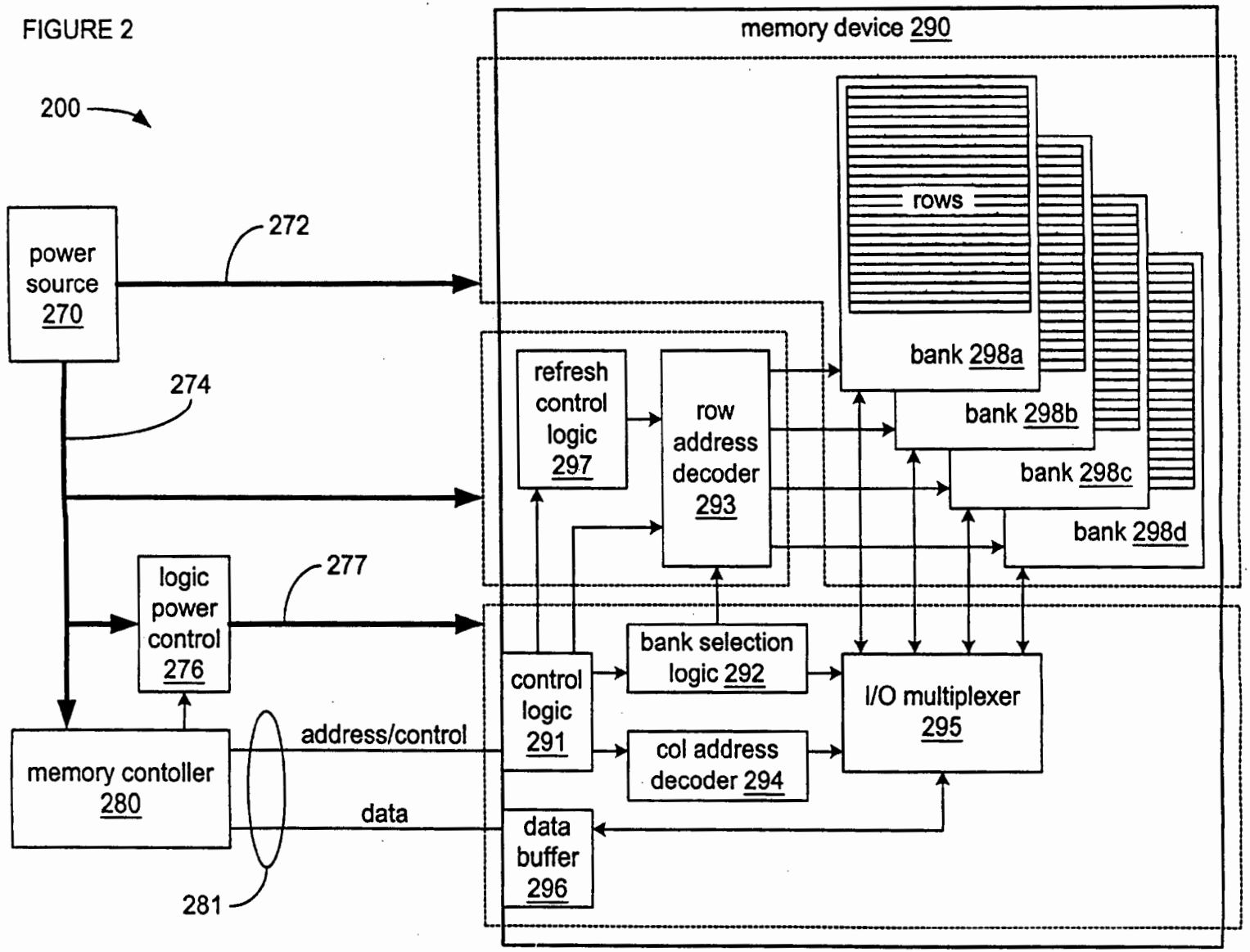

100
memory device 190
rows
bank 198a
bank 198b
bank 198c
bank 198d
power source 170
172
174
refresh control logic 197
row address decoder 193
logic power control 176
177
bank selection logic 192
control logic 191
I/O multiplexer 195
col address decoder 194
memory contoller 180
address/control
data
data buffer 196
181

FIGURE 2



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FIGURE 3

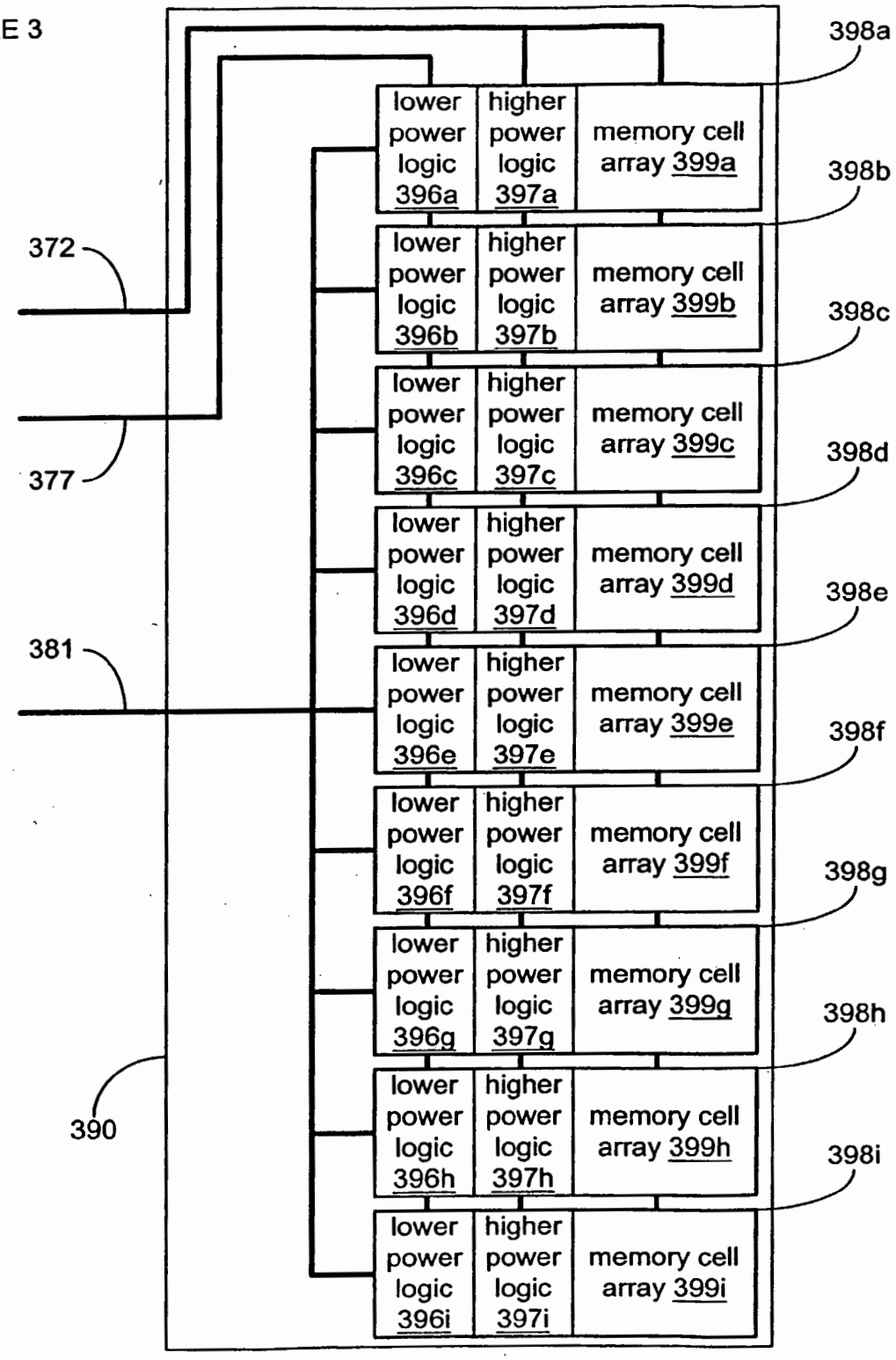

398a
lower power logic 396a
higher power logic 397a
memory cell array 399a
398b
372
lower power logic 396b
higher power logic 397b
memory cell array 399b
398c
lower power logic 396c
higher power logic 397c
memory cell array 399c
377
398d
lower power logic 396d
higher power logic 397d
memory cell array 399d
398e
381
lower power logic 396e
higher power logic 397e
memory cell array 399e
398f
lower power logic 396f
higher power logic 397f
memory cell array 399f
398g
lower power logic 396g
higher power logic 397g
memory cell array 399g
398h
390
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higher power logic 397h
memory cell array 399h
398i
lower power logic 396i
higher power logic 397i
memory cell array 399i

FIGURE 4

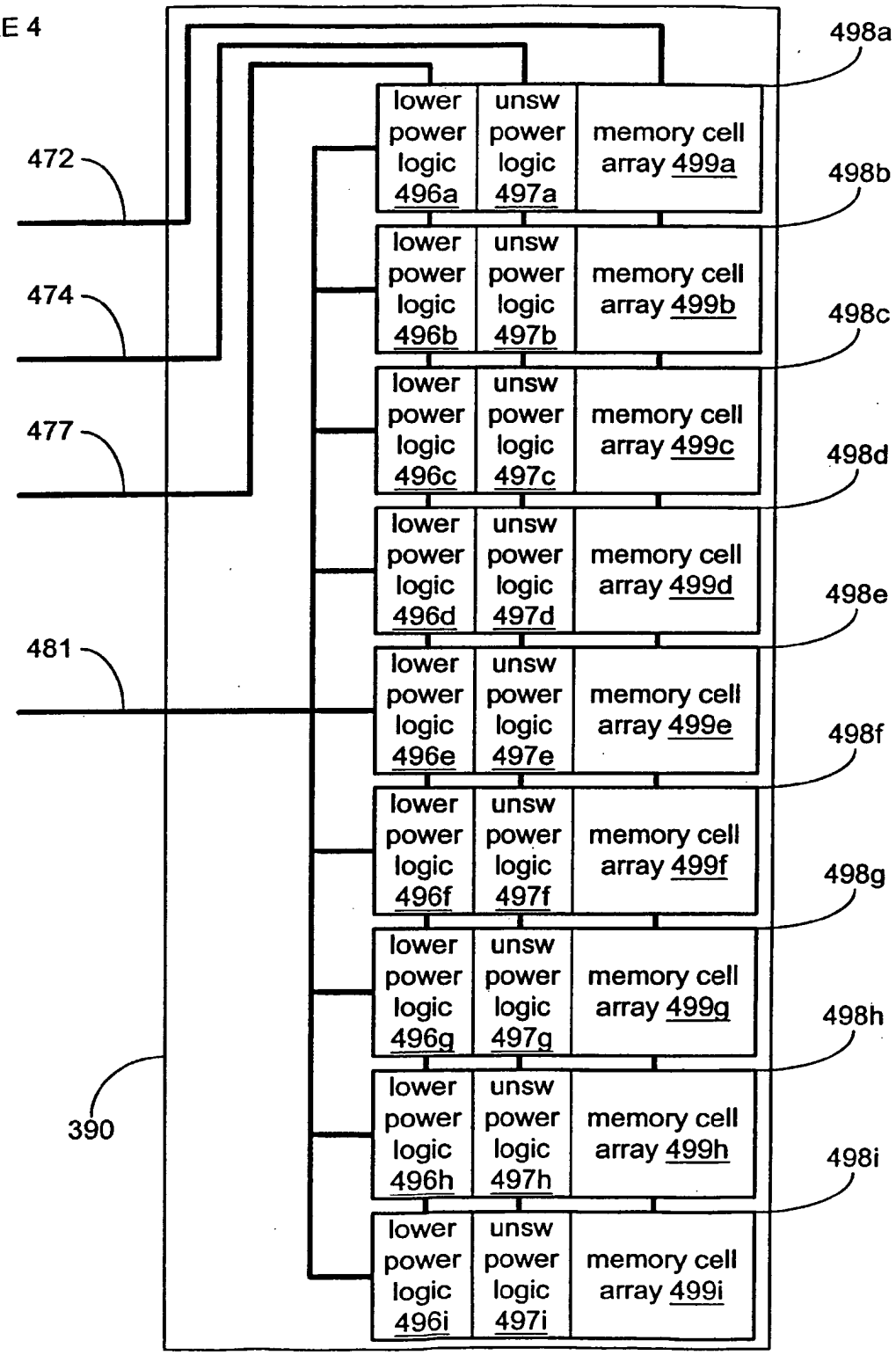

498a
498b
498c
498d
498e
498f
498g
498h
498i
472
474
477
481
390
lower power logic 496a
unsw power logic 497a
memory cell array 499a
lower power logic 496b
unsw power logic 497b
memory cell array 499b
lower power logic 496c
unsw power logic 497c
memory cell array 499c
lower power logic 496d
unsw power logic 497d
memory cell array 499d
lower power logic 496e
unsw power logic 497e
memory cell array 499e
lower power logic 496f
unsw power logic 497f
memory cell array 499f
lower power logic 496g
unsw power logic 497g
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lower power logic 496h
unsw power logic 497h
memory cell array 499h
lower power logic 496i
unsw power logic 497i
memory cell array 499i

FIGURE 5

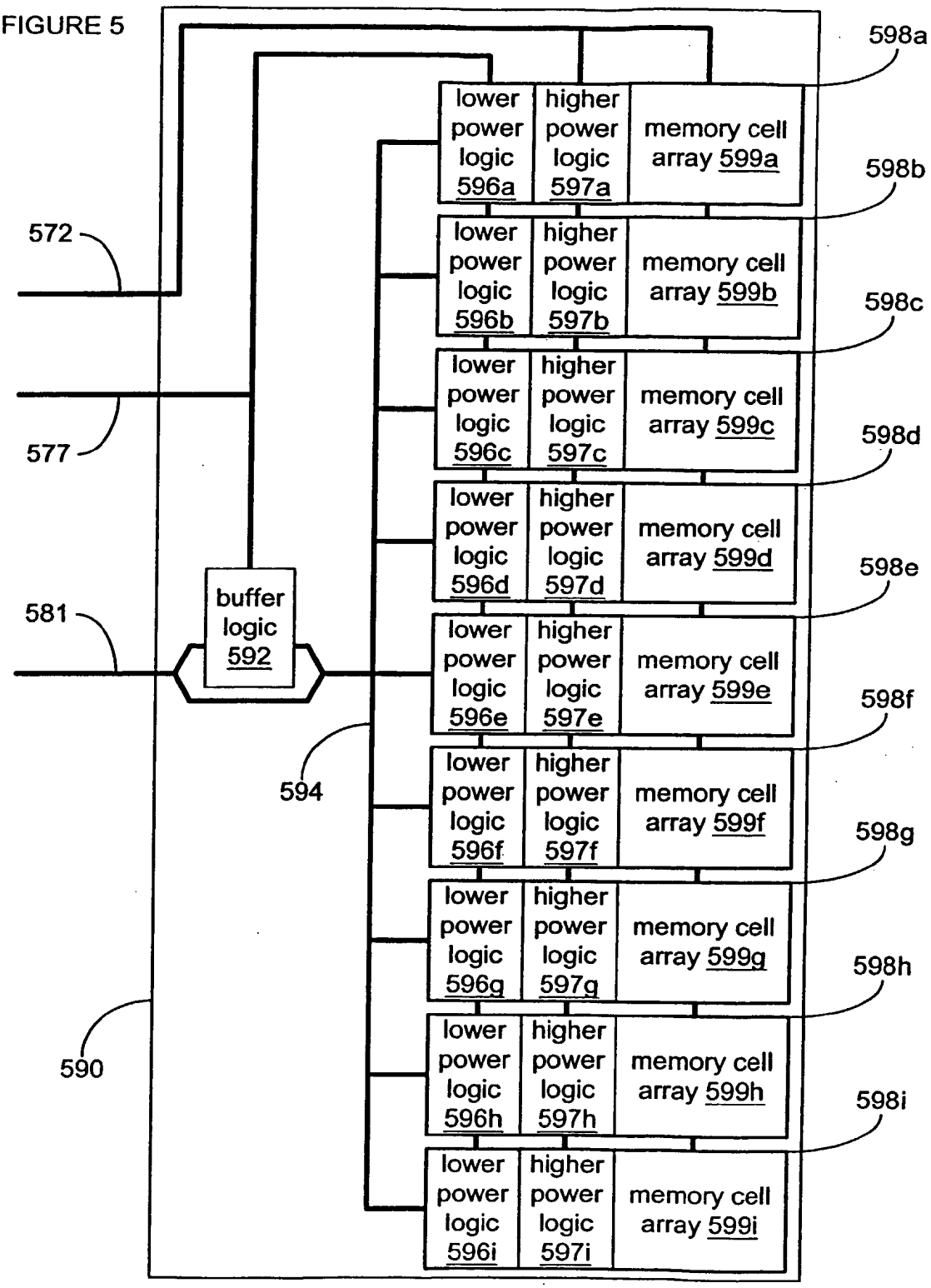

598a
598b
598c
598d
598e
598f
598g
598h
598i
572
577
581
590
594
buffer logic 592
lower power logic 596a
higher power logic 597a
memory cell array 599a
lower power logic 596b
higher power logic 597b
memory cell array 599b
lower power logic 596c
higher power logic 597c
memory cell array 599c
lower power logic 596d
higher power logic 597d
memory cell array 599d
lower power logic 596e
higher power logic 597e
memory cell array 599e
lower power logic 596f
higher power logic 597f
memory cell array 599f
lower power logic 596g
higher power logic 597g
memory cell array 599g
lower power logic 596h
higher power logic 597h
memory cell array 599h
lower power logic 596i
higher power logic 597i
memory cell array 599i

FIGURE 6

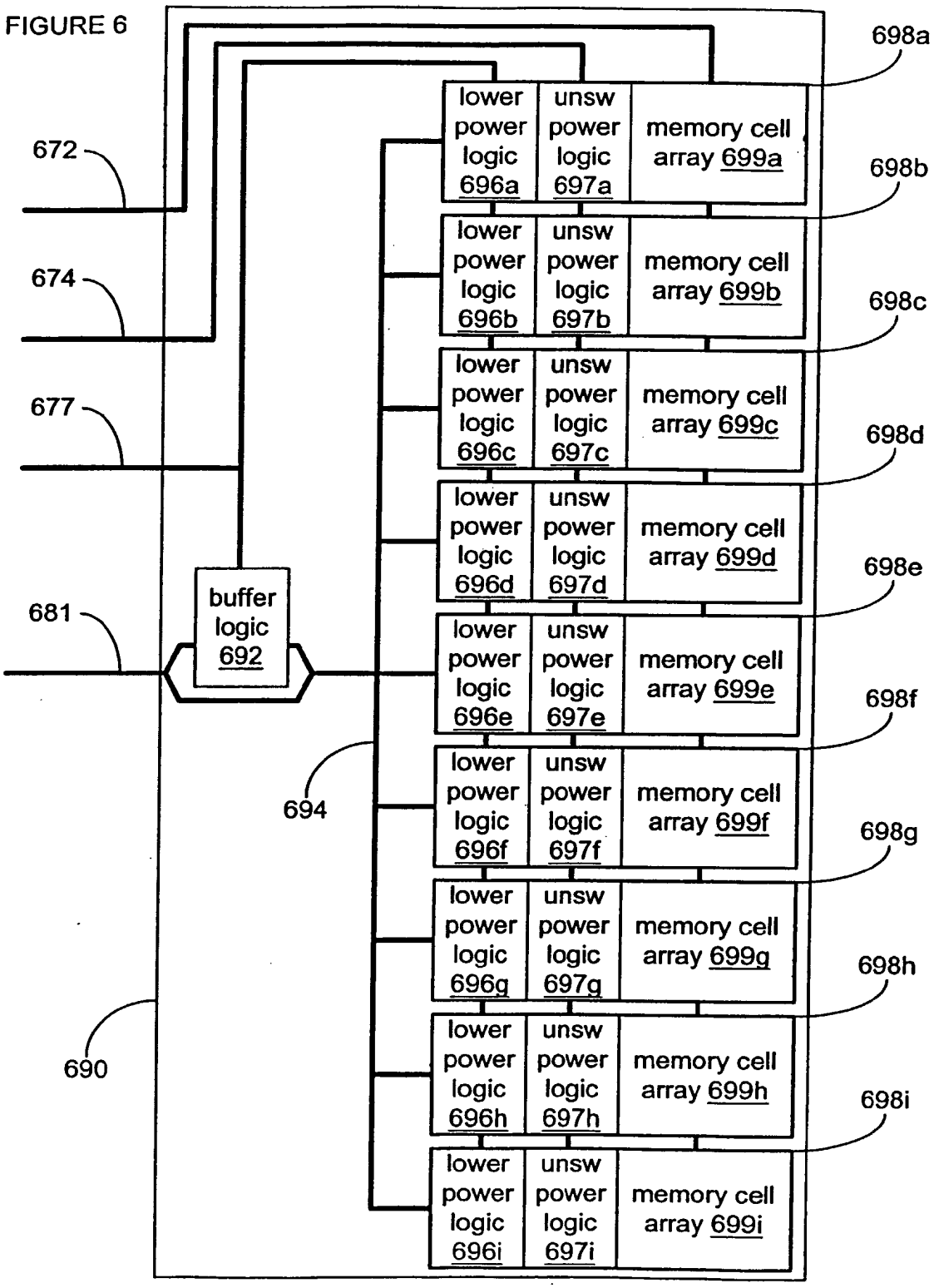

672
674
677
681
690
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buffer logic 692
lower power logic 696a
unsw power logic 697a
memory cell array 699a
698a
lower power logic 696b
unsw power logic 697b
memory cell array 699b
698b
lower power logic 696c
unsw power logic 697c
memory cell array 699c
698c
lower power logic 696d
unsw power logic 697d
memory cell array 699d
698d
lower power logic 696e
unsw power logic 697e
memory cell array 699e
698e
lower power logic 696f
unsw power logic 697f
memory cell array 699f
698f
lower power logic 696g
unsw power logic 697g
memory cell array 699g
698g
lower power logic 696h
unsw power logic 697h
memory cell array 699h
698h
lower power logic 696i
unsw power logic 697i
memory cell array 699i
698i

FIGURE 7

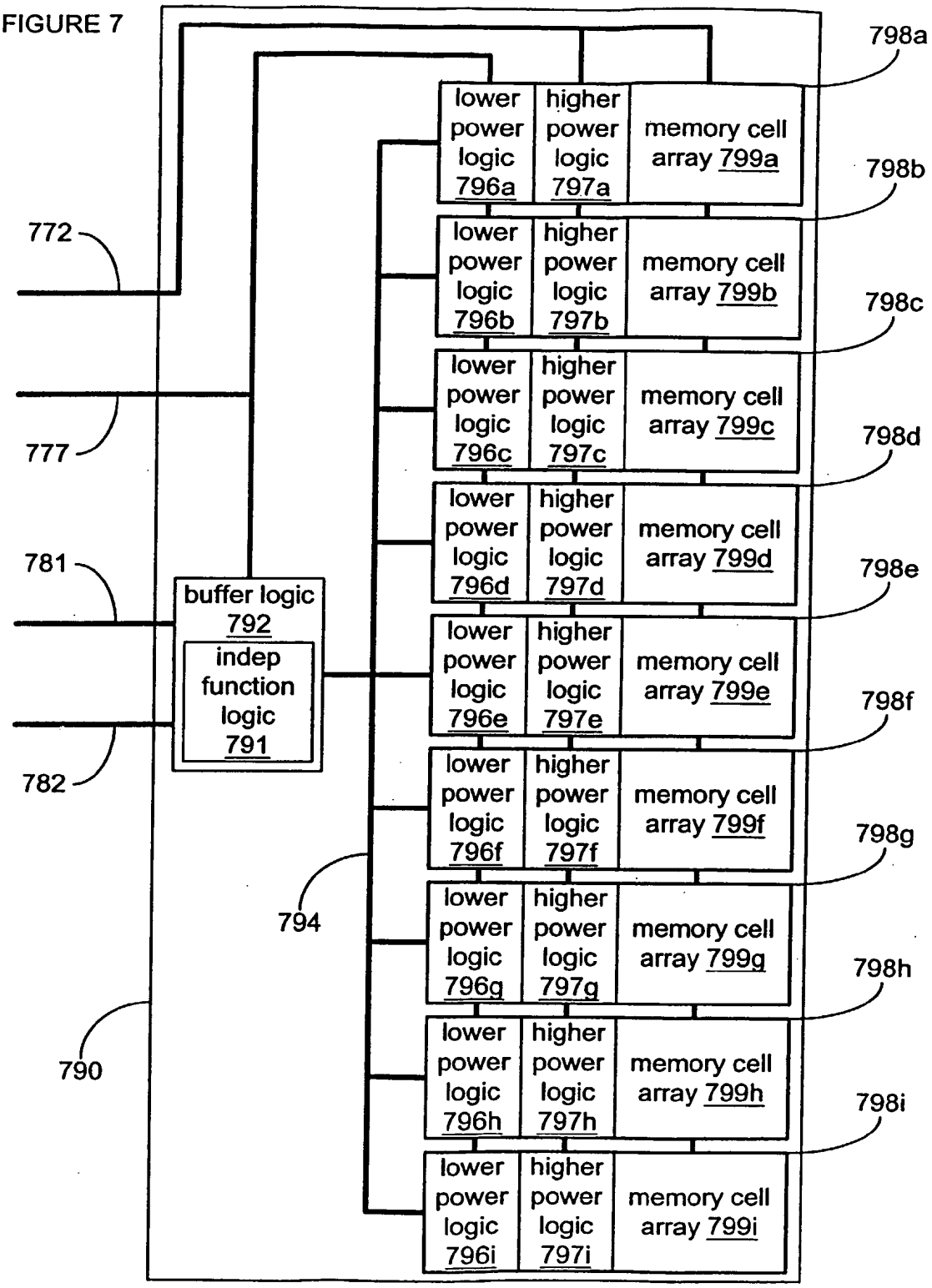
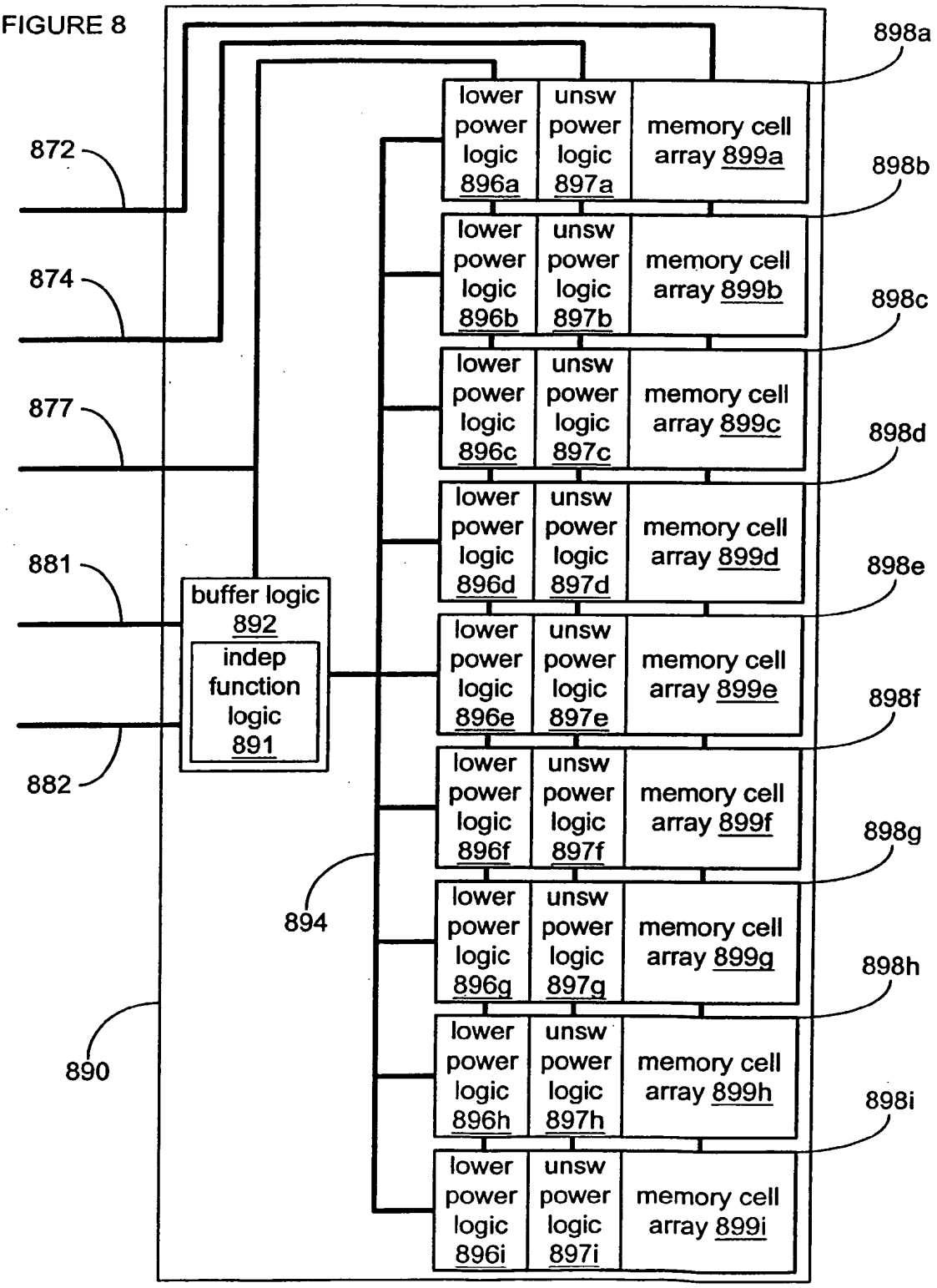

798a
798b
798c
798d
798e
798f
798g
798h
798i
772
777
781
782
790
794
buffer logic 792
indep function logic 791
lower power logic 796a
higher power logic 797a
memory cell array 799a
lower power logic 796b
higher power logic 797b
memory cell array 799b
lower power logic 796c
higher power logic 797c
memory cell array 799c
lower power logic 796d
higher power logic 797d
memory cell array 799d
lower power logic 796e
higher power logic 797e
memory cell array 799e
lower power logic 796f
higher power logic 797f
memory cell array 799f
lower power logic 796g
higher power logic 797g
memory cell array 799g
lower power logic 796h
higher power logic 797h
memory cell array 799h
lower power logic 796i
higher power logic 797i
memory cell array 799i

FIGURE 8


898a
898b
898c
898d
898e
898f
898g
898h
898i
872
874
877
881
882
890
894
buffer logic 892
indep function logic 891
lower power logic 896a
unsw power logic 897a
memory cell array 899a
lower power logic 896b
unsw power logic 897b
memory cell array 899b
lower power logic 896c
unsw power logic 897c
memory cell array 899c
lower power logic 896d
unsw power logic 897d
memory cell array 899d
lower power logic 896e
unsw power logic 897e
memory cell array 899e
lower power logic 896f
unsw power logic 897f
memory cell array 899f
lower power logic 896g
unsw power logic 897g
memory cell array 899g
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memory cell array 899h
lower power logic 896i
unsw power logic 897i
memory cell array 899i

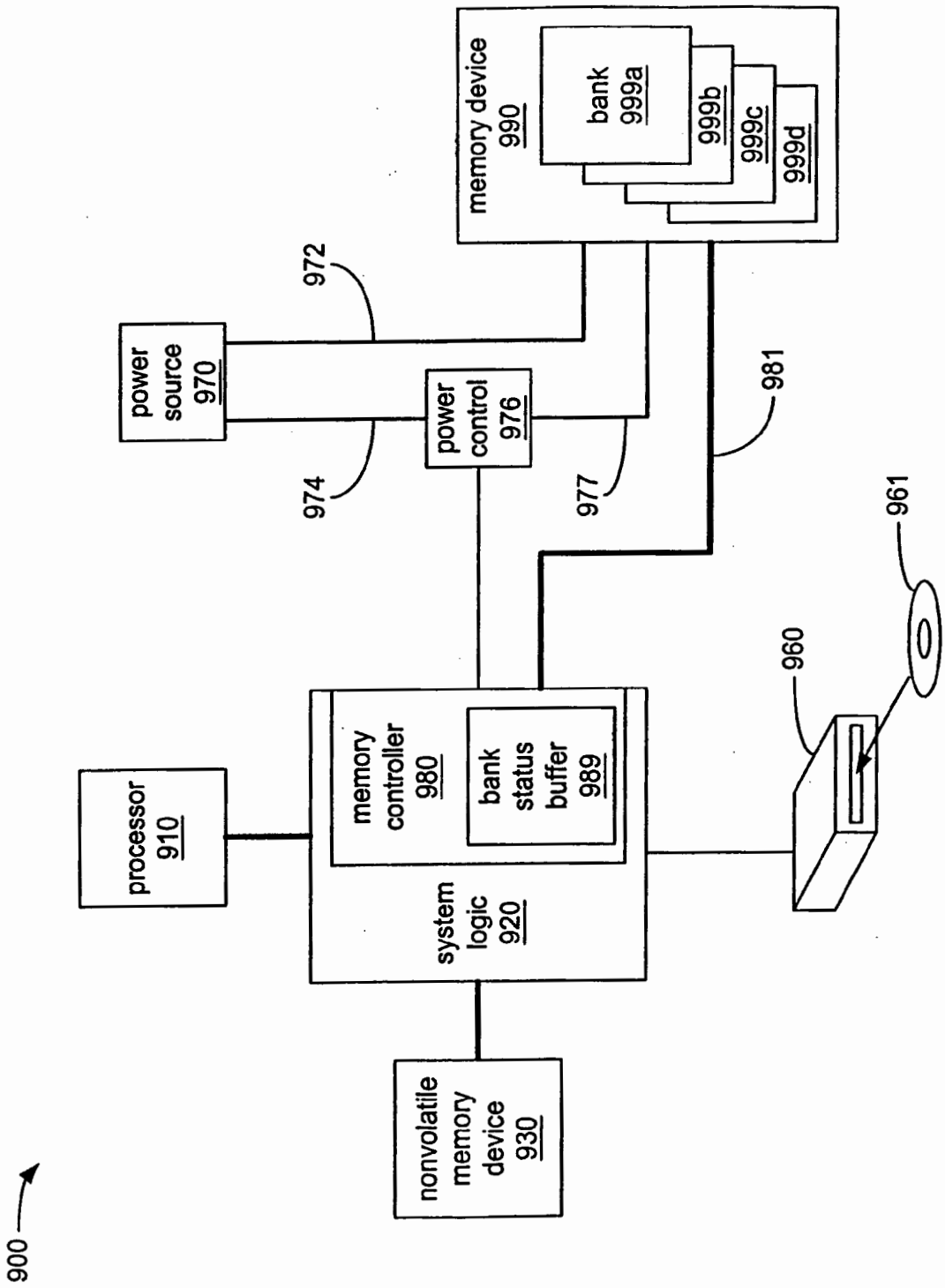


FIGURE 9

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INTERNATIONAL SEARCH REPORT

Inter al Application No
PCT/EP2004/043496

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C11/406 G11C11/4074 G11C5/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 074 993 A (MITSUBISHI DENKI KABUSHIKI KAISHA) 7 February 2001 (2001-02-07) paragraphs '0101!, '0107!; figures 1-6,16-22	1-32

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 April 2005	12/05/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Vidal Verdu, J.

Form PCT/ISA/210 (second sheet) (January 2004)

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INTERNATIONAL SEARCH REPORT

Interr ıl Application No
PCT/US2004/043496

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Form PCT/ISA/210 (patent family annex) (January 2004)

PatentOrder

Publication number: **JP2006268419 A2**
Publication country: JAPAN
Publication type: APPLICATION
Publication date: 20061005
Application number: JP20050085423
Application date: 20050324
Priority: JP20050085423 [20050324]
Assignee: 日本電気株式会社
Assignee^{std}: NEC CORP
Inventor: 服部 悟
Inventor^{std}: HATTORI SATORU
International class^{8}: G06F1/26; G06F1/30; G06F12/16; H02J9/00
Title: MEMORY BACKUP CIRCUIT AND ELECTRONIC EQUIPMENT USING THE SAME
メモリバックアップ回路およびこれを用いた電子機器

Abstract:

PROBLEM TO BE SOLVED: To prolong the service life of a battery by avoiding a backup malfunction caused by a single failure of a power failure detection circuit. SOLUTION: For example, a memory backup circuit of a disk array device is provided with a direct current power source circuit for inputting external power and outputting a direct current voltage necessary to the circuit; a first power failure detection circuit for monitoring an input state of the external power; a second power failure detection circuit for monitoring an output voltage of the direct current power source circuit; a backup power source for supplying power to a nonvolatile memory when the external power is lost; a memory control means for executing backup control of the nonvolatile memory in the case of receiving a power failure detection signal from the first or second power failure detecting means; and a switching means for supplying the power of the backup power source to the memory control means for a prescribed time when only the second power failure detecting means detects voltage reduction.

【課題】 停電検出回路の単一故障によるバックアップ動作不良を回避し、バッテリの長寿命化を実現する。【解決手段】 例えばディスクアレイ装置のメモリバックアップ回路に、外部電力を入力し回路に必要な直流電圧を出力する直流電源回路と、前記外部電力の入力状態を監視する第１の停電検出回路と、前記直流電源回路の出力電圧を監視する第２の停電検出回路と、前記外部電力の消失時に揮発性メモリへ電力を供給するバックアップ電源と、前記第１または第２の停電検出手段から停電検出信号を受けた場合に前記揮発性メモリのバックアップ制御を実施するメモリ制御手段と、前記第２の停電検出手段のみが電圧低下を検出した場合に前記バックアップ電源の電力を所定期間前記メモリ制御手段へ供給するスイッチ手段とを設ける。【選択図】 図１

Claims:

1. 外部電力を入力し回路に必要な直流電圧を出力する直流電源回路と、前記外部電力の入力状態を監視する第１の停電検出回路と、前記直流電源回路の出力電圧を監視する第２の停電検出回路と、前記外部電力の消失時に揮発性メモリへ電力を供給するバックアップ電源と、前記第１または第２の停電検出手段から停電検出信号を受けた場合に前記揮発性メモリのバックアップ制御を実施するメモリ制御手段と、前記第２の停電検出手段のみが電圧低下を検出した場合に前記バックアップ電源の電力を所定期間前記メモリ制御手段へ供給するスイッチ手段を備えることを特徴とするメモリバックアップ回路。

2. 請求項１に記載のメモリバックアップ回路において、前記第２の停電検出回路が電圧低下を検出した場合に検出信号を所定期間だけ出力するタイマ回路を備えることを特徴とするメモリバックアップ回路。

3. 請求項２に記載のメモリバックアップ回路において、前記スイッチ手段は、前記第１の停電検出回路の停電検出信号がなく、且つ前記タイマ回路の検出信号がある場合に、前記バックアップ電源の電力を前記メモリ制御手段に供給するよう制御されることを特徴とするメモリバックアップ回路。

4. 請求項１乃至３のいずれかに記載のメモリバックアップ回路において、前記メモリ制御手段は、前記第１または第２の停電検出手段から停電検出信号を受けた場合に、前記揮発性メモリの格納データを不揮発性メモリに待避させる処理を所定期間行い、その後前記揮発性メモリをセルフリフレッシュモードに移行させることを特徴とするメモリバックアップ回路。

5. 請求項１乃至４のいずれかに記載のメモリバックアップ回路を具備することを特徴とする電子機器。

6. 請求項５に記載の電子機器であって、当該機器がディスクアレイ装置であることを特徴とする電子機器。

1. circuit that outputs a DC voltage DC power supply circuits necessary to enter a foreign power, and power failure detection circuit to monitor the status of the first input of said external power to monitor the output voltage of said DC power supply power failure detection circuit and a second, to provide power and backup power to volatile memory upon loss of external power, wherein said volatile memory when the power failure detection signal is received from the power failure detection means the first or second control means for controlling the memory to perform backups, and comprising switch means for supplying said memory control means to supply backup power above the predetermined period when the voltage drop is detected, only the second power failure detector memory backup circuit to.

2. In memory backup circuit according to claim 1, memory backup and a timer circuit comprises a predetermined period to output a detection signal when detecting a voltage drop detection circuit of the second power outage circuit.

3. In memory backup circuit according to claim 2, wherein the switch means, without the power failure detection signal of the first power failure detection circuit, if the detection signal and said timer circuit, said backup power supply and a memory backup circuit is controlled to supply power to said memory control means.

4. In memory backup circuit according to any one of claims 1 to 3, wherein the memory control means, when the power failure detection signal is received from the detection means first or second power failure, said volatile processing is performed at a predetermined time saved in nonvolatile memory to store data in memory, and a memory backup circuit can move the self-refresh mode and then said volatile memory.

5. electronic device characterized by comprising a memory backup circuit according to any one of claims 1 to 4.

6. The electronic apparatus according to claim 5, wherein the electronic device and the disk array device in question.

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Description:

[0001] 本発明はメモリバックアップ回路に関し、特に、停電時に揮発性メモリの内容を確実に保護する技術に関する。

[0002] 従来より、例えば不意の停電時等に、電子機器における揮発性メモリの内容を保護する技術が提案されている。例えば特許文献１には、主電源の出力低下や電源供給の停止を検知して、バックアップ電源の電力を内容保持の必要があるメモリのみに供給するようにした電源供給回路が開示されている。また、特許文献２には電源回路の出力電圧低下を瞬時に検知し、予備電源を用いてＣＰＵに電源を供給することにより、ＣＰＵで行われる各種処理等の経過や過程を記憶するメモリの記憶内容が保持されるようにした電卓が開示されている。また、特許文献３には、停電を検知すると直ちに実行中のプログラムを中断して停電回復時に必要なデータをメモリに書き込み、その後停電が回復すれば中断していたプログラムを再開し処理を続行するが、停電が続いた場合にはＣＰＵの動作を停止し、電力回復時にメモリに保持されているデータを復旧する回路が開示されている。

[0003] 特開２００１－１７５３６４号公報特開２００３－６７０８９号公報特開平５－１０８５０３号公報

[0004] しかしながら、上記特許文献１の回路では、停電が長引いてバッテリ残量がなくなったときにメモリ内容を消失してしまうという問題がある。また、特許文献２の回路では、主電源または商用電源の電圧低下時に瞬時にバックアップ電源に切り替えるため、短期間の瞬時停電や外乱による停電検出回路の誤作動などのたびにバッテリから不要な電力が消費されてしまい、バッテリ電源の寿命が短縮されてしまうという問題がある。また、特許文献３の装置は予備の電源回路を備えるものではなく、停電が続いた場合はＣＰＵの内容を不揮発性メモリに書き込んで動作を停止してしまうため、待避できなかった揮発性メモリの内容が保証されないという問題がある。

[**0001**] The present invention relates to a memory backup circuit, in particular, a technique for reliably protect the contents of volatile memory during a power outage.

[**0002**] Conventionally, a sudden power outage, etc. For example, techniques have been proposed to protect the contents of volatile memory in electronic devices. Patent Document 1, for example, to detect outages and power output decrease of the main power has been disclosed power supply circuit has to supply only the memory that needs to retain what power backup power. In addition, Patent Document 2 drops instantly detects the output voltage of power supply to supply power to the CPU by using a spare power supply, and storage memory for storing process is performed in the course of various processes such as CPU calculator has been disclosed as the contents are retained. In addition, Patent Document 3, the write data into memory needed during the recovery power outages to interrupt a running program immediately when it detects a power failure, to continue the process and restart the program had been suspended if the recovery of a power failure then that, if followed by a power failure stopped the operation of the CPU, which discloses a circuit for recovering data that is held in memory during power recovery.

[**0003**] Open Patent Publication No. 2001-175364 Open Patent Publication No. 2003-67089 No. Hei 5-108503 Gazette

[**0004**] However, the circuit in Patent Document 1, there is a problem that you lose your memory when the battery is no longer the prolonged power outage. In addition, the circuit in Patent Document 2, to switch to backup power to instantly battery during a utility power or mains power is not needed from the battery each time, such as malfunction detection circuit for power failure or disturbance instantaneous power failure of short-term have lost its consumption, there is a problem that the life of the battery power is reduced. The apparatus of Patent Document 3 is not equipped with a spare power circuit, because if you followed a power failure shut down the operation by writing non-volatile memory the contents of the CPU, volatile memory could not be evacuated There is a problem that does not guarantee the content.

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[0005] 本発明は、直流電源回路の一次側電圧を第１の停電検出回路で監視してメモリバックアップする手段の他に、直流電源回路の二次側出力電圧を監視する第２の停電検出回路を設け、第１の停電検出回路が故障して停電検出ができない場合でも第２の停電検出回路で検出し、一定時間制御回路全体をバッテリにてバックアップすることにより、停電検出回路の単一故障によるバックアップ動作不良を回避し、バッテリの長寿命化を実現する回路を提供することを目的とする。

[0006] 上記目的を達成するために、本発明にかかるメモリバックアップ回路は、外部電力を入力し回路に必要な直流電圧を出力する直流電源回路と、前記外部電力の入力状態を監視する第１の停電検出回路と、前記直流電源回路の出力電圧を監視する第２の停電検出回路と、前記外部電力の消失時に揮発性メモリへ電力を供給するバックアップ電源と、前記第１または第２の停電検出手段から停電検出信号を受けた場合に前記揮発性メモリのバックアップ制御を実施するメモリ制御手段と、前記第２の停電検出手段のみが電圧低下を検出した場合に前記バックアップ電源の電力を所定期間前記メモリ制御手段へ供給するスイッチ手段を備えることを特徴とする。

[0007] このメモリバックアップ回路において、前記第２の停電検出回路が電圧低下を検出した場合に検出信号を所定期間だけ出力するタイマ回路を備えることを特徴とする。

[0008] 前記スイッチ手段は、前記第１の停電検出回路の停電検出信号がなく、且つ前記タイマ回路の検出信号がある場合に、前記バックアップ電源の電力を前記メモリ制御手段に供給するよう制御されることを特徴とする。

[0009] 前記メモリ制御手段は、前記第１または第２の停電検出手段から停電検出信号を受けた場合に、前記揮発性メモリの格納データを不揮発性メモリに待避させる処理を所定期間行い、その後前記揮発性メモリをセルフリフレッシュモードに移行させることを特徴とする。

[0010] 本発明にかかる電子機器は、上記のメモリバックアップ回路を具備することを特徴とする。

[**0005**] The invention, in addition to the means of memory backup power failure detection circuit monitors the voltage of the first primary of the DC power supply circuit, the secondary side of DC power supply circuit The second failure detection circuit is provided that monitors the output voltage detection circuit detects a power failure can not be detected even if the second blackout and power failure detection circuit of the first failure, the backup battery at a certain time the entire control circuit by to avoid a malfunction due to a single failure of backup power failure detection circuit, which aims to provide a circuit to achieve longer battery life.

[**0006**] To achieve the above object, memory backup circuit according to the present invention, a circuit that outputs a DC voltage DC power supply circuits necessary to enter a foreign power, said detection circuit and a power failure the first to monitor the input state of the external power detection circuit and a power outage in the second to monitor the output voltage of the DC power supply, wherein the backup power supply supplies power to volatile memory upon loss of power said external and control means for controlling the memory to perform a backup of said volatile memory when the power failure detection signal is received from the detection means the first or second power failure, the voltage drop is detected, only the second power failure detector and comprising switch means for supplying said memory control means to a predetermined time period if said backup power supply.

[**0007**] in the backup memory circuit, comprising a timer circuit and outputting a predetermined period detection signal when it detects a voltage drop of the second power failure detection circuit be.

[**0008**] said switch means, without the power failure detection signal of the first power failure detection circuit, if the detection signal and said timer circuit, said backup power supply and a control that is supplied to said memory control means.

[**0009**] The memory control unit, said if the power failure detection signal is received from the detection means first or second power failure, nonvolatile memory to said volatile memory for storing data processing is performed at a predetermined time period to retract, and a

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また、当該機器がディスクアレイ装置であることを特徴とする。

[0011] 外部入力電源の一次側電圧を監視する第１の停電検出回路と、メモリ手段およびメモリ制御手段への供給電力すなわち二次側電圧を監視する第２の停電検出手段とを設けることにより、第１の電圧検出回路が故障して停電検出が正常に行えない場合でも、電圧低下を検出して必要な対策を講じることが可能となる。また、この場合にバックアップ電源を所定期間メモリ制御回路に接続することにより、何らかの理由で外部電力の停電が検出されなかった場合でもバックアップ処理を行うことが可能となる。

[0012] また、第２の停電検出回路が電圧低下を検出したときに所定期間信号を出力するタイマ回路を設け、当該期間後にメモリ制御回路へのバックアップ電力の供給を停止することにより停電時のバックアップ電力の消耗を最小限に抑えることができる。

[0013] また、第１の停電検出回路の停電検出信号がなく、且つタイマ回路の検出信号がある場合に、バックアップ電源の電力をメモリ制御手段に供給するように制御することにより、第１の停電検出回路が正常に動作している場合はバックアップ電力の無駄な消費を抑えてバックアップ期間を長期化させることができる。

[0014] 上記の構成により第１または第２の停電検出回路で電圧低下が検出された場合に所定期間メモリ制御回路の動作が保証されるため、この期間内にメモリ制御回路が揮発性メモリの格納データを不揮発性メモリに待避させ、その後前記揮発性メモリをセルフリフレッシュモードに移行させることにより、メモリ内容を保護することができる。

[0015] このようなバックアップ回路はキャッシュメモリを用いる様々な電子機器に適用することができるが、特に上位装置との入出力データを多く格納し性能と信頼性の双方が求められるディスクアレイ装置に好適に用いることができる。

transition to self-refresh mode can be a volatile memory and then said.

[**0010**] electronic device according to the invention, characterized in that it comprises a memory backup circuit above. Further, characterized in that said device is a disk array.

[**0011**] and the first power failure detection circuit monitors the external input supply voltage of the primary, secondary voltage of the monitor, ie the power supplied to the memory control means and memory means By providing a second power failure detection means, be performed normally even if the power failure detection and failure of the first voltage detection circuit, it is possible to take the necessary measures to detect the voltage drops. In addition, by connecting to the memory control circuit backup power if the predetermined period, it becomes possible to perform the backup process even if no external power outages are detected for some reason.

[**0012**] also set a timer circuit that outputs a signal when a predetermined period detection circuit detects a voltage drop of the second power outage, backup power to the memory control circuit after a period can minimize power consumption by stopping the backup during power supply.

[**0013**] In addition, there is no power failure detection signal of the first power failure detection circuit, if there is a timer circuit and the detection signal is supplied to power memory backup power supply control means By controlling the way, if you have power failure detection circuitry is working properly first can prolong the period backup reduces backup power wasted.

[**0014**] To be guaranteed a certain period of operation of the memory control circuit when the voltage drop detection circuit detects a power failure by the first or second configuration described above, this period will be saved to nonvolatile memory for storing data in volatile memory in the memory control circuit, by making the transition to self-refresh mode, said volatile memory and then be able to protect the contents of memory.

[**0015**] such that the backup circuit can be applied to various electronic devices used for cache memory, performance and reliability of input data and to store more equipment, especially high can

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[0016] 本発明を実施するための最良の実施形態について、図面を参照しながら以下に詳細に説明する。図１は、本発明を実現する一実施例の構成を示すブロック図である。本発明は揮発性メモリに保証すべき内容が一時的に格納される電子機器全般に適用することができるが、本実施例ではディスクアレイ装置のメモリバックアップ回路として説明する。

[0017] 図１を参照すると、本実施例にかかるディスクアレイ装置のバックアップ回路は、商用交流電源１０からの交流電圧を所定の直流電圧に変換する直流電源回路２０と、当該電源回路２０内に設けられた一次側停電検出回路２２と、メモリ制御回路２４と、直流電源二次側出力をメモリ制御回路２４が必要とする所定の電圧に変換するメモリ制御回路用ＤＣＤＣコンバータ２６と、ＤＩＭＭ（Dual Inline Memory Module）等に代表される揮発性メモリ２８と、直流電源二次側出力を揮発性メモリ２８が必要とする所定の電圧に変換する揮発性メモリ用ＤＣＤＣコンバータ３０と、停電時バックアップ用の二次電池３２と、該二次電池３２を充電するための充電回路３４と、直流電源回路二次側出力電圧の低下をメモリ制御回路２４に通知する第２の停電検出回路４０と、二次電池３２の電力供給を制御する放電制御回路５０と、逆流防止ダイオード６２、６４、６６とを備えている。

[0018] 第２の停電検出回路４０は、上述した各ＤＣＤＣコンバータ２６，２８に供給される二次側出力電圧を監視する入力電圧監視回路４２と、この入力電圧監視回路が電圧不足を検出したとき、一定時間幅のパルスを出力するタイマ回路４４とを備えている。また、放電制御回路５０は、二次電池３２と直流電源回路二次側出力７０との間を閉路する半導体スイッチ５２と、逆流防止ダイオード５４と、タイマ回路４４の出力と一次側停電検出回路２１からの停電検出信号とを入力とし、一次側停電検出信号がなくタイマ回路の二次側停電検出信号があるときにスイッチ５２を短絡する２入力ＮＡＮＤ回路５６とを備えている。

[0019] 入力電圧監視回路４２は、例えば基準電圧発生源とコンパレータ等で構成される。また、タ

be suitably used for both the disk array may be required.

[**0016**] For the best embodiment for carrying out the invention will be described in detail below with reference to the drawings. Figure 1 is a block diagram showing the configuration of an embodiment of the present invention to achieve. The invention may be applied to general electronic equipment that is stored temporarily in volatile memory contents to be guaranteed, in this embodiment is described as a disk array device memory backup circuit.

[**0017**] Referring to Figure 1, the backup disk array circuit according to this embodiment, the DC power supply that converts AC voltage into a predetermined DC voltage from the commercial AC power supply 10 circuit 20, a primary power failure detection circuit 22 provided in said power supply circuit 20, memory control circuit 24, converted to a predetermined voltage to the memory control and memory control circuit 24 must have a secondary side output DC power supply DCDC converter circuit 26 and, DIMM (Dual Inline Memory Module) and a volatile memory 28 as represented by, for conversion into a volatile memory that requires a predetermined voltage to the volatile memory 28 on the secondary side output DC power supply DCDC converter with 30, 32 and a secondary battery for backup during power outages and the charging circuit 34 for charging said secondary battery 32, a first memory control circuit 24 notifies the output voltage drops below the DC power supply circuits 2 power failure detection circuit 40, and discharge control circuit 50 controls power to the secondary battery 32, and 62,64,66 and a backflow prevention diode.

[**0018**] 40 The second power failure detection circuit, a voltage monitoring circuit 42 monitors the secondary side output voltage DCDC converter is supplied to each of the above 26, 28, this when it detects an input under-voltage monitoring circuit, which includes a timer circuit 44 outputs a pulse of fixed duration. In addition, the control circuit 50 discharges, the switch 52 semiconductor cycles between 70 and secondary output circuit DC power supply 32 and a secondary battery, the diode 54 prevents reverse flow detection circuit 21 blackout primary output of the circuit 44 timer as input signal from the power failure detection, has a two-input NAND circuit 56 and switch 52 shorts out

イマ回路４４は、例えばワンショット回路を用いることができる。また、本実施例では半導体スイッチ５２としてＰチャンネルＭＯＳＦＥＴを使用しているが、これはバイポーラトランジスタや、電磁式リレー等を用いるようにしてもよい。さらに、放電制御回路５０を構成する２入力ＮＡＮＤ回路５６は、後述する所望の動作を得られるものであれば他の回路素子を用いて構成してもよい。

[0020] この回路の動作を、図２に示すタイムチャートを参照しながら説明する。商用交流電源１０が正常に入力されているとき、直流電源回路２０からの直流電圧はダイオード６２を経由してメモリ制御回路用ＤＣＤＣコンバータ２６に供給されるとともに、ダイオード６４を経由して揮発性メモリ用ＤＣＤＣコンバータ３０に供給され、メモリ制御回路２４および揮発性メモリ２８が駆動される。また、直流電源回路２０からの出力電圧は充電回路３４に供給され、二次電池３２が充電される。停電検出回路２２は直流電源回路２０に入力される商用交流電圧を監視しており、また、入力電圧監視回路４２は直流電源回路２０の二次側出力電圧を監視している。

[0021] まず、直流電源回路２０の停電検出回路２２が正常な場合の停電時の動作を説明する。停電検出回路２２は直流電源回路２０に入力される商用交流電圧を監視しており、ＡＣ入力電圧が規定レベル以下に低下し且つ一定時間経過した場合に（図２ａ）、第１の停電検出信号４３をローレベルに駆動して、Ｔ１時間後に停電することをメモリ制御回路２４に予告する（図２ｂ）。すなわち、一般に商用電源１０が停電してから直流電源回路２０の出力電圧がメモリ制御回路２４の動作電圧の下限まで低下するまでの時間が数１０ｍｓあるが、この時間からメモリ制御回路２４が後述するバックアップ動作を実施するのに必要な時間Ｔ１を残した段階で停電検出信号４３をローレベルに駆動する。このタイミングは装置の構成や消費電力等の実施環境に応じて予め適宜設定されているものとする。

[0022] メモリ制御回路２４は第１の停電検出信号４３を受けると、所定の手順で上位装置（図示せず）との入出力処理動作を停止するとともに、上

the power failure detection signal when there is a secondary side of the timer circuit has no primary power failure detection signal.

[**0019**] 42 voltage monitoring circuit is configured as a comparator with a reference voltage source and example. In addition, the timer circuit 44, a one-shot circuit can be used, for example. Also, in this embodiment is a P-channel MOSFET using a semiconductor switch 52, and this is a bipolar transistor, may be used such as electromagnetic relays. In addition, two-input NAND circuit 56 constituting a discharge control circuit 50 may be configured for as long as the other circuit elements to obtain the desired behavior described below.

[**0020**] an operation of this circuit will be described with reference to the time chart shown in Figure 2. When it is entered correctly and 10 commercial AC power supply DC voltage from the power supply circuit 20 DC is supplied to the DCDC converter 26 for the memory control circuit via a diode 62, the volatile memory via a diode 64 for DCDC converter 30 is supplied to, volatile memory 28 is driven and the memory control circuit 24. In addition, the output voltage from the DC power supply circuit 20 is supplied to the charging circuit 34, is charged secondary battery 32. Power failure detection circuit 22 which monitors the commercial AC voltage is input to a DC power supply circuit 20, and voltage monitoring circuit 42 which monitors the input voltage of the secondary side output DC power supply circuit 20.

[**0021**] First, when describing the operation during power failure detection circuit 22 is normal for the DC power supply circuit 20. Power failure detection circuit 22 which monitors the commercial AC voltage is input to a DC power supply circuit 20, and a period of time when the level drops below the specified input voltage AC (2a figure), the first power failure detection signal driven to a low level 43, you notice that the memory control circuit 24 hours after the blackout T1 (2b figure). In other words, there 10ms several time drops to lower the operating voltage of 24 memory control circuit output voltage of the circuit 20, the DC power supply from the lights of 10 commercial power, generally below 24 memory control circuit from this time driven low at power failure detection signal 43 leaving the T1 time required to perform the backup operation. This time shall have been appropriately set in advance according to the

記時間Ｔ１内に揮発性メモリ２４の格納データを所定の不揮発性メモリ（図示せず）に待避させ、待避できなかったデータは該メモリ内に格納したまま、揮発性メモリ２８を省電力モードに移行させて動作を停止する。この省電力モードは一般にセルフリフレッシュモードと呼ばれるものであり、内部のリフレッシュ・カウンタを用いて自動的にリフレッシュ動作を実行することにより、クロックを非活性にしてメモリの消費電力を低く抑える動作モードである。

[0023] これにより、一次側での停電検出回路２２が正常な場合には、図２（ｂ）に示す時間Ｔ１の開始時にメモリバックアップ処理が開始され、直流電源回路２０の出力電圧がメモリ制御回路２４の動作保証範囲内にある時間Ｔ１内にバックアップ処理が完了する。時間Ｔ１経過後に直流電源回路２０からの供給電圧が停止するためメモリ制御回路用ＤＣＤＣコンバータの入力電圧が消失し（図２ｇ）、メモリ制御回路２４は動作を停止するが、揮発性メモリ用ＤＣＤＣコンバータ３０には二次電池３２の電圧が供給されており（図２ｆ）、揮発性メモリ２８に残った内容は保護される。

[0024] 一方、停電時に一次側の停電検出回路２２が故障している場合や、商用交流電源１０が正常であっても直流電源回路２０の二次側出力７０が何らかの故障により出力低下または停止した場合には、停電検出回路２２から停電検出信号が出力されず（図２ｂに破線で示す状態）、メモリ制御回路２４は時間Ｔ１の開始時からバックアップ処理を開始することが適わない。この場合、数１０ｍｓ遅れて入力電圧監視回路４２が二次側電圧の低下を検出するが（図２ｃ）、これと同時にメモリ制御回路用ＤＣＤＣコンバータ２６への入力電圧も消失するためバックアップ処理を実施することができない。この場合にも二次電池３２の残量がある限り揮発性メモリ２８の内容は保護されるが、バッテリ残量がなくなればデータがすべて消失してしまう。そこで本発明では、この場合に二次電池３２の電力をメモリ制御回路用ＤＣＤＣコンバータ２６へ一定期間供給する構成を付加することにより、メモリ内容を不揮発性メモリに待避させて確実に保護するようにしている。

environment of implementing the device configuration and power consumption.

[**0022**] 24 receives the memory control circuit and power failure detection signal 43 the first step in a given host device (not shown) to stop the operation and output processing non-volatile memory for storing predetermined data in a time T1 volatile memory 24 (not shown) will be saved to the data could not be saved is stored in memory while said power to the volatile memory 28 To stop the operation will be moving to. This power saving mode is what is commonly referred to as self-refresh mode by automatically executing a refresh operation using the internal refresh counter, low power operating mode of the memory clock to be inactivated There.

[**0023**] This is normal when the power failure detection circuit 22 on the primary side of Figure 2 (b) the memory backup process starts at the beginning of time T1 shown in backup process is completed within the guaranteed operating time T1 in the range of the memory control circuit 24 output voltage DC power supply circuit 20. Lost input voltage of the DCDC converter for memory control circuit for stopping the voltage supply circuit 20 DC power supply after a time T1 (2g figure), 24 memory control circuit will stop working, DCDC converters for volatile The 30 and 32 is supplied to the secondary battery voltage (2f figure), what remained volatile memory 28 is protected.

[**0024**] On the other hand, has failed or if the primary power failure detection circuit 22 during a power outage, the secondary side of DC power supply circuit 20 even commercial AC power supply 10 is normally If output decreases or stops for any failure by the output 70 is not the power failure detection signal is output from the power failure detection circuit 22 (state shown by broken lines in Figure 2b), the backup memory control circuit 24 from the start time T1 no match to begin. In this case, to detect the secondary voltage drop in voltage monitoring circuit 42 the number of 10ms input lag (2c figure), is also not implemented the backup process for DCDC converter input voltage to the memory control circuit 26 simultaneously with can not be. The contents of volatile memory 28 as long as the remaining 32 secondary battery that can be protected in this case, all the data disappears when there are no battery. The present invention therefore, by adding

[0025] 入力電圧監視回路４２は、直流電源回路２０の二次側出力電圧が各ＤＣＤＣコンバータ２６，３０の動作保証範囲レベル以上かを常時監視しており、電圧が所定値まで低下したときに、後段のタイマ回路４４を駆動する（図２ｃおよびｄ）。これにより一定期間パルス信号が出力され（図２ｅ）、メモリ制御回路２４およびＮＡＮＤ回路５６に供給される。２入力ＮＡＮＤ回路５６は、第１の停電検出信号４４がハイレベルであって（図２ｂ）、且つタイマ回路４４の出力信号がハイレベルのとき（図２ｅ）、ローレベルの出力となり、一定期間ＦＥＴスイッチ５２をＯＮにする（図２ｆに破線で示す）。これにより、タイマ回路４４が第２の停電検出信号４５を出力している時間Ｔ２の間、二次電池３２とメモリ制御回路用ＤＣＤＣコンバータ２６とが接続され（図２ｈ）、メモリ制御回路２４がバックアップ動作可能となる。タイマ回路４４からの第２の停電検出信号４５はメモリ制御回路２４に供給され、これをトリガとしてメモリ制御回路２４は揮発性メモリ２８の内容を不揮発性メモリに待避させ、揮発性メモリ２８をセルフリフレッシュモードに切り替える。したがって、タイマ回路４４が第２の停電検出信号４５を出力する時間Ｔ２は、メモリ制御回路２４がバックアップ処理に必要な時間であることが望ましく、好ましくは時間Ｔ１と同じ長さである。

[0026] なお、第１の停電検出信号が正常に出力される場合には、図２のタイミングチャートにおいて実線で示すように動作し、上述した半導体スイッチ５２をＯＮさせずに省電力モードへ切り替わるため、停電のたびに二次電池３２から不要な電力が消費されるのを防止することができる。

[0027] 以上に詳細に説明したように、本発明によれば、直流電源回路の一次側電圧を監視する停電検出回路が故障して停電検出が正常に行えない場合でも、二次側出力電圧を監視して第２の停電検出信号を生成するとともに、揮発性メモリを省電力モードに移行させるまでの制御に必要な時間だけメモリ制御回路をバッテリ駆動するようにしたため、確実にメモリバックアップを行うことができる。また、直流電源回路の一次側は正常であっても、二次側出力回路が故障することにより出力

a configuration to provide a period of time to DCDC converter 26 for the memory control circuit power to 32 secondary battery in this case, to ensure protection will be saved to nonvolatile memory the memory contents that.

[**0025**] 42 Input voltage monitoring circuit, which constantly monitors the level of the guaranteed operating range greater than or equal 26,30 DCDC converter for each secondary output voltage of the DC power supply circuit 20 When the voltage drops to a predetermined value, the timer circuit 44 to drive the subsequent stage (d and Figure 2c). Pulse signal is output which period (2e figure), and NAND circuit 56 is supplied to the memory control circuit 24. 2-input NAND circuit 56 provides a high level of the first power failure detection signal 44 (2b figure), the high level output signal of the timer circuit 44 and (2e figure), the output becomes low, the period Turning ON the FET switch 52 (shown in broken lines in Figure 2f). Thus, during the time T2 that the output 45 signal failure detection of the second circuit 44, the timer is connected with the DCDC converter 26 for the memory control circuit 32 and rechargeable battery (2h figure), 24 memory control circuit back up and operational. 45 signal failure detection of a second from 44 to timer circuit is supplied to control circuit 24 memory 24 memory control circuit as a trigger, it will be saved to nonvolatile memory contents of the memory 28 a volatile, self-memory 28 volatile The refresh mode switch. Thus, T2 time failure detection signal output 45 of the second timer circuit 44, it is desirable that the time required to backup memory control circuit 24, preferably as long as the time T1.

[**0026**] Furthermore, if the power failure detection signal is output to the first successfully operates as a solid line in the timing chart shown in Figure 2, the above-mentioned semiconductor switch 52 Since switching to power saving mode without ON, it is possible to prevent unnecessary power is consumed whenever the secondary battery 32 to power outages.

[**0027**] As described in detail above, according to the invention, failure detection and failure to properly power failure detection circuit to monitor the primary voltage of the DC power supply circuit Even If you can, as well as to generate a signal failure detection of a second to monitor the output voltage of secondary side, the battery-powered control circuit memory as the time required to

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電圧が低下したような場合も同様に、本発明により確実にバックアップを行うことができる。さらに、一次側の停電検出回路が正常に動作している場合には、バッテリ電源をメモリ制御回路に供給することなくバックアップされる構成としたため、停電検出時に必ずバッテリ電源を制御回路に接続するような構成に比してバッテリの長寿命化を実現することができる。

[0028] 以上、本発明の実施例について詳細に説明したが、本発明の技術的範囲は上記実施例に何ら限定されるものではなく、請求項の記載の意図する範囲を超えない限りにおいて、他の様々な変形例として実現することができる。例えば、上記実施例ではタイマ回路４４にワンショット回路を用いる構成としているが、スイッチ５２を所定期間だけＯＮにする動作が得られれば他の構成を用いてもよい。また、上記実施例はディスクアレイ装置のメモリバックアップ回路として説明しているが、他のストレージシステムやコンピュータなど、装置あるいはＣＰＵの入出力処理にキャッシュメモリを用いるあらゆる電子機器に適用することができる。

control up to move into a power saving mode the volatile memory because, as can be reliably back to the memory. In addition, the primary side DC power supply circuit, even normal, as well as if the output voltage drops by the secondary output circuit failure, the backup can be performed reliably by the present invention. In addition, if operating properly circuit failure detection on the primary side, so that the configuration is backed up without having to be supplied to the memory control circuit the battery power to connect to a control circuit to battery power whenever the power failure detection it is possible to achieve longer battery life compared to the structure.

[**0028**] than has been described in detail an embodiment of the invention, the technical scope of the invention is not intended to be limited to the above embodiments described in claim exceed the intended scope of the extent, it is possible to achieve a variety of other modified examples. For example, in the above examples have been configured for a one-shot circuit and timer circuit 44, other configurations may be used to work If you get a predetermined time period is set to ON switch 52. In addition, the above examples have been described as the backup disk array device memory circuit, and computer storage systems and other electronic devices that can be applied to any use of cache memory or CPU to handle input and output devices.

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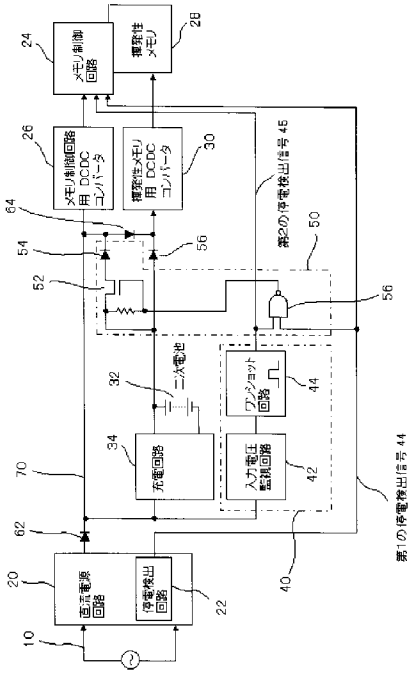
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(54)【発明の名称】メモリバックアップ回路およびこれを用いた電子機器

(57)【要約】

【課題】　停電検出回路の単一故障によるバックアップ動作不良を回避し、バッテリの長寿命化を実現する。
【解決手段】　例えばディスクアレイ装置のメモリバックアップ回路に、外部電力を入力し回路に必要な直流電圧を出力する直流電源回路と、前記外部電力の入力状態を監視する第１の停電検出回路と、前記直流電源回路の出力電圧を監視する第２の停電検出回路と、前記外部電力の消失時に揮発性メモリへ電力を供給するバックアップ電源と、前記第１または第２の停電検出手段から停電検出信号を受けた場合に前記揮発性メモリのバックアップ制御を実施するメモリ制御手段と、前記第２の停電検出手段のみが電圧低下を検出した場合に前記バックアップ電源の電力を所定期間前記メモリ制御手段へ供給するスイッチ手段とを設ける。
【選択図】　図１



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【特許請求の範囲】
【請求項１】
外部電力を入力し回路に必要な直流電圧を出力する直流電源回路と、前記外部電力の入力状態を監視する第１の停電検出回路と、前記直流電源回路の出力電圧を監視する第２の停電検出回路と、前記外部電力の消失時に揮発性メモリへ電力を供給するバックアップ電源と、前記第１または第２の停電検出手段から停電検出信号を受けた場合に前記揮発性メモリのバックアップ制御を実施するメモリ制御手段と、前記第２の停電検出手段のみが電圧低下を検出した場合に前記バックアップ電源の電力を所定期間前記メモリ制御手段へ供給するスイッチ手段を備えることを特徴とするメモリバックアップ回路。
【請求項２】
請求項１に記載のメモリバックアップ回路において、前記第２の停電検出回路が電圧低下を検出した場合に検出信号を所定期間だけ出力するタイマ回路を備えることを特徴とするメモリバックアップ回路。
【請求項３】
請求項２に記載のメモリバックアップ回路において、前記スイッチ手段は、前記第１の停電検出回路の停電検出信号がなく、且つ前記タイマ回路の検出信号がある場合に、前記バックアップ電源の電力を前記メモリ制御手段に供給するよう制御されることを特徴とするメモリバックアップ回路。
【請求項４】
請求項１乃至３のいずれかに記載のメモリバックアップ回路において、前記メモリ制御手段は、前記第１または第２の停電検出手段から停電検出信号を受けた場合に、前記揮発性メモリの格納データを不揮発性メモリに待避させる処理を所定期間行い、その後前記揮発性メモリをセルフリフレッシュモードに移行させることを特徴とするメモリバックアップ回路。
【請求項５】
請求項１乃至４のいずれかに記載のメモリバックアップ回路を具備することを特徴とする電子機器。
【請求項６】
請求項５に記載の電子機器であって、当該機器がディスクアレイ装置であることを特徴とする電子機器。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明はメモリバックアップ回路に関し、特に、停電時に揮発性メモリの内容を確実に保護する技術に関する。
【背景技術】
【０００２】
従来より、例えば不意の停電時等に、電子機器における揮発性メモリの内容を保護する技術が提案されている。例えば特許文献１には、主電源の出力低下や電源供給の停止を検知して、バックアップ電源の電力を内容保持の必要があるメモリのみに供給するようにした電源供給回路が開示されている。また、特許文献２には電源回路の出力電圧低下を瞬時に検知し、予備電源を用いてＣＰＵに電源を供給することにより、ＣＰＵで行われる各種処理等の経過や過程を記憶するメモリの記憶内容が保持されるようにした電卓が開示されている。また、特許文献３には、停電を検知すると直ちに実行中のプログラムを中断して停電回復時に必要なデータをメモリに書き込み、その後停電が回復すれば中断していたプログラムを再開し処理を続行するが、停電が続いた場合にはＣＰＵの動作を停止し、電力回復時にメモリに保持されているデータを復旧する回路が開示されている。
【０００３】
【特許文献１】特開２００１－１７５３６４号公報
【特許文献２】特開２００３－６７０８９号公報

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【特許文献３】特開平５－１０８５０３号公報
【発明の開示】
【発明が解決しようとする課題】
【０００４】
しかしながら、上記特許文献１の回路では、停電が長引いてバッテリ残量がなくなったときにメモリ内容を消失してしまうという問題がある。また、特許文献２の回路では、主電源または商用電源の電圧低下時に瞬時にバックアップ電源に切り替えるため、短期間の瞬時停電や外乱による停電検出回路の誤作動などのたびにバッテリから不要な電力が消費されてしまい、バッテリ電源の寿命が短縮されてしまうという問題がある。また、特許文献３の装置は予備の電源回路を備えるものではなく、停電が続いた場合はＣＰＵの内容を不揮発性メモリに書き込んで動作を停止してしまうため、待避できなかった揮発性メモリの内容が保証されないという問題がある。
【０００５】
本発明は、直流電源回路の一次側電圧を第１の停電検出回路で監視してメモリバックアップする手段の他に、直流電源回路の二次側出力電圧を監視する第２の停電検出回路を設け、第１の停電検出回路が故障して停電検出ができない場合でも第２の停電検出回路で検出し、一定時間制御回路全体をバッテリにてバックアップすることにより、停電検出回路の単一故障によるバックアップ動作不良を回避し、バッテリの長寿命化を実現する回路を提供することを目的とする。
【課題を解決するための手段】
【０００６】
上記目的を達成するために、本発明にかかるメモリバックアップ回路は、外部電力を入力し回路に必要な直流電圧を出力する直流電源回路と、前記外部電力の入力状態を監視する第１の停電検出回路と、前記直流電源回路の出力電圧を監視する第２の停電検出回路と、前記外部電力の消失時に揮発性メモリへ電力を供給するバックアップ電源と、前記第１または第２の停電検出手段から停電検出信号を受けた場合に前記揮発性メモリのバックアップ制御を実施するメモリ制御手段と、前記第２の停電検出手段のみが電圧低下を検出した場合に前記バックアップ電源の電力を所定期間前記メモリ制御手段へ供給するスイッチ手段を備えることを特徴とする。
【０００７】
このメモリバックアップ回路において、前記第２の停電検出回路が電圧低下を検出した場合に検出信号を所定期間だけ出力するタイマ回路を備えることを特徴とする。
【０００８】
前記スイッチ手段は、前記第１の停電検出回路の停電検出信号がなく、且つ前記タイマ回路の検出信号がある場合に、前記バックアップ電源の電力を前記メモリ制御手段に供給するよう制御されることを特徴とする。
【０００９】
前記メモリ制御手段は、前記第１または第２の停電検出手段から停電検出信号を受けた場合に、前記揮発性メモリの格納データを不揮発性メモリに待避させる処理を所定期間行い、その後前記揮発性メモリをセルフリフレッシュモードに移行させることを特徴とする。
【００１０】
本発明にかかる電子機器は、上記のメモリバックアップ回路を具備することを特徴とする。また、当該機器がディスクアレイ装置であることを特徴とする。
【発明の効果】
【００１１】
外部入力電源の一次側電圧を監視する第１の停電検出回路と、メモリ手段およびメモリ制御手段への供給電力すなわち二次側電圧を監視する第２の停電検出手段とを設けることにより、第１の電圧検出回路が故障して停電検出が正常に行えない場合でも、電圧低下を検出して必要な対策を講じることが可能となる。また、この場合にバックアップ電源を所

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定期間メモリ制御回路に接続することにより、何らかの理由で外部電力の停電が検出されなかった場合でもバックアップ処理を行うことが可能となる。

【００１２】

また、第２の停電検出回路が電圧低下を検出したときに所定期間信号を出力するタイマ回路を設け、当該期間後にメモリ制御回路へのバックアップ電力の供給を停止することにより停電時のバックアップ電力の消耗を最小限に抑えることができる。

【００１３】

また、第１の停電検出回路の停電検出信号がなく、且つタイマ回路の検出信号がある場合に、バックアップ電源の電力をメモリ制御手段に供給するように制御することにより、第１の停電検出回路が正常に動作している場合はバックアップ電力の無駄な消費を抑えてバックアップ期間を長期化させることができる。

【００１４】

上記の構成により第１または第２の停電検出回路で電圧低下が検出された場合に所定期間メモリ制御回路の動作が保証されるため、この期間内にメモリ制御回路が揮発性メモリの格納データを不揮発性メモリに待避させ、その後前記揮発性メモリをセルフリフレッシュモードに移行させることにより、メモリ内容を保護することができる。

【００１５】

このようなバックアップ回路はキャッシュメモリを用いる様々な電子機器に適用することができるが、特に上位装置との入出力データを多く格納し性能と信頼性の双方が求められるディスクアレイ装置に好適に用いることができる。

【発明を実施するための最良の形態】

【００１６】

本発明を実施するための最良の実施形態について、図面を参照しながら以下に詳細に説明する。図１は、本発明を実現する一実施例の構成を示すブロック図である。本発明は揮発性メモリに保証すべき内容が一時的に格納される電子機器全般に適用することができるが、本実施例ではディスクアレイ装置のメモリバックアップ回路として説明する。

【００１７】

図１を参照すると、本実施例にかかるディスクアレイ装置のバックアップ回路は、商用交流電源１０からの交流電圧を所定の直流電圧に変換する直流電源回路２０と、当該電源回路２０内に設けられた一次側停電検出回路２２と、メモリ制御回路２４と、直流電源二次側出力をメモリ制御回路２４が必要とする所定の電圧に変換するメモリ制御回路用ＤＣＤＣコンバータ２６と、ＤＩＭＭ（Dual Inline Memory Module）等に代表される揮発性メモリ２８と、直流電源二次側出力を揮発性メモリ２８が必要とする所定の電圧に変換する揮発性メモリ用ＤＣＤＣコンバータ３０と、停電時バックアップ用の二次電池３２と、該二次電池３２を充電するための充電回路３４と、直流電源回路二次側出力電圧の低下をメモリ制御回路２４に通知する第２の停電検出回路４０と、二次電池３２の電力供給を制御する放電制御回路５０と、逆流防止ダイオード６２、６４、６６とを備えている。

【００１８】

第２の停電検出回路４０は、上述した各ＤＣＤＣコンバータ２６，２８に供給される二次側出力電圧を監視する入力電圧監視回路４２と、この入力電圧監視回路が電圧不足を検出したとき、一定時間幅のパルスを出力するタイマ回路４４とを備えている。また、放電制御回路５０は、二次電池３２と直流電源回路二次側出力７０との間を閉路する半導体スイッチ５２と、逆流防止ダイオード５４と、タイマ回路４４の出力と一次側停電検出回路２１からの停電検出信号とを入力とし、一次側停電検出信号がなくタイマ回路の二次側停電検出信号があるときにスイッチ５２を短絡する２入力ＮＡＮＤ回路５６とを備えている。

【００１９】

入力電圧監視回路４２は、例えば基準電圧発生源とコンパレータ等で構成される。また、タイマ回路４４は、例えばワンショット回路を用いることができる。また、本実施例では半導体スイッチ５２としてＰチャンネルＭＯＳＦＥＴを使用しているが、これはバイポ

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ーラトランジスタや、電磁式リレー等を用いるようにしてもよい。さらに、放電制御回路５０を構成する２入力ＮＡＮＤ回路５６は、後述する所望の動作を得られるものであれば他の回路素子を用いて構成してもよい。

【００２０】

この回路の動作を、図２に示すタイムチャートを参照しながら説明する。商用交流電源１０が正常に入力されているとき、直流電源回路２０からの直流電圧はダイオード６２を経由してメモリ制御回路用ＤＣＤＣコンバータ２６に供給されるとともに、ダイオード６４を経由して揮発性メモリ用ＤＣＤＣコンバータ３０に供給され、メモリ制御回路２４および揮発性メモリ２８が駆動される。また、直流電源回路２０からの出力電圧は充電回路３４に供給され、二次電池３２が充電される。停電検出回路２２は直流電源回路２０に入力される商用交流電圧を監視しており、また、入力電圧監視回路４２は直流電源回路２０の二次側出力電圧を監視している。

【００２１】

まず、直流電源回路２０の停電検出回路２２が正常な場合の停電時の動作を説明する。停電検出回路２２は直流電源回路２０に入力される商用交流電圧を監視しており、ＡＣ入力電圧が規定レベル以下に低下し且つ一定時間経過した場合に（図２ａ）、第１の停電検出信号４３をローレベルに駆動して、Ｔ１時間後に停電することをメモリ制御回路２４に予告する（図２ｂ）。すなわち、一般に商用電源１０が停電してから直流電源回路２０の出力電圧がメモリ制御回路２４の動作電圧の下限まで低下するまでの時間が数１０ｍｓあるが、この時間からメモリ制御回路２４が後述するバックアップ動作を実施するのに必要な時間Ｔ１を残した段階で停電検出信号４３をローレベルに駆動する。このタイミングは装置の構成や消費電力等の実施環境に応じて予め適宜設定されているものとする。

【００２２】

メモリ制御回路２４は第１の停電検出信号４３を受けると、所定の手順で上位装置（図示せず）との入出力処理動作を停止するとともに、上記時間Ｔ１内に揮発性メモリ２４の格納データを所定の不揮発性メモリ（図示せず）に待避させ、待避できなかったデータは該メモリ内に格納したまま、揮発性メモリ２８を省電力モードに移行させて動作を停止する。この省電力モードは一般にセルフリフレッシュモードと呼ばれるものであり、内部のリフレッシュ・カウンタを用いて自動的にリフレッシュ動作を実行することにより、クロックを非活性にしてメモリの消費電力を低く抑える動作モードである。

【００２３】

これにより、一次側での停電検出回路２２が正常な場合には、図２（ｂ）に示す時間Ｔ１の開始時にメモリバックアップ処理が開始され、直流電源回路２０の出力電圧がメモリ制御回路２４の動作保証範囲内にある時間Ｔ１内にバックアップ処理が完了する。時間Ｔ１経過後に直流電源回路２０からの供給電圧が停止するためメモリ制御回路用ＤＣＤＣコンバータの入力電圧が消失し（図２ｇ）、メモリ制御回路２４は動作を停止するが、揮発性メモリ用ＤＣＤＣコンバータ３０には二次電池３２の電圧が供給されており（図２ｆ）、揮発性メモリ２８に残った内容は保護される。

【００２４】

一方、停電時に一次側の停電検出回路２２が故障している場合や、商用交流電源１０が正常であっても直流電源回路２０の二次側出力７０が何らかの故障により出力低下または停止した場合には、停電検出回路２２から停電検出信号が出力されず（図２ｂに破線で示す状態）、メモリ制御回路２４は時間Ｔ１の開始時からバックアップ処理を開始することが適わない。この場合、数１０ｍｓ遅れて入力電圧監視回路４２が二次側電圧の低下を検出するが（図２ｃ）、これと同時にメモリ制御回路用ＤＣＤＣコンバータ２６への入力電圧も消失するためバックアップ処理を実施することができない。この場合にも二次電池３２の残量がある限り揮発性メモリ２８の内容は保護されるが、バッテリ残量がなくなればデータがすべて消失してしまう。そこで本発明では、この場合に二次電池３２の電力をメモリ制御回路用ＤＣＤＣコンバータ２６へ一定期間供給する構成を付加することにより、メモリ内容を不揮発性メモリに待避させて確実に保護するようにしている。

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【００２５】
入力電圧監視回路４２は、直流電源回路２０の二次側出力電圧が各ＤＣＤＣコンバータ２６，３０の動作保証範囲レベル以上かを常時監視しており、電圧が所定値まで低下したときに、後段のタイマ回路４４を駆動する（図２ｃおよびｄ）。これにより一定期間パルス信号が出力され（図２ｅ）、メモリ制御回路２４およびＮＡＮＤ回路５６に供給される。２入力ＮＡＮＤ回路５６は、第１の停電検出信号４４がハイレベルであって（図２ｂ）、且つタイマ回路４４の出力信号がハイレベルのとき（図２ｅ）、ローレベルの出力となり、一定期間ＦＥＴスイッチ５２をＯＮにする（図２ｆに破線で示す）。これにより、タイマ回路４４が第２の停電検出信号４５を出力している時間Ｔ２の間、二次電池３２とメモリ制御回路用ＤＣＤＣコンバータ２６とが接続され（図２ｈ）、メモリ制御回路２４がバックアップ動作可能となる。タイマ回路４４からの第２の停電検出信号４５はメモリ制御回路２４に供給され、これをトリガとしてメモリ制御回路２４は揮発性メモリ２８の内容を不揮発性メモリに待避させ、揮発性メモリ２８をセルフリフレッシュモードに切り替える。したがって、タイマ回路４４が第２の停電検出信号４５を出力する時間Ｔ２は、メモリ制御回路２４がバックアップ処理に必要な時間であることが望ましく、好ましくは時間Ｔ１と同じ長さである。

【００２６】
なお、第１の停電検出信号が正常に出力される場合には、図２のタイミングチャートにおいて実線で示すように動作し、上述した半導体スイッチ５２をＯＮさせずに省電力モードへ切り替わるため、停電のたびに二次電池３２から不要な電力が消費されるのを防止することができる。

【００２７】
以上に詳細に説明したように、本発明によれば、直流電源回路の一次側電圧を監視する停電検出回路が故障して停電検出が正常に行えない場合でも、二次側出力電圧を監視して第２の停電検出信号を生成するとともに、揮発性メモリを省電力モードに移行させるまでの制御に必要な時間だけメモリ制御回路をバッテリ駆動するようにしたため、確実にメモリバックアップを行うことができる。また、直流電源回路の一次側は正常であっても、二次側出力回路が故障することにより出力電圧が低下したような場合も同様に、本発明により確実にバックアップを行うことができる。さらに、一次側の停電検出回路が正常に動作している場合には、バッテリ電源をメモリ制御回路に供給することなくバックアップされる構成としたため、停電検出時に必ずバッテリ電源を制御回路に接続するような構成に比してバッテリの長寿命化を実現することができる。

【００２８】
以上、本発明の実施例について詳細に説明したが、本発明の技術的範囲は上記実施例に何ら限定されるものではなく、請求項の記載の意図する範囲を超えない限りにおいて、他の様々な変形例として実現することができる。例えば、上記実施例ではタイマ回路４４にワンショット回路を用いる構成としているが、スイッチ５２を所定期間だけＯＮにする動作が得られれば他の構成を用いてもよい。また、上記実施例はディスクアレイ装置のメモリバックアップ回路として説明しているが、他のストレージシステムやコンピュータなど、装置あるいはＣＰＵの入出力処理にキャッシュメモリを用いるあらゆる電子機器に適用することができる。

【産業上の利用可能性】

【００２９】
本発明に係るメモリバックアップ回路は、不意の停電時などに確実に揮発性メモリの内容をバックアップするものであり、例えばディスクアレイ装置のキャッシュメモリのバックアップ回路として好適に用いることができる。

【図面の簡単な説明】

【００３０】
【図１】本発明にかかるメモリバックアップ回路の構成を示すブロック図である。
【図２】図１に示す回路の動作を説明するためのタイムチャートである。

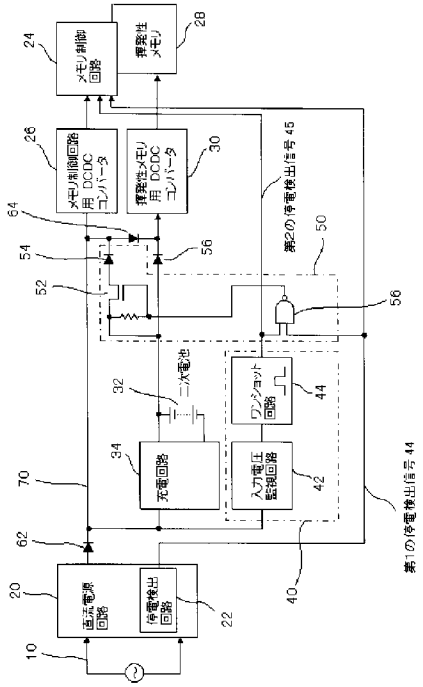
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【符号の説明】

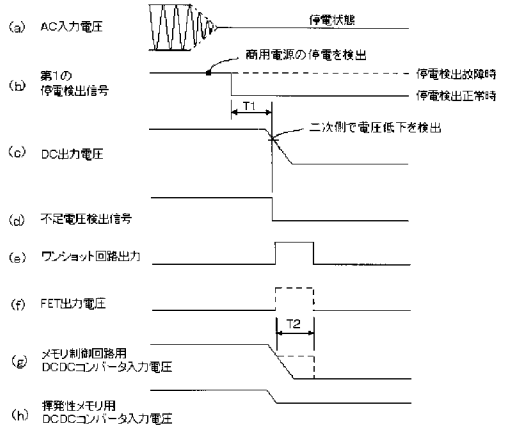
【００３１】

１０　　商用電源
２０　　直流電源回路
２２　　停電検出回路
２４　　メモリ制御回路
２６　　メモリ制御回路用ＤＣＤＣコンバータ
２８　　揮発性メモリ
３０　　揮発性メモリ用ＤＣＤＣコンバータ
３２　　二次電源
３４　　充電回路
４０　　第２の停電検出回路
４２　　入力電圧監視回路
４４　　タイマ回路
５０　　放電制御回路
５２　　半導体スイッチ
５４　　ダイオード
５６　　２入力ＮＡＮＤ回路
６２，６４，６６　ダイオード

【図１】



【図２】



フロントページの続き

(51)Int.Cl.	F I	テーマコード（参考）
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PTO/SB/08a (01-22)
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Application Number	17582797
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First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

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Examiner Name	FARROKH
Attorney Docket Number	022955-000090

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	ISL6537 "ACPI Regulator/Controller for Dual Channel DDR Memory Systems", Renesas, 16 pages, 07/18/2007, taken from internet on 16 April 2024 from: https://www.renesas.com/us/en/document/dst/isl6537-datasheet	☐
	2	ISL6532 "ACPI Regulator/Controller for Dual Channel DDR Memory Systems", Intersil, 16 pages, 07/2004, taken from internet on 17 April 2024 from: https://www.mouser.com/datasheet/2/465/intersil_fn9120-342258.pdf	☐
	3	NXP "Hardware and Layout Design Considerations for DDR Memory Interfaces", Freescale Semiconductor, Inc., 48 pages, 2007, taken from internet on 16 April 2024 from: https://www.nxp.com/docs/en/application-note/AN2582.pdf	☐
	4	TKDM "TKDM - A Reconfigurable Co-processor in a PC's Memory Slot", Plessi, 8 pages, 12/17/2003, taken from internet on 17 April 2024 from: https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=615235db2bed5bb4823f9c3a9d383a92e1f602c7	☐
	5	ISL6534 "Dual PWM with Linear", Renesas, 29 pages, 11/18/2005, taken from internet on 16 April 2024 from: https://dir.heisener.com/DatasheetDownload/ISL6534CV-TR5229.pdf	☐
	6	MAXIM "DC-DC Converter Tutorial", Maxim, 14 pages, 11/29/2001, taken from internet on 16 April 2024 from: https://pdfserv.maximintegrated.com/en/an/DCDC_Converter_Tutorial.pdf	☐
	7	TONG et al., "A System Level Implementation of Rijndael on a Memory-slot based FPGA Card", Tong, 8 pages, 01/2003, taken from internet on 06 June 2024 from: https://phwl.org/assets/papers/aes_fpt02.pdf	☐
	8	National Semiconductor (November 2006). LP3913 Power Management IC for Flash Memory Based Portable Media Players. Retrieved from https://datasheetspdf.com/pdf-file/572488/NationalSemiconductor/LP3913/1. See pages 1-3.	☐
	9	Intersil (December 2006). ISL6227 Dual Mobile-Friendly PWM Controller with DDR Option. Retrieved from http://pdfhtml.ic37.com/pdf_file_A/20200531/pdf_pdf/pdf5/INTERSIL/ISL6227_datasheet_647405/105904/ISL6227_datasheet.pdf. See pages 2, 10, 12, 14 & 20.	☐
	10	Xlinix (July 2005). OPB Synchronous DRAM (SDRAM) Controller (v1.00e). Retrieved from https://datasheet.datasheetarchive.com/originals/library/Datasheet-080/DASF007621.pdf. See pages 9 & 11.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17582797
	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2138
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	11	Phillips (2003). New multimarket products quarterly highlights. Retrieved from https://datasheet.datasheetarchive.com/originals/library/Datasheets-DAV2/DSADA0022280.pdf	☐
	12	Maxim (September 2005). Buck Converters Proliferate in Handhelds as Features and Processing Power Increase. Retrieved from https://datasheet.datasheetarchive.com/originals/library/Datasheet-081/DASF0031684.pdf	☐
	13	Keller, S. J. (2006). The Physical Design of the ILLIAC 6 Supercomputing Platform (Doctoral dissertation, University of Illinois at Urbana-Champaign). See pages 12, 13 & highlighted sections.	☐
	14	Interstill (2004). Power Management Application Guide for Altera FPGAs. Retrieved from https://www.datasheetarchive.com/pdf/download.php?id=c9facaf95737a8327c7217fbff086b497d4f48&type=P&term=buck%2520SDRAM. See pages 4 & 9.	☐
	15	Summit (2006). Application Note 59. Retrieved from https://www.datasheetarchive.com/pdf/download.php?id=a7ccb0edb0c2b62d33ea2ca63eeb31b0884da8&type=P&term=buck%2520SDRAM. See pages 1, 3 & 4.	☐
	16	National Semiconductor (2007). Application note AN-1608. Retrieved from https://www.datasheetarchive.com/pdf/download.php?id=c08bde6d6162bdd65a909e9aa5fbce116b8c2c&type=P&term=buck%2520SDRAM. See page 2.	☐
	17	Analog Devices (2006). TIgerSHARC Embedded Processor ADSP-TS201S.	☐
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	19	Texas Instruments (2001). Designing for Small-Size, High Frequency Applications Using TPS546xx DC/DC Converters.	☐
	20	Intersil (2002). Powering DDR Memory in Desktop Computers and Datacomm Systems. Retrieved from https://datasheet.datasheetarchive.com/originals/library/Datasheet-02/DSA0031945.pdf	☐
	21	Intel (2002). Mobile Intel® Pentium® 4 Processor-M and Intel® 845MP/845MZ Chipset Platform Design Guide.	☐

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	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	22	Asus (2001). A7V133 A7V133-C jumperfree PC133/VC133 200/266MHz FSB AGP Pro/4X Socket A Motherboard User's Manual.	☐
	23	Trescases, O. (2007). Integrated Power-Supplies for Portable Applications.	☐
	24	Van Schaik, C. F. (2002). The Development of a Node for a Hardware Reconfigurable Parallel Processor (Master's thesis, University of Cape Town).	☐
	25	Boroyevich, D. (2004). Power Electronics Building Blocks," Plug and Play", Hardware and Software Control Architectures. VIRGINIA POLYTECHNIC INST AND STATE UNIV BLACKSBURG OFFICE OF SPONSORED PROGRAMS.	☐
	26	McPartland, R. J., Loeper, D. J., Higgins, F. P., Singh, R., MacDonald, G., Komoriya, G., ... & Leung, C. W. (2000, May). SRAM Embedded Memory with Low Cost, FLASH EEPROM-Switch-Controlled Redundancy. In Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (Cat. No. 00CH37044) (pp. 287-289). IEEE.	☐
	27	Crisp, R. (1997). Direct Rambus Technology: The New Main Memory Standard. IEEE Micro, 17(6), 18-28. PC2–4200/ PC2–3200 DDR2	☐
	28	PC2–4200/PC2–3200 DDR2 Registered Mini-DIMM. (December 2006). Design Spec Rev. 2.0. Retrievable from https://www.jedec.org/standards-documents/docs/module-42014	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97(e) to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ A certification statement is not submitted herewith.

FEE

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

COPIES

☐ An identification of an earlier application pursuant to 37 CFR 1.98 (d) (1) is attached.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-09-24
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/582,797	Filing Date 01/24/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	10/01/2024							
	Total (37 CFR 1.16(i))	* 42	Minus	** 20	= 22		x $100 =	2200
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	2200

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT								
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/LAVINIA D JOHNSON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/582,797	**10/01/2024 02:15:28 PM Z ET**	**022955-000090**

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3546	FILED BY	LISA MARGARET ELLIOTT
PATENT CENTER #	67393003	FILING DATE	01/24/2022
CUSTOMER #	151145	FIRST NAMED INVENTOR	Chi-She Chen
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Khaled Shami

Documents

TOTAL DOCUMENTS: 9

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Supplemental IDS Letter.pdf	1	Miscellaneous Incoming Letter	142 KB
Supplemental IDS_IDS5_022955-000090.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	1355 KB
NPL--EX1018_Petition_IPR833_SKhynix.pdf	70	Non Patent Literature	428 KB
NPL--EX1014_Petition_IPR833_SanDisk.pdf	69	Non Patent Literature	1046 KB
NPL--EX2013_JEDEC_Standard_SDRAM_Unbuffered_SO-DIMM.pdf	26	Non Patent Literature	1891 KB

NPL--Paper25 - Sams Reply to POR - IPR2022-00996.pdf	57	Non Patent Literature	6338 KB
NPL--EX2031_Decl_MangioneSmith.pdf	144	Non Patent Literature	14332 KB
NPL--FBDIMM_Architecture-and-Protocol_JEDEC-Standard_JESD206-01_Jan2007.pdf	128	Non Patent Literature	15933 KB
Resp to 8-8-24 NFOA.pdf	45	Amendment/Request for Reconsideration-After Non-Final Rejection	972 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
Supplemental IDS Letter.pdf	86745618B5D3DBC3AF380EE5F02437D0DBD2C369B3A3A5D19849B8931CE5321C9AC0DC330B315667AE8288161B3CF72C1B513DCB1BB4926616373B1C69B22403
Supplemental IDS_IDS5_022955-000090.pdf	28402219937F2773E864697664AD08EA6A08B3727A48EE458900AA3023517A21DCA244BAC1C2BEF2195FE396FF3E96C52CAA9F5D8C7D4C2940568B1612F466D3
NPL--EX1018_Petition_IPR833_SKhynix.pdf	DB0997DBEE895EE773EC8DA276A188488AEA187171E25CADC3CC977073FCE0911D2C963CE783B3918CCDA4475BB0F9917212C74955C56E46222CF2C60C077CE4
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NPL--EX2013_JEDEC_Standard_SDRAM_Unbuffered_SO-DIMM.pdf	83914DDB9D7CF89B7E59C2BFE59D9DF732635C222FFB9748356408C74BD75D9EA415164BE54C028A6D9F797597D46DD8B3D27857D9C6E238A73C3CF6207AB670
NPL--Paper25 - Sams Reply to POR - IPR2022-00996.pdf	A8A5C782F5322FD90F7BD7AB2C8C1FD2CF8F09573D32611508E1D0678F532AC9CCFA51B22DBEE03BBF0D859F69EFA0163E196E6ECD13545E08B56B471486CD4E
NPL--EX2031_Decl_MangioneSmith.pdf	CFAE365C9A72938E273056177FB9F5BD715B930043EDAE0A0403EC7CB650B0C9A3F499F5A0995354AB61FFE5FB924D4BEFCBEEA2DE29D7B9AFF006C8EBDD4B49
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Standard_JESD206-01_Jan2007.pdf	A2DD7C6C9729DCD4237DC954828A7F2
Resp to 8-8-24 NFOA.pdf	42CF9F65180E3A4831BF38DA97FD6D332BF48A0D4B4E296C7DE1C2455CE3630FC86D32A9B352CDBA82BFDE9CB361641673F6314C2B9F026FDEFC1EF3CC8B8A27

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/582,797	**10/01/2024 02:15:28 PM Z ET**	**022955-000090**

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

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APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
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PATENT CENTER #	67393003	AUTHORIZED BY	Khaled Shami
CUSTOMER #	151145	FILING DATE	01/24/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Chi-She Chen

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
DA / 220585	**E202401E17107460**	**LISA MARGARET ELLIOTT**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	260.00	1	260.00
1202	EACH CLAIM IN EXCESS OF 20	100.00	22	2200.00
			TOTAL AMOUNT:	**$2,460.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc. CONFIRMATION NO.: 3546

SERIAL NO.: 17/582,797 ART UNIT: 2138

FILING DATE: January 24, 2022 EXAMINER: HASHEM FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Supplemental Information Disclosure Statement

Commissioner:

Applicant submits this Supplemental Information Disclosure Statement. The non-final Office Action issued on August 8, 2024, states that the Information Disclosure Statements submitted on May 28, 2024, have been considered by the examiner. However, some references in the Information Disclosure Statement filed on May 28, 2024, were crossed out in the List of References cited by applicant and considered by examiner issued on August 8, 2024. Therefore, the applicant re-submits those references in the Supplemental Information Disclosure Statement.

The appropriate fee for submitting an Information Disclosure Statement is also being submitted. The Commissioner is hereby authorized to charge any fees which may be required of this application, or credit any overpayment, to Deposit Account No. 22-0585.

Respectfully submitted,

Dated: October 1, 2024

/Khaled Shami/
Khaled Shami
Reg. No. 38745
Attorney for Applicant

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(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	Chi-She Chen
Art Unit	2138
Examiner Name	HASHEM FARROKH
Attorney Docket Number	022955-000090

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	1	Exhibit 2031, IPR 2022-00996, Declaration of Dr. William Henry Mangione-Smith regarding US Patent No. 11,016,918, 144 pages, executed on March 28, 2023.	☐
	2	Paper 25, IPR 2022-00996, Petitioner's Reply to Patent Owner's Response, filed June 20, 2023, 57 pages.	☐
	3	Exhibit 1014, Petition for Inter Partes Review of US Patent No. 8,301,833, filed June 20, 2014, 69 pages.	☐
	4	Exhibit 1018, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 13, 2017, 70 pages.	☐
	5	Exhibit 2013, JEDEC Standard No. 21-C, Page 4.20.3-1; PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, 26 pages. downloaded August 16, 2022.	☐
	6	FBDIMM: Architecture and Protocol, JEDEC Standard JESD206.01, January 2007, 128 pages.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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CERTIFICATION STATEMENT

Please see 37 CFR 1.97(e) to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ A certification statement is not submitted herewith.

FEE

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

COPIES

☐ An identification of an earlier application pursuant to 37 CFR 1.98 (d) (1) is attached.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-10-01
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc. CONF. NO: 3546

APPLICATION NO: 17/582,797 ART UNIT: 2138

FILING DATE: January 24, 2022 EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Commissioner:

In response to the non-final Office Action mailed August 8, 2024, Applicant submits the following Amendment and Remarks.

Listing of Claims begins on page **2.**

Remarks begin on page **22**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Currently amended) A dual in-line memory module (DIMM) configured to fit into a memory ~~slot connector~~socket of a system board of a ~~host~~ computer system, the memory ~~slot connector~~socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits, wherein system power from the ~~host~~ system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board, a 1-bit wide double data rate (DDR) data signal ~~signals~~ is electrically conducted between the ~~host~~ system board ~~system~~ and the DIMM ~~are transferred~~ via the memory socket by each data conduit of the set of data conduits, and address and control signals are electrically conducted from the ~~host~~ system board ~~are transferred~~ to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having a form factor with a width dimension and a height dimension, the PCB including:

an interface having edge connections disposed along the width dimension and configured to fit into the memory ~~slot connector of the host system~~socket, the edge connections including:

a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits,

a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and

a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits;

~~the PCB further including~~ a set of voltage supply lines electrically connected to

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the first set of edge connections, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board;

a set of data lines electrically ~~connected~~ coupled to respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; and

a set of address and control lines electrically ~~connected~~ coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

a controller ~~including a voltage monitor circuit and nonvolatile memory, the controller~~ coupled to the PCB and electrically connected to the ~~to an~~ input voltage supply line~~ of the set of voltage supply lines~~, the controller configured to receive the input voltage via the input voltage supply line, the controller including:

nonvolatile memory;

a data storage element configured to store a plurality of data bits;

a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element; and

a voltage monitor circuit electrically connected to the input voltage supply line and coupled to the logic element, the voltage monitor circuit configured to: ~~(i) monitor an~~ compare the input voltage ~~supplied via the input voltage supply line~~ to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage;~~,~~ and

~~(ii) generate a trigger signal upon detecting~~ detect a trigger condition;~~, and (iii) transmit the trigger signal to at least one other portion of the controller,~~

wherein ~~the controller is configured to perform~~, in response to the detected trigger condition~~signal~~, the logic element is configured to perform a plurality of write operations, including:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations;~~,~~

wherein, when the system power is provided to the DIMM from the system board:

~~and wherein~~ the trigger condition occurs when the input voltage goes above both ~~exceeds~~ the first and second ~~a first preset~~ threshold voltages~~voltage that is above an operating voltage of the DIMM~~; and

wherein:

a specified operating voltage value is within a range of operating voltage values of the DIMM,

the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value,

the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value,

the first threshold voltage corresponds to the lower operating voltage value, and

the second threshold voltage corresponds to the upper operating voltage value;

a set of components coupled to the PCB, the set of components including a plurality of ~~double data rate (~~DDR~~)~~ synchronous dynamic random access memory (DDR SDRAM) ~~devices~~packages coupled to the set of address and control lines and to the set of data lines, ~~the~~ each DDR SDRAM package of the plurality of DDR SDRAM packages~~devices~~ having a bit width of m bits and configured ~~being operable~~ to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines ~~based on control and~~ in response to

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Ex. 1002, p. 1125

address and control signals received ~~from the host system~~ via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and

first, second, third, and fourth converter circuits ~~buck converters~~ coupled to the PCB and to the input voltage supply line, ~~and~~ each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the system board, ~~from the input voltage supply line and~~ the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, ~~to deliver~~ from the power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages ~~to the set of components~~ via first, second, third, and fourth regulated voltage~~s~~ lines, respectively, ~~the first, second, third and fourth buck converters being further configured to generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and to output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively,~~ the set of components including:

a first component electrically connected to the first regulated voltage line and powered by ~~configured to receive power via at least~~ the first regulated voltage ~~line~~ when the system power is provided to the DIMM from the system board; ~~,~~

a second component electrically connected to the second regulated voltage line and powered by ~~configured to receive power via at least~~ the second regulated voltage ~~line~~ when the system power is provided to the DIMM from the system board; ~~,~~

a third component electrically connected to the third regulated voltage line and powered by ~~configured to receive power via at least~~ the third regulated voltage ~~line~~ when the system power is provided to the DIMM from the system board; ~~,~~ and

a fourth component electrically connected to the fourth regulated voltage line and powered by ~~configured to receive power via at least~~ the fourth regulated voltage ~~line~~ when the system power is provided to the DIMM from the system board; ~~,~~

wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit; and

wherein each component of the set of components:

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Ex. 1002, p. 1126

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage ~~voltages~~ lines;~~,~~ and

(ii)~~receives power~~ when the system power is provided to the DIMM from the system board, is powered:

- only by one or more of the first, second, third, and fourth converter circuits; and
- only via the one or more of the first, second, third, and fourth regulated voltage lines;~~, and~~

~~wherein the DIMM is configurable to operate in any of a plurality of states including a first state and a second state, wherein the controller is further configured to control power delivery to one or more components of the set of components for the DIMM to operate in the first state or the second state, whereby power to the set of components via the first, second, third, and fourth regulated voltage lines is turned on when the DIMM is operating in the first state, and whereby power to the first component via the first regulated voltage line is turned off and power to the second, third, and fourth components via the second, third and fourth regulated voltage lines is turned on when the DIMM is operating in the second state.~~

wherein the plurality of DDR SDRAM packages includes:

a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

when the system power is provided to the DIMM from the system board:

- the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR

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Ex. 1002, p. 1127

SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and

- the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.

3 – 27. (Canceled)

28. (New) The DIMM of claim 2, wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when the system power is provided to the DIMM from the system board.

29. (New) The DIMM of claim 2, wherein the data storage element is a buffer configured to store the plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.

30. (New) The DIMM of claim 2, wherein the width dimension is 133.35 millimeters.

31. (New) The DIMM of claim 30, wherein the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.

32. (New) The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations.

33. (New) The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on groups of

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Ex. 1002, p. 1128

data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.

34. (New) The DIMM of claim 2, wherein, when the system power is provided to the DIMM from the system board, the nonvolatile memory is not powered using the first regulated voltage.

35. (New) The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

36. (New) The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

37. (New) The DIMM of claim 35, wherein, prior to performing the third write operation, the logic element is further configured to perform (i) a first read operation of the plurality of read operations to read the first set of data bits from the first portion of the data storage element, and (ii) a second read operation of the plurality of read operations to read the second set of data bits from the second portion of the data storage element, and to generate the third set of data bits based on the read first and second sets of data bits.

38. (New) The DIMM of claim 2, wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, one or more read operations.

39. (New) The DIMM of claim 38, wherein the logic element is further configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM packages, respectively.

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Ex. 1002, p. 1129

40. (New) The DIMM of claim 38, wherein the logic element is further configured to perform (i) first and second read operations of the one or more read operations, and (ii) subsequently, the first and second write operations.

41. (New) The DIMM of claim 2, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

42. (New) The DIMM of claim 2, wherein, in response to the detected trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.

43. (New) The DIMM of claim 2, wherein, when the system power is provided to the DIMM from the system board, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.

44. (New) A dual in-line memory module (DIMM) configured to fit into a memory socket of a system board of a computer system, the memory socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits, wherein system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board, a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having a form factor with a width dimension and a height dimension, the PCB including:

an interface having edge connections disposed along the width dimension and configured to fit into the memory socket, the edge connections including:

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Ex. 1002, p. 1130

a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits,

a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and

a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits;

a set of voltage supply lines electrically connected to the first set of edge connections, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board;

a set of data lines electrically coupled to respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; and

a set of address and control lines electrically coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

a controller coupled to the PCB and electrically connected to the input voltage supply line, the controller configured to receive the system power and the input voltage via the input voltage supply line, the controller including:

nonvolatile memory;

a data storage element configured to store a plurality of data bits; and

a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element; and

a voltage monitor circuit electrically connected to the input voltage supply line and coupled to the logic element, the voltage monitor circuit configured to:

compare the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage; and

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Ex. 1002, p. 1131

detect a trigger condition;

wherein, in response to the detected trigger condition, the logic element is configured to periodically perform at regular intervals of time a plurality of write operations, including:

a first write operation to write a first set of data bits into a first portion of the data storage element; and

a second write operation to write a second set of data bits into a second portion of the data storage element;

wherein, when the system power is provided to the DIMM from the system board:

- the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and

wherein:

- a specified operating voltage value is within a range of operating voltage values of the DIMM,
- the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value,
- the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value,
- the first threshold voltage corresponds to the lower operating voltage value, and
- the second threshold voltage corresponds to the upper operating voltage value;

a set of components coupled to the PCB, the set of components including a plurality of DDR synchronous dynamic random access memory (DDR SDRAM) packages coupled to the set of address and control lines and to the set of data lines, each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and configured to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines in response to address and control signals received via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and

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Ex. 1002, p. 1132

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the system board, the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltages lines, respectively, the set of components including:

a first component electrically connected to the first regulated voltage line and powered by the first regulated voltage when the system power is provided to the DIMM from the system board;

a second component electrically connected to the second regulated voltage line and powered by the second regulated voltage when the system power is provided to the DIMM from the system board;

a third component electrically connected to the third regulated voltage line and powered by the third regulated voltage when the system power is provided to the DIMM from the system board; and

a fourth component electrically connected to the fourth regulated voltage line and powered by the fourth regulated voltage when the system power is provided to the DIMM from the system board;

wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit; and

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) when the system power is provided to the DIMM from the system board, is powered:

- only by one or more of the first, second, third, and fourth converter circuits; and
- only via the one or more of the first, second, third, and fourth

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Ex. 1002, p. 1133

regulated voltage lines;

wherein the plurality of DDR SDRAM packages includes:

a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

when the system power is provided to the DIMM from the system board:

- the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.

45. (New) The DIMM of claim 44, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations; and wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform at regular intervals of time all of the first and second write operations followed by the third write operation.

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46. (New) The DIMM of claim 45, wherein, the logic element is further configured to perform the third write operation by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

47. (New) The DIMM of claim 45, wherein, prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on groups of data bits stored in the data storage element.

48. (New) The DIMM of claim 44, wherein, when the system power is provided to the DIMM from the system board, the nonvolatile memory is not powered using the first regulated voltage.

49. (New) The DIMM of claim 44, wherein, in response to the detected trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.

50. (New) The DIMM of claim 46, wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

51. (New) The DIMM of claim 44, wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM packages, respectively.

52. (New) The DIMM of claim 44, wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time a plurality of read operations.

53. (New) The DIMM of claim 46, wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition,

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periodically at regular intervals of time one or more read operations to read data bits from the data storage element and to generate the third set of data bits based on the read data bits.

54. (New) The DIMM of claim 44, wherein the width dimension is 133.35 millimeters.

55. (New) The DIMM of claim 54, wherein the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.

56. (New) The DIMM of claim 45, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

57. (New) The DIMM of claim 44, wherein, when the system power is provided to the DIMM from the system board, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.

58. (New) A dual in-line memory module (DIMM) configured to fit into a memory socket of a system board of a computer system, the memory socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits, wherein system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board, a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having a form factor with a width dimension and a height dimension, the PCB including:

an interface having edge connections disposed along the width dimension and

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configured to fit into the memory socket, the edge connections including:

a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits,

a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and

a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits;

a set of voltage supply lines electrically connected to the first set of edge connections, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board;

a set of data lines electrically coupled to respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; and

a set of address and control lines electrically coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

a controller coupled to the PCB and electrically connected to the input voltage supply line, the controller configured to receive the input voltage via the input voltage supply line, the controller including:

nonvolatile memory;

a data storage element configured to store a plurality of data bits; and

a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element;

a voltage monitor circuit electrically connected to the input voltage supply line and coupled to the logic element, the voltage monitor circuit configured to:

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compare the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage; and

detect a trigger condition;

wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond a plurality of write operations, including:

a first write operation to write a first set of data bits into a first portion of the data storage element; and

a second write operation to write a second set of data bits into a second portion of the data storage element;

wherein, when the system power is provided to the DIMM from the system board:

- the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and

wherein:

- a specified operating voltage value is within a range of operating voltage values of the DIMM,
- the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value,
- the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value,
- the first threshold voltage corresponds to the lower operating voltage value, and
- the second threshold voltage corresponds to the upper operating voltage value;

a set of components coupled to the PCB, the set of components including a plurality of DDR synchronous dynamic random access memory (DDR SDRAM) packages coupled to the set of address and control lines and to the set of data lines, each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and configured to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines in

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response to address and control signals received via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and

first, second, third, and fourth voltage reducing circuits coupled to the PCB and to the input voltage supply line, each of the first, second, third, and fourth voltage reducing circuits configured to, in response to the detected trigger condition, receive power from the controller when the system power is provided to the DIMM from the system board, the first, second, third, and fourth voltage reducing circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the system power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltages lines, respectively, the set of components including:

a first component electrically connected to the first regulated voltage line and powered by the first regulated voltage when the system power is provided to the DIMM from the system board;

a second component electrically connected to the second regulated voltage line and powered by the second regulated voltage when the system power is provided to the DIMM from the system board;

a third component electrically connected to the third regulated voltage line and powered by the third regulated voltage when the system power is provided to the DIMM from the system board; and

a fourth component electrically connected to the fourth regulated voltage line and powered by the fourth regulated voltage when the system power is provided to the DIMM from the system board;

and

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) when the system power is provided to the DIMM from the system board, is powered:

- only by one or more of the first, second, third, and fourth voltage reducing circuits; and

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- only via the one or more of the first, second, third, and fourth regulated voltage lines;

wherein the plurality of DDR SDRAM packages includes:

a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

when the system power is provided to the DIMM from the system board:

- the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.

59. (New) The DIMM of claim 56, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations; and wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond all of the first and second write operations followed by

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the third write operation.

60. (New) The DIMM of claim 57, wherein the logic element is further configured to perform the third write operation by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

61. (New) The DIMM of claim 56, wherein, in response to the detected trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.

62. (New) The DIMM of claim 56, wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond a plurality of read operations prior to performing the first and second write operations.

63. (New) The DIMM of claim 60, wherein the logic element is further configured to perform a first and second read operations of the plurality of read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM packages, respectively.

64. (New) The DIMM of claim 56, wherein the width dimension is 133.35 millimeters.

65. (New) The DIMM of claim 62, wherein the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.

66. (New) The DIMM of claim 56, wherein each of the first, second, and third voltage reducing circuits is a buck converter.

67. (New) The DIMM of claim 56, wherein, when the system power is provided to the DIMM from the system board, the nonvolatile memory is not powered using the first regulated voltage.

68. (New) The DIMM of claim 58, wherein, when the system power is provided to the DIMM from the system board, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and

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wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.

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REMARKS

By this Proposed Amendment, submitted for purposes of discussion only, Applicant has **amended claim 2**; **canceled claims 6-8 and 11 and 14-27**; and **added new claims 28-68**. (Claims 3-5, 9-10, and 12-13 were previously canceled).

Claims 2 and 28-68 are now pending.

Amendment to Claims

Claim 2, has been amended for improved clarity in particularly pointing out and distinctly claiming certain aspects of the invention. No amendment made is related to the statutory requirements of patentability unless expressly stated herein. No amendment is made for the purpose of narrowing the scope of any claim, unless Applicant argues herein that such amendment is made to distinguish over a particular identified reference or combination of references.

For the examiner's convenience, claim 2 is reproduced hereinbelow in clean version for ease of reading:

2. (Currently amended) A dual in-line memory module (DIMM) configured to fit into a memory socket of a system board of a computer system, the memory socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits, wherein system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board, a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:

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a printed circuit board (PCB) having a form factor with a width dimension and a height dimension, the PCB including:

an interface having edge connections disposed along the width dimension and configured to fit into the memory socket, the edge connections including:

a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits,

a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and

a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits;

a set of voltage supply lines electrically connected to the first set of edge connections, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board;

a set of data lines electrically coupled to respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; and

a set of address and control lines electrically coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

a controller coupled to the PCB and electrically connected to the input voltage supply line, the controller configured to receive the input voltage via the input voltage supply line, the controller including:

nonvolatile memory;

a data storage element configured to store a plurality of data bits;

a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element; and

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a voltage monitor circuit electrically connected to the input voltage supply line and coupled to the logic element, the voltage monitor circuit configured to:

compare the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage; and

detect a trigger condition;

wherein, in response to the detected trigger condition, the logic element is configured to perform a plurality of write operations, including:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations;

wherein, when the system power is provided to the DIMM from the system board:

the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and

wherein:

a specified operating voltage value is within a range of operating voltage values of the DIMM,

the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value,

the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value,

the first threshold voltage corresponds to the lower operating voltage value, and

the second threshold voltage corresponds to the upper operating voltage value;

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a set of components coupled to the PCB, the set of components including a plurality of DDR synchronous dynamic random access memory (DDR SDRAM) packages coupled to the set of address and control lines and to the set of data lines, each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and configured to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines in response to address and control signals received via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the system board, the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltage lines, respectively, the set of components including:

a first component electrically connected to the first regulated voltage line and powered by the first regulated voltage when the system power is provided to the DIMM from the system board;

a second component electrically connected to the second regulated voltage line and powered by the second regulated voltage when the system power is provided to the DIMM from the system board;

a third component electrically connected to the third regulated voltage line and powered by the third regulated voltage when the system power is provided to the DIMM from the system board; and

a fourth component electrically connected to the fourth regulated voltage line and powered by the fourth regulated voltage when the system power is provided to the DIMM from the system board;

wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit; and

wherein each component of the set of components:

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(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) when the system power is provided to the DIMM from the system board, is powered:

- only by one or more of the first, second, third, and fourth converter circuits; and
- only via the one or more of the first, second, third, and fourth regulated voltage lines;

wherein the plurality of DDR SDRAM packages includes:

a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

when the system power is provided to the DIMM from the system board:

- the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory

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socket, and the total number of data conduits is at least 72 data conduits.

Canceled Claims

Claims 6-8 and 11 and 14-27 have been canceled without prejudice or disclaimer of the subject matter contained therein.

Newly-Added Claims

Claims 28-68 have been added to further particularly point out and distinctly claim certain aspects of the invention.

Examiner Interview

Applicants gratefully acknowledge Examiner Farrokh's courtesy and consideration during the telephonic Examiner Interview of September 6, 2024 with the Applicants' undersigned representative and Mr. Marwan Fawal, technology expert. The arguments below were raised with the Examiner but no agreement was reached.

Rejection(s) Under 35 U.S.C. § 103(a)

Claims 2, 6-8, 11, 15-18, and 20-24 stand rejected under pre-AIA 35 US.C. 103(a) as allegedly being unpatentable over Harris et al. "Harris" (US 2006/0174140 A1) in view of FBDIMM Standards (Exhibitions 1027, 2028 provided by Applicant) and Amidi et al. "Amidi" (US 7,724,604 B2).

Claims 14, 18, 19, and 25 rejected under pre-AIA 35 U.S.C. 103(a) as allegedly being unpatentable over Harris, FBDIMM Standards, and Amidi as applied to claims 6, 18, and 24, and further in view of Levkovitz et al. "Levkovitz" (US 2007/0088838 A1).

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The Examiner asserts that the rejection is based on information provided in Trial Termination or Final Written Decision (hereinafter Trial-T[er]m (*sic*), dated 12/06/2023) by the USPTO Trial and Appeal Board on Application 17/138,766 (now US patent 11,016,918 B2), which appears, in most part, to be based on Exhibition 1001, IPR 2022-00996. The Examiner alleges that the "instant Application, which is a continuation of US Patent 11,016,918 B2 includes substantially the same or similar claim limitations." (Office Action, p. 4, ll. 4-9).

In the Office Action, the Examiner also states that he "considers the claims of Application 17/582, 797, that substantially include limitations similar to claims of Applications 17/138, 766 and 17/328, 019, not to be patentable. Therefore, the Examiner as shown below rejected the claims." (*Id.*, p. 3, ll. 6-9).

Support for all of the below amendments has been provided in the attachment accompanying this paper. The support is provided by claim number in a table within the attachment.

To advance the prosecution of this application, the Applicant has canceled claims 6-8, 11, 15-18, and 20-24 without prejudice or disclaimer; amended claim 2; and added new claims 28-68. Applicant acknowledges the Trial-Term cited by the Examiner in the Office Action mailed August 8, 2024, but maintains that the rejected claims 2, 6-8, 11, 15-18, and 20-24 (that is, prior to the instant amendment) contain limitations that are novel and unobvious over the references cited in Trial-Term and by the Examiner.

In fact, the Applicant will establish below that specific claim limitations included in the rejected claim 2, both before and after the instant amendment, describe a module that is structurally and operationally patentably distinguishable over the applied references. For instance, the limitations before the instant amendment (pre-amendment limitations) require that the four buck converters generate regulated voltages from the system power received through the input voltage supply line that is connected to a first set of edge connections that are connected to the set of power conduits of the memory socket, and that the power from the host system is provided to the DIMM via the set of power conduits of the memory socket. Harris expressly

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teaches against providing power from the system board or from the main board voltage sources to any memory module, as will be discussed further below.

In relevant part, pre-amendment claim 2 recites:

> "**A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system**, the **memory slot connector including a set of power conduits**, a set of data conduits, and a set of address and control conduits, **wherein power from the host system is provided to the DIMM via the set of power conduits," … "**a printed circuit board (**PCB) having edge connections configured to fit into the memory slot connector** of the host system, the edge connections including **a first set of edge connections configured to be electrically connected to the set of power conduits**," … "the PCB further including **a set of voltage supply lines electrically connected to the first set of edge connections**, ," … "the controller coupled to the PCB and to **an input voltage supply line of the set of voltage supply lines**" … "**first, second, third and fourth buck converters** coupled to the PCB and to the input voltage supply line and **configured to receive power from the input voltage supply line and to deliver power to the set of components** via first, second, third and fourth regulated voltages lines, the first, second, third and fourth buck converters being further **configured to generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line**, and to output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines,…**.** (Emphasis added).

As instantly amended, claim 2 recites:

> A dual in-line memory module (DIMM) configured to fit into a memory socket of a system board of a computer system, the **memory socket including a set of power conduits**" … , **wherein system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board**," … "PCB including…**a first set of edge connections** configured to be **electrically connected to respective power conduits of the set of power conduits**," … "**a set of voltage supply lines electrically connected to the first set of edge connections**, the set of voltage supply lines including **an**

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> **input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board**" … "first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, **each of the first, second, third, and fourth converter circuits configured to**, in response to the detected trigger condition, **receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the system board**, the first, second, third, and fourth converter circuits **configured to (i) generate** first, second, third, and fourth **regulated voltages**, respectively, **from the power supplied by the input voltage supply line**, … . (Emphasis added).

It can be seen that claim 2 as instantly amended still require that the system power is received by the DIMM from the memory socket of a system board of a computer system in a particular form (i.e., via the input voltage supply) and on particular pins of the memory socket (i.e. first set of edge connection electrically connected to respective power conduits of the set of power conduits of the memory socket), and that the converter circuits generates the regulated voltages from the power supplied to the DIMM from the system board via the set of power conduits of the memory socket.

As the Office Action acknowledges, the memory module 100A of Harris receives its power through an external source. ("Fig. 1B Harris shows a block diagram of memory module 100B comprising DRAM devices 110, inputs a plurality voltages 120 from **e[x]ternal** (sic) source and generates a plurality of regulated voltages 106 and 108," Office Action, p. 5, ll. 3-5, emphasis added).

Applicant respectfully maintains that Harris expressly teaches away from providing power to any memory module assembly via the memory socket from the system board of the computer system.

First, Harris recognized and described, at ¶0002, significant power supply concerns particularly in advanced memory designs, implemented at the time, that "**industry standard memory modules, e.g., Dual In-line Memory Modules (DIMMS)** populated with … (DRAM) devices, **are provided with power supply rails (on a relatively large number of pins) that are**

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powered from system board or main board voltage sources, and are specific to the memory technology." (Emphasis added).

Second, Harris recognized and described, at ¶0002, that "[a]s the performance of the DRAM technology goes up, and timing margin shrink, **it is becoming increasingly more difficult for the system board sources to provide tightly regulated power for the DRAM** cores as well as input/output (I/O) interface buffers." (Emphasis added).

Third, Harris concludes, at ¶0002, and states that **"[o]ne skilled in the art will recognize … that these issues are particularly significant for [computer] systems** that are deployed in infrastructures" **because "it is difficult to mix memory technology on a system board or provide upgrades to next generation DRAM technology in a cost-effective manner**." (Emphasis added).

In summary, Harris has recognized and teaches that (i) particularly significant power supply concerns exist for computer systems using industry standard DIMMS that are powered from the system board or the main board voltage sources, (ii) it is more difficult to provide tightly regulated power for the DRAM from the system board power sources via large number of pins of standard DIMM memory socket, and (iii) any one skilled in the art will recognize these particularly significant issues because when power is provided to the DIMMs from the system board, then it is difficult to mix DIMMs with different memory technology on such system board or being able to provide upgrades to next generation DRAM in a cost-effective manner.

In ¶0003, Harris described his invention as "**a voltage distribution system for a memory board assembly**, comprising means for **supplying a voltage to the memory board assembly from an external source**".

In the context of ¶¶ 0002-0003, Harris has identified particularly significant problems associated with advanced memory designs using standard DIMMs that are powered from the system board and teaches that his innovative solution to these significant problems is by supplying power to the DIMM from an external voltage source and locally converting the external voltage by an on-board voltage regulator.

Thus, Harris' external voltage source would not be understood by a skilled person in the art to be supplied to the standard interface DIMM from the system board, and Harris' description

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offers further detailed evidence that underscores this understanding.

Harris teaches several recognized advantages, in ¶0011, specifically for large memory capacity scaling, hot-pluggability, and DRAM technology independence:

> [0011] … Since the Vdd and Vcc power supply rails are rendered independent from external voltage sources, the overall power supply interface to the memory module 100A is improved to better support **large memory capacity scaling, hot-pluggability, DRAM technology independence (e.g., DDR2, DDR3, DDR4, and other DRAM types)**, . . . as well as provide improved system-level cost sharing. Additionally, memory performance is also improved because of tighter voltage regulation.

This passage ¶ 0011, makes clear that the DIMM of Harris draws power from a source external to the system board, i.e. "external voltage sources," as does a reference to "hot-pluggability" especially in light of DRAM technology independence. Each DDR generation standardizes a different set of voltages for memory modules, and all DDR4, DDR3, DDR2, and DDR system boards provide system power exclusively to the DIMM via the socket. Thus, the ONLY way to have hot pluggability and DRAM technology independence as sought by Harris is to have power from a source external to the system board.

This power source external to the system board is further confirmed to be received by the module on external source path 104, in ¶ 0010 of Harris, and illustrated in Fig. 1A and Fig. 1B:

> [0010] In accordance with the teachings of the present patent disclosure, at least one on-board voltage regulator module (VRM) is provided as part of the memory board assembly module 100A for converting **an externally supplied voltage** level **available on external source path 104** into appropriate local Voltage levels that power the first and second Voltage paths, i.e., the Vdd and V paths 108, 106, respectively. …

Harris further teaches, by way of example in ¶ 0012, that the 72 pins required by standard 2-ranks FBD module (36 DRAM devices) to receive power from the system board would be replaced by 6 pins when power is provided from an external (+12V) voltage source. Harris expressly teaches a clear advantage of providing power to DIMM from external sources is by being able to supply power to support large scale capacity DIMMs, such as a 144 DRAM devices of an 8-ranks FBD, using 24 pins from the external (+12V) voltage source.

> [0012] By way of example, **a standard FBD module requires** 28V pins (for DRAM devices) and 8V pins (for buffer and logic) and associated Ground

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> returns, resulting in **a total of 72 pins that provide a power supply interface for up to two X4 DRAM ranks (36 devices) and buffer logic**. A voltage-independent FBD design incorporating the embodiment of FIG. 1A is capable of replacing these power supply interface pins **with as few as six +12V pins (from an external voltage source)**, ... Alternatively, **using additional power supply pins** would provide the capability **to support even more devices**. For instance, **with 12 supply pins (at +12V)**, the embodiment of **FIG. 1A can provide enough power to Supply 4 ranks (i.e., 72 devices)**. Likewise, **a memory assembly of 8 ranks (144 devices) may be powered with 24 pins at +12V**.

Even more conclusive evidence of the advantages sought by Harris are disclosed in ¶ 0019 which eliminates any doubts that Harris does not provide power to the DIMM from the system board by expressly stating the elimination of the system board power supply and associated voltage planes. Furthermore, Harris expressly describes the cost reduction associated with the elimination of system-board-specific power supply or regulator, associated components, and heavy etch power planes on the system board. Harris further describes, and as a direct result of the elimination of the system board power supply, that additional advantages can be realized such as a smaller connector, improved signal integrity, or reservation of extra pins for implementing addition standard or proprietary functions.

> [0019] Based on the foregoing Detailed Description, it should be appreciated that an implementation of the embodiments described herein thus **provides a technology-independent voltage distribution** scheme for memory devices **wherein system board power supply and associated voltage plane(s) are eliminated.** Accordingly, power Supply designs complexity as well as **the cost of memory-specific power distribution are reduced**. Cost savings may include, for example, **elimination of system-board-specific power supply or regulator output**, **associated bypass capacitor arrangements, heavy etch or power planes**. Also, under the **technology-independent Voltage distribution scheme disclosed** herein, **cost of memory power regulation scales with populated memory devices**, rather than being pre-provisioned for maximum memory capacity as is typically the case in existing systems. **Additionally, one or more of the following advantages may be realized** in an exemplary Voltage distribution embodiment: provision of tighter, lower inductance regulation which decreases Voltage variability and increases timing margins; **reduction in the pin count on DIMM connector to system board** or memory riser card (**whereby a smaller connector** or wider pin spacing may be accommodated); **improved signal integrity due to reduced crosstalk on the same size connector**; and **reservation of extra pins for implementing additional standard or proprietary functions**.

This clarifies that Harris cannot read on Claim 2, either before or after the instant amended, as the entirety of the disclosure of Harris conveys to one of ordinary skill in the art that

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Harris does not use the DIMM connector to obtain power from the system board. Rather, as shown immediately above, Harris looks to remove the system board power supply and/or repurpose the memory socket pins that would have connected to the power source of the system board.

It is conclusive that Harris teaches (i) the elimination of system-board-specific power supply components and, importantly, the heavy etch power planes used to distribute the voltage supply on the system board to the DIMM connector, and (ii) that the power provided to Harris' memory module does not come from the system board or through the DIMM connector.

Thus, Harris teaches away from providing power from the system board or from the main board voltage sources to the DIMM via the DIMM connector as required by claim 2.

Thus, Claim 2 is allowable for at least this reason. New Claims 44 and 58 also recite the same language and are therefore allowable for at least this reason. The Claims which depend from Claims 2, 44, and 58 are also allowable for at least this reason.

Claim 2 has been further amended to recite "a set of data conduits including at least 72 data conduits" and "a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits." Similar to the power discussed above, the data signals are received by the DIMM from the memory socket of a system board of a computer system in a particular form (i.e., the 1-bit wide DDR per data conduit) and on particular pins of the memory socket (i.e. each of the second set of edge connections electrically connected to a respective data conduit of the set of data conduits of the memory socket). Harris makes no disclosure of signaling protocol other than disclosing that the DIMM which Harris is modifying is an FBDIMM. The FBDIMM standards outline the signaling protocol to be used on FBDIMM systems. In that protocol, address and control information as well as data are packetized in what the standard refers to as "frames." These frames have a header and footer in addition to the multiplexed address and control and data information. Thus, the frames include far more than a single bit. Moreover, they are not DDR data signals as defined in JEDEC standards. Again, these are defined in the FBDIMM standard as something different – namely "frames." The terminology in the FBDIMM

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standards is purposely used by JEDEC to avoid any confusion with data signals as defined in other JEDEC standards, namely all non-FBDIMM DDR standards.

Moreover, the FBDIMM standards make clear that there are not 72 data conduits. Even if the conduits which do exist in FBDIMM, which are called "lanes" (which unmistakably convey frames including BOTH address and control and data signals) are counted as data conduits, there are only 24. The southbound link has 10 lanes, while the northbound link has 14 lanes. Thus, the FBDIMM standards, which must be relied upon as Harris lacks disclosure beyond referencing the FBDIMM standards, fail to disclose the above elements of Claim 2.

Claim 2 is allowable for at least this additional reason. New Claims 44 and 58 also recite the same language and are therefore allowable for at least this additional reason. The Claims which depend from Claims 2, 44, and 58 are also allowable for at least this additional reason.

Claim 2 has been further amended to recite:

> a printed circuit board (PCB) having a form factor with a width dimension and a height dimension, the PCB including:
> an interface having edge connections disposed along the width dimension and configured to fit into the memory socket, the edge connections including:
> a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits,
> a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and
> a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits;
> a set of voltage supply lines electrically connected to the first set of edge connections, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board;
> a set of data lines electrically coupled to respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; and
> a set of address and control lines electrically coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

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The applied prior art does not disclose the claimed dedicated set of edge connections and data lines for data; rather, data in Harris and FBDIMM shares the address and control edge connections and lines because a serial protocol is utilized. Both references are JEDEC standard modules, at least insofar as they use the packetized signaling protocol laid out in the AMB/FBDIMM standards (obviously, Harris is non-standard regarding its power architecture). In that packetized signaling protocol, data and command/control/address signals do not travel on separate lines, because they are sent in packetized forms called "frames" – "After initialization the host communicates with the AMBs on the channel using southbound frames of information containing commands and data." JESD206.01, pg. 55

Thus, the data signals are not received or outputted on "the set of data conduits" and the address and control signals are not received on "the set of address and control conduits" as recited in the claim, rather they are transferred in a packetized format on the same set of conduits, referred to as "lanes" by JESD206.01.

Moreover, the FBDIMM Standards provide no cure for this defect, as they use the same FBDIMM protocols as Harris.

Thus, Claim 2 is allowable for at least this additional reason. New Claims 44 and 58 also recite the same language and are therefore allowable for at least this additional reason. The Claims which depend from Claims 2, 44, and 58 are also allowable for at least this additional reason.

Claim 2 has further been amended to state that:

> first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the system board …

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and

> wherein each component of the set of components:
> (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
> (ii) when the system power is provided to the DIMM from the system board, is powered:
> - only by one or more of the first, second, third, and fourth converter circuits; and
> - only via the one or more of the first, second, third, and fourth regulated voltage lines;

These features are distinguishable from the applied references, at least because the plurality of DDR SDRAM packages is required to be powered "only by one or more of the first, second, third, and fourth converter circuits, and only via the one or more of the first, second, third, and fourth regulated voltage lines". In contrast, Amidi, for example, is operable to switch DRAM memory supply 660 to battery power depending on a comparison to a reference voltage. Amidi Col 4, Lines 44-55 expressly state:

> Signal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two. If system supply 605 has a greater magnitude than reference voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660. If system supply 605 has a magnitude lower than reference voltage 675, then signal 670 causes power switch multiplexer 655 to choose battery power 650 for memory supply 660. Reference voltage 675 is generated in one embodiment by a resistive Voltage divider using resistors 677 and 673 in series between a voltage rail and ground.

This defect is not cured by Harris or FBDIMM at least because they do not recite a response to a trigger condition and Claim 2 is allowable for at least this additional reason. New Claims 44 and 58 also recite the same language and are therefore allowable for at least this additional reason. The Claims which depend from Claims 2, 44, and 58 are also allowable for at least this additional reason.

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Moreover, the Office Action alleges that Amidi discloses "a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to (i) monitor an input voltage supplied via the input voltage supply line, (ii) generate a trigger signal upon detecting a trigger condition, and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM" (Office Action, p. 7, ll. 14-28) as previously recited, prior to the present amendment.

However, Amidi merely discloses transferring control of the volatile memory to the memory module so that the memory module can provide necessary self-refresh signaling to preserve the volatile memory contents upon power supply failure.[1] (Amidi, col. 8, ll. 38-41) Moreover, in Amidi, this is performed using back up battery power. (*Id.*, l. 37) By comparison, claim 2 previously claimed "wherein the controller is configured to perform in response to the trigger signal, a write operation to write data into the nonvolatile memory," and has now been clarifyingly amended to claim a controller including a logic element that, in response to the detected trigger condition, is configured to perform a plurality of write operations. Similarly claim 44 recites a controller including a logic element that, in response to the detected trigger condition, is configured to periodically perform at regular intervals of time a plurality of write operations; and claim 58 recites a controller including a logic element that, in response to the detected trigger condition, is configured to periodically perform every millisecond a plurality of write operations. Levkovitz, cited in the Office Action for allegedly showing these features

[1] "Self-refresh," as explained to the Examiner during the Examiner Interview, is a term of art that defines a state of the DIMM, or individual DDR SDRAM device, in which it receives sufficient power to preserve its information content, but is not accessible for reading or writing. ("The Self Refresh command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation." Ex 1026 JEDEC Standard JESD79-2B Jan 2005)

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(Office Action, p. 6, ll. 14-18) is not properly combinable with Amidi because Amidi uses battery backup power upon detection of power loss to transfer management of volatile memory so that its contents are preserved, whereas Levkovitz performs regular write operations (backups) as a precaution under normal operating conditions and writes volatile memory information into nonvolatile memory such as hard disc, without the urgency of power loss. The contention in the Office Action that the teachings of Levkovitz are combinable with those of Amidi to arrive at the claimed performance of a plurality of write operations by a logic element of a controller in response to a trigger condition is impermissibly grounded in hindsight gleaned from familiarity with Applicant's disclosure. There can be no doubt that such a combination would either change the principle of operation of one of either of the references. A change in the principle of operation is an indicia of non-obviousness. MPEP 2143.01(VI)

Claim 2 has further been amended to state that "the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode." As explained in the note above, "self-refresh mode" is a term of art meaning that the memory device is not accessible for read or write. This is not the case in Amidi, which was cited in the Final Written Decision of the '918 and '054 patents, and relied upon in the Office Action for current limitations, and which at least fails to disclose "the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode," of the current amendment. Amidi discloses that all the DRAM are forced into self-refresh mode. Specifically, Amidi states that a "signal from the trp timer advances the state machine 1100 to self-refresh entry state 1170, with self-refresh initiated for the memory module. The state machine then advances automatically to self refresh state 1180, and stays there automatically self-refreshing the memory module. A reset signal or an exit 5 signal will move the state machine 1100 back to idle state 1110, ending the self-refresh process, such as when a system sufficiently recovers power." (Col. 7, Lines 1-8)

In the Applicant-Initiated Interview Summary filed by the Examiner on 9/13/24, Section V states "Amidi teaches that memory (comprising backup power) may operate in backup mode, in response, for example, in response [*sic*] to change to voltage level (e.g., a triggering

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condition). The backup comprises a plurality of write operations." Applicant has addressed Amidi having the DRAM enter self-refresh mode when switching to backup power supply. It should be noted that self-refresh cannot include performing ANY write operations. Rather, to avoid data loss, the DRAM cells are themselves refreshed to maintain the data as it was when power was lost. Thus, Amidi's battery is used for backup power, but the data is not "backed up" by writing the data to another location. Rather, the data stays right where it was prior to power loss, specifically, in the DRAM.

Additionally, there is only one action which may be termed a "write operation" after the trigger condition is detected in Amidi. Amidi, Col. 8, Lines 30-36 state "If one or both of the clock collapsing or the power Supply diminishing occurs, then at module 1440, the process moves the memory module into a clock and power fault detection state. This may include setting a power fail interrupt bit in a register, indicating that a power failure was detected (or a clock failure) and the memory module assumed control." The writing/setting of the power fail interrupt bit in a register is the only action involving a change in the state of a single bit taken post trigger condition in Amidi. Thus, Amidi does not disclose a plurality of write operations after the detection of a trigger condition.

The Office Action also cites U.S. Patent Publication No. 2007/0088838 to Levkovitz ("Levkovitz"), and specifically to paragraph [0075]. Paragraph [0075] of Levkovitz states:

> In some embodiments, for example, utilizing volatile memory unit 118, a pre-defined memory "dumping" process may be used. For example, content items ready for serving may be received by ad server 110 from control server 120, may be stored in volatile memory unit 118, and optionally may not be stored in a non-volatile memory of ad server 110. Ad server 110 may serve content items directly from its volatile memory unit 118, and may further store in memory unit 118 a log tracking the activity or servings done by ad server 110. Periodically, for example, at pre-defined time intervals (e.g., every 60 seconds, every 5 minutes, every hour, etc.) or upon serving a certain number of servings of content items (e.g., every 100 impressions, every 500 impressions, etc.), ad server 110 may "dump" or copy the activity log data into a non-volatile memory unit, e.g., included in ad server 110 or database 140. This may allow ad server 110, for example, to rapidly serve content items from its rapidly-available volatile memory unit 118, instead of from a slower non-volatile memory (e.g., database 140 or other database); and the periodical

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"dumping" process of activity logs may limit the data loss in case of a power outage which may erase the volatile memory unit 118.

From this passage, a POSITA would conclude that the activity log is copied to NVM as part of a regular course of operation. Thus, there would be no motivation to combine Levkovitz with Amidi, as the setting of the bit which even if it were construed as a write operation it must be for a single bit and is done only Amidi detecting power failure. There would have to be a teaching or suggestion to perform periodic writes after the trigger condition in Amidi, but after the trigger condition, Amidi very distinctly wants to conserve power as much as possible, not perform write after write. Thus, Amidi chooses to supply power to the DRAMs from backup power source (battery) and put the DIMM (DRAMs) in self-refresh. In contrast, Claims 2, 44, and 58 recite "wherein, in response to the detected trigger condition, the logic element is configured to perform a plurality of write operations," or "wherein, in response to the detected trigger condition, the logic element is configured to perform at regular intervals of time a plurality of write operations," or "wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond a plurality of write operations."

Harris and FBDIMM Standards cannot cure this deficiency because they do not disclose any kind of backup write operation. The S3 mode discussed in the FBDIMM standards is also self-refresh, so it suffers from the same deficiencies as Amidi.

Claims 2, 44, and 58 and the claims which depend therefrom are allowable for at least this additional reason.

Claim 2, 44, and 58, as currently amended, recite:

wherein the plurality of DDR SDRAM packages includes:
a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;
a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and
when the system power is provided to the DIMM from the system board:

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- the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.

While Harris, the FBDIMM Standards, and Amidi all disclose ranks generally, they do not disclose the specific limitations recited above. Harris specifically discloses that its DIMM "may be configured as having one or more ranks (e.g., 2, 4, 8, or more)." Amidi does not use the term rank in the disclosure; rather, Amidi only very generally discloses "Mounted on memory card 310 are memory chips 320 (320A-I as illustrated) and resistors 330 (330A-I as illustrated)." The FBDIMM Standards, specifically, JESD205 disclose several raw card configurations with ranks. The ranks have eight devices and are not sub-grouped below the rank level. This is confirmed by the Pin Description on page 29 of that standard:

$\overline{CS}$[1:0]A, $\overline{CS}$[1:0]B	Chip Select (one per rank)	4

The Pin Description only describes a single chip select for each rank.

This is further confirmed by the Pin Description of JESD 82-20. On page 82 of that standard, the table with the pin description discloses:

$\overline{CS0}$A-$\overline{CS1}$A, $\overline{CS0}$B-$\overline{CS1}$B	O	**Chip Select:** Used with $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ to specify the SDRAM command. These signals are used for selecting one of two SDRAM ranks. $\overline{CS0}$ is used to select the first rank and $\overline{CS1}$ is used to select the second rank.

Thus, the chip select disclosed is used to select a rank and not some subgrouping below the rank or ranks.

As described above, the FBDIMM standards make clear that there are not at least 72 data conduits to communicate at least 72 1-bit wide DDR signals between the DIMM and the computer system. Even if conduits which do exist in FBDIMM, are used as serial communication "lanes" (which unmistakably convey frames including BOTH address and control and data) are counted as data conduits, there are only 24 lane conduits in FBDIMM. The southbound link has 10 lanes, while the northbound link has 14 lanes. Thus, the FBDIMM standards, which must be relied upon as Harris lacks disclosure beyond referencing the FBDIMM standards, fail to disclose the above elements of Claim 2.

Thus, individually or in combination, Harris, FBDIMM Standards, and Amidi cannot disclose:

> wherein the plurality of DDR SDRAM packages includes:
> a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;
> a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and
> when the system power is provided to the DIMM by the system board:
> • the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;
> • the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
> • the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and
> wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.

as recited by Claims 2, 44, and 58. Claims 2, 44, and 58 and the claims which depend

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therefrom are allowable for at least this additional reason.

Claims 2, 44, and 58 have been further amended to recite:

> first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the system board

and have been separately amended to recite that:

- the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;

Amidi discloses switching to a backup power system upon power fault and placing the DRAM in self-refresh mode, as is discussed in detail above. FBDIMM standards disclose an "S3 mode," discussed in part above. However, in S3 mode, the DRAM are in self refresh just like Amidi, as is disclosed on Page 21 of JESD 82-20:

> 6. Command/Address output control in S3 mode. When the Advanced Memory Buffer core logic is in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low. In S3 mode, 1.8V supply is on. 1.5V, Vtt, and 3.3V are off. DRAMs are in self refresh, and the CKE signals must be driven low.

Harris discussed no trigger condition and therefore no operation post trigger condition. Thus, Harris, FBDIMM standards, and Amidi, alone or in combination cannot disclose:

> first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the system board

and

- the first and second groups of DDR SDRAM packages are configured to be

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accessible and not in self-refresh mode;

as recited by Claims 2, 44, and 58. Thus, Claims 2, 44, and 58 and the Claims which depend therefrom are allowable for at least this additional reason.

Conclusion

Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Respectfully submitted,

Date: October 1, 2024

/Khaled Shami/

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Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3546	FILED BY	LISA MARGARET ELLIOTT
PATENT CENTER #	67397793	FILING DATE	01/24/2022
CUSTOMER #	151145	FIRST NAMED INVENTOR	Chi-She Chen
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Khaled Shami

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Attachment showing support for all Claim elements.pdf	68	Applicant Arguments/Remarks Made in an Amendment	3961 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
Attachment showing support for all Claim elements.pdf	664A60D5E02B93DE404ECD392B24A269EF0CFF62BA367F93CE8F0734294DFBF3B276DF753BFEAB6E3E64D7BAFB0B7913BCA3B5B6BA5013FF49DFB57D6E55F47C

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.