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APPLICANT: Netlist, Inc.

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TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

AMENDMENT

Commissioner:

In response to the final Office Action mailed January 24, 2025, Applicant submits the following Amendment and Remarks.

Listing of Claims begins on page **2**.

Remarks begin on page **29**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Currently amended) A dual in-line memory module (DIMM) configured to fit into a memory ~~socket~~ slot connector of a system board of a computer system, the memory ~~socket~~ slot connector including a set of power conduits, a set of data conduits ~~including at least 72 data conduits~~, and a set of address and control conduits, wherein ~~system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board~~, a 1-bit wide double data rate (DDR) data signal signals are transferred is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are delivered electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:

~~a printed circuit board (PCB) having a form factor with a width dimension and a height dimension, the PCB including:~~

~~an interface having edge connections disposed along the width dimension and configured to fit into the memory sockets~~ slot connector of the system board, the edge connections including:

a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

a second set of edge connections ~~each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and~~

a third set of edge connections configured to be electrically connected to ~~respective address and control conduits of the set of address and control conduits,~~[[;]]

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM, ~~the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board;~~

a set of data lines electrically ~~coupled~~ connected to ~~respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines;~~ and

a set of address and control lines electrically ~~coupled~~ connected to ~~respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;~~

a controller including a voltage monitor circuit and nonvolatile memory, ~~the controller coupled to the PCB and electrically connected to the~~ to an input voltage supply line of the set of voltage supply lines, ~~the controller configured to receive the input voltage via the input voltage supply line, the controller including;~~

~~nonvolatile memory;~~

~~a data storage element configured to store a plurality of data bits;~~

~~a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element; and~~

~~a voltage monitor circuit electrically connected to the input voltage supply line and coupled to the logic element, the voltage monitor circuit configured to: (i) monitor and compare the input voltage supplied via the input voltage supply line to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage; and (ii) generate a trigger signal upon detecting detect a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the detected trigger conditionsignal, the logic element is configured to perform a plurality of write operations, including:~~

~~a first write operation to write a first set of data bits into a first portion of the data storage element;~~

~~a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently~~

~~a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations;~~

~~wherein, when the system power is provided to the DIMM from the system board:~~

~~the trigger condition occurs when the input voltage exceeds a first threshold voltagegoes above both the first and second threshold voltages; and~~

~~wherein:~~

~~a specified operating voltage value is within a range of operating voltage values of the DIMM, the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value;~~

~~the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value, the first threshold voltage corresponds to the lower operating voltage value, and the second threshold voltage corresponds to the upper operating voltage value;~~

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (DDR-SDRAM) packages ~~devices~~ coupled to the set of address and control lines and to the set of data lines, ~~each the~~ DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of ~~m bits and configured devices being operable to receive or output m-1 bit wide DDR data signals via respective m data lines of the set of data lines in response to~~ based on address and control signals received from the system board via ~~address and control lines of the set of address and control lines, wherein m is equal to four or eight, and~~

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, ~~and each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the~~ input voltage supply line and to deliver power ~~system board, the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltage lines, respectively,~~

wherein the set of components includes~~including~~:

a first component configured to receive power via at least electrically ~~connected to the first regulated voltage line and powered by the first regulated voltage when the system power is provided to the DIMM from the system board;~~

a second component configured to receive power via at least electrically ~~connected to the second regulated voltage line and powered by the second regulated voltage when the system power is provided to the DIMM from the system board;~~

a third component configured to receive power via at least electrically
~~connected to the third regulated voltage line and powered by the third regulated~~
~~voltage when the system power is provided to the DIMM from the system board; and~~

a fourth component electrically configured to receive power via at least
~~connected to the fourth regulated voltage line and powered by the fourth regulated~~
~~voltage when the system power is provided to the DIMM from the system board;~~

~~wherein each of the first, second, and third converter circuits is a buck converter,~~
~~and the fourth converter circuit is a voltage reducing circuit; and~~

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third,
and fourth regulated voltage lines; and

(ii) receives power when the system power is provided to the DIMM
~~from the system board, is powered:~~

~~only by one or more of the first, second, third, and fourth converter~~
~~circuits; and only via the one or more of the first, second, third, and~~
~~fourth regulated voltage lines.[];[]~~

wherein the DIMM is configurable to operate in any of a plurality of states including a
first state and a second state, wherein the controller is further configured to control power
delivery to one or more components of the set of components for the DIMM to operate in the
first state or the second state, whereby power to the set of components via the first, second,
third, and fourth regulated voltage lines is turned on when the DIMM is operating in the first
state, and whereby power to the first component via the first regulated voltage line is turned off
and power to the second, third, and fourth components via the second, third and fourth
regulated voltage

lines is turned on when the DIMM is operating in the second state

~~wherein the plurality of DDR SDRAM packages includes:~~

~~a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;~~

~~a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and~~

~~when the system power is provided to the DIMM from the system board:~~

- ~~• the first and second groups of DDR SDRAM packages are configured to be accessible and not in self refresh mode;~~
- ~~• the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and~~
- ~~• the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and~~
- ~~• wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.~~

3 – 27. (Canceled)

28. (Currently Amended) The DIMM of claim 2, wherein the ~~second component is further connected to the first regulated voltage line and is powered by the first and second~~

~~regulated voltages when the system power is provided to the DIMM from the system board~~ plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

wherein when power from the power rails of the system board is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines;
- the at least 40 1-bit wide DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit wide DDR error-correcting code (ECC) data signals; and

the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

29. (Currently Amended) The DIMM of claim 2, wherein the controller further includes: ~~data storage element is a buffer configured to store the plurality of data bits or a~~

~~First In First- Out (FIFO) buffer configured to store the plurality of data bits.~~

a data storage element configured to store a plurality of data bits and a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and wherein the write operation conducted by the controller in response to the trigger signal includes:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

30. (Currently Amended) The DIMM of claim 2, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage. the PCB has a form factor with a width and a height dimension, and wherein the width dimension is 133.35 millimeters.

31. (Currently Amended) The DIMM of claim ~~30~~ 2, wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when power from the power rails of the system board is provided to the DIMM. the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.

32. (Currently Amended) The DIMM of claim ~~2~~ 29, wherein, prior to performing the third write operation, the logic element is ~~further~~ configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations.

33. (Currently Amended) The DIMM of claim ~~2~~ 29, wherein, prior to performing the third write operation, the logic element is ~~further~~ configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.

34. (Currently Amended) The DIMM of claim 2, wherein, when power from the power rails of the system board is provided to the DIMM~~the system power is provided to the DIMM from the system board~~, the nonvolatile memory is not powered using the first regulated voltage.

35. (Currently Amended) The DIMM of claim ~~2~~ 29, wherein, prior to performing the third write operation, the logic element is ~~further~~ configured to perform, in response to the detected trigger ~~conditions~~signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

36. (Currently Amended) The DIMM of claim ~~29~~ 2, wherein, prior to performing the third write operation, the logic element is ~~further~~ configured to perform, in response to the detected trigger ~~conditions~~signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

37. (Currently Amended) The DIMM of claim ~~23~~ 5, wherein, ~~prior to performing the third write operation, the logic element is further configured to perform (i) a first read operation of the plurality of read operations to read the first set of data bits from the first portion of the data storage element, and (ii) a second read operation of the plurality of read operations to read the second set of data bits from the second portion of the data storage element, and to generate the third set of data bits based on the read first and second sets of data bits.~~ each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.

38. (Currently Amended) The DIMM of claim ~~29~~ 2, wherein, prior to performing the first and second write operations, the logic element is ~~further~~ configured to perform, in

response to the detected trigger ~~condition~~signal, one or more read operations.

39. (Currently Amended) The DIMM of claim 38, wherein the logic element is ~~further~~ configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM ~~packages~~devices, respectively.

40. (Canceled)

41. (Currently Amended) The DIMM of claim 29 ~~2~~, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.

42. (Currently Amended) The DIMM of claim 29, wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits, ~~in response to the detected trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.~~

43. (Currently Amended) The DIMM of claim 23 ~~1~~, wherein, when power from the power rails of the system board is provided to the DIMM ~~the system power is provided to the DIMM from the system board~~, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

44. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory ~~socket~~ slot connector of a system board of a computer system, the memory ~~socket~~ slot connector including a set of power conduits, a set of data conduits ~~including at least 72 data conduits~~, and a set of address and control conduits, wherein ~~system power from the system board is provided to the DIMM via the memory socket by the set of power~~

~~conduits and the DIMM is configured to operate using only the provided system power from the system board, a 1-bit wide double data rate (DDR) data signals are transferred is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are delivered from the system board electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:~~

~~a printed circuit board (PCB) having a form factor with a width dimension and a height dimension, the PCB edge connections configured to fit into the memory slot connector of the system board, the edge connections including:~~

~~an interface having edge connections disposed along the width dimension and configured to fit into the memory socket, the edge connections including:~~

~~a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,~~

~~a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits[[:]],~~

~~a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board[[:]]~~

~~a set of data lines electrically coupled to respective edge connections of connected to the second set of edge connections, wherein each data line of the set of~~

~~data lines is configured to electrically conduct a 1-bit wide DDR data signal, and
wherein the set of data lines includes at least 72 data lines; and~~

~~a set of address and control lines electrically coupled to respective edge
connections of electrically connected to the third set of edge connections and configured
to electrically conduct address and control signals;~~

~~a controller including coupled to the PCB and electrically connected to the input
voltage supply line, the controller configured to receive the system power and the input
voltage via the input voltage supply line, the controller including:~~

~~nonvolatile memory;~~

~~a data storage element configured to store a plurality of data bits; and~~

~~a logic element coupled to the nonvolatile memory and the data storage element
and configured to electrically communicate with the nonvolatile memory and the data
storage element; and~~

~~a voltage monitor circuit and a data storage element configured to store a
plurality of data bits, the controller coupled to the PCB and electrically connected to
the an input voltage supply line of the set of voltage supply lines, and coupled to the
logic element, the voltage monitor circuit configured to:~~

- ~~(i) monitor an input voltage supplied via the input voltage supply
line; and~~
- ~~(ii) generate a trigger signal upon detecting a trigger condition; and~~
- ~~(iii) transmit the trigger signal to at least one other portion of the
controller, wherein, compare the input voltage to a plurality of
threshold voltages including a first threshold voltage and a
second threshold voltage; and
detect a trigger condition;~~

~~wherein, in response to the detected trigger condition, the logic element
-in response to the detected trigger condition, the controller is configured to
periodically perform, at regular intervals of time, a plurality of write operations,
including[[:]]~~

a first write operation to write a first set of data bits into a first portion of the data storage element; and

a second write operation to write a second set of data bits into a second portion of the data storage element;

wherein, when the system power is provided to the DIMM from the system board:

- the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and

wherein:

- a specified operating voltage value is within a range of operating voltage values of the DIMM;
- the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value;
- the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value;
- the first threshold voltage corresponds to the lower operating voltage value; and
- the second threshold voltage corresponds to the upper operating voltage value;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (DDR SDRAM) packages coupled to the set of address and control lines and to the set of data lines, the each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and configured devices being operable to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines based on in response to address and control signals received from the system board via the set of address and control lines via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and

first, second, third, and fourth converters ~~circuits~~ coupled to the PCB and to the input voltage supply line, ~~each of the first, second, third, and fourth converter circuits~~ and configured to, ~~in response to the detected trigger condition,~~ receive power ~~supplied by~~ from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines, ~~when the system power is provided to the DIMM from the system board,~~ the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power supplied by the input voltage supply line, and

(ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltages lines, respectively, wherein the set of components includes ~~including~~:

a first component ~~electrically connected to the first regulated voltage line and powered by~~ configured to receive power via the first regulated voltage line ~~when the system power is provided to the DIMM from the system board;~~

a second component ~~electrically connected to the second regulated voltage line and powered by~~ configured to receive power via the second regulated voltage line ~~when the system power is provided to the DIMM from the system board;~~

a third component ~~electrically connected to the third regulated voltage line and powered by~~ configured to receive power via the third regulated voltage line ~~when the system power is provided to the DIMM from the system board; and~~

a fourth component ~~electrically connected to the fourth regulated voltage line and powered by~~ configured to receive power via the fourth regulated voltage line ~~when the system power is provided to the DIMM from the system board;~~

~~wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit; and~~

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) receives power ~~when the system power is provided to the DIMM from the system board, is powered:~~

- ~~only by one or more of the first, second, third, and~~

~~fourth converter circuits; and~~
only via the one or more of the first, second, third, and fourth regulated voltage lines.~~[[;]]~~

~~wherein the plurality of DDR SDRAM packages includes:~~

~~a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;~~

~~a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and~~

~~when the system power is provided to the DIMM from the system board:~~

- ~~• the first and second groups of DDR SDRAM packages are configured to be accessible and not in self refresh mode;~~
- ~~• the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and~~
- ~~• the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and~~

~~wherein the sum of the 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.~~

45. (Currently Amended) The DIMM of claim 44, wherein the controller further

includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.

~~the plurality of write operations further includes a third write operation subsequent to the first and second write operations; and wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform at regular intervals of time all of the first and second write operations followed by the third write operation.~~

46. (Currently Amended) The DIMM of claim 44~~5~~, ~~wherein, the logic element is further configured to perform the third write operation by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations~~ wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;
a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals

and eight 1-bit wide DDR error-correcting code (ECC) data signals; and wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector socket, and the total number of data conduits is at least 72 data conduits.

47. (Currently Amended) The DIMM of claim 45, wherein, ~~prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on groups of data bits stored in the data storage element~~ the logic element is configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.

48. (Currently Amended) The DIMM of claim 44, wherein, when ~~the system~~ power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

49. (Currently Amended) The DIMM of claim 47, wherein, ~~in response to the detected trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal~~ the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

50. (Currently Amended) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is ~~further~~ configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

51. (Currently Amended) The DIMM of claim 47~~4~~, wherein, prior to performing the first and second write operations, the logic element is ~~further~~ configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM ~~packages~~devices, respectively.

52. (Currently Amended) The DIMM of claim 44, wherein, ~~prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time a plurality of read operations~~ when power is provided to the DIMM from the power rails of the system board, the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

53. (Currently Amended) The DIMM of claim 52~~46~~, wherein, ~~prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read data bits from the data storage element and to generate the third set of data bits based on the read data bits~~ when power is provided to the DIMM from the power rails of the system board, the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages.

54. (Currently Amended) The DIMM of claim 49, wherein the logic element is further to perform the third write operation by writing the third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations ~~44, wherein the width dimension is 133.35 millimeters.~~

55. (Currently Amended) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on the groups of data bits stored in the data storage element ~~54, wherein the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.~~

56. (Currently Amended) The DIMM of claim 49~~5~~, wherein the third write operation

comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

57. (Currently Amended) The DIMM of claim 5244, wherein ~~[[,]]~~ when ~~the system~~ power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and ~~the input voltage is~~ below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

58. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory ~~socket~~ slot connector of a system board of a computer system, the memory ~~socket~~ slot connector including a set of power conduits, a set of data conduits ~~including at least 72 data conduits~~, and a set of address and control conduits, wherein ~~system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board~~, a 1-bit wide double data rate (DDR) data signals are transferred ~~is electrically conducted~~ between the system board and the DIMM via ~~the memory socket by each data conduit of the set of data conduits~~, and ~~address and control signals are delivered from the system board electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits~~, the DIMM comprising:

a printed circuit board (PCB) having ~~a form factor with a width dimension and a height dimension~~, the PCB edge connections configured to fit into the memory slot connector, the edge connections including:

~~an interface having edge connections disposed along the width dimension and configured to fit into the memory socket~~, the edge connections including:

a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits and operable to deliver to

the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

~~a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and~~

~~a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits[[:]],~~

~~a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board[[:]]~~

~~a set of data lines electrically coupled to respective edge connections of connected to the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines[[:]] and~~

~~a set of address and control lines electrically coupled to respective edge connections of connected to the third set of edge connections, wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines and configured to electrically conduct address and control signals;~~

~~a controller including coupled to the PCB and electrically connected to the input voltage supply line, the controller configured to receive the system power and the input voltage via the input voltage supply line, the controller including:~~

~~nonvolatile memory;~~

~~a data storage element configured to store a plurality of data bits; and~~

~~a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element; and~~

~~a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and electrically connected to the~~ an input voltage supply line of the set of voltage supply lines, and coupled to the logic element; the voltage monitor circuit configured to:

- ~~(i)~~ monitor an input voltage supplied via the input voltage supply line; and
- ~~(ii)~~ generate a trigger signal upon detecting a trigger condition; and
- ~~(iii)~~ transmit the trigger signal to at least one other portion of the controller, wherein the ~~compare the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage; and~~
detect a trigger condition;

~~wherein, in response to the detected trigger condition, the logic element controller is configured to periodically perform every millisecond, in response to the trigger signal, a plurality of write operations, including:~~

~~a first one or more write operations operation to write a first set of data bits into a first portion of the data storage element; and~~

~~a second write operation to write a second set of data bits into a second portion of the data storage element;~~

~~wherein, when the system power is provided to the DIMM from the system board:~~

- ~~• the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and~~

~~wherein:~~

- ~~• a specified operating voltage value is within a range of operating voltage values of the DIMM;~~

- ~~the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value;~~
- ~~the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value;~~
- ~~the first threshold voltage corresponds to the lower operating voltage value; and~~
- ~~the second threshold voltage corresponds to the upper operating voltage value;~~

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (DDR SDRAM) packages ~~devices~~ coupled to the set of address and control lines and to the set of data lines, ~~the each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and configured~~ devices being operable to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines based on in response to address and control signals received from the system board via the set of address and control lines ~~via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and~~

first, second, third, and fourth ~~voltage reducing circuits~~ converter circuits coupled to the PCB and to the input voltage supply line, ~~each of the first, second, third, and fourth converter circuits~~ and configured to, in response to the detected trigger condition, receive power supplied by from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines, when the system power is provided to the DIMM from the system board, the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltages lines, respectively, wherein the set of components includes including:

a first component ~~electrically connected to the first regulated voltage line and powered by~~configured to receive power via the first regulated voltage line~~when the system power is provided to the DIMM from the system board;~~

a second component ~~electrically connected to the second regulated voltage line and powered by~~ configured to receive power via the second regulated voltage line~~when the system power is provided to the DIMM from the system board;~~

a third component ~~electrically connected to the third regulated voltage line and powered by~~ configured to receive power via the third regulated voltage line~~when the system power is provided to the DIMM from the system board; and~~

a fourth component ~~electrically connected to the fourth regulated voltage line and powered by~~ configured to receive power via the fourth regulated voltage line~~when the system power is provided to the DIMM from the system board;~~

~~wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit; and~~

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) receives power ~~when the system power is provided to the DIMM from the system board, is powered:~~

- ~~only by one or more of the first, second, third, and fourth converter circuits; and~~

only via the one or more of the first, second, third, and fourth regulated voltage lines;

wherein the plurality of DDR SDRAM ~~packages~~ devices includes:

a first group of at least five DDR SDRAM ~~packages~~ devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; and

a second group of at least four DDR SDRAM ~~packages~~ devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; ~~and~~

~~when the system power is provided to the DIMM from the system board:~~

- ~~• the first and second groups of DDR SDRAM packages are~~ configured to be accessible and not in self-refresh mode;
- ~~• the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and~~
- ~~• the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and~~

~~wherein the sum of the 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.~~

59. (Currently Amended) The DIMM of claim 586, ~~wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations; and wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.~~

wherein when power from the power rails of the system board is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM devices is configured to be enabled, in response

- to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and
- wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector socket, and the total number of data conduits is at least 72 data conduits

60. (Currently Amended) The DIMM of claim 597, wherein the logic element is ~~further~~ configured to perform ~~the a~~ third write operation ~~by~~ subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

61. (Currently Amended) The DIMM of claim 560, wherein, ~~in response to the detected trigger condition, the voltage monitor circuit is further configured to generate and transmit a~~ trigger signal the logic element is configured to perform, prior to the first and second write operations, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

62. (Currently Amended) The DIMM of claim 586, wherein, ~~in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond a plurality of read operations prior to performing the first and second write operations~~ when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

63. (Currently Amended) The DIMM of claim 5860, wherein ~~the logic element is further configured to perform a first and second read operations of the plurality of read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM packages, respectively~~ when power is provided to the DIMM from the power rails of the system board, the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

64. (Currently Amended) The DIMM of claim 563, wherein when power is provided to the DIMM from the power rails of the system board, the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages. ~~the width dimension is 133.35 millimeters.~~

65. (Currently Amended) The DIMM of claim 58 62, wherein the controller further includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to wire a second set of data bits into a second portion of the data storage element ~~the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.~~

66. (Currently Amended) The DIMM of claim 586, wherein each of the first, second, and third ~~voltage-reducing~~ converter circuits is a buck converter.

67. (Currently Amended) The DIMM of claim 586, wherein, when ~~the system~~ power is provided to the DIMM from the power rails of ~~from~~ the system board, the nonvolatile memory is not powered using the first regulated voltage.

68. (Currently Amended) The DIMM of claim 6358, wherein, when ~~the system~~ power is provided to the DIMM from the power rails of ~~from~~ the system board, an additional trigger condition occurs when the input voltage is above the first threshold and ~~the input voltage is~~ below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

REMARKS

The final Office Action mailed January 24, 2025, has been carefully considered.

Reconsideration in view of the following remarks is respectfully requested.

By this Amendment, Applicant has **amended claims 2 and 28-39 and 41-68; and canceled claim 40.**

Claims 2 and 28-39 and 41-68 are now pending and subject to examination.

For convenience, a Claim Support Table is provided below as Appendix A, as a well as a clean copy of the amended claims as Appendix B.

Interview Record

Applicant gratefully acknowledges the courtesy and consideration extended to Applicant's undersigned representative during the telephone interview with Examiner Farrokh on Wednesday March 5, 2025.

During the interview, Applicant explained that support for the instant amendment can be found in the specification, and that the accompanying Support Table detailed the location in the specification for said support by mapping each claim limitation to an example location in the written description and/or drawings at which it is discussed.

The Examiner specifically inquired about the support for “conduits” (plural), despite the discussion only of “conduit” (singular) in the specification. Applicant explained that the specification (para. [00123], FIGS. 2 and 12, etc.) describes a memory slot connector on the system board which the edge connectors of the DIMM plug into. The memory slot connector is further described as having a conduit that connects to an edge connector so that power can be transmitted from the system board to the DIMM. Other edge connectors of the DIMM serve to transmit data and control signals, while others still transmit address signals. These other edge connectors are also described as plugging into the memory slot connector on the system board, and the same reasoning—that the connections are made by way of corresponding conduits in the

memory slot connector—clearly applies. Therefore while not explicitly described, the presence of conduits for the transfer of data, address and control signals in addition to the data conduit is at least implicit as would be understood by a person of ordinary skill in the art.

The Examiner also inquired about the 1-bit wide DDR data signals, and for example the receipt or output of the claimed “40 1-bit wide DDR data signals.” The Examiner’s attention is respectfully directed to for example para. [00178] discussing the portions, or slices, into which a data word may be divided. It will be appreciated that a data word is the collection of bits that may for example be written into or read from volatile or nonvolatile memory, buffer, or other components. The word may comprise 72 individual bits, and may be sliced into two portions—for example a 32-bit portion, and a 40-bit portion. Other sized slices, or portions, as well as more than two portions, are also contemplated, and the portions may be handled by the inventive DIMM in unison or separately from one another.

Applicant also directed the Examiner’s attention to the added limitation “wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM” in the independent claims, which clarifies the intended scope of the limitation “the DIMM is configured to operate using only the provided system power from the system board” from the prior claim version. Applicant explained that this limitation is supported for example in FIG. 16, which shows the power module 1100 receiving power “from system” at nodes Vdd and gnd corresponding to the system’s power rails. It was explained that this contrasts starkly with the teachings of Harris et al. (US 2006/0174140, “Harris”), whose module derives power from an external power supply, and teaches away from supplying power to the memory module from the power rails of a system board, as further explained below.

Rejection(s) Under 35 U.S.C. § 112, First Paragraph

Claims 2 and 28-68 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement for allegedly containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C.

112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant has canceled claim 40, and has amended claims 2, 28-39 and 41-68 to re-write or cancel some of the limitations that are the basis of the instant 35 U.S.C. § 112, first paragraph rejection. Where other such limitations remain, attention is respectfully directed the Claim Support Table below, which maps all claim limitations to their support in the specification.

It is respectfully submitted that claims 2, 28-39 and 41-68 are now in compliance with 35 U.S.C. § 112, first paragraph, and the rejection thereunder should be withdrawn.

Amendment to Claims

The claims have been amended for improved clarity in particularly pointing out and distinctly claiming certain aspects of the invention. No amendment made is related to the statutory requirements of patentability unless expressly stated herein. No amendment is made for the purpose of narrowing the scope of any claim, unless Applicant argues herein that such amendment is made to distinguish over a particular identified reference or combination of references.

Rejection(s) Under 35 U.S.C. § 112(b) (or Pre-AIA 35 U.S.C. § 112, Second Paragraph)

Claims 2, 44 and 58 stand rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for allegedly failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention.

The limitation “trigger condition occurs when the input voltage goes above both the first and second threshold voltages” has been moved from the prior version of independent claim 2 to the current version of dependent claims 53 and 64. The support for this limitation can be found for example in para. [00130], which describes *inter alia* two thresholds, stating that “a trigger condition occurs when the voltage goes below a threshold or above another threshold.” According to this statement, “a threshold” can be considered the first, lower threshold, and

“another threshold” can be considered the second, upper threshold. If the input voltages goes above the second, upper threshold, then by definition it also goes above the first lower threshold. This therefore satisfies the language of the claims that “trigger condition occurs when the input voltage goes above both the first and second threshold voltages.”

The limitation relating to the DDR SDRAM devices being “configured to be accessible and not in self-refresh mode” has been moved from the prior version of independent claim 2 to the current version of dependent claims 28, 46 and 59. Support for this limitation can be found for example in para. [00178], which states that, *inter alia*, “In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or “slice”) may comprise 40 bits of the data word, and the second portion (or “slice”) may comprise the remaining 32 bits of the data word.” (Emphasis added) Thus in this configuration the 72-bit data word comprises an accessible 40-bit slice and an accessible 32-bit slice. Para. [00178] then states that “the process of ‘slicing’ the volatile memory during a backup includes [1] bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer.” In 1 above, the 32-bit slice becomes accessible and not in self-refresh; and in 2 above, the 40-bit slice becomes accessible and not in self-refresh mode. Both of these states satisfy the claim language of the DDR SDRAM devices being “configured to be accessible and not in self-refresh mode.”

It is respectfully submitted that the claims are in compliance with 35 U.S.C. § 112(b) (or pre-AIA 35 U.S.C. § 112, second paragraph), and the rejection thereunder should be withdrawn.

Harris Teaches Away from the Claimed Invention

In the Response to Remarks, the Office Action continues to cite Harris (U.S. Publication No. 2006/0174140) as relevant to the claimed invention. Harris, however, teaches away from the claimed invention. In particular, independent claims 2, 44 and 58, as amended, each recite “wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM.” (Emphasis added)

Contrary to the above claimed feature, Harris teaches “[t]o cope with power requirements, industry standard memory modules, e.g., Dual In-line Memory Modules (DIMMS) populated with dynamic random access memory (DRAM) devices, are provided with **power supply rails** (on a relatively large number of pins) that are **powered from system board or main board voltage sources**, and are specific to the memory technology. As the performance of the DRAM technology goes up, and timing margins shrink, **it is becoming increasingly more difficult for the system board sources to provide tightly regulated power for the DRAM cores** as well as input/output (I/O) interface buffers. Furthermore, each generation of DIMM/DRAM technology requires a different power supply which keeps getting lower (e.g., 3.3V, 2.5V, 1.8V, 1.5V and beyond), **thereby making it difficult to mix memory technologies on a system board**, or provide upgrades to next generation DRAM technology in a cost-effective manner.” (Harris at para. [0002], emphasis added.) Thus, Harris explicitly teaches away from using the power rails of the system board of the host computer system to supply power to the DIMM.

That the voltage powering the memory module of Harris does not come from the power rails and conduits of the memory slot connector of the system board is further evident from the term “external” used to describe it. This term is introduced in Harris’ Summary section (para. [0003]) as a counterpoint to the description of the conventional configuration in which DIMMs “provided with power supply rails . . . that are powered from system board or main board voltage sources, and are specific to the memory technology.” (Para. [0002]) This is problematic, Harris explains, because the specificity to the memory technology means DIMMs are customized to particular DRAMs due to the DRAMs’ specific power requirements, that impose specific conduit/memory slot connector constraints, and therefore, when improved DRAM technology emerges, DIMMs have to be completely redesigned rather than just adapted to the new improvements. (*Id.*) Harris’ external voltage source allows such adaptation because the conduit/memory slot connector power configuration constraints are removed when power is provided externally instead. The memory slot connector becomes independent of the power requirements of the DRAMs, which can be satisfied by provision of an external voltage, according to Harris.

This voltage independence of the memory slot connector is further explained in para. [0012], which states that “A voltage-independent FBD design incorporating the embodiment of FIG. 1A is capable of replacing these power supply interface pins with as few as six +12V pins (*from an external voltage source*).” (Emphasis added.) In addition, a further advantage of the voltage independence of the memory slot connector is described in para. [0014], which states that since voltage is provided externally, a variety of sources can be used, including “any combination of known or heretofore unknown voltage Supplies, either regulated or unregulated, and even including variable voltages.” In addition, Harris states at para. [0012] that due to this independence, “the overall power supply interface to the memory module 100A is improved to better support large memory capacity scaling, hot-pluggability, DRAM technology independence (e.g., DDR2, DDR3, DDR4, and other DRAM types), high DRAM device count (i.e., amenable to multi-ranking), as well as provide improved system-level cost sharing. Additionally, memory performance is also improved because of tighter voltage regulation.”

All these explanations inescapably point to the conclusion that the gist of Harris’ invention is to use an external power source that does not come from the power rails and conduits of the memory slot connector of the system board of a computer system, which directly contravenes the arrangement of “a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM” set forth in all the independent claims. Harris thus teaches away from the claimed invention, and cannot be relied upon as a basis for rejecting any of the pending claims. It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743 (Fed. Cir. 1983); see also MPEP 2145.X.D.2.

Canceled Claims

Claim 40 has been canceled without prejudice or disclaimer of the subject matter contained therein.

Conclusion

Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Respectfully submitted,

Date: March 24, 2025
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APPENDIX A
Claim Support Table

Claim Element	Limitation	Support
2.1	A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals between the system board and the DIMM are transferred via the set of data conduits, and control signals are delivered from the system board to the DIMM via the set of address and control conduits	Para. [00123] “For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.” Dual in-line memory module (DIMM) has an edge connector 1022 that includes edge connections for power, data, and address and control signals designed to fit into a memory socket of a computer system. See Figs. 2 and 12:

slot connector of the system board, the edge connections including: a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM, a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits.

certain embodiments **provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.** For example, the interface 1022 can comprise **a standard 240-pin DDR2 edge connector.**”

This paragraph describes the contact of the edge connections and the slot connector, as well as a JEDEC standard 240 pin DDR2 edge connector. The JEDEC standard specifies what voltages the system voltage regulator is to provide to which pins in the slot, which are then passed on to the edge connector.

When the interface 1022 edge connector is inserted into the memory socket of the computer system, edge connections will mate with corresponding conduits and an electrical connection is established for system power, data, and address and control signals to be electrically conducted to the edge connections on the PCB, and PCB traces also called lines allow signals and power/voltage to be electrically conducted on the PCB.

Fig. 2 which shows the DIMM in the socket on the motherboard:

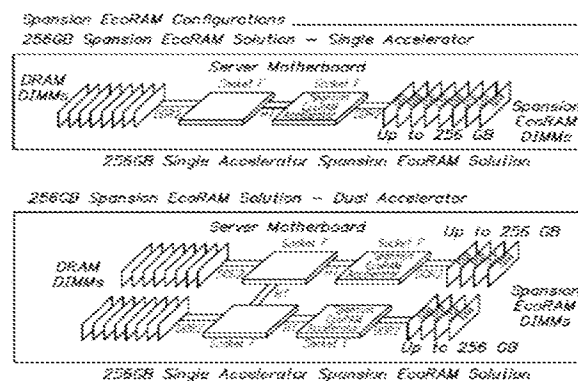
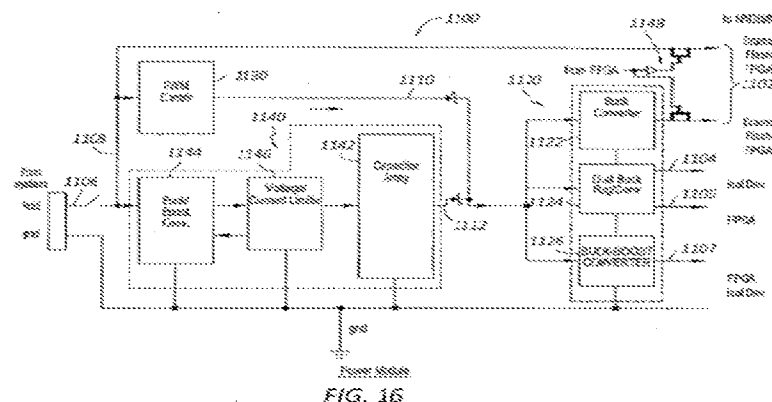


FIG. 2
(PRIOR ART)

Note the power rails (Vdd and Gnd) of the system board coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 16.



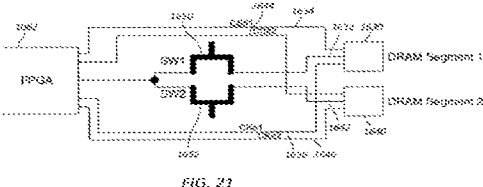
		The DIMM operates using only the system power provided from the system board, for example as specified and is well known in the JEDEC standard 240-pin DDR2 edge connector.
2.3	a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM, a set of data lines electrically coupled to the second set of edge connections, and a set of address and control lines electrically connected to the third set of edge connections,	Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 12, Fig. 13, Fig. 14 and Fig. 16. For example, in Fig. 12 the input voltage supply lines are shown electrically connected to the Voltage Monitor 1050. FIG. 12 FIG. 16 For example, the respective power rails (Vdd and gnd) are labeled “from system”, on left of Fig. 16, are electrically connected via a set of voltage supply lines to the PWM Controller 1130, and the ground supply line (gnd). Para. [00124] “For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.” These are coupled to the data lines (by way of edge connections) of the Standard DIMM Interface 1022 by way of the switch 1052. Note also the address and control lines from edge connections of the Standard DIMM Interface 1022 coupled to the DRAM 1030 through the Switch 1052 in FIG. 12.
2.4	a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit	The specification discloses a controller 1062 designed to seamlessly integrate with various other components described within the memory system 1010 that enhances performance (speed), efficiency and reduces cost. The controller 1062 comprises a microcontroller unit (MCU) 1060, logic element 1070, buffer, voltage monitor circuit 1050, and one or more additional components. Logic element 1070 comprises internal nonvolatile memory, one or more integrated circuits and various discrete electrical elements. The controller 1062 receives system power from the standard DIMM interface 1022. For example,

	configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;	support is found in at least [00127], [00133], and [00172]; and Fig. 12, Fig. 13, Fig. 14, and Fig. 16. Para. [00133] “The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022.” Fig. 14 depicts the voltage monitoring circuit 1050 receiving the input voltage via interface 1022 and coupled to the logic element 1070 Para. [00133] “In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.” Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.” The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”
2.5	a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the	FIG. 12 Para. [00124] “Volatile memory elements 1032 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).” Para. [00172] “In one embodiment, for example, the volatile memory subsystem 1030 comprises a 72-bit data bus (e.g., each data word at each addressable

	set of address and control lines; location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.” And Para. [00122] “In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein.” And Para. [00124] “In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and synchronous DRAM (SDRAM). For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032. The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, volatile memory elements 1032 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein.”	
2.6	first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines	FIG. 16

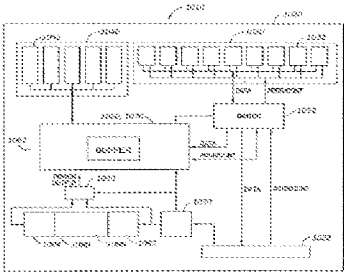
		converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system. For example, the buck converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.”
2.7	wherein the set of components includes: - a first component configured to receive power via at least the first regulated voltage line; - a second component configured to receive power via at least the second regulated voltage line; - a third component configured to receive power via at least the third regulated voltage line; and - a fourth component electrically configured to receive power via at	FIG. 16 FIG. 12 On the left of FIG. 16, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck converter 1122, dual buck converter 1124, and

	least the fourth regulated voltage line	buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively. On the right, each of the DRAMs is shown as being connected to the first regulated voltage, for example. On the right, the isolation device is shown as being connected to the second regulated voltage, for example. On the right, the FPGA 1070 is shown as being connected to the third regulated voltage, for example. On the right, the MCU 1060 is shown as also being connected to the fourth regulated voltage, as is shown in the embodiment of FIG. 12, the MCU 1060 is part of the controller 1062. This is further specified in the text of the disclosure: Para. [00148] “the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.” As shown in FIG. 12, above, the controller 1062 includes the components FPGA 1070, and the MCU 1060, and thus needs two different voltages for each of the components 1070, 1060.
2.8	wherein each component of the set of components: (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines	FIG. 16

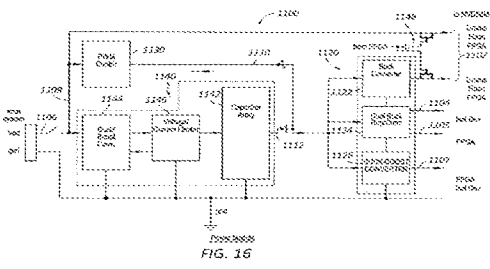
		from the first power subsystem in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.” The system power is provided to the PWM controller 1130 and from there to the four converter circuits (conversion element 1120) is the only power to the module. In the second state all components are powered from the power supplied from one or more of the four converter circuits via one or more of the four regulated voltages. There is no alternative power source claimed.
28.1	wherein the plurality of DDR SDRAM devices includes: a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and	FIG. 21  Chip Select 1 and Chip Select 2 going to each group is shown in FIG. 21 above. Para. [00172] “FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology including two DRAM segments 1630, 1640 for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from the first DRAM segment 1630 and the second DRAM segment 1640 of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062.” Para. [00177] “In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.” Para. [00178] “In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain

		embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash)." This claim is limited to x4 and x8 DRAM. When using x8, it takes five DRAM to receive or output 40 bits. The remaining bits in the word are 32, which means it would take four x8 DRAM to complete receiving or outputting the word. Thus, you have a module with a total of nine DRAM (5+4) as shown in FIG. 13 and discussed in Para. [00126]. If x4 are used, the number of DRAM are correspondingly more.
28.2	when power from the power rails of the system board is provided to the DIMM: • each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode; • the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second	Para. [00173] "In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are not accessible when they are in self-refresh mode, and maintain stored information and are accessible when they are in active mode." Para. [00178] "In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into

	group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; •the at least 40 1-bit wide DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit wide DDR error-correcting code (ECC) data signals	self-refresh in the example embodiment.” Thus according to [00178], 72-bit data word comprises an accessible 40-bit slice and an accessible 32-bit slice. Para. [00178] also states that “the process of ‘slicing’ the volatile memory during a backup includes [1] bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer.” In 1 above, the 32-bit slice is accessible and not in self-refresh; and in 2 above, the 40-bit slice is accessible and not in self-refresh mode. Para. [00182] “In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.”
28.3	the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.	Para. [00123] “The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.” Para. [00172] “In one embodiment, for example, the volatile memory subsystem 1030 comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.” Para. [00178] “In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or “slice”) may comprise 40 bits of the data word, and the second portion (or “slice”) may comprise the remaining 32 bits of the data word.”
29.1	a data storage element configured to store a plurality of data bits and a logic element coupled to the nonvolatile memory and the data storage element and	The current application specification discloses a controller 1062 designed to seamlessly integrate with various other components described within the memory system 1010 that enhances performance (speed), efficiency and reduces cost. The controller 1062 comprises a microcontroller unit (MCU) 1060, logic element 1070, buffer, voltage monitor circuit 1050, and one or more additional components. Logic element 1070 comprises internal nonvolatile memory, one or more integrated circuits and various discrete

	configured to electrically communicate with the nonvolatile memory and the data storage element,	electrical elements. The controller 1062 receives system power from the standard DIMM interface 1022. For example, support is found in at least [00127], [00133], and [00172]; and Fig. 12, Fig. 13, Fig. 14, and Fig. 16. Para. [00127] “FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein.” FIG. 14  A buffer (data storage element) is shown in Fig. 13 and Fig. 14, and disclosed to store data in at least 172, and 178. Para. [00172] “In certain embodiments, the controller 1062 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO).” Para. [00178] “For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA.” For example, FIG. 13 shows controller 1062 comprising a buffer. Para. [00127] “Referring to FIG. 12, in certain embodiments, the logic element 1070 comprises a field-programmable gate array (FPGA). In certain embodiments, the logic element 1070 comprises an FPGA available from Lattice Semiconductor Corporation which includes an internal flash. In certain other embodiments, the logic element 1070 comprises an FPOA available from another vendor. The internal flash can improve the speed of the memory system 1010 and save physical space. Other types of logic elements 1070 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 1070 is a custom device. In certain embodiments, the logic element 1070 comprises various discrete electrical elements, while in certain other embodiments, the logic element 1070 comprises one or more integrated circuits. FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into
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		a single controller 1062 in accordance with certain embodiments described herein. In certain embodiments, the controller 1062 includes one or more other components. For example, in one embodiment, an FPGA without an internal flash is used and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA.” FIG. 12
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		“In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.” The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.
30	when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage	Para. [00133] “In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.” Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.” The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”
31	wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when power from the power rails of the system board is provided to the DIMM	FIG. 16  Para. [00148] “In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the

		memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052. ”
32	wherein, prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations	Para. [00178] “The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”
33	wherein, prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations	Para. [00179] “In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer.”
34	wherein, when power from the power rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.	Para. [00149] “In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102. ”
35	wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of	Para. [00178] “The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash). ” Para. [00178] “The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash). ”

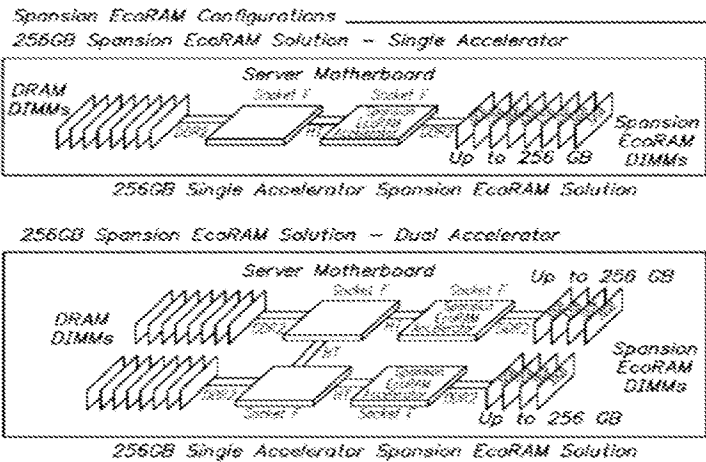
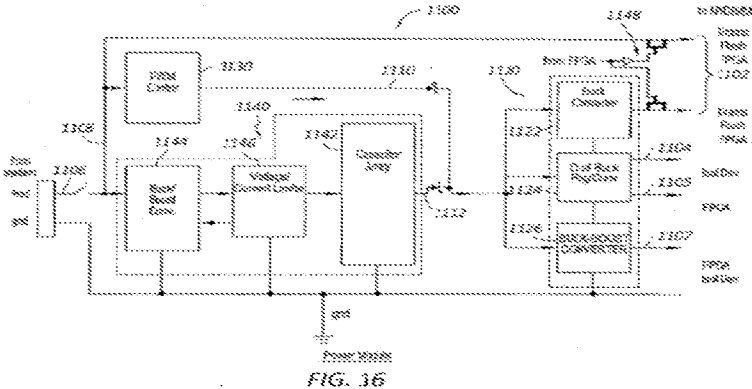
	data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.	Para. [00179] “In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.”
35	wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.	Para. [00178] “The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).” Difference from Claim 35 is the read from the buffer is a plurality of steps in Claim 35, and specifically two steps here. Same sentence in Para. [00178] supports both scenarios. Para. [00174] “In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040.” Reading a data word or a block of words to be written into the NVM.
37	wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.	Para. [00148] “The conversion element 1120 may comprise a plurality of sub blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010.” And Para. [00148] “In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system.”
38	wherein, prior to performing the first and second write operations, the logic element is further configured to	Para. [00178] “The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”

	perform, in response to the detected trigger signal, one or more read operations.	Para. [00179] “In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.”
39	wherein the logic element is further configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.	Para. [00130] “In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.” Para. [00174] “In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040. In certain embodiments, this process is called “slicing” the volatile memory subsystem 1030.” Para. [00177] “In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”
41	wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.	FIG. 21 Para. [00172] “FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010.” Para. [00177] “The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion

		(also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.” FIG. 13 As can be seen in FIG. 13, the transfer from the DRAM occurs on a connection on the right side of the buffer, and the transfer to NVM will occur on a connection on the left side of the buffer.
42	wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.	A buffer (data storage element) is shown in Fig. 13 and Fig. 14, and disclosed to store data in at least 172, and 178. Para. [00172] “In certain embodiments, the controller 1062 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO).” Para. [00178] “For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA.” For example, FIG. 13 shows controller 1062 comprising a buffer:
43.1	wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold	Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In

	and below the second threshold; and wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.	some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.”
44.1	A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals between the system board and the DIMM are transferred via the set of data conduits, and control signals are delivered from the system board to the DIMM via the set of address and control conduits	Para. [00123] “For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.” Dual in-line memory module (DIMM) has an edge connector 1022 that includes edge connections for power, data, and address and control signals

		“The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown). For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system . . . For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.”
44.2	the DIMM comprising: a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the edge connections including: a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM, a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits,	Para. [00123] “The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown). For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.” This paragraph describes the contact of the edge connections and the slot connector, as well as a JEDEC standard 240 pin DDR2 edge connector. The JEDEC standard specifies what voltages the system voltage regulator is to provide to which pins in the slot, which are then passed on to the edge connector. When the interface 1022 edge connector is inserted into the memory socket of the computer system, edge connections will mate with corresponding conduits and an electrical connection is established for system power, data, and address and control signals to be electrically conducted to the edge connections on the PCB, and PCB traces also called lines allow signals and power/voltage to be electrically conducted on the PCB.

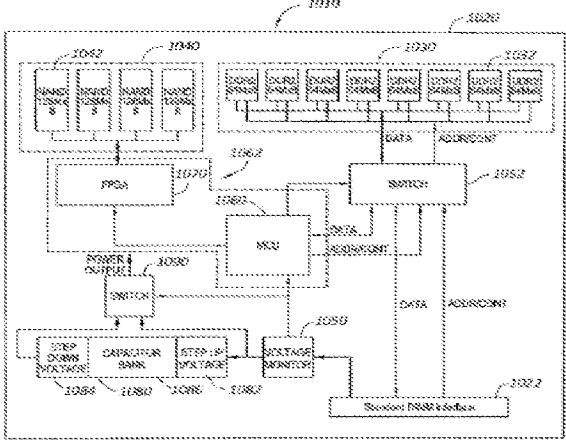
		Fig. 2 which shows the DIMM in the socket on the motherboard:  FIG. 2 (PRIOR ART) Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 16.  FIG. 16 The DIMM operates using only the system power provided from the system board, for example as specified and is well known in the JEDEC standard 240-pin DDR2 edge connector.
44.3	a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge	Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 12, Fig. 13, Fig. 14 and Fig. 16. For example, in Fig. 12 the input voltage supply lines is shown electrically connected to the Voltage Monitor 1050. FIG. 12

connections of the DIMM a set of data lines electrically coupled to the second set of edge connections, and a set of address and control lines electrically to the third set of edge connections ,	
FIG. 16	
For example, respective power conduits (Vdd and gnd) of the set of power conduits of the memory socket are labeled “from system”, on left of Fig. 16, are electrically connected via a set of voltage supply lines to the PWM Controller 1130, and the ground supply line (gnd). Para. [00124] “For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.” Note also the address and control lines from the Standard DIMM Interface 1022 coupled to the DRAM 1030 through the Switch 1052 in FIG. 12.	FIG. 16 For example, respective power conduits (Vdd and gnd) of the set of power conduits of the memory socket are labeled “from system”, on left of Fig. 16, are electrically connected via a set of voltage supply lines to the PWM Controller 1130, and the ground supply line (gnd). Para. [00124] “For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.” Note also the address and control lines from the Standard DIMM Interface 1022 coupled to the DRAM 1030 through the Switch 1052 in FIG. 12.
44.4 a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage	The current application specification discloses a controller 1062 designed to seamlessly integrate with various other components described within the memory system 1010 that enhances performance (speed), efficiency and reduces cost. The controller 1062 comprises a microcontroller unit (MCU) 1060, logic element 1070, buffer, voltage monitor circuit 1050, and one or more additional components. Logic element 1070 comprises internal nonvolatile memory, one or more integrated circuits and various discrete electrical elements. The controller 1062 receives system power from the standard DIMM interface 1022. For example, support is found in at least [00127], [00133], and [00172]; and Fig. 12, Fig. 13, Fig. 14, and Fig. 16.

	supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;	A buffer (data storage element) is shown in Fig. 13 and Fig. 14, and disclosed to store data in at least 172, and 178. Para. [00172] “In certain embodiments, the controller 1062 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO).” Para. [00133] “The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022.” “In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060)” Fig. 14 depicts the voltage monitoring circuit 1050 receiving the input voltage via interface 1022 and coupled to the logic element 1070 Para. [00133] “In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.” Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.” The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”
44.5	a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM	FIG. 12

devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines;

FIG. 12



Para. [00124]

“**Volatile memory elements 1032 compatible with certain embodiments described herein have packaging** which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).”

Para. [00172]

“In one embodiment, for example, the volatile memory subsystem 1030 comprises a **72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)**, the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”

And

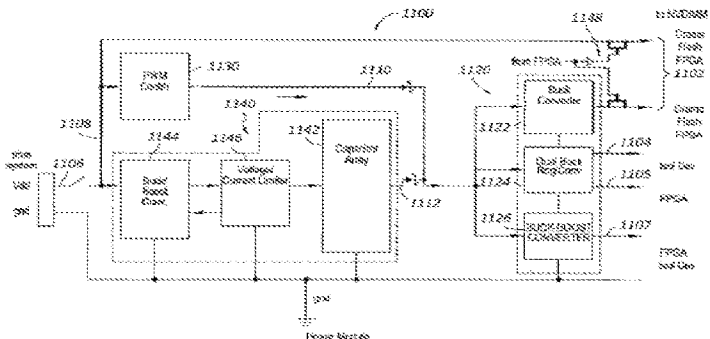
Para. [00122]

“In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein.”

And

Para. [00124]

“In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. **Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and synchronous DRAM (SDRAM).** For example, in the block diagram of FIG. 12, **the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.** The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, **volatile memory elements 1032 having bit widths of 4, 8, 16, 32,**

		as well as other bit widths, are compatible with certain embodiments described herein.”
44.6	first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines	FIG. 16  FIG. 16 On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck converter 1122, dual buck converter 1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively. Para. [00148] “The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system. For example, the buck converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage

		1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.”
44.7	wherein the set of components includes: - a first component configured to receive power via at least the first regulated voltage line; - a second component configured to receive power via at least the second regulated voltage line; - a third component configured to receive power via at least the third regulated voltage line; and - a fourth component electrically configured to receive power via at least the fourth regulated voltage line	FIG. 16 FIG. 12 On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck convertor 1122, dual buck converter1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively. On the right, each of the DRAM are shown as being connected to the first regulated voltage, for example. On the right, the isolation device is shown as being connected to the second regulated voltage, for example. On the right, the FPGA 1070 is shown as being connected to the third regulated voltage, for example. On the right, the MCU 1060 is shown as also being connected to the fourth regulated voltage, as is shown in the embodiment of FIG. 12, the MCU 1060 is part of the controller 1062. This is further specified in the text of the disclosure: Para. [00148] “the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.”

		As shown in FIG. 12, above, the controller 1062 includes the components FPGA 1070, and the MCU 1060, and thus needs two different voltages for each of the components 1070, 1060.
44.8	wherein each component of the set of components: (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines.	FIG. 16

	communicate with the nonvolatile memory and the data storage element.	FIG. 14
46.1	wherein the plurality of DDR SDRAM devices includes: a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;	FIG. 21 FIG. 21 Chip Select 1 and Chip Select 2 going to each group is shown in FIG. 21 above. Para. [00172] “FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology including two DRAM segments 1630, 1640 for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from the first DRAM segment 1630 and the second DRAM segment 1640 of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062.” Para. [00177] “In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from

		the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.” Para. [00178] “In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).” This claim is limited to x4 and x8 DRAM. When using x8, it takes five DRAM to receive or output 40 bits. The remaining bits in the word are 32, which means it would take four x8 DRAM to complete receiving or outputting the word. Thus, you have a module with a total of nine DRAM (5+4) as shown in FIG. 13 and discussed in Para. [00126]. If x4 are used, the number of DRAM are correspondingly more
46.2	wherein when power from the power rails of the system board is provided to the DIMM: • each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode; • the first group of DDR SDRAM packages is configured to be	Para. [00173] “In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are not accessible when they are in self-refresh mode, and maintain stored information and are accessible when they are in active mode.” Para. [00178] “In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during

	enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and	a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment.” Thus according to [00178], 72 bit data word comprises an accessible 40-bit slice and an accessible 32-bit slice. Para. [00178] also states that “the process of ‘slicing’ the volatile memory during a backup includes [1] bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer.” In 1 above, the 32-bit slice is accessible and not in self-refresh; and in 2 above, the 40-bit slice is accessible and not in self-refresh mode. Para. [00182] “In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.”
46.3	wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.	Para. [00123] “The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.” Para. [00172] “In one embodiment, for example, the volatile memory subsystem 1030 comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32

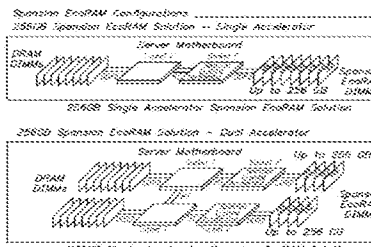
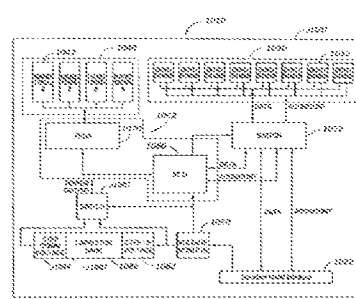
		bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.” Para. [00178] “In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.”
47	wherein the logic element is further configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.	Para. [00174] “In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040. In certain embodiments, this process is called "slicing" the volatile memory subsystem 1030.” Para. [00177] “In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.” For the chain of system power electrical connection to the controller, see 2.1, 2.4, 2.5, and 2.6 above.
48	wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.	Para. [00149] “In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102.”
49	wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during	Para. [00177] “In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.” Para. [00130] “In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a

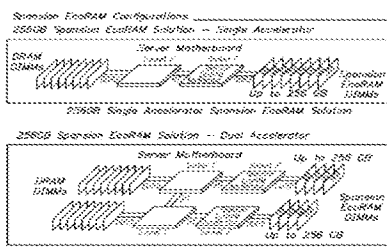
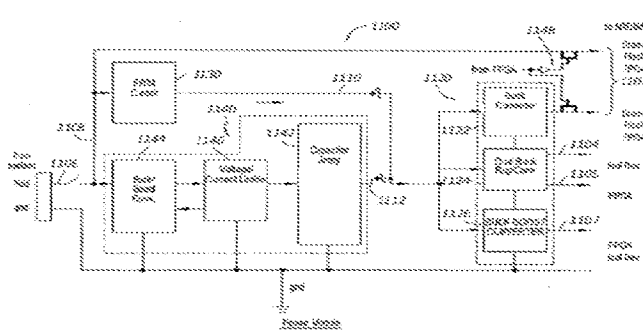
	the first and second write operations, and wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.	backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.”
50	wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits, respectively.	Para. [00130] “In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.” Para. [00178] “The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer.”
51	wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time, one or more read operations to read the	Para. [00130] “In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.” Para. [00177] “The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion

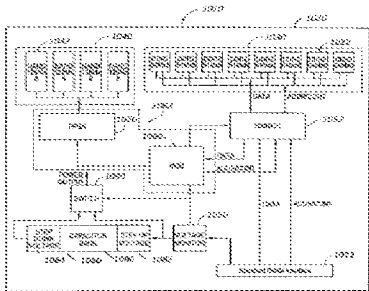
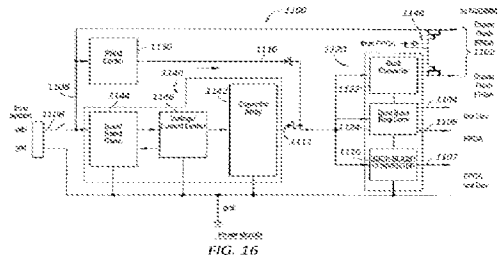
	first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.	(also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”
52	wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.	Para. [00133] “In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.” Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.” The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”
53	wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages.	Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. Para. [00130] thus describes <i>inter alia</i> two thresholds, stating that “a trigger condition occurs when the voltage goes below a threshold or above another threshold.” From this statement, “a threshold” can be considered the first, lower threshold, and “another threshold” can be considered the second, upper threshold. If the input voltages goes above the second, upper threshold, then by definition it also goes above the first lower threshold.
54	wherein the logic element is further configured to perform the third write operation by writing the third set of data bits from the data	Para. [00177] “In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data

	storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations	word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.” Para. [00178] “ The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash). ”
55	wherein, prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on the groups of data bits stored in the data storage element	Para. [00178] “ The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”
56	wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.	FIG. 21

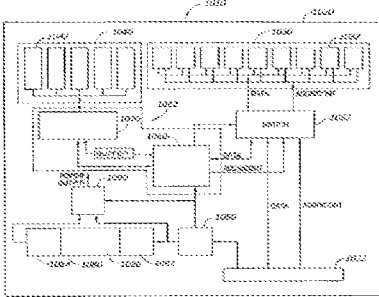
		FIG. 13 As can be seen in FIG. 13, the transfer from the DRAM occurs on a connection on the right side of the buffer, and the transfer to NVM will occur on a connection on the left side of the buffer.
57	wherein when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal	Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.”
58.1	A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals between the system board and the	Para. [00123] “For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.”

	DIMM are transferred via the set of data conduits, and control signals are delivered from the system board to the DIMM via the set of address and control conduits	Dual in-line memory module (DIMM) has a edge connector 1022 that includes edge connections for power, data, and address and control signals designed to fit into a memory socket of a computer system. See Figure 2 and  FIG. 2 (PRIOR ART) Fig. 12. The memory socket of a computer system includes pins soldered onto the system board that provide electrical conduits for system power, data, and address and control signals from the system board to be electrically connected to corresponding edge connections of the edge connector 1022 when it is inserted into the memory socket. Para. [00123] “The PCB 1020 can comprise an interface 1022 that is configured to be in  FIG. 12 electrical communication with the host system (not shown). For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system . . . For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.”
58.2	the DIMM comprising: a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the edge connections including: a first set of edge connections configured	Para. [00123] “The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown). For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.”

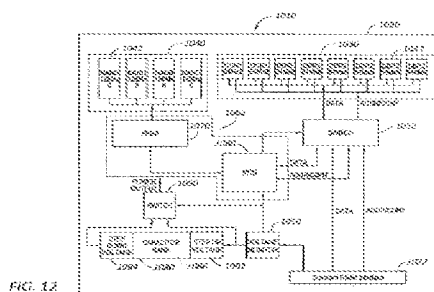
	to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM, a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits,	This paragraph describes the contact of the edge connections and the slot connector, as well as a JEDEC standard 240 pin DDR2 edge connector. The JEDEC standard specifies what voltages the system voltage regulator is to provide to which pins in the slot, which are then passed on to the edge connector. When the interface 1022 edge connector is inserted into the memory socket of the computer system, edge connections will mate with corresponding conduits and an electrical connection is established for system power, data, and address and control signals to be electrically conducted to the edge connections on the PCB, and PCB traces also called lines allow signals and power/voltage to be electrically conducted on the PCB. Fig. 2 which shows the DIMM in the socket on the motherboard:  FIG. 2 (PRIOR ART) Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 16.  FIG. 16 The DIMM operates using only the system power provided from the system board, for example as specified and is well known in the JEDEC standard 240-pin DDR2 edge connector.
58.3	a set of voltage supply lines electrically connected to the first set of edge connections and	Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 12, Fig. 13, Fig. 14 and

	configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM a set of data lines electrically coupled to the second set of edge connections, and a set of address and control lines electrically to the third set of edge connections,	Fig. 16. For example, in Fig. 12 the input voltage supply lines is shown electrically connected to the Voltage Monitor 1050. FIG. 12  FIG. 12 FIG. 16  FIG. 16 For example, respective power conduits (Vdd and gnd) of the set of power conduits of the memory socket are labeled “from system”, on left of Fig. 16, are electrically connected via a set of voltage supply lines to the PWM Controller 1130, and the ground supply line (gnd). Para. [00124] “For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.” Note also the address and control lines from the Standard DIMM Interface 1022 coupled to the DRAM 1030 through the Switch 1052 in FIG. 12.
58.4	wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines;	Para. [00178] “In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions

		of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment.” Para. [00182] “In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.” And Para. [00172] “In one embodiment, for example, the volatile memory subsystem 1030 comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.” The embodiment of FIG. 13 shows nine x8 DRAM devices for a data bus bit width of 72:
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	monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the data storage element;	“In certain embodiments, the controller 1062 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO).” Para. [00178] “For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA.” For example, FIG. 13 shows controller 1062 comprising a buffer:  FIG. 13 Para. [00133] “The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022.” “In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060)” Fig. 14 depicts the voltage monitoring circuit 1050 receiving the input voltage via interface 1022 and coupled to the logic element 1070 Para. [00133] “In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.” Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.” The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”
58.6	a set of components coupled to the PCB, the set of components	FIG. 12

including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines;



Para. [00124]

“Volatile memory elements 1032 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).”

Para. [00172]

“In one embodiment, for example, the volatile memory subsystem 1030 comprises a **72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)**, the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”

And

Para. [00122]

“In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein.”

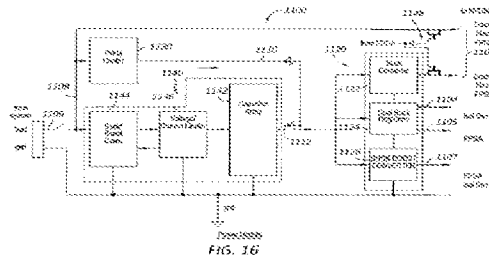
And

Para. [00124]

“In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. **Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and synchronous DRAM (SDRAM).** For example, in the block diagram of FIG. 12, **the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.** The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, **volatile memory elements 1032 having bit widths of 4, 8, 16, 32,** as well as other bit widths, are compatible with certain embodiments described herein.”

58.7	first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines
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FIG. 16



On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck convertor 1122, dual buck converter 1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively.

Para. [00148]

“The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system. For example, the buck converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.”

58.8	wherein the set of components includes: - a first component configured to receive power via the first regulated voltage line; - a second component configured to receive power via the second regulated voltage line; - a third component configured to receive power via the third regulated voltage line; - and - a fourth component electrically configured to receive power via the fourth regulated voltage line	FIG. 16 FIG. 12 On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck convertor 1122, dual buck converter1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively. On the right, each of the DRAM are shown as being connected to the first regulated voltage, for example. On the right, the isolation device is shown as being connected to the second regulated voltage, for example. On the right, the FPGA 1070 is shown as being connected to the third regulated voltage, for example. On the right, the MCU 1060 is shown as also being connected to the fourth regulated voltage, as is shown in the embodiment of FIG. 12, the MCU 1060 is part of the controller 1062. This is further specified in the text of the disclosure: Para. [00148] “the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.” As shown in FIG. 12, above, the controller 1062 includes the components FPGA 1070, and the MCU 1060, and thus needs two different voltages for each of the components 1070, 1060
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58.9	wherein each component of the set of components: (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines	FIG. 16 On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 that, when the system power is received, couples power to each of the four converter circuits via voltage 1110. Para. [00145] “In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120.” Para. [00151] “The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. During the second condition, the method 1200 comprises providing the first voltage 1102 and the second voltage 1104 to the memory system 1010 from the first power subsystem in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.” The system power is provided to the PWM controller 1130 and from there to the four converter circuits (conversion element 1120) is the only power to the module. In the second state all components are powered from the power supplied from one or more of the four converter circuits via one or more of the four regulated voltages. There is no alternative power source claimed.
58.10	wherein the plurality of DDR SDRAM devices includes: a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;	FIG. 21 Chip Select 1 and Chip Select 2 going to each group is shown in FIG. 21 above. Para. [00172]

	a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal	“FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology including two DRAM segments 1630, 1640 for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from the first DRAM segment 1630 and the second DRAM segment 1640 of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062.” Para. [00177] “In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.” Para. [00178] “In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).” This claim is limited to x4 and x8 DRAM. When using x8, it takes five DRAM to receive or output 40 bits. The remaining bits in the word are 32, which means it would take four x8 DRAM to complete receiving or outputting
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		the word. Thus, you have a module with a total of nine DRAM (5+4) as shown in FIG. 13 and discussed in Para. [00126]. If x4 are used, the number of DRAM are correspondingly more.
59.1	wherein when power from the power rails of the system board is provided to the DIMM: • each group of the first and second groups of DDR SDRAM is configured to be accessible and not in self-refresh mode; • the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and • the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and	Para. [00173] “In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are not accessible when they are in self-refresh mode, and maintain stored information and are accessible when they are in active mode.” Para. [00178] “In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment.” Thus according to [00178], 72-bit data word comprises an accessible 40-bit slice and an accessible 32-bit slice. Para. [00178] also states that “the process of ‘slicing’ the volatile memory during a backup includes [1] bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer.” In 1 above, the 32-bit slice is accessible and not in self-refresh; and in 2 above, the 40-bit slice is accessible and not in self-refresh mode. Para. [00182] “In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.”

59.2	wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.	Para. [00123] “The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.” Para. [00172] “In one embodiment, for example, the volatile memory subsystem 1030 comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.” Para. [00178] “In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.”
60	wherein the logic element is further configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.	Para. [00177] “In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”
61	wherein the logic element is further configured to perform, prior to the first write operation and the second write operation, first and second read operations by reading the first and	<u>[00172]</u> <u>FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010.</u> <u>The controller read first and second data slices (sets of data bits) from first and second groups of DDR SDRAM packages, and then write the first and second sets of data bits into the controller 1062 (data storage element).</u>

	second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.	
62	wherein when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.	Para. [00149] “In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102.”
63	when the power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.	Para. [00133] “In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.” Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.” The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”
64	wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages.	Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.” Para. [00130] thus describes <i>inter alia</i> two thresholds, stating that “a trigger condition occurs when the voltage goes below a threshold or above another threshold.” From this statement, “a threshold” can be considered the first, lower threshold, and “another threshold” can be considered the second, upper threshold. If the input voltages goes above the second, upper threshold, then by definition it also goes above the first lower threshold.

65	wherein the controller further includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to write a second set of data bits into a second portion of the data storage element	The specification discloses a controller 1062 designed to seamlessly integrate with various other components described within the memory system 1010 that enhances performance (speed), efficiency and reduces cost. The controller 1062 comprises a microcontroller unit (MCU) 1060, logic element 1070, buffer, voltage monitor circuit 1050, and one or more additional components. Logic element 1070 comprises internal nonvolatile memory, one or more integrated circuits and various discrete electrical elements. The controller 1062 receives system power from the standard DIMM interface 1022. For example, support is found in at least [00127], [00133], and [00172]; and Fig. 12, Fig. 13, Fig. 14, and Fig. 16. Para. [00133] “The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022.” Fig. 14 depicts the voltage monitoring circuit 1050 receiving the input voltage via interface 1022 and coupled to the logic element 1070. Para. [00130] “In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.” Para. [00177] “In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”
66	wherein each of the first, second, and third converter circuits is a buck converter.	Para. [00148] “The conversion element 1120 may comprise a plurality of sub blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010.” And Para. [00148] “In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the

		fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system. ”
67	wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.	Para. [00149] “In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102. ”
68	wherein, when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.	Para. [00130] “In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage . For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage . In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value , such as, for example, 10 percent above a specified operating voltage . In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. ”

APPENDIX B

Clean Copy of Amended Claims

1. (Canceled)

2. (Currently amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM are transferred via the set of data conduits, and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

a second set of edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the

controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via at least the first regulated voltage line;

a second component configured to receive power via at least the second regulated voltage line;

a third component configured to receive power via at least the third regulated voltage line; and

a fourth component electrically configured to receive power via at least the fourth regulated voltage line; and

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines.

3– 27. (Canceled)

28. (Currently Amended) The DIMM of claim 2, wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

wherein when power from the power rails of the system board is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines;
- the at least 40 1-bit wide DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit wide DDR error-correcting code (ECC) data signals; and

the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

29. (Currently Amended) The DIMM of claim 2, wherein the controller further

includes:

a data storage element configured to store a plurality of data bits and a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and wherein the write operation conducted by the controller in response to the trigger signal includes:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

30. (Currently Amended) The DIMM of claim 2, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.

31. (Currently Amended) The DIMM of claim 2, wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when power from the power rails of the system board is provided to the DIMM.

32. (Currently Amended) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations.

33. (Currently Amended) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based

on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.

34. (Currently Amended) The DIMM of claim 2, wherein, when power from the power rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.

35. (Currently Amended) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

36. (Currently Amended) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

37. (Currently Amended) The DIMM of claim 2, wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.

38. (Currently Amended) The DIMM of claim 29, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger signal, one or more read operations.

39. (Currently amended) The DIMM of claim 38, wherein the logic element is configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices,

respectively.

40. (Canceled)

41. (Currently Amended) The DIMM of claim 29, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.

42. (Currently Amended) The DIMM of claim 29, wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.

43. (Currently Amended) The DIMM of claim 31, wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

44. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the

system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
- (ii) generate a trigger signal upon detecting a trigger condition; and
- (iii) transmit the trigger signal to at least one other portion of the controller,

wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via the first regulated voltage line;

a second component configured to receive power via the second regulated voltage line;

a third component configured to receive power via the third regulated voltage line; and

a fourth component electrically configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines.

45. (Currently Amended) The DIMM of claim 44, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.

46. (Currently Amended) The DIMM of claim 44, wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

47. (Currently Amended) The DIMM of claim 45, wherein the logic element is configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.

48. (Currently Amended) The DIMM of claim 44, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

49. (Currently Amended) The DIMM of claim 47, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

50. (Currently Amended) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

51. (Currently Amended) The DIMM of claim 47, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

52. (Currently Amended) The DIMM of claim 44, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

53. (Currently Amended) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages.

54. (Currently Amended) The DIMM of claim 49, wherein the logic element is configured to perform the third write operation by writing the third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

55. (Currently Amended) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on

the groups of data bits stored in the data storage element.

56. (Currently Amended) The DIMM of claim 49, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

57. (Currently Amended) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

58. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector, the edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections, wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
- (ii) generate a trigger signal upon detecting a trigger condition; and
- (iii) transmit the trigger signal to at least one other portion of the controller,

wherein the controller is configured to perform, in response to the trigger signal, one or more write operations to write data into the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via the first regulated voltage line;

a second component configured to receive power via the second regulated voltage line;

a third component configured to receive power via the third regulated voltage line; and

a fourth component electrically configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines;

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; and

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal.

59. (Currently Amended) The DIMM of claim 58, wherein when power from the power rails of the system board is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals

and eight 1-bit wide DDR error-correcting code (ECC) data signals; and
wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

60. (Currently Amended) The DIMM of claim 65, wherein the logic element is configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

61. (Currently Amended) The DIMM of claim 65, wherein the logic element is configured to perform, prior to the first and second write operations, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

62. (Currently Amended) The DIMM of claim 58, wherein when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

63. (Currently Amended) The DIMM of claim 58, when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

64. (Currently Amended) The DIMM of claim 63, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages.

65. (Currently Amended) The DIMM of claim 58, wherein the controller further

includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to wire a second set of data bits into a second portion of the data storage element.

66. (Currently Amended) The DIMM of claim 58, wherein each of the first, second, and third converter circuits is a buck converter.

67. (Currently Amended) The DIMM of claim 58, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

68. (Currently Amended) The DIMM of claim 63, wherein, when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.



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PETITION TO MAKE SPECIAL BASED ON AGE FOR ADVANCEMENT OF EXAMINATION UNDER 37 CFR 1.102(c)(1)

APPLICATION #	ATTORNEY DOCKET #	FILED ON
17582797	022955-000090	01/24/2022

In re Application of Chi-She Chen

This is a decision on the electronic petition under 37 CFR 1.102(c)(1), filed April 07, 2025 to make above-identified application special based on applicant's age as set forth in MPEP § 708.02, Section II.

The petition is **GRANTED**.

A grantable petition to make an application special under 37 CFR 1.102(c)(1), MPEP § 708.02, Section II:Applicant's

Age must include a statement by applicant or a registered practitioner having evidence that applicant is at least 65 years of age. No fee is required.

Accordingly, the above-identified application has been accorded "special" status and will be taken up for action by the examiner upon the completion of all pre-examination processing.

Telephone inquiries concerning this electronic decision should be directed to the Office of Petitions at 571-272-3282.

All other inquiries concerning either the examination or status of the application should be directed to the Technology Center.



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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
04/07/2025 04:33:33 PM Z ET

ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY Khaled Shami

PATENT CENTER # 69900618

FILING DATE 01/24/2022

CUSTOMER # 151145

FIRST NAMED
INVENTOR Chi-She Chen

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY -

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
petition-request.pdf	1	ePetition Request Form	29 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
petition-request.pdf	9B08C3FE87991DEF0EF284A91CDE4F7DE9663696B6FDA3D5 BA8CA884B367BB033E71A9E69F938200F112C0E1EFE3FD492 54251729346D2FE64FD17645BC57145

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

Samsung Electronics Co., Ltd.
Ex. 1002, p. 1498

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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**PETITION TO MAKE SPECIAL BASED ON AGE FOR ADVANCEMENT OF EXAMINATION
UNDER 37 CFR 1.102(c)(1)**

APPLICATION #
17582797

ATTORNEY DOCKET #
022955-000090

FILING DATE
01/24/2022

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

Confirmation
Number **3546**

Filing Date **01/24/2022**

Art Unit **2138**

First Named
Inventor **Chi-She Chen**

Examiner **HASHEM FARROKH**

Attention: Office of Petitions

An application may be made special for advancement of examination upon filing of a petition showing that the applicant is 65 years of age, or more. No fee is required with such a petition. See 37 CFR 1.102(c)(1) and MPEP 708.02 (II).

APPLICANT HEREBY PETITIONS TO MAKE SPECIAL FOR ADVANCEMENT OF EXAMINATION IN THIS APPLICATION UNDER 37 CFR 1.102(c)(1) and MPEP 708.02 (II) ON THE BASIS OF THE APPLICANT'S AGE.

A grantable petition requires one of the following items:

- (1) Statement by one named inventor in the application that he/she is 65 years of age, or more; or
- (2) Certification by a registered attorney/agent having evidence such as a birth certificate, passport, driver's license, etc. showing one named inventor in the application is 65 years of age, or more.

Name of Inventor who is 65 years of age, or older

Given Name	Middle Name	Family Name	Suffix
Chi-She	—	Chen	—

Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office, and I certify that I am in possession of evidence, and will retain such in the application file record, showing that the inventor listed above is 65 years of age, or more.

Signature	Name	Registration #
/Khaled Shami/	Khaled Shami	38745



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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
04/17/2025 05:30:05 PM Z ET

ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY LISA MARGARET ELLIOTT

PATENT CENTER # 70056716

FILING DATE 01/24/2022

CUSTOMER # 151145

FIRST NAMED
INVENTOR Chi-She Chen

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Khaled Shami

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Supplemental Amendment.pdf	18	Supplemental Response or Supplemental Amendment	166 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
Supplemental Amendment.pdf	6E7E89AE824138B12BC9995CACC9EC517E5FC3DDB74ED010 D618177C95410DB41D1468C7CF32C4DA231D8BEF2D1F0844 319154BEE2B9EE4D8BD2B43781C447B5

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 1501

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 3546

APPLICATION NO: 17/582,797

ART UNIT: 2138

FILING DATE: January 24, 2022

EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT

Commissioner:

In further response to the final Office Action mailed January 24, 2025, Applicant submits the following Supplemental Amendment.

Listing of Claims begins on page **2**.

Remarks begin on page **29**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)
2. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM ~~are transferred~~ via the set of data conduits, and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

a second set of edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via at least the first regulated voltage line;

a second component configured to receive power via at least the second regulated voltage line;

a third component configured to receive power via at least the third regulated voltage line; and

a fourth component ~~electrically~~ configured to receive power via at least the fourth regulated voltage line; ~~and~~

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth

regulated voltage lines; and

- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines;
- the at least 40 1-bit DDR data signals include at least 32 1-bit ~~wide~~ DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and

the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

3– 28. (Canceled)

29. (Previously Presented) The DIMM of claim 2, wherein the controller further includes:

a data storage element configured to store a plurality of data bits and a logic element

coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and wherein the write operation conducted by the controller in response to the trigger signal includes:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

30. (Previously Presented) The DIMM of claim 2, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.

31. (Previously Presented) The DIMM of claim 2, wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when power from the power rails of the system board is provided to the DIMM.

32. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations.

33. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.

34. (Previously Presented) The DIMM of claim 2, wherein, when power from the power

rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.

35. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

36. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

37. (Previously Presented) The DIMM of claim 2, wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.

38. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger signal, one or more read operations.

39. (Previously Presented) The DIMM of claim 38, wherein the logic element is configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

40. (Canceled)

41. (Previously Presented) The DIMM of claim 29, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a

transfer of the first and second sets of data bits into the data storage element via a second connection.

42. (Previously Presented) The DIMM of claim 29, wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.

43. (Previously Presented) The DIMM of claim 31, wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

44. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the

power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections,
and

a set of address and control lines electrically~~electrically~~ connected to the third set of edge connections;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
 - (ii) generate a trigger signal upon detecting a trigger condition; and
 - (iii) transmit the trigger signal to at least one other portion of the controller,
- wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via the first regulated voltage line;

a second component configured to receive power via the second regulated voltage line;

a third component configured to receive power via the third regulated voltage line; and

a fourth component ~~electrically~~ configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; ~~and~~

(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the at least 40 1-bit DDR data signals include 32 1-bit ~~wide~~ DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

45. (Previously Presented) The DIMM of claim 44, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.

46. (Canceled)

47. (Previously Presented) The DIMM of claim 45, wherein the logic element is configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.

48. (Previously Presented) The DIMM of claim 44, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

49. (Previously Presented) The DIMM of claim 47, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

50. (Previously Presented) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

51. (Previously Presented) The DIMM of claim 47, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

52. (Previously Presented) The DIMM of claim 44, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

53. (Currently Amended) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above ~~both the first and the second threshold voltages~~ a specified operating voltage.

54. (Previously Presented) The DIMM of claim 49, wherein the logic element is configured to perform the third write operation by writing the third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

55. (Previously Presented) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on the groups of data bits stored in the data storage element.

56. (Previously Presented) The DIMM of claim 49, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

57. (Previously Presented) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when

the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

58. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector, the edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections, wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit ~~wide~~-DDR data signal, and

wherein the set of data lines includes at least 72 data lines;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
 - (ii) generate a trigger signal upon detecting a trigger condition; and
 - (iii) transmit the trigger signal to at least one other portion of the controller,
- wherein the controller is configured to perform, in response to the trigger signal, one or more write operations to write data into the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

- a first component configured to receive power via the first regulated voltage line;
- a second component configured to receive power via the second regulated voltage line;
- a third component configured to receive power via the third regulated voltage line; and
- a fourth component ~~electrically~~ configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth

- regulated voltage lines; and
- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines;

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; and

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal, and

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the at least 40 1-bit ~~wide~~ DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

59. (Canceled)

60. (Previously Presented) The DIMM of claim 65, wherein the logic element is configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein

the third set of data bits includes the first and second set of data bits written during the first and second write operations.

61. (Previously Presented) The DIMM of claim 65, wherein the logic element is configured to perform, prior to the first and second write operations, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

62. (Previously Presented) The DIMM of claim 58, wherein when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

63. (Previously Presented) The DIMM of claim 58, when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

64. (Currently Amended) The DIMM of claim 63, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above ~~both the first and the second threshold voltages~~ a specified operating voltage.

65. (Previously Presented) The DIMM of claim 58, wherein the controller further includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to wire a second set of data bits into a second portion of the data storage element.

66. (Previously Presented) The DIMM of claim 58, wherein each of the first, second, and third converter circuits is a buck converter.

67. (Previously Presented) The DIMM of claim 586, wherein, when power is provided to

the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

68. (Previously Presented) The DIMM of claim 63, wherein, when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

REMARKS

The final Office Action mailed January 24, 2025, has been carefully considered.

Reconsideration in view of the following remarks is respectfully requested.

By this Amendment, Applicant has **amended claims 2, 44, 53, 58, and 64; and canceled claims 28, 46, and 59.**

Claims 2, 29-39 and 41-45, 47-58, and 60-68 are now pending and subject to examination.

Interview Record

Applicant gratefully acknowledges the courtesy and consideration extended to Applicant's undersigned representative and Mr. Richard Kim of Netlist, Inc. during the telephone interviews with Examiner Farrokh on April 10, 16 and 17, 2025.

During the interviews, support for the claim limitations, as well as prior art reference Harris (U.S. Publication No. 2006/0174140), were discussed. The instant Supplemental Amendment, which includes adding the limitations from dependent claims 28, 46, and 59 to the respective independent claims was proposed. No agreement was reached.

Canceled Claims

Claims 28, 46, and 59 have been canceled without prejudice or disclaimer of the subject matter contained therein.

Conclusion

Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Respectfully submitted,

Date: April 17, 2025
Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Customer No.: 151145
Tel: (202) 467-8800

/Khaled Shami/
Khaled Shami, Reg. No. 38,745

<i>Examiner-Initiated Interview Summary</i>	Application No. 17/582,797	Applicant(s) Chen et al.		
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (First Inventor to File) Status No	Page 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	Title	Type
HASHEM FARROKH	Primary Examiner	Telephonic
Khaled Shami	Attorney	

Date of Interview: 18 April 2025

Issues Discussed:

Other

Request for an examiner amendment to correct a minor error in the claim numbering. Examiner made a telephone call to to the applicant, Mr. Khaled Shami (Reg. # 38,745) to inform the Applicant that claims in Application 17/582,797 are in condition for allowance except for a minor claim dependency error. Examiner inquired whether the applicant is willing to amend (e.g., change the claim dependency) the dependent claim 67 depending from claim 586 to depend from claim 58 instead. Applicant agreed and authorized the Examiner to make the amendment (see accompanying notice of allowance).

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04 Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing	

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	

CPC						
Symbol					Type	Version
G06F	/	13	/	28	F	2013-01-01
G06F	/	12	/	0246	I	2013-01-01
G06F	/	13	/	1694	I	2013-01-01
G06F	/	1	/	185	I	2013-01-01
G06F	/	12	/	0638	I	2013-01-01
G06F	/	13	/	4243	I	2013-01-01
G11C	/	7	/	1072	I	2013-01-01
G11C	/	14	/	0018	I	2013-01-01
G06F	/	3	/	0613	I	2013-01-01
G06F	/	3	/	0659	I	2013-01-01
G06F	/	3	/	0685	I	2013-01-01
G06F	/	13	/	4027	I	2013-01-01
G06F	/	2212	/	205	A	2013-01-01
G06F	/	2212	/	7208	A	2013-01-01

CPC Combination Sets					
Symbol				Type	Set
	/		/		

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 38	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138 (Primary Examiner) _____ (Date) _____		19 April 2025 O.G. Print Claim(s) 2	O.G. Print Figure 6

Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G06F	/	13	/ 28
G06F	/	1	/ 18

NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
711	110

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	38	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	19 April 2025	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	2	6

Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☐ T.D.
 ☐ R.1.47

CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19		28	15	37		46	22	55	33	64
1	2		11		20	2	29	7	38	18	47	23	56	35	65
	3		12		21	11	30	8	39	25	48	28	57	38	66
	4		13		22	12	31		40	19	49	29	58	30	67
	5		14		23	3	32	9	41	20	50		59	34	68
	6		15		24	4	33	10	42	24	51	36	60		
	7		16		25	14	34	13	43	26	52	37	61		
	8		17		26	5	35	16	44	27	53	31	62		
	9		18		27	6	36	17	45	21	54	32	63		

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	38	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	19 April 2025	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	2	6

Search Notes 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

CPC - Searched*		
Symbol	Date	Examiner
G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/ 205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00	10/06/2022	HF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	110	10/06/2022	HF
711	110	11/01/2023	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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<i>Search Notes</i> 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search	10/06/2022	HF
EAST Text, CPC, FACET Search	10/06/2022	HF
IP Search	10/06/2022	HF
Google Search	10/06/2022	HF
Inventor/Assignee Search Updated	07/07/2023	HF
EAST Text, CPC, FACET Search Updated	07/07/2023	HF
Inventor/Assignee Search Updated	10/31/2023	HF
EAST Text, CPC, FACET Search Updated	10/31/2023	HF
Inventor/Assignee Search Updated	02/22/2024	HF
EAST Text, CPC, FACET Search Updated	02/22/2024	HF
Inventor/Assignee Search Updated	08/05/2024	HF
EAST Text, CPC, FACET Search Updated	08/05/2024	HF
Inventor/Assignee Search Updated	01/19/2025	HF
EAST Text, CPC, FACET Search Updated	01/19/2025	HF
Inventor/Assignee Search Updated	04/18/2025	HF
EAST Text, CPC, FACET Search Updated	04/18/2025	HF

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G06F3/0685	G06F3/00	04/18/2025	HF
G06F13/28	G06F13/00	04/18/2025	HF
G06F2212/205	G06F2212/00	04/18/2025	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L178	1	"17582797"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/04/18 01:25 PM
L179	1	"17582797"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/04/18 02:45 PM
L180	8	((plurality OR multiple OR several) SAME (((synchronous ADJ dynamic ADJ random ADJ access ADJ memory) OR SDRAM OR DDR\$1) near2 (devices OR chips OR dies)) SAME (coupled OR connected) SAME (regulated near2 voltage)))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/04/18 06:00 PM
L181	7	((((plurality OR multiple OR several) WITH (((synchronous ADJ dynamic ADJ random ADJ access ADJ memory) OR SDRAM OR DDR\$1) near2 (devices OR chips OR dies)) WITH (coupled OR connected) SAME (regulated near2 voltage))))).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/04/18 06:01 PM
L182	5	181 AND ("BHAKTA; JAYESH".ine. OR "CHEN; CHI-SHE".ine. OR "MILTON; SCOTT H.".ine. OR "SOLOMON; JEFFREY C.".ine.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/04/18 06:01 PM
L183	5	180 AND ("NETLIST, INC.".ase.)	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2025/04/18 06:03 PM
L184	8	180 AND ((G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/205 OR G06F2212/7208 OR	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/04/18 06:03 PM

		G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00).cpc. OR (711/110).ccls. OR (G06F1/18 OR G06F12/02 OR G06F12/06 OR G06F13/16 OR G06F13/28 OR G06F13/40 OR G06F13/42 OR G06F3/06 OR G11C14/00 OR G11C7/10).ipc.)					
L185	0	(group OR cluster OR multiple OR plurality OR pool) SAME ((double ADJ data ADJ rate) OR DDR) near2 (devices OR chips OR dies) SAME ((connected OR attached OR hav\$3 OR "same") near2 (chip ADJ select))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/04/18 06:12 PM
L186	0	(group OR cluster OR multiple OR plurality OR pool) SAME ((double ADJ data ADJ rate) OR DDR) near2 (devices OR chips OR dies) SAME ((connected OR attached OR hav\$3 OR "same") near2 (chip ADJ select))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2025/04/18 06:13 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

Bibliographic Data

Application No: 17/582,797

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged: /HASHEM FARROKH/

Examiner's Signature

Initials

Title:

MEMORY WITH ON-MODULE POWER MANAGEMENT

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
01/24/2022	711	2138	022955-000090
RULE			

APPLICANTS

Netlist, Inc., Irvine, CA, UNITED STATES

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Scott H. Milton, Irvine, CA, UNITED STATES

Jayesh Bhakta, Cerritos, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 17328019 05/24/2021 PAT 11232054

17328019 is a CON of 17138766 12/30/2020 PAT 11016918

17138766 is a CON of 15934416 03/23/2018ABN

15934416 is a CON of 14840865 08/31/2015 PAT 9928186

14840865 is a CON of 14489269 09/17/2014 PAT 9158684

14489269 is a CON of 13559476 07/26/2012 PAT 8874831

13559476 has PRO of 61512871 07/28/2011

13559476 is a CIP of 12240916 09/29/2008 PAT 8301833

12240916 is a CON of 12131873 06/02/2008ABN

12131873 has PRO of 60941586 06/01/2007

FOREIGN APPLICATIONS

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STATE OR COUNTRY

UNITED STATES

ADDRESS

Samsung Electronics Co., Ltd.
Ex. 1002, p. 1529

Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152
UNITED STATES

FILING FEE RECEIVED

\$1,980



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NOTICE OF ALLOWANCE AND FEE(S) DUE

151145 7590 04/28/2025
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

EXAMINER	
FARROKH, HASHEM	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 04/28/2025

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

TITLE OF INVENTION: MEMORY WITH ON-MODULE POWER MANAGEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1290	\$0.00	\$0.00	\$1290	07/28/2025

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

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151145 7590 04/28/2025
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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

TITLE OF INVENTION: MEMORY WITH ON-MODULE POWER MANAGEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1290	\$0.00	\$0.00	\$1290	07/28/2025

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2138	711-110000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546
151145	7590	04/28/2025	EXAMINER	
Vorys, Sater, Seymour and Pease LLP			FARROKH, HASHEM	
1909 K Street, NW				
9th Floor				
Washington, DC 20006-1152			ART UNIT	PAPER NUMBER
			2138	
DATE MAILED: 04/28/2025				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).

<https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf>

Routine uses of the information in this record may include disclosure to:

- 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
- 2) a federal, state, local, or international agency, in response to its request;
- 3) a contractor of the USPTO having need for the information in order to perform a contract;
- 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
- 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
- 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
- 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
- 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
- 9) the Office of Personnel Management (OPM) for personnel research purposes; and
- 10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Notice of Allowability	Application No. 17/582,797	Applicant(s) Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 04/17/2025.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 2,29-39,41-45,47-58 and 60-68 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov**.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____. 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☒ Interview Summary (PTO-413), Paper No./Mail Date. <u>04/18/2025</u> .	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
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/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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DETAIL ACTION

Notice of Pre-AIA or AIA Status

1. *The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.*

Continued Examination Under 37 CFR 1.114

2. *A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/24/2025 has been entered.*

Response to Remarks

3. *In the previous office action mailed 01/24/2025, the claims were rejected under the 35 USC 112, first paragraphs as not complying with the written description requirement. The Applicant has overcome the 112 rejection.*

Examiner's Amendment

4. *An Examiner initiated interview with Applicant, Mr. Khaled Shami (Reg. # 38,745), was conducted on 04/18/2025. The Examiner informed the Applicant*

that claims in Application 17/582,797 are in condition for allowance except for a minor claim dependency error. Examiner inquired whether the applicant is willing to amend (e.g., change the claim dependency) the dependent claim 67 depending from claim 586 to depend from claim 58 instead.

Applicant agreed and authorized the Examiner to make the amendment. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment. It must be submitted no later than the payment of the issue fee.

Please amend the claim 67 as follow:

Claim 67:

Line 1, replace "DIMM of claim 586" with --DIMM of claim 58--

Allowable Subject Matter

Claims 2, 29-39, 41-45, 47-58, and 60-67 are allowed.

6. The invention directed to a hybrid memory System comprising volatile memory sub-system (e.g., DDR SDRAM DIMM) and non-volatile memory system (e.g., NAND flash memory). The memory system interface to the host system via edge connectors having separate conduits assigned for data, address, and power lines. A first group of DDR SDRAM devices are selected/enabled to be access in parallel by a first chip select signal and a second group of DDR SDRAM devices are selected/enabled to be access in parallel by a second chip select signal. The

reason for allowance of the independent claim 2 are the following: in interpreting the pending claims, in light of the specification, the Examiner finds the claimed invention to be patentably distinct from the prior art of record. The prior art of record neither anticipates, nor renders obvious the recited combination as a whole, including the limitation of “wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and

- the at least 40 1-bit DDR data signals include 32 1-bit wide-DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.”

7. *Independent claims 29-39, 41-43, 45, 47-57, and 60-67 are allowable at least for reasons recited above including all the limitations of the allowable independent base claim upon which they depend..*

8. *Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."*

Conclusion

9. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.*

11. *If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Tim Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.*

12. *Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. For questions regarding access to the Private PAIR system,*

contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786- 9199 (IN USA OR CANADA) or 571-272-1000.

***/HASHEM FARROKH/
Primary Examiner, Art Unit 2138***

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/582,797	Filing Date 01/24/2022	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *		x \$100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *		x \$480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	05/19/2025	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	* 47	Minus	** 42	= 5	x \$200 =	1000
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	x \$600 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	1000
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE	
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/TAWANA E CAMPBELL/	
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".							
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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ELECTRONIC PAYMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
05/19/2025 04:45:58 PM Z ET

ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY LISA MARGARET ELLIOTT

PATENT CENTER # 70486857

AUTHORIZED BY Khaled Shami

CUSTOMER # 151145

FILING DATE 01/24/2022

CORRESPONDENCE ADDRESS -

FIRST NAMED INVENTOR Chi-She Chen

Payment Information

PAYMENT METHOD
DA / 220585

PAYMENT TRANSACTION ID
E20255IG46339020

PAYMENT AUTHORIZED BY
LISA MARGARET ELLIOTT

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
1202	EACH CLAIM IN EXCESS OF 20	200.00	5	1000.00
1820	REQUEST FOR CONTINUED EXAMINATION (RCE)- 2ND AND SUBSEQUENT REQUEST (SEE 37 CFR 1.114)	2860.00	1	2860.00
TOTAL AMOUNT:				\$3,860.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

Samsung Electronics Co., Ltd.
Ex. 1002, p. 1542

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

Application Number	17582797	Filing Date	2022-01-24	Docket Number (if applicable)	022955-000090	Art Unit	2138
First Named Inventor	CHEN			Examiner Name	FARROKH		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
Deposit Account No 220585

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2025-05-19
Name	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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www.uspto.gov**ELECTRONIC ACKNOWLEDGEMENT RECEIPT**APPLICATION #
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022955-000090**Title of Invention**

MEMORY WITH ON-MODULE POWER MANAGEMENT

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under 35 USC 111(a)

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CONFIRMATION # 3546

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Documents**TOTAL DOCUMENTS: 2**

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Amendment and RCE after Allowance.pdf	18	Amendment Submitted/Entered with Filing of Continued Prosecution Application (CPA)/Request for Continued Examination(RCE)	167 KB
RCE - 022955-90.pdf	3	Request for Continued Examination (RCE)	1631 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
Amendment and RCE after Allowance.pdf	4B69A59336605C9F08BEFEBBA2CD1A642035A0EC71827E79F B21DC7AE94FB3E81E0BD463ADC78E64EDD075C1E5485A440

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Ex. 1002, p. 1547

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RCE - 022955-90.pdf

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AC7B5AF126C8785CB2F1A5A996955CF228F28B2D2E16899AB
F28A6B3FC5F5DF8FB3DD3F67C93185E8

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 3546

APPLICATION NO: 17/582,797

ART UNIT: 2138

FILING DATE: January 24, 2022

EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

Mail Stop RCE

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Submission Under 37 CFR § 1.313 of Amendment and RCE

After Allowance and Prior to Payment of Issue Fee

Commissioner:

Applicant gratefully acknowledges the issuance of the Notice of Allowance of April 28, 2025. Applicant respectfully submits under 37 CFR § 1.313 the instant Amendment and Request for Continued Examination after allowance and prior to payment of the Issue Fee.

Listing of Claims begins on page **2**.

Remarks begin on page **18**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)
2. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

a second set of edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via at least the first regulated voltage line;

a second component configured to receive power via at least the second regulated voltage line;

a third component configured to receive power via at least the third regulated voltage line; and

a fourth component configured to receive power via at least the fourth regulated voltage line;

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, ~~and~~

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each configured to receive ~~connected to a first chip select line configured to electrically conduct~~ a first chip select signal;

a second group of at least four DDR SDRAM devices that are each configured to receive ~~connected to a second chip select line configured to electrically conduct~~ a second chip select signal; ~~and~~

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least ~~[[40]]~~32 1-bit DDR data signals in parallel via at least ~~[[40]]~~32 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via ~~[[the]]~~an integer number of data lines of the set of data lines;
- ~~the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error correcting code (ECC) data signals; and~~

wherein the sum of the at least ~~[[40]]~~32 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least ~~[[72]]~~64 data conduits.

3– 28. (Canceled)

29. (Previously Presented) The DIMM of claim 2, wherein the controller further includes:

a data storage element configured to store a plurality of data bits and a logic element

coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and wherein the write operation conducted by the controller in response to the trigger signal includes:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

30. (Previously Presented) The DIMM of claim 2, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.

31. (Previously Presented) The DIMM of claim 2, wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when power from the power rails of the system board is provided to the DIMM.

32. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations.

33. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.

34. (Previously Presented) The DIMM of claim 2, wherein, when power from the power

rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.

35. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

36. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

37. (Previously Presented) The DIMM of claim 2, wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.

38. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger signal, one or more read operations.

39. (Previously Presented) The DIMM of claim 38, wherein the logic element is configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

40. (Canceled)

41. (Previously Presented) The DIMM of claim 29, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a

transfer of the first and second sets of data bits into the data storage element via a second connection.

42. (Previously Presented) The DIMM of claim 29, wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.

43. (Previously Presented) The DIMM of claim 31, wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

44. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the

power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections,
and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
 - (ii) generate a trigger signal upon detecting a trigger condition; and
 - (iii) transmit the trigger signal to at least one other portion of the controller,
- wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via the first regulated voltage line;

a second component configured to receive power via the second regulated voltage line;

a third component configured to receive power via the third regulated voltage line; and

a fourth component configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines;

(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each configured to receive ~~connected to a first chip select line configured to electrically conduct~~ a first chip select signal;

a second group of at least four DDR SDRAM devices that are each configured to receive ~~connected to a second chip select line configured to electrically conduct~~ a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least ~~[[40]]~~32 1-bit DDR data signals in parallel via at least ~~[[40]]~~32 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via ~~[[the]]~~an integer number of data lines of the set of data lines; and

- ~~the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and~~

wherein the sum of the at least ~~[[40]]~~32 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least ~~[[72]]~~64 data conduits.

45. (Previously Presented) The DIMM of claim 44, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.

46. (Canceled)

47. (Previously Presented) The DIMM of claim 45, wherein the logic element is configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.

48. (Previously Presented) The DIMM of claim 44, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

49. (Previously Presented) The DIMM of claim 47, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

50. (Previously Presented) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element,

respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

51. (Previously Presented) The DIMM of claim 47, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

52. (Previously Presented) The DIMM of claim 44, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

53. (Previously Presented) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.

54. (Previously Presented) The DIMM of claim 49, wherein the logic element is configured to perform the third write operation by writing the third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

55. (Previously Presented) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on the groups of data bits stored in the data storage element.

56. (Previously Presented) The DIMM of claim 49, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

57. (Previously Presented) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

58. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector, the PCB ~~edge connections~~ including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections, wherein the set of data lines are electrically coupled to respective edge

connections of the second set of edge connection, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit DDR data signal, ~~and wherein the set of data lines includes at least 72 data lines;~~

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
- (ii) generate a trigger signal upon detecting a trigger condition; and
- (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, one or more write operations to write data into the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via the first regulated voltage line;

a second component configured to receive power via the second regulated voltage line;

a third component configured to receive power via the third regulated voltage line; and

a fourth component configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines;

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each configured to receive ~~connected to a first chip select line configured to electrically conduct~~ a first chip select signal; and

a second group of at least four DDR SDRAM devices that are each configured to receive ~~connected to a second chip select line configured to electrically conduct~~ a second chip select signal, and

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least ~~[[40]]~~32 1-bit DDR data signals in parallel via at least ~~[[40]]~~32 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via ~~[[the]]~~an integer number of data lines of the set of data lines; and
- ~~• the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error correcting code (ECC) data signals; and~~

wherein the sum of the at least ~~[[40]]~~32 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least ~~[[72]]~~64 data conduits.

59. (Canceled)

60. (Previously Presented) The DIMM of claim 65, wherein the logic element is configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

61. (Previously Presented) The DIMM of claim 65, wherein the logic element is configured to perform, prior to the first and second write operations, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

62. (Previously Presented) The DIMM of claim 58, wherein when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

63. (Previously Presented) The DIMM of claim 58, when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

64. (Previously Presented) The DIMM of claim 63, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.

65. (Previously Presented) The DIMM of claim 58, wherein the controller further includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to wire a second set of data bits into a second portion of the data storage element.

66. (Previously Presented) The DIMM of claim 58, wherein each of the first, second, and third converter circuits is a buck converter.

67. (Previously Presented) The DIMM of claim 58, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

68. (Previously Presented) The DIMM of claim 63, wherein, when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

69. (New) The DIMM of claim 2, wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output the integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines

70. (New) The DIMM of claim 69, wherein the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals.

71. (New) The DIMM of claim 69, wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

72. (New) The DIMM of claim 44, wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the

first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output the integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines

73. (New) The DIMM of claim 72, wherein the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals.

74. (New) The DIMM of claim 72, wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

75. (New) The DIMM of claim 58, wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output the integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines

76. (New) The DIMM of claim 75, wherein the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals.

77. (New) The DIMM of claim 75, wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

REMARKS

Applicant respectfully submits that the claims of the present application define patentable subject matter and should be passed to allowance.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant submission, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Respectfully submitted,

Date: May 19, 2025
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UNITED STATES PATENT AND TRADEMARK OFFICE

USPTO Automated Interview Request (AIR)

May 20 2025

This paper requesting to schedule and/or conduct an interview is appropriate because:

I have previously submitted an authorization for internet communications in a patent application. See form SB/0439.

Name(s) :

Khaled Shami

S-signature:

/Khaled Shami/

Registration Number:

38745

U.S. Application Number:

17582797

Confirmation Number:

3546

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Proposed Time of Interview:

5-28-2025 2:00 PM ET

Alternative Proposed Time(s) of Interview:

5-29-2025 2:00 PM ET

Alternative Proposed Time(s) of Interview:

5-30-2025 2:00 PM ET

Preferred Interview Type:

Telephonic

I am the applicant or applicant's representative for this application.

Topic for Discussion:

Newly-submitted amendment with RCE, prior art and support



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17/582,797

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Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
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CONFIRMATION # 3546

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CUSTOMER # 151145

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Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
Summary of Telephone Interview and Examiners Amendment.pdf	16	Applicant summary of interview with examiner	152 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
Summary of Telephone Interview and Examiners Amendment.pdf	013DCA47EE1919E1FD16C8DF9B1E8BF86701D73F49E1DF0B A11F13B344818ED9C07F360C6CE06B338A4F464E71F658C74 558CAE3598EB2FE0D452A0D1BAE489E

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Samsung Electronics Co., Ltd.
Ex. 1002, p. 1568

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 3546

APPLICATION NO: 17/582,797

ART UNIT: 2138

FILING DATE: January 24, 2022

EXAMINER: FARROKH, Hashem

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT

SUMMARY OF TELEPHONE INTERVIEW

On May 28, 2025, a telephone interview was conducted between Examiner Farrokh and Applicant's attorney of record, Mr. Khaled Shami, and Mr. Richard C. Kim, VP of IP strategy at Netlist, Inc. Applicant sincerely thanks Examiner Farrokh for his time and consideration during the interview.

During the interview, it was agreed that Examiner Farrokh would enter, by Examiner's Amendment, claim changes that were discussed in order to place the application in condition for allowance. The claim changes are shown below in a courtesy copy provided for the Examiner's convenience. Specifically, they include clarifying amendments to independent claims 2, 44 and 58, and cancellation, without prejudice or disclaimer, of dependent claims 69-77.

COURTESY COPY OF EXAMINER'S AMENDMENT FOR ALLOWANCE

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Canceled)
2. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

a second set of edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via at least the first regulated voltage line;

a second component configured to receive power via at least the second regulated voltage line;

a third component configured to receive power via at least the third regulated voltage line; and

a fourth component configured to receive power via at least the fourth regulated voltage line;

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth

regulated voltage lines; and

- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, ~~and~~

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are ~~each~~ configured to simultaneously receive a first chip select signal;

a second group of at least four DDR SDRAM devices that are ~~each~~ configured to simultaneously receive a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 32 1-bit DDR data signals in parallel via at least 32 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and

wherein the sum of the at least 32 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 64 data conduits.

3– 28. (Previously Canceled)

29. (Previously Presented) The DIMM of claim 2, wherein the controller further includes:

a data storage element configured to store a plurality of data bits and a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and wherein the write operation conducted by the controller in response to the trigger signal includes:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

30. (Previously Presented) The DIMM of claim 2, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.

31. (Previously Presented) The DIMM of claim 2, wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when power from the power rails of the system board is provided to the DIMM.

32. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations.

33. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.

34. (Previously Presented) The DIMM of claim 2, wherein, when power from the power rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.

35. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third

write operation, the logic element is configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

36. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

37. (Previously Presented) The DIMM of claim 2, wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.

38. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger signal, one or more read operations.

39. (Previously Presented) The DIMM of claim 38, wherein the logic element is configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

40. (Previously Canceled)

41. (Previously Presented) The DIMM of claim 29, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.

42. (Previously Presented) The DIMM of claim 29, wherein the data storage element is a

buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.

43. (Previously Presented) The DIMM of claim 31, wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

44. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections,

and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
 - (ii) generate a trigger signal upon detecting a trigger condition; and
 - (iii) transmit the trigger signal to at least one other portion of the controller,
- wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via the first regulated voltage line;

a second component configured to receive power via the second regulated voltage line;

a third component configured to receive power via the third regulated voltage

line; and

a fourth component configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines;
- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are ~~each~~ configured to simultaneously receive a first chip select signal;

a second group of at least four DDR SDRAM devices that are ~~each~~ configured to simultaneously receive a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 32 1-bit DDR data signals in parallel via at least 32 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and

wherein the sum of the at least 32 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 64 data conduits.

45. (Previously Presented) The DIMM of claim 44, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory

and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.

46. (Previously Canceled)

47. (Previously Presented) The DIMM of claim 45, wherein the logic element is configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.

48. (Previously Presented) The DIMM of claim 44, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

49. (Previously Presented) The DIMM of claim 47, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

50. (Previously Presented) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

51. (Previously Presented) The DIMM of claim 47, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

52. (Previously Presented) The DIMM of claim 44, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

53. (Previously Presented) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.

54. (Previously Presented) The DIMM of claim 49, wherein the logic element is configured to perform the third write operation by writing the third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

55. (Previously Presented) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on the groups of data bits stored in the data storage element.

56. (Previously Presented) The DIMM of claim 49, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

57. (Previously Presented) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

58. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector

including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector, the PCB including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections, wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit DDR data signal;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
- (ii) generate a trigger signal upon detecting a trigger condition; and

- (iii) transmit the trigger signal to at least one other portion of the controller,
wherein the controller is configured to perform, in response to the trigger signal,
one or more write operations to write data into the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

- a first component configured to receive power via the first regulated voltage line;

- a second component configured to receive power via the second regulated voltage line;

- a third component configured to receive power via the third regulated voltage line; and

- a fourth component configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines;

wherein the plurality of DDR SDRAM devices includes:

- a first group of at least five DDR SDRAM devices that are each configured to

simultaneously receive a first chip select signal; and

a second group of at least four DDR SDRAM devices that are ~~each~~ configured to simultaneously receive a second chip select signal, and

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 32 1-bit DDR data signals in parallel via at least 32 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and

wherein the sum of the at least 32 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 64 data conduits.

59. (Previously Canceled)

60. (Previously Presented) The DIMM of claim 65, wherein the logic element is configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

61. (Previously Presented) The DIMM of claim 65, wherein the logic element is configured to perform, prior to the first and second write operations, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

62. (Previously Presented) The DIMM of claim 58, wherein when power is provided to the

DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

63. (Previously Presented) The DIMM of claim 58, when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

64. (Previously Presented) The DIMM of claim 63, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.

65. (Previously Presented) The DIMM of claim 58, wherein the controller further includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to wire a second set of data bits into a second portion of the data storage element.

66. (Previously Presented) The DIMM of claim 58, wherein each of the first, second, and third converter circuits is a buck converter.

67. (Previously Presented) The DIMM of claim 58, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

68. (Previously Presented) The DIMM of claim 63, wherein, when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and
wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

69-77. (Previously Canceled)

Respectfully submitted,

Date: May 29, 2025

/Khaled Shami/

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Customer No.: 151145

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/582,797	Filing Date 01/24/2022	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x \$100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x \$480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED - PART II

	(Column 1)		(Column 2)	(Column 3)	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	06/03/2025		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total (37 CFR 1.16(i))	*	38	Minus	** 47	= 0
	Independent (37 CFR 1.16(h))	*	3	Minus	*** 3	= 0
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						0
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total (37 CFR 1.16(i))	*		Minus	**	=
	Independent (37 CFR 1.16(h))	*		Minus	***	=
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						Supervisory Prog. Sup. Spec.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/LISA E FULTON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".						
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION #
17/582,797

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022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY LISA MARGARET ELLIOTT

PATENT CENTER # 70715685

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CUSTOMER # 151145

FIRST NAMED
INVENTOR Chi-She Chen

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Khaled Shami

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
022955-000090 - Supplemental Amendment - 2025-06-03.pdf	17	Supplemental Response or Supplemental Amendment	164 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
022955-000090 - Supplemental Amendment - 2025-06-03.pdf	0968D5C8B7FFFE9674143900E478404E6D5EE1BDA3C3369F8 D4FB387AA6A651D940B8FAF9F50C75BF252683E5EF27641F0 D5A2C2AC93C943145839BB9045C103

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Samsung Electronics Co., Ltd.
Ex. 1002, p. 1587

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 3546

APPLICATION NO: 17/582,797

ART UNIT: 2138

FILING DATE: January 24, 2022

EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

Mail Stop RCE

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Supplemental Amendment and Examiner Interview Summary

Commissioner:

Applicant thanks Examiner Farrokh for his time and consideration extended to the undersigned representative and to Mr. Richard C. Kim, in-house counsel at Netlist, Inc., during the telephone interview conducted on June 2, 2025. During the interview, Examiner Farrokh indicated that two prior art references, 2004/0193777 (LaBerge) and 2004/0143773 (Chen) may be used to reject the currently pending claims, filed on May 19, 2025 (Submission Under 37 CFR § 1.313 of Amendment and RCE After Allowance and Prior to Payment of Issue Fee). Applicant argued there is no motivation to combine LaBerge or Chen with Harris to arrive at the claimed invention, and the combinations do not teach all limitations of the claims. No agreement was reached on these points.

However, Examiner Farrokh stated that if the claims were restored to their previously allowed form, as of April 17, 2025 (Supplemental Amendment), and allowed by the Examiner in the Notice of Allowance of April 28, 2025, then they would again be allowed. Without agreeing on the rejections, and solely to expedite prosecution of the present application to allowance, the claims are amended herein without prejudice or disclaimer, to restore the claims to their previously allowed form. Per the agreement reached during the telephone interview, Applicant respectfully requests the Examiner to promptly pass the application to allowance.

Listing of Claims begins on page 2.

Remarks begin on page 17.

AMENDMENT OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Canceled)
2. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

a second set of edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via at least the first regulated voltage line;

a second component configured to receive power via at least the second regulated voltage line;

a third component configured to receive power via at least the third regulated voltage line; and

a fourth component configured to receive power via at least the fourth regulated voltage line;

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, ~~and~~

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each ~~configured to receive~~ connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each ~~configured to receive~~ connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least ~~[[32]]~~40 1-bit DDR data signals in parallel via at least ~~[[32]]~~40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;
- the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least ~~[[32]]~~40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least ~~[[64]]~~72 data conduits.

3– 28. (Previously Canceled)

29. (Previously Presented) The DIMM of claim 2, wherein the controller further includes:

a data storage element configured to store a plurality of data bits and a logic element

coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and wherein the write operation conducted by the controller in response to the trigger signal includes:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

30. (Previously Presented) The DIMM of claim 2, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.

31. (Previously Presented) The DIMM of claim 2, wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when power from the power rails of the system board is provided to the DIMM.

32. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations.

33. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.

34. (Previously Presented) The DIMM of claim 2, wherein, when power from the power

rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.

35. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

36. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

37. (Previously Presented) The DIMM of claim 2, wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.

38. (Previously Presented) The DIMM of claim 29, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger signal, one or more read operations.

39. (Previously Presented) The DIMM of claim 38, wherein the logic element is configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

40. (Previously Canceled)

41. (Previously Presented) The DIMM of claim 29, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a

transfer of the first and second sets of data bits into the data storage element via a second connection.

42. (Previously Presented) The DIMM of claim 29, wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.

43. (Previously Presented) The DIMM of claim 31, wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

44. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the

power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections,
and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
 - (ii) generate a trigger signal upon detecting a trigger condition; and
 - (iii) transmit the trigger signal to at least one other portion of the controller,
- wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via the first regulated voltage line;

a second component configured to receive power via the second regulated voltage line;

a third component configured to receive power via the third regulated voltage line; and

a fourth component configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines;

(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each ~~configured to receive~~ connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each ~~configured to receive~~ connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least ~~[[32]]~~40 1-bit DDR data signals in parallel via at least ~~[[32]]~~40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and

- the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least ~~[[32]]~~40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least ~~[[64]]~~72 data conduits.

45. (Previously Presented) The DIMM of claim 44, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.

46. (Previously Canceled)

47. (Previously Presented) The DIMM of claim 45, wherein the logic element is configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.

48. (Previously Presented) The DIMM of claim 44, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

49. (Previously Presented) The DIMM of claim 47, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

50. (Previously Presented) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element,

respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

51. (Previously Presented) The DIMM of claim 47, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

52. (Previously Presented) The DIMM of claim 44, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

53. (Previously Presented) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.

54. (Previously Presented) The DIMM of claim 49, wherein the logic element is configured to perform the third write operation by writing the third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

55. (Previously Presented) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on the groups of data bits stored in the data storage element.

56. (Previously Presented) The DIMM of claim 49, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

57. (Previously Presented) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

58. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector, the PCB including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections, wherein the set of data lines are electrically coupled to respective edge

connections of the second set of edge connection, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit DDR data signal;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
 - (ii) generate a trigger signal upon detecting a trigger condition; and
 - (iii) transmit the trigger signal to at least one other portion of the controller,
- wherein the controller is configured to perform, in response to the trigger signal, one or more write operations to write data into the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via the first regulated voltage line;

a second component configured to receive power via the second regulated voltage line;

a third component configured to receive power via the third regulated voltage line; and

a fourth component configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines;

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each ~~configured to receive~~ connected to a first chip select line configured to electrically conduct a first chip select signal; and

a second group of at least four DDR SDRAM devices that are each ~~configured to receive~~ connected to a second chip select line configured to electrically conduct a second chip select signal, and

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least ~~[[32]]~~40 1-bit DDR data signals in parallel via at least ~~[[32]]~~40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and
- the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least ~~[[32]]~~40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least ~~[[64]]~~72 data conduits.

59. (Previously Canceled)

60. (Previously Presented) The DIMM of claim 65, wherein the logic element is configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

61. (Previously Presented) The DIMM of claim 65, wherein the logic element is configured to perform, prior to the first and second write operations, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

62. (Previously Presented) The DIMM of claim 58, wherein when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

63. (Previously Presented) The DIMM of claim 58, when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

64. (Previously Presented) The DIMM of claim 63, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.

65. (Previously Presented) The DIMM of claim 58, wherein the controller further includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to write a second set of data bits into a second portion of the data storage element.

66. (Previously Presented) The DIMM of claim 58, wherein each of the first, second, and third converter circuits is a buck converter.

67. (Previously Presented) The DIMM of claim 58, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

68. (Previously Presented) The DIMM of claim 63, wherein, when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

69-77. (Canceled)

REMARKS

Independent claims 2, 44 and 58 are amended herein to restore them to their previously allowed form, and with a correction of minor typographical error (“edge connections” replaced with “PCB”) as previously discussed with the Examiner. The amendments herein are made without prejudice or disclaimer and solely for the purpose of expediting prosecution of the present application to allowance. Per the agreement reached during the telephone interview on June 2, 2025, Applicant respectfully submits that the claims of the present application define patentable subject matter and should be passed to allowance.

Applicant does not believe that extensions of time are necessary. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585. Respectfully submitted,

Date: June 3, 2025
Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Customer No.: 151145
Tel: (202) 467-8800

/Khaled Shami/
Khaled Shami, Reg. No. 38,745

<i>Applicant-Initiated Interview Summary</i>	Application No. 17/582,797	Applicant(s) Chen et al.		
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (First Inventor to File) Status No	Page 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	Title	Type
HASHEM FARROKH	Primary Examiner	Telephonic
Khaled Shami	Attorney	
Richard C. Kim	Applicant Counsel	

Date of Interview: 02 June 2025

Issues Discussed:

35 U.S.C. 103

An Applicant initiated interview with Applicant, Mr. Khaled Shami (reg. # 38,745), was conducted on 06/02/2025. The purpose of interview was to discuss the amendment of independent claims in the communication filed on 05/19/2025. During the interview, Examiner indicated the prior art references of LaBerge (US 2004/0193777) and Chen (US 2004/0143773) teach or render obvious the newly added limitations. During the interview an agreement reached that, except for some minor amendment, if the claim restored to the previously allowed version submitted on 04/17/2025, the claims would be in condition for allowance.

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04 Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing	

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	

CPC						
Symbol					Type	Version
G06F	/	13	/	28	F	2013-01-01
G06F	/	12	/	0246	I	2013-01-01
G06F	/	13	/	1694	I	2013-01-01
G06F	/	1	/	185	I	2013-01-01
G06F	/	12	/	0638	I	2013-01-01
G06F	/	13	/	4243	I	2013-01-01
G11C	/	7	/	1072	I	2013-01-01
G11C	/	14	/	0018	I	2013-01-01
G06F	/	3	/	0613	I	2013-01-01
G06F	/	3	/	0659	I	2013-01-01
G06F	/	3	/	0685	I	2013-01-01
G06F	/	13	/	4027	I	2013-01-01
G06F	/	2212	/	205	A	2013-01-01
G06F	/	2212	/	7208	A	2013-01-01

CPC Combination Sets					
Symbol				Type	Set
	/		/		

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 38	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138 (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 2	O.G. Print Figure 6

Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G06F	/	13	/ 28
G06F	/	1	/ 18
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
711	110

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	38	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	05 June 2025	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	2	6

Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19		28	15	37		46	22	55	33	64
1	2		11		20	2	29	7	38	18	47	23	56	35	65
	3		12		21	11	30	8	39	25	48	28	57	38	66
	4		13		22	12	31		40	19	49	29	58	30	67
	5		14		23	3	32	9	41	20	50		59	34	68
	6		15		24	4	33	10	42	24	51	36	60		
	7		16		25	14	34	13	43	26	52	37	61		
	8		17		26	5	35	16	44	27	53	31	62		
	9		18		27	6	36	17	45	21	54	32	63		

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 38	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138 (Primary Examiner) _____ (Date) 05 June 2025		O.G. Print Claim(s) 2	O.G. Print Figure 6

Search Notes 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

CPC - Searched*		
Symbol	Date	Examiner
G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/ 205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00	10/06/2022	HF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	110	10/06/2022	HF
711	110	11/01/2023	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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<i>Search Notes</i> 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search	10/06/2022	HF
EAST Text, CPC, FACET Search	10/06/2022	HF
IP Search	10/06/2022	HF
Google Search	10/06/2022	HF
Inventor/Assignee Search Updated	07/07/2023	HF
EAST Text, CPC, FACET Search Updated	07/07/2023	HF
Inventor/Assignee Search Updated	10/31/2023	HF
EAST Text, CPC, FACET Search Updated	10/31/2023	HF
Inventor/Assignee Search Updated	02/22/2024	HF
EAST Text, CPC, FACET Search Updated	02/22/2024	HF
Inventor/Assignee Search Updated	08/05/2024	HF
EAST Text, CPC, FACET Search Updated	08/05/2024	HF
Inventor/Assignee Search Updated	01/19/2025	HF
EAST Text, CPC, FACET Search Updated	01/19/2025	HF
Inventor/Assignee Search Updated	04/18/2025	HF
EAST Text, CPC, FACET Search Updated	04/18/2025	HF
Inventor/Assignee Search Updated	06/05/2025	HF
EAST Text, CPC, FACET Search Updated	06/05/2025	HF

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G06F3/0685	G06F3/00	04/18/2025	HF
G06F13/28	G06F13/00	04/18/2025	HF
G06F2212/205	G06F2212/00	04/18/2025	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L200	0	(group OR pool OR cluster) SAME (least near5 five near5 DDR near5 SDRAM) near5 (devices OR chips OR dies) SAME (each near3 (connected OR attached)) near5 (chip ADJ select\$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2025/06/05 02:12 PM
L201	0	(group OR pool OR cluster) SAME ((plurality OR multiple OR pool) near5 DDR near5 SDRAM) near5 (devices OR chips OR dies) SAME (each near3 (connected OR attached)) near5 (chip ADJ select\$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2025/06/05 02:14 PM
L202	0	(group OR pool OR cluster) SAME ((rank OR bank) near5 DDR near5 SDRAM) near5 (devices OR chips OR dies) SAME (each near3 (connected OR attached)) near5 (chip ADJ select\$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2025/06/05 02:15 PM
L203	0	(five) SAME ((rank OR bank) near5 DDR near5 SDRAM) near5 (devices OR chips OR dies) SAME (each near3 (connected OR attached)) near5 (chip ADJ select\$3)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2025/06/05 02:37 PM
L204	17	(group OR pool OR cluster OR plurality OR two OR five) SAME ((double\$1data\$1rate OR DDR) near3 ((synchronous near3 dynamic near3 random near3 access near3 memory) OR SDRAM)) SAME (devices OR chips OR dies OR ASICs) SAME (simultaneously OR concurrently OR parallel) SAME (chip	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/06/05 02:39 PM

		near3 (select\$3 OR enabl\$3))					
L205	0	((group OR pool OR cluster OR plurality OR two OR five) SAME ((double\$1data\$1rate OR DDR) near3 ((synchronous near3 dynamic near3 random near3 access near3 memory) OR SDRAM)) SAME (devices OR chips OR dies OR ASICs) SAME (simultaneously OR concurrently OR parallel) SAME (chip near3 (select\$3 OR enabl\$3))).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/06/05 02:39 PM
L206	0	((first near5 second near5 third near5 fourth) OR (plurality OR multiple)) SAME (voltage near2 (converter OR regulator)) SAME ((coupled OR connected) near5 ((printed ADJ circuit ADJ board) OR PCB)) SAME (input near5 (voltage near5 supply near5 line))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/06/05 02:53 PM
L207	7	((plurality OR multiple OR several OR pool) SAME (((synchronous ADJ dynamic ADJ random ADJ access ADJ memory) OR SDRAM OR DDR\$1) near2 (devices OR chips OR dies)) SAME (coupled OR connected) SAME (regulated near2 voltage))).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/06/05 02:56 PM
L208	8	((plurality OR multiple OR several OR pool) SAME (((synchronous ADJ dynamic ADJ random ADJ access ADJ memory) OR SDRAM OR DDR\$1) near2 (devices OR chips OR dies)) SAME (coupled OR	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/06/05 02:56 PM

		connected) SAME (regulated near2 voltage)))					
L209	5	207 AND ("BHAKTA; JAYESH".ine. OR "CHEN; CHI-SHE".ine. OR "MILTON; SCOTT H.".ine. OR "SOLOMON; JEFFREY C.".ine.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/06/05 02:57 PM
L210	0	204 AND ("NETLIST, INC.".ase.)	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2025/06/05 02:59 PM
L211	5	208 AND ("NETLIST, INC.".ase.)	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2025/06/05 03:01 PM
L212	8	208 AND ((G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00).cpc. OR (711/110).ccls. OR (G06F1/18 OR G06F12/02 OR G06F12/06 OR G06F13/16 OR G06F13/28 OR G06F13/40 OR G06F13/42 OR G06F3/06 OR G11C14/00 OR G11C7/10).ipc.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2025/06/05 03:01 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

Bibliographic Data

Application No: 17/582,797

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged: /HASHEM FARROKH/

Examiner's Signature

Initials

Title:

MEMORY WITH ON-MODULE POWER MANAGEMENT

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
01/24/2022	711	2138	022955-000090
RULE			

APPLICANTS

Netlist, Inc., Irvine, CA, UNITED STATES

INVENTORS

Chi-She Chen, Walnut, CA, UNITED STATES

Jeffrey C. Solomon, Irvine, CA, UNITED STATES

Scott H. Milton, Irvine, CA, UNITED STATES

Jayesh Bhakta, Cerritos, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 17328019 05/24/2021 PAT 11232054

17328019 is a CON of 17138766 12/30/2020 PAT 11016918

17138766 is a CON of 15934416 03/23/2018ABN

15934416 is a CON of 14840865 08/31/2015 PAT 9928186

14840865 is a CON of 14489269 09/17/2014 PAT 9158684

14489269 is a CON of 13559476 07/26/2012 PAT 8874831

13559476 has PRO of 61512871 07/28/2011

13559476 is a CIP of 12240916 09/29/2008 PAT 8301833

12240916 is a CON of 12131873 06/02/2008ABN

12131873 has PRO of 60941586 06/01/2007

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

02/01/2022

STATE OR COUNTRY

UNITED STATES

ADDRESS

Samsung Electronics Co., Ltd.
Ex. 1002, p. 1615

Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152
UNITED STATES

FILING FEE RECEIVED

\$1,980



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NOTICE OF ALLOWANCE AND FEE(S) DUE

151145 7590 06/18/2025
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

EXAMINER	
FARROKH, HASHEM	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 06/18/2025

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

TITLE OF INVENTION: MEMORY WITH ON-MODULE POWER MANAGEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1290	\$0.00	\$0.00	\$1290	09/18/2025

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

151145 7590 06/18/2025
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

TITLE OF INVENTION: MEMORY WITH ON-MODULE POWER MANAGEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1290	\$0.00	\$0.00	\$1290	09/18/2025

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2138	711-110000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546
151145	7590	06/18/2025	EXAMINER	
Vorys, Sater, Seymour and Pease LLP			FARROKH, HASHEM	
1909 K Street, NW				
9th Floor			ART UNIT	
Washington, DC 20006-1152			PAPER NUMBER	
			2138	
DATE MAILED: 06/18/2025				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).

<https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf>

Routine uses of the information in this record may include disclosure to:

- 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
- 2) a federal, state, local, or international agency, in response to its request;
- 3) a contractor of the USPTO having need for the information in order to perform a contract;
- 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
- 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
- 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
- 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
- 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
- 9) the Office of Personnel Management (OPM) for personnel research purposes; and
- 10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Notice of Allowability	Application No. 17/582,797	Applicant(s) Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 06/03/2025.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 2,29-39,41-45,47-58 and 60-68. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov**.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____. | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material _____. | 7. ☐ Other _____. |
| 4. ☒ Interview Summary (PTO-413),
Paper No./Mail Date <u>06/02/2025</u> . | |

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

DETAIL ACTION

Notice of Pre-AIA or AIA Status

1. *The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.*

Continued Examination Under 37 CFR 1.114

2. *A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/19/2025 has been entered.*
3. *This office action is in response to claim amendment filed on 06/03/2025. There are a total 38 claims pending in the application. Claims 1, 3-27, 40, 46, 59, and 69-77 have been canceled; claims 2, 44, and 58 have been amended; and no new claims have been added.*

Response to Remarks

4. *Applicant's arguments have been fully considered and they are persuadable. Thus, pending claims 2, 29-39, 41-45, 47-58, and 60-67 are considered to be allowable (see also the attached interview summary).*

Allowable Subject Matter

5. Claims 2, 29-39, 41-45, 47-58, and 60-67 are allowed.

The invention directed to a hybrid memory system comprising volatile memory sub-system (e.g., DDR SDRAM DIMM) and non-volatile memory system (e.g., NAND flash memory). The memory system interface to the host system via edge connectors having separate conduits assigned for data, address, and power lines. A first group of DDR SDRAM devices are selected/enabled to be accessed in parallel by a first chip select signal and a second group of DDR SDRAM devices are selected/enabled to be accessed in parallel by a second chip select signal. The reason for allowance of the independent claim 2 are the following: in interpreting the pending claims, in light of the specification, the Examiner finds the claimed invention to be patentably distinct from the prior art of record. The prior art of record neither anticipates, nor renders obvious the recited combination as a whole, including the limitation of: "wherein each component of the set of components: (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and wherein the plurality of DDR SDRAM devices includes: a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode: the first group of DDR SDRAM

devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 32 1-bit DDR data signals in parallel via at least 32 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and wherein the sum of the at least 32 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 64 data conduits.”

Independent claims 44 and 58 include similar limitations as claim 1 and are allowed for the reasons recited above with respect to claim 1.

6. *Independent claims **29-39, 41-43, 45, 47-57, and 60-67** are allowable at least for reasons recited above including all the limitations of the allowable independent base claim upon which they depend.*

7. *Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”*

Conclusion

Art Unit: 2138

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Tim Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

UNITED STATES
PATENT AND TRADEMARK OFFICEP.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov**ELECTRONIC ACKNOWLEDGEMENT RECEIPT**APPLICATION #
17/582,797RECEIPT DATE / TIME
06/24/2025 04:13:28 PM Z ETATTORNEY DOCKET #
022955-000090**Title of Invention**

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application InformationAPPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY Lauren Siefke

PATENT CENTER # 71055701

FILING DATE 01/24/2022

CUSTOMER # 151145

FIRST NAMED
INVENTOR Chi-She ChenCORRESPONDENCE
ADDRESS -

AUTHORIZED BY Michael Messinger

Documents**TOTAL DOCUMENTS: 1**

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2025-06-24- Issue Fee - 022955-90.pdf	1	Issue Fee Payment (PTO-85B)	124 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2025-06-24- Issue Fee - 022955-90.pdf	193428BFD4E0867A974792662B9120D236478374F4BB5C929F C7F4AD3511B045665F1B197C6A651E46BCC1FE2F671777793 A998232A5BC77EF3CD4C547D7DA59

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 1626

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC PAYMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
06/24/2025 04:13:28 PM Z ET

ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY Lauren Siefke

PATENT CENTER # 71055701

AUTHORIZED BY Michael Messinger

CUSTOMER # 151145

FILING DATE 01/24/2022

CORRESPONDENCE ADDRESS -

FIRST NAMED INVENTOR Chi-She Chen

Payment Information

PAYMENT METHOD
DA / 220585

PAYMENT TRANSACTION ID
E20256NG14266729

PAYMENT AUTHORIZED BY
Lauren Siefke

PRE-AUTHORIZED ACCOUNT
220585

PRE-AUTHORIZED CATEGORY
37 CFR 1.16 (National application filing, search, and examination fees); 37 CFR 1.17 (Patent application and reexamination processing fees); 37 CFR 1.19 (Document supply fees); 37 CFR 1.20 (Post Issuance fees); 37 CFR 1.21 (Miscellaneous fees and charges)

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
1501	UTILITY ISSUE FEE	1290.00	1	1290.00
TOTAL AMOUNT:				\$1,290.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement

Samsung Electronics Co., Ltd.

Ex. 1002, p. 1628

Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

151145 7590 06/18/2025
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

TITLE OF INVENTION: MEMORY WITH ON-MODULE POWER MANAGEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1290	\$0.00	\$0.00	\$1290	09/18/2025

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2138	711-110000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Vorys, Sater, Seymour and Pease LLP

2 Khaled Shami

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE
NETLIST, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Irvine, California, UNITED STATES OF AMERICA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 220585

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Michael Messinger/

Date June 24, 2025

Typed or printed name Michael Messinger

Registration No. 37575

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	~~2135~~ 2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

U.S. PATENTS

[Remove](#)

Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
Change(s) applied to document, P.H./ 11/21/2023	1	10949339		2021-03-16	~~Netlist, Inc.~~ Lee et al.	
	2	10860506		2020-12-08	~~Netlist, Inc.~~ Lee et al.	
	3	10217523		2019-02-26	~~Netlist, Inc.~~ Lee et al.	
	4	10474595		2019-11-12	~~Netlist, Inc.~~ Lee	
	5	9858218		2018-01-02	~~Netlist, Inc.~~ Lee	
	6	7619912		2009-11-17	~~Netlist, Inc.~~ Bhakta et al.	
	7	11232054		2022-01-25	~~Netlist, Inc.~~ Chen et al.	
	8	8026405				

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2135
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
Change(s) applied to document, /P.H./ 11/21/2023	1	20190004985		2019-01-03	~~Netlist, Inc.~~ Lee et al.	
	2	20060174140		2006-08-03	Shaun Harris, et al.	
	3	20060080515		2006-04-13	~~LEFTHAND NETWORKS, INC.~~ Spiers et al.	
	4	20080238536		2008-10-02	~~ELPIDA MEMORY, INC.~~ Hayashi et al.	
	5	20100257304		2010-10-07	~~GOOGLE INC.~~ Rajan et al.	
	6	20100205470		2010-08-12	~~STEC, Inc.~~ Moshayedi et al.	
	7	20080101147		2008-05-01	Hossein Amidi	
	8	20070136523		2007-06-14	Randy Bonella, et al.	
	9	20090034354		2009-02-05	~~MICRON TECHNOLOGY, INC.~~ Resnick	

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FOREIGN PATENT DOCUMENTS

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2135
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

Change(s) applied to document 9 P.H./ 1/21/2023	9	6798709		2004-09-28	Sim et al. ~~Samsung Electronics Co., Ltd.~~	
	10	6856556		2005-02-15	Hajeck ~~Silicon Systems, Inc.~~	
	11	7023187		2006-04-04	Shearon et al. ~~Interoil Americas Inc.~~	
	12	7692938		2010-04-06	Petter ~~Northern Power Systems, Inc.~~	
	13	5563839		1996-10-18	Herd et al. ~~Sintel Corporation~~	
	14	6693840		2004-02-17	Matsushita Electric Industrial Co., Ltd. Shimada et al.	
	15	7061214		2006-06-13	Mayega et al. ~~Texas Instruments Incorporated~~	
	16	5630096		1997-05-13	Microunity Systems Engineering, Inc. Zuravleff et al.	
	17	10672458		2020-06-02	Shaeffer et al. ~~Rambus Inc.~~	
	18	6067241		2000-05-23	Lu ~~International Power Devices, Inc.~~	

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Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2135 2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

U.S. PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
Change(s) applied to document, P.H./ 11/21/2023	1	11016918		2021-05-25	~~Netlist, Inc.~~ Chen et al.	
	2	8301833		2012-10-10	~~Netlist, Inc.~~ Chen et al.	
	3	8874831		2014-10-28	~~Netlist, Inc.~~ Lee et al.	
	4	9158684		2015-10-13	~~Netlist, Inc.~~ Lee et al.	
	5	9928186		2018-03-27	~~Netlist, Inc.~~ Lee et al.	
	6	7724604		2010-05-25	~~SMART Modular Technologies, Inc.~~ Amidi et al.	
	7	7719866		2010-05-18	~~Agence Spatiale Europeenne~~ Boldo	
	8	7721130		2010-05-18	~~Qimonda AG~~ Prete et al.	

**POWER OF ATTORNEY TO PROSECUTE APPLICATIONS
BEFORE THE USPTO**

I hereby revoke all previous powers of attorney given in the application identified with this filing or in the attached statement under 37 CFR 3.73(c):

I hereby appoint: Practitioner(s) associated with the Customer Number: **207012**

Please change the correspondence address for the application identified with this filing or in the attached statement under 37 CFR 3.73(c) to:

The address associated with the above-mentioned Customer Number: **207012**

Applicant Name and Address:

NETLIST, INC
111 Academy Way, Suite 100
Irvine, California 92617
UNITED STATES OF AMERICA

Signature of Applicant

The individual whose signature and title is supplied below is authorized to act on behalf of the Applicant

Signature Rich Kim Date 6-10-25

Name Richard Kim Telephone 949-679-0124

Title Vice President of Intellectual Property Strategy



UNITED STATES
PATENT AND TRADEMARK OFFICE

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Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
06/30/2025 05:37:59 PM Z ET

ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3546	FILED BY	LISA MARGARET ELLIOTT
PATENT CENTER #	71153942	FILING DATE	01/24/2022
CUSTOMER #	151145	FIRST NAMED INVENTOR	Chi-She Chen
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Khaled Shami

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA Netlist 207012_Signed 6-10-2025.pdf	1	Power of Attorney	34 KB
022955-90 - X - 17582797 - 3546 - aia373c.pdf	3	Assignee showing of ownership per 37 CFR 3.73	123 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
POA Netlist 207012_Signed 6- 10-2025.pdf	794914ECA68B16D47E940FE5C960FC376FED75D1292CB1BD 108E048FFBCB9D8F03676352EA6A89A9CEC04C3AF466E9DA F8C4095511687C78D450D575127E6109
022955-90 - X - 17582797 -	9092C7E5045AA0F5194AA6BE68E3148937A705274261951705

Samsung Electronics Co., Ltd.
Ex. 1002, p. 1636

3546 - aia373c.pdf

2D2EA9FE612DDFFB27AB3EE1557BEE2E75A874A07DEB3FF3
CF607FCE16DFDB00563C934BFFB356

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no person is required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: NETLIST, INC.Application No./Patent No.: 17/582,797 Filed/Issue Date: 01-24-2022Titled: MEMORY WITH ON-MODULE POWER MANAGEMENTNETLIST, INC., a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 034531, Frame 0385, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Samsung Electronics Co., Ltd.

Ex. 1002, p. 1638

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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4. From: _____ To: _____

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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).



As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Khaled Shami/

Signature

Khaled Shami

Printed or Typed Name

June 30, 2025

Date

38745

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/582,797	01/24/2022	Chi-She Chen	022955-000090

CONFIRMATION NO. 3546

151145
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

POWER OF ATTORNEY NOTICE



OC000000091067886

Date Mailed: 07/08/2025

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/30/2025.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/ytdemisse/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/582,797	01/24/2022	Chi-She Chen	022955-000090

CONFIRMATION NO. 3546

POA ACCEPTANCE LETTER



OC000000091067901

207012
Netlist Inc.
1909 K St., NW
9th Floor
Washington, DC 20006-1152

Date Mailed: 07/08/2025

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/30/2025.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	07/29/2025	12373366	022955-000090	3546

207012 7590 07/16/2025
Netlist Inc.
1909 K St., NW
9th Floor
Washington, DC 20006-1152

ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at <https://patentcenter.uspto.gov/>. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at <https://certifiedcopycenter.uspto.gov/index.html>. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (<https://patentcenter.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PATENT CENTER site <https://patentcenter.uspto.gov> for additional inventors):

Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott H. Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

APPLICANT(s) (Please see PATENT CENTER site <https://patentcenter.uspto.gov> for additional applicants):

Netlist, Inc., Irvine, CA;

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546
207012	7590	07/29/2025	EXAMINER	
Netlist Inc. 1909 K St., NW 9th Floor Washington, DC 20006-1152			FARROKH, HASHEM	
			ART UNIT	PAPER NUMBER
			2138	
			NOTIFICATION DATE	DELIVERY MODE
			07/29/2025	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

frubio@netlist.com
rkim@netlist.com
vorys_docketing@cardinal-ip.com



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APPLICATION NO.	ISSUE DATE	PATENT NO.
17/582,797	29-Jul-2025	12373366

Netlist Inc.
1909 K St., NW
Washington, DC 20006-1152

EGRANT NOTIFICATION

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The electronic patent grant is the official patent grant under 35 U.S.C. 153. For more information, please visit <https://www.uspto.gov/electronicgrants>