

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMART MODULAR TECHNOLOGIES INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2014-01370
Patent 8,301,833 B1

Before: LINDA M. GAUDETTE, BRYAN F. MOORE, and
GEORGIANNA W. BRADEN, *Administrative Patent Judges*.

MOORE, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Smart Modular Technologies Inc. (“Petitioner”) filed a Corrected Petition requesting an *inter partes* review of claims 1–30 of US Patent No. 8,301,833 B1 (Ex. 1009, “the ’833 patent”). Paper 8 (“Pet.”). Netlist, Inc. (“Patent Owner”) filed a Preliminary Response. Paper 11 (“Prelim. Resp.”).

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if “the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Pursuant to 35 U.S.C. § 314, the Board does not find a reasonable likelihood that Petitioner would prevail with respect to at least one claim of the ’833 patent and, thus, does not authorize an *inter partes* review to be instituted as to those claims.

A. Related Proceedings

Petitioner recites the District Court proceedings related to this *inter partes* review. Pet. 2–3. This *inter partes* review challenges the same patent at issue in the decision entered in IPR2014-00994 in which we denied institution. IPR2014-00994 (Paper 8).

B. The ’833 Patent

The invention in the ’833 patent relates to a specific configuration of hybrid memory systems that addresses non-volatile memory backup while running the volatile memory subsystem at lower power, and, therefore, at lower clock speeds. Ex. 1001, col. 16, ll. 29–34. Specifically, the alleged invention of the ’833 patent includes circuitry for providing a regular high-speed clock frequency (first clock frequency) during communications between the host and the volatile memory subsystem, and a slower clock frequency during communications between the volatile memory subsystem (using a third clock frequency) and the non-volatile memory subsystem (using a second clock frequency). *Id.* at col. 21, ll. 5–21. Further, the second and third clock frequencies may be substantially equal. *Id.* at col. 21,

ll. 23–24.

C. Illustrative Claim

Of the challenged claims, 1 and 5 are independent claims. Claim 1 is illustrative of the claimed subject matter of the '833 patent, and is reproduced below:

1. A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:

operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;

operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem; and

operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

D. Prior Art Relied Upon

Petitioner relies upon the following prior art references:

Reference	Patent Number	Exhibit Number
Fukuzo '295Pub	US 2006/0294295 A1	Ex. 1012
Leete '210Pub	US 2004/0190210 A1	Ex. 1013
Ichikawa '142	US 7,600,142 B2	Ex. 1014
Long '552	US 7,421,552 B2	Ex. 1015
Tsunoda '618	US 7,062,618 B2	Ex. 1016

E. The Asserted Grounds

Petitioner asserts that the challenged claims are unpatentable based on the following grounds:

Reference[s]	Basis	Claims Challenged
Fukuzo '295Pub	§ 102	1, 2, 4, 6–13, 15, 16, 18, 20, and 22–29 ¹
Fukuzo '295Pub and Leete '210Pub	§ 103	3, 5, 14, 17, 19, 21 and 30
Ichikawa '142	§ 102	1, 2, 7, 8, 11–13, 15, 18, 23, 24 and 27–29
Ichikawa '142 and Leete '210Pub	§ 103	3–6, 9, 10, 14, 16, 17, 19–22, 25, 26, and 30
Long '552	§ 102	1, 2, 4, 5, 7, 12, 13, 15, 18, 20, 21, 23, 28, and 29 ²

¹ We note the challenged claims are listed at page 6 of the Petition. Also, analysis is provided starting at page 26 of the Petition. Although Claim 16 is not listed, analysis provided at page 29 of the Petition.

² We note the Petition isn't consistent. The challenged claims are listed as 1, 2, 4, 5, 12, 13, 15, 18, 20, 21, 28, and 29. Pet. 7. Nonetheless, analysis

Reference[s]	Basis	Claims Challenged
Long '552 and Leete '210Pub	§ 103	3, 6–11, 14, 16, 17, 19, 22–27, and 30
Tsunoda '618	§ 102	1, 2, 4, 5, 12, 13, 15, 16, 18, 20, 21, 28, and 29
Tsunoda '618 and Leete '210Pub	§ 103	3, 6–11, 14, 16, 17, 19, 22–27, and 30

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner and Patent Owner propose constructions for several terms. Pet. 19–24; Prelim Resp. 15–21. We determine that none of the terms cited by the parties require explicit construction for the purpose of this Decision.

provided for claims 1, 2, 4, 5, 7, 12, 13, 15, 18, 20, 21, 23, 28, and 29. See Pet. 43–44.

B. Claims 1, 2, 4, 6–13, 15, 16, 18, 20, and 22–29—Anticipation by Fukuzo '295Pub (Ex. 1013)

Petitioner argues that claims 1, 2, 4, 6–13, 15, 16, 18, 20, and 22–29 are anticipated by Fukuzo '295Pub under 35 U.S.C. § 102(b). Pet. 24–30. Fukuzo '295Pub discloses an SDRAM memory chip device that comprises a non-volatile memory controller operating a nonvolatile memory and a FIFO memory. Ex. 1013, Abstract, ¶ 27. Fukuzo '295Pub's SDRAM memory chip device is used to store data to its internal SDRAM memory array (volatile memory) and to external FLASH (nonvolatile memory) using at least two additional pins as compared with conventional SDRAM standard. *Id.* Two further pins reflecting the flash memory status provide appropriate issuance of load or store signals by the host. *Id.* Fukuzo '295Pub teaches using foreground and background operations such that read/write operations to volatile memory can occur simultaneously with read/write operations to non-volatile memory. *Id.*

Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend. Claim 1 recites “operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.” Claim 15 recites “the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency.” Figure 3 of Fukuzo

'295Pub is reproduced below.

FIG 3

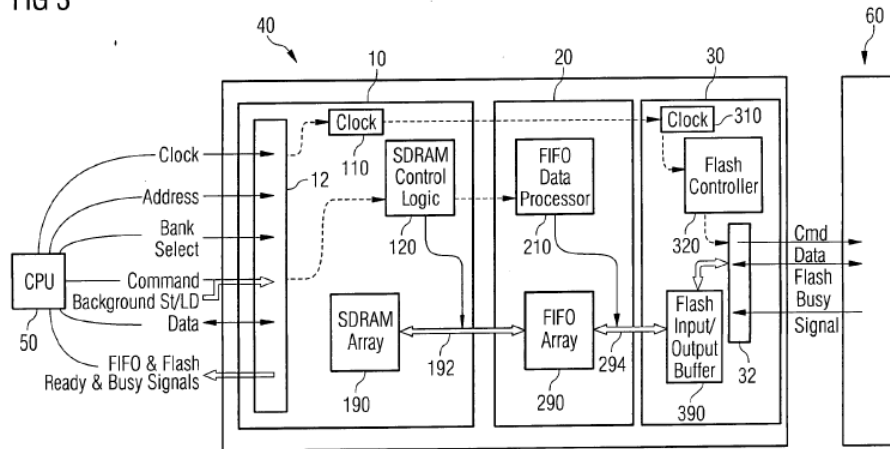


Figure 3, above, depicts a schematic block diagram of a memory chip device according to the invention of the Fukuzo '295Pub device.

Petitioner asserts that Fukuzo '295Pub's disclosure of FIFO Buffer 20 is the claimed volatile memory subsystem and Fukuzo '295Pub's disclosure that FIFO Buffer 20 operates at 130 MHz is the claimed first clock frequency. Pet. 25 (citing Ex. 1013 ¶¶ 84, 127). Further, Petitioner asserts that one of ordinary skill in the art would understand that FIFO Buffer 20 receives the same clock as the flash memory system (clocked at 20Mz) though FIFO timing generator 211, thus FIFO Buffer 20 meets the limitation to a third clock frequency. Pet. 14 (citing Ex. 1013 ¶¶ 84, 87–88). Petitioner's expert repeats this assertion without further explanation. Ex. 1010 ¶ 40. We are not persuaded by Petitioner's argument or cited disclosure.

Petitioner states, without explanation, that “the FIFO SDRAM buffer receives the same clock of the flash memory system, via the FIFO timing generator.” Pet. 25. However, the cited disclosure, other than for a line in

Figure 3 between FIFO Buffer 20 and FIFO timing generator 211, does not disclose explicitly that the FIFO timing generator 211 provides the flash clock signal to FIFO Buffer 20. At best, the cited disclosure states that there is “data transfer between the SDRAM FIFO memory array 290 and the flash memory input/output buffer 390 (second data transfer bus 294).” Ex. 1001 ¶ 103. Petitioner’s declarant, Dr. Nader Baghezadeh, does not provide any further explanation. Ex. 1010 ¶ 40. Petitioner does not explain sufficiently how or why FIFO timing generator 211 provides a clock signal that runs FIFO Buffer 20 at 20 MHz. See Prelim. Resp. 27.

Anticipation requires the disclosure in a single prior art reference of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1458 (Fed. Cir. 1984). We are not persuaded Petitioner has shown sufficiently that Fukuzo ’295Pub discloses the limitations to “operating the volatile memory subsystem at a third clock frequency . . . the third clock frequency being less than the first clock frequency” and “the volatile memory subsystem further being operable at a third clock frequency . . . the third clock frequency being less than the clock first frequency,” as recited in independent claims 1 and 15.

Thus, upon review of Petitioner’s analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood it would prevail with respect to claims 1 and 15, or claims 2, 4, 6–13, 16, 18, 20, and 22–29 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Fukuzo ’295Pub.

C. Claims 3, 5, 14, 17, 19, 21 and 30—Obviousness over Fukuzo '295Pub and Leete '210Pub (Ex.1013)

Petitioner argues that claims 3, 5, 14, 17, 19, 21 and 30 would have been obvious over Fukuzo '295Pub and Leete '210Pub under 35 U.S.C. § 103(a). Pet. 30–32. Claims 3, 5, 14, 17, 19, 21 and 30 depend from independent claims 1 and 15. As discussed above, Fukuzo '295Pub fails to teach or suggest all of the elements of independent claims 1 and 15. Petitioner does not assert that Leete '210Pub overcomes the aforementioned deficiency in Fukuzo '295Pub. Thus, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood it would prevail with respect to claims 3, 5, 14, 17, 19, 21 and 30, on the ground that these claims would have been obvious over Fukuzo '295Pub and Leete '210Pub.

D. Claims 1, 2, 7, 8, 11–13, 15, 18, 23, 24 and 27–29— Anticipated by Ichikawa '142 (Ex. 1014)

Petitioner argues that claims 1, 2, 7, 8, 11–13, 15, 18, 23, 24 and 27–29 are anticipated by Ichikawa '142 under 35 U.S.C. § 102(b). Pet. 32–35. Ichikawa '142 discloses a system including volatile memory RAM 13 and nonvolatile memory system combining serial input-output (SIO) 14 with external flash memory 30. Ex. 1014, 1:12–16, 1:23–25, 1:27–28, Fig 2. Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend.

Claim 1 recites “operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.” Claim 15 recites “the volatile memory subsystem further being

operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency.”

Petitioner asserts that Ichikawa ’142’s disclosure of RAM 13 as the volatile memory subsystem discloses a first clock frequency because Ichikawa ’142 “discloses that RAM 13 is clocked at 5 MHz during read and write operations with the CPU 11” and Ishikawa’s disclosure of RAM 13 as the volatile memory subsystem discloses a second clock frequency because Ichikawa ’142 “discloses that RAM [13] functions at the 1 MHz clock during operations with SIO and external flash memory.” Pet. 33 (citing Ex. 1014, 4:29–41, 55–61, 2:38–40, 3:50–56). The cited portions of Ichikawa ’142 recite: “the 5-MHZ clock signal CKH is supplied to the CPU 11” (Ex. 1014, 4:37–38); “[t]he CPU 11 carries out prescribed computation and control processing . . . in synchronization with a clock signal CLK” (*id.* at 3:50–53); “[n]ormally, the central processing unit operates on a first clock signal” (*id.* at 2:38–39); and

Operating on the 1-MHZ clock signal, the CPU 11 reads one byte of the data stored in the RAM 13 (step 44), supplies the data to the serial input-output interface 14 (step 45), and gives a serial transfer command (step 46). Also operating on the 1-MHZ clock signal, the serial input-output interface 14 converts the data received from the CPU 11 to serial data and transfers the data to the external memory device 30 (step 47).

id. at 4:55–61. We are not persuaded by this cited disclosure.

The cited disclosure states that CPU 11 is operating on either a 5 MHz clock signal or a 1 MHz clock signal. There is an underlying assumption in Petitioner’s argument that RAM 13 is clocked at the same speed as the CPU. Petitioner does not provide sufficient support for this

assumption. See Prelim. Resp. 44–45. Petitioner relies on its declarant, Dr. Bagherzadeh, for the proposition that “a POSITA would understand that the external flash memory and the RAM are communicating at the same frequency of 1 MHz to be able to transfer data between the components,” (Pet. 33–34 (citing Ex. 1010 (Bagherzadeh Decl.) ¶¶ 86, 87)), but Dr. Bagherzadeh provides no evidentiary support for this conclusory statement. We note that the ’833 patent shows explicitly that controller 62 provides a specific clock signal to the volatile and nonvolatile memory subsystems. Ex. 1001, 17:1–14, Fig. 7, 8. We are not persuaded Petitioner has shown sufficiently that Ichikawa ’142 discloses these limitations.

Therefore, upon review of Petitioner’s analysis and supporting evidence, we determine Petitioner has not demonstrated that there is a reasonable likelihood it would prevail with respect to claims 1 and 15, and claims 2, 7, 8, 11–13, 18, 23, 24 and 27–29 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Ichikawa ’142.

E. Claims 3–6, 9, 10, 14, 16, 17, 19–22, 25, 26, and 30—Obviousness over Ichikawa ’142 and Leete ’210Pub

Petitioner argues that claims 3–6, 9, 10, 14, 16, 17, 19–22, 25, 26, and 30 would have been obvious over Ichikawa ’142 and Leete ’210Pub under 35 U.S.C. § 103(a). Pet. 35–41. Claims 3–6, 9, 10, 14, 16, 17, 19–22, 25, 26, and 30 depend from independent claims 1 and 15. As discussed above, Ichikawa ’142 fails to teach or suggest all of the elements of independent claims 1 and 15. Petitioner does not assert that Leete ’210Pub overcomes the aforementioned deficiency in Ichikawa ’142. Thus, upon review of Petitioner’s analysis and supporting evidence, we determine that Petitioner has not demonstrated there is a reasonable likelihood it would prevail with

respect to claims 3–6, 9, 10, 14, 16, 17, 19–22, 25, 26, and 30, on the ground that these claims would have been obvious over Ichikawa '142 and Leete '210Pub.

*F. Claims 1, 2, 4, 5, 7, 12, 13, 15, 18, 20, 21, 23, 28, and 29—
Anticipation by Long '552 (Ex. 1015)*

Petitioner argues that claims 1, 2, 4, 5, 7, 12, 13, 15, 18, 20, 21, 23, 28, and 29 are anticipated by Long '552 under 35 U.S.C. § 102(b). Pet. 41–44. Long '552 discloses a system including volatile memory cache 42 and nonvolatile memory vault 44. Ex. 1015, 3:47–50. Further, Long '552 discloses that the device is configured to operate at a fast clock speed, supplied with 50 to 100 watts of power when communicating normally with the host. *Id.*, 4:46–53 and 3:50–59). Long '552 discloses that the device is configured to operate at a significantly slower clock speed, supplied with 30 watts of power when communicating with the non-volatile memory 44. *Id.* 4:54–61.

Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend. Claim 1 recites “operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.” Claim 15 recites “the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency.”

Petitioner asserts that Long '552's disclosure of controller 40³ as the volatile memory subsystem meets the limitation to a first clock frequency

³ We note that the Petition says “RAM 13,” but that's apparently a

because Long '552 discloses that the processing circuitry of controller 40 is clocked at a relatively fast clock signal supported by 50-100 watts of power during read and write operations with the host. Pet. 42. (citing Ex. 1015, 4:46–53; 3:50–59). The cited portion of Long '552 recites:

The clock generator circuit 46 is configured to provide a relatively-fast clock signal (or multiple clock signals) to the processing circuitry of the controller 40 during normal operation when the controller 40 is performing data storage operations on behalf of the set of hosts 22.

Ex. 1014, 4:46–51.

Petitioner asserts that Long '552 teaches a third clock frequency because “the flash memory vault is clocked at a significantly slower clock supported by less than 30 watts of power, which is applicable during read and write operations with the storage cache 42” and “one of ordinary skill would understand that since the available power is significantly less than during the host communication processes, the speed is significantly less for all the components in operation.” Pet. 42. (citing Ex. 1015, 4:54–61; Ex. 1010 ¶¶ 134–135). We are not persuaded by this cited disclosure.

The citation provided does not state that storage cache 42 or flash-based memory vault 44 is clocked at a relatively fast clock signal. Rather, the cited disclosure notes that the processing circuitry of the controller is running at a relatively high clock speed and then is run on a significantly slower clock speed at a later time. This disclosure is silent as to whether

typographical error because Long doesn't teach a RAM 13, and the cited section is about clock generator circuit 46 driving circuitry of controller 40 at “a relatively-fast clock signal (or multiple clock signals).”

storage cache 42 or flash-based memory vault 44 is running at the relatively high clock speed along with the controller. *See* Prelim. Resp. 48–49. Thus, it cannot be determined whether storage cache 42 or flash-based memory vault 44 is forced to run at a significantly lower clock speed when the available power is reduced. Petitioner does not provide objective evidence sufficient to support a finding that storage cache 42 must be necessarily clocked at the same speed as the controller. Additionally, the conclusory statements of Petitioner’s declarant that a “person of ordinary skill in the art would know from education and experience that the speed is proportional to the maximum power available to the components” and “since the available power is significantly less than during the host communication processes, the speed is significantly less for all the components in operation,” do not explain adequately how the this claim limitation is met. Ex. 1010 ¶ 134; *see also, e.g., In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) (“[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.” (citations omitted)); *Velandier v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) (“In giving more weight to prior publications than to subsequent conclusory statements by experts, the Board acted well within [its] discretion.”). For example, these statements in the Petition and Bagherzadeh declaration do not make clear whether clock speed being proportional to available power is always the case or whether anything in the Long reference teaches these alleged facts. Thus, we are not persuaded Petitioner has shown sufficiently that Long ’552 discloses these limitations.

Therefore, upon review of Petitioner’s analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a

reasonable likelihood that it would prevail with respect to claims 1 and 15, and claims 2, 4, 5, 7, 12, 13, 18, 20, 21, 23, 28, and 29 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Long '552.

G. Claims 3, 6–11, 14, 16, 17, 19, 22–27, and 30—Obviousness over Long '552 and Leete '210Pub

Petitioner argues that claims 3, 6–11, 14, 16, 17, 19, 22–27, and 30 would have been obvious over Long '552 and Leete '210Pub under 35 U.S.C. § 103(a). Pet. 44–50. Claims 3, 6–11, 14, 16, 17, 19, 22–27, and 30 depend from independent claims 1 and 15. As discussed above, Long '552 fails to teach or suggest all of the elements of independent claims 1 and 15. Petitioner does not assert that Leete '210Pub overcomes the aforementioned deficiency in Long '552. Thus, upon review of Petitioner's analysis and supporting evidence, we determine Petitioner has not demonstrated that there is a reasonable likelihood it would prevail with respect to claims 3, 6–11, 14, 16, 17, 19, 22–27, and 30, on the ground that these claims would have been obvious over Long '552 and Leete '210Pub.

H. Claims 1, 2, 4, 5, 12, 13, 15, 16, 18, 20, 21, 28, and 29—Anticipation by Tsunoda '618 (Ex. 1016)

Petitioner argues that claims 1, 2, 4, 5, 12, 13, 15, 16, 18, 20, 21, 28, and 29 are anticipated by Tsunoda '618 under 35 U.S.C. § 102(b). Pet. 50–54. Tsunoda '618 discloses a system including SDRAM volatile memory cache 4010 and flash non-volatile memory 4020. Ex. 1016, 4:2-6. Further, Tsunoda '618 discloses that the device is configured to operate the volatile memory 42 at a high SDRAM speed, when communicating normally with the host (*id.*, 13:51–53, 11:51–54, and 12:27–31). Tsunoda '618 discloses that the device is configured to operate at a speed different from the high

speed, when communicating with the non-volatile memory 44. *Id.* 12:21–25, 13:55–58, and 11:51–54.

Below we discuss independent claims 1 and 15, from which all other dependent claims challenged in this ground depend. Claim 1 recites “operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.” Claim 15 recites “the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency.”

Petitioner asserts that Tsunoda ’618’s disclosure of speed matching buffer 108 within the SDRAM discloses a first clock frequency. Pet. 51–52 (citing Ex. 1016, 11:51–54). We are not persuaded by this cited disclosure.

Petitioner apparently reads buffer 108 and SDRAM 103 on the volatile memory subsystem. However, speed matching buffer 108 is a part of memory control unit 104. Ex. 1016, Fig. 1. Reading the controller as the volatile memory subsystem is inconsistent with Tsunoda ’618’s disclosure that controller 62 is *separate from* the volatile and non-volatile memory subsystems. Ex. 1001, Fig. 1. Controller 62 provides the clock signal to the volatile and nonvolatile memory subsystems. Ex. 1001, Fig. 6. As Patent Owner points out, Petitioner does not explain sufficiently why the controller is a part of the volatile memory subsystem. See Prelim. Resp. 56–58. We find that one of ordinary skill at the time of the invention would not have considered reasonably Tsunoda ’618 as disclosing a volatile memory subsystem that operates at the first and third clock frequencies. Thus, , we

are not persuaded Petitioner has shown sufficiently that Tsunoda '618 discloses these limitations.

Therefore, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it would prevail with respect to claims 1 and 15, and claims 2, 4, 5, 12, 13, 16, 18, 20, 21, 28, and 29 that depend ultimately from claims 1 and 15, on the ground that these claims are anticipated by Tsunoda '618.

I. Claims 3, 6–11, 14, 17, 19, 22–27, and 30—Obviousness over Tsunoda '618 and Leete '210Pub

Petitioner argues that claims 3, 6–11, 14, 17, 19, 22–27, and 30 would have been obvious over Tsunoda '618 and Leete '210Pub under 35 U.S.C. § 103(a). Pet. 54–59. Claims 3, 6–11, 14, 17, 19, 22–27, and 30 depend from independent claims 1 and 15. As discussed above, Tsunoda '618 fails to teach or suggest all of the elements of independent claims 1 and 15. Petitioner does not assert that Leete '210Pub overcomes the aforementioned deficiency in Tsunoda '618. Thus, upon review of Petitioner's analysis and supporting evidence, we determine that Petitioner has not demonstrated that there is a reasonable likelihood that it would prevail with respect to claims 3, 6–11, 14, 17, 19, 22–27, and 30, on the ground that these claims would have been obvious over Tsunoda '618 and Leete '210Pub.

III. CONCLUSION

The information presented does not show that there is a reasonable likelihood that Petitioner would prevail at trial with respect to at least one claim of the '833 patent, based on any ground presented in the Petition. We deny the Petition for *inter partes* review of claims 1–30.

IV. ORDER

Accordingly, it is

ORDERED that that the Petition is *denied* as to all challenged claims,
and no trial is instituted.

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Patent 8,301,833 B1

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