UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner

Patent No. 11,232,054
Issued: January 25, 2022
Filed: May 24, 2021
Inventors: Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta

Title: Flash-DRAM Hybrid Memory Module

Inter Partes Review No. IPR2022-00999

DECLARATION OF DR. ANDREW WOLFE REGARDING U.S. PATENT NO. 11,232,054

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd. ("Samsung") as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 11,232,054 ("the 054 Patent") (Ex. 1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. My professional qualifications, experience, publications and presentations, and a listing of previous cases in which I have provided expert testimony are set forth in my CV, attached as Exhibit 1004.

3. I am the founder and sole employee of Wolfe Consulting. Through Wolfe Consulting, I provide technical and business analytics to businesses on processor technology, computer systems, consumer electronics, software, design tools, data security, cryptography and intellectual property issues. I have more than thirty years' experience developing products, researching, consulting, and teaching in those fields. In that time, I have worked as a computer architect, computer system designer, and as an executive in the PC and electronics business. I have also taught at some of the world's leading institutions in those fields, including

Stanford University, Princeton University, Carnegie Mellon University, and Santa Clara University.

4. In 1985, I earned the B.S.E.E. degree in Electrical Engineering and Computer Science from the Johns Hopkins University. In 1987, I received the M.S. degree in Electrical and Computer Engineering from Carnegie Mellon University and in 1992, I received the Ph.D. degree in Computer Engineering from Carnegie Mellon University. My doctoral dissertation proposed a new approach for the architecture of a computer processor.

5. I have more than 35 years of experience as a computer architect, computer system designer, personal computer graphics designer, educator, and executive in the electronics industry.

6. In 1983, I began designing touch sensors, microprocessor-based computer systems, and I/O (input/output) cards for personal computers as a senior design engineer for Touch Technology, Inc. During the course of my design projects with Technology, I designed I/O cards for PC-compatible computer systems, including the IBM PC-AT, to interface with interactive touch-based computer terminals that I designed for use in public information systems. I continued designing and developing related technology as a consultant to the Carroll Touch division of AMP, Inc., where in 1986 I designed one of the first custom touch-screen integrated circuits. I designed the touch/pen input system for

the Linus WriteTop, which many believe to be the first commercial tablet computer.

7. From 1986 through 1987, I designed and built a high-performance computer system as a student at Carnegie Mellon University. From 1986 through early 1988, I also developed the curriculum, and supervised the teaching laboratory, for processor design courses.

8. In the latter part of 1989, I worked as a senior design engineer for ESL-TRW Advanced Technology Division. While at ESL-TRW, I designed and built a bus interface and memory controller for a workstation-based computer system, and also worked on the design of a multiprocessor system.

9. At the end of 1989, I (along with some partners) reacquired the rights to the technology I had developed at Touch Technology and at AMP, and founded The Graphics Technology Company. Over the next seven years, as an officer and a consultant for The Graphics Technology Company, I managed the company's engineering development activities and personally developed dozens of touch screen sensors, controllers, and interactive touch-based computer systems.

10. I have consulted, formally and informally, for a number of fabless semiconductor companies. In particular, I have served on the technology advisory boards for two processor design companies: BOPS, Inc., where I chaired the board, and Siroyan Ltd., where I served in a similar role for three networking chip

companies – Intellon, Inc., Comsilica, Inc., and Entridia, Inc. – and one 3D game accelerator company, Ageria, Inc.

11. I have also served as a technology advisor to Motorola and to several venture capital funds in the U.S. and Europe. Currently, I am a director at Turtle Beach Corporation, providing guidance in its development of premium audio peripheral devices for a variety of commercial electronic products.

12. From 1991 through 1997, I served on the Faculty of Princeton University as an Assistant Professor of Electrical Engineering. At Princeton, I taught undergraduate and graduate-level courses in Computer Architecture, Advanced Computer Architecture, Display Technology, and Microprocessor Systems, and conducted sponsored research in the area of computer systems and related topics. From 1999 through 2002, I taught a Computer Architecture course to both undergraduate and graduate students at Stanford University multiple times as a Consulting Professor. At Princeton, I received several teaching awards, both from students and from the School of Engineering. I have also taught advanced microprocessor architecture to industry professionals in IEEE and ACM sponsored seminars. I am currently a lecturer at Santa Clara University teaching courses on Microprocessor Systems, Advanced Logic Design, Real-Time Computing, and Mechatronics. I teach about memory, including DDR SDRAM and flash memory,

in several of my classes and rely on the JEDEC specifications as industry standards.

13. From 1997 through 2002, I held a variety of executive positions at a publicly held fabless semiconductor company originally called S3, Inc. and later called Sonicblue Inc. I held the positions of Chief Technology Officer, Vice President of System Integration Products, Senior Vice President of Business Development, and Director of Technology, among others.

14. In the roles listed above, I worked with and managed architecture and design teams responsible for the development of SRAM and DRAM memories, graphics chip memory controllers, and CPU memory controllers. I also worked with memory vendors and memory standards bodies, directly and through my staff, on the development of memory technology and standards. I have been involved with interpreting and understanding JEDEC memory standards since at least 1997. For many years, I had a direct-report staff member who would attend JEDEC meetings and bring me both proposed and final standards for review and comment. I also have used proposed and final JEDEC standards for chips, modules, and protocols to guide product decisions and to facilitate technical discussions with corporate partners and with consulting clients. I supervised design teams that implemented memory controllers for successful commercial products that interoperated with JEDEC-compliant DDR memory chips and memory modules.

15. My teams also developed the Rio MP3 players and a music delivery platform and webstore backend service for selling music. In 1999, this music delivery system was spun out as a separate company called RioPort.com. I served on the RioPort.com board of directors and became involved in their product and technology strategy. I also managed engineering and marketing for the Rio product line for a period of time as an interim general manager. The Rio MP3 players were among the first consumer products to incorporate large quantities of NAND flash memory. I worked with CEOs and General Managers at several leading flash memory suppliers on strategic planning for the flash market. I also worked with my engineering teams to evaluate and implement flash memory protocols and select flash memory form factors. During my time at SonicBlue we launched more than 30 new consumer electronics products.

16. I served as a board member and technical advisor as KBGear Inc. from 1999-2001. KBGear Inc. designed and produced digital cameras and music players.

17. I have published more than fifty peer-reviewed papers in computer architecture and computer systems and IC design. I have also chaired IEEE and ACM conferences in microarchitecture and integrated circuit design and served as an associate editor for IEEE and ACM journals. I served on the IEEE Computer Society Awards committee. I am an IEEE Fellow and a Member of ACM. I am a

named inventor on at least fifty-seven U.S. patents and thirty-seven foreign patents.

18. I have been the invited keynote speaker at the ACM/IEEE International Symposium on Microarchitecture and at the International Conference on Multimedia. I have also been an invited speaker on various aspects of technology or the PC industry at numerous industry events including the Intel Developer's Forum, Microsoft Windows Hardware Engineering Conference, Microprocessor Forum, Embedded Systems Conference, Comdex, and Consumer Electronics Show as well as at the Harvard Business School and the University Illinois Law School. I have been interviewed on subjects related to technology and the electronics industry by publications such as the Wall Street Journal, New York Times, LA Times, Time, Newsweek, Forbes, and Fortune as well as CNN, NPR, and the BBC. I have also spoken at dozens of universities including MIT, Stanford, University of Texas, Carnegie Mellon, UCLA, University of Michigan, Rice University, and Duke University.

C. Compensation and Prior Testimony

19. I am being compensated at a rate of $600.00 per hour for my study and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

20. My CV, attached as Exhibit 1004, lists all other cases in which, during the previous 4 years, I have testified as an expert at trial or by deposition.

D. Information Considered

21. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Exhibit List at the end of this declaration.

22. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

23. My analysis of the materials produced in this matter is ongoing and I will continue to review any new materials as it is provided. This declaration represents only those opinions I have formed to date.

II. LEGAL STANDARDS FOR PATENTABILITY

24. In expressing my opinions and considering the subject matter of the claims of the 054 Patent, I am relying upon certain basic legal principles that have been explained to me.

25. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

26. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and generally includes patents and printed publications (*e.g.*, books, journal publications, articles on websites, product manuals, *etc*.).

27. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the 054 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

28. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

29. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

30. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. In this declaration I focus on "obviousness." My understanding of the legal standard for "obviousness" is set forth below.

31. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

32. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the asserted claims of the 054 Patent would have been considered obvious as of the priority date of the patent.

34. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

35. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

36. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being

associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors" suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

37. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

38. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a Skilled Artisan would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

39. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that does no more than yield predictable results, which are inferences and creative steps that a Skilled Artisan would employ.

40. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

41. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or

derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

42. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

43. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art

references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

44. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

45. I understand that a person of ordinary skill is also a person of ordinary creativity.

46. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was

obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE 054 PATENT

A. Effective Filing Date of the 054 Patent: No Earlier Than June 2, 2008

47. The 054 Patent is a continuation of, *inter alia*, a utility application filed December 30, 2020 ("766 Application") (Ex. 1013), and also claims priority to U.S. Provisional Application No. 60/941,586 ("586 Provisional Application") (Ex. 1005), filed June 1, 2007. Ex. 1001 (054 Patent), (63). The 766 Application has issued as U.S. Patent No. 11,016,918 ("918 Patent"). Ex. 1054 (918). The disclosure of the 054 Patent is nearly identical to the disclosure of the 918 Patent. As such, citations to the 054 Patent in this declaration apply equally to the 918 Patent and citations to the 918 Patent in this declaration apply equally to the 054 Patent. The 918 Patent is a continuation-in-part of a utility application, U.S. Patent Application No. 12/240,916 (Ex. 1007), filed September 29, 2008, which is a continuation of an abandoned utility application, U.S. Application No. 12/131,873 ("873 Application") (Ex. 1006), filed June 2, 2008.

48. In my opinion, as explained below, the effective filing date for the claims of the 054 Patent is no earlier than June 2, 2008 (the filing date of the 873 Application, Ex. 1006). In any event, all of the prior art I rely upon for my invalidity opinions predates June 1, 2007.

1. Several Limitations in All Claims Are Unsupported by the 586 Provisional Application Filed June 1, 2007

49. I have been asked to give my opinion as to whether, from the perspective of a Skilled Artisan, the 586 Provisional Application shows that the inventor actually invented what is claimed in each of the claims of the 054 Patent, and possessed the claimed subject matter, as of the provisional filing date of June 1, 2007. When considering that question, I have considered whether the 586 Provisional Application explicitly or inherently discloses the elements of the claims. To determine whether the provisional inherently discloses an element, I considered whether any element not explicitly disclosed would be necessarily comprehended in the description provided by a Skilled Artisan. I understand that the knowledge of ordinary artisans may be used to inform what is actually in the provisional, but not to teach limitations that are not in the provisional, even if those limitations would be rendered obvious by the disclosure in the provisional.

50. I conclude that certain elements of each claim in the 054 Patent is not adequately disclosed in the 586 Provisional Application, including but not limited to those discussed below.

a) Voltage Conversion Circuit Comprising Buck Converters – Claims 1, 16, 24

51. Each of independent claims 1, 16, and 24 include a limitation requiring "a voltage conversion circuit" which includes at least "three buck converters." Ex. 1001 (054 Patent), cls. 1, 16, 24.

52. There is no disclosure in the 586 Provisional Application of a voltage conversion circuit including at least three "buck converters." *See* Ex. 1005. A Skilled Artisan would have understood at the time that a "buck converter" refers to a certain type of dc-dc switch-mode converter which produces a lower (step-down) average output voltage than the input dc voltage. Ex. 1032 (Mohan) at pp. 161 and 164. Instead of a "buck converter," the 586 Provisional discloses a "step-down transformer 84" which "acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 32 and 3.0V to the non-volatile flash memory elements 42) during power down." Ex. 1005 at [0017].

53. A Skilled Artisan would have understood at the time that a "buck converter" is different from a "step-down transformer" described in the 586 Provisional. To the extent the term "transformer" is meant to cover changing the voltage by any means which produces a regulated voltage, a Skilled Artisan would have understood that a step-down regulated voltage can also be provided by means other than a "buck converter," e.g., by a linear regulator, such as a low-dropout

regulator (LDO). A Skilled Artisan would have understood that an LDO is different from the claimed "buck converter." *See, e.g.,* Ex. 1059 at 5:23-30 ("Switch mode buck converters have become popular due to two attractive features: first, they are more efficient than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, they can provide relatively high currents with lower power dissipation on chip than an LDO can.").

54. Thus, it is my opinion that Patent Owner cannot show that the 586 Provisional Application's disclosure supports the limitations of the "voltage conversion circuit" which includes at least "three buck converters" as recited in the independent claims of the 054 Patent.

b) Dual Buck Converter – Claim 15

55. Claim 15 includes a limitation requiring two buck converters to "operate as a dual buck converter." Ex. 1001 (054), cl. 15.

56. There is no disclosure in the 586 Provisional Application of buck converters or dual buck converters. *See* Ex. 1005.

57. Thus, it is my opinion that Patent Owner cannot show that the 586 Provisional Application's disclosure supports the limitations of a "dual buck converter" as recited in claim 15 of the 054 Patent.

c) Diodes – Claims 20, 22, 27, 28

58. Each of claims 20, 22, 27, and 28 include a limitation requiring a "first diode" or a "second diode." Ex. 1001 (054 Patent), cls. 20, 22, 27, and 28.

59. There is no disclosure in the 586 Provisional Application of diodes. *See* Ex. 1005.

60. Thus, it is my opinion that Patent Owner cannot show that the 586 Provisional Application's disclosure supports the limitations of a "first diode" or a "second diode" as recited in claims 20, 22, 27, and 28 of the 054 Patent.

B. Person of Ordinary Skill in the Art

61. Based on my experience and the prior art I discuss herein, I believe a person of ordinary skill in the art in the field of the 054 Patent in 2008 ("POSITA" or "Skilled Artisan") would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system,

including standard communication busses and protocols, such as PCI and SMBus busses and protocols. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers. Such a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry.

C. Overview of The 054 Patent

62. The 054 Patent states that it describes "a memory system having a volatile memory subsystem, a non-volatile memory subsystem, a controller coupled to the non-volatile memory subsystem, and a circuit coupled to the volatile memory subsystem, to the controller, and to a host system." Ex. 1001 (054 Patent) at 8:1-5. The 054 Patent explains that "[i]n a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system." Ex. 1001 (054 Patent) at 8:5-10. The 054 Patent further explains that "[i]n a second mode of operation, the circuit is operable to selectively couple the

controller to the volatile memory subsystem to allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, and the circuit is operable to selectively isolate the volatile memory subsystem from the host system." Ex. 1001 (054 Patent) at 8:10-16.

63. The 054 Patent describes embodiments wherein "[t]he controller backs up the volatile memory using the non-volatile memory in the event of a trigger condition." Ex. 1001 (054 Patent) at 20:21-22. It lists "trigger conditions" including "a power failure, power reduction, request by the host system, etc." Ex. 1001 (054 Patent) at 20:23-24. It further describes that the trigger condition can occur when the memory system detects that the system voltage is above or below a certain threshold. Ex. 1001 (054 Patent) at 24:23-33.

64. Figure 12 of the 054 Patent depicts an exemplary memory system of the invention:

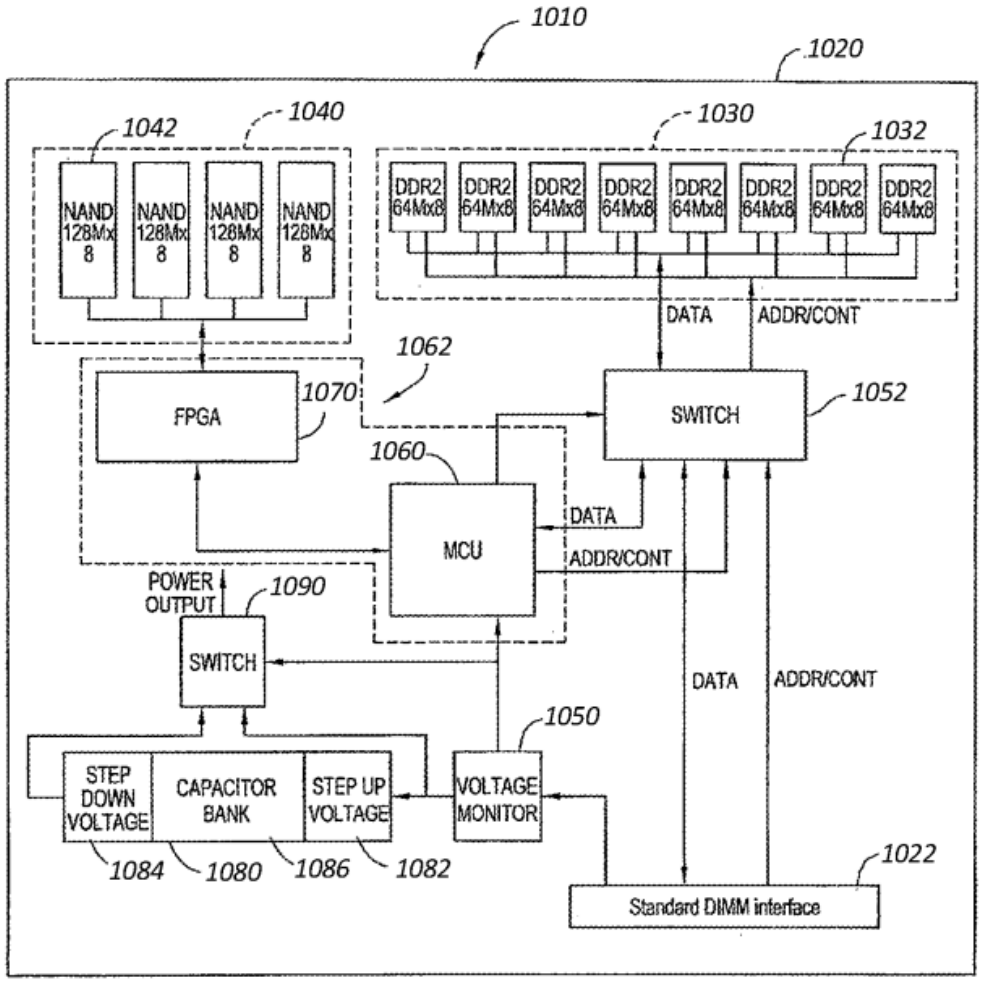


FIG. 12

Ex. 1001 (054 Patent) at Fig. 12. With reference to figure 12, the 054 Patent describes that "[t]he memory system 1010 can be coupled to a host computer system and can include a volatile memory subsystem 1030, a non-volatile memory subsystem 1040, and a controller 1062 operatively coupled to the non-volatile memory subsystem 1040." Ex. 1001 (054 Patent) at 21:16-20. The system includes

a "second power supply 1080" comprising either "capacitors" or a "battery" to supply power during a power disruption. *Id.* at 26:8-43.

65. The volatile memory subsystem 1030 "comprises a plurality of volatile memory elements 1032." Ex. 1001 (054 Patent) at 22:9-10. The volatile memory elements 1032 can comprise "dynamic random-access memory (DRAM) elements" including, but not limited to, "DDR, DDR2, DDR3, and synchronous DRAM (SDRAM)" elements. Ex. 1001 (054 Patent) at 22:17-22. The volatile memory elements 1032 may also comprise "other types of memory elements such as static random-access memory (SRAM)." Ex. 1001 (054 Patent) at 22:24-26.

66. The controller 1062 "may comprise a microcontroller unit (MCU) 1060 and a logic element 1070." Ex. 1001 (054 Patent) at 24:36-37. The MCU 1060 "provides memory management for the non-volatile memory subsystem 1040 and controls data transfer between the volatile memory subsystem 30 [*sic*, 1030] and the nonvolatile memory subsystem 1040." Ex. 1001 (054 Patent) at 24:38-41. The logic element 1070 in figure 12 is labeled as an FPGA (field-programmable gate array). Ex. 1001 (054 Patent) at Fig. 12, 23:1-3.

67. The non-volatile memory subsystem 1040 "comprises a plurality of non-volatile memory elements 1042." Ex. 1001 (054 Patent) at 22:10-12. The non-volatile memory elements 1042 can comprise "one or more flash elements" including, but not limited to, "NOR flash, NAND flash, ONE-NAND flash, and

multi-level cell (MLC)." Ex. 1001 (054 Patent) at 22:36-40. The 054 Patent describes that the non-volatile memory subsystem 1040 may be used "as a flash 'mirror' to provide backup of the volatile memory subsystem 1030 in the event of certain system conditions," i.e. trigger conditions. Ex. 1001 (054 Patent) at 24:9-16.

68. As shown in figure 12, the above described components of the memory system 1010 reside on "a printed-circuit board (PCB) 1020." Ex. 1001 (054 Patent) at 21:25-26. The PCB 1020 can "comprise an interface 1022 that is configured to be in electrical communication with the host system." Ex. 1001 (054 Patent) at 21:65-67. The interface 1022 can further "comprise a plurality of edge connections" that connect to the host system. Ex. 1001 (054 Patent) at 22:1-3. The interface 1022 "provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system." Ex. 1001 (054 Patent) at 22:3-6.

69. The 054 Patent further describes that, in some embodiments, "the memory system 1010 includes at least one circuit 1052 configured to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030." Ex. 1001 (054 Patent) at 21:20-23. It further describes that, in some embodiments, "the at least one circuit 1052 comprises one or more switches coupled to the volatile memory subsystem 1030, to the controller 1062, and to the

host computer." Ex. 1001 (054 Patent) at 23:28-32. These switches "respon[d] to signals (e.g., from the controller 1620) to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030 and to selectively operatively couple the controller 1062 to the volatile memory subsystem 1030." Ex. 1001 (054 Patent) at 23:32-40.

70. As depicted in figure 12, the memory system 1010 may also include a "voltage monitor 1050" which "monitors the voltage supplied by the host system via the interface 1022." Ex. 1001 (054 Patent) at 25:8-10. The 054 Patent describes that "upon detecting a low voltage condition," the voltage monitor 1050 "may transmit a signal to the controller 1062 indicative of the detected condition." Ex. 1001 (054 Patent) at 25:11-15. The controller 1062 can then respond to the signal by "transmitting a signal to the at least one circuit 1052 to operatively couple the controller [(1062)] to the volatile memory system 1030, such that the memory system 1010 enters the second state." Ex. 1001 (054 Patent) at 25:15-20. This process can result in the execution of a write cycle whereby "data is read from the volatile memory subsystem 1030 and is transferred to the non-volatile memory subsystem 1040 via the MCU 1060." Ex. 1001 (054 Patent) at 25:20-27.

71. Figure 16 of the 054 Patent depicts an exemplary power module of the memory system:

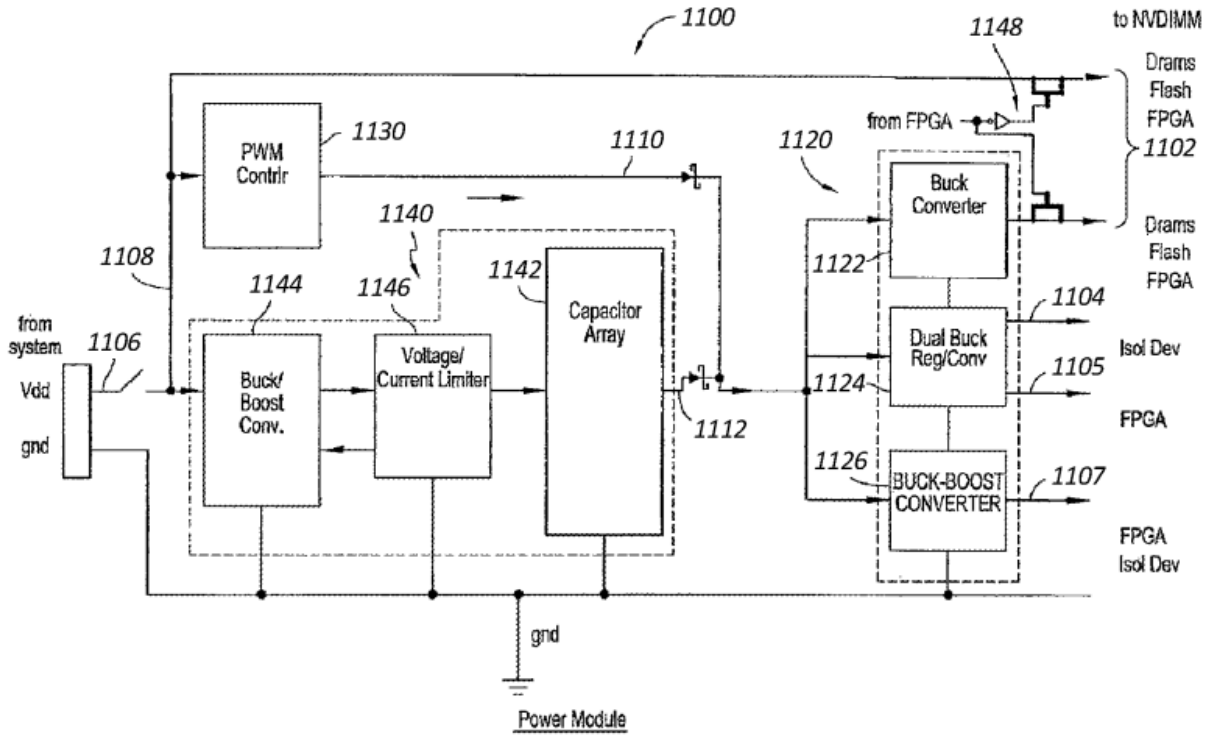
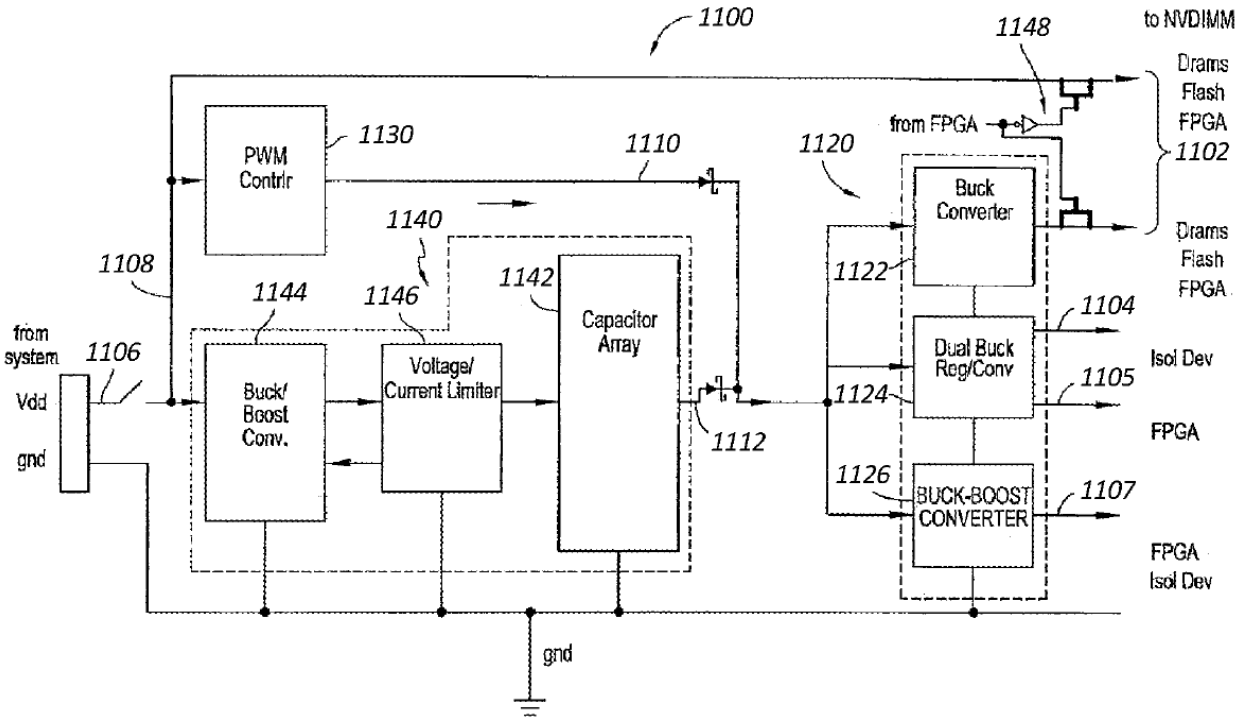


FIG. 16

Ex. 1001 (054 Patent) at Fig. 16. The power module 1100 depicted in figure 16, "provides power to the various components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition." Ex. 1001 (054 Patent) at 27:61-65. Specifically, the 054 Patent describes that "[t]he power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040." Ex. 1001 (054 Patent) at 28:3-5. It states that "[t]he plurality of

voltages comprises at least a first voltage 1102 and a second voltage 1104." Ex. 1001 (054 Patent) at 28:5-7.

72. As illustrated in figure 16, the 054 Patent describes that the power module 1100 includes block 1130 as a "first power element," block 1140 as a "second power element," and block 1120 as a "voltage conversion element." Ex. 1001 (054 Patent) at 28:7-22. As depicted in the excerpt of figure 16 below, "the first power element 1130" can "comprise a pulse-width modulation power controller."



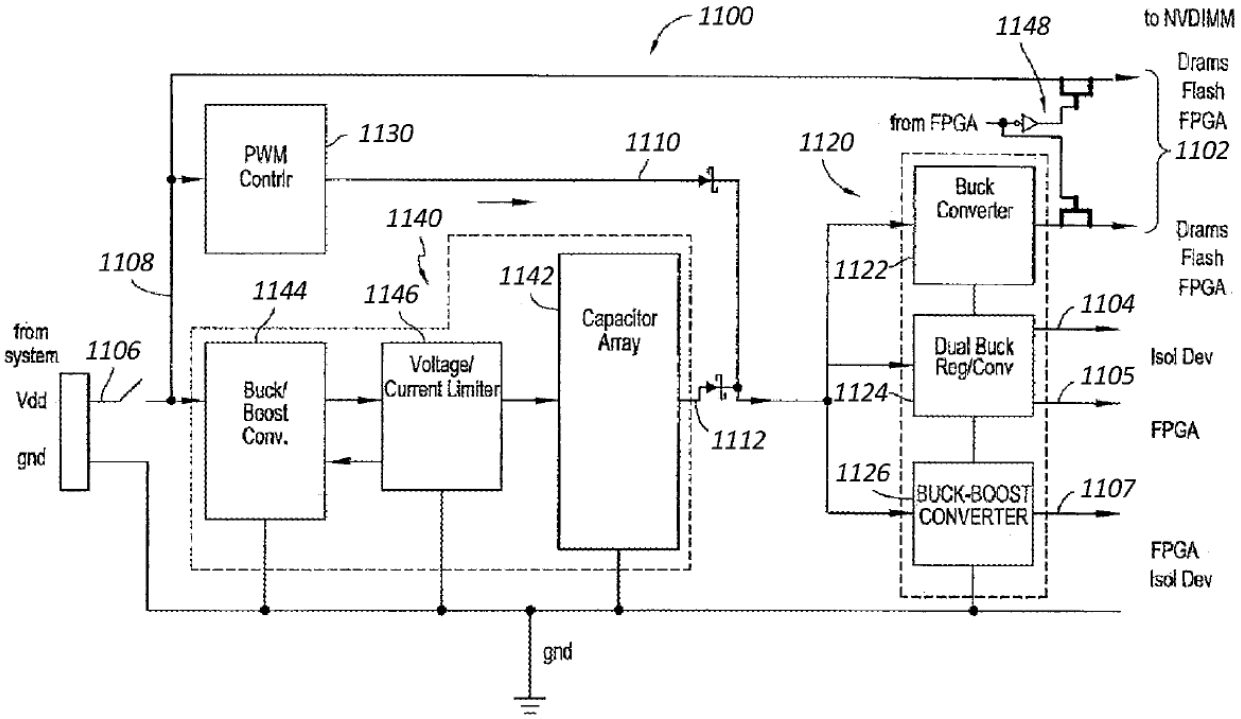
Ex. 1001 (054 Patent) at 28:13-15, Fig. 16. The first power element 1130 receives an input voltage, described in the patent as "the third voltage 1108." Ex. 1001 (054 Patent) at 28:8. Upon receiving the input voltage 1108, the first power element

"selectively provide[s] a fourth voltage 1110 to the conversion element 1120." Ex. 1001 (054 Patent) at 28:11-13. For example, the patent describes that the first power element 1130 can "receive a 1.8V input system voltage as the third voltage 1108" and "output a modulated 5V output as the fourth voltage 1110." Ex. 1001 (054 Patent) at 28:15-19.

73. As depicted in the excerpt of figure 16 above, "the second power element 1140" comprises "a capacitor array 1142," "a buck-boost converter 1144," and "a voltage/current limiter 1146." Ex. 1001 (054 Patent) at 28:61-65. In other embodiments "a pure boost converter may be used instead of a buck-boost converter." Ex. 1001 (054 Patent) at 29:14-16. Additionally, "only one capacitor may be used instead of a capacitor array 1142." Ex. 1001 (054 Patent) at 29:16-17. The second power element 1140 receives the same input voltage as the first power element (1108 as shown in figure 16). Ex. 1001 (054 Patent) at Fig. 16, 29:3-6. Upon receiving the input voltage 1108, the second power element 1140 "selectively provide[s] a fifth voltage 1112 to the conversion element 1120." Ex. 1001 (054 Patent) at 28:21-22. For example, the patent describes that the "the buck-boost converter 1144 receives a 1.8V system voltage (first voltage 1108) and boosts the voltage to 4.3V which is outputted to the voltage current limiter 1146." Ex. 1001 (054 Patent) at 29:3-6. The voltage current limiter "limits the current

going to the capacitor array 1142 to 1A and stops charging the array 1142 when it is charged to 4.3V." Ex. 1001 (054 Patent) at 29:6-9.

74. The 054 Patent describes generally that "[t]he conversion element 1120" can comprise "one or more buck converters and/or one or more buck-boost converters." Ex. 1001 (054 Patent) at 29:18-19. As shown in the excerpt of figure 16 below, the conversion element 1120 may contain "a plurality of sub-blocks 1122, 1124, 1126."



Ex. 1001 (054 Patent) at Fig. 16. The sub-blocks can comprise "various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010." Ex. 1001 (054 Patent) at 29:20-27. Specifically, "sub-block 1122 comprises a buck

converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter." Ex. 1001 (054 Patent) at 29:27-31. The conversion element 1120 receives as voltage input "either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100." Ex. 1001 (054 Patent) at 29:33-38. The conversion element 1120 then "reduces the input to an appropriate amount for powering various components of the memory system." Ex. 1001 (054 Patent) at 29:38-39. For example, "the buck-converter of sub-block 1122 can provide 1.8V," labeled as first voltage 1102 in figure 16 (and described as a first voltage), to the volatile memory elements, the non-volatile memory elements, and the controller. Ex. 1001 (054 Patent) at 29:39-44, Fig. 16. The "sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory subsystem 1010." Ex. 1001 (054 Patent) at 29:44-46. For example, "the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052," and the third "voltage 1105 is 1.2V and is used to power the controller 1062." Ex. 1001 (054 Patent) at 29:46-50. And sub-block 1126 can provide a fourth "voltage 1107 to the memory system 1010." Ex. 1001 (054 Patent) at 29:50-51. For example, "the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052." Ex. 1001 (054 Patent) at 29:51-52.

75. The 054 Patent describes that the power module 1100 "can be configured to be operated in at least three states." Ex. 1001 (054 Patent) at 28:26-27. In the first state, "the first voltage 1102 is provided to the memory system 1010 from the input 1106 and the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130." Ex. 1001 (054 Patent) at 28:27-31. In the second state, "the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120." Ex. 1001 (054 Patent) at 28:31-34. In the third state, "the fifth voltage 1112 is provided to the conversion element 1120 from the second power element 1140 and the first voltage 1104 is provided to the memory system 1010 from the conversion element 1120." Ex. 1001 (054 Patent) at 34-38. The 054 Patent further describes that "the power module 1100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition has occurred." Ex. 1001 (054 Patent) at 28:39-43.

D. The Prosecution History of The 054 Patent

1. Provisional Application No. 60/941,586 (June 1, 2007)

76. The applicants filed Provisional Application No. 60/941,586 ("586 Provisional Application"), titled "Non-Volatile Memory Module," on June 1, 2007.

Ex. 1005 (586 Provisional Application File History) at 1, 13. As discussed above, this application does not provide support for all of the limitations in the claims of the 054 Patent. *Supra* ¶¶47-60.

2. Application No. 12/131,873 (June 2, 2008) (abandoned)

77. The applicants filed U.S. Patent Application No. 12/131,873 ("873 Application"), titled "Non-Volatile Memory Module," on June 2, 2008. Ex. 1006 (873 Application File History) at 1. The 873 Application claims benefit of the 586 Provisional Application, filed on June 1, 2007. *Id.* The 873 Application presented 54 claims at filing, 1-54. Ex. 1006 (873 Application File History) at 33-40.

78. On September 16, 2008, the applicants of the 873 Application filed a Preliminary Amendment, cancelling claims 21-54. Ex. 1006 (873 Application File History) at 67-71.

79. The applicants subsequently abandoned the 873 Application. Ex. 1006 (873 Application File History) at 96.

3. Application No. 12/240,916 ('833 Patent)

80. The applicants filed U.S. Patent Application No. 12/240,916 ("916 Application"), titled "Non-Volatile Memory Module," on September 29, 2008. Ex. 1007 (916 Application File History) at 61. The 916 Application is a continuation of the 873 Application, filed on June 2, 2008, and claims benefit of the 586

Provisional Application, filed on June 1, 2007. *Id.* at 3. The 916 Application presented 54 claims at filing, 1-54. Ex. 1007 at 35-43.

81. On March 31, 2011, the examiner issued an Office Action subjecting claims 1-54 to a restriction and/or election requirement as being drawn to four distinct inventions. Ex. 1007 at 120-123.

1) First Invention: "Claims 1-20, and 43-49, drawn to a non-volatile and a volatile memory systems." *Id.* at 120.
2) Second Invention: "Claims 21-26, drawn to a power module for a volatile and non-volatile memory including a voltage conversion element." *Id.*
3) Third Invention: "Claims 37-42, drawn to non-volatile and a volatile memory systems wherein the memory systems operate at different frequencies depending on the mode of operation." *Id.*
4) Fourth Invention: "Claims 50-54, drawn to restoring data." *Id.*

82. On May 20, 2011, the applicants of the 916 Application filed a Preliminary Amendment in response to the restriction requirement, withdrawing claims 1-36 and 43-54 and electing to prosecute only the third invention identified by the examiner, including claims 37-42. Ex. 1007 at 125-133. The applicants made this election without traverse. *Id.* at 133.

83. In my opinion, the claims of the 054 Patent differ from the "Third Invention" that was elected for prosecution in the 916 Application (which later issued as the '833 Patent, as discussed below). For example, the "Third Invention" requires that "the memory systems operate at different frequencies depending on the mode of operation," which is not a limitation found in any of the claims of the 054 Patent.

84. On July 29, 2011, the examiner rejected claims 37-42 as being obvious over Li et al. [US 6,336,174] in view of Oshikiri [US 2007/0192627]. Ex. 1007 at 141-147.

85. On October 18, 2011, the applicants of the 916 Application filed a reply to the Office Action dated July 29, 2011, adding claims 55-90 and arguing that the examiner's obviousness rejection was improper. Ex. 1007 at 169-184.

86. On February 1, 2012, the examiner issued a Final Office Action maintaining the obviousness rejection, rejecting newly added claims 61-62, 64-76, 83-84, and 86-90 as being similarly unpatentable over Li et al. in view of Oshikiri, and rejecting claims 63 and 85 as being indefinite. Ex. 1007 at 191-200. The examiner also restricted newly added claims 55-60 and 77-82 as being directed to a non-elected invention, namely "different embodiments for the claimed trigger condition." Ex. 1007 at 190-191. These restricted claims included limitations defining the trigger condition as "a drop below a voltage threshold," "a rise above

a voltage threshold," and "a drop below a first voltage threshold or a rise above a second voltage threshold," among others. *Id.* at 177, 180.

87. On March 2, 2012, the applicants of the 916 Application filed a reply to the Final Office Action dated February 1, 2012, including claim amendments to overcome the obviousness and indefiniteness rejections. Ex. 1007 at 204-208, 210. Applicants also canceled claims 55-60 and 77-82 in response to the examiner's restriction. Ex. 1007 at 205, 207, 209.

88. On April 3, 2012, after a request for continued examination, the examiner issued an Office Action rejecting claims 37-42, 61-62, 64-76, 83-84, and 86-90 as being obvious over Li et al. in view of Cope [US 2008/0195806]. Ex. 1007 at 232-239. The examiner also rejected claims 38 and 72 as being indefinite. Ex. 1007 at 231-232.

89. On May 24, 2012, the applicants filed a reply to the Office Action dated April 3, 2012, including claim amendments to overcome the indefiniteness rejections. Ex. 1007 at 246-251. Applicants also argued that the obviousness rejections were improper. Ex. 1007 at 251-259.

90. On September 17, 2012, the examiner issued a Notice of Allowance, allowing claims 37-42, 61-76, and 83-90 of the 916 Application. Ex. 1007 at 288-294. The 916 Application issued as U.S. Patent No. 8,301,833 ("'833 Patent") on October 30, 2012. Ex. 1007 at 320.

91. To my knowledge, four IPR petitions have been filed against the '833 Patent, by SanDisk Corporation, Smart Modular Technologies Inc., SK hynix Inc. et al., and Micron Technology, Inc. et al., respectively. *See* Ex. 1014; Ex. 1016; Ex. 1018; Ex. 1022. The PTAB denied institution for the first three IPR petitions. *See* Ex. 1015; Ex. 1017; Ex. 1019. The PTAB has not yet made an institution decision in response to the fourth IPR petition, which was filed on January 14, 2022. *See* Ex. 1022.

4. Provisional App No. 61/512,871 (July 28, 2011)

92. The applicants filed Provisional Application No. 61/512,871 ("871 Provisional Application"), titled "High Density DIMMs," on July 28, 2011. Ex. 1008 (871 Provisional Application File History) at 1-3, 47.

5. Application No. 13/559,476 ('831 Patent)

93. The applicants filed U.S. Patent Application No. 13/559,476 ("476 Application"), titled "Flash-DRAM Hybrid Memory Module," on July 26, 2012. Ex. 1009 at 63. The 476 application claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1009 at 237; *supra* Sections III.D.1-III.D.4. The 476 Application presented 24 claims at filing, 1-24. Ex. 1009 at 38-43.

94. On March 28, 2014, the applicants of the 476 Application filed a Preliminary Amendment, amending claims 1, 13, and 25 and cancelling claims 6-8, 10-12, 15, 17, and 20. Ex. 1009 at 141-147.

95. On May 6, 2014, the examiner issued a Notice of Allowance, allowing claims 1-5, 9, 13, 14, 16, 18, 19, and 21-24 of the 476 Application. Ex. 1009 at 151-160. However, the examiner granted a later priority date than the applicants claimed:

> [T]he inventive entity of each of the prior-filed applications is/are not the same inventive entity of the present application. Prior filed provisional application 61/512871 has single inventor, Hyun Lee (a distinct inventive entity), and prior filed CIP application 12/240916 has four inventors: Chi-She Chen, Jeffrey Solomon, Scott Milton, and Jayesh Bhakta (a different distinct inventive entity), while the present application has five inventors: Hyun Lee, Chi-She Chen, Jeffrey Solomon, Scott Milton, and Jayesh Bhakta (another different distinct inventive entity).

Ex. 1009 at 157. The examiner concluded that "[t]he priority date granted to the examination of the present application is 7/26/2012." Ex. 1009 at 157.

96. On May 16, 2014, the examiner conducted an interview with the applicant's representative after which the examiner concluded that the 476 Application is entitled to claim priority based on the 871 Provisional Application, filed July 28, 2011, and the 916 Application, filed September 29, 2008. Ex. 1009 at 212-217.

97. The 476 Application issued as U.S. Patent No. 8,874,831 ("'831 Patent") on October 28, 2014. Ex. 1009 at 312. On January 17, 2017, an IPR petition was filed against the '831 Patent by SK hynix Inc., et al. *See* Ex. 1020. On July 5, 2018, the PTAB issued a final written decision invalidating all claims of the '831 Patent. *See* Ex. 1021 at 41.

6. Application No. 14/489,269 ('830 Patent)

98. The applicants filed U.S. Patent Application No. 14/489,269 ("269 Application"), titled "Flash-DRAM Hybrid Memory Module," on September 17, 2014. Ex. 1010 (269 Application File History) at 57. The 269 Application is a continuation of the 476 Application, filed July 26, 2012, which claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1010 at 1; *supra* Sections III.D.1-III.D.5. The 269 Application presented 1 claim at filing. Ex. 1010 at 37.

99. On May 15, 2015, the applicants of the 269 Application filed a Preliminary Amendment, cancelling claim 1 and adding new claims 2-25. Ex. 1010 at 88-93.

100. On July 8, 2015, the examiner issued a Notice of Allowance, allowing claims 2-25 of the 269 Application. Ex. 1010 at 103-112. However, the examiner granted a later priority date than the applicants claimed because "[t]he disclosures of the prior-filed applications [Nos. 12/240,916, 12/131,873, and 60/941,586] fail to provide adequate support or enablement" because "the claimed feature 'data manager' . . . lacks proper antecedent basis or clear support [in the identified applications]." Ex. 1010 at 108-109. The examiner concluded that "[t]he effective priority date that the present claims are entitled to therefore becomes 7/28/2011 based upon the earliest priority claim to Non-provisional 61/512,871." Ex. 1010 at 109.

101. The 269 Application issued as U.S. Patent No. 9,128,830 on September 08, 2015. Ex. 1010 at 145.

7. Application No. 14/840,865 ('186 Patent)

102. The applicants filed U.S. Patent Application No. 14/840,865 ("865 Application"), titled "Flash-DRAM Hybrid Memory Module," on August 31, 2015. Ex. 1011 (865 Application File History) at 63. The 865 Application is a continuation of the 269 Application, filed September 17, 2014, which is a

continuation of the 476 Application, filed July 26, 2012, which claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1011 at 25; *supra* Sections III.D.1-III.D.6. The 865 Application presented 1 claim at filing. Ex. 1011 at 61.

103. On April 21, 2016, the examiner rejected claim 1 on the ground of double patenting as claiming the same invention as claim 1 of U.S. Patent 9,158,684. Ex. 1011 at 100-101.

104. On October 20, 2016, the applicants of the 865 Application filed a reply to the Office Action dated April 21, 2016, cancelling claim 1 and adding claims 2-22. Ex. 1011 at 133-140.

105. On November 18, 2016, the examiner issued a Notice of Allowance, allowing claims 2-22 of the 865 Application. Ex. 1011 at 155-159. However, the examiner granted a later priority date than the applicants claimed because "[t]he disclosures of the prior-filed applications [Nos. 12/240,916, 12/131,873, and 60/941,586] fail to provide adequate support or enablement" because "the claimed feature 'data manager' . . . lacks proper antecedent basis or clear support [in the identified parent applications]." Ex. 1011 at 160-161. The examiner concluded that "[t]he effective priority date that claims 2-22 are entitled to therefore becomes

7/28/2011 based upon the earliest priority claim being that to parent application to Non-provisional 61/512,871." Ex. 1011 at 161.

106. On May 5, 2017, in response to a request for continued examination, the examiner issued an Office Action rejecting claims 2-13 and 17-22 as being anticipated by Best, [U.S. 2010/0110748 Al] and objecting to claims 10 and 14-16. Ex. 1011 at 218-228.

107. On November 06, 2017, the applicants of the 865 Application filed a reply to the Office Action dated May 5, 2017, amending claims 2, 10, and 14-17 and arguing that the examiner's anticipation-based rejection was improper. Ex. 1011 at 273-291.

108. On November 11, 2017, the examiner issued a Notice of Allowance, allowing claims 2-22 of the 865 Application. Ex. 1011 at 293-297. The 865 Application issued as U.S. Patent No. 9,928,186 on March 27, 2018. Ex. 1011 at 338.

8. Application No. 15/934,416 (abandoned)

109. The applicants filed U.S. Patent Application No. 15/934,416 ("416 Application"), titled "Flash-DRAM Hybrid Memory Module," on March 23, 2018. Ex. 1012 (416 Application File History) at 76. The 416 Application is a continuation of the 865 Application, filed August 31, 2015, which is a continuation of the 269 Application, filed September 17, 2014, which is a continuation of the

476 Application, filed July 26, 2012, which claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1012 at 19; *supra* Sections III.D.1-III.D.7. The 416 Application presented 1 claim at filing. Ex. 1012 at 55.

110. On March 21, 2019, the examiner rejected claim 1 on the ground of double patenting as claiming the same invention as claim 1 of U.S. Patent 9,928,186. Ex. 1012 at 203.

111. On July 22, 2019, the applicants of the 416 Application filed a reply to the Office Action dated March 21, 2019, cancelling claim 1 and adding claims 2-21. Ex. 1012 at 249-255. On August 26, 2019, the applicants filed supplemental amendments to the claims. Ex. 1012 at 262-269.

112. On October 15, 2019, the examiner filed a Final Office Action, rejecting claims 6-8, 13-17, and 21 for failing to comply with written description requirement. Ex. 1012 at 275-277. The examiner also rejected claims 2-5, 9-12, and 18-19 as either anticipated by Fukuzo [US 2006/0294295 A1] or obvious over Fukuzo in view of Shiota et al. [US 2003/0147297 Al]. Ex. 1012 at 277-282.

113. On March 12, 2020, after a request for continued examination, the applicants filed a reply to the Office Action dated October 15, 2019, amending

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claim 2 and arguing that examiner's rejections were improper. Ex. 1012 at 307-318.

114. On April 2, 2020, the examiner filed an Office Action, rejecting claims 6-8, 13-17, and 21 for failing to comply with written description requirement. Ex. 1012 at 331-332. The examiner also rejected claims 2-5, 9-12, and 18-19 as either anticipated by Fukuzo [US 2006/0294295 A1] or obvious over Fukuzo in view of Shiota et al. [US 2003/0147297 Al]. Ex. 1012 at 324-340.

115. On October 2, 2020, the applicants filed a reply to the Office Action dated April 2, 2020, amending claims 2-21 and arguing that the examiner's anticipation/obviousness rejections were improper. Ex. 1012 at 377-390.

116. On January 1, 2021, the examiner filed a Final Office Action, rejecting claims 2, 6-7, 10, 12, 17, and 19 as anticipated by Bonella et al. [US 2007/0136523 Al], claims 3-5, 11, and 15 as obvious over Bonella et al. in view of Prete et al. [US 2008/0126624 Al], claims 8 and 16 as obvious over Bonella et al. in view of Randell et al. [US 2005/0183472 A1] [*sic*, U.S. Patent No. 8,086,788], and claims 9, 13-14, 18, and 20-21 as obvious over Bonella et al. in view of Kita [US 2005/0144418 A1]. Ex. 1012 at 397-413.

117. The applicants subsequently abandoned the 416 Application. Ex. 1012 at 454-455.

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9. Application No. 17/138,766 ('918 Patent)

118. The applicants filed U.S. Patent Application No. 17/138,766 ("766 Application"), titled "Flash-DRAM Hybrid Memory Module," on December 30, 2020. Ex. 1013 (766 Application File History) at 125. The 766 Application is a continuation of the 416 Application, filed March 23, 2018, which is a continuation of the 865 Application, filed August 31, 2015, which is a continuation of the 269 Application, filed September 17, 2014, which is a continuation of the 476 Application, filed July 26, 2012, which claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1013 (766 Application File History) at 29; *supra* Sections III.D.1-III.D.8. The 766 Application presented 30 claims at filing, 1-30. Ex. 1013 at 104-110.

119. On March 2, 2021, the examiner issued an Office Action rejecting claims 1-15 and 21 as being indefinite and allowing claims 1-16 and 22-30. Ex. 1013 at 137-143.

120. On March 11, 2021, the applicants of the 766 Application filed a reply to the Office Action dated March 2, 2021, amending claims 1 and 21 to recite "a

first one of the second and fourth voltage amplitudes is less than ~~the other~~a second one of the second and fourth voltage amplitudes." Ex. 1013 at 166.

121. On March 24, 2021, the examiner issued a Notice of Allowance, allowing claims 1-30 of the 766 Application. Ex. 1013 (766 Application File History) at 284-288. The 766 Application issued as U.S. Patent No. 11,016,918 on May 25, 2021. Ex. 1013 (766 Application File History) at 450.

10. Application No. 17/328,019 (054 Patent)

122. The applicants filed U.S. Patent Application No. 17/328,019 ("019 Application"), titled "Flash-DRAM Hybrid Memory Module," on May 24, 2021. Ex. 1002 (019 Application File History) at 111. The 019 Application is a continuation of the 766 Application, filed December 30, 2020, which is a continuation of the 416 Application, filed March 23, 2018, which is a continuation of the 865 Application, filed August 31, 2015, which is a continuation of the 269 Application, filed September 17, 2014, which is a continuation of the 476 Application, filed July 26, 2012, which claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1002 at 5; *supra* Sections III.D.1-III.D.9. The 019 Application presented 1 claim at filing. Ex. 1002 at 80.

123. On June 4, 2021, the applicants of the 019 Application filed a Preliminary Amendment, cancelling claim 1 and adding new claims 2-31. Ex. 1002 at 128-137.

124. On September 27, 2021, the examiner issued an Office Action rejecting claims 2-15, 20, 22-23, and 26-31, objecting to claims 24-25 as being dependent upon a rejected base claim, and allowing claims 16-19 and 21. Ex. 1002 at 359-369. Specifically, the examiner rejected claims 20, 22, and 30-31 as failing to comply with the written description requirement because each claim included at least one limitation reciting "a first diode" or "a second diode." Ex. 1002 at 362-363. The examiner also rejected claims 2-15, 23, and 26-29 on grounds of non-statutory double patenting as being unpatentable over claims 1-30 of U.S. Patent 11,016,918. Ex. 1002 at 363-367.

125. On November 19, 2021, the applicants of the 019 Application filed a reply to the Office Action dated September 27, 2021, amending claims 2, 5-6, 8-11, 15-17, and 23-27, cancelling claims 14, 28-29, and adding claims 32-34. Ex. 1002 at 446-454. The applicants also argued that the examiner's rejection of claims 20, 22, and 30-31 for insufficient written description was improper because the claimed first and second diodes were depicted in figure 16 of the application. Ex. 1002 at 455-456. Additionally, the applicants submitted a terminal disclaimer to

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overcome the non-statutory double patenting rejection of claims 2-15, 23, and 26-29. Ex. 1002 at 456.

126. On December 10, 2021, the examiner issued a Notice of Allowance, allowing claims 2-13, 15-27, and 30-34 of the 054 Application. Ex. 1002 at 471-478. The examiner provided the following reasons for allowance:

Allowable Subject Matter

3. Claims 2-13, 15-27, and 30-34 allowed.

The following is an examiner's statement of reasons for allowance:

4. The prior art of record does not teach or suggest the distinct features "a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three

> regulated voltages", *recited in the independent claims 2 and 23. The dependent claims 3-13, 15, and 32-33 are allowed by virtue of their dependency from the independent claim 2. The dependent claims 24-27 and 30-31 are allowed by virtue of their dependency from the independent claim 23.*
>
> 5. *The prior art of record does not teach or suggest the distinct features* "a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage, wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state", *recited in the independent claim 16. The dependent claims 17-22 and 34 are allowed by virtue of their dependency from the independent claim 16.*

Id. at 476-77.

127. The 019 Application issued as U.S. Patent No. 11,232,054 on January 25, 2022. Ex. 1002 at 500; Ex. 1001.

E. Construction of Terms Used in the 054 Patent Claims

128. I understand that claim terms should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. For purposes of my analysis below, I do not believe that any of the claims of the 054 Patent require an explicit claim construction. While I understand that Patent Owner appears to have interpreted some of the claim terms broadly for purposes of infringement, *see*, *e.g.*, Ex. 1071 at 39-46; Ex. 1073 at 55-

62, and that a narrower interpretation may be more reasonable, in my opinion the claims are obvious under either interpretation, as shown by my analysis below.

IV. OVERVIEW OF THE PRIOR ART

A. Prior Art

1. U.S. Patent Publication No. 2006/0174140 to Harris (Ex. 1023)

129. U.S. Patent Publication No. 2006/0174140 to Harris ("Harris"), titled "Voltage Distribution System and Method for a Memory Assembly," was published on August 3, 2006 and relates to U.S. Patent Application No. 11/047,304 filed on January 31, 2005. Ex. 1023 at 1. Harris was not cited during prosecution of the 054 Patent. *See* Ex. 1001 (054 Patent) at 2-3 ("U.S. PATENT DOCUMENTS"). Harris discloses a memory assembly module including an on-board voltage regulator module to convert an externally supplied voltage to appropriate local voltage levels. *Id.* at Abstract. Figure 1A illustrates such a memory module.

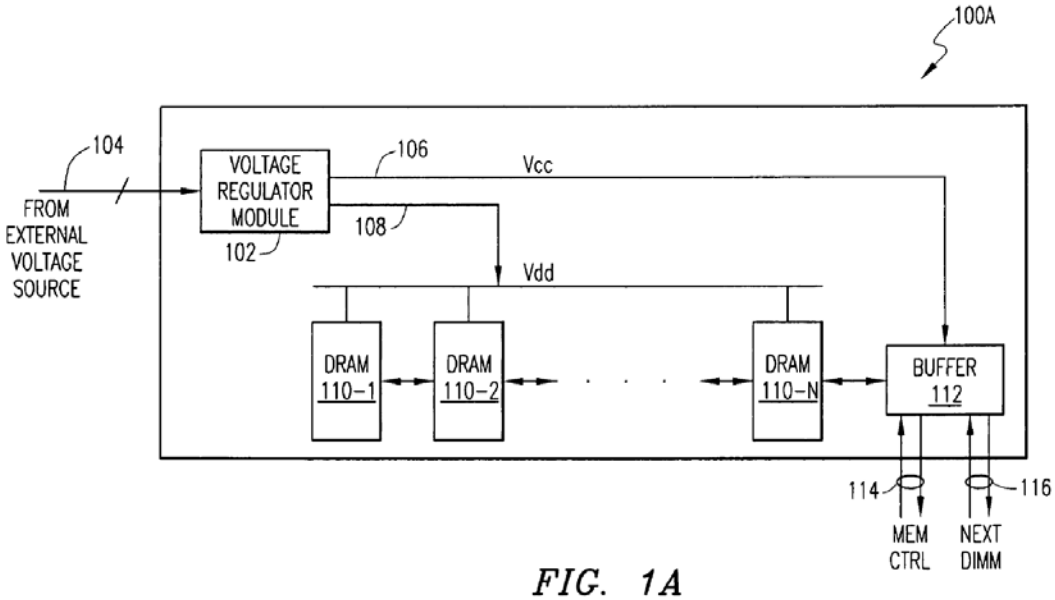


FIG. 1A

Id. at Fig. 1A. The memory module 100A connected to an input voltage path from an external voltage source (104), a bidirectional memory controller interface path (114), and a daisy-chain interface (116). *Id.* at [0009], Fig. 1A. A voltage regulator module (102), or VRM, is provided on-board the memory module 100A to convert the externally supplied voltage (104) into the appropriate local voltage levels. *Id.* at [0010], Fig. 1A. As shown in Figure 1A above, VRM (102) outputs Vcc (106) and Vdd (108). *Id.* Vcc (106) is provided to a buffer (112), and Vdd (108) is provided to dynamic random access memory (DRAM) devices (110-1 to 100-N). *Id.*, [0009], Fig. 1A.

130. Harris explicitly contemplates implementations using any one of several common and known memory technologies. For example, Harris explains that one benefit of its power supply solution is DRAM technology independence.

Id. at [0011]. That technology expressly includes DDR2, DDR3, and DDR4. *Id.* Harris also explains that local supply voltage conversion for a memory module can be implemented in a form factor with a component height compatible with applicable Joint Electron Device Engineering Counsel (JEDEC) standards. *See id.* at [0013]. In addition to implementations for various standard DRAM technologies, Harris explains that its memory module can be an unbuffered DIMM, registered DIMM (RDMM), or fully buffered DIMM (FBD). *See id.* at [0009]. As explained below and above, *supra* ¶61, a Skilled Artisan would have been familiar with these well-known technologies and the corresponding JEDEC standards.

2. U.S. Patent No. 7,724,604 to Amidi (Ex. 1024)

131. U.S. Patent No. 7,724,604 to Amidi ("Amidi"), titled "Clock and Power Fault Detection for Memory Modules," was filed on October 25, 2006, *see* Ex. 1024, and was published on May 1, 2008, *see* Ex. 1055. Amidi was not cited during prosecution of the 054 Patent. *See* Ex. 1001 at 2-3 ("U.S. PATENT DOCUMENTS").

132. Amidi discloses a system for fault detection, such as detecting voltage or power faults, that includes a "battery, battery regulation circuitry, volatile memory, memory control state machine, controller, clock detection circuit and voltage detection circuit [that] are all collectively included in a unitary memory module." Ex. 1024 at Abstract. As shown below in Figure 5 of Amidi, the power

management block is provided two voltage supplies and outputs a third voltage supply.

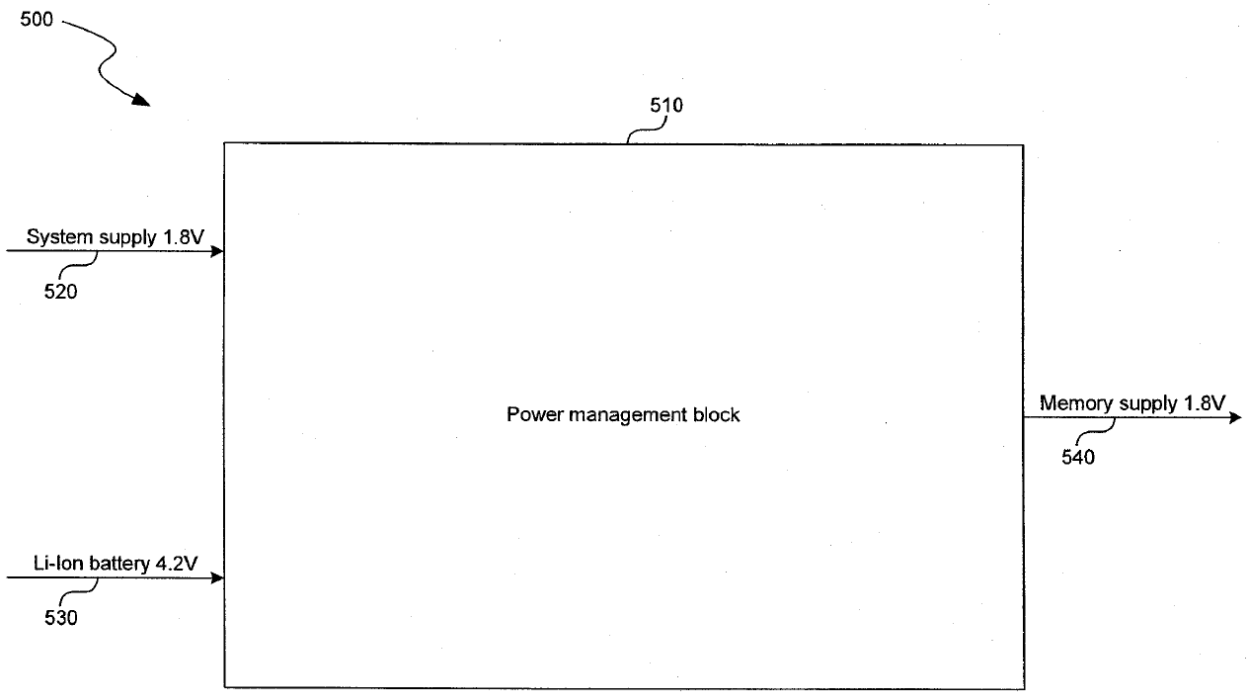


FIG. 5

Id. at Fig. 5. In particular, the system supply 520 and li-ion battery 530 are provided to the power management module 510 that outputs memory supply 540. *Id.* at 4:14-22, Fig. 5 (power management block 510). Amidi explains that the power management block 500 ensures "a stable power supply even in the face of disruptions in system supply 520, for example." *Id.* at 4:20-22. Amidi also explains that these disruptions are detected by, for example, comparing the external power supply to a reference voltage (e.g., 3.0-volt reference for a 3.3-volt supply) to

determine whether the power supply is below the reference. *See id.* at 8:23-36, Fig. 14.

3. U.S. Patent Publication No. 2006/0080515 to Spiers (Ex. 1025)

133. U.S. Patent Publication No. 2006/0080515 to Spiers ("Spiers"), titled "Non-Volatile Memory Backup for Network Storage System," was published on April 13, 2006, and relates to U.S. Patent Application No. 10/711,901 filed on October 12, 2004. Ex. 1025 at 1. Spiers was cited during prosecution of the 054 Patent but was not discussed by the applicant or the examiner in that application or any earlier applications. *See* Ex. 1001 at 3 ("U.S. PATENT DOCUMENTS"); *see generally* Ex. 1002. As shown in Figure 5 of Spiers, reproduced below, Spiers discloses a memory module (backup device 144).

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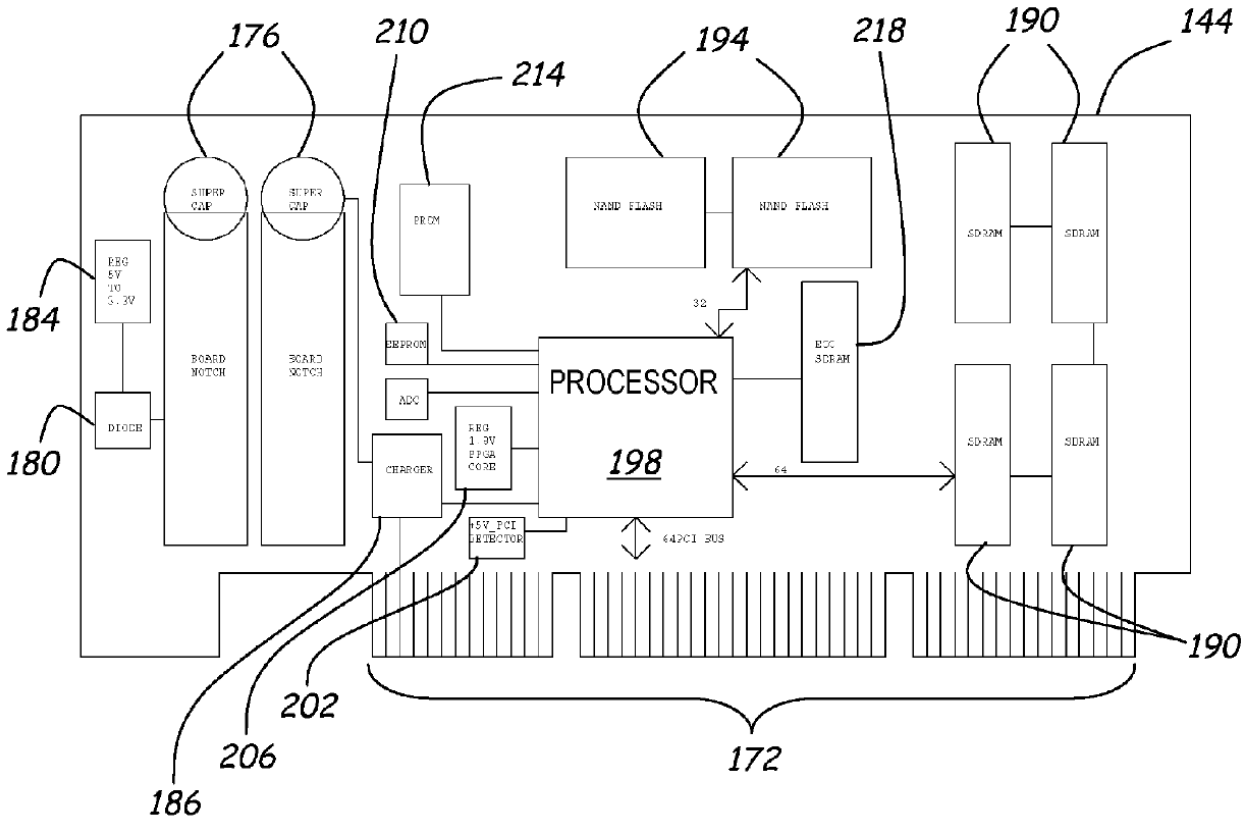


FIG.5

Id. at Fig. 5. The module includes a processor (198) for interfacing with the host computer system through an interface (connector 172), with on-board volatile memory (190 and 218), and with on-board, non-volatile memory (194). *Id.* The module also includes a temporary backup power supply (including supercapacitors 176) to provide a power source for moving data from the volatile memory to the non-volatile memory in the event of a power failure. *Id.* at [0037].

4. JEDEC Standards for Fully Buffered Dual In-Line Memory Module ("FBDIMM Standards") (Exs. 1027-28)

134. I understand that the JEDEC Solid State Technology Association published the standard Fully Buffered Dual In-Line Memory Module (FBDIMM) Advanced Memory Buffer (AMB) in March 2007 ("JESD82-20"). Ex. 1027 at Cover; *see* Ex. 1029 at ¶7. JESD82-20 was not cited during prosecution of the 054 Patent. *See* Ex. 1001 at 3-5 ("Other Publications"). In addition, I understand that the JEDEC Solid State Technology Association published the standard DDR2 SDRAM FBDIMM Design Specification in March 2007 ("JESD205"). Ex. 1028 at Cover; *see* Ex. 1029 at ¶7.

135. JESD205 was disclosed in an IDS filed by the applicant of the 054 Patent but was not discussed by the examiner or applicant in that application or any earlier applications. See Ex. 1001 at 3-5 ("Other Publications"); see generally Ex. 1002.

136. JESD82-20 (Ex. 1027) and JESD205 (Ex. 1028) (collectively, "FBDIMM Standards") are related to each other, and cite to each other, and both concern Fully Buffered DIMMs (FBDIMMs). *See* Ex. 1027 (JESD82-20) at 5 (citing "DDR2 Fully Buffered DIMM Design Specification," which is Ex. 1028 (JESD205)). JESD82-20 concerns the "AMB" buffer on the FBDIMM, and explains that the AMB buffer "supports DDR2SDRAM main memory" and "allows buffering of memory traffic to support large memory capacities." Ex. 1027

at p.1. The AMB interface "is responsible for handling FBD channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the FBD channel." *Id.* "Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind [the AMB] on the DIMM." *Id.* Similar to the 054 Patent, JESD82-20 specifies multiple supply voltages for the AMB buffer, as shown in the table below.

Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

Id. at p.83 (excerpt of Table 9.2). In particular, there are four voltage supplies at three different voltage amplitudes. VCC provides a 1.5-volt nominal supply for core input/output (I/O), VCCFBD provides a 1.5-volt nominal supply for high-speed I/O on the fully-buffered DIMM (FBD), VDD provides a 1.8-volt nominal supply for double-data rate (DDR2) I/O, and VDDSPD provides a 3.3-volt nominal supply for system management bus (SMB or SMBus) receivers and electro-static discharge (ESD) diodes. *Id.*

137. JESD205 describes the electrical and mechanical requirements for the FBDIMM module itself (which includes the AMB buffer described in JESD82-20

discussed above). Ex. 1028 at p.9. Similar to the 054 Patent, JESD205 specifies multiple supply voltages, as shown in the table below.

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})

Id. at 9. In particular, there are several voltage supplies at four different voltage amplitudes. The first supply voltage listed in the table is typically 1.8 volts for V_{DD} and V_{DDQ} on the DRAM and V_{DDQ} for the AMB. The second supply voltage listed in the table is typically 1.5 volts for V_{CC} and V_{CCFBD} on the AMB. The third supply voltage listed is typically one-half of V_{DD} or 0.9 volts for V_{TT} on the DRAM interface. And the fourth supply voltage listed in the table is typically 3.3 volts for V_{DDSPD}.

5. U.S. Patent No. 6,856,556 to Hajeck (Ex. 1038)

138. U.S. Patent No. 6,856,556 to Hajeck ("Hajeck"), titled "Storage subsystem with embedded circuit for protecting against anomalies in power signal from host," was issued on February 15, 2005, and relates to U.S. Patent Application No. 10/406,805 filed April 3, 2003. Ex. 1038 at 1. Hajeck was not cited during prosecution of the 054 Patent. Ex. 1001 at 2-3 ("U.S. PATENT DOCUMENTS"). Hajeck recognizes the need to detect "anomalies" by monitoring

the power input to a memory subsystem, including those with volatile and non-volatile memory. Ex. 1038 at Abstract, Fig. 1, 2:64-3:2. Hajeck also recognizes that its protection of memory subsystems is not limited to flash memory cards, but applies to volatile memory subsystems that store data in DRAM. *See id.* at 1:10-13 ("protecting storage subsystems, such as but not limited to flash memory cards, from damage and data loss caused by irregularities in a power signal provided by a host"), 4:62-65 ("The protection circuitry and methods of the present invention may also be incorporated into other types of storage subsystems, including volatile storage subsystems that store data within DRAM or SRAM."). In particular, Hajeck discloses a voltage detection circuit 48, as shown in Figure 1 below.

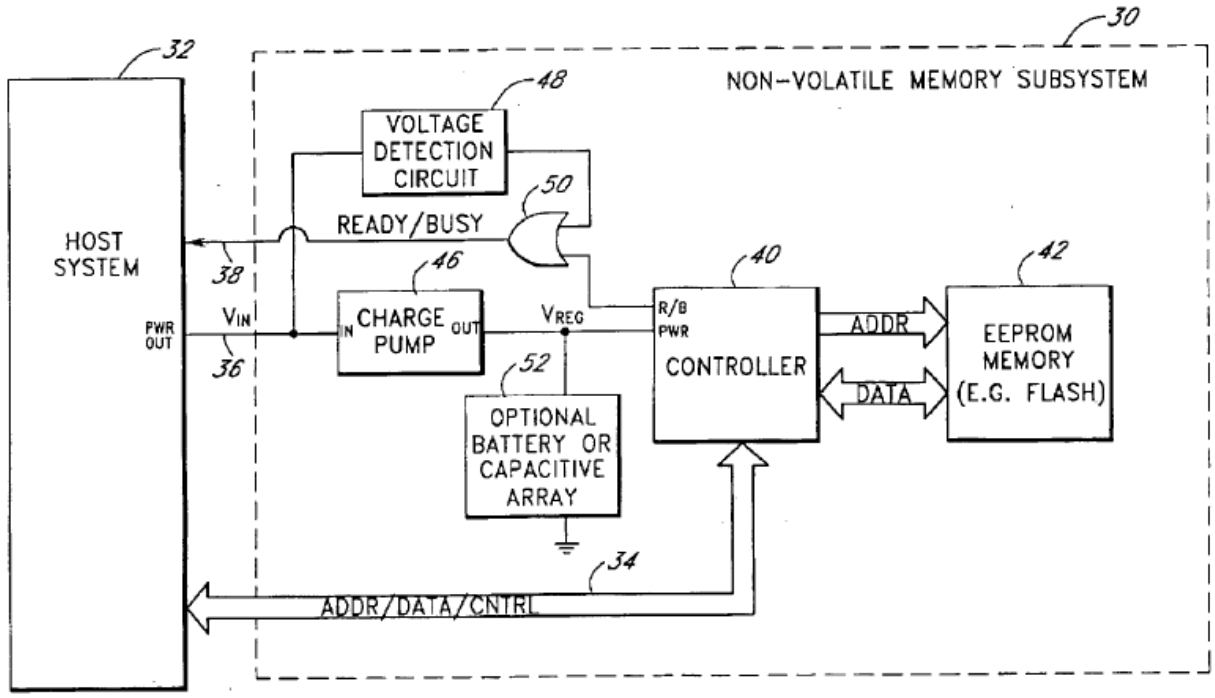


FIG. 1

Id. at Fig. 1. Hajeck explains that the circuit can be a "conventional voltage detection circuit" and is "responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line 36, and for driving the ready/busy signal to the 'busy' state when such anomalies are detected." *Id.* at 3:30-34. For example, the circuit may be designed for undervoltage detection by "generat[ing] a 'busy' signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts." *Id.* at 3:34-37. The circuit can also be designed for overvoltage detection by "generat[ing] a busy signal when the voltage exceeds a certain level . . . ." *Id.* at 3:37-39. In addition, Hajeck teaches that to avoid "rapid transitions between the 'ready' and 'busy'

states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition." Further, Hajeck teaches how a memory subsystem continues operations for a period of time after an anomaly is detected. *See id.* at 4:10-20 ("Even if the anomaly is in the form of a complete interruption or termination of power from the host 32, the charge pump 46 continues to provide power to the controller 40 (and possibly to other active components, as mentioned above) for at least the minimum time period, T_{VREG}, needed to complete all outstanding operations. For example, if a write operation is in progress and the memory subsystem 30 has write data stored in its volatile RAM buffer (not shown), backup power will be provided for a time period sufficient for the controller 40 to finish writing this data to the EEPROM memory 42, and if necessary, to back up any configuration data stored in volatile memory.").

B. Background Technology

1. JEDEC Standards

139. A Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory devices and memory modules at the time. *See supra* ¶61. For example, Harris discloses Double Data Rate (DDR) memory devices, including DDR2, DDR3 and DDR4 memories. *See* Ex. 1023 at [0009], [0011]. A Skilled Artisan would have understood that

these memories were already standardized, such as DDR2 and DDR3, or were in the process of being standardized by JEDEC, such as DDR4. Each of these standard JEDEC memory devices is discussed below. Harris also discloses Dual In-Line Memory Modules (DIMMs), including unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), and fully-buffered DIMMs (FBDs or FBDIMMs). *See* Ex. 1023 at [0009]. A Skilled Artisan would have understood that these memory modules were already standardized, including the Advanced Memory Buffers (AMB) for FBDIMMs as discussed above, *supra* ¶¶134-137.

a) DDR SDRAM Specification (JESD79) (Ex. 1045)

140. I understand that the JEDEC Solid State Technology Association published the standard DDR SDRAM Specification in June 2000 ("JESD79"). Ex. 1045 at Cover. Similar to the 054 Patent, JESD79 specifies multiple supply voltages, as shown in the table below.

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6
I/O Termination Voltage (system)	VTT	VREF–0.04	VREF+0.04	V	7

Id. at p.54 (excerpt of "Electrical Characteristics and DC Operation Conditions"). In particular, the nominal supply voltage VDD is 2.5 volts or 3.3 volts. The nominal input/output (I/O) supply voltage VDDQ is 2.5 volts, which is the average of the minimum voltage at 2.3 volts and maximum voltage at 2.7 volts. The

nominal I/O reference voltage VREF is half of VDDQ or 1.25 volts, as is the nominal I/O termination voltage VTT.

b) DDR2 SDRAM Specification (JESD79-2B) (Ex. 1026)

141. I understand that the JEDEC Solid State Technology Association published the standard DDR2 SDRAM Specification in September 2003 ("JESD79-2B"). Ex. 1026 at Cover. Similar to the 054 Patent, JESD79-2B specifies multiple supply voltages, as shown in the table below.

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	2. 3
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	4

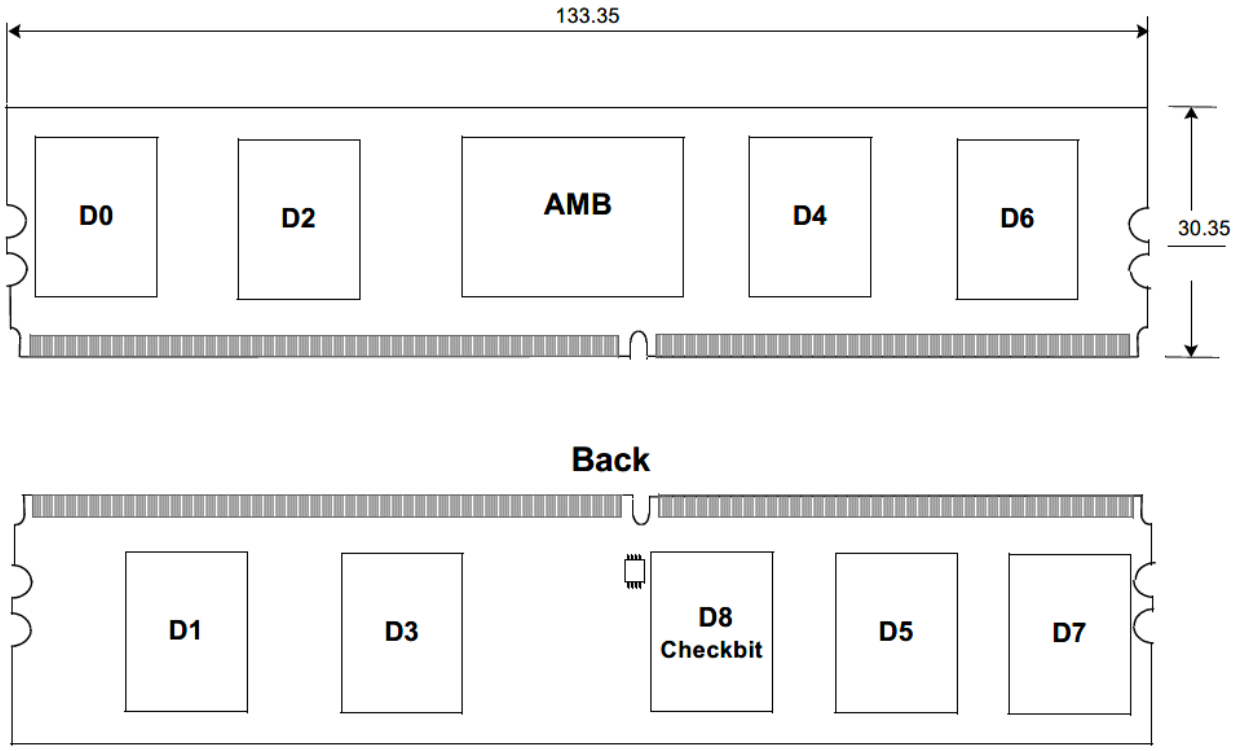
NOTE 1 There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.
NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
NOTE 4 VTT of transmitting device must track VREF of receiving device.
NOTE 5 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

Ex. 1026 at p.49 (Table 16). In particular, there are five symbols for voltages at two different voltage amplitudes. VDD is a supply voltage typically at 1.8 volts, VDDL is a supply voltage for a delay-locked loop (DLL) typically at 1.8 volts, VDDQ is a supply voltage for output typically at 1.8 volts, VREF is an input reference voltage typically at one-half of VDDQ or 0.9 volts, and VTT is a termination voltage that is typically at VREF, or one-half of VDDQ (0.9 volts). As

I noted above, Harris explicitly references standard DDR2 memory technology. *Supra* ¶130.

c) FBDIMM Standards (Exs. 1027-28)

142. As mentioned above, Harris expressly states that its memory module can be implemented as a fully-buffered DIMM (FBD or FB-DIMM). *Supra* ¶¶130, 134, 137, 139. As shown in the example FBDIMM below, a Skilled Artisan would have understood that an FBDIMM includes an advanced memory buffer (AMB) and one or more memory devices (e.g., DDR2 SDRAM).



Ex. 1028 at 37; *see also id.* at 9, 13-16, 38-40. The AMB has a high-speed differential point-to-point link terminated at 1.5 volts and the DRAM uses an interface terminated at 0.9 volts. *Id.* at 9 ("Supply voltages," "Buffer Interface,"

and "DRAM Interface"), 13-16 (illustrating AMB device with V_{CC} termination and DRAM devices with V_{TT} termination).

d) DDR3 SDRAM Specification (JESD79-3A) (Ex. 1046)

143. I understand that the JEDEC Solid State Technology Association published revision A of the standard DDR3 SDRAM Specification in September 2007 ("JESD79-3A"). Ex. 1046 at Cover. Similar to the 054 Patent, JESD79-3A specifies multiple supply voltages, including those shown in the table below.

V_{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V

Id. at p.13. The power supply VDD is provided at 1.5 volts +/- 0.075 volts and the power supply VDDQ is provided at 1.5 volts +/- 0.075 volts.

2. PCI Bus Standards (Ex. 1031)

144. At the time of the 054 Patent, devices utilizing the peripheral component interconnect ("PCI") local bus were well known. Accordingly, a Skilled Artisan would have been familiar with the PCI Local Bus Specification, which governed the "protocol, electrical, mechanical, and configuration specification" for such components and expansion boards. *See* Ex. 1031 at p.1.

145. For example, a Skilled Artisan would have known that the PCI Local Bus Specification established the required and optional pins for each device under the PCI standard. *See id.* at p.7, Fig. 2-1 (reproduced below).

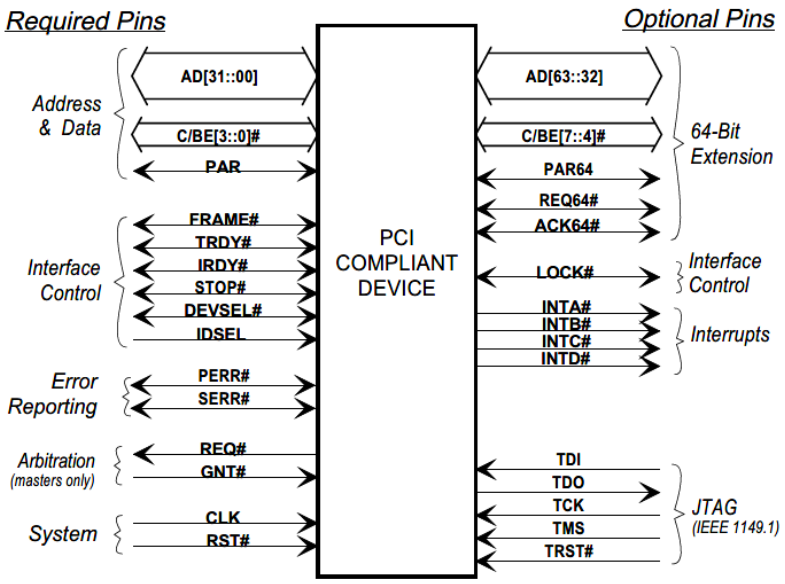


Figure 2-1: PCI Pin List

Accordingly, a Skilled Artisan would have known that all PCI devices receive, among other signals, address, data, and clock signals through pins connecting the PCI device to the host system. *See id.* at Fig. 2-1, pp.8-9.

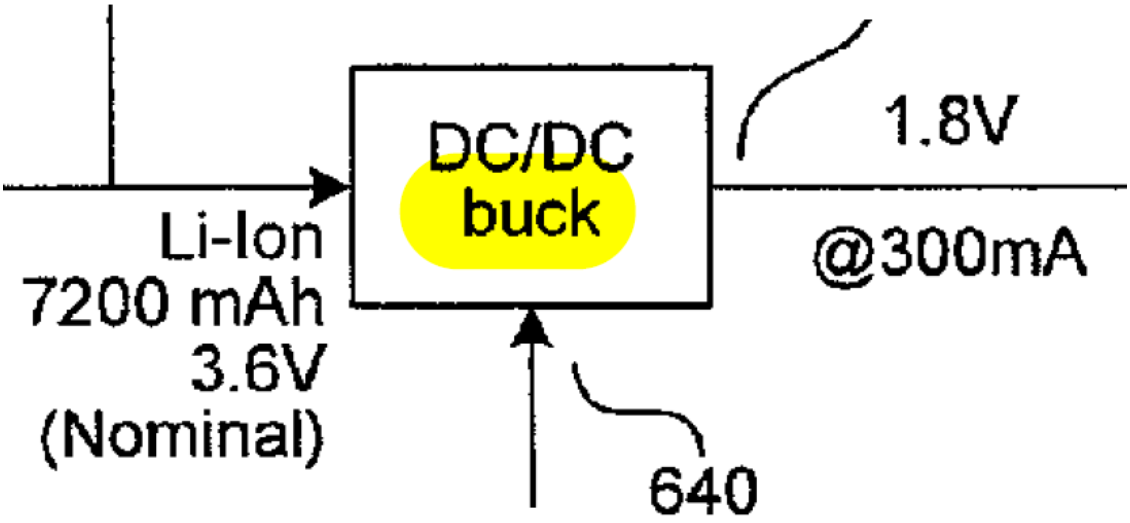
146. A Skilled Artisan would have also known that the PCI Local Bus Standard established the power requirements for PCI devices, including expansion boards. *See id.* at p.137 (discussing power requirements generally), pp.150-51 (discussing power requirements for expansion boards). In particular, the standard specifies that all PCI connectors require four power rails (+5V, +3.3V, +12V, and -12V). *See id.* at p.137. However, the standard further specifies that expansion boards can draw all of their power through the +5V or +3.3V power rails. *See id.* at p.150. Accordingly, a Skilled Artisan would have known that a PCI expansion board could be powered via the +5V input from the host system.

3. Buck Converters (Exs. 1032, 1058)

147. At the time of the 054 Patent, buck converters were well-known switching devices used to step down the voltage between its input and output. Buck converters were one of "the most basic building blocks in power electronics." EX1050 at 1:21. For example, Simplified Design of Switching Power Supplies by John D. Lenk ("Lenk") discloses that a "buck circuit is used when the input voltage is always greater than the desired output voltage (and is also known as a *step-down* converter)." Ex. 1058 at 3 (describing Fig. 1-3), 5 (Fig. 1-3). In particular, the duty cycle of the switching converter determines the output voltage relative to the input voltage. *Id.* at 5 ("1.3 Switching-Regulatory Theory") ("The output voltage V_O is always equal to the input voltage V_{IN}, times the duty cycle D, or $V_O = DV_{IN}$."). Lenk also shows that the configurations and waveforms for a theoretical buck converter were well-known to a Skilled Artisan. *See id.* at 12-16 ("1.5.4. Buck or Step-Down").

148. As another example, Power Electronics: Converters, Applications, and Design by Ned Mohan et al. ("Mohan") discloses that a step-down or buck converter is a "basic converter topolog[y]." Ex. 1032 at 161. Mohan explains that, "[a]s the name implies, a step-down converter produces a lower average output voltage than the dc input voltage V_d." *Id.* at 164. Similar to Lenk, Mohan explains that the output voltage can be controlled "[b]y varying the duty ratio." *Id.*

149. As a further example, Amidi discloses using a buck converter on a memory module to convert a higher input voltage to a lower output voltage. *See, e.g.*, Ex. 1024 at Fig. 6 (showing a DC/DC buck converter 640 to step down a higher voltage to a lower one, reproduced below in part, annotated).



150. As I explained above, a Skilled Artisan would have understood that a step-down regulated voltage can also be provided by means other than a "buck converter." *Supra* ¶53. For example, a non-switching, linear regulator, such as a low-dropout regulator (LDO) can be used to reduce the output voltage relative to the input voltage. However, a Skilled Artisan would have also understood that an LDO is substantially different from the claimed "buck converter." *See, e.g.*, Ex. 1059 at 5:23-30 ("Switch mode buck converters have become popular due to two attractive features: first, they are more efficient than traditional low drop out

regulators (LDO) (e.g., up to 95%) and second, they can provide relatively high currents with lower power dissipation on chip than an LDO can.").

C. The Combinations Relied on Here

151. The combinations analyzed here were obvious to a Skilled Artisan at the time and are straightforward applications of the teaching of the prior art. Each of the Grounds discussed below involves the combination of prior art references in view of the knowledge of a Skilled Artisan.

152. Ground 1 involves Harris in view of the FBDIMM Standards. In this combination, I discuss three voltage mappings (A, B, and C), as described below.

153. Ground 2 involves the references in Ground 1 (Harris in view of the FBDIMM Standards) in combination with Amidi, which discloses a memory module with battery backup. This combination involves the same voltage mappings as Ground 1.

154. Ground 3 involves Ground 2 in view of Hajeck, which discloses detecting undervoltage and overvoltage conditions. This combination involves the same voltage mappings as Ground 2.

155. Ground 4 involves Spiers in view of Amidi. In this combination, I discuss two voltage mappings (A and B), including voltages corresponding to DDR2 or DDR3 DRAMs.

156. Ground 5 involves Ground 4 in view of Hajeck, which discloses detecting undervoltage and overvoltage conditions. This combination involves the same voltage mappings as Ground 4.

D. Reasons to Combine

157. A Skilled Artisan would have been motivated to make these combinations for at least the following reasons.

1. Ground 1: Harris in view of JEDEC's FBDIMM Standards

158. As mentioned above, Ground 1 involves Harris in view of the FBDIMM Standards. *Supra* ¶152.

159. A Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory devices and memory modules already standardized, or in the process of being standardized, at the time. For example, Harris discloses Double Data Rate (DDR) memory devices, including DDR2, DDR3 and DDR4 memories. *See* Ex. 1023 at [0009], [0011]. A Skilled Artisan would have understood that these memories were already standardized, such as DDR2 and DDR3, or were in the process of being standardized by JEDEC, such as DDR4. *Supra* ¶140 (DDR SDRAM), ¶141 (DDR2 SDRAM), ¶142 (FBDIMM), ¶143 (DDR3 SDRAM). Harris also discloses Dual In-Line Memory Modules (DIMMs), including unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), and fully-buffered DIMMs (FBDIMMs). *See*

Ex. 1023 at [0009]. A Skilled Artisan would have understood that these memory modules were already standardized, including FBDIMMs with an Advanced Memory Buffer (AMB). *See id.*; *see also* Ex. 1027, Ex. 1028.

160. Similarly, the 054 Patent discloses widely-known JEDEC standards. For example, the background of the 054 Patent references a "JEDEC standard DRAM DIMM." Ex. 1001 at 3:42-43; *see also id.* at 3:12-13 ("form factor of a standard DIMM"), 17:59-61 ("standard access protocol, such as JEDEC's DDR DRAM"). The 054 Patent also references specific standards, "such as DDR, DDR2, DDR3, DDR4" (*id.* at 13:42-43), and connectors, such as "a standard 240-pin DDR2 edge connector" (*id.* at 22:7-8).

161. Like the 054 Patent, Harris discloses that its memory module with on-board voltage conversion can be implemented in a form factor that is compatible with JEDEC standards. *Supra* ¶129; *see* Ex. 1023 at Abstract, Fig. 1A, [0009], [0011], [0013]. Indeed, Harris discloses different types of standard memory devices (e.g., DDR2, DDR3, and DDR4) and standard memory modules (e.g., UDIMM, RDIMM, FBDIMM). *Id.* The JEDEC standards describe requirements for many aspects of memory modules and devices, including for the voltage supply of JEDEC-compliant devices. In fact, Harris expressly discloses "industry standard memory modules" and such "power requirements." Ex. 1023 at [0002], [0012] (describing power supply rails for standard modules). Harris also teaches

generating appropriate local voltage levels for powering memory devices and buffer circuits on the memory module. *See, e.g., id.* at Abstract ("A memory assembly module including an on-board voltage regulator for converting an externally supplied voltage into appropriate local voltage levels for powering memory devices of the memory assembly module."), [0009] ("a Vdd path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices" and "the Vcc path may be energized to appropriate voltage levels depending on the buffer and DIMM technology"). Thus, a Skilled Artisan implementing the memory module teachings of Harris would have done so in view of this knowledge as evidenced by the relevant JEDEC memory standards.

162. In my view, a Skilled Artisan would have been familiar with the relevant JEDEC memory standards, including the FBDIMM Standards. Even if one were to argue that Harris does not sufficiently disclose a memory module in accordance with the teachings of these JEDEC memory standards or that a Skilled Artisan would not be familiar with the FBDIMM Standards, it would have been obvious to a Skilled Artisan who would have been motivated to implement Harris's module using memory devices and/or buffer devices standardized by JEDEC, including the FBDIMM Standards, as explained below.

163. Harris expressly refers to JEDEC and describes JEDEC-standardized memory. *Supra* ¶159. Such memory standards were widely-recognized and used to implement memory at the time and standard memory devices compliant with the JEDEC standards were readily available as well. In particular, a Skilled Artisan would have been motivated to combine Harris with the FBDIMM Standards. *See generally* Exs. 1027, 1028. Harris expressly contemplates implementing its module as an FBDIMM, which includes an AMB (buffer). Ex. 1023 at [0009] ("[T]he DIMM configuration of an exemplary memory module may include . . . fully buffered DIMMs (FBDs) . . . ."), [0012] (providing an example of a "standard FBD module").

164. In fact, Harris provides embodiments that relate to an FBDIMM. For example, as shown in Figure 1A below, the DIMM 100A includes a buffer 112 that receives voltage supplies through a Vcc path and is coupled to a bidirectional memory controller interface path 114 and daisy-chain interface 116. *Id.* at Fig. 1A, [0009] ("bidirectional memory controller interface path 114 as well as a second voltage path 106, typically referred to as a V_{CC} path, are provided with respect to the buffer component 112 , wherein the V_{CC} path may be energized to appropriate voltage levels depending on the buffer and DIMM technology" and "a suitable daisy-chain interface 116 is provided for coupling the buffer component 112 to a next memory module").

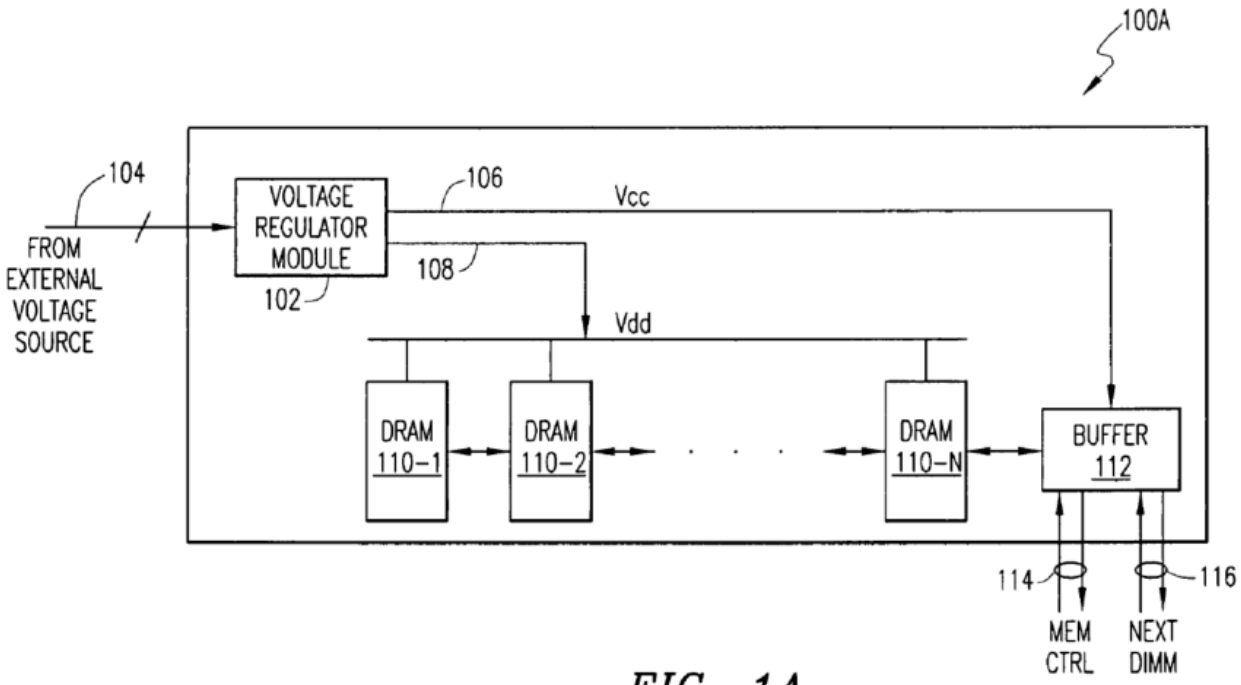


FIG. 1A

Harris explains that the buffer is provided for buffering command, address, and data signals for the memory devices—a function of FBDIMMs that a Skilled Artisan would have recognized. *Id.* at [0009] ("In the illustrated embodiment of Fig. 1A, for instance, the DIMM configuration of the memory module 100A is exemplified as a fully buffered DIMM wherein a buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices 110-1 through 110-N").

165. As another example of FBDIMMs, Figure 3 of Harris is a block diagram of a memory assembly 300 with daisy-chained memory boards 306-1 through 306-M.

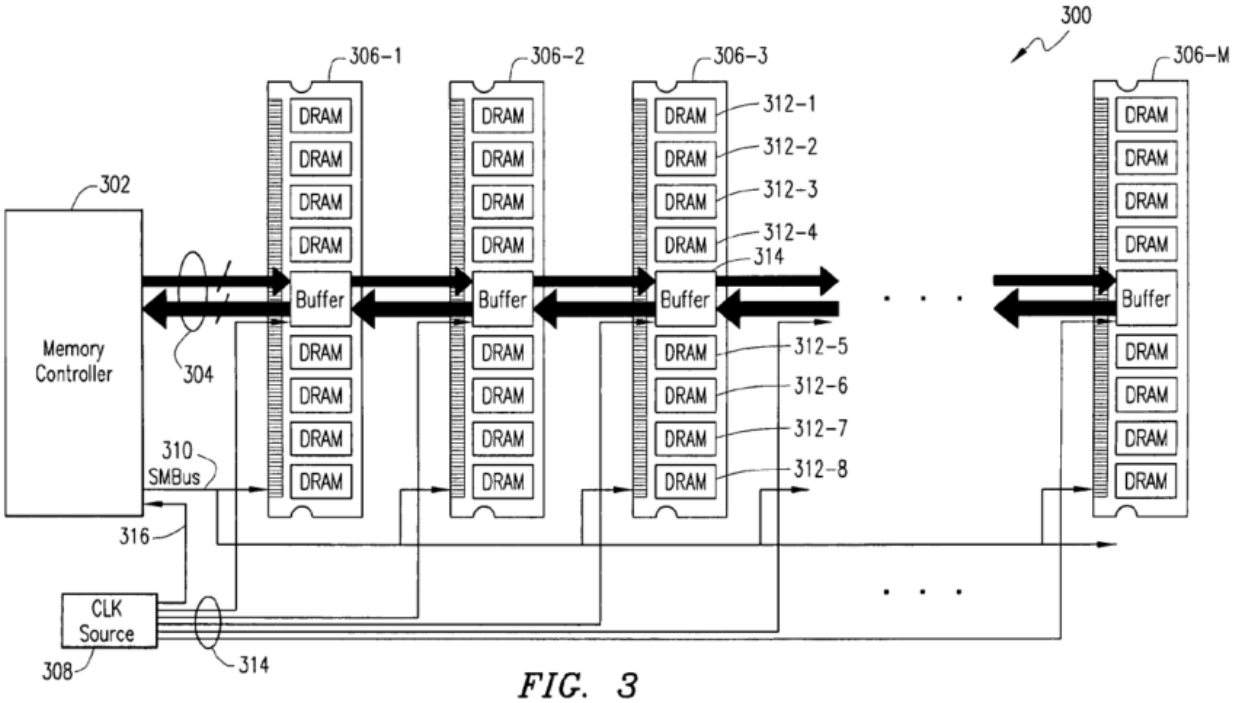


FIG. 3

Ex. 1023 at Fig. 3, [0017]. As shown, memory boards 306 include buffers 314 that are daisy-chained together by a bidirectional memory link. *See id.* Again, this is a feature of FBDIMMs that a Skilled Artisan would have recognized. Accordingly, a Skilled Artisan would have looked to the FBDIMM Standards to implement the memory module teachings of Harris to create an FBDIMM with an AMB buffer. In addition to this explicit motivation in Harris, using the FBDIMM Standards to implement an FBDIMM with an AMB buffer is a predictable variation to a Skilled Artisan given that the AMB standard was well-known in the field of memory technology that was readily available at the time in a cost-effective manner for daisy-chain topologies. *See, e.g.*, Ex. 1027 (JESD82-20) at p. 1 ("The Advanced Memory Buffer allows buffering of memory traffic to support large memory

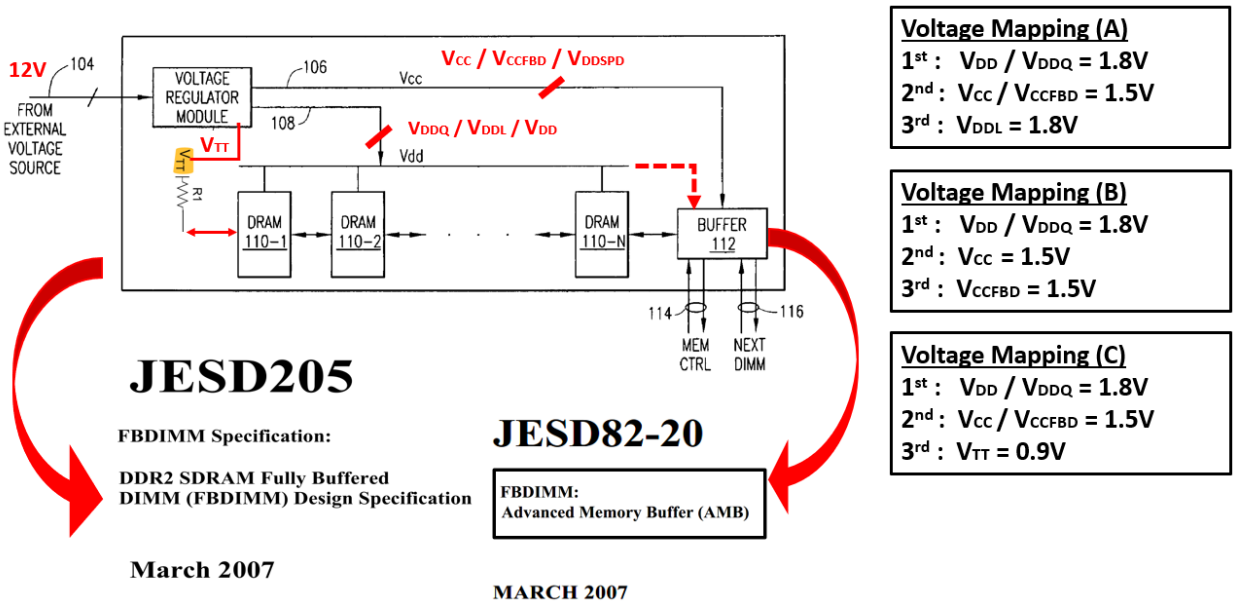
capacities. ... Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM."); *see also* Ex. 1060 at 1:65-2:3 (describing the desirability of "meeting JEDEC standards for synchronous DRAMs so that versatile synchronous DRAMs may be provided and applied in many design applications"). Additionally, the combination simply combines prior art elements (e.g., Harris's memory module with a standard AMB) in known ways to yield predictable results in accordance with the relevant standards (e.g., an FBDIMM-compliant memory module with on-board voltage conversion).

166. As part of the FBDIMM Standards, the JESD205 DDR2 SDRAM FBDIMM Design Specification is a document that a Skilled Artisan would have been motivated to combine with Harris. *See generally* Ex. 1028. As explained above, Harris expressly contemplates implementing its module as an FBDIMM. *Supra* ¶¶163-165; *see also* Ex. 1023 at [0009], [0012], [0017], Figs. 1A, 3. Accordingly, a Skilled Artisan would have looked to the FBDIMM Standards (including JESD205) to implement the memory module teachings of Harris for an FBDIMM, such as one with DDR2 SDRAM memory. In addition to this explicit motivation in Harris, using the FBDIMM Standards (including JESD205) to implement an FBDIMM is a predictable variation to a Skilled Artisan given that

the FBDIMM Standards were well-known in the field of memory technology and were readily available at the time in a cost-effective manner for daisy-chain topologies. *See, e.g.*, Ex. 1027 (JESD82-20) at p. 1 ("The Advanced Memory Buffer allows buffering of memory traffic to support large memory capacities. ... Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM."); *see also* Zuravleff (5,630,096) Ex. 1060 at 1:65-2:3 (describing the desirability of "meeting JEDEC standards for synchronous DRAMs so that versatile synchronous DRAMs may be provided and applied in many design applications"). Additionally, the combination simply combines prior art elements (e.g., Harris's memory module satisfying the FBDIMM design specification) to yield predictable results in accordance with the relevant standards at the time (e.g., an FBDIMM-compliant memory module with on-board voltage conversion).

167. In the combination of Harris and the FBDIMM Standards, a Skilled Artisan would have understood that multiple voltage supplies would be provided to the components of the memory module for proper operation. Accordingly, at least the following three voltage mappings would have been apparent to a Skilled Artisan, as shown in the figure below with examples of voltage amplitudes for the voltage supplies.

Ground 1: Harris with JEDEC's FBDIMM Standards



Ex. 1023 (Harris) at Fig. 1A (annotated); Ex. 1027 (JESD82-20); Ex. 1028 (JESD205). As shown, a 12-volt supply from an external voltage source is provided to the FBDIMM, as disclosed by Harris. *See, e.g.*, Ex. 1023 at [0012], [0013], [0016], [0020]. In accordance with JEDEC's FBDIMM Standards, Harris's Voltage Regulator Module provides several voltage supplies to the Advanced Memory Buffer (AMB, buffer 112), including VCC, VCCFBD, and VDD/VDDQ. Ex. 1023 (Harris) at [0009] ("the Vcc path may be energized to appropriate voltage levels depending on the buffer and DIMM technology"); *see also id.* at [0014] (disclosing a redundancy implementation with a "plurality of on-board VRMs"), Fig. 1B. In accordance with JEDEC's FBDIMM Standards, Harris's Voltage Regulator Module provides several voltage supplies to the memory devices (DRAM 110-1 to 110-N), including VDD, VDDL, VDDQ, and VTT. *Id*. at [0009]

("a Vdd path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices").

168. To the extent Patent Owner argues that two different voltage amplitudes recited in the claims can have the same amplitude, voltage mapping (A) ("Ground 1A") includes three voltage supplies at three voltage amplitudes. The first voltage is VDD or VDDQ (e.g., each at 1.8 volts); the second voltage is VCC or VCCFBD (e.g., each at 1.5 volts); and the third voltage is VDDL (e.g., at 1.8 volts):

- VDD or VDDQ (e.g., each at 1.8 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1028 (JESD205) at 9; *see also* Ex. 1027 (JESD82-20) at 31-32 (AMB receiving "V_{DD} Supply voltage DRAM interface"), 44 (describing DRAM interface on AMB receiving V_{DD}), 83 (same), Ex. 1028 at 9 (V_{DD}/V_{DDQ} for DRAM and AMB), 11, 13-16, 30, 33 (same).
- VCC or VCCFBD (e.g., each at 1.5 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1027 at 78, 82, 83; Ex. 1028 (JESD205) at 9, 30-32.
- VDDL (e.g., at 1.8 volts). *See, e.g.*, Ex. 1028 (JESD205) at 17-20; Ex. 1026 (JESD79-2B) at p.6.

169. Similarly, to the extent Patent Owner argues that two different voltage amplitudes recited in the claims can have the same amplitude, voltage mapping (B) ("Ground 1B") includes three voltage supplies at three voltage amplitudes. The first voltage is VDD or VDDQ (e.g., at 1.8 volts); the second voltage is VCC (e.g., at 1.5 volts); and the third voltage is VCCFBD (e.g., at 1.5 volts):

- VDD or VDDQ (e.g., each at 1.8 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1028 (JESD205) at 9, 17-20; Ex. 1026 (JESD79-2B) at pp.6-7; *see also* Ex. 1027 (JESD82-20) at 31-32 (AMB receiving "V_{DD} Supply voltage DRAM interface"), 44 (describing DRAM interface on AMB receiving V_{DD}), 83 (same), Ex. 1028 at 9 (V_{DD}/V_{DDQ} for DRAM and AMB), 11, 13-16, 30, 33 (same).

- VCC (e.g., at 1.5 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1027 at 78, 82, 83; Ex. 1028 (JESD205) at 9.

- VCCFBD (e.g., at 1.5 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1027 at 78, 82, 83; Ex. 1028 (JESD205) at 9, 30-32.

170. Voltage mapping (C) ("Ground 1C") includes three voltage supplies at three different voltage amplitudes. The first voltage is VDD or VDDQ (e.g., each at 1.8 volts); the second voltage is VCC or VCCFBD (e.g., each at 1.5 volts); and the third voltage is VTT (e.g., at 0.9 volts):

- VDD or VDDQ (e.g., each at 1.8 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1028 (JESD205) at 9, 17-20; Ex. 1026 (JESD79-2B) at pp.6-7; *see also* Ex. 1027 (JESD82-20) at 31-32 (AMB receiving "V_{DD} Supply voltage DRAM interface"), 44 (describing DRAM interface on AMB receiving V_{DD}), 83 (same), Ex. 1028 at 9 (V_{DD}/V_{DDQ} for DRAM and AMB), 11, 13-16, 30, 33 (same).

- VCC or VCCFBD (e.g., each at 1.5 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1027 at 78, 82, 83; Ex. 1028 (JESD205) at 9, 30-32.

- VTT (e.g., at 0.9 volts). *See, e.g.*, Ex. 1028 (JESD205) at 9, 15, 68.

2. Ground 2: Ground 1 in view of Amidi

171. Ground 2 involves Ground 1 in view of Amidi. *Supra* ¶153. As explained above, Ground 1 involves Harris in view of the FBDIMM Standards. *Supra* ¶¶152, 158-170. As explained below, it would have been obvious to a Skilled Artisan to incorporate battery backup power, as taught by Amidi, when implementing the memory module teachings of Harris to address the case of a power outage or clock malfunction. *See, e.g.*, Ex. 1024 at 1:28-35.

172. Harris and Amidi are both in the field of memory technology, and more specifically disclose memory modules. *See* Ex. 1023 at Abstract; Ex. 1024 at Abstract. Harris itself is concerned with reliability of the power supply and teaches an option to use redundant external power sources. *See* Ex. 1023 at [0014] (describing a "redundancy implementation"), [0016] (describing a "redundant VRM" to "power a redundant voltage path"), Figs. 1B, 2. Similar to the redundant implementation in Harris, Amidi teaches a redundant power source. *See, e.g.*, Ex. 1024 at Abstract. Amidi recognizes that it is useful to keep data on the memory module with a backup power supply on the module itself, such as a battery supply, when the entire system surrounding the memory module loses power. *See* Ex. 1024 at 1:28-35 ("Thus, it may be useful to provide an option for keeping data in volatile memory even when a surrounding system loses power. Moreover, it may also be useful to keep data in volatile memory when a surrounding system suffers some

form of an error which causes a clock to malfunction even though power is still supplied. Likewise, it may be useful to provide volatile memory which has non-volatile characteristics in short- or medium-term time periods."), 2:6-26 ("A system, method and apparatus is provided for a clock and power fault detection for a memory module. . . . For example, one may provide a system with a controller which detects voltage levels and clock signals, a state machine for operating a memory in backup mode, and a battery and supporting circuitry for supplying backup power. Similarly, one may provide a process which operates to detect voltage and clock signals, initiate backup operations, maintain memory (through refresh, for example), and detect a recovery status. Providing such a system or process within a memory module can be very helpful, as it avoids the need for system circuitry in a computer system or similar device which can maintain a memory module from outside the module. Moreover, such a system or process may be tuned to the specific memory module, instead of requiring overhead to deal with many different types of memory modules, for example."). Therefore, a Skilled Artisan would have been motivated to use Amidi's on-board redundant power source when implementing the FBDIMM memory module of Harris to keep data on the memory module with a backup power supply when the external supply to the memory module loses power.

Samsung Electronics Co., Ltd.
Ex. 1069, p. 82

173. In particular, a Skilled Artisan would have been motivated to use the backup power management and logic functionality of Amidi that includes monitoring the system supply, detecting faults, initiating backup power, and initiating refresh operations in the volatile memory to maintain data. Ex. 1024 at 2:6-26, Fig. 15. Although I understand that bodily incorporation is not required for obviousness, Amidi's functionality could be incorporated in the FBDIMM memory module of Harris as illustrated below in an annotated version of Figure 5 of Amidi and Figure 1A of Harris.

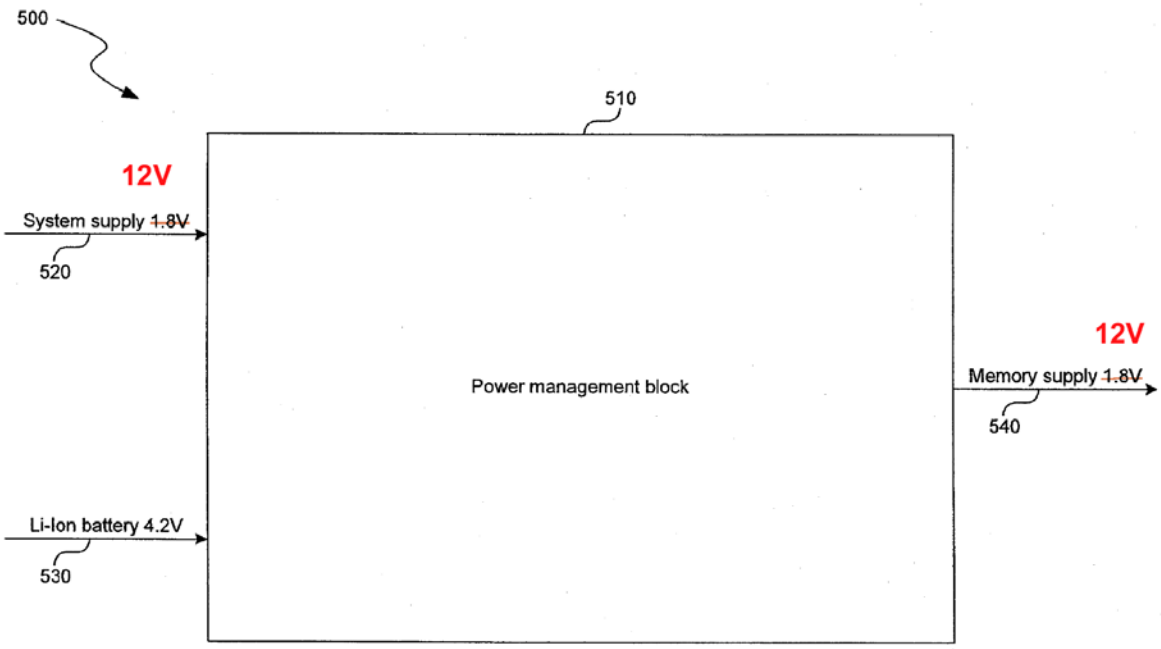


FIG. 5

Ex. 1024 at Fig. 5 (annotated with teachings of Harris). As shown in annotated Figure 5 of Amidi, a Skilled Artisan would have recognized that the power management block of Amidi would be modified to receive the external voltage

source of Harris instead of the 1.8-volt system supply in Amidi. *See* Ex. 1024 at Fig. 5 (annotated above). Such a modification would have been well within the level of skill at the time. *See, e.g.*, Ex. 1058 at 5 ("Switching-Regulator Theory") and 12-15 ("Buck or Step-Down"). Amidi itself discloses converting the 4.2-volt lithium-ion battery input to the power management block 510 to a voltage of 1.8V for the memory supply 540. *See* Ex. 1024 at Fig. 5. Amidi also discloses in its Figure 6 embodiment that a DC/DC boost converter is used to step-up a voltage to a higher voltage level, a DC/DC buck converter is used to step-down a voltage to a lower voltage level, and a lithium-ion battery charger is provided a 5.0-volt supply. *See id.* at Fig. 6 (DC/DC boost converter 610 converting 1.8 volts system supply to 5.0 volts for a Li-Ion battery charger 620, DC/DC buck converter 640 converting 3.6 volts (nominal) from the battery to 1.8 volts for the memory power supply), 4:23-60 (describing Figure 6 embodiment). In addition, Harris expressly describes an embodiment in which the external voltage source of 12-volts is converted by the on-board VRM to the stepped-down voltage levels required on the memory module. *See* Ex. 1023 at [0012], [0013], [0016], [0020]; *see also* Ex. 1023 at pp. 3-4 (claims 4, 15, 23, 33).

174. In the combination, a Skilled Artisan would have understood to use switching DC-DC converters, such as buck and boost converters as taught by both Harris and Amidi, and select those to correspond to the voltages used in Harris. Ex.

1023 at [0010] ("Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM 102 for purposes of the present patent disclosure."); Ex. 1024 at Fig. 6 (showing the use of buck and boost converters to convert voltages to different levels). For example, a buck converter would step-down the 12-volt supply of Harris to a 5-volt supply for the lithium-ion battery charger of Amidi, and a boost converter steps-up the lithium-ion battery's voltage (e.g., 4.2 volts) to the 12-volt level used by the memory module, as Harris teaches. *See* Ex. 1024 at 4:14-60, Figs. 5-6; *see also* Ex. 1058 at 5 ("Switching-Regulator Theory") and 12-15 ("Buck or Step-Down"); Ex. 1032 at 161 (describing "dc-dc Switch-Mode Converters," including "Step-down (buck) converter[s]" and "Step-up (boost) converter[s]," and explaining that "only the step-down and the step-up are the basic converter topologies"). Thus, the power management block of Amidi outputs either the 12-volt external voltage or the battery supply boosted to the same voltage level.

175. Furthermore, a Skilled Artisan would have understood that Harris's module has a mode called S3 mode when implemented in accordance with the FBDIMM standards. In S3 mode, power to selected parts of the FBDIMM is switched off and the DRAM devices are put into a self-refreshing mode to save power without losing the data stored in those volatile DRAM devices. Ex. 1027 (JESD82-20) at 21 ("When the Advanced Memory Buffer core logic is in S3

power mode, … 1.8V supply is on. 1.5V, Vtt, and 3.3V are off. DRAMs are in self refresh …"), 39 ("S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode"). A Skilled Artisan would have recognized that the FBDIMM S3 mode of Harris's module is similar to Amidi's DRAM self-refreshing functionality. Ex. 1024 at Fig. 11, 2:16-19 ("Similarly, one may provide a process which operates to … maintain memory (through refresh, for example)"). Thus, a Skilled Artisan would have been motivated to use the S3 mode that was already available in Harris's module when implementing the backup power supply and logic functionality of Amidi, because S3 mode performs the function of refreshing the memory (e.g., self refresh), just like in Amidi. Indeed, a Skilled Artisan would have understood that the S3 mode was described in the FBDIMM standards for the very purpose of saving power in FBDIMM modules like Harris's which are used in servers and workstations. Ex. 1027 (JESD82-20) at 39 ("S3 current Specification … "very lower power state"); Ex. 1028 at 9 ("These SDRAM FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations.").

176. As shown in the annotations to Figure 1A of Harris in view of Amidi's teachings, a Skilled Artisan would have been motivated to implement the memory module of Harris with the functionality of Amidi's power management

and logic blocks for detecting system failures, and switching over to battery backup power.

Ground 2: Ground 1 and Battery Backup of Amidi

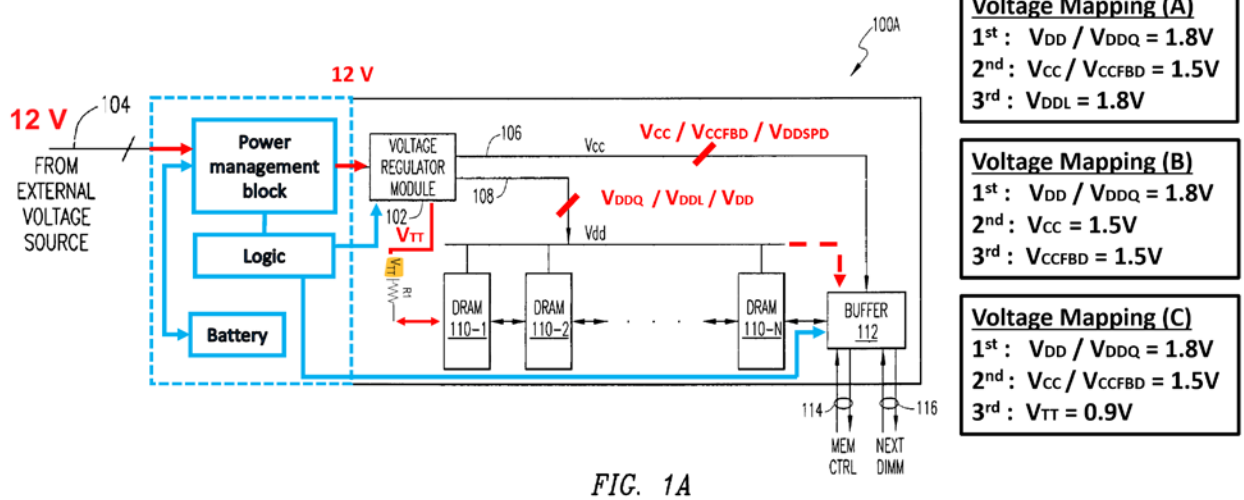


FIG. 1A

Ex. 1023 at Fig. 1A (annotated with teachings of Amidi). As shown, a 12-volt supply, sourced from either the 12-volt external voltage source or the boosted battery supply, is provided to the Voltage Regulator Module (102). *See e.g.*, Ex. 1023 at [0012], [0013], [0016], [0020]. Several voltage supplies are provided to the Advanced Memory Buffer (AMB, buffer 112), including VCC, VCCFBD, VDDSPD and VDD. In addition, several voltage supplies are provided to the memory devices (DRAM 110-1 to 110-N), including VDD, VDDL, VDDQ, and VTT. Further, the VTT voltage supply is provided to termination resistors on the memory module. *See, e.g.*, Ex. 1026 at pp. 6-7, p. 9 (describing power-up sequence for VDD, VDDQ, VDDL, and VTT), 49 (recommended range for VDD, VDDQ,

VDDL and VTT), 55 and 71 (showing VTT coupled through termination resistor, and defining VTT as half of VDDQ).

177. This straightforward modification of Harris's memory module in view of the teachings of Harris and Amidi and the knowledge of a Skilled Artisan simply uses a known technique (e.g., Amidi's battery backup techniques) to improve a similar device (e.g., Harris's memory module) in the same way (e.g., to provide a backup power supply using a battery). In addition, the modification merely applies a known technique (e.g., providing a backup power supply) to a known device (e.g., a memory module) that is ready for improvement to yield predictable results (e.g., redundancy when the system supply or clock fails).

178. As shown in the annotated figure above, there are at least three voltage mappings apparent to a Skilled Artisan. To the extent Patent Owner argues that two different voltage amplitudes recited in the claims can have the same amplitude, voltage mapping (A) ("Ground 2A") includes three voltage supplies at, for example, three voltage amplitudes. The first voltage is VDD or VDDQ (e.g., each at 1.8 volts); the second voltage is VCC or VCCFBD (e.g., each at 1.5 volts); and the third voltage is VDDL (e.g., at 1.8 volts). Voltage mapping (A) under Ground 2 is nearly identical to voltage mapping (A) under Ground 1. *See supra* ¶168.

179. Similarly, to the extent Patent Owner argues that two different voltage amplitudes recited in the claims can have the same amplitude, voltage mapping (B) ("Ground 2B") includes three voltage supplies, for example, at three voltage amplitudes. The first voltage is VDD or VDDQ (e.g., at 1.8 volts); the second voltage is VCC (e.g., at 1.5 volts); and the third voltage is VCCFBD (e.g., at 1.5 volts). Voltage mapping (B) under Ground 2 is nearly identical to voltage mapping (B) under Ground 1. *See supra* ¶169.

180. Voltage mapping (C) ("Ground 2C") includes three voltage supplies, for example, at three different voltage amplitudes. The first voltage is VDD or VDDQ (e.g., each at 1.8 volts); the second voltage is VCC or VCCFBD (e.g., each at 1.5 volts); and the third voltage is VTT (e.g., at 0.9 volts). Voltage mapping (C) under Ground 2 is nearly identical to voltage mapping (C) under Ground 1. *See supra* ¶170.

3. Ground 3: Ground 2 in view of Hajeck

181. Ground 3 involves Ground 2 in view of Hajeck, Ex. 1038 (US 6,856,556). It would have been obvious to a Skilled Artisan to combine the references in Ground 2 for the reasons discussed above. As discussed below, it would have been also obvious to a Skilled Artisan to combine the references in Ground 2 with the disclosure of Hajeck.

182. As discussed above, Hajeck is directed to "protecting storage subsystems, such as but not limited to flash memory cards, from damage and data loss caused by irregularities in a power signal provided by a host." Ex. 1038 at 1:10-13; *see supra* ¶138. In particular, Hajeck explains that "[t]he protection circuitry and methods of the present invention may also be incorporated into other types of storage subsystems, including volatile storage subsystems that store data within DRAM." *Id*. at 4:62-65.

183. Therefore, a Skilled Artisan would have understood that Hajeck is in the same field of memory subsystems as and analogous art to the 054 Patent and the prior art references of Ground 2, including Amidi and Harris, as each is directed to solving the problem of reliable data storage and, in particular, to protect against power failures. *See, e.g.*, Ex. 1038 (Hajeck) at Title ("Storage subsystem with embedded circuit for protecting against anomalies in power signal from host"), Ex. 1024 (Amidi) at Title ("Clock and power fault detection for memory modules"), Ex. 1023 (Harris) at Figs. 1B and 2, [0014], [0016] (disclosing using redundant power sources), Ex. 1001 at 11:15-21 ("The examples of FIGS. 3A and 3B are directed to architectures of a non-volatile DIMM (NVDIMM) NVDIMM system that may use a power subsystem (not shown) that can include a battery or a capacitor as a means for energy storage to copy DRAM memory data into Flash

memory when power loss occurs, is detected, or is anticipated to occur during operation.").

184. For example, Amidi discloses that "[s]ignal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two. If system supply 605 has a greater magnitude than reference voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660. If system supply 605 has a magnitude lower than reference voltage 675, then signal 670 causes power switch multiplexer 655 to choose battery power 650 for memory supply 660." Ex.1024 at 4:44-53. A Skilled Artisan would have understood from this disclosure that Amidi's voltage supervisory functionality switches to backup power when the input voltage is below a first threshold.

185. Hajeck explains that a "significant problem in the area of storage subsystems relates to data loss, data corruption, and circuitry damage caused by interruptions and other irregularities in the power signal supplied by the host system." Ex. 1038 at 1:15-18. For example, "power signal anomalies, such as power surges and spikes, can additionally cause permanent damage to the circuitry of the storage subsystem." *Id*. at 1:28-31. To solve these problems, Hajeck discloses a "voltage detection circuit 48 [that] is responsible for detecting anomalies in the power signal VIN supplied by the host on line 36, and for driving

the ready/busy signal to the 'busy' state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit 48 may be designed to generate a 'busy' signal whenever VIN falls below a certain level, such as 2.6 or 2.7 volts. The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected. To inhibit rapid transitions between the 'ready' and 'busy' states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition." Ex. 1038 at 3:30-40.

186. A Skilled Artisan would have understood from this disclosure of Amidi and Hajeck that Amidi's voltage supervisory block can be modified to detect voltage anomalies and switch to the backup power not only "[i]f system supply 605 has a magnitude lower than reference voltage 675" as disclosed by Amidi, Ex. 1024 at 4:44-53, but also "when the voltage exceeds a certain level" as taught by Hajeck, Ex. 1038 at 3:30-40. A Skilled Artisan would have been motivated to detect voltage anomalies when the input voltage is above a threshold in order to protect against "power signal anomalies, such as power surges and spikes, [which] can additionally cause permanent damage to the circuitry of the storage subsystem" as taught by Hajeck. Ex. 1038 at 1:28-31. For example, Harris specifically discloses a need to detect input voltages more than 15% above the

expected voltage, thus providing a motivation to include the functionality of Hajeck's voltage detection circuit 48 in the combination of Ground 3. *See* Ex. 1023 (Harris) at [0013] ("Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated, allowing low cost power distribution for system boards (such as, e.g., motherboards, cell boards, et cetera) wherein design requirements for bypass/hold-up capacitors may be relaxed or minimized.").

187. Indeed, the problems caused by such overvoltage conditions, and solutions to detect and protect against them, were well known at the time. *See, e.g.*, Ex. 1065 (Resnick) at [0002] ("Semiconductor devices, like most electronic products, are sensitive in their operation to supplied voltage levels. If voltage levels at working parts are lower than specified minimum requirements, the parts may malfunction. If voltage levels are higher than specified maximum requirements, the parts may malfunction and can also suffer catastrophic failure. In semiconductor memory devices, for example, such as Dynamic Random Access Memories (DRAMs), inadequate voltage levels may cause memory parts to malfunction by reading out or storing incorrect information."). A Skilled Artisan would have understood that, to avoid these well-known problems, a "conventional voltage detection circuit" referenced by Hajeck was readily available at the time

and was configured to detect both under and over voltage conditions. Ex. 1038 at 3:30-40; *see also* Ex. 1061 (ADM1060 Supervisory/Sequencing Circuit) at 15 ("All of the [supply fault] detectors can be programmed to detect undervoltage, overvoltage, or out-of-window (undervoltage or overvoltage) conditions"); Ex. 1063 (LMC6953 PCI Local Bus Power Supervisor) at 1 ("Under and over voltage detectors for 5V and 3.3.V") and 2 (listing specific Over Voltage and Under-Voltage Thresholds).

188. Therefore, modifying Amidi's voltage supervisory block to detect both undervoltage and over voltage conditions would have been obvious to a Skilled Artisan to prevent known problems caused by overvoltage conditions and was well within the level of skill at the time since "conventional," readily available voltage detection circuits implemented over and under voltage protection and the combination provided the predictable result of switching to backup power when such overvoltage and undervoltage conditions were detected.

4. Ground 4: Spiers in view of Amidi

189. Ground 4 involves Spiers in view of Amidi. *Supra* ¶155.

190. Spiers and Amidi are analogous art to the 054 Patent, as they are directed to providing data backup in memory modules in case of power failure.

191. The 054 Patent discloses a memory module for data backup that includes a volatile memory subsystem (1030, yellow), a non-volatile memory

subsystem (1040, green), circuitry (red) for interfacing with the computer system through a standard interface (orange), on one hand, and with the volatile (yellow) and non-volatile (green) memory subsystems on the other hand. Ex. 1001 (054 Patent) at Fig. 12 (reproduced below, annotated).

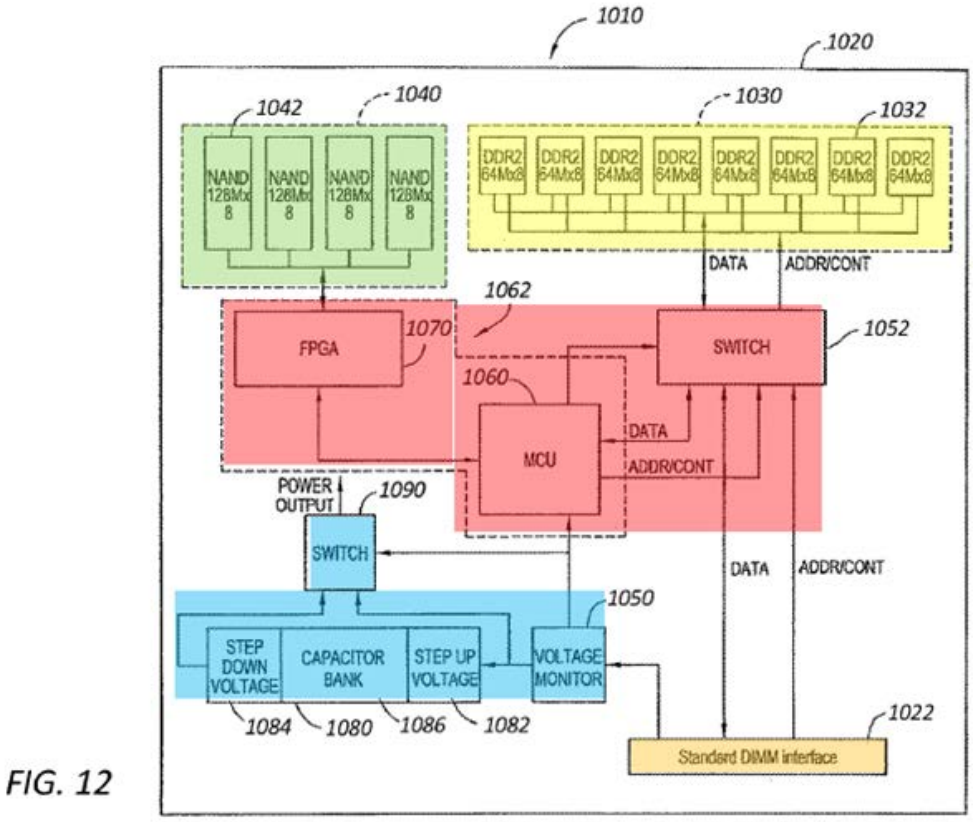
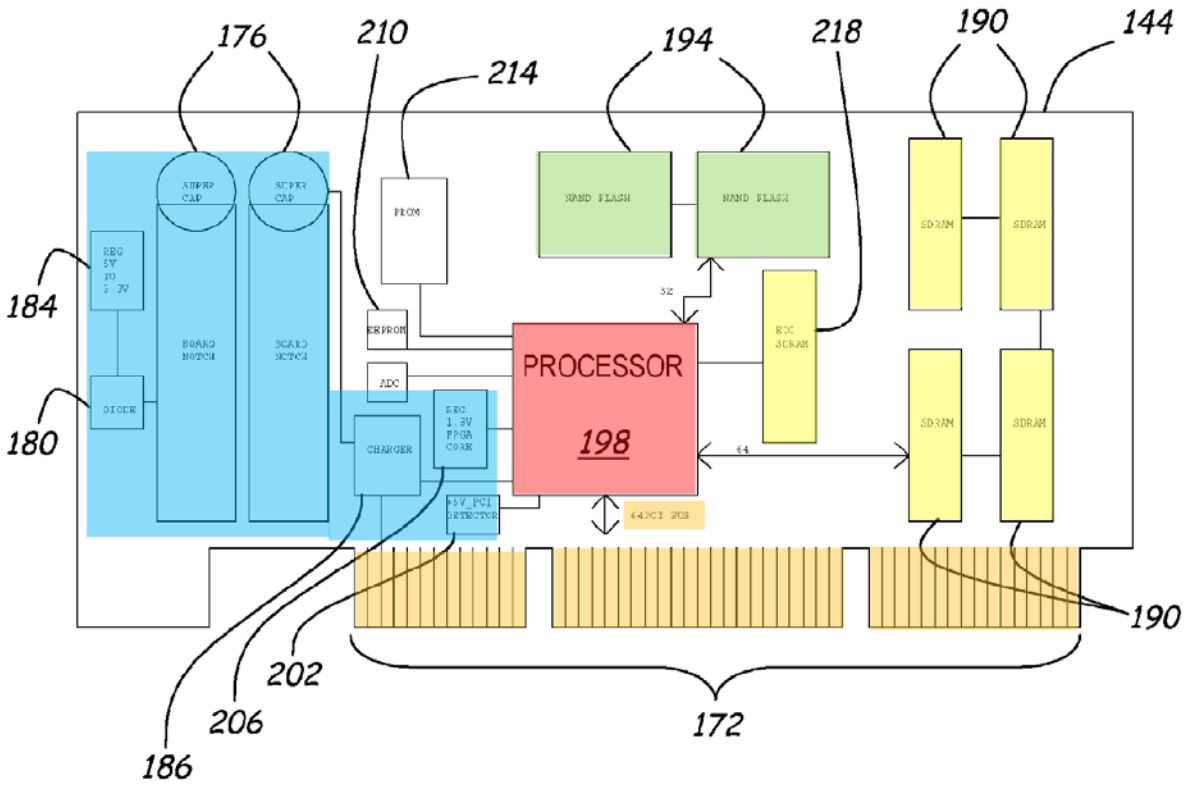


FIG. 12

192. The 054 Patent's module also includes a backup power supply (blue) based on a capacitor bank (180) which is used to power the memory module while the circuitry (red) transfers data from the volatile (yellow) to the non-volatile (green) memory if a voltage monitor (1050) detects a power interruption. *Id*. at 11:15-21, 20:43-57.

193. Years before the earliest priority date claimed by the 054 Patent, Spiers disclosed substantially the same structure. Just like in the 054 Patent, the memory module of Spiers (backup device 144) includes a processor (red) for interfacing with the computer system through a standard interface (orange), on one hand, and with on-board volatile (yellow) and non-volatile (green) memory, on the other hand. Ex. 1025 at Title, [0001], Fig. 5 (reproduced below, annotated). The backup device of Spiers also includes its own temporary power supply (blue). *Id*. at Fig. 5.



194. As shown in Fig. 5, the backup device of Spiers, in an embodiment, is implemented in a PCI card with volatile SDRAM memories (190 and 218, yellow)

and non-volatile memories (green) including NAND flash memories (194). *Id*. at [0037]. The 054 Patent uses the same type of memories. A Skilled Artisan would have understood that SDRAM and flash memory devices were "off-the-shelf components that are commercially available." *See, e.g.*, Ex. 1064 (Bonella) at [0029] (disclosing a memory module with DRAM and FLASH memory) and [0032] (explaining that these were "off-the-shelf components"); *see also id*. at [0036] (identifying DDR2 DRAM as an example for DRAM devices).

195. As in the 054 Patent, Spiers's backup power supply (blue) is implemented using capacitors (176), although Spiers also discloses that it can use "a battery, or any other suitable power source." Ex. 1025 at Abstract. The backup power supply also includes a charger (186) to charge the capacitors (or the battery) when the power through the PCI connector is available. *Id.* at [0037]. If a power detection circuit 202 detects power interruption, the processor (198) "switches to the backup power source and receives power from the backup power source while moving the data from the backup volatile memory to the backup non-volatile memory." *Id.* at Abstract, [0037]. Spiers discloses that the backup power supply includes voltage converters, such as voltage regulators 184 and 206, to supply regulated voltage to the components, including processor 198, that participate in this operation of moving the data from the volatile to the non-volatile memory. *Id.*

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196. Amidi also discloses power fault detection for memory modules. Ex. 1024 at Title. Amidi uses a battery as the backup power source (like the alternative implementation of Spiers), and discloses further details about its power management block that handles power interruptions, including the use of buck converters (e.g., 640) to provide backup power for the memory devices and logic devices controlling the power management in case of power failure. *Id*. at Fig. 6 (reproduced below).

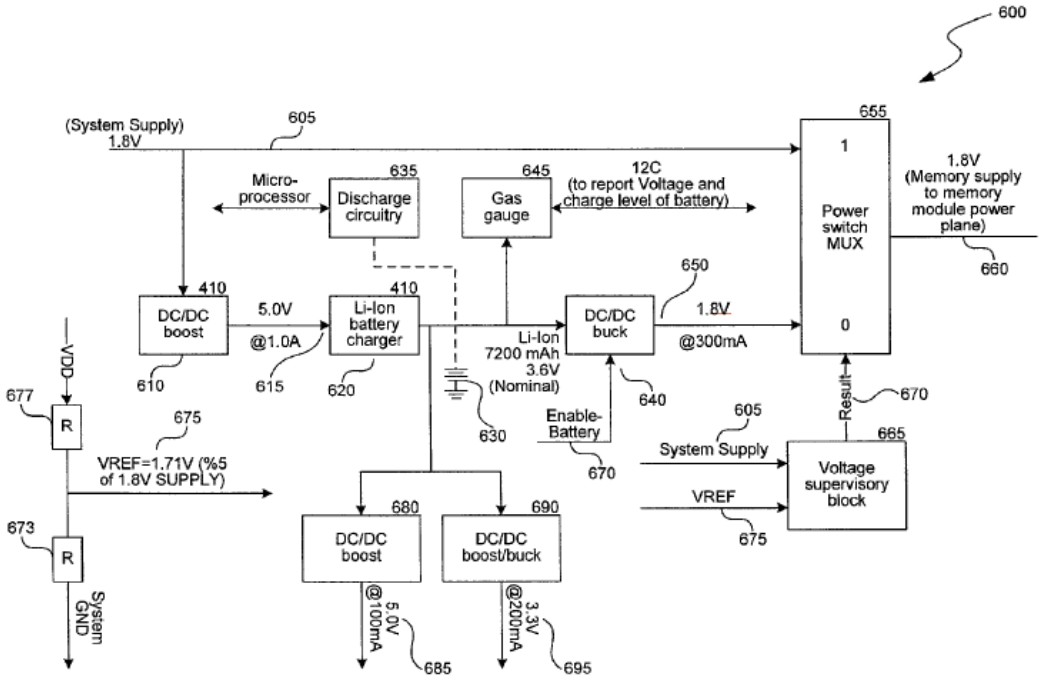
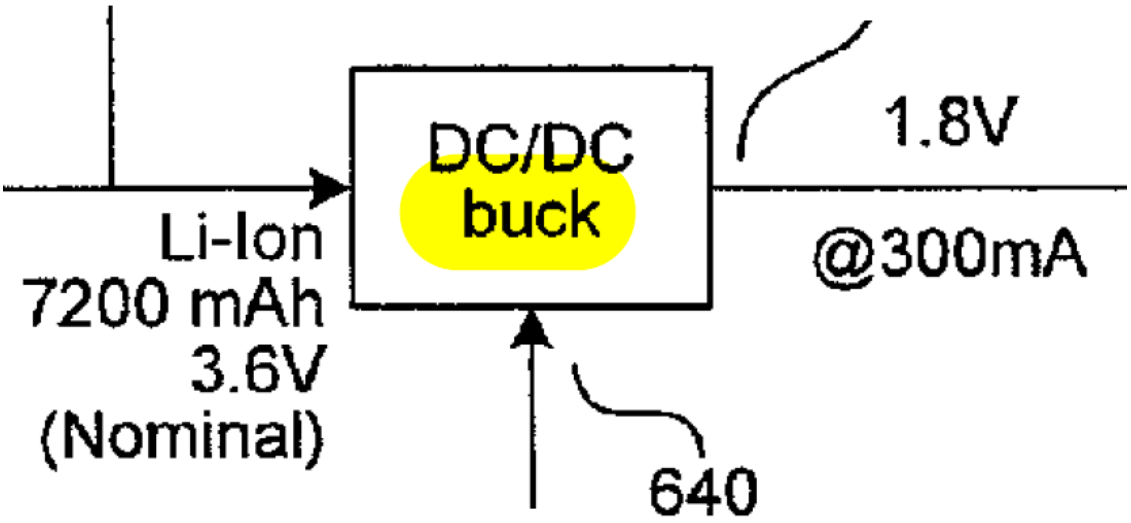


FIG. 6

197. Accordingly, a Skilled Artisan would have been motivated to consult Amidi's disclosure and look for specific implementation details when implementing the memory module of Spiers. For example, Spiers discloses volatile memory including SDRAM devices without identifying any specific

SDRAM devices. Ex. 1025, e.g., at Fig. 5 and [0010, 0037-38]. Therefore, a Skilled Artisan would have been motivated to look at analogous prior art references, such as Amidi, which discloses specific types of SDRAM devices, such as DDR, and DDR2 SDRAMs, to be used in memory modules. Ex. 1024 at Figs. 3 and 13, 7:52-59, 10:17-20. As another example, Spiers discloses voltage regulators 184 and 206 without identifying any specific voltage regulator. Ex. 1025 at Fig. 5 and [0037]. Therefore, a Skilled Artisan would have been motivated to look at analogous prior art references, such as Amidi, which discloses specific types of voltage regulators, such as boost, buck, and boost/buck voltage converters, to be used for providing regulated voltages on a memory module. Ex. 1024 at Fig. 6 (reproduced below in part, annotated) and 4:30-43.



198. Similarly, Spiers discloses switching a power supply from the system power to the backup power, Ex.1025, e.g., at Abstract and Fig. 14, and Amidi

discloses a specific structure, a power switch multiplexer, for implementing such a switch, Ex. 1024 at Fig. 7 and 4:56-5:9. Therefore, it would have been obvious to a Skilled Artisan to combine the teaching of Spiers and Amidi.

199. Furthermore, a Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory devices and memory modules already standardized, or in the process of being standardized, at the time. *See supra* ¶61. For example, Spiers discloses SDRAM memory devices. *See* Ex. 1025 at [0010]. A Skilled Artisan would have understood that such SDRAM memory devices were already standardized, including DDR2 and DDR3 SDRAMs, or were in the process of being standardized by JEDEC, such as DDR4 SDRAMs. *See* Ex. 1026; Ex. 1046. A Skilled Artisan would have also understood that these JEDEC standards describe requirements, among others, for the voltage supply of the corresponding JEDEC compliant devices.

200. Similarly, the 054 Patent discloses and relies on widely-known JEDEC standards. For example, the background of the 054 Patent references a "JEDEC standard DRAM DIMM." Ex. 1001 at 3:42-43; *see also id.* at 3:12-13 ("form factor of a standard DIMM"), 17:59-61 ("standard access protocol, such as JEDEC's DDR DRAM"). The 054 Patent also references specific standards, "such as DDR, DDR2, DDR3, DDR4" (*id.* at 13:42-43), and standard connectors, such as "a standard 240-pin DDR2 edge connector" (*id.* at 22:7-8).

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201. A Skilled Artisan would have thus recognized, and been motivated to use, DDR2 or DDR3 SDRAMs when implementing the SDRAMs in the backup device of Spiers, and to power the DRAMs according to the relevant JEDEC standards (e.g., JESD79-2B and JESD79-3A). *See* Ex. 1026; Ex. 1046. Accordingly, at least the following voltage mappings would have been apparent to a Skilled Artisan, as shown in the figure below with examples of voltage amplitudes for the voltage supplies.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

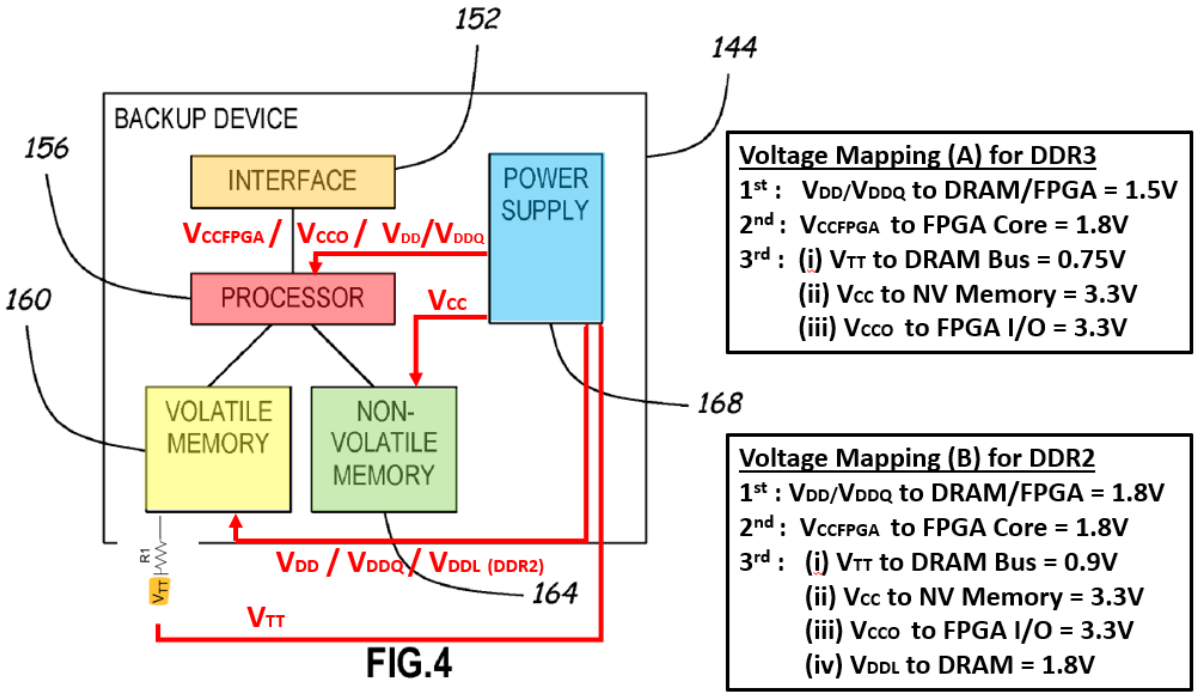


FIG.4

Ex. 1025 at Fig. 4 (annotated). A Skilled Artisan would have also understood that the choice to use either DDR2 or DDR3 DRAMs would dictate the voltages that must be produced by the power supply (blue, above) for V_{DD} and V_{TT}.

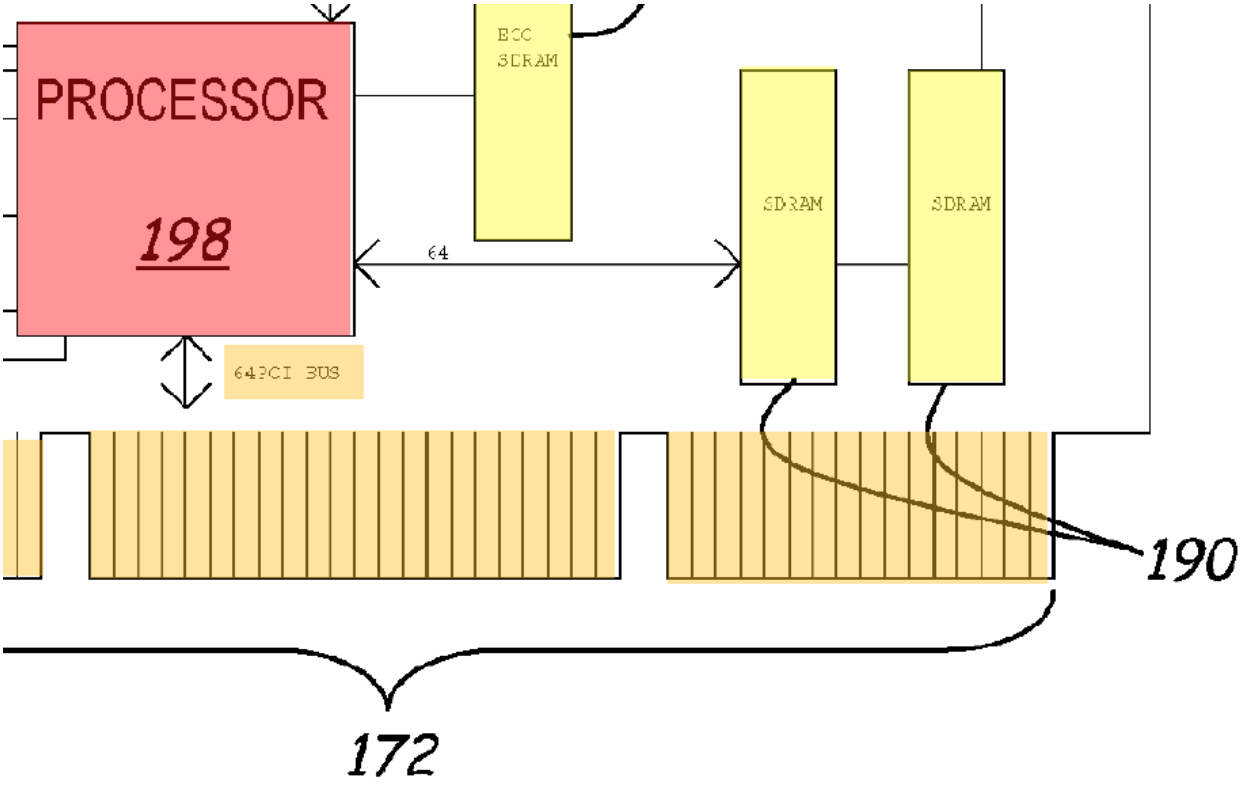
202. Voltage Mapping (A) ("Ground 4A") corresponds to an implementation of Spiers's backup device with DDR3 DRAMs and includes three voltage supplies, for example, at three different voltage amplitudes. The first voltage is VDD or VDDQ (e.g., at 1.5 volts); the second voltage is VCCFPGA (e.g., at 1.8 volts); and the third voltage is VTT (e.g., at 0.75 volts), VCC (e.g., at 3.3 volts), or VCCO (e.g., at 3.3 volts).

- VDD or VDDQ (e.g., at 1.5 volts). *See, e.g.*, Ex. 1046 (JESD 79-3A) at p.10.
- VCCFPGA (e.g., at 1.8 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1042 (Murata Power Supply Reference Guide for Xilinx FPGAs) at 2, 16.
- VTT (e.g., at 0.75 volts). *See, e.g.*, Ex. 1045 (JESD79) at pp. 8, 54, 60; Ex. 1046 (JESD 79-3A) at pp. 15, 109, 123.
- VCC or VCCO (e.g., each at 3.3 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1042 (Murata Power Supply Reference Guide for Xilinx FPGAs) at 2, 16; Ex. 1049 (Micron, NAND Flash Memory Datasheet) at 1, 38.

203. For example, a Skilled Artisan would have understood that, in an implementation of Spiers where DDR3 DRAMs are used for the volatile memory (yellow, above), the VDD (and VDDQ) supply voltage is provided to the DRAMs at 1.5 volts and that the DRAMs are coupled, through a termination resistor, to the termination voltage VTT, which is equal to one-half of VDD/VDDQ or 0.75 volts ("Voltage Mapping A"). *See* Ex. 1046 at pp. 10, 15 (explaining the order of turning

on VDD, VDDQ and VTT), 109 (defining VTT as half of VDDQ), 123 (showing VTT being coupled through RTT).

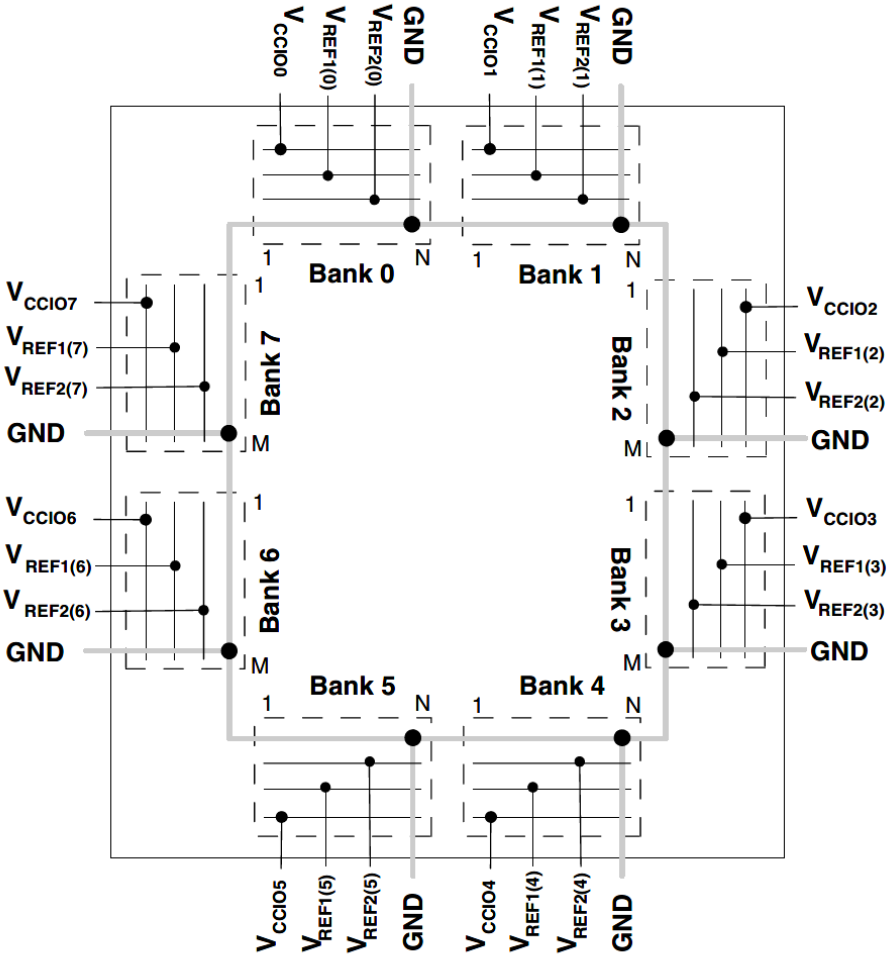
204. A Skilled Artisan would have understood from this disclosure of Spiers that processor 198, like the AMB in the FBDIMM standards, receives the same VDD/VDDQ voltage as the SDRAMs in order to interface with the SDRAMs. *See, e.g.*, Ex. 1025 at Fig. 5 (reproduced below in part, showing a 64-bit bus between the processor 198, red, and the SDRAMs 190, yellow).



Indeed, a Skilled Artisan would have understood at the time that FPGAs, like the FPGA processor 198 of Spiers, were configured to receive a separate voltage to interface with devices that use a voltage for communication other than the FPGA

core. *See, e.g.*, Ex. 1067 (LatticeXP FPGA datasheet), 2-23 (Fig. 2-27, reproduced below showing separate voltages VCCIO0-VCCIO7, one for each interface of the FPGA); 2-24 through 2-25 (Table listing different communication standards supported by the FPGA).

Figure 2-27. LatticeXP Banks



Note: N and M are the maximum number of I/Os per bank.

Therefore, a Skilled Artisan would have understood that the processor 198 which interfaces with SDRAM devices also receives the VDD/VDDQ voltage of the SDRAMs in addition to their own power supply in order to meet the specific

SDRAM voltage requirements for signaling. *See, e.g.*, Ex. 1026 (JESD79-2B) at 49-91 (AC & DC operating conditions); Ex. 1046 (JESD79-3A) at 100-126 (Chapters 7-9, including AC & DC Operating Conditions, AC and DC Input Measurement Levels, AC and DC Output Measurement Levels); Ex. 1067 (LatticeXP FPGA datasheet), 2-23 (Fig. 2-27, reproduced above showing separate voltages VCCIO0-VCCIO7, one for each interface of the FPGA); 2-24 through 2-25 (Table listing different communication standards supported by the FPGA); Ex. 1027 at pp.7, 29 (describing a power supply of an AMB as "I/O buffer voltage for DDR2 buffers" and "Supply voltage DRAM Interface").

205. Voltage Mapping (B) ("Ground 4B") corresponds to an implementation of Spiers's backup device with DDR2 DRAMs and includes three voltage supplies at, for example, three different voltage amplitudes. The first voltage is VDD or VDDQ (e.g., at 1.8 volts); the second voltage is VCCFPGA (e.g., at 1.8 volts); and the third voltage is VTT (e.g., at 0.9 volts), VCC (e.g., at 3.3 volts), or VCCO (e.g., at 3.3 volts), or to the extent Patent Owner argues that two different voltage amplitudes recited in the claims can have the same amplitude, the third voltage is VDDL (e.g., at 1.8 volts).

- VDD or VDDQ (e.g., at 1.8 volts). *See, e.g.*, Ex. 1026 (JESD79-2B) at p.7.
- VCCFPGA (e.g., at 1.8 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1042 (Murata Power Supply Reference Guide for Xilinx FPGAs) at 2, 16.

- VTT (e.g., at 0.9 volts). *See, e.g.*, Ex. 1028 (JESD205) at 9, 15, 68.
- VCC or VCCO (e.g., each at 3.3 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1042 (Murata Power Supply Reference Guide for Xilinx FPGAs) at 2, 16; Ex. 1049 (Micron, NAND Flash Memory Datasheet) at 1, 38.
- VDDL (e.g., at 1.8 volts). *See, e.g.*, Ex. 1028 (JESD205) at 9, 17-20; Ex. 1026 (JESD79-2B) at p.6.

206. For example, a Skilled Artisan would have understood that, in an implementation of Spiers where DDR2 DRAMs are used for the volatile memory (yellow, above), the VDD (and VDDQ) supply voltage is provided to the DRAMs at 1.8 volts and that the DRAMs are coupled, through a termination resistor, to the termination voltage VTT at 0.9 volts ("Voltage Mapping B"). *See* Ex. 1026 at pp. 6-7, p. 9 (describing power-up sequence for VDD, VDDQ, VDDL, and VTT), 49 (recommended range for VDD, VDDQ, VDDL and VTT), 55 and 71 (showing VTT coupled through termination resistor, and defining VTT as half of VDDQ).

207. Further, "Voltage Mapping A(ii)" and "Voltage Mapping B(ii)" each maps the VCC voltage to the third voltage at 3.3 volts for the non-volatile memory (green, figure above) and "Voltage Mapping A(iii)" and "Voltage Mapping B(iii)" each maps the VCCO voltage to the third voltage at 3.3 volts for the FPGA input/output (I/O) (red, above). In addition, a Skilled Artisan would have understood that, in an implementation of Spiers where DDR2 DRAMs are used for the volatile memory (yellow, above), the VDDL supply voltage, which is mapped

to the third voltage in "Voltage Mapping B(iv)," is provided to the DRAMs at 1.8 volts for a delay-locked loop. Ex. 1026 at p.49 (Table 16).

5. Ground 5: Ground 4 in view of Hajeck

208. Ground 5 involves Ground 4 in view of Hajeck. Ex. 1038 (US 6,856,556). It would have been obvious to a Skilled Artisan to combine the references in Ground 4 for the reasons discussed above. As discussed below, it would have been also obvious to a Skilled Artisan to combine Ground 4 with the disclosure of Hajeck.

209. For the reasons discussed above with reference to Grounds 3, Hajeck is analogous art to the 054 Patent and to Amidi. *Supra* ¶¶181-188. Hajeck is also analogous art to Spiers since both are directed to solving the problem of preventing data loss in memory modules in case of power anomalies, such as power failure. Ex. 1038 (Hajeck) at 4:10-21 ("Even if the anomaly is in the form of a complete interruption or termination of power from the host 32, the charge pump 46 continues to provide power to the controller 40 (and possibly to other active components, as mentioned above) for at least the minimum time period, TVREG, needed to complete all outstanding operations. For example, if a write operation is in progress and the memory subsystem 30 has write data stored in its volatile RAM buffer (not shown), backup power will be provided for a time period sufficient for the controller 40 to finish writing this data to the EEPROM memory 42, and if

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necessary, to back up any configuration data stored in volatile memory."); Ex. 1025 (Spiers) at Abstract ("The backup data storage device further includes a backup power source such as a capacitor, a battery, or any other suitable power source, and upon detection of a power interruption, switches to the backup power source and receives power from the backup power source while moving the data from the backup volatile memory to the backup non-volatile memory.").

210. Spiers explains that a "common requirement is that the data storage system securely store data, meaning that stored data will not be lost in the event of a power loss or other failure of the storage system." Ex. 1025 at [0002]. To detect a power failure, Spiers discloses "monitoring the voltage at a +5 volt pin" and "a power detection circuit that, in this [PCI card] embodiment, is a +5V PCI detector 202." *Id*. at [0037] and [0054]. A Skilled Artisan would have understood from this disclosure that, in the PCI implementation, Spiers uses a known PCI voltage detector which monitors the +5 volt power supply to detect a power failure.

211. As discussed above with reference to Ground 3, Hajeck discloses the problems related to both undervoltage and overvoltage conditions and, to solve these problems, Hajeck discloses a "voltage detection circuit 48 [that] is responsible for detecting anomalies in the power signal VIN .... A conventional voltage detection circuit may be used … to generate a 'busy' signal whenever VIN falls below a certain level … [and] may also be designed to generate a busy signal

when the voltage exceeds a certain level, and/or when other types of anomalies are detected." Ex. 1038 at 3:30-40. A Skilled Artisan would have understood that, to avoid these well-known problems, a "conventional voltage detection circuit" referenced by Hajeck was readily available at the time and was configured to detect both under and over voltage conditions. Ex. 1038 at 3:30-40; *see also* Ex. 1061 (ADM1060 Supervisory/Sequencing Circuit) at 15 ("All of the [supply fault] detectors can be programmed to detect undervoltage, overvoltage, or out-of-window (undervoltage or overvoltage) conditions"). A Skilled Artisan would have understood that such a voltage detection circuit was available specifically for monitoring PCI power supplies. Ex. 1063 (LMC6953 PCI Local Bus Power Supervisor) at 1 ("Under and over voltage detectors for 5V and 3.3.V") and 2 (listing a typical Over Voltage Threshold of 5.6V and a typical Under-Voltage Threshold of 4.4V for a 5V power supply).

212. A Skilled Artisan would have understood from this disclosure of Spiers and Hajeck that Spiers's +5V PCI detector can be implemented to detect voltage anomalies and switch to the backup power "whenever VIN falls below a certain level … [and] when the voltage exceeds a certain level" as taught by Hajeck, Ex. 1038 at 3:30-40. A Skilled Artisan would have been motivated to detect voltage anomalies in both cases. For example, when Spiers's +5V PCI detector detects that the input voltage is above a threshold, switching to the backup

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voltage would protect against "power signal anomalies, such as power surges and spikes, [which] can additionally cause permanent damage to the circuitry of the storage subsystem" as taught by Hajeck. Ex. 1038 at 1:28-31.

213. Therefore, implementing Spiers's +5V PCI detector to detect both undervoltage and overvoltage conditions would have been obvious to a Skilled Artisan at the time in order to prevent known problems caused by overvoltage conditions. Such an implementation was well within the level of skill at the time since "conventional," readily available voltage detection circuits for PCI cards implemented over and under voltage protection and provided the predictable result of switching to backup power when such overvoltage and undervoltage conditions were detected.

V. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE 054 PATENT

214. My analysis below is based on my understanding of the law and other information discussed above, including the five Grounds and various voltage mappings discussed above.

A. Claims 1-30 Are Unpatentable Over Grounds 1, 2, and/or 3

215. As explained below claims 1-3, 15 are unpatentable over Ground 1 (Harris in view of the FBDIMM Standards). In addition, claims 1-30 are unpatentable over Ground 2 (Ground 1 further in view of Amidi) and Ground 3 (Ground 2 further in view of Hajeck).

1. Claim 1 is Unpatentable

216. Claim 1 is unpatentable as the prior art references in each of Ground 1 (Voltage Mappings A, B, and C) and Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [1.a] Preamble

217. The preamble of claim 1 requires "*[a] memory module comprising.*"

218. Harris teaches and discloses this limitation to a Skilled Artisan in each of Grounds 1 through 3. In addition, for Grounds 1, 2, and 3, Harris in view of the FBDIMM Standards teaches and discloses this limitation to a Skilled Artisan.

219. Harris explains that "industry standard memory modules, e.g., Dual In-line ***Memory Modules*** (DIMMS) [are] populated with dynamic random access memory (DRAM) devices." Ex. 1023 at [0002] (emphasis added); *see also id.* at [0009] ("memory module 100A [] may be embodied as a memory board assembly operable in a computer system"). Harris discloses that the DIMM can have different configurations, including registered DIMMs (RDIMMs) or fully buffered DIMMs (FBDs). *See id.* at [0009] ("[T]he DIMM configuration of an exemplary memory module may include unbuffered DIMMs, registered DIMMs (RDIMMs), or fully buffered DIMMs (FBDs) ...").

220. For example, as shown in Figure 1A of below, Harris discloses an embodiment with an FBD.

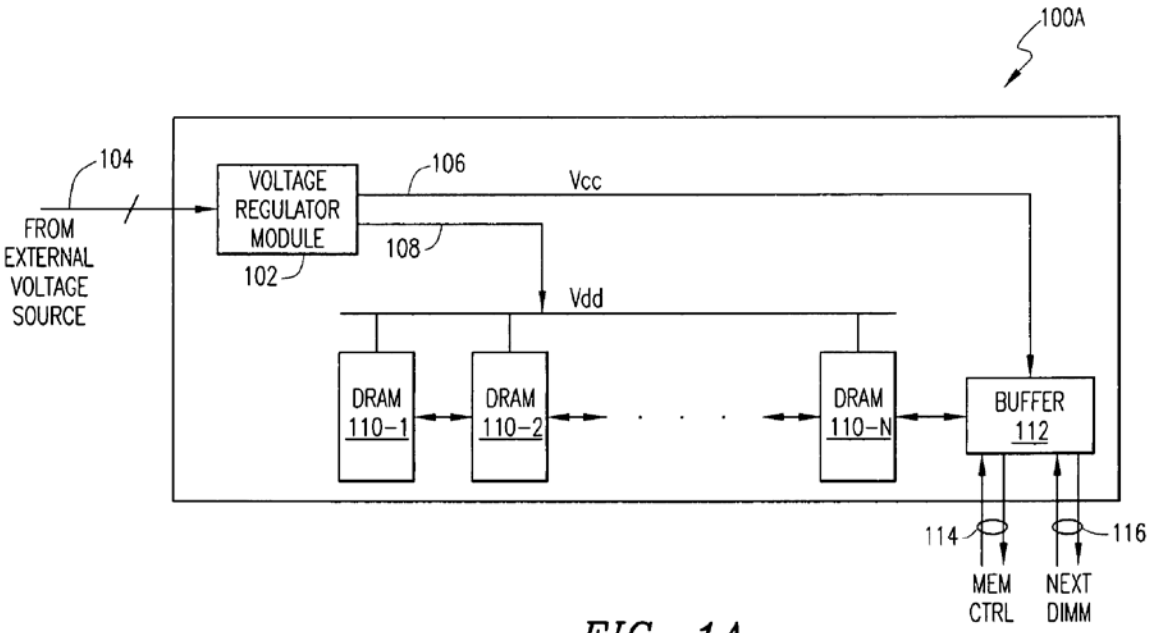


FIG. 1A

Id. at Fig. 1A; *see also id.* at [0009] ("[T]he DIMM configuration of the memory module 100A is exemplified as ***a fully buffered DIMM*** wherein a buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices 110-1 through 110-N.") (emphasis added).

221. As shown below in Figure 3, Harris also discloses an FBD implemented in a system such that the "memory controller 302 is operable to drive a bidirectional memory link 304 to which a plurality of memory boards 306-1 through 306-M are coupled in a daisy-chain fashion at their respective buffers." *Id.* at [0017].

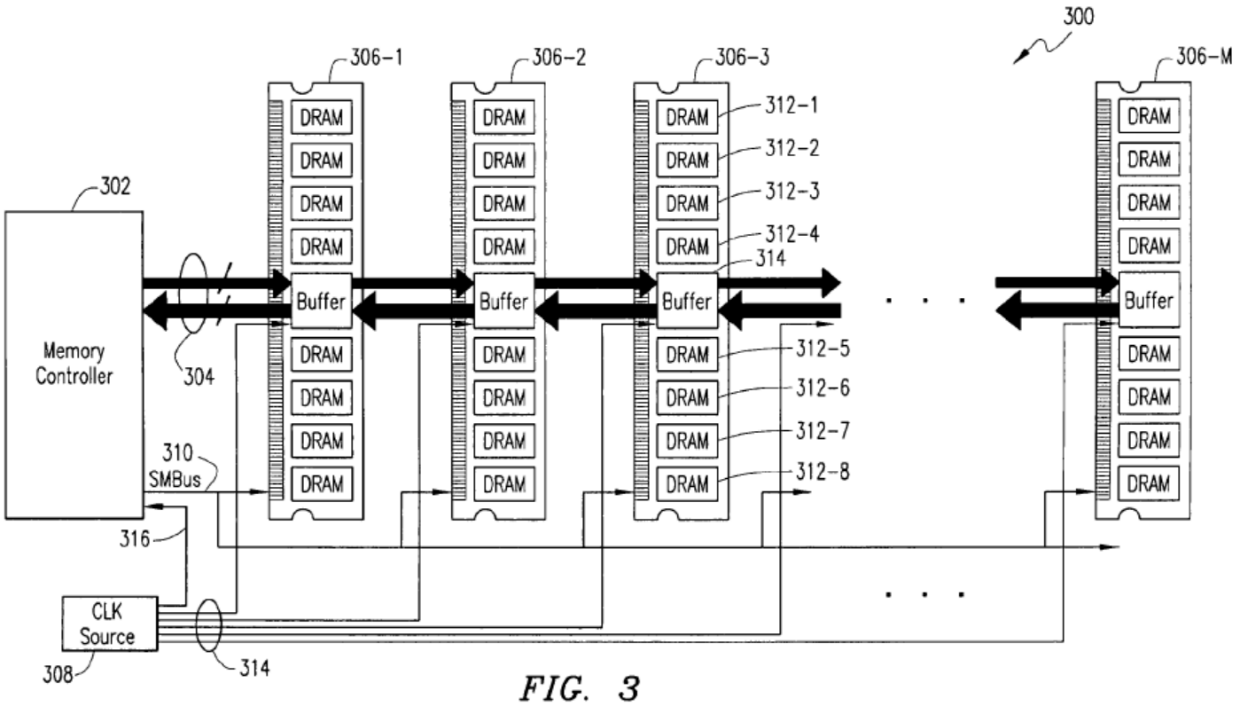
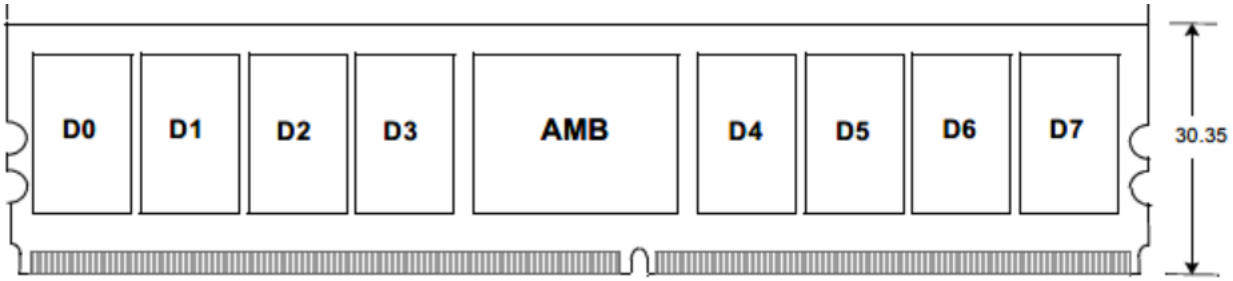


FIG. 3

Id. at Fig. 3.

222. A Skilled Artisan would have recognized that "industry standard memory modules" include fully buffered memory modules with form factors standardized by the Joint Electron Device Engineering Council (JEDEC). Ex. 1023 at [0013]; [0020] ("advantageously accommodat[ing]" "industry-standard form factors"). For example, a Skilled Artisan would have recognized that the JEDEC standard JESD205 (part of the FBDIMM Standards) discloses a "DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification." Ex. 1028 at 1. A Skilled Artisan would have also readily recognized that Harris discloses a form factor for its fully buffered memory module that is similar to that in the corresponding JEDEC standard. *Compare* a "memory board 306" of Ex. 1023 at Fig. 3

(reproduced above) *with* the front of raw cards B and C in Ex. 1028 at 38 (reproduced below, in part).



223. Accordingly, to the extent the preamble of claim 1 is limiting, Harris alone, or in combination with the FBDIMM Standards, satisfies "*[a] memory module comprising*."

b) [1.b] Printed Circuit Board Having an Interface

224. Claim 1 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*"

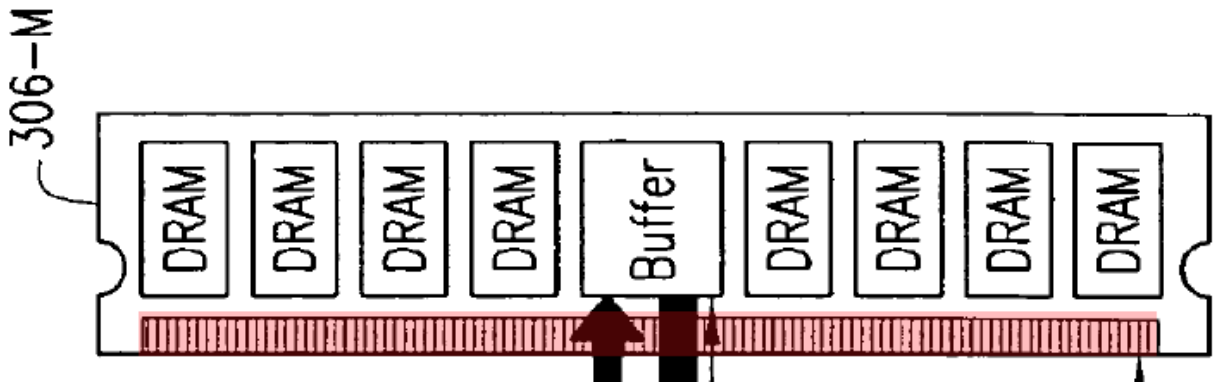
225. Harris teaches and discloses this limitation to a Skilled Artisan in each of Grounds 1 through 3. In addition, for Grounds 1, 2, and 3, Harris in view of the FBDIMM Standards teaches and discloses this limitation to a Skilled Artisan.

226. Harris discloses a printed circuit board (PCB), such as one for the fully buffered DIMM 100A. Ex. 1023 at Fig. 1A. In particular, Harris contemplates using "both sides of the printed circuit board" to implement a DIMM and using a

form factor including the printed circuit board that is compatible with the JEDEC standards. *Id.* at [0013] ("It is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the ***printed circuit board***, and at a component height compatible with applicable Joint Electron Device Engineering Council (JEDEC) standards.") (emphasis added); *see also id.* at [0003], [0009], [0016], [0017] (reciting "memory board"), 3-4 (claims 1-36) (same), Figs. 1B, 3. This disclosure in Harris is consistent with the understanding of a Skilled Artisan that a memory module in the form factor of a fully buffered DIMM is implemented on a printed circuit board. *See* Ex. 1028 at 10 ("The reference designs for the DIMM PCBs are called the "raw cards", abbreviated R/C."), 84 ("DIMM printed circuit board design uses six, eight or ten layers of glass epoxy material"); *see also* Ex. 1027 at 77 (discussing "simplifie[d] PCB routing"). Examples of PCB "raw cards" are also disclosed by the JEDEC standards. *See, e.g.*, Ex. 1028 at 38 (illustrating Raw Cards B and C); Ex. 1027 at 38-39 (addressing various Raw Cards). Thus, Harris alone, or in combination with the FBDIMM Standards (includes JESD82-20 and JESD205) satisfies a "*printed circuit board (PCB)*."

227. Harris also discloses that the PCB of its memory module has a DIMM connector with pins. Ex. 1023 at [0019] ("one or more of the following advantages

may be realized in an exemplary voltage distribution embodiment: . . . reduction in the pin count on DIMM connector to system board or memory riser card (whereby a smaller connector or wider pin spacing may be accommodated)"); *see also id.* at [0002] and [0012] (discussing specific pin counts for power). For example, Figure 3 of Harris is annotated in red below to show an edge connector of the DIMM with multiple connections.



Id. at Fig. 3 (reproduced in part and annotated).

228. A Skilled Artisan would have recognized that such a DIMM connector is part of an interface and is configured to fit into a corresponding slot connector of a host system according to relevant industry standards. *See, e.g.*, Ex. 1023 at [0002] and [0012] (discussing specific pin counts of the interface for power), [0013] ("By way of an additional variation in implementation, the form factor associated with the memory assembly module 100A may be suitably modified (e.g., removing the board's connector keyway) so as to ensure that a memory assembly module embodying the teachings of the present disclosure is not

interchangeable with the standard DIMM, thereby preventing any accidental damage."), Figs. 3, 4 (showing memory controller 302 or memory control 408 of host system); Ex. 1028 at 38 (illustrating raw cards B and C with a connector keyway). For example, JESD82-20 (part of the FBDIMM Standards) discloses that there could be large lane-to-lane skew at the DIMM "gold finger." Ex. 1027 at 43. As another example, JESD205 (part of the FBDIMM Standards) discloses that an FBD includes "PCB edge connector contacts [that] shall be gold-plated" (Ex. 1028 at 84), and that there is a voltage drop between the edge connector and the motherboard (*id.* at 100). Thus, Harris alone, or in combination with the FBDIMM Standards, satisfies the PCB "*having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections*."

229. Harris also discloses edge connections of the interface "*configured to couple power, data, address and control signals between the memory module and the host system*." As shown below in Figure 1A, Harris discloses that the memory module 100A is provided an input 104 from an external voltage source.

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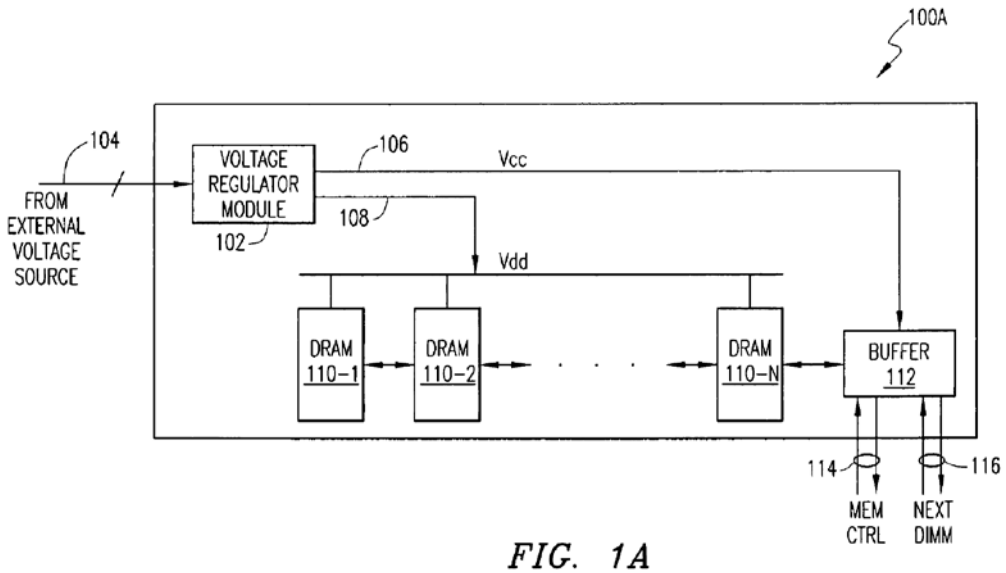


FIG. 1A

Ex. 1023 at Fig. 1A, [0010]. Harris also discloses that a standard FBD module has a connector with a specific number of pins to couple power between the module and host system. *See* Ex. 1023 at [0012] ("By way of example, a standard FBD module requires 28 Vdd pins (for DRAM devices) and 8 Vcc pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic."). Harris also provides examples of voltage-independent designs with differing number of pins for power. *See id.* (describing designs with six pins, 12 pins, and 24 pins); *see also id.* at [0019] ("reduction in the pin count on DIMM connector to system board").

230. Harris also discloses a connector with pins for data, address, and control signals between the memory module and host system. As shown below in

Figure 1A of Harris, the buffer 112 of memory module 100A is coupled to a bidirectional memory controller interface path 114 and a daisy-chain interface 116 to the next DIMM.

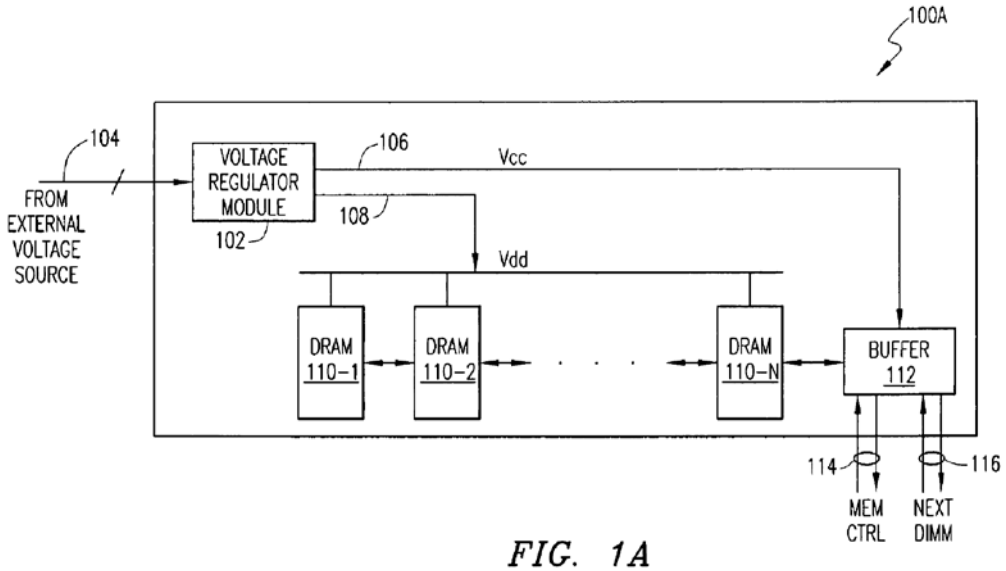
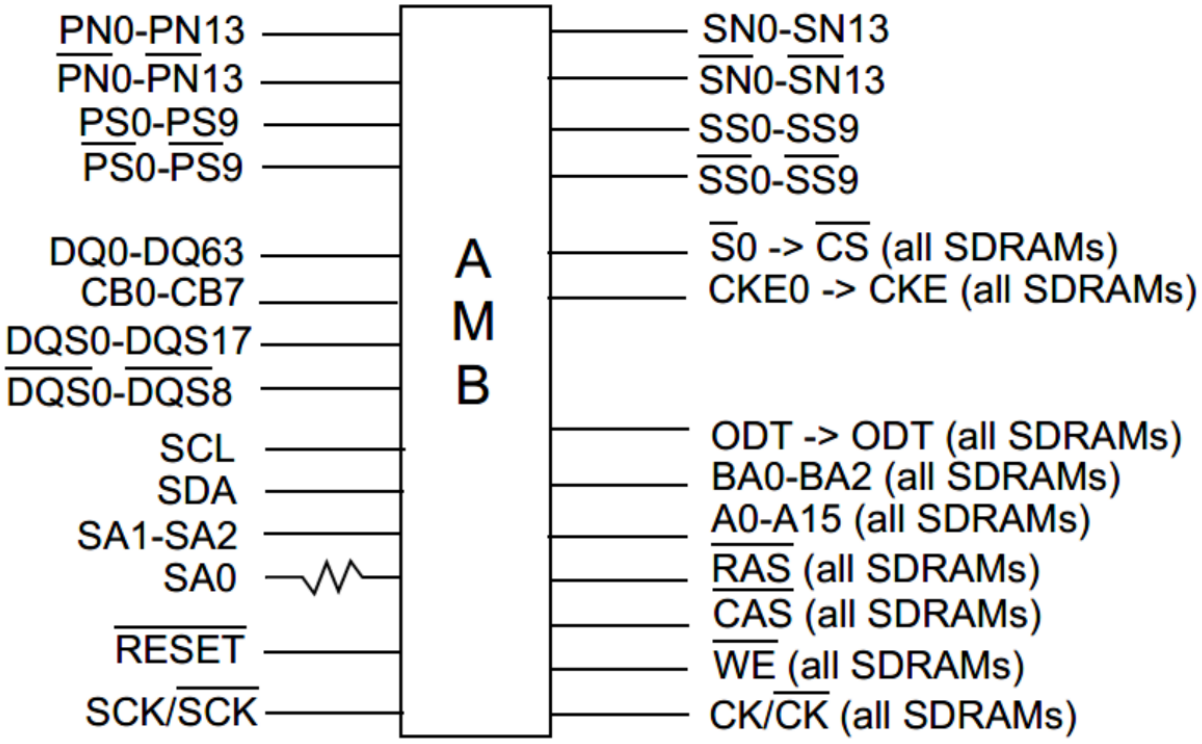


FIG. 1A

Id. at Fig. 1A; *see also id.* at Fig. 3 (buffer 314 and bidirectional memory link 304), [0017] (describing Fig. 3). A Skilled Artisan would have recognized that these connections couple data, address, and control signals. For example, Harris discloses that the buffer 112 is provided for "buffering ***command/address (C/A)*** space as well as ***data*** space at least for a portion of the memory devices 110-1 through 110-N." *Id.* at [0009] (emphasis added). In addition, Figure 1A of Harris (reproduced above) identifies the bidirectional memory controller path 114 as for "MEM CTRL" or memory control.

231. A Skilled Artisan would also have recognized that an FBDIMM connector, such as the one disclosed in Figures 1A and 3 of Harris, couples data, address, and control signals between the DIMM and host system. For example, below is an excerpt of a block diagram for Raw Card Version A from JESD205 (part of the FBDIMM Standards).



Ex. 1028 at 13 (excerpted); *see also id.* at 29 (AMB Pin Description). As shown, the AMB is coupled to multiple data signals (e.g., DQ0-DQ63), address signals (e.g., A0-A15), and control signals (e.g., RAS, CAS, WE, CS). *Id.*; *see also* Ex. 1026 (JESD79-2B) at 6, 46-47, 52. The AMB is also coupled to multiple signals for bi-directional communication, such as the Primary Northbound (e.g., PN0-PN13) and Primary Southbound (e.g., PS0-PS9) links. A Skilled Artisan would

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have recognized that the AMB buffer is responsible for buffering and converting the bi-directional communications with data, address, and control signal information into data, address, and control signals for the memory devices. For example, the block diagram for Raw Card Version A from JESD205 (part of the FBDIMM Standards) indicates that the data, address, and control signals are for "all SDRAMs." Ex. 1028 at 13. This indicates to a Skilled Artisan that the signals are provided for the memory devices on the DIMM. As another example, JESD82-20 (part of the FBDIMM Standards) discloses that each link to the AMB connects the AMB "to a host memory controller or an adjacent FBD." Ex. 1027 at 4. A block diagram of these connections is shown in Figure 1.2 below.

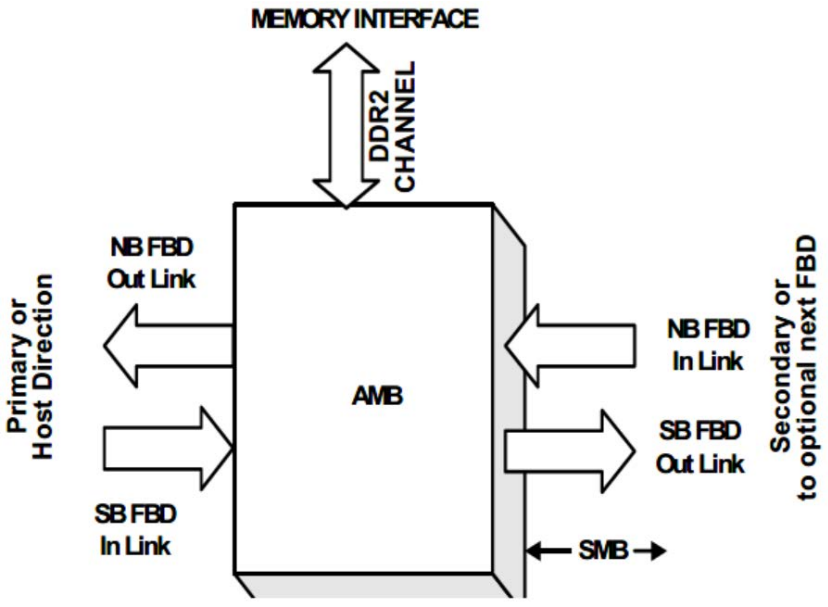
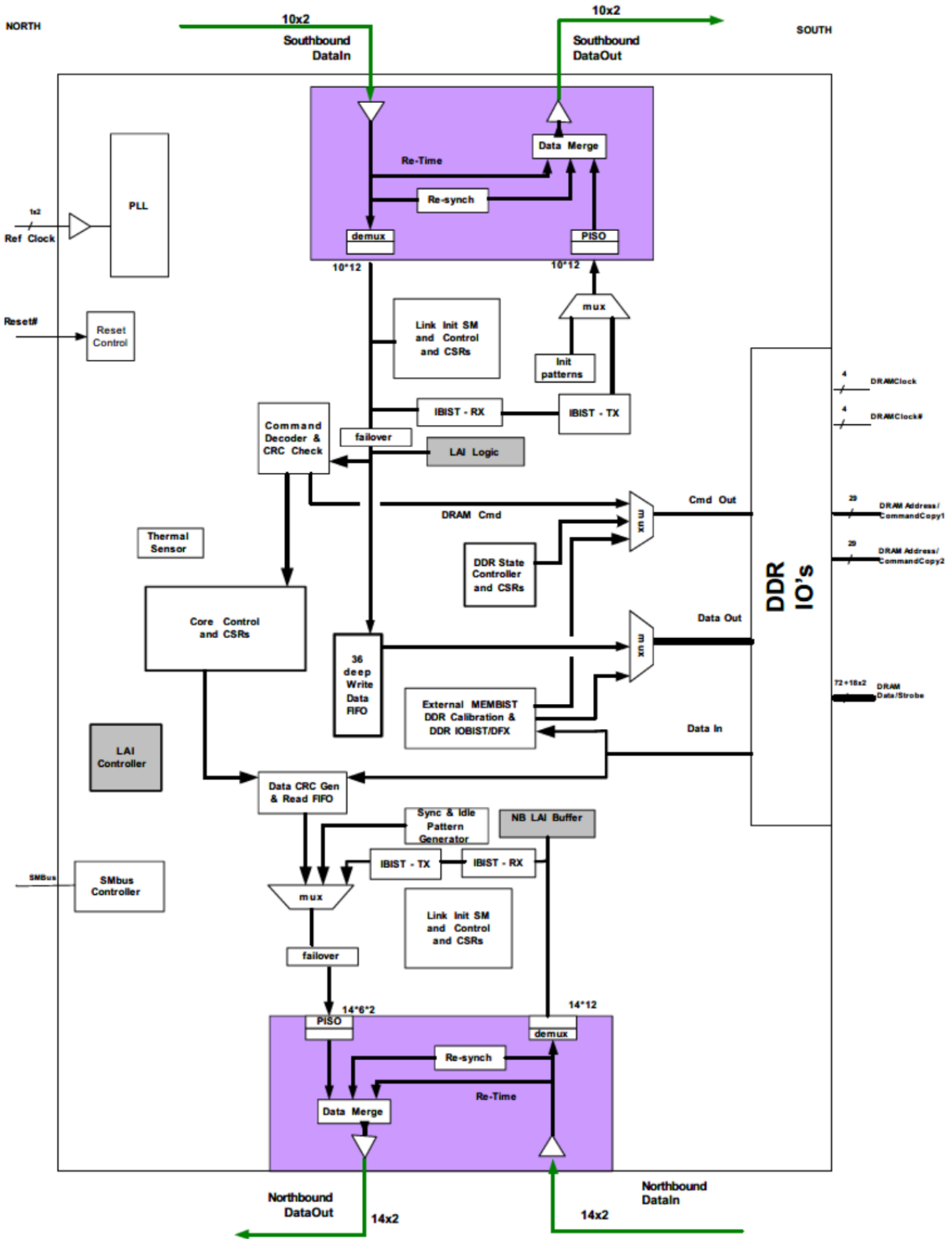


Figure 1.2 — Advanced Memory Buffer Interfaces

Id. JESD82-20 also discloses the following block diagram of the AMB.


NORTH
10x2
Southbound DataIn
10x2
Southbound DataOut
SOUTH
Re-Time
Data Merge
Re-synch
demux
PISO
10*12
10*12
PLL
1x2
Ref Clock
Reset#
Reset Control
Link Init SM and Control and CSRs
mux
Init patterns
IBIST - RX
IBIST - TX
Command Decoder & CRC Check
failover
LAI Logic
DRAM Cmd
Cmd Out
mux
Thermal Sensor
DDR State Controller and CSRs
Core Control and CSRs
36 deep Write Data FIFO
Data Out
mux
External MEMBIST DDR Calibration & DDR IOBIST/DFX
Data In
LAI Controller
Data CRC Gen & Read FIFO
Sync & Idle Pattern Generator
NB LAI Buffer
SMBus
SMbus Controller
IBIST - TX
IBIST - RX
mux
Link Init SM and Control and CSRs
failover
14*6*2
14*12
PISO
demux
Re-synch
Re-Time
Data Merge
Northbound DataOut
14x2
Northbound DataIn
14x2
DDR IO's
4
DRAMClock
4
DRAMClock#
29
DRAM Address/ CommandCopy1
29
DRAM Address/ CommandCopy2
72+18x2
DRAM Data/Strobe

See id. at 3 (Figure 1.1). As shown, the data flow of the AMB includes conversion of communications, such as those on the Northbound and Southbound links, into data, address, and control signals for the memory devices, such as the signals coupled to the "DDR IO's" block. Harris satisfies "*configured to couple power, data, address and control signals between the memory module and the host system*."

232. Accordingly, Harris alone, or in combination with part of the FBDIMM Standards, satisfies "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*"

c) [1.c] A Voltage Conversion Circuit

233. Claim 1 requires "*a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages.*"

234. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

235. As explained above, Harris alone, or in combination with the FBDIMM Standards, satisfies a memory module that includes "*a printed circuit*

board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system." *Supra* ¶¶224-232. In addition, Harris discloses a memory module with an on-board voltage regulator module (VRM) to convert an externally supplied voltage level to appropriate local voltage levels. Ex. 1023 at [0010] ("[A]t least one on-board voltage regulator module (VRM) is provided as part of the memory board assembly module 100A for converting an externally supplied voltage level available on external source path 104 into appropriate local voltage levels that power the first and second voltage paths, i.e., the Vdd and Vcc paths 108, 106, respectively."). Accordingly, a Skilled Artisan would have recognized that the "on-board" voltage regulator module, as Harris discloses, satisfies "*a voltage conversion circuit coupled to the PCB*" as required by the claim.

236. According to Harris, the on-board conversion for the voltage regulator module is preferably implemented using a high-frequency switching voltage converter. Ex. 1023 at [0010] ("Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels."). A Skilled Artisan would have recognized the "tightly-controlled voltage levels" generated by

the high-frequency switching voltage converter, as Harris discloses, are each "*regulated voltages"* as required by the claim.

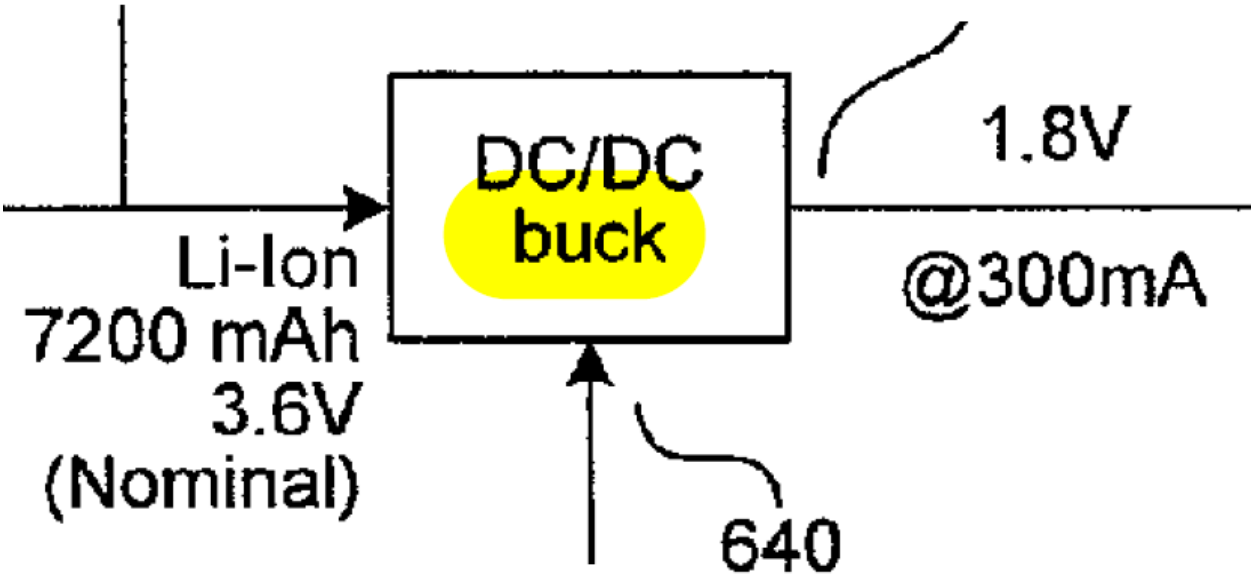
237. As explained below for each of the Grounds and voltage mappings, it would have been obvious to a Skilled Artisan for the "*voltage conversion circuit . . . to provide at least three regulated voltages*." *See infra* ¶¶242-260.

238. In addition, it would have been obvious that the voltage conversion circuit includes "*at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages*." Harris discloses examples of the externally supplied voltage level and appropriate local voltage levels. For example, the externally supplied voltage level is implemented as 12-volts with as few as six pins. *See* Ex. 1023 at [0012] ("A voltage-independent FBD design incorporating the embodiment of FIG. 1A is capable of replacing these power supply interface pins with ***as few as six +12V pins (from an external voltage source)***, with local conversion to Vdd (to DRAM) and Vcc (to buffer/logic) being added. Alternatively, using additional power supply pins would provide the capability to support even more devices. For instance, with 12 supply pins (at +12V), the embodiment of FIG. 1A can provide enough power to supply 4 ranks (i.e., 72 devices). Likewise, a memory assembly of 8 ranks (144 devices) may be powered with 24 pins at +12V.") (emphasis added). Also, the appropriate local voltage levels for the Vdd and Vcc supplies range from around 0.5 to 3.5

volts. *See id.* at [0009] ("a first voltage path 108, typically referred to as a Vdd path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices, e.g., ***from about 0.5V to 3.5V or more***" and "a second voltage path 106, typically referred to as a Vcc path, are provided with respect to the buffer component 112, wherein the Vcc path may be energized to appropriate voltage levels depending on the buffer and DIMM technology, e.g., ***from about 0.5V to 3.5V or more***") (emphasis added).

239. A Skilled Artisan would have understood, and it would have been obvious to her, to implement a high-frequency switching converter in Harris that steps down the input voltage (e.g., 12 volts) to each of the lower output voltages (e.g., less than 3.5 volts) as "*buck converters each of which is configured to produce a regulated voltage*" as required by the claim. As explained above, buck converters were well-known switching devices commonly used to step down the voltage between its input and output. *Supra* ¶¶147-150; *see also* Ex. 1058 at 3 (describing Fig. 1-3), 5 (Fig. 1-3, "1.3 Switching-Regulatory Theory," "The output voltage V_O is always equal to the input voltage V_{IN}, times the duty cycle D, or $V_O = DV_{IN}$."), 12-16 ("1.5.4. Buck or Step-Down"); Ex. 1032 at 161 (step-down or buck converter is a "basic converter topolog[y]."), 164 ("[a]s the name implies, a step-down converter produces a lower average output voltage than the dc input voltage V_d."); Ex. 1024 (Amidi) at Fig. 6 (showing a DC/DC buck converter 640 to

step down a higher voltage to a lower one, reproduced below in part, annotated); Ex. 1023 (Harris) at [0014] (disclosing a redundancy implementation with a "plurality of on-board VRMs"), Fig. 1B.



In fact, a buck converter was a conventional device that a Skilled Artisan would have used for implementing "a ***high-frequency switching voltage converter*** capable of generating tightly-controlled voltage levels," as disclosed by Harris (Ex. 1023, at [0012, 0010]), because a "***voltage-reducing switching converter***" was commonly referred to as a "***buck converter***." Ex. 1030 (Boldo), 2:41-43, *See also id.* at 2:32-40, 5:34-44.

240. In addition, a Skilled Artisan would have understood, and been motivated by, the fact that a buck converter efficiently steps down the voltage without generating excess heat or requiring excessively large cooling devices. For

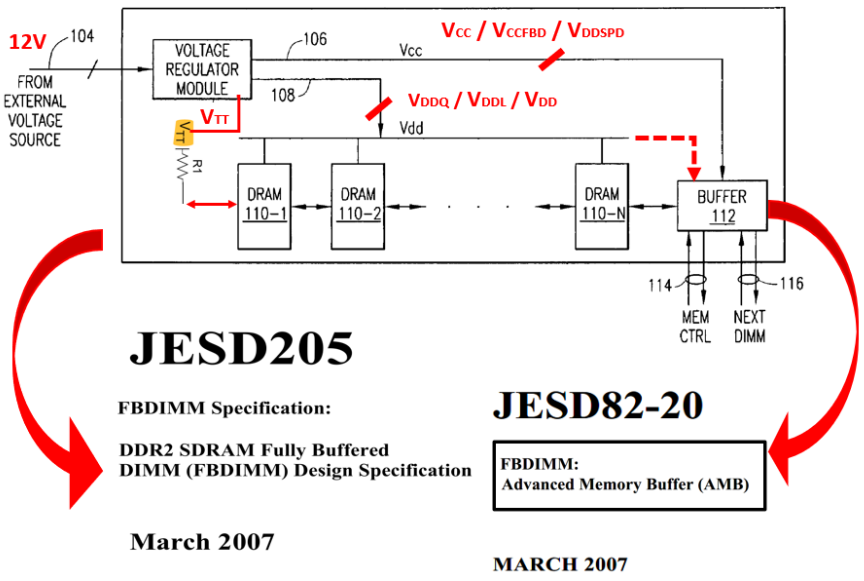
example, U.S. Patent No. 7,061,214 to Mayega *et al.* states that "[s]witch mode buck converters have become popular due to two attractive features: first, they are more efficient than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, ***they can provide relatively high currents with lower power dissipation on chip than an LDO can***." Ex. 1059 at 5:23-30 (emphasis added); *see also* Ex. 1034 at 1:58-2:1 (describing charge pump circuits as "generally inefficient and consume large amounts of current"); Ex. 1040 (Texas Instruments TPS51020) at 1 (describing "high efficiency applications" across loads), Figs. 22-25 (showing efficiency versus output current); Ex. 1041 (FAN5026 Dual DDR/Dual-Output PWM Controller) at 1, 13 (describing high efficiency operation "over a wide range of loads"); Ex. 1048 at 3 (specifying an efficiency of 75%); Ex. 1058 at 5 ("1.3 Switching-Regulator Theory") ("The high efficiency of switching regulators is the result of operating the series transistor in a switching mode."); Ex. 1062 at 11 (explaining that "lower dissipation" of electronic devices, such as a Class D amplifier, "saves the cost (and space) of cooling apparatus like heat sinks or fans"); Ex. 1064 at [0101] (discussing "Power loss algo[r]ithm" to flash DRAM to FLASH during a "power los event" in which the "VR Efficiency" is 85%).

241. In the grounds and voltage mappings described below, a Skilled Artisan would have understood that each of VDD, VDDQ, VDDL, VCC, VCCFBD, and VTT have a voltage amplitude (e.g., between 0.9 and 3.3 volts) that

is less than the voltage amplitude of the external voltage source (e.g., 12 volts). Thus, the prior art in each of Grounds 1 through 3 satisfies a voltage conversion circuit that includes "*at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages*."

242. For Ground 1 (Harris in view of the FBDIMM Standards), Ground 2 (Ground 1 further view of Amidi), and Ground 3 (Ground 2 further view of Hajeck), the prior art references in each of the grounds renders obvious the claimed "*at least three regulated voltages*" including the following three voltage mappings shown in the figure below. The voltage mappings for Ground 3 are the same as Ground 2.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{DDL} = 1.8V

Voltage Mapping (B)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} = 1.5V
3rd : V_{CCFBD} = 1.5V

Voltage Mapping (C)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{TT} = 0.9V

Ground 2: Ground 1 and Battery Backup of Amidi

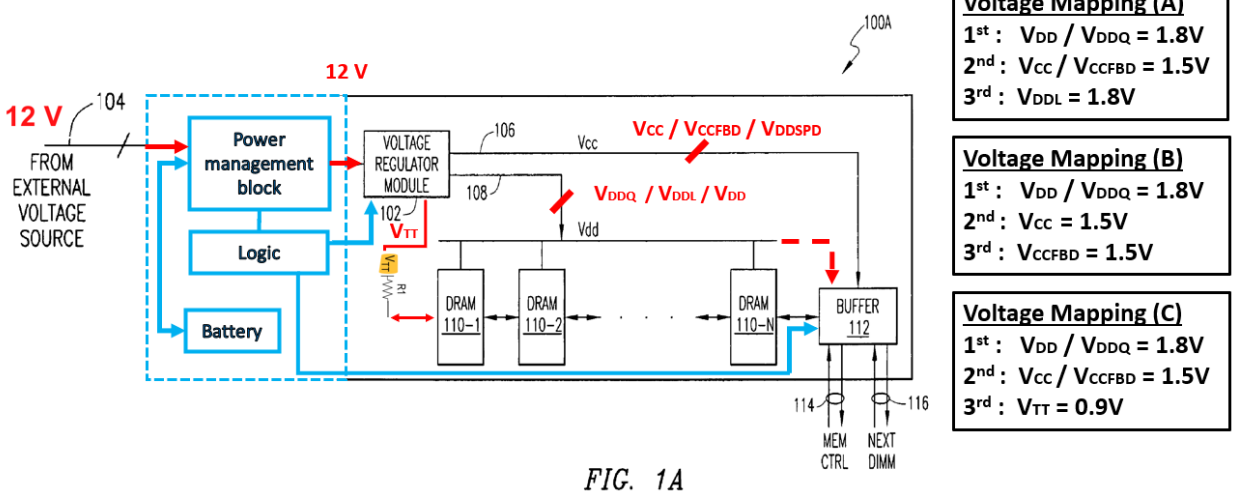


FIG. 1A

Ex. 1023 at Fig. 1A (annotated); *see also supra* ¶¶158-170 (reasons to combine for Ground 1), ¶¶171-180 (reasons to combine for Ground 2), ¶¶181-188 (reasons to combine for Ground 3).

243. In "Voltage Mapping (A)" of Grounds 1, 2, and 3, the VDD or VDDQ voltage supply (e.g., at 1.8 volts) is the first regulated voltage, the VCC or VCCFBD voltage supply (e.g., at 1.5 volts) is the second regulated voltage, and the VDDL voltage supply (e.g., at 1.8 volts) is the third regulated voltage.

244. In "Voltage Mapping (B)" of Grounds 1, 2, and 3, the VDD or VDDQ voltage supply (e.g., at 1.8 volts) is the first regulated voltage, the VCC voltage supply (e.g., at 1.5 volts) is the second regulated voltage, and the VCCFBD voltage supply (e.g., at 1.5 volts) is the third regulated voltage.

245. In "Voltage Mapping (C)" of Grounds 1, 2, and 3, the VDD or VDDQ voltage supply (e.g., at 1.8 volts) is the first regulated voltage, the VCC or

VCCFBD voltage supply (e.g., at 1.5 volts) is the second regulated voltage, and the VTT voltage supply (e.g., at 0.9 volts) is the third regulated voltage.

(1) VDD, VDDQ, and/or VDDL

246. With regards to VDD and/or VDDQ (first regulated voltage) and VDDL (example of third regulated voltage), Harris discloses, for example, that the VDD supply is 1.8 volts for DDR2 memory devices. Ex. 1023 at Fig. 1A, [0009]. In particular, Harris explains that the memory devices on the memory module "can be of any known or heretofore unknown DDR type, e.g., DDR2 (operable with 1.8 V)." *Id.* at [0009]. A Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with DDR2 memory devices couples those devices to multiple, separate voltage sources, called VDD, VDDQ, and VDDL, which each provides a 1.8-volt supply.

247. For example, JESD205 (part of the FBDIMM Standards) discloses that the memory devices (DRAM) and the buffer (AMB) are provided several supply voltages, as shown in the table below.

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply

Ex. 1028 at 9 (excerpted). As shown, the DRAM is provided VDD and VDDQ, each typically at 1.8 volts, and VTT typically at 0.9 volts. *Id.* In addition, the AMB

is provided VDD/VDDQ (typically 1.8 volts), as well as VCC and VCCFBD, each typically at 1.5 volts. *Id.*; *see also* Ex. 1027 (JESD82-20) at 31-32 (AMB receiving "V_{DD} Supply voltage DRAM interface"), 44 (describing DRAM interface on AMB receiving V_{DD}), p.83 (listing VCC, VCCFBD, and VDD power supplies provided to AMB); *see also* Ex. 1028 (JESD205) at 9 (V_{DD}/V_{DDQ} for DRAM and AMB), 11, 13-16, 30, 33 (same). JESD205 (part of the FBDIMM Standards) also discloses the pin assignments of DDR2 SDRAM memory, which include a VDDL supply voltage. *See* Ex. 1028 at 17-20.

248. A Skilled Artisan would also have recognized that the VDDL voltage supply is provided to DDR2 SDRAM memory at a voltage amplitude of 1.8 volts. For example, JESD79-2B discloses that VDDL, similar to VDD and VDDQ, has a voltage amplitude of 1.8 volts. Ex. 1026 at pp.6-7 (excerpted and reproduced below with annotations).

NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**

Symbol	Type	Function
V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

249. JESD79-2B also discloses that, in one implementation, the three voltage supplies—VDD, VDDQ, and VDDL—can be turned on and off separately, thus suggesting to a Skilled Artisan that these voltages are provided by separate converters. *See* Ex. 1026 at 9. As shown below, in one implementation, VDD is applied before or at the same time as VDDL, VDDL is applied before or at the same time as VDDQ, and VDDQ is applied before or at the same time as VTT and Vref.

1. Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT*1 at a low state (all other inputs may be undefined.)

   - VDD, VDDL and VDDQ are driven from a single power converter output, AND
   - VTT is limited to 0.95 V max, AND
   - Vref tracks VDDQ/2.

   or

   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.

   at least one of these two sets of conditions must be met.

Id. at 9. Furthermore, JESD79-2B expressly recommends an isolated voltage source for VDDL. *Id.* at 2-3 ("VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ."). Thus, a Skilled Artisan would have understood that separate voltage converters would enable the power up and initialization sequence in which VDD is applied before VDDL, VDDL before VDDQ, and VDDQ before VTT and Vref and isolated voltage source for VDDL.

250. Further, a Skilled Artisan would have recognized that any of the converters generating VDD, VDDQ, or VDDL satisfies a buck converter for the first and/or third of the "*at least three regulated voltages*" as each converts a higher voltage (e.g., 12 volts) to a lower one at, for example, 1.8 volts. *See supra* ¶¶238-239, 147-150; *see also* Ex. 1058 (Lenk) at 3, 5, 12-16, Fig. 1-3; Ex. 1032 (Mohan) at 161, 164; Ex. 1024 (Amidi) at Fig. 6.

(2) VCC or VCCFBD

251. With regards to VCC or VCCFBD (the second and/or third regulated voltages), Harris discloses that a VCC supply is provided to the buffer. For example, Figure 1A of Harris shows that VCC is generated by the voltage regulator module 102 and provided to the buffer 112.

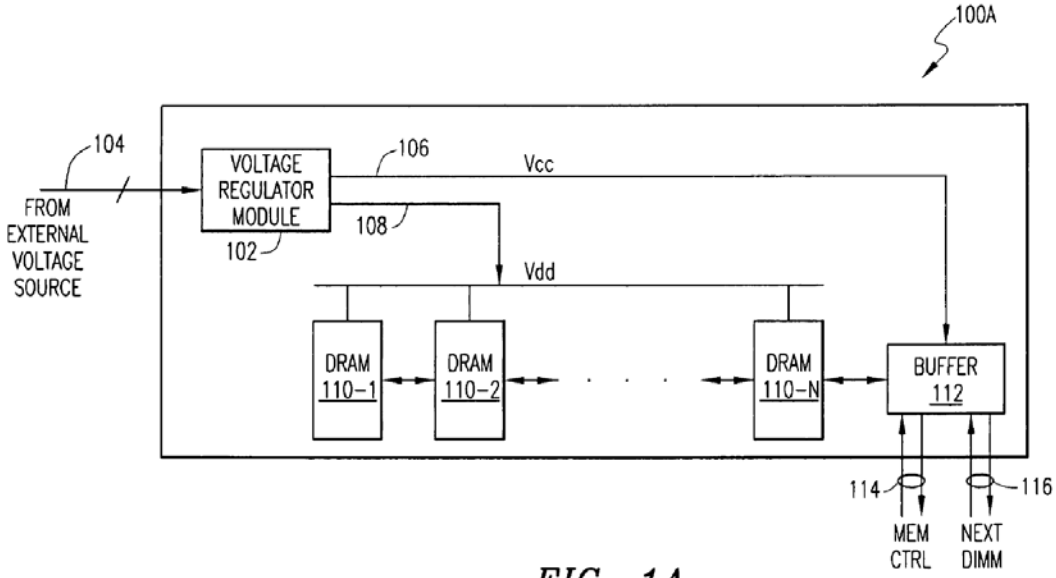


FIG. 1A

Ex. 1023 at Fig. 1A.

252. Harris explains that the appropriate voltage levels for the VCC path depend on the buffer and DIMM technology, such as from 0.5 volts to 3.5 volts. Ex. 1023 at [0009] ("In the illustrated embodiment of FIG. 1A, for instance, the DIMM configuration of the memory module 100A is exemplified as a fully buffered DIMM wherein a buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices 110-1 through 110-N. A bidirectional memory controller interface path 114 as well as a second voltage path 106, typically referred to as a Vcc path, are provided with respect to the buffer component 112, wherein the Vcc path may be energized to appropriate voltage levels depending on the buffer and DIMM technology, e.g., from about 0.5V to 3.5V or more.").

253. A Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with buffer/logic component 112 for buffering command, address, and data signals requires multiple separate voltage sources in accordance with the relevant JEDEC standards. Ex. 1023 at [0009], Fig. 1A; Ex. 1027 (JESD82-20, part of FBDIMM Standards) at 83 (listing VCC, VCCFBD, and VDD power supplies provided to AMB; excerpted and reproduced below with annotations); Ex. 1028 (JESD205, part of FBDIMM Standards) at 9 (listing VDDQ, VCC, and VCCFBD power supplied provided to AMB).

Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

254. In particular, a Skilled Artisan would have recognized that an Advanced Memory Buffer (AMB) for a Fully Buffered DIMM (FB-DIMM) performed the functions Harris describes for buffer/logic component 112. Harris describes memory module 100A in Figure 1A as a "fully buffered DIMM" and explains that buffer/logic component 112 on memory module 100A buffers command, address, and data signals. *See* Ex. 1023 at [0009]. The multiple power supplies for the AMB buffer include VCC and VCCFBD, which are each 1.5 volts. Ex. 1023 at Fig. 1A; Ex. 1027 at 83; Ex. 1028 at 9. Thus, a Skilled Artisan would have recognized that, in Harris's FB-DIMM implementation with the buffer/logic 112 (AMB), the voltage regulator module 102 converts the input supply voltage (e.g., 12 volts) down to VCC and VCCFBD supply voltage at 1.5 volts.

255. Similar to the multiple voltage sources for the memory devices (DRAMs) in Harris (e.g., 1.8 volts for DDR2 SDRAMs), a Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an FBDIMM implementation of Harris couples the AMBs to multiple, separate voltage sources called VCC and VCCFBD. *Supra* ¶¶239, 250, 147-150; *see also* Ex. 1058 at 3, 5,

12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6; Ex. 1023 at Fig. 1A, [0010], [0012]. In particular, the AMB specification, JESD82-20 (part of the FBDIMM Standards), specifies that VCC for the core of the AMB and VCCFBD for the fully buffered DIMM (FBD) high speed input/output functionality each has a voltage level of 1.5 volts. Ex. 1023 at Fig. 1A (annotated above); Ex. 1027 at 78, 82; Ex. 1028 at 9. A Skilled Artisan would have understood that having separate power converters for VCC and VCCFBD, as suggested by the FBDIMM Standards by specifying separate power supplies, provides independence of these power supplies to allow improved stability for each supply and flexibility for power management. *See id.*; *supra* ¶249 (citing Ex. 1026 at 2, 3, 9 (explaining that voltage supplies can be turned on and off separately and a voltage can be "isolated"); *see, e.g.*, Ex. 1033 (U.S. Patent No. 7,721,130 to Prete) at 12:50-58 (disclosing selectively turning off power to different interfaces of an AMB).

256. Further, a Skilled Artisan would have recognized that any of the converters generating VCC or VCCFBD satisfies a buck converter for the second and/or third ones of the "*at least three regulated voltages*" as each converts a higher voltage (e.g., 12 volts) to a lower one at, for example, 1.5 volts. *See supra* ¶¶238-239, 147-150; *see also* Ex. 1058 (Lenk) at 3, 5, 12-16, Fig. 1-3; Ex. 1032 (Mohan) at 161, 164; Ex. 1024 (Amidi) at Fig. 6.

(3) VTT

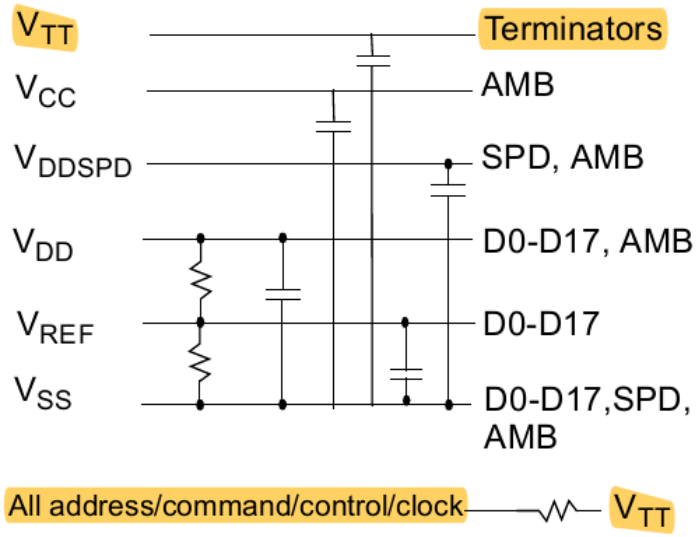
257. With regards to VTT (the third regulated voltage in "Voltage Mapping (C)"), as discussed above with reference to an FBDIMM with DDR2 SDRAM, a Skilled Artisan would have understood that an FBDIMM, like that disclosed in Harris, requires a supply voltage called VTT for proper operation of the DDR2 memory device interfaces. *Supra* ¶¶141, 137, 140, 141, 155, 167, 170. For example, JESD205 (part of the FBDIMM Standards) discloses that the FBDIMM receives a memory devices (DRAM) interface supply voltage VTT (which tracks the V_{DD}/V_{DDQ} supply voltage).

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply

Ex. 1028 at 9 (excerpted). As shown, VTT is typically one-half the voltage of V_{DD}/V_{DDQ}, or in the case of DDR2 SDRAM, 0.9 volts. *Id.* A Skilled Artisan would have recognized that the JEDEC standard requires VTT as a termination voltage whose amplitude is half of VDD, and the same as a reference voltage, VREF. *Id.* at 43 ("VREF [] tracks VDD/2").

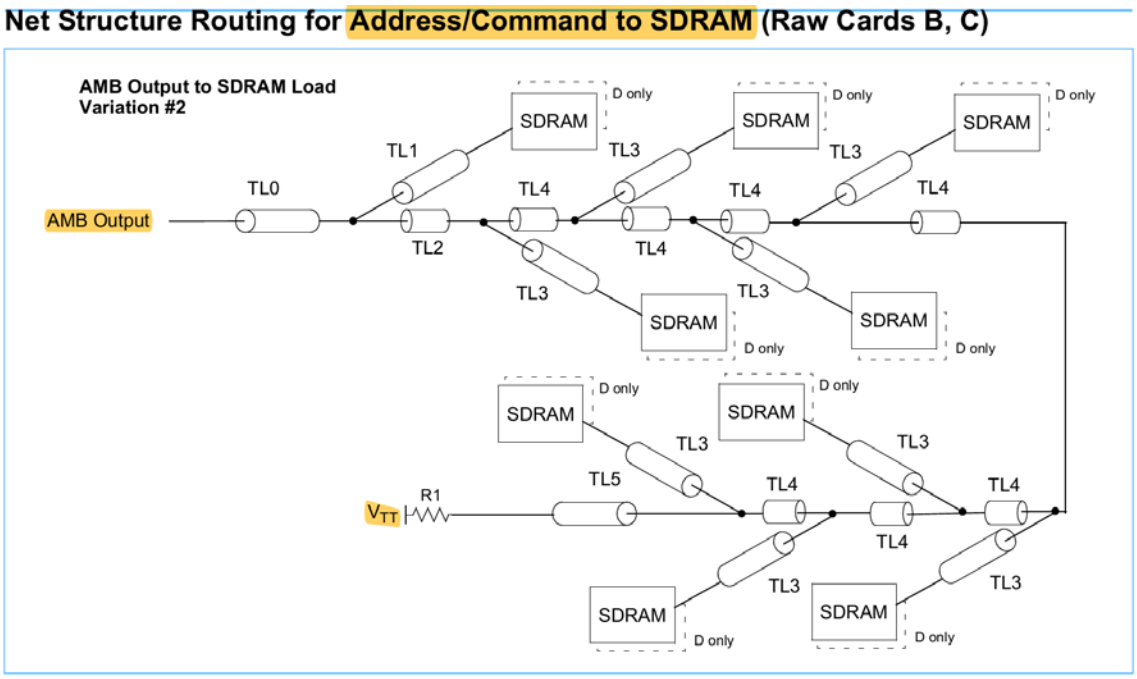
258. A Skilled Artisan would have also recognized that an FBDIMM with DDR2 SDRAM devices, like an embodiment disclosed in Harris, requires a VTT voltage supply to properly terminate the signals on the clock, address, command,

and/or control lines between the buffer/logic component 112 and the DRAM memory devices 110. *See, e.g.*, Ex. 1028 at 15 (excerpted and reproduced below, and annotated); Ex. 1023 at Fig. 1A.



As shown, the VTT voltage supply is provided to termination resistors for all address, command, control, and clock signals. *See id.*; *see also* Ex. 1026 at pp. 6-7, p. 9 (describing power-up sequence for VDD, VDDQ, VDDL, and VTT), 49 (recommended range for VDD, VDDQ, VDDL and VTT), 55 and 71 (showing VTT coupled through termination resistor, and defining VTT as half of VDDQ).

259. As another example, JESD205 (part of the FBDIMM Standards) explains in detail how to apply the VTT termination voltage for the address and command signal lines to the DDR2 SDRAM. *See, e.g.*, Ex. 1028 at 68 (excerpted and reproduced below).



Therefore, a Skilled Artisan would have recognized that, to properly terminate the clock, address, command, and/or control signals, an FBDIMM implementation of Harris includes a converter generating the VTT voltage supply that satisfies a buck converter for the third one of the "*at least three regulated voltages*" as it converts a higher voltage (e.g., 12 volts) to a lower one at, for example, 0.9 volts for DDR2 SDRAM memory devices. *See supra* ¶¶238-239, 147-150; *see also* Ex. 1058 (Lenk) at 3, 5, 12-16, Fig. 1-3; Ex. 1032 (Mohan) at 161, 164; Ex. 1024 (Amidi) at Fig. 6.

260. Accordingly, Harris alone or in view of the FBDIMM Standards (Ground 1), further in view of Amidi (Ground 2), and further in view of Amidi and Hajeck (Ground 3) each satisfies "*a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage*

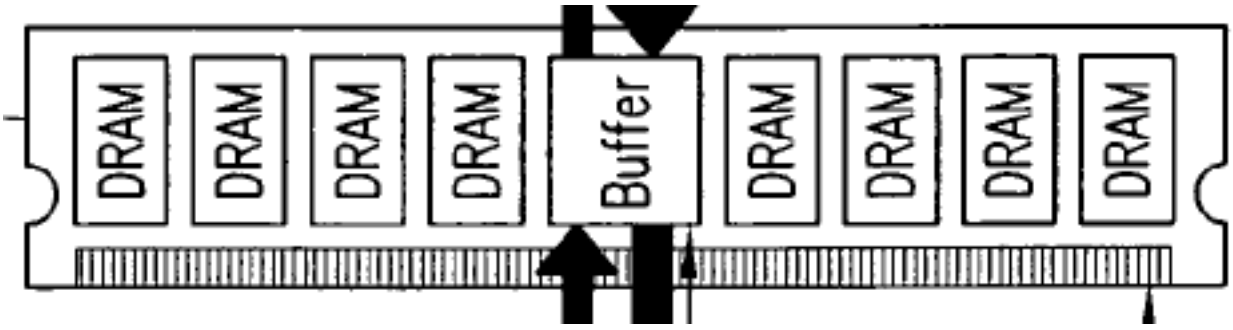
conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages."

d) [1.d] A Plurality of Components Coupled to the PCB

(1) [1.d.1] Plurality of components each coupled to at least one regulated voltage

261. Claim 1 requires "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages.*"

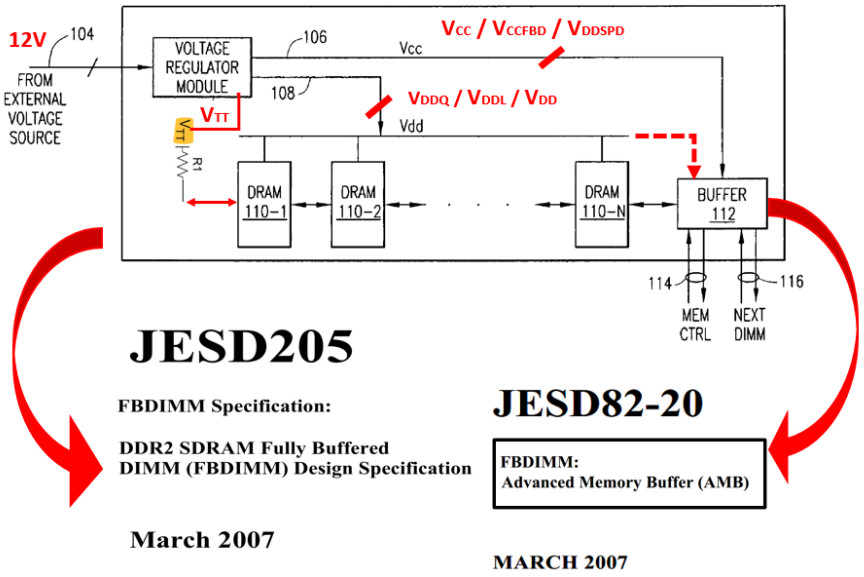
262. As explained above for claim limitation [1.b], Harris discloses using both sides of "*a printed circuit board (PCB)*" to implement a memory module. *Supra* ¶226; Ex. 1023 at [0013]. For example, Harris discloses that a buffer and DRAMs are "*components coupled to the PCB.*" Ex. 1023 at Fig. 3 (reproduced below in part).



263. As explained above for claim limitation [1.c], the prior art references in each of Grounds 1-3 satisfies "*a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is*

configured to produce a regulated voltage of the at least three regulated voltages." *Supra* ¶¶233-260. For example, in Grounds 1 and 2, DRAMs 110 are coupled to regulated voltages VDD, VDDQ, and VDDL, and Buffer 112 is coupled to VCC, VCCFBD, and VDDSPD. In Ground 3, the same components are coupled to the same regulated voltages as in Ground 2.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V

Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V

Ground 2: Ground 1 and Battery Backup of Amidi

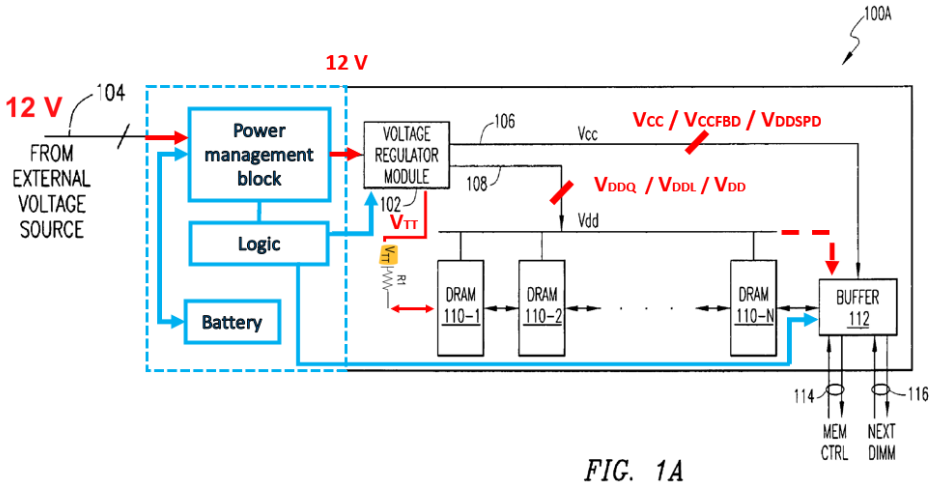


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V

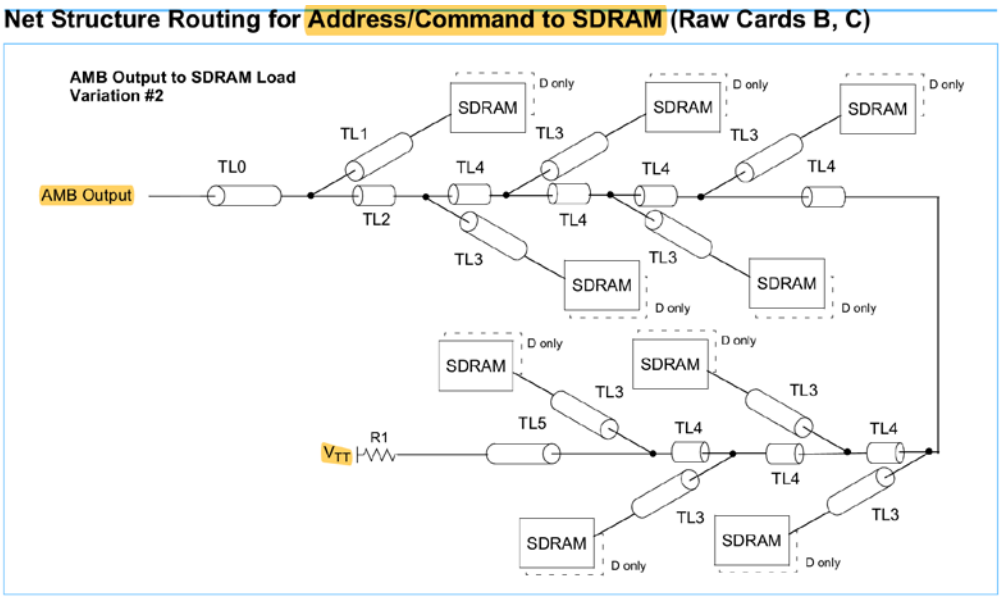
Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V

Further, as described by JESD205 (part of the FBDIMM Standards), the regulated voltage VDD/VDDQ is also coupled to the Buffer (AMB). Ex. 1028 at 9 (disclosing V_{DD} and V_{DDQ} supply for DRAM and AMB).

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply

See also Ex. 1028 at 11 (describing VDD as "DRAM Power and AMB DRAM I/O Power"), 30 (same), 33 (describing VDDQ as a critical specification of the AMB's SDRAM interface), 13-16 (showing VDD coupled to memory chips and AMB); Ex. 1027 (JESD82-20) at 31-32 (describing AMB receiving "V_{DD} Supply voltage DRAM Interface"), 44 (describing DRAM interface on AMB receiving V_{DD}), 83 (same). A Skilled Artisan would have understood from this disclosure that the AMB receives the VDD/VDDQ voltage in order to interface with DRAM devices. The JESD205 FBDIMM standard further discloses that the regulated voltage VTT is coupled to termination resistors (R1 below) and, through those resistors, to the SDRAMs and the Buffer (AMB). Ex. 1028 at 68 (reproduced below in part, annotated).



264. As explained for Grounds 1-3 for claim limitation [1.c], the "three regulated voltages" across the grounds and voltage mappings include the VDD, VDDQ, VDDL, VCC, VCCFBD, and VTT regulated voltages. *Supra* ¶¶233-260. As explained for Grounds 1A, 2A, and 3A, VDD or VDDQ is the first regulated voltage, VCC or VCCFBD is the second regulated voltage, and VDDL is the third regulated voltage. As explained for Grounds 1B, 2B, and 3B, VDD or VDDQ is the first regulated voltage, VCC is the second regulated voltage, and VCCFBD is the third regulated voltage. As explained for Grounds 1C, 2C, and 3C, VDD or VDDQ is the first regulated voltage, VCC or VCCFBD is the second regulated voltage, and VTT is the third regulated voltage.

265. Further, as explained, VDD, VDDQ, VDDL, and VTT are provided to the memory devices, such as DDR2 SDRAM. *See supra* ¶¶246-250 (VDD, VDDQ, and/or VDDL), ¶¶257-260 (VTT); *see e.g.*, Ex. 1023 at Fig. 1A; Ex. 1027

at p.83; Ex. 1028 at 9, 17-20. In addition, as explained, VDD, VDDQ, VCC, and VCCFBD are provided to the buffer, such as an AMB buffer for FBDIMMs. *Supra* ¶¶246-250 (VDD, VDDQ), ¶¶251-255 (VCC, VCCFBD); *see e.g.*, Ex. 1023 at Fig. 1A; Ex. 1027 at p.83; Ex. 1028 at 9, 17-20.

266. Accordingly, the prior art references in each of Grounds 1-3 satisfies "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages*."

(2) [1.d.2] Plurality of components including SDRAM devices

267. Claim 1 requires "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices*."

268. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

269. Harris teaches and discloses "*a plurality of synchronous dynamic random access memory (SDRAM) devices*" included as components on the memory module to a Skilled Artisan. In an embodiment, Harris discloses that the memory devices are standard dynamic random access memory (DRAM) devices, such as DDR2, which a Skilled Artisan would have understood are synchronous DRAM devices. *See* Ex. 1023 at Fig. 1A, [0009] ("In one configuration, the memory module 100A may be implemented as a Dual In-line Memory Module

(DIMM) wherein each of the memory devices 110-1 through 110-N comprises a Double Data Rate (DDR) dynamic random access memory (DRAM) device ... Also, the memory devices can be of any known or heretofore unknown DDR type, e.g., DDR2 (operable with 1.8 V), DDR3 (operable with 1.35V to 1.5V), and the like."); *see also* Ex. 1023 at [0011] ("Since the V_{dd} and V_{cc} power supply rails are rendered independent from external voltage sources, the overall power supply interface to the memory module 100A is improved to better support . . . DRAM technology independence (e.g., DDR2, DDR3, DDR4, and other DRAM types) . . ."); Ex. 1045 at 1 (Double Data Rate (DDR) SDRAM Specification, JESD79, a JEDEC standard), Ex. 1026 (DDR2 SDRAM Specification, JESD79-2B, a JEDEC standard), Ex. 1046 (DDR3 SDRAM, JESD79-3A, a JEDEC standard), Ex. 1028 (DDR2 SDRAM FBDIMM Design Specification, JESD205, a JEDEC standard).

270. Further, as explained above for claim limitation [1.d.1], the corresponding voltages, such as VDD, VDDQ, VDDL, and VTT regulated voltages, are provided to the memory devices, such as DDR2 (VDD, VDDQ, VDDL, VTT). *Supra* ¶¶246-250 (VDD, VDDQ, and/or VDDL), ¶¶257-260 (VTT); *see e.g.*, Ex. 1023 at Fig. 1A; Ex. 1027 at p.83; Ex. 1028 at 9, 17-20.

271. Accordingly, the prior art references in each of Grounds 1-3 satisfies "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices*."

(3) [1.d.3] A first circuit coupled to the SDRAM devices and first set of edge connections

272. Claim 1 requires "*a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections*."

273. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

274. As discussed for claim limitation [1.b], Harris alone, or in combination with FBDIMM Standards, satisfies "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*" *See supra* ¶¶224-232. In addition, Harris discloses that the buffer includes "*a first circuit*" that is coupled to the memory devices ("*the plurality of SDRAM devices*") and bidirectional memory interface paths ("*a first set of edge connections of the plurality of edge connections*") in order to buffer command, address, and data space. As shown in Figure 1A of Harris below, buffer 112 is coupled between DRAM 110-1 through 110-N, on one hand, and paths 114 and 116, on the other.

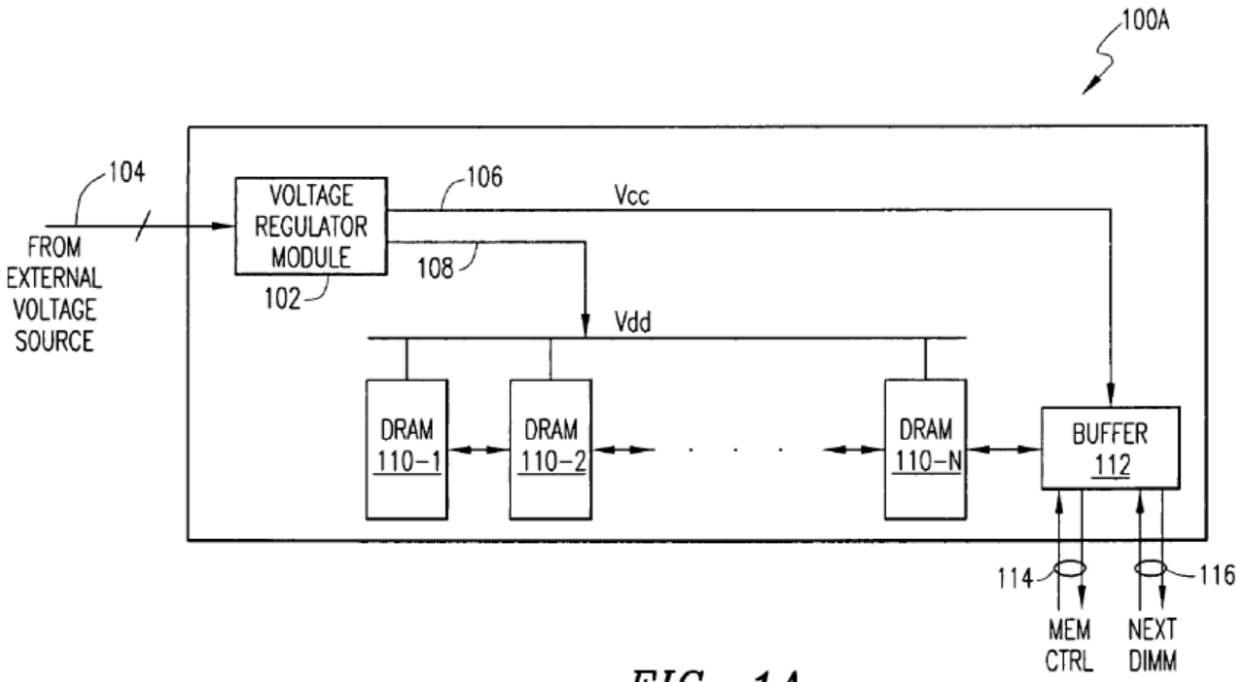


FIG. 1A

Ex. 1023 at Fig. 1A; *see also id.* at [0009] ("In the illustrated embodiment of FIG. 1A, for instance, the DIMM configuration of the memory module 100A is exemplified as a fully buffered DIMM wherein a buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices 110-1 through 110-N. A bidirectional memory controller interface path 114 as well as a second voltage path 106, typically referred to as a Vcc path, are provided with respect to the buffer component 112, wherein the Vcc path may be energized to appropriate voltage levels depending on the buffer and DIMM technology, e.g., from about 0.5V to 3.5V or more. In addition, where multiple memory assemblies are daisy-chained on a single memory

controller channel, a suitable daisy-chain interface 116 is provided for coupling the buffer component 112 to a next memory module.").

275. In addition, as shown in Figure 3 of Harris, the bidirectional interface paths 304 are coupled through a set of connections on the edge connector(s) of the memory module(s) 306-1 through 306-M.

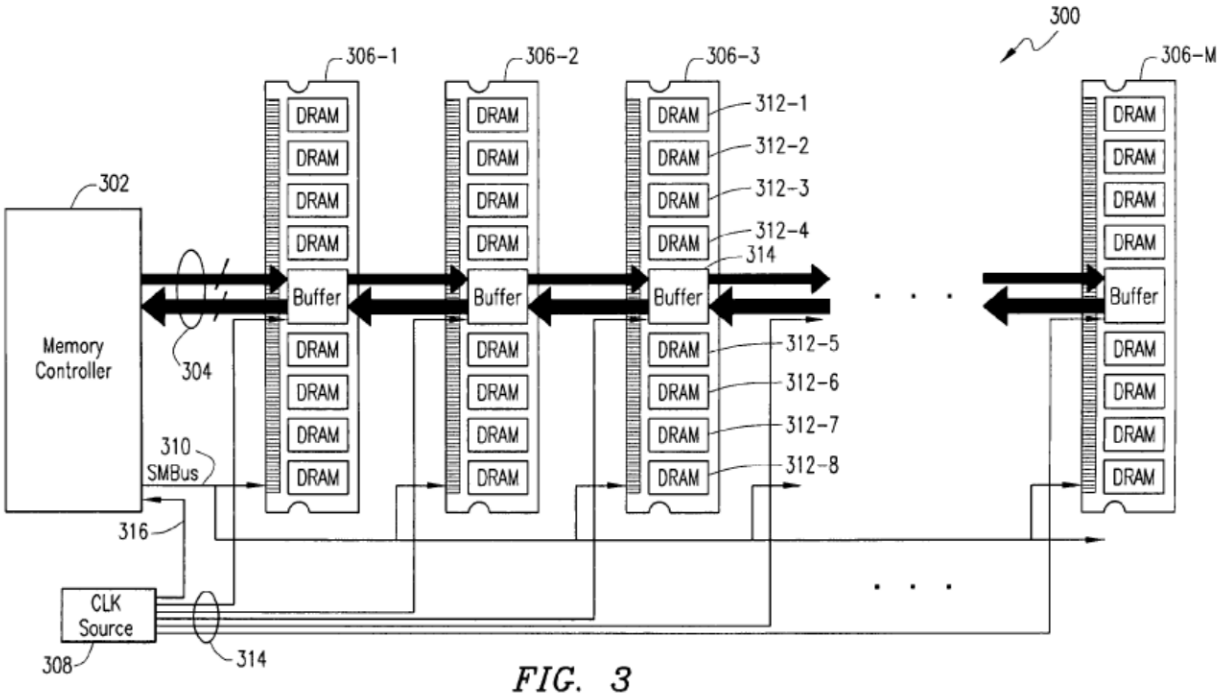


FIG. 3

Ex. 1023 at Fig. 3; *see also id.* at [0019] ("one or more of the following advantages may be realized in an exemplary voltage distribution embodiment: . . . reduction in the pin count on DIMM connector to system board or memory riser card (whereby a smaller connector or wider pin spacing may be accommodated)"); *see also id.* at [0002] and [0012] (discussing specific pin counts for power).

276. In addition, a Skilled Artisan would have recognized that the buffer in Harris is coupled between the plurality of SDRAM devices and a first set of edge connections of the plurality of edge connections the SDRAM devices. For example, JESD205 (part of the FBDIMM Standards) discloses that an FBDIMM includes a "PCB edge connector contacts [that] shall be gold-plated" (Ex. 1028 at 84), and that there is a voltage drop between the edge connector and the motherboard (*id.* at 100). Additionally, JESD205 discloses that standard FBDIMM connector pins include northbound and southbound data (*id.* at 11 (listing PN, PS, SN, and SS pins)) that are coupled to the Advanced Memory Buffer (AMB) (*id.* at 13 (showing AMB connected to PN, PS, SN, and SS signals)). Similarly, JESD82-20 (part of the FBDIMM Standards) discloses a DIMM "gold finger[s]" (Ex. 1027 at 43) that include PN, PS, SN, and SS pins (*id.* at 81), which are represent read and write data paths between the AMB and either a host or the next AMB in a daisy-chained configuration (*id.* at 81). *See also* Ex. 1027 at 3 (Figure 1.1) (showing data flow for the AMB buffer including conversion of communications, such as those on the Northbound and Southbound links, into data, address, and control signals for the memory devices, such as the signals coupled to the "DDR IO's" block).

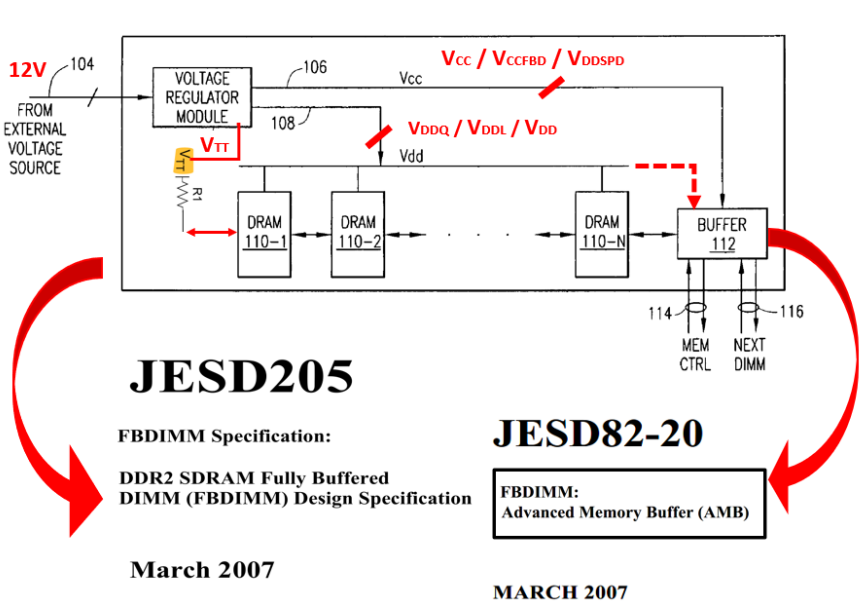
277. Accordingly, the prior art references in each of Grounds 1-3 satisfies "*a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections*."

(4) [1.d.4] Wherein the first circuit is coupled to first and second regulated voltages

278. Claim 1 requires "*wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages*."

279. As explained above for claim limitation [1.c], the prior art references in each of Grounds 1-3 satisfies "*a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages.*" *Supra* ¶¶233-260. As shown in the figures below for Grounds 1 through 2, each of the grounds and voltage mappings maps VDD or VDDQ to the "*first regulated voltage*" and VCC or VCCFBD to the "*second regulated voltage*." *See id.* Ground 3 has the same voltage mappings as Ground 2.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : Vcc / VCCFBD = 1.5V
3rd : VDDL = 1.8V

Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : Vcc = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : Vcc / VCCFBD = 1.5V
3rd : VTT = 0.9V

JESD205

FBDIMM Specification:

DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification

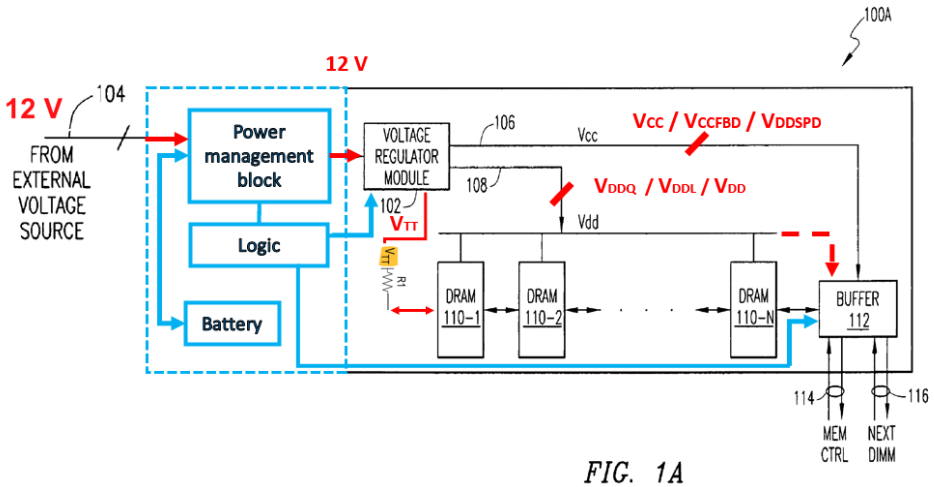
March 2007

JESD82-20

FBDIMM: Advanced Memory Buffer (AMB)

MARCH 2007

Ground 2: Ground 1 and Battery Backup of Amidi



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : Vcc / VCCFBD = 1.5V
3rd : VDDL = 1.8V

Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : Vcc = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : Vcc / VCCFBD = 1.5V
3rd : VTT = 0.9V

FIG. 1A

280. As explained below, a Skilled Artisan would have understood that each of these voltages is coupled to the buffer that includes the "*first circuit*," as disclosed by Harris.

281. With regards to the "*first regulated voltage*," a Skilled Artisan would have recognized that in an implementation of Harris, at least the memory devices

(e.g., DDR2 or DDR4 SDRAM) are coupled to voltage supplies called VDD and VDDQ, as disclosed by the relevant JEDEC standards. *See supra* ¶¶246-250 (VDD or VDDQ for Grounds 1, 2, and 3); *see also* Ex. 1028 (JESD205) at 9 (listing VDD and VDDQ for DRAM), 15 (showing VDD coupled to D0-D17 for DRAM).

282. A Skilled Artisan would also have recognized that VDD or VDDQ are coupled to the buffer as a supply for the DDR memory input/output interface. For example, JESD82-20 (part of FBDIMM Standards) describes VDD/VDDQ as "supply for DDR IO" (Ex. 1027 at p.83) and an "I/O buffer voltage" (Ex. 1027 at 20). *See also* Ex. 1027, pp.168-175 (Pin Assignments for the buffer including VDD), p.44 (describing recommendation voltages for DRAM interface), p. 3 (Figure 1.1) (showing data flow for the AMB buffer including signals coupled to the "DDR IO's" block). Similarly, JESD205 (Ex. 1028, part of FBDIMM Standards) discloses that VDD/VDDQ is a supply for I/O (at 30) and an interface voltage (Ex. 1028 at 33). *See also* Ex. 1028 at 9 (disclosing VDD/VDDQ coupled to the memory devices and the buffer AMB), 13-16 (showing VDD coupled to memory devices and AMB), 31-32 (pin assignments for the buffer including VDD). Thus, the buffer that is disclosed in Harris is coupled to VDD or VDDQ ("*the first regulated voltage*").

283. With regards to the "*second regulated voltage*," Harris illustrates that VCC coupled to the buffer 112 in Figure 1A. Ex. 1023 at Fig. 1A. Also, a Skilled

Artisan would have recognized that an Advanced Memory Buffer (AMB) for an FB-DIMM, such as the FB-DIMM disclosed by Harris in an embodiment, is also provided a voltage supply VCCFBD at 1.5 volts. *See, e.g.*, Ex. 1027 at 78, 82-83. Thus, the buffer that is disclosed in Harris is also coupled to VCC or VCCFBD ("*the second regulated voltage*").

284. Accordingly, the prior art references in each of Grounds 1-3 disclose to a Skilled Artisan "*wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages*."

(5) [1.d.5] Wherein the SDRAM devices are coupled to the first regulated voltage

285. Claim 1 requires "*wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages*."

286. As discussed above, in each of Grounds 1-3, the buffer is coupled to the first and second regulated voltages. *See supra* ¶¶278-284. The first regulated voltage is mapped to VDD or VDDQ. *See supra* ¶¶246-250 (VDD/VDDQ for Grounds 1, 2, and 3). A Skilled Artisan would have understood that VDD and VDDQ are each coupled to the memory devices ("*the plurality of SDRAM devices*"). For example, Harris illustrates in Figure 1A that VDD is coupled to the memory devices (DRAM 110-1 to 110-N), as shown below.

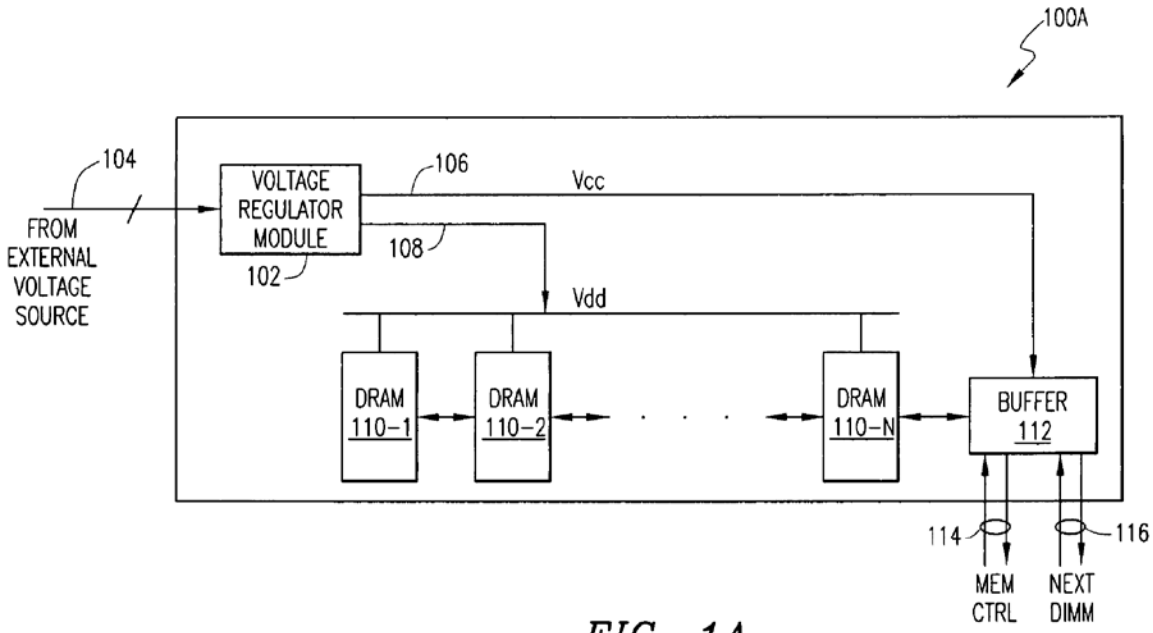


FIG. 1A

Ex. 1023 at Fig. 1A. A Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with memory devices, such as DDR2 SDRAMs, couples those devices to multiple, separate voltage sources, called VDD, VDDQ, and VDDL. *See supra* ¶¶246-250 (VDD/VDDQ for Grounds 1, 2, and 3); *see also* Ex. 1023 at [0009]; Ex. 1028 at 9, 17-20; Ex. 1026 at p.2-3, 6-7, 9.

287. Accordingly, the prior art references in each of Grounds 1-3 satisfies "*wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages*."

2. Claim 2 is Unpatentable

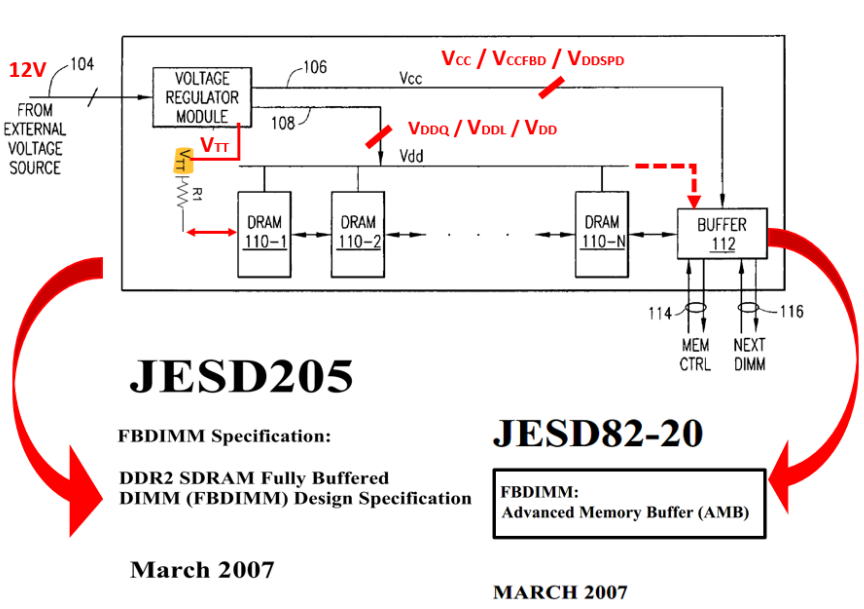
a) [2.a] Wherein the First and Second Regulated Voltages Have Respective First and Second Voltage Amplitudes

288. Claim 2 is unpatentable as the prior art references in each of Grounds 1, 2, and 3 (Voltage Mappings A, B, and C) render the claim obvious.

289. Claim 2 requires "*[t]he memory module of claim 1, wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude*."

290. As explained above for claim limitation [1.c], the prior art references in each of Grounds 1-3 satisfies "*a voltage conversion circuit . . . configured to provide at least three regulated voltages . . . .*" *See supra* ¶¶233-260. As explained for Voltage Mappings A, B, and C for Grounds 1, 2, and 3, the first regulated voltage is VDD or VDDQ at 1.8 volts and the second regulated voltage is VCC or VCCFBD at 1.5 volts.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{DDL} = 1.8V

Voltage Mapping (B)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} = 1.5V
3rd : V_{CCFBD} = 1.5V

Voltage Mapping (C)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{TT} = 0.9V

JESD205

FBDIMM Specification:

DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification

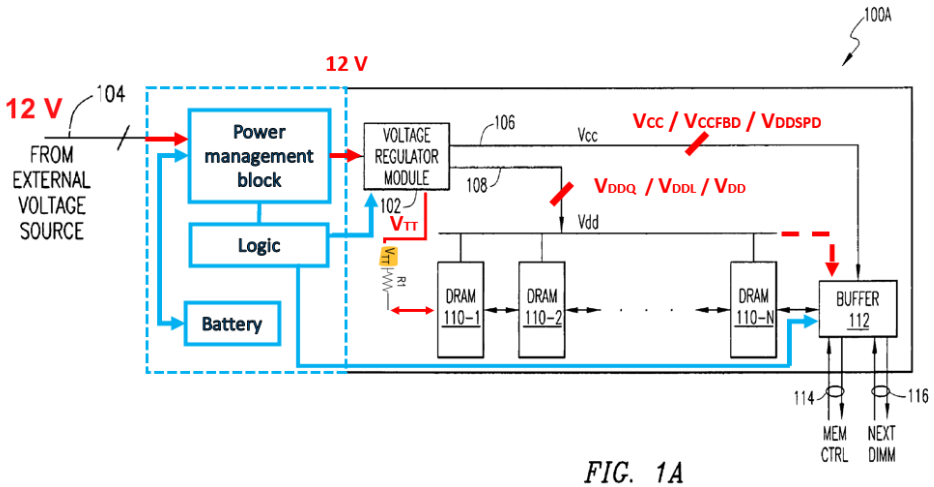
March 2007

JESD82-20

FBDIMM: Advanced Memory Buffer (AMB)

MARCH 2007

Ground 2: Ground 1 and Battery Backup of Amidi



Voltage Mapping (A)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{DDL} = 1.8V

Voltage Mapping (B)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} = 1.5V
3rd : V_{CCFBD} = 1.5V

Voltage Mapping (C)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{TT} = 0.9V

FIG. 1A

291. As shown, the VDD/VDDQ voltage supplies have a voltage amplitude of 1.8 volts and are coupled to the DRAM 110 and Buffer 112, and the VCC/VCCFBD voltage supplies have a voltage amplitude of 1.5 volts and are coupled to the Buffer 112. *See id.*; *see also* Ex. 1023 (Harris) at Fig. 1A, [0009]; Ex. 1028 (JESD205; part of FBDIMM Standards) at 9 (DRAM provided VDD and

VDDQ, each typically at 1.8 volts, and AMB buffer provided VCC and VCCFBD, each typically at 1.5 volts, and VDDQ typically at 1.8 volts); Ex. 1027 (JESD82-20; part of FBDIMM Standards) at p. 83 (listing VCC, VCCFBD, and VDD power supplies provided to AMB); Ex. 1026 (JESD79-2B) at pp.6-7 (VDD and VDDQ, each at 1.8 volts).

292. Accordingly, the prior art in each of Grounds 1 through 3 satisfies the "*wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude*" limitation.

b) [2.b] Wherein One of the First and Second Voltage Amplitudes is Less Than the Other

293. Claim 2 requires "*wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes*."

294. The prior art references in each of Grounds 1 through 3 teaches and discloses this limitation to a Skilled Artisan.

295. As explained for Voltage Mappings A, B, and C for Grounds 1, 2, and 3, the first regulated voltage is VDD or VDDQ at 1.8 volts and the second regulated voltage is VCC or VCCFBD at 1.5 volts. Thus, the second voltage amplitude—1.5 volts—is less than the first voltage amplitude of 1.8 volts. *See supra* ¶¶233-260 (claim limitation [1.c]), ¶¶290-291 (claim limitation [2.a]).

296. Accordingly, the prior art references in each of Grounds 1-3 satisfies the "*wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes*" limitation.

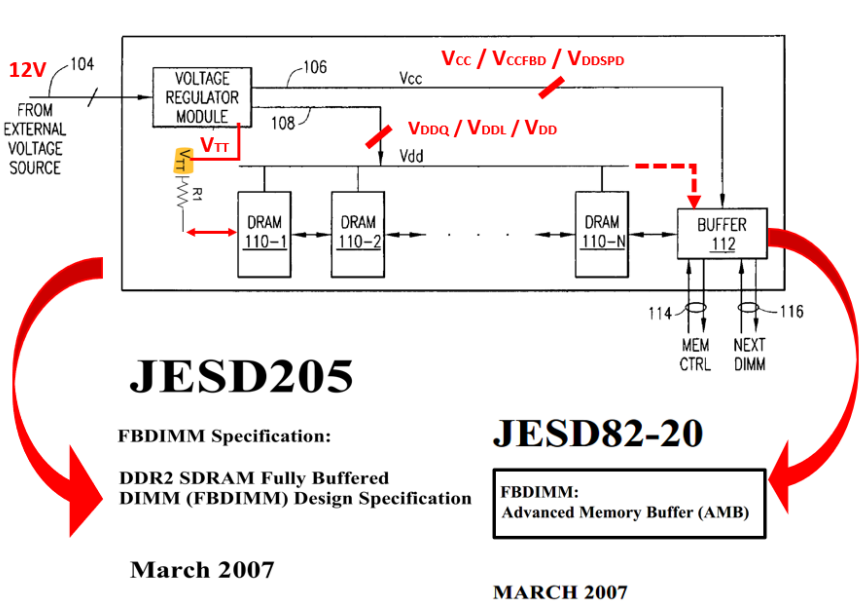
3. Claim 3 is Unpatentable

297. Claim 3 is unpatentable as the prior art references in each of Grounds 1, 2, 3 (Voltage Mapping A) render the claim obvious.

298. Claim 3 requires "*[t]he memory module of claim 1, wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts*."

299. As explained above for claim limitation [1.c], the prior art references in each of Grounds 1-3 satisfies "*a voltage conversion circuit . . . configured to provide at least three regulated voltages . . . .*" *See supra* ¶¶233-260. As explained for Voltage Mapping A for Grounds 1, 2, and 3, the third regulated voltage is VDDL at 1.8 volts (for DDR2 memory devices).

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V

Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V

Ground 2: Ground 1 and Battery Backup of Amidi

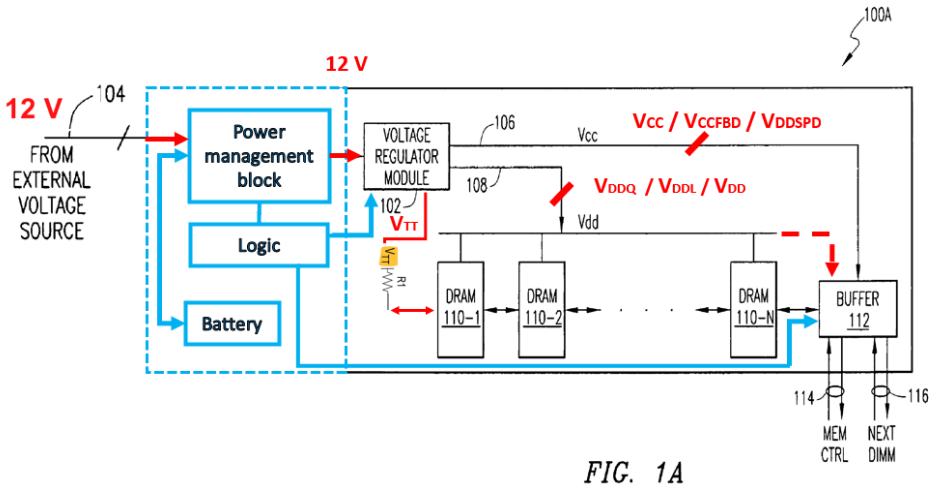


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V

Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V

300. As shown, the VDDL voltage supply has a voltage amplitude of 1.8 volts and is coupled to the DRAM 110. *See supra* ¶¶246-250; *see also* Ex. 1023 (Harris) at [0009] (disclosing memory devices "can be of any known or heretofore unknown DDR type, e.g., DDR2 (operable with 1.8 V)."); Ex. 1028 (JESD205; part of the FBDIMM Standards) at 17-20 (describing pin assignments for DDR2

SDRAM memory, including a VDDL voltage supply); Ex. 1026 (JESD79-2B) at pp. 6 (listing VDDL supply voltage at a voltage amplitude of 1.8 volts), 9 (describing that VDDL can be applied before or at the same time as VDDQ); Ex. 1026 at pp. 2-3 ("VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ.").

301. Accordingly, the prior art references in each of Grounds 1, 2, 3 (Voltage Mapping A) satisfies the "*wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts*" limitation.

4. Claim 4 is Unpatentable

302. Claim 4 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [4.a] Preamble

303. The preamble of claim 4 requires "*[t]he memory module of claim 1, further comprising*."

304. As explained above for claim 1, to the extent the preamble is limiting, it is satisfied by Harris alone, or in combination with the FBDIMM Standards, which disclose a memory module. *Supra* ¶¶216-287; *see, e.g.*, Ex. 1023 (Harris) at Figs. 1A, 3. Similarly, Amidi discloses a memory module with voltage monitoring.

Ex. 1024 (Amidi) at Figs. 4, 6, 15 (illustrating a memory module with voltage monitoring).

305. Accordingly, to the extent the preamble of claim 4 is limiting, the prior art references in each of Grounds 2 and 3 satisfies "*[t]he memory module of claim 1, further comprising*."

b) [4.b] Voltage Monitor Circuit

306. Claim 4 requires "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage*."

307. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

308. As discussed above, it would have been obvious to a Skilled Artisan to incorporate the functionality of battery backup power, as taught by Amidi, when implementing the memory module teachings of Harris to address the case of a power or clock malfunction. *See supra* ¶¶171-180 (Ground 2). As shown in the figures below, Grounds 2/3 disclose a memory module with battery backup power

for when there is a power or clock malfunction. As previously discussed, Ground 3 has the same Voltage Mappings as Ground 2. *Supra* ¶¶181-188.

Ground 2: Ground 1 and Battery Backup of Amidi

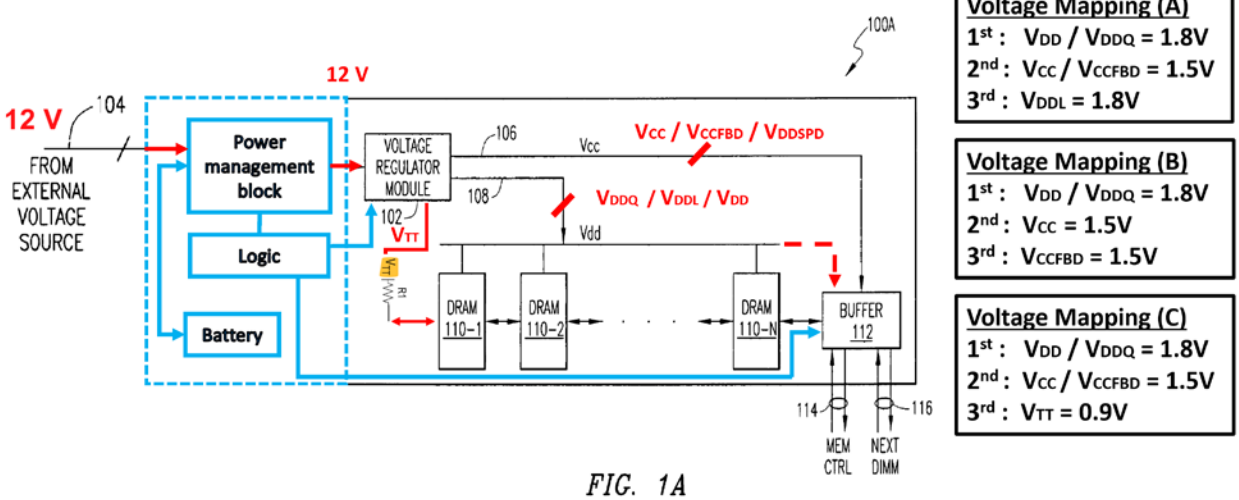


FIG. 1A

Ex. 1023 at Fig. 1A (annotated with teachings of Amidi); *see, e.g.*, Ex. 1024 at Abstract, 1:28-35, 2:6-26, Figs. 5, 6. As shown, the memory module includes power management and logic functionality as well as a battery, as taught by Amidi. The power management functionality is coupled to the external voltage source 104 and battery, on one hand, and the voltage regulator module 102, on the other. And, the logic functionality is coupled to the power management functionality, the voltage regulator module 102, and the buffer 112. *See id.*

309. In each of the combinations, Amidi teaches and discloses a "*voltage monitor circuit*" that implements the power supervisory functionality, such as the power supervisory module 480, the voltage supervisory block 665, and the voltage supervisory block 800. As shown below in Figure 4 of Amidi, the power

supervisory module 480 (annotated in red) is coupled to the PCB that has an edge connector (annotated in orange).

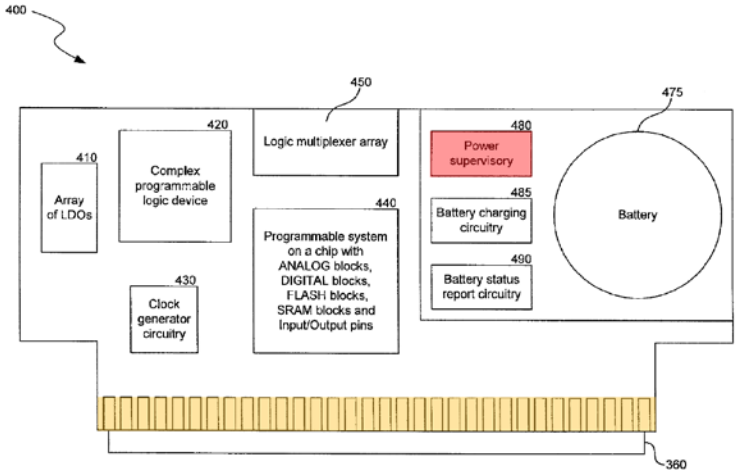
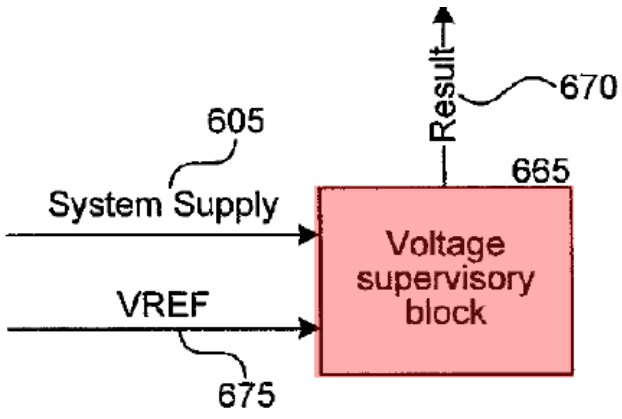


FIG. 4

Ex. 1024 at Fig. 4 (annotated). Thus, Amidi describes "*a voltage monitor circuit coupled to the PCB*."

310. In addition, as shown below in Figure 6 of Amidi, it also describes a "Voltage supervisory block" 665 (annotated in red in figure below) that is configured to monitor the "System Supply" 605 to determine if there is a power malfunction.



Ex. 1024 at Fig. 6 (excerpted and annotated), 5:35-43. As Amidi explains, "Signal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two. If system supply 605 has a greater magnitude than reference voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660. If system supply 605 has a magnitude lower than reference voltage 675, then signal 670 causes power switch multiplexer 655 to choose battery power 650 for memory supply 660." *Id.* at 5:35-43. Thus, Amidi's voltage supervisory block is configured to monitor the system supply that is configured to produce signal 670 ("*a trigger signal*") that is generated in response to the system supply having a voltage amplitude below a specified reference voltage ("*in response to the input voltage having a voltage amplitude below a predetermined threshold voltage*"). *See id.*; *see also id.* at 8:23-29, Fig. 14 (illustrating a method that includes monitoring the input power supply at 1435), Fig. 15 and 9:8-12 (describing monitoring system, including monitoring input power supply for proper levels).

311. Further, as shown below in Figure 8 of Amidi, it also describes a voltage supervisory block 800 that includes voltage supervisory circuitry 835.

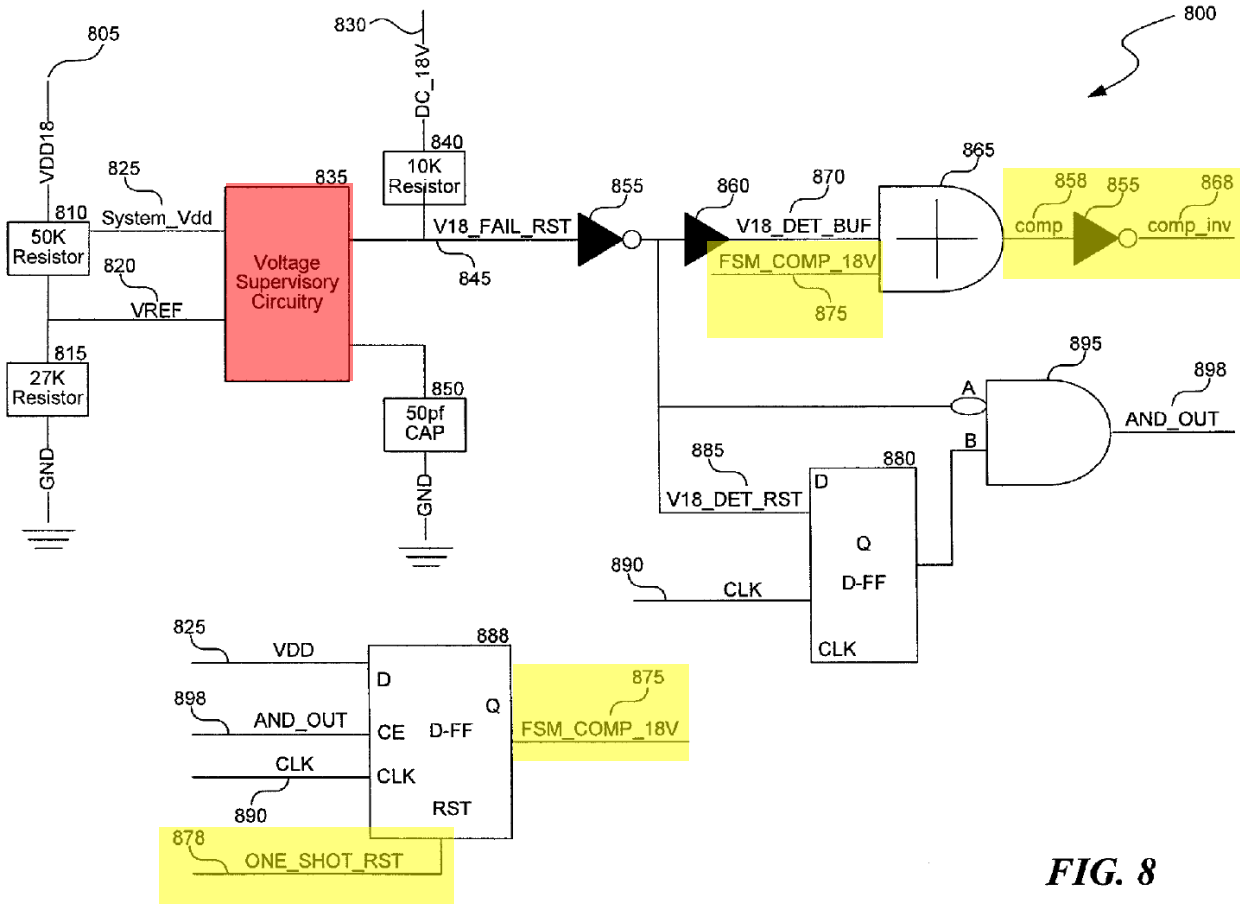


FIG. 8

Ex. 1024 at Fig. 8 (annotated). As Amidi explains, "[v]oltage supervisory block 800 compares a system voltage with a reference voltage [(annotated in red in Figure 8 above)], and generates output signals with various logic components to control other parts of the power supply circuitry." *Id.* at 5:31-34. In addition, as annotated in yellow in Figure 8 above, a "[o]ne-shot reset signal 878 resets flip-flop 888, thereby clearing [finite state machine] signal 875" (*id.* at 5:61-62), which is used to produce "[c]omparison signal 858 and inverted comparison signal 868 [which] may be used as a logically paired set of signals to control a power multiplexer such as that of FIG. 7" (*id.* at 5:51-53). *See also id.* at 5:48-50, Fig. 7.

Thus, Amidi's voltage supervisory block 800 compares the system voltage with a reference voltage and generates a signal that is used to set a finite state machine signal and control a power multiplexer, and receives a one-shot signal to reset or clear the finite state machine signal and the power multiplexer.

312. Moreover, as shown below in Figure 14 of Amidi, it explains that the memory module moves into a power fault detection state at module 1440 when power fault is detected (annotated in red in Figure 14 below), initiates a self-refresh state for the memory at module 1450 (annotated in orange in Figure 14 below), and exits self-refresh and switches over to system power at modules 1460, 1470, 1480, and 1490 (annotated in yellow in Figure 14 below).

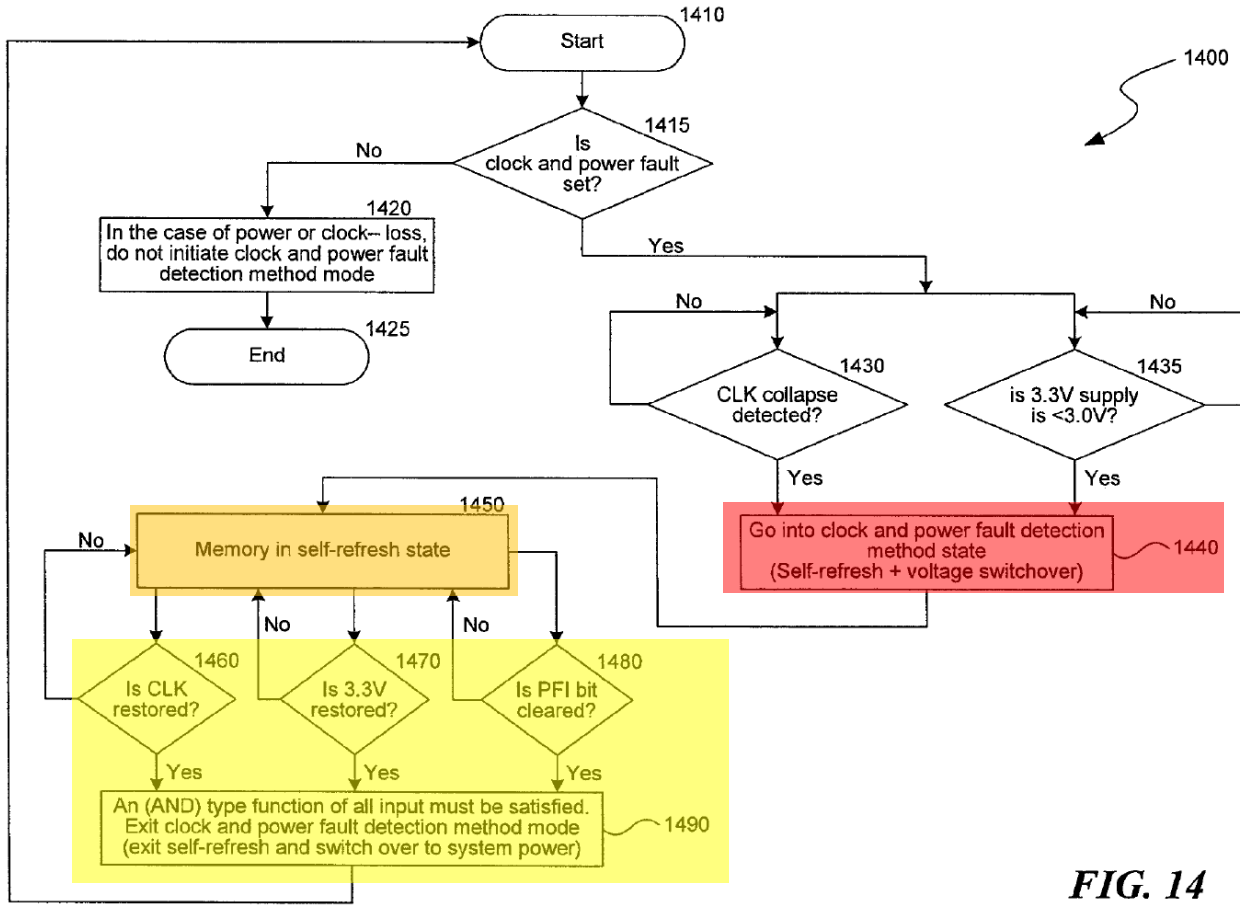


FIG. 14

Ex. 1024 at Fig. 14 (annotated). Amidi explains that module 1440 "may include setting a power fail interrupt bit in a register, indicating that a power failure was detected (or a clock failure) and the memory module assumed control." *Id.* at 8:30-36. In the self-refresh state at module 1450, "refresh is controlled by the memory module's on-board circuitry, rather than by system signals." *Id.* at 8:38-41. Then, at module 1460, "a check is made as to whether the clock signal is restored" (*id.* at 8:43-44), at module 1470, "a check is made as to whether the power rail is restored" (*id.* at 8:44-47), and at module 1480, a check is made as to "whether a bit has been cleared indicating the system is ready to take back control of the memory

module" such as by checking the "power fail interrupt bit" (*id.* at 8:51-54). As Amidi explains, "[t]ypically each of modules 1460, 1470 and 1480 must be satisfied—the power supply must be stable, the clock must be stable, and the power fail bit must be clear—before the memory module will release operation back to the system." *Id.* at 8:54-58; *see also id.* at Figs. 11 (illustrating entry and exit for the self-refresh state), 12 (illustrating finite state machine signals 1215 produced by Programmable System on a Chip (PSOC) 1210 and finite state machine 1230), 8:59-62. Thus, Amidi teaches that the "*voltage monitor circuit*" also detects when the host system makes a request to indicate that it is ready to take back control of the memory module, such as by clearing the power fail interrupt bit.

313. In the combinations illustrated and described above for Grounds 2 and 3, Amidi's voltage supervisory block is part of the power management and logic functionality that is coupled to the external voltage source of Harris that is input at 12 volts. *See, e.g.*, Ex. 1024 (Amidi) at Figs. 5, 6; Ex. 1023 (Harris) at [0010], [0012]. Harris discloses and teaches that the external voltage source 104, such as one at 12 volts, is received through some of the edge connections of the memory module, as explained for claim limitation [1.b] ("*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple*

power, data, address and control signals between the memory module and the host system"). *See supra* ¶¶224-232; *see also* Ex. 1023 (Harris) at [0010], [0012] (describing the number of pins for a 12 volt input **from an external voltage source** in various implementations) (emphasis added), [0019], Fig. 1A. In addition, Harris alone or in combination with the FBDIMM Standards discloses a buffer for buffering data, address, and control signals that are coupled to a first set of edge connections, as explained for claim limitation [1.d.3] ("*a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections*"). *See supra* ¶¶272-277. Thus, Harris and Amidi teach and disclose that Amidi's voltage supervisory block is coupled to a second set of the edge connections on Harris's memory module in which the voltage supervisory block is configured to monitor the external voltage source, such as one at 12 volts, that is received from the second set of edge connections. ("*a voltage monitor circuit coupled . . . to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections*").

314. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge*

Samsung Electronics Co., Ltd.
Ex. 1069, p. 170

connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage."

c) [4.c] Wherein the memory module transitions from a first operable state to a second operable state

315. Claim 4 requires "*wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal*."

316. The prior art references in each of Grounds 2 and 3 teaches this limitation to a Skilled Artisan.

317. As discussed above for claim limitation [4.b], the prior art references in each of Grounds 2 and 3 satisfy ". . . *the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage*." *Supra* ¶¶306-314. As discussed above, it would have been obvious to a Skilled Artisan to incorporate the functionality of battery backup power, as taught by Amidi, when implementing the memory module teachings of Harris in order to avoid data loss and/or damaging the device in case of a power or clock malfunction. *Supra* ¶¶171-180 (Ground 2). In the combination, the memory module operates on an external voltage source when the voltage amplitude of the external voltage source is above a specified threshold voltage ("*a first operable state*") and the module operates on a backup voltage source, such as a battery backup, by entering a self-refresh state when the

voltage amplitude of the external voltage source is below a specified threshold voltage ("*a second operable state*").

318. As explained by Amidi, the transition from the "*first operable state*" to the "*second*" is performed in response to a trigger (signal 670):

> "Signal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two. If system supply 605 has a greater magnitude than reference voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660. If system supply 605 has a magnitude lower than reference voltage 675, then signal 670 causes power switch multiplexer 655 to choose battery power 650 for memory supply 660."

Ex. 1024 at 4:44-52; *see also id.* at Figs. 6-8, 4:60-5:24 (describing Fig. 7), 5:25-62 (describing Fig. 8, including voltage supervisory circuitry 835 and "output signals with various logic components to control other parts of the power supply circuitry").

319. Amidi also explains that upon initiating battery backup power, the memory module maintains its memory in a self-refresh state (the "*second operable state*"):

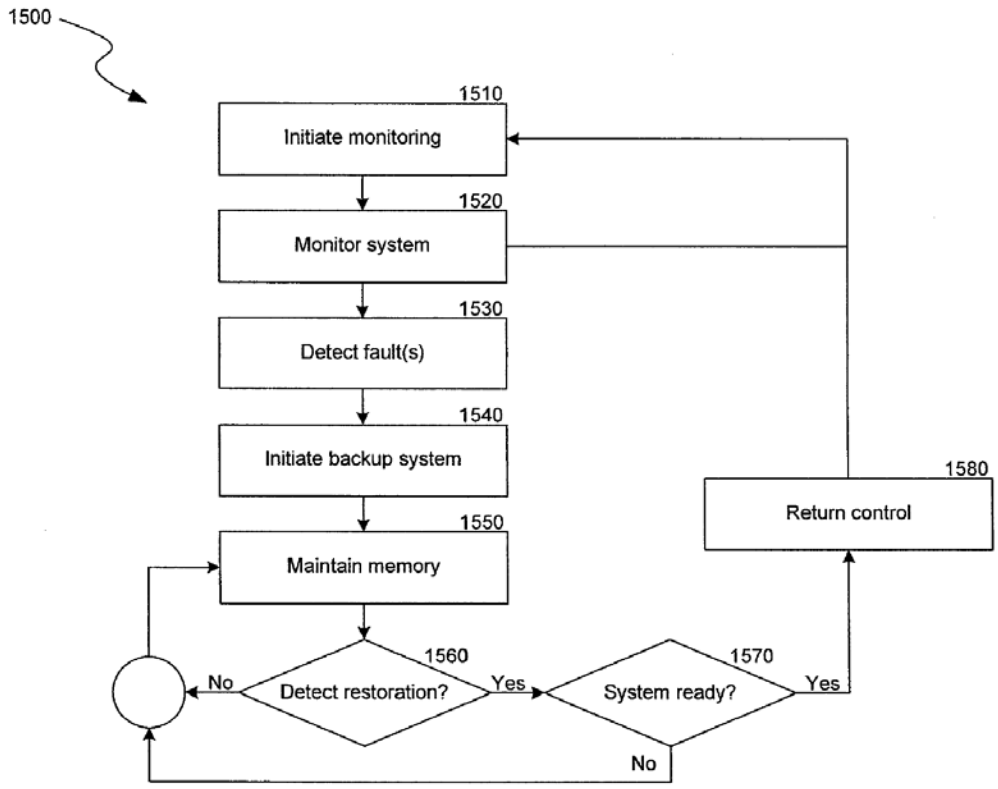


FIG. 15

Ex. 1024 at Fig. 15. Specifically, "[a]t module 1520, the system is monitored, with power and clock signals checked for proper levels (power) or proper signals (clock). At module 1530, a fault is detected, whether in the clock or power signals (or both). The backup system is initiated at module 1540, with the system taking over supply of the clock and power signals. … With the backup system operating, the memory module is maintained at module 1550—power is supplied from a battery and a clock signal is generated to allow the module to refresh memory." *Id.* at 9:8-22. A Skilled Artisan would have understood from Amidi's disclosure that, in response to the signal detecting a fault in power (e.g., signal 670 in Figure 6 of

Amidi), the memory module transitions from a first state that depends on the system for the supply of power into a second state that depends on battery backup for the supply of power to maintain the data in the memory devices.

320. Similarly, as shown below in Figure 14, Amidi explains that, after a power or clock fault is detected, the memory module moves into a power fault detection state at step 1440 ("Self-refresh + voltage switchover," annotated in red in Figure 14 below) and initiates a self-refresh state for the memory at step 1450 (annotated in orange in Figure 14 below), and exits the self-refresh state and switches back to system power at step 1490 if all conditions 1460, 1470, and 1480 are satisfied (annotated in yellow in Figure 14 below).

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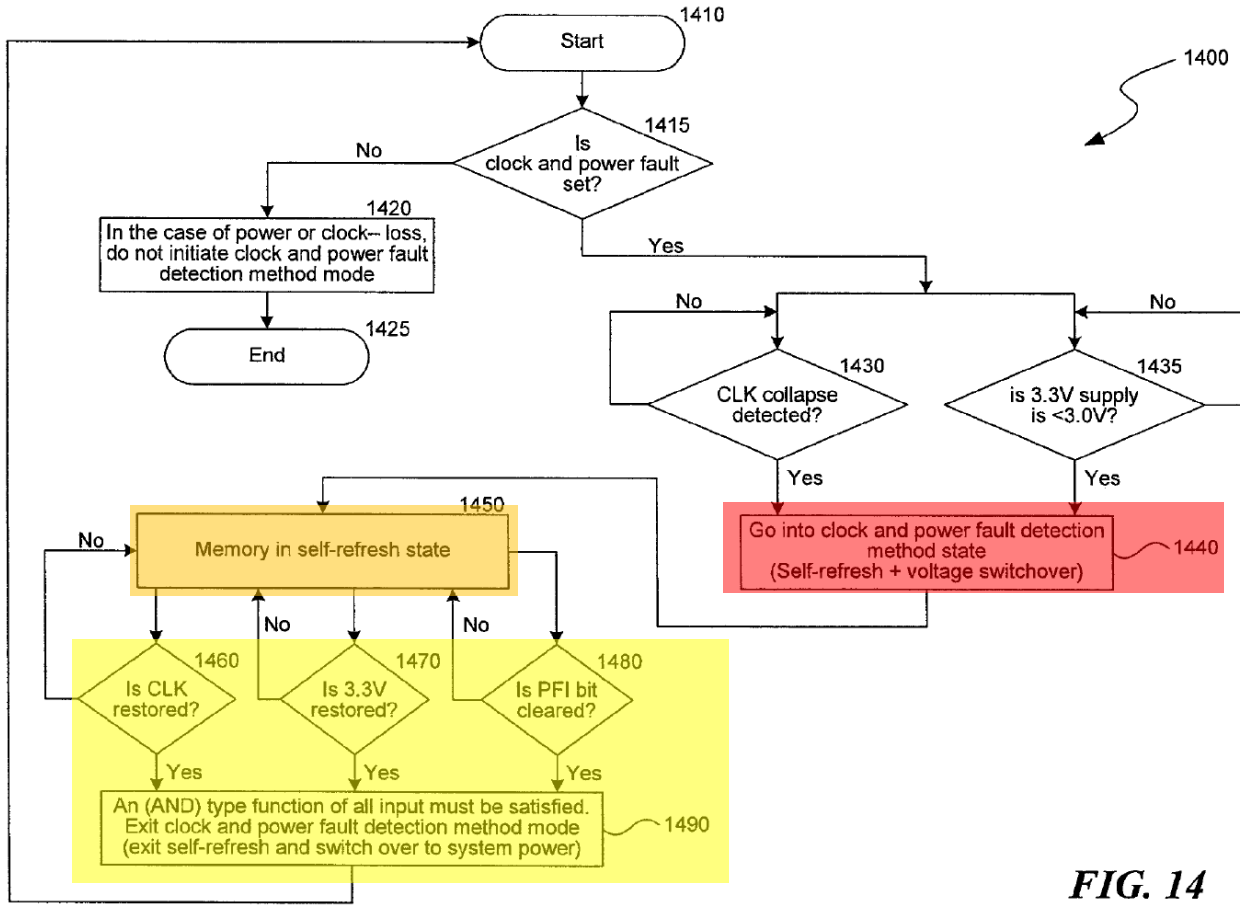


FIG. 14

Ex. 1024 at Fig. 14 (annotated). Amidi explains that step 1440 "may include setting a power fail interrupt bit in a register, indicating that a power failure was detected (or a clock failure) and the memory module assumed control." *Id.* at 8:30-36. In the self-refresh state (1450, orange), "refresh is controlled by the memory module's on-board circuitry, rather than by system signals." *Id.* at 8:38-41. A Skilled Artisan would have understood from Amidi's disclosure that, in response to the signal detecting a fault in power (e.g., at step 1435) the memory module transitions from a "*first operable state*" that depends on the system for the supply of power into a "*second operable state*" (e.g., 1450, orange) that depends on

battery backup for the supply of power to maintain the data in the memory devices during a self-refresh state. As discussed for claim limitation [5.b] below, a Skilled Artisan would have been motivated to implement Amidi's logic functionality using the S3 sleep mode functionality of the Buffer 112, as disclosed by Harris to a Skilled Artisan, that performs the function of refreshing the memory (e.g., self-refresh), just like in Amidi. *See infra* ¶¶330-331.

321. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies "*wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal*."

5. Claim 5 is Unpatentable

322. Claim 5 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [5.a] Preamble

323. The preamble of claim 5 requires "*[t]he memory module of claim 4, further comprising*."

324. As explained above for claim 4, to the extent the preamble is limiting, it is satisfied by the prior art references in each of Grounds 2 and 3, which discloses a memory module. *Supra* ¶¶302-321; *see, e.g.*, Ex. 1023 (Harris) at Figs. 1A, 3; Ex. 1024 (Amidi) at Figs. 6, 14-15.

325. Accordingly, to the extent the preamble of claim 5 is limiting, the prior art references in each of Grounds 2 and 3 satisfies "*[t]he memory module of claim 4, further comprising*."

b) [5.b] Controller Coupled to the Voltage Monitor Circuit

326. Claim 5 requires "*a controller coupled to the voltage monitor circuit*."

327. The prior art references in each of Grounds 2 and 3 teaches this limitation to a Skilled Artisan.

328. As discussed above, it would have been obvious to a Skilled Artisan to incorporate the functionality of battery backup power, as taught by Amidi, when implementing the memory module teachings of Harris to address the case of a power or clock malfunction. *Supra* ¶¶171-180 (Ground 2), ¶¶181-188 (Ground 3). As shown in the figures below, Grounds 2/3 disclose a memory module with battery backup power when there is a power or clock malfunction.

Ground 2: Ground 1 and Battery Backup of Amidi

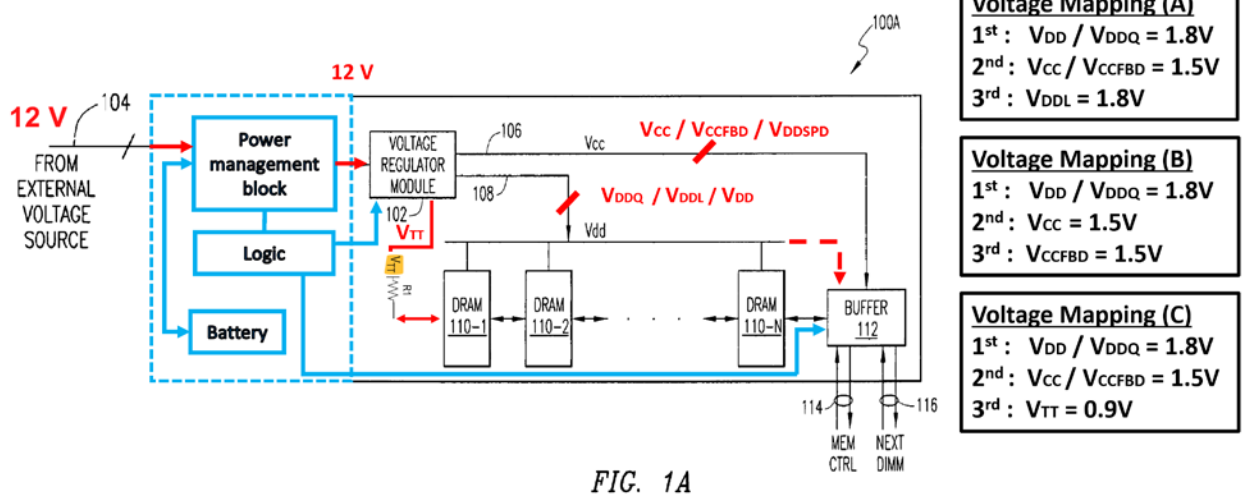


FIG. 1A

Ex. 1023 at Fig. 1A (annotated with teachings of Amidi); *see, e.g.*, Ex. 1024 at Abstract, 1:28-35, 2:6-26, Figs. 5, 6. As shown, the memory module includes a power management and logic functionality as well as a battery, as taught by Amidi. The power management functionality is coupled to the external voltage source 104 and battery, on one hand, and the voltage regulator module 102, on the other. And, the logic functionality is coupled to the power management functionality, the voltage regulator module 102, and the buffer 112. *See id.* And, as discussed above for claim limitation [4.b], Amidi teaches and discloses a "*voltage monitor circuit*" that implements power supervisory functionality, such as the power supervisory module 480, the voltage supervisory block 665, and the voltage supervisory block 800. *See supra* ¶¶306-314. As Amidi explains, the voltage supervisory block 665 generates a signal 670 in response to the system supply having a magnitude lower than the reference voltage. *See* Ex. 1024 at 4:44-52, Figs. 6-8. In response to the signal, Amidi teaches that the memory module operates on a battery backup supply instead of a system supply. *See supra* ¶¶315-321; Ex. 1024 at 9:8-22, Fig. 15.

329. Amidi discloses functionality that controls logic operations in the case of a power failure ("*a controller*"). For example, Amidi discloses that, in the case of power failure, a memory module's power control system disconnects the system address and command signals from the memory module and, instead, a Finite State Machine generates refresh commands for the memory devices. Ex. 1024 at Fig. 12

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(reproduced and annotated below), 7:24-34 ("This allows PSOC 1210 to produce finite state machine signals 1215 and timer signals 1225. These signals are used to control finite state machine 1230, which produces signals that control refresh of memory of a memory module. This also produces signal logic multiplexer select signal 1255, which selects an input for multiplexer 1240. Multiplexer 1240 is a logic signal multiplexer, accepting as input a set of system control and command bus signals 1235 and sets of finite state machine control and command bus signals 1245 to produce memory control and command bus signals."); *see also id.* at Fig. 8 and 5:31-34 ("Voltage supervisory block 800 compares a system voltage with a reference voltage, and generates output signals with various logic components to control other parts of the power supply circuitry.").

330. Furthermore, a Skilled Artisan would have recognized that when implementing the memory module in Harris, the buffer 112 would have supported being placed in an S3 sleep mode when the external voltage source is decoupled in response to Amidi's voltage supervisory block. For example, JESD82-20 (part of the FBDIMM Standards, focused on the AMB buffer), discloses that "S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode." Ex. 1027 at 39 (Section 4.1.3). It also discloses that "[w]hen the Advanced Memory Buffer [AMB] core logic is in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other

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command/address pins, will be driven low. In S3 mode, 1.8V supply is on. 1.5V, Vtt, and 3.3V are off. DRAMs are in self refresh, and the CKE signals must be driven low." *Id.* at 21 (point 6). Therefore, a Skilled Artisan would have been motivated to use the S3 mode of the buffer 112 when implementing the backup power supply and logic functionality, as disclosed in Amidi, because S3 mode performs the function of refreshing the memory (e.g., self refresh), just like in Amidi.

331. Accordingly, a Skilled Artisan would have been motivated to implement Amidi's logic functionality using the S3 sleep mode functionality of the buffer 112, as disclosed by Harris to a Skilled Artisan. Indeed, a Skilled Artisan would have understood that the S3 sleep mode uses a small amount of power, thus extends the life of the battery when backup power is used. *See also* Ex. 1039 at [0065] (describing power saving operations for AMB). Further, using the S3 sleep mode of the buffer 112 would avoid duplicating similar functionality in the combination.

332. In the combination, Amidi's power management functionality would monitor the system supply (using a "*voltage monitor circuit*") and if a fault is detected, trigger the backup supply and Amidi's logic functionality to initiate the S3 sleep mode functionality of the buffer 112 ("*controller*") to place the DRAM in self-refresh. Thus, the logic and S3 sleep mode functionality ("*controller*") is

coupled to Amidi's voltage supervisory block ("*coupled to the voltage monitor circuit*").

333. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*controller coupled to the voltage monitor circuit*" limitation.

c) [5.c] Wherein the Controller is Configured to Perform One or More Operations

334. Claim 5 requires "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*."

335. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan. As discussed above for claim limitation [5.b], the logic functionality in the combination ("*controller*") is coupled to the monitoring functionality (e.g., voltage supervisory block in Amidi) ("*coupled to the voltage monitor circuit*"). *Supra* ¶¶326-333.

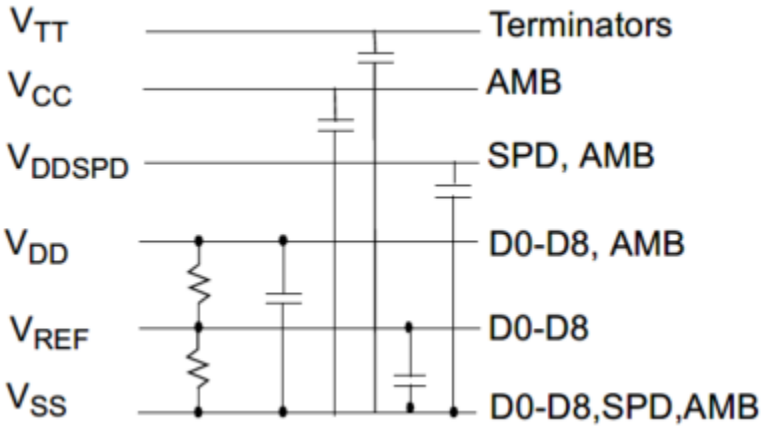
336. In particular, Amidi's voltage supervisory block and associated logic detects a fault in the system supply and in response generates a trigger signal. *Supra* ¶¶306-314 ([4.b]), 315-321 ([4.c]) (discussing the voltage supervisory block in the combination). In response to the trigger signal, Amidi's power management and logic functionality switches to battery backup power supply (*see id.*) and initiates the logic in Harris's buffer 112 to place the DRAM in self-refresh using the S3 sleep mode functionality (*see supra* ¶¶326-333 ([5.b])). Thus, the prior art

references in Grounds 2 and 3 teach and disclose "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations*."

337. To the extent Netlist asserts that the limitation of "*a write operation to transfer data to non-volatile memory*" is satisfied by writing configuration information into a non-volatile memory, the prior art references in Grounds 2 and 3 also teach and disclose this limitation. Specifically, Harris discloses to a Skilled Artisan that when implementing a memory module with the buffer 112, logic in the buffer (part of the "*controller*") writes control and status information into non-volatile memory before entering S3 sleep mode and recovers the stored information before resuming normal operations. *See* Ex. 1027 (JESD82-20, part of FBDIMM Standards) at 25 (Section 3.7.3) ("The following [Control and Status Registers] should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin."); *see also id.* at 95 (Table 11.7) (showing DAREFTC, MTR, DSREFTC, DRC registers), 96 (Table 11.8) (showing S3RESTORE registers), 141 ("Section 11.6.1.3 S3RESTORE[15:0] : DDR State Restore").

338. A Skilled Artisan would have understood that the non-volatile memory can be internal or external to the buffer 112. For example, JESD205 (part of the FBDIMM Standards) discloses that the VDDSPD voltage supply at 3.3 volts is coupled to both the AMB buffer and serial presence detect (SPD) EEPROM.

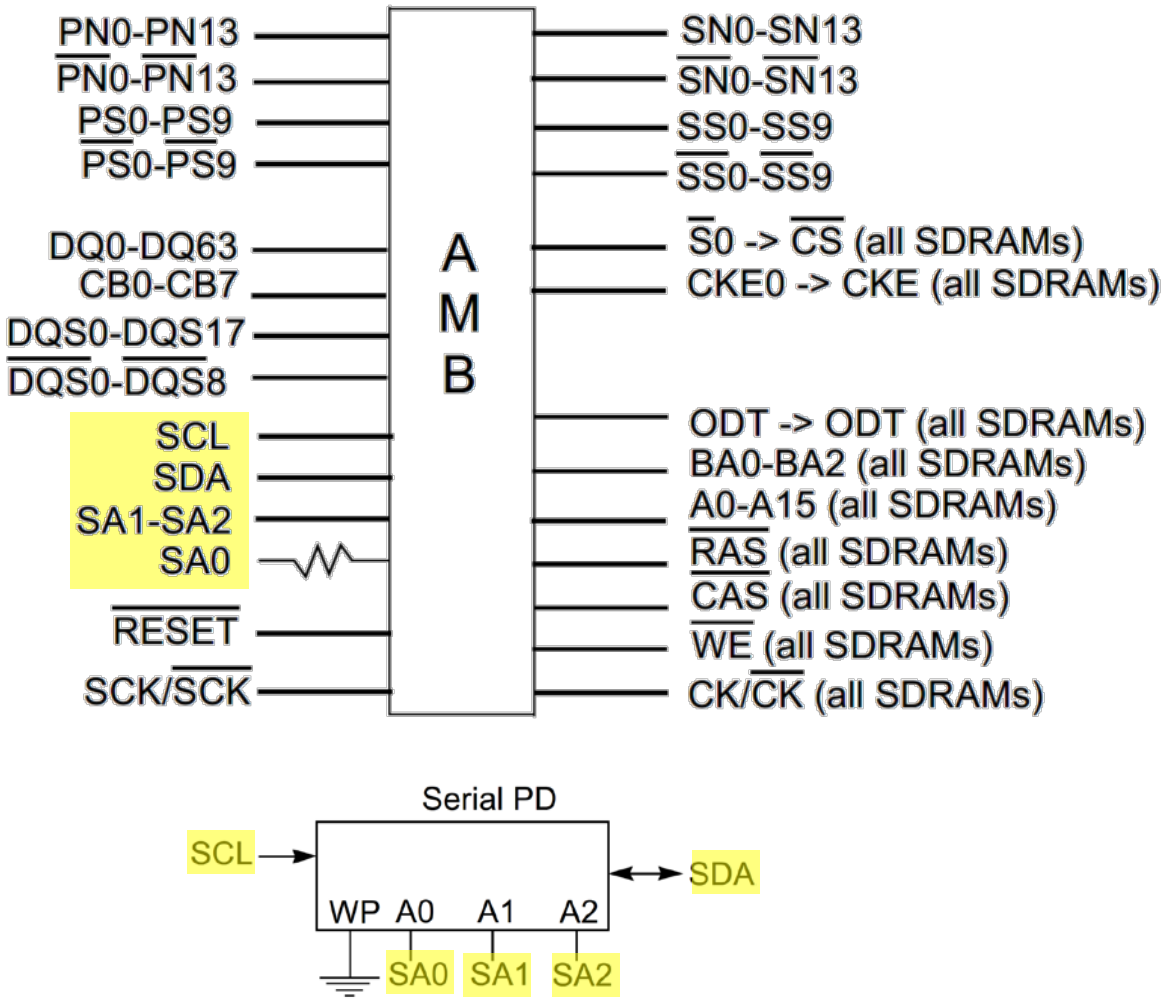
Ex. 1028 at 13-16 (excerpt from p.13 reproduced below), 30 ("SPD Power (3.3 Volt)"), 32 (illustrating AMB pin assignment for VDDSPD at AB27).



This indicates to a Skilled Artisan that the AMB buffer, like the SPD, can contain non-volatile memory, such as an EEPROM, for storing data using a higher voltage supply at 3.3 volts. Furthermore, it would have been obvious to a Skilled Artisan to implement the buffer 112 with an internal non-volatile memory because it would decrease the number of components, interfaces and interconnections on the memory module, resulting in a cheaper, faster, and more secure solution. *See e.g.*, Ex. 1023 (Harris) at [0002] (discussing cost-effective support for next generation DRAM technology), [0012] (discussing reduced pins), [0019] (discussing a "reduction in the pin count" and reserving "extra pins for implementing additional or proprietary functions"); Ex. 1066 at 26:64-27:4 ("In embodiments, modes of operation are determined in response to a control signal from master 2101, or other circuit or in response to reading configuration information ***stored in a separate storage circuit in a device, such as an SPD device or register on the buffer or***

controller device, disposed on system 2600. Modes of operation may be determined at initialization, periodically or during calibration of system 2600.") (emphasis added); Ex. 1067 (LatticeXP Datasheet) at 1 (describing FPGA technology with internal non-volatile memory and explaining its advantages, including "Instant-on—powers up in microseconds," "No external configuration memory," "Excellent design security, no bitstream to intercept") and 2 ("With this [re-programmable non-volatile] technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. In addition, instant-on capability allows for easy interfacing in many applications.").

339. With regards to non-volatile memory that is external to the buffer, JESD205 (part of the FBDIMM Standards) illustrates that the SPD EEPROM, a non-volatile memory, is coupled to the AMB buffer via the SCL, SA0, SA1, SA2, and SDA signals.



Ex. 1028 at 13 (excerpted and annotated). Accordingly, a Skilled Artisan would have understood that the non-volatile memory is internal or external to the buffer 112. Thus, the "*controller*" includes logic in the buffer 112 for S3 sleep mode functionality, which is configured to perform several operations, including storing data, as required by the S3 sleep mode, to non-volatile memory (e.g., internal or external to the buffer) ("*the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*").

340. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*" limitation.

6. Claim 6 is Unpatentable

341. Claim 6 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [6.a] Preamble

342. The preamble of claim 6 requires "*[t]he memory module of claim 1, further comprising*."

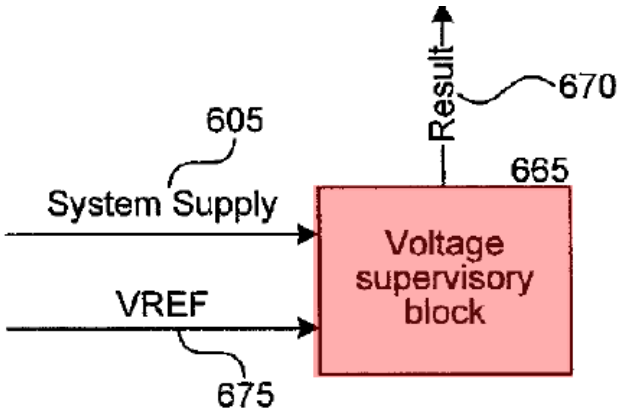
343. As explained above for claim 1, to the extent the preamble is limiting, it is satisfied by Harris alone, or in combination with the FBDIMM Standards, which disclose a memory module. *Supra* ¶¶216-287; *see, e.g.*, Ex. 1023 (Harris) at Figs. 1A, 3. Similarly, Amidi discloses a memory module with voltage monitoring. Ex. 1024 (Amidi) at Figs. 4, 6, 15 (illustrating a memory module with voltage monitoring).

344. Accordingly, the extent the preamble of claim 6 is limiting, the prior art references in each of Grounds 2 and 3 satisfies "*[t]he memory module of claim 1, further comprising*."

b) [6.b] Voltage Monitor Circuit

345. Claim 6 requires "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage*."

346. For the reasons discussed above with reference to claim limitation [4.b], the prior art references in each of Grounds 2 and 3 disclose and render obvious "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage*" to a Skilled Artisan. *Supra* ¶¶306-314. As discussed, Amidi discloses a voltage supervisory block included in a "*voltage monitor circuit*" that, in the combination, monitors Harris's external voltage source 104, such as one at 12 volts, which is received through some of the edge connections of Harris's memory module.



Ex. 1024 at Fig. 6 (excerpted and annotated), 5:35-43.

347. Although Amidi teaches and discloses a circuit configured to detect an undervoltage ("*the input voltage having a voltage amplitude below a predetermined threshold voltage*"), as recited in claim limitation 4[b] and addressed above, Harris teaches both undervoltage and overvoltage detection. *Supra* ¶¶306-314; *see also* Ex. 1024 (Amidi) at 5:35-43, 8:23-29, 9:8-12, Figs. 6, 14. In particular, Harris teaches that a memory module can accommodate up to a 15% variation above and below the nominal external supply voltage ("*input voltage*") that is not supplied directly to the memory devices or logic components of the memory module. Ex. 1023 (Harris) at [0013] ("Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated . . . ."). Accordingly, Harris teaches that a memory module needs to detect and protect against an input voltage amplitude greater than 15% above a

nominal value or less than 15% below a nominal value, which cannot be accommodated.

348. A Skilled Artisan would have understood from, and been motivated by, this disclosure and teaching in Harris to include overvoltage detection in addition to undervoltage detection as taught by Amidi. As long as the input voltage amplitude remains within that range above or below 15% of the nominal value, such as 12 volts, that system supply voltage is provided to Harris's voltage regulator module, but when the system supply is beyond this range, the combination switches to battery backup, as Amidi teaches, to avoid supplying voltages that Harris's memory module cannot accommodate. *See* Ex. 1023 (Harris) at [0013]. Thus, a Skilled Artisan would have been motivated to modify Amidi's Voltage Supervisory Block 665 to generate a signal ("*trigger signal*") such that the battery backup is selected if the system supply voltage is less than 85% of the nominal value, such as 10.2 volts for a 12-volt supply, (*see* "*the input voltage having a voltage amplitude below a predetermined threshold voltage*" of claim 4 above) or if it is greater than 115% of the nominal value, such as 13.8 volts for a 12-volt supply ("*the input voltage having a voltage amplitude above a predetermined threshold voltage*"). Otherwise, the system supply is selected when the system supply voltage ("*input voltage*") is between the "*predetermined*

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threshold voltage" of claim 4 and the "*predetermined threshold voltage*" of claim 6.

349. Such a modification of Amidi's Voltage Supervisory Block was well within the level of skill of a Skilled Artisan at the time.

350. For example, U.S. Patent Publication No. 2009/0034354 to Resnick ("Resnick") describes generating "an alarm signal if the difference between the operating voltage and the reference voltage indicates the operating voltage is outside of a normal operating range" for a memory device. Ex. 1065 at Abstract, [0002], [0014], Fig. 1. For example, the alarm signal is generated when "the operating voltage [is] above an upper threshold or below a lower threshold." *Id.* at Fig. 5 (block 530). Resnick explains that a "voltage sensor 110 may be configured to signal an alarm in the case where the operating voltage is outside of a range" which relates to the "magnitude of the voltage [going] beyond a predetermined threshold level, which may be an upper or lower level relative to an expected, or normal operating voltage." *Id.* at [0018]. Further, "[i]f the operating voltage is above or below the relevant threshold, voltage sensor 110 may indicate the voltage failure by sending a flag such as alarm signal 112 to a pin on semiconductor memory device 100 for signaling the alarm externally." *Id.* at [0019]; *see also id.* at [0031], [0033], Figs. 1-3. Thus, by way of example, Resnick shows that, at the time, a Skilled Artisan would have been able to design a voltage detection circuit

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that detects different types of anomalies on a memory module, including the amplitude of the voltage going beyond a predetermined level, and that indicates a voltage failure by sending a flag such as an alarm signal.

351. As another example, a National Semiconductor datasheet for LMC6953 describes an over-voltage threshold of 5.6 volts for a 5-volt power supply. *See* Ex. 1063 at 1-2 (reproduced below and annotated for both over-voltage and under-voltage).

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

352. As another example, an Analog Devices datasheet for ADM1066 describes programmable circuits to "detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out-of-window fault (undervoltage or overvoltage)." Ex. 1061 at 15; *see also* Ex. 1062 at 15 ("Two comparators are

dedicated to each input so that undervoltage and overvoltage detection can be implemented . . . .").

353. Accordingly, the prior art references in Ground 2 (Grounds 1 in view of Amidi) satisfies the limitation.

354. To the extent one were to argue that overvoltage detection was not obvious in light of Ground 2, it would have been obvious in further view of Hajeck, as part of Ground 3. As explained above, a Skilled Artisan would have been motivated to combine the references in Ground 2 with Hajeck. *See supra* ¶¶181-188; *see also supra* ¶138. U.S. Patent No. 6,858,556 to Hajeck ("Hajeck") describes the operation of a "conventional voltage detection circuit." Ex. 1038 at 3:33-34; *see also id.* at Abstract, 1:62-2:7, 3:30-4:9. Hajeck discloses:

> "[A] voltage detection circuit 48 [that] is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line 36, and for driving the ready/busy signal to the 'busy' state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit 48 may be designed to generate a 'busy' signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. **The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected**. To inhibit rapid transitions between the 'ready' and 'busy' states, the **voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition**."

Id. at 3:30-43 (emphasis added). Thus, Hajeck shows that, at the time, a Skilled Artisan would have been able to design a voltage detection circuit that detects

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multiple types of anomalies, including when the voltage exceeds a certain level, and that provides hysteresis and holds its output for a period of time after a state transition. In light of Hajeck's and Amidi's teachings, a Skilled Artisan would have understood that Amidi's voltage supervisory block would be modified to detect voltage anomalies and switch to the backup power not only "[i]f system supply 605 has a magnitude lower than reference voltage 675" as disclosed by Amidi (Ex. 1024 at 4:44-53), but also "when the voltage exceeds a certain level" as taught by Hajeck (Ex. 1038 at 3:30-40). Indeed, as discussed above, the problems caused by such overvoltage conditions, and solutions to detect and protect against them, were well known at the time. Accordingly, a Skilled Artisan would have understood that, to avoid these well-known problems, Hajeck's "conventional voltage detection circuit" teachings on detecting both under- and over-voltage conditions were readily available at the time. Ex. 1038 at 3:30-40.

355. Accordingly, the prior art references in each of Grounds 2 and 3 also satisfies "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage*."

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c) [6.c] Wherein the Memory Module Transitions from a First Operable State to a Second Operable State

356. Claim 6 requires "*wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal*."

357. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

358. For the reasons discussed above with reference to claim limitation [4.c], the prior art references in each of Grounds 2 and 3 satisfy this limitation. *Supra* ¶¶315-321.

359. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy "*wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal*."

7. Claim 7 is Unpatentable

360. Claim 7 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [7.a] Preamble

361. The preamble of claim 7 requires "*[t]he memory module of claim 6, further comprising*."

362. As explained above for claim 6, the prior art references in each of Grounds 2 and 3 satisfy the limitations of claim 6. *Supra* ¶¶342-359.

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363. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy "[t]he memory module of claim 6, further comprising."

b) [7.b] Controller Coupled to the Voltage Monitor Circuit

364. Claim 7 requires "*a controller coupled to the voltage monitor circuit*."

365. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

366. For the reasons discussed above with reference to claim limitation [5.b], the prior art references in each of Grounds 2 and 3 discloses and renders obvious "*a controller coupled to the voltage monitor circuit*" to a Skilled Artisan. *Supra* ¶¶326-333.

367. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy the "*a controller coupled to the voltage monitor circuit*" limitation.

c) [7.c] Wherein the Controller is Configured to Perform One or More Operations

368. Claim 7 requires "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*."

369. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

370. For the reasons discussed above with reference to claim limitation [5.c], the prior art references in each of Grounds 2 and 3 discloses and renders

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obvious "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*" to a Skilled Artisan. *Supra* ¶¶334-340.

371. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy the "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*" limitation.

8. Claim 8 is Unpatentable

372. Claim 8 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [8.a] Preamble

373. The preamble of claim 8 requires "*[t]he memory module of claim 1, further comprising*."

374. As explained above for claim 1, to the extent the preamble is limiting, it is satisfied by Harris alone, or in combination with the FBDIMM Standards, which disclose a memory module. *Supra* ¶¶216-287; *see, e.g.*, Ex. 1023 (Harris) at Figs. 1A, 3. Similarly, Amidi discloses a memory module with voltage monitoring. Ex. 1024 (Amidi) at Figs. 4, 6, 15 (illustrating a memory module with voltage monitoring).

375. Accordingly, to the extent the preamble of claim 6 is limiting, the prior art references in each of Grounds 2 and 3 satisfies "*[t]he memory module of claim 1, further comprising*."

b) [8.b] A Controller, Including a Voltage Monitor Circuit, Coupled to the PCB

376. Claim 8 requires "*a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections*."

377. For the reasons discussed above with reference to claim limitations [4.b] and [5.b], the prior art references in each of Grounds 2 and 3 discloses and renders obvious "*a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections*" to a Skilled Artisan. *Supra* ¶¶306-314 (claim limitation [4.b]), ¶¶326-333 (claim limitation [5.b]).

378. In each of the combinations, Amidi teaches and discloses a "*voltage monitor circuit*" that implements power supervisory functionality, such as the power supervisory module 480, the voltage supervisory block 665, and the voltage supervisory block 800. As shown below in Figure 4 of Amidi, the power supervisory module 480 (annotated in red) is coupled to the PCB that has an edge connector (annotated in yellow).

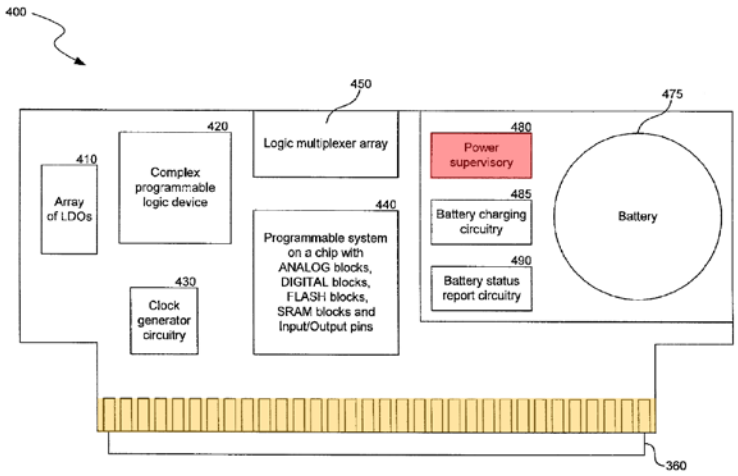


FIG. 4

Ex. 1024 at Fig. 4 (annotated); *see also id.* at Fig. 6 and 5:35-43 (describing voltage supervisory block 665), 8:23-62, Fig. 14 (illustrating a method that includes monitoring the input power supply at 1435, detecting a power fault at 1440, initiating a self-refresh state at 1450, and exiting the self-refresh state at 1460-1490), Fig. 15 and 9:8-12 (describing monitoring system, including monitoring input power supply for proper levels), Figs. 7-8, 5:31-62 (describing voltage supervisory block 800 and control of a power multiplexer). In the combination for claim 8, the power supervisory circuitry of Amidi is part of the "*controller*" and is "*coupled to the PCB*" of the memory module. In addition, the "*controller*" includes supervisory module 480, voltage supervisory block 665, and voltage supervisory block 800 ("*including a voltage monitor circuit*"). Further, as explained above for claim limitation [4.b], Amidi's voltage supervisory block is configured to monitor the external voltage source, such as one at 12 volts, that is

received from the second set of edge connections ("*voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections*"). *Supra* ¶¶306-314 (claim limitation [4.b]); *see also* Ex. 1023 at [0010], [0012], [0019], Fig. 1A; Ex. 1024 (Amidi) at Figs. 5, 6.

379. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies "*a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections*."

c) [8.c] Wherein the Voltage Monitor Circuit Transmits a Signal to Portion(s) of the Controller

380. Claim 8 requires "*wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller*."

381. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

382. For the reasons discussed above with reference to claim limitations [4.c] and [5.c], the prior art references in each of Grounds 2 and 3 discloses and renders obvious "*wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or*

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more portions of the controller" to a Skilled Artisan. *Supra* ¶¶315-321 (claim limitation [4.c]), ¶¶334-340 (claim limitation [5.c]).

383. For example, Amidi teaches that its voltage supervisory block (part of the "*voltage monitor circuit*") "compares a system voltage with a reference voltage" and "generates output signals with various logic components to control other parts of the power supply circuitry." Ex. 1024 at 5:31-34; *see also id.* at 4:44-52, Figs. 6-8. Thus, Amidi teaches and discloses "*the voltage monitor circuit detecting a power threshold condition*" to a Skilled Artisan.

384. In response to the generated output signals, Amidi teaches that the power management functionality on the memory module (a "*portion[] of the controller*") switches from the system supply to a battery backup supply (e.g., voltage supervisory block 665 generates a signal to switch the power multiplexer 665 from the system supply to a battery backup supply) and the logic functionality on the memory module (another "*portion[] of the controller*") initiates and maintains the data (e.g. self-refresh) in the DRAM (e.g., a finite state machine signal, such as signal 875 in Amidi, initiates self-refresh). *See supra* ¶¶315-321; Ex. 1024 at 7:24-34, 9:8-22, Figs. 6, 8, 12, 15. As explained above for claim limitation [5.b], a Skilled Artisan would have been motivated to implement Amidi's logic functionality using the S3 sleep mode functionality of the Buffer 112 to place the DRAM in self-refresh (also a "*portion[] of the controller*"), as taught

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and disclosed by Harris to a Skilled Artisan. *See supra* ¶¶326-333. Thus, the combination teaches and discloses to a Skilled Artisan that the voltage supervisory block transmits output signals to the power management functionality and logic functionality to switch to battery backup and to initiate self-refresh of the memory ("*the voltage monitor circuit transmits a signal to one or more portions of the controller*").

385. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy "*wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller*."

9. Claim 9 is Unpatentable

386. Claim 9 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [9.a] Wherein the Voltage Monitor Circuit Detects an Amplitude of the Input Voltage Being Above a First Predetermined Threshold Voltage

387. Claim 9 requires "*[t]he memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage*."

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388. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

389. For the reasons discussed above with reference to claim limitations [4.b], [6.b], and [8.c], the prior art references in each of Grounds 2 and 3 discloses and renders obvious "*wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage*" to a Skilled Artisan. *Supra* ¶¶306-314 (claim limitation [4.b]), ¶¶345-355 (claim limitation [6.b]), ¶¶380-385 (claim limitation [8.c]). For Ground 2, a Skilled Artisan would have been motivated to modify Amidi's voltage supervisory block (e.g., voltage supervisory block 665) to generate a signal ("*trigger signal*") such that the battery backup is selected if the system supply voltage is less than 85% of the nominal value, such as 10.2 volts for a 12-volt supply, (*see* "*the input voltage having a voltage amplitude below a predetermined threshold voltage*" of claim 4 above) or if it is greater than 115% of the nominal value, such as 13.8 volts for a 12-volt supply ("*the input voltage having a voltage amplitude above a predetermined threshold voltage*" of claim 6 above). For Ground 3, a Skilled Artisan would have understood that Amidi's voltage supervisory block would be modified to detect voltage anomalies and switch to the backup power not only "[i]f system supply 605 has a magnitude lower than reference voltage 675" as disclosed by Amidi

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(Ex. 1024 at 4:44-53), but also "when the voltage exceeds a certain level" as taught by Hajeck (Ex. 1038 at 3:30-40). *See supra* ¶355.

390. According, the prior art references in each of Grounds 2 and 3 satisfy the "*wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage*" limitation.

b) [9.b] Wherein the First Predetermined Threshold Voltage is Above a Specified Operating Voltage

391. Claim 9 requires "*wherein the first predetermined threshold voltage is above a specified operating voltage*."

392. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

393. For the reasons discussed above with reference to claim limitations [4.b] and [6.b], the prior art references in each of Grounds 2 and 3 disclose and renders obvious that the "*first predetermined threshold voltage*" corresponds to a tolerance above the nominal external voltage, which the module can safely handle during operation ("*a specified operating voltage*"). *Supra* ¶¶306-314 (claim limitation [4.b]), ¶¶345-355 (claim limitation [6.b]). For Grounds 2 and 3, the nominal external voltage is 12V, as taught by Harris. *See, e.g.*, Ex. 1023 at [0012]. Harris teaches that the module can safely handle a tolerance of 15%. *See id.* at [0013]. And, Amidi teaches that the module can safely handle a tolerance of 5% or

10%. *See* Ex. 1024 at Figs. 6, 14, 8:23-36; *see also* Ex. 1063 at 1-2 (around a 10% tolerance); Ex. 1027 (JESD82-20, part of FBDIMM Standards) at p.32 (same).

394. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy the "*wherein the first predetermined threshold voltage is above a specified operating voltage*" limitation.

10. Claim 10 is Unpatentable

395. Claim 10 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

396. Claim 10 requires "*[t]he memory module of claim 9, wherein the first predetermined threshold voltage is ten percent above the specified operating voltage*."

397. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

398. As discussed above with reference to claim limitations [4.b] and [6.b] and claim 9, the combinations including Harris and Amidi teaches and discloses that the "*first predetermined threshold voltage*" is 15 percent above a nominal value of the system supply voltage (e.g., 12V) ("*specified operating voltage*"). *Supra* ¶¶306-314 (claim limitation [4.b]), ¶¶345-355 (claim limitation [6.b]), ¶¶386-394 (claim 9).

399. In addition, a 5 percent tolerance was also obvious to a Skilled Artisan at the time. For example, Amidi discloses a 5 percent tolerance in the specific implementation shown in its Figure 6. *See* Ex. 1024 (Amidi) at Fig. 6 ("VREF=1.71V (%5 of 1.8V SUPPLY"). Similarly, JEDEC's DDR2 SDRAM Specification, JESD79-2B, discloses a tolerance of approximately 5 percent. Ex. 1026 at pp.6-7 ("1.8V +/- 0.1V").

400. A Skilled Artisan would have understood that any values between 5 and 15 percent were equally obvious and accounted for nothing more than an obvious design choice. For example in Harris, the external voltage (12V) is stepped down by voltage regulators to the voltages used by the parts in the module, including the memory devices. Thus, a Skilled Artisan would have understood that the tolerance on the input voltage (+/-15%, Ex. 1023 at [0013]) can be larger than the tolerance of the memory devices (5%, e.g., Ex. 1026 at pp.6-7). Therefore, a Skilled Artisan would have understood and been motivated to select a tolerance between 5% and 15% for the module. A Skilled Artisan would have also understood that allowing too high a tolerance carries the risk of losing data or damaging the devices on the memory module because the module cannot "tolerate" the voltage change. Ex. 1023 at [0013] (explaining the "tolerance" Harris's module can handle). A Skilled Artisan would have also understood that setting too low a tolerance carries the risk of unnecessary interruptions of operation powered by the

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system supply, because the module could "tolerate" the temporary change of the power. *Id.* In particular, a Skilled Artisan would have understood that the choice of around a 10 percent tolerance provided a reasonable compromise between the risks associated with too high a tolerance and too low a tolerance. For example, a National Semiconductor datasheet for LMC6953 describes a tolerance for over-voltage and under-voltage protection of approximately 10 percent. Ex. 1063 at 1-2 (describing an Over-Voltage Threshold of about 5.6V and an Under-Voltage Threshold of about 4.4V for a +5V power supply, excerpted and annotated below).

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

401. As another example of the choice of around a 10 percent tolerance providing a reasonable compromise between the risks associated with too high a tolerance and too low a tolerance, Amidi discloses an implementation for monitoring a power rail of 3.3V and comparing it to a 3.0V reference voltage,

corresponding to a "*below a predetermined threshold voltage*" of claim [4.b] of about 10 percent below the power rail's nominal voltage. *See* Ex. 1024 at Fig. 14 (reproduced below, annotated), 8:23-36; *see also* Ex. 1027 at 32 (stating VDDSPD has a typical voltage of 3.3 volts with a minimum voltage 10 percent below the typical voltage, or 3.0 volts, and a maximum voltage 10 percent above the typical voltage, or 3.6 volts).

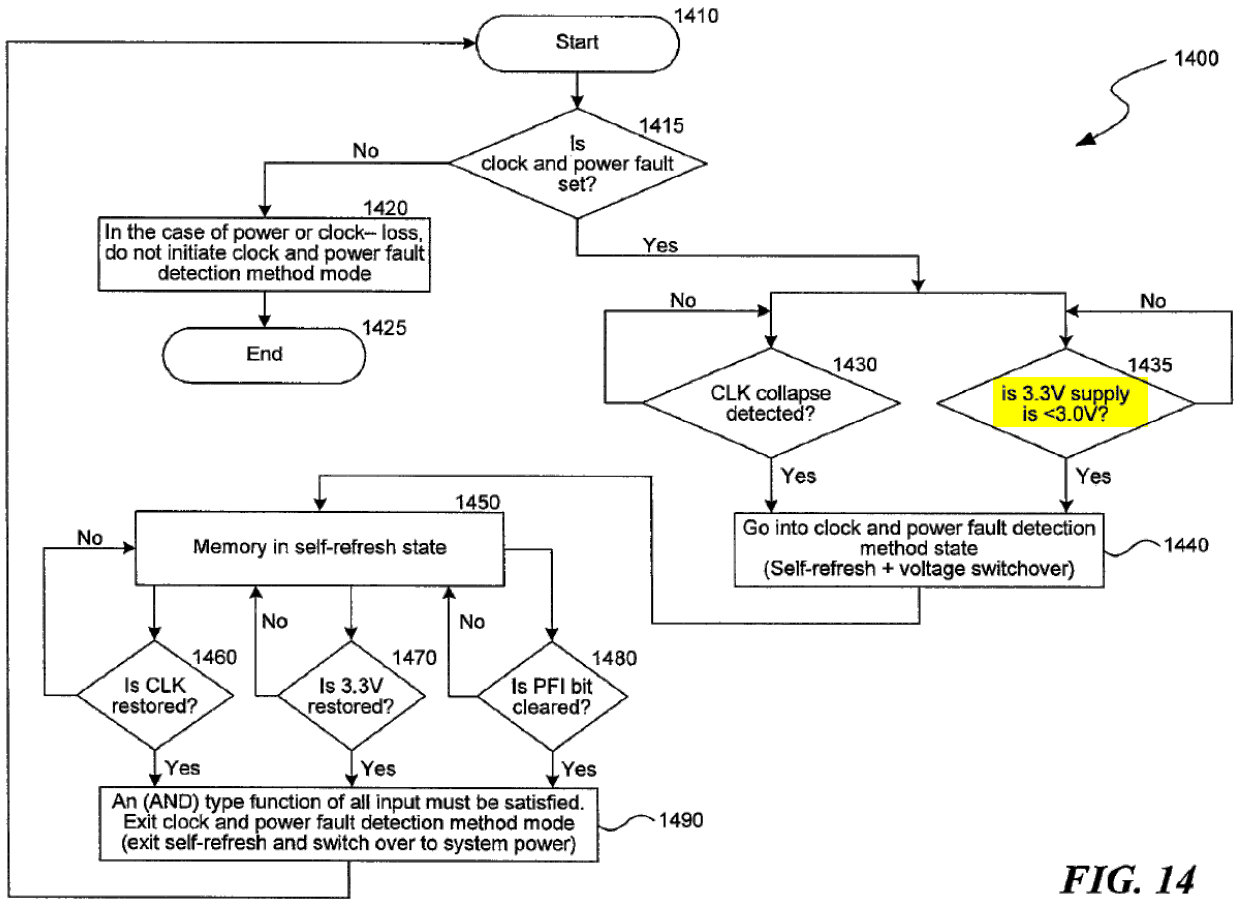


FIG. 14

Therefore, a Skilled Artisan would have understood that "*wherein the first predetermined threshold voltage is ten percent above the specified operating voltage*" was obvious in view of the prior art references in Grounds 2 and 3.

402. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein the first predetermined threshold voltage is ten percent above the specified operating voltage*" limitation.

11. Claim 11 is Unpatentable

403. Claim 11 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [11.a] Wherein the Voltage Monitor Circuit Detects an Amplitude of the Input Voltage Being Below a Second Predetermined Threshold Voltage

404. Claim 11 requires "*[t]he memory module of claim 9, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage*."

405. For the reasons discussed above with reference to claim limitations [4.b], [6.b], [8.c], [9.a], the prior art references in each of Grounds 2 and 3 discloses and renders obvious "*wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage*" to a Skilled Artisan. *Supra* ¶¶306-314 (claim limitation [4.b]), ¶¶345-355 (claim limitation [6.b]), ¶¶380-385 (claim limitation [8.c]), ¶¶387-390 (claim limitation [9.a]). For Ground 2, a Skilled Artisan would have been motivated to

modify Amidi's voltage supervisory block (e.g., voltage supervisory block 665) to generate a signal ("*trigger signal*") such that the battery backup is selected if the system supply voltage is less than 85% of the nominal value, such as 10.2 volts for a 12-volt supply, ("*an amplitude of the input voltage being below a second predetermined threshold voltage*") or if it is greater than 115% of the nominal value, such as 13.8 volts for a 12-volt supply ("*an amplitude of the input voltage being above a first predetermined threshold voltage*" of claim 9 above). For Ground 3, a Skilled Artisan would have understood that Amidi's voltage supervisory block would be modified to detect voltage anomalies and switch to the backup power not only "[i]f system supply 605 has a magnitude lower than reference voltage 675" as disclosed by Amidi (Ex. 1024 at 4:44-53), but also "when the voltage exceeds a certain level" as taught by Hajeck (Ex. 1038 at 3:30-40). *See supra* ¶355.

406. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy the "*wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage*" limitation.

b) [11.b] Wherein the Second Predetermined Threshold Voltage is Below the Specified Operating Voltage

407. Claim 11 requires "*wherein the second predetermined threshold voltage is below the specified operating voltage*."

408. For the reasons discussed above with reference to claim limitations [4.b], [6.b], [8.c], [9.b], the prior art references in each of Grounds 2 and 3 discloses and renders obvious "*wherein the second predetermined threshold voltage is below the specified operating voltage*" to a Skilled Artisan. *Supra* ¶¶306-314 (claim limitation [4.b]), ¶¶345-355 (claim limitation [6.b]), ¶¶380-385 (claim limitation [8.c]), ¶¶391-394 (claim limitation [9.b]).

409. For the reasons discussed above with reference to claim limitations [4.b] and [6.b], the prior art references in each of Grounds 2 and 3 disclose and renders obvious that the "*first predetermined threshold voltage*" corresponds to a tolerance above the nominal external voltage ("*the specified operating voltage*"), in which the module can safely handle such a tolerance during operation. *Supra* ¶¶306-314 (claim limitation [4.b]), ¶¶345-355 (claim limitation [6.b]). Similarly, the disclose and render obvious that the "*second predetermined threshold voltage*" corresponds to a tolerance below the nominal external voltage ("*the specified operating voltage*"), in which the module can safely handle such a tolerance during operation. *See id.* For Grounds 2 and 3, the nominal external voltage is 12V, as taught by Harris. *See, e.g.*, Ex. 1023 at [0012]. Harris teaches that the module can safely handle a tolerance of 15%. *See id.* at [0013]. And, Amidi teaches that the module can safely handle a tolerance of 5% or 10%. *See* Ex. 1024 at Figs. 6, 14,

8:23-36; *see also* Ex. 1063 at 1-2 (around a 10% tolerance); Ex. 1027 (JESD82-20, part of FBDIMM Standards) at p.32 (same).

410. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy the "*wherein the second predetermined threshold voltage is below the specified operating voltage*" limitation.

c) [11.c] Wherein the Memory Module Transitions from a First Operable State to a Second Operable State

411. Claim 11 requires "*wherein the memory module transitions from a first operable state to a second operable state in response to the signal*."

412. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

413. For the reasons discussed above with reference to claim limitation [4.c], the prior art references in each of Grounds 2 and 3 satisfy this limitation. *Supra* ¶¶315-321.

414. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy the "*wherein the memory module transitions from a first operable state to a second operable state in response to the signal*" limitation.

12. Claim 12 is Unpatentable

415. Claim 12 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

416. Claim 12 requires "*[t]he memory module of claim 11, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage*."

417. As discussed for claim 10, the prior art references in each of Grounds 2 and 3 satisfy the "*wherein the first predetermined threshold voltage is ten percent above the specified operating voltage*" limitation. *Supra* ¶¶395-402. For the same reasons why the "*first predetermined threshold voltage*" is "*ten percent above the specified operating voltage*," the same combinations render obvious that "*the second predetermined threshold voltage is ten percent below the specified operating voltage*."

418. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy "*[t]he memory module of claim 11, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage*."

13. Claim 13 is Unpatentable

419. Claim 13 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

420. Claim 13 requires "*[t]he memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage*."

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421. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

422. For the reasons discussed above with reference to claim limitation [4.b], the prior art references in each of Grounds 2 and 3 satisfy this limitation. *Supra* ¶¶306-314.

423. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy the "*wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage*" limitation.

14. Claim 14 is Unpatentable

424. Claim 14 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

425. Claim 14 requires "*[t]he memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system*."

426. Harris in view of the JEDEC FBDIMM standards and Amidi discloses and renders obvious this limitation to a Skilled Artisan. As discussed above with reference to claim limitations [4.b], [5.b], and [8.b], Amidi teaches a "*voltage monitoring circuit*" that includes a voltage supervisory block (665), to monitor an input voltage of the system supply (605) and controlling a signal (670) which

selects the system supply or the battery backup power. Ex. 1024 at Fig. 6, 4:44-55; *see supra* ¶¶306-314 (claim limitation [4.b]), ¶¶326-333 (claim limitation [5.b]), ¶¶376-379 (claim limitation [8.b]). Amidi also discloses a process for monitoring power for a memory module. Ex. 1024 at 8:62-66, Fig. 15 (reproduced below).

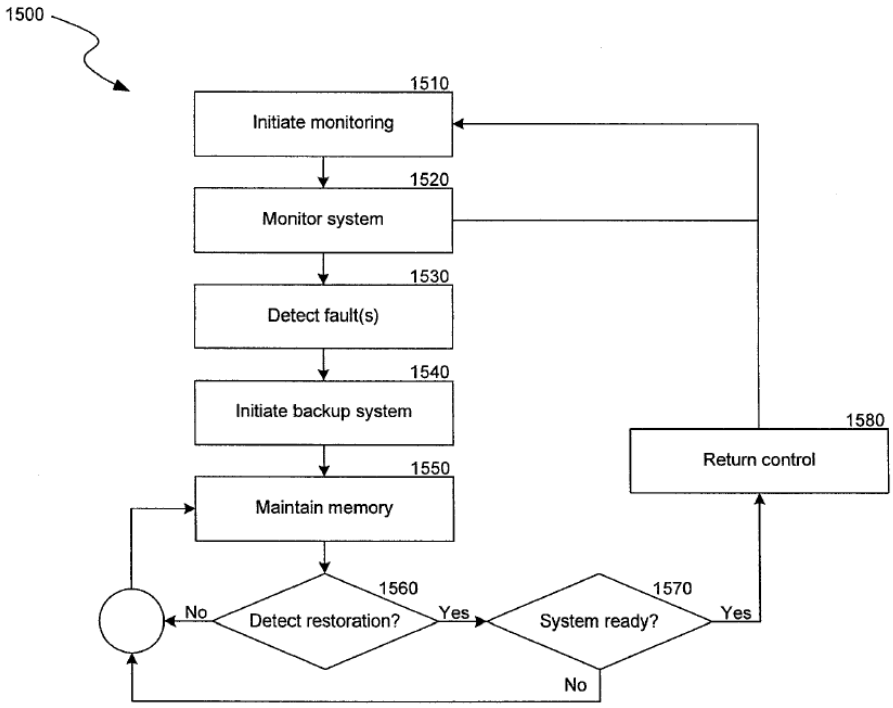


FIG. 15

427. Amidi explains that the process includes detecting a fault in the power signal and initiating the backup system on the module, which takes over supplying the clock and power signals. *Id*. at Fig. 15 (steps 1530, 1540), 9:11-22. Amidi further explains that, after the power is restored, the voltage monitor circuit detects a request by the host system to return control to the host system. *Id.* at Fig. 15 (step

1570, "System ready?"), 9:23-39 ("…determines at module 1570 whether the system has signaled that it is ready to handle power and clock signaling").

428. In particular, Amidi discloses that the voltage monitoring circuit detects whether the power is restored. *Id.* at Fig. 15 (step 1560), 9:23-25 ("A determination is then made as to whether a restored signal is detected for the clock and power signals at module 1560."). The voltage monitoring circuit also detects whether the system has requested, by clearing a bit indicating backup mode, that the module should return control to the host system. *Id.* at Fig. 15 (step 1570), 9:27-33 ("… the process then determines at module 1570 whether the system has signaled that it is ready to handle power and clock signaling. One signal that may be used is clearing the asserted bit of the memory module which was asserted to indicate backup mode at module 1540. Thus, the bit may be asserted for backup mode by the module and cleared for restoration by the system."). If the host system cleared the backup-mode bit, control of the module is returned to the host system to handle the power and clock signals. *Id.* at Fig. 15 (step 1580), 9:36-39 ("If the system has signaled that it is ready to handle power and clock signals, then control is returned to the system at module 1580..."); *see also id.* at Fig. 14 (step 1480), 8:30-62.

429. A Skilled Artisan would have understood from this disclosure in Amidi that, if the power is restored after a failure, Amidi's voltage monitor circuit

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(including voltage supervisory block 800) detects "*a request by the host system*" when it detects whether the host system has cleared the backup-mode bit (step 1570, "System ready?"). If the host system cleared that bit, the voltage monitor circuit returns the control of the module to the host, including handling of the power signal, as requested by the host. *See* Fig. 8, 5:31-62, Fig. 14 (step 1480 "checks whether a bit has been cleared indicating the system is ready to take back control of the memory module"), 8:30-62; *supra* ¶¶311-312.

430. Accordingly, the prior art references in each of Grounds 2 and 3 satisfy "*the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system*" limitation.

15. Claim 15 is Unpatentable

431. Claim 15 is unpatentable as the prior art references in each of Ground 1 (Voltage Mappings A, B, and C) and Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

432. Claim 15 requires "*[t]he memory module of claim 1, wherein two of the at least three buck converters are configured to operate as a dual-buck converter*."

433. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

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434. The 054 Patent illustrates a "*dual buck converter*" as simply having two outputted voltages:

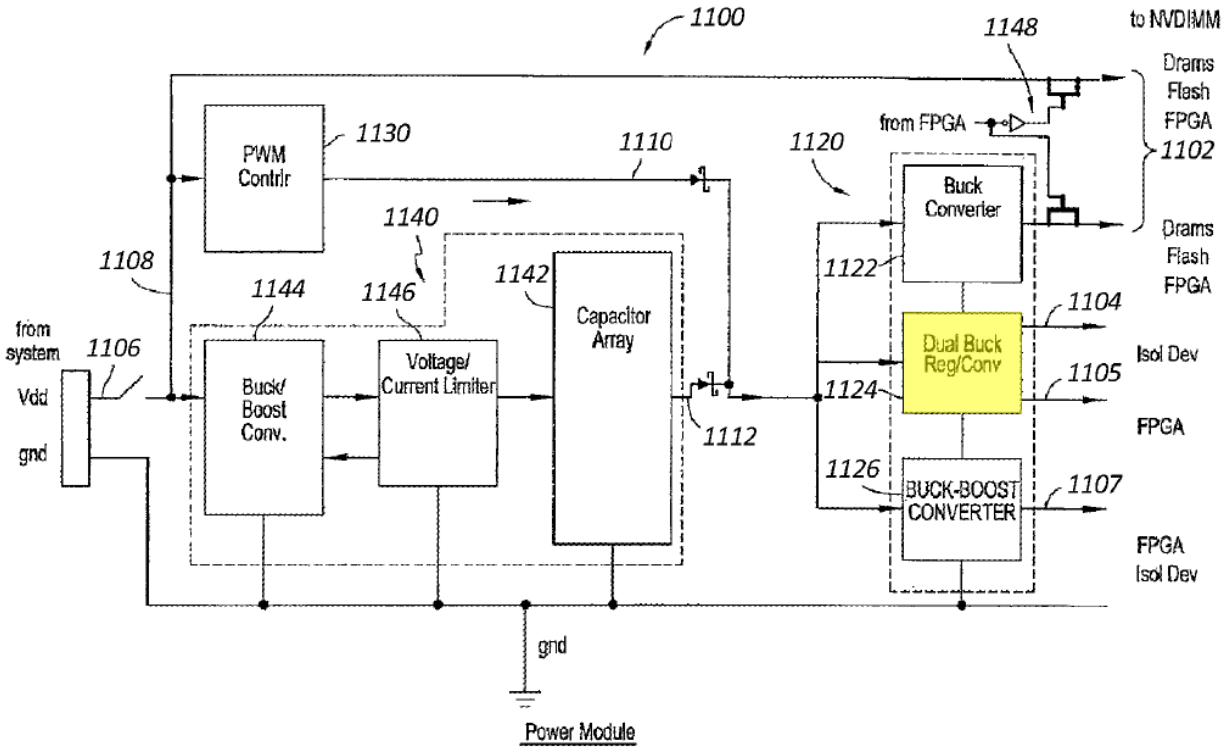


FIG. 16

Ex. 1001, at 29:28-29 ("sub-block 1124 comprises a dual buck converter"), Fig. 16 (annotated above, "Dual Buck Reg/Conv" 1124).

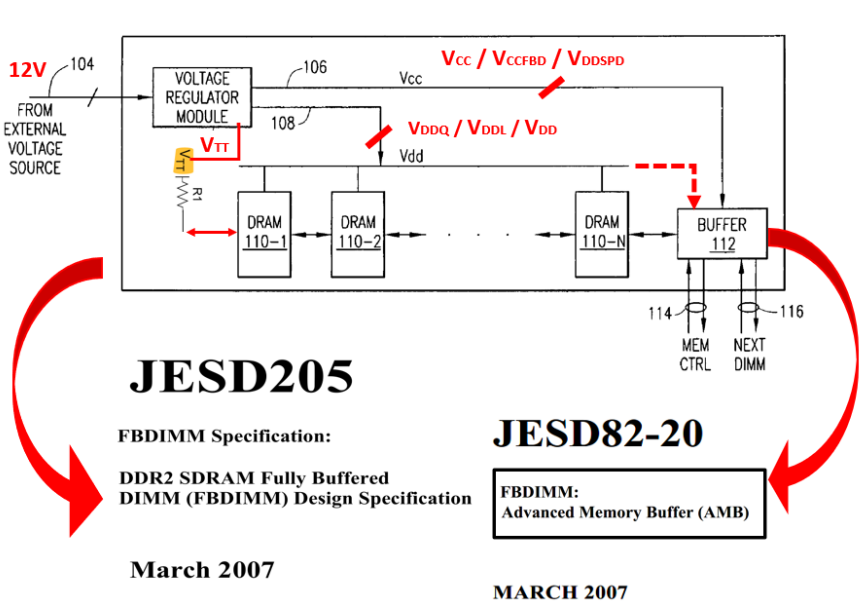
435. It would have been obvious, in view of the prior art references in each of Grounds 1 through 3, and the knowledge of a Skilled Artisan, to implement two of the at least three buck converters as a dual buck converter.

436. As explained above for claim limitation [1.c], the prior-art references in each of Grounds 1-3 satisfies "…*wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated*

voltage of the at least three regulated voltages." *Supra* ¶¶233-260. The voltage mappings are the same between Grounds 1, 2, and 3. *Supra* ¶¶242-245. As explained, the on-board voltage regulator module includes a first one of the "*three buck converters*" that provides, for example, any one of VDD or VDDQ as the first "*regulated voltage*" to the Buffer (112 above) and memory devices, such as DDR2 SDRAM. *Supra* ¶¶246-250. It also includes a second one of the "*three buck converters*" that provides, for example, any one of VCC or VCCFBD as the second "*regulated voltage*" to the Buffer (112 above). *Supra* ¶¶251-256. It also includes the third one of the "*three buck converters*" that provides, for example, any one of VDDL, VCCFBD, or VTT as the third "*regulated voltage*" to the memory devices, Buffer, and/or resistors. *Supra* ¶¶246-260.

437. For Ground 1 (Harris in view of the FBDIMM Standards), I discussed three mappings for the "*regulated voltages*," as shown in the figure below.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V

Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V

Ex. 1023 at Fig. 1A (annotated). For Ground 1, the first voltage is VDD or VDDQ, the second voltage is VCC or VCCFBD, and the third voltage is VDDL, VCCFBD, or VTT. The voltage mappings for Ground 2 (Ground 1 in view of Amidi) and Ground 3 (Ground 2 in view of Hajeck) are the same as those for Ground 1, as shown, for example, in the figure below for Ground 2.

Ground 2: Ground 1 and Battery Backup of Amidi

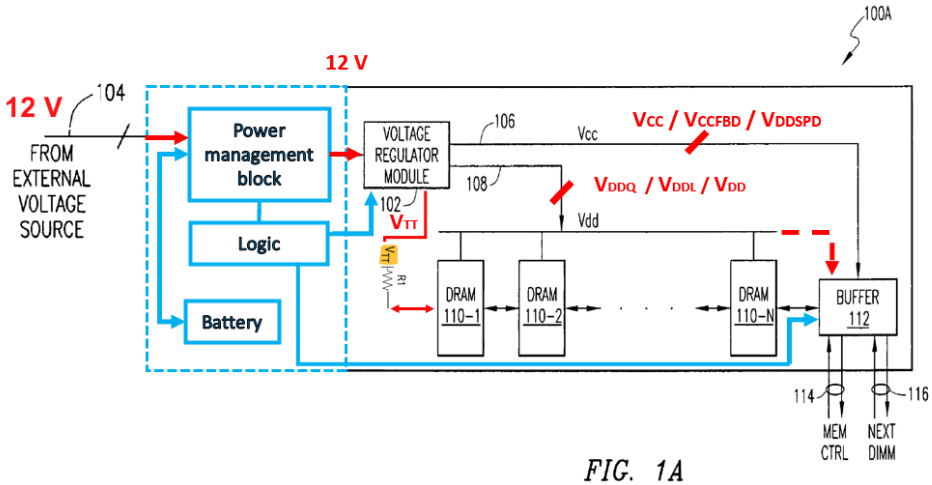


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V

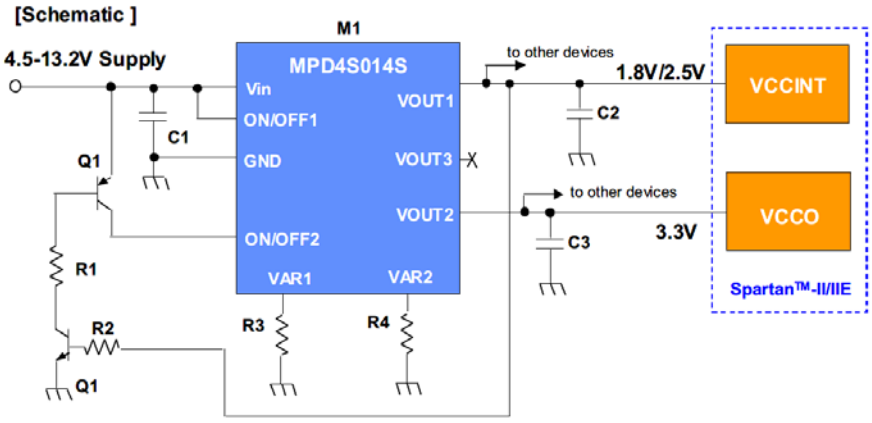
Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V

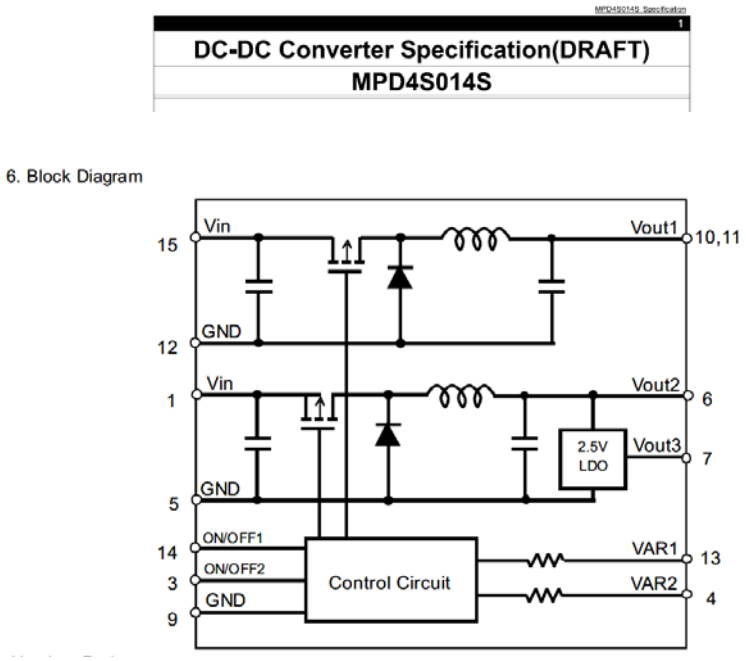
438. Additionally, as discussed for claim limitation [1.c], under Patent Owner's interpretation that two of the three buck converters can provide the same voltage amplitude, two buck converters can provide the same amplitude and be implemented as a dual buck converter. *Supra* ¶168-169, 242-244; Ex. 1073 at 59-61. For example, as shown above in the annotated figure for Grounds 1, 2, and 3, under Voltage Mapping A, a Skilled Artisan would have recognized that the VDD/VDDQ voltage supply (the first "*regulated voltage*") and VDDL voltage supply (the third "*regulated voltage*") each have a voltage amplitude of 1.8 volts. Ex. 1023 at Fig. 1A (annotated above); Ex. 1024 at 6-7 (annotated above).

439. For each of the grounds and voltage mappings, a Skilled Artisan would have been motivated to use a "*dual buck converter*" to implement any two of the "*three buck converters*" to provide any two of the "*three regulated voltages*" because the two converters in a dual buck converter can be operated independently to provide different required voltages, and using a dual buck converter would use fewer integrated circuits, pins, and interconnections on the module, therefore simplifying its design as described below. Further, a Skilled Artisan would have recognized that such "*dual buck converters*" were designed, and readily available on the market at the time, for the functionality required by memory devices or modules.

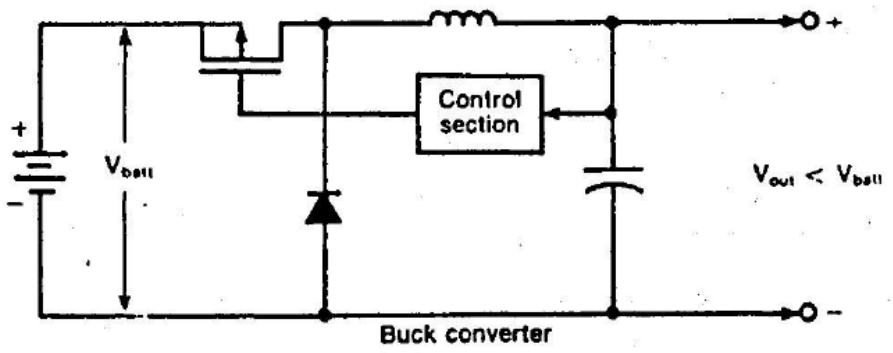
440. For example, Murata offered a MPD4S014S dual buck converter with two different output voltages (e.g., 1.8V and 3.3V):



Ex. 1042 at 16. The block diagram for the MPDS014S is shown below:



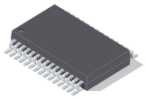
Ex. 1048 at 1-2. A Skilled Artisan would recognize from the block diagram above that there are two buck converters, as confirmed by the following figure from the Lenk textbook:



Ex. 1058 at 5. Thus, as shown above, the Murata MPD4S014S is a "*dual buck converter*" similar to Figure 16 of the 054 Patent because it outputs two regulated voltages from two buck converters.

441. As another example, Texas Instruments offered a TPS51020 dual buck voltage converter for DDR or DDR2.

TEXAS INSTRUMENTS



TPS51020

SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

Ex. 1040 at 1. The TPS51020 was used, for example, to implement a dual buck converter for the VDDQ and VTT voltage supplies (similar to Ground 1C). *See id.* at 11 ("TPS51020 gives a complete function set required for the DDR termination supply such as VDDQ/2 tracking V_{TT}").

442. As another example, Fairchild Semiconductor offered a FAN5026 Dual-Output PWM Controller:

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Applications

■ DDR V_{DDQ} and V_{TT} voltage generation

Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

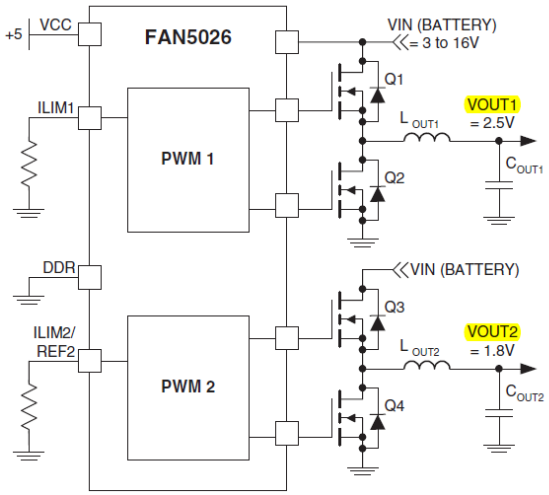


Figure 1. Dual Output Regulator

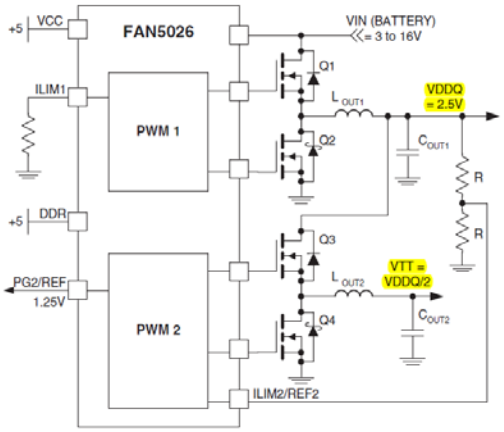


Figure 2. Typical Application

Ex. 1041 at 1 ("The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider."); *see also id.* at 2, 9. The two outputs could be implemented to provide two different voltages, such as VDDQ and VTT (similar to Ground 1C) or voltage supplies at 2.5 volts and 1.8 volts. *See, e.g., id.* at 2 (Figs. 1 and 2), 7-8 (Figs. 4 and 5).

443. As shown above, dual buck converters were common and commercially available. Furthermore, an additional benefit of dual buck converters, like those above, was that the phases of the two voltages could be adjusted relative to each other, thus reducing any input "ripple" and improving performance. *See*, *e.g.*, Ex. 1041 at 9 ("When used as a dual converter …, out-of-phase operation with 180 degree phase shift reduces input current ripple."); Ex. 1040 at 10 ("Two channels are operated in 180 degrees out-of-phase interleave switching mode. This interleaving helps reduce the input current ripple requirement for the input capacitor.").

444. As a further example, U.S. Patent No. 7,023187 to Shearon ("Shearon") discloses a "dual buck-mode PWM power supply" that outputs two voltage supplies, such as VDDQ and VTT (similar to Ground 1C), with phase shifting. *See* Ex. 1047 at 3:49-50 (brief description of Fig. 2), 4:37-56 (describing Vout1), 5:46-59 (describing Vout2), Fig. 2 (illustrating dual buck-mode converter with Vout1 and Vout2).

445. Accordingly, it would have been obvious, in view of the prior art references in each of Grounds 1 through 3, and the knowledge of a Skilled Artisan, to implement any two of the three buck converters as a dual buck converter.

446. I understand that Patent Owner has interpreted the claimed "*dual buck converter*" as reading on a *dual-phase* buck converter with a *single* output (such as

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VDD). *See* Ex. 1073 at 49-50, 58. The 054 Patent (and the related 918 Patent) neither shows nor describes a dual-phase buck converter with a single output as a "*dual buck converter*."

447. Under Patent Owner's interpretation of the "*dual buck converter*," Ex. 10741, at 41, 43, a dual-phase buck converter would have been obvious given that Harris specifically discloses that the appropriate local voltage levels are, for example, provided by a "***multi-phase*** synchronous Pulse-Width Modulated (PWM) controllers." Ex. 1023 at [0010] ("Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM 102 for purposes of the present patent disclosure. For instance, multi-phase synchronous Pulse-Width Modulated (PWM) controllers . . . .") *see also* Ex. 1032 at 161-64 (describing use of PWM controllers for buck converters). The "multiphase buck converter" circuits disclosed by Harris were known to provide several advantages, including "lower ripple," "higher current capability," and "smaller size." Ex. 1050 at 3:36-37, 2:19-20. Thus, in light of Harris's express teaching, it would have been obvious to use a dual-phase buck converter (for VDD, for example) to reduce ripples and decrease the size of the circuit, thus satisfying Patent Owner's apparent interpretation for "*dual buck converter*."

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448. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies the "*wherein two of the at least three buck converters are configured to operate as a dual-buck converter*" limitation.

16. Claim 16 is Unpatentable

449. Claim 16 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [16.a] Preamble

450. The preamble of claim 16 requires "*[a] memory module comprising*."

451. As shown in the table below, the preamble of Claim 16 is identical to the preamble Claim 1:

Claim 1	**Claim 16**
[1.a] A memory module comprising:	[16.a] A memory module comprising:

452. As discussed above with reference to claim element [1.a], to the extent the preamble of claim 1 is limiting, Harris alone, or in combination with the FBDIMM Standards, satisfies "[a] memory module." *See* ¶¶217-223.

b) [16.b] Printed Circuit Board

453. Claim 16 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system*."

454. As shown in the table below, claim element [16.b] is very similar to claim element [1.b]:

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Claim 1	**Claim 16**
[1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;	[16.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;

455. As discussed above with reference to claim 1, Harris alone, or in combination with the FBDIMM Standards, satisfies this limitation. *See* ¶¶ 224-232.

c) [16.c] Voltage Conversion Circuit

456. Claim 16 requires "*a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages*."

457. As shown in the table below, claim element [16.c] is very similar to claim element [1.c]:

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Claim 1	Claim 16
[1.c] a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;	[16.c] a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

458. As discussed above with reference to claim element [1.c], the prior art in each of Grounds 1 through 3 satisfies this limitation. *See* ¶¶233-260.

d) [16.d] A Plurality of Components Coupled to the PCB

(1) [16.d.1] Plurality of components each coupled to at least one regulated voltage

459. Claim 16 requires "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages*."

460. As shown in the table below, claim element [16.d.1] is very similar to claim element [1.d.1]:

Claim 1	Claim 16
[1.d.1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages,	[16.d.1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages,

461. As discussed above with reference to claim element [1.d.1], the prior art references in each of Grounds 1-3 satisfies this limitation. *See* ¶¶ 261-266.

(2) [16.d.2] Plurality of components includes SDRAM devices

462. Claim 16 requires "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices*."

463. As shown in the table below, claim element [16.d.2] is very similar to claim elements [1.d.2]:

Claim 1	**Claim 16**
[1.d.2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and	[16.d.2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices

464. As discussed above with reference to claim elements [1.d.2], the prior art references in each of Grounds 1-3 satisfies this limitation. *See* ¶¶ 267-271.

3) [16.d.3] The SDRAM devices are coupled to the first regulated voltage

465. Claim 16 requires "*the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages*."

466. As shown in the table below, claim element [16.d.3] is very similar to claim element [1.d.5]:

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Claim 1	**Claim 16**
[1.d.5] wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.	[16.d.3] the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages

467. As discussed above with reference to claim element [1.d.5], the prior art references in each of Grounds 1-3 satisfies this limitation. *See* ¶¶ 285-287.

e) [16.e] A Controller Coupled to the PCB

(1) [16.e.1] The Controller Includes a Voltage Monitor Circuit

468. Claim 16 require "*a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage*."

469. As shown in the table below, claim element [16.e.1] is very similar to claim limitations [1.b], [8.b], and [9.a]:

Claims 1, 8, 9	**Claim 16**
[8.b] a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections, [1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system; [9.a] The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage,	[16.e.1] a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage

470. As discussed above with reference to claim to claim limitations [1.b], [8.b], and [9.a], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶224-232 (claim limitation [1.b]), ¶¶376-379 (claim limitation [8.b]), ¶¶387-390 (claim limitation [9.a]).

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471. Furthermore, a Skilled Artisan would have understood that Amidi's voltage supervisory block (665) (part of the "*voltage monitor circuit*") is "*configured to detect an amplitude change in the input voltage,*" for example, when the external system supply changes by crossing the reference voltage.

(2) [16.e.2] Wherein the Memory Module Transitions from a First Operable State to a Second Operable State

472. Claim 16 requires "*wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state*."

473. As shown in the table below, claim element [16.e.2] is very similar to claim element [4.c]:

Claim 4	**Claim 16**
[4.c] wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.	[16.e.2] wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state

474. As discussed above with reference to claim element [4.c], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *See* ¶¶ 315-319.

17. Claim 17 is Unpatentable

475. Claim 17 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

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476. Claim 17 requires "*[t]he memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage*."

477. As shown in the table below, claim 17 is very similar to claim elements limitations [4.b] and [6.b]:

Claims 4, 6	**Claim 17**
[4.b] . . . the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, [6.b] . . . the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage,	[17] The memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage.

478. As discussed above with reference to claim elements [4.b] and [6.b], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *See* ¶¶306-314 (claim limitation [4.b]), ¶¶345-355 (claim limitation [6.b]).

18. Claim 18 is Unpatentable

479. Claim 18 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

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a) [18.a] Wherein, in the First Operable State, Voltage Conversion Circuit Provides First Regulated Voltage to SDRAM Devices Using First Pre-Regulated Voltage

480. Claim 18 requires "*[t]he memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage*." The "*first pre-regulated voltage*" is in addition to the "*input voltage*" from [16.e.2].

481. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

482. As discussed above with reference to claim element [4.c] and [16.e.2], the combination teaches a "*first operable state*" in which the memory module operates on the external voltage source when its amplitude is above a threshold and a "*second operable state*" in which the memory module operates on the battery backup when the external voltage source amplitude is below a threshold. *Supra* ¶¶315-319, 472-474.

483. As discussed above with reference to claim elements [16.d.3] and [1.d.5], the combination teaches that "*the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices*." *Supra* ¶¶465-467 (claim element [16.d.3]), ¶¶285-287 (claim element [1.d.5]). As explained, a Skilled Artisan would have understood that a "*first regulated voltage,*" mapped to VDD or VDDQ, is provided to the memory devices ("*plurality of SDRAM*

devices"). Ex. 1023 (Harris) at Fig. 1A. And, a Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with memory devices, such as DDR2 SDRAMs, couples those devices to multiple, separate voltage sources, called VDD, VDDQ, and VDDL. *See supra* ¶¶246-250 (VDD/VDDQ for Grounds 1, 2, and 3); *see also* Ex. 1023 at [0009]; Ex. 1028 at 9, 17-20; Ex. 1026 at p.2-3, 6-7, 9.

484. I understand that Patent Owner has indicated the "*pre-regulated voltage*" as recited in the claims of the related 918 Patent is satisfied by an input voltage which has pre-determined tolerances or limits. *See* Ex. 1073 at 49-50 (pointing to input voltage received from "Power edge connection"). Under such a claim interpretation, the combination also teaches "*the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage*." For example, Harris discloses such a "pre-regulated" input supply voltage which is at 12 volts with a 15% tolerance. Ex. 1023 at [0013]; *see also id.* [0014] ("It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltage.").

485. To the extent the "*pre-regulated voltage*" requires a voltage be "pre-regulated" on the memory board itself, *see* Ex. 1001 at 28:53-58, or one argues that a voltage within a fixed percentage of a typical value is not "pre-regulated," this

claim limitation still would have been obvious to a Skilled Artisan. For example in the Harris-Amidi combination, it would have been obvious to perform a "pre-regulation" in Amidi's power management block when adapting it to couple to Harris's voltage regulator module. Ex. 1024 (Amidi)at Fig. 5 (first below, annotated with teachings of Harris); Ex. 1023 at Fig. 1A (second below, annotated to illustrate the Harris-Amidi combination); *see also* Ex. 1024 at Fig. 6 (showing the backup battery voltage (e.g., 4.2V) being converted, thus pre-regulated, to the voltage level required at the output of the power management block (e.g., 12V)).

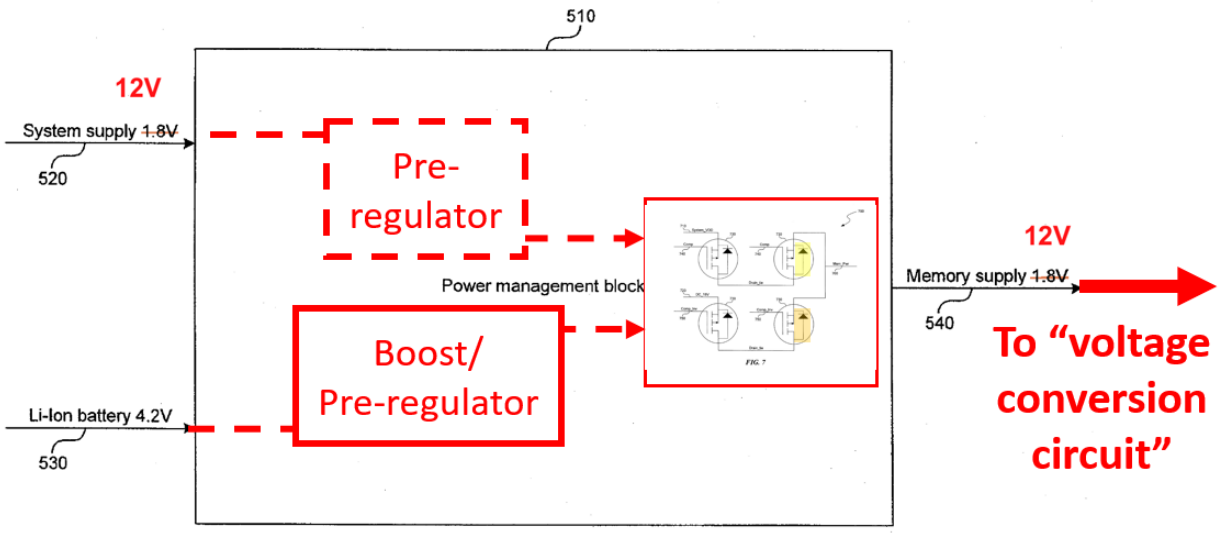


FIG. 5

Ground 2: Ground 1 and Battery Backup of Amidi

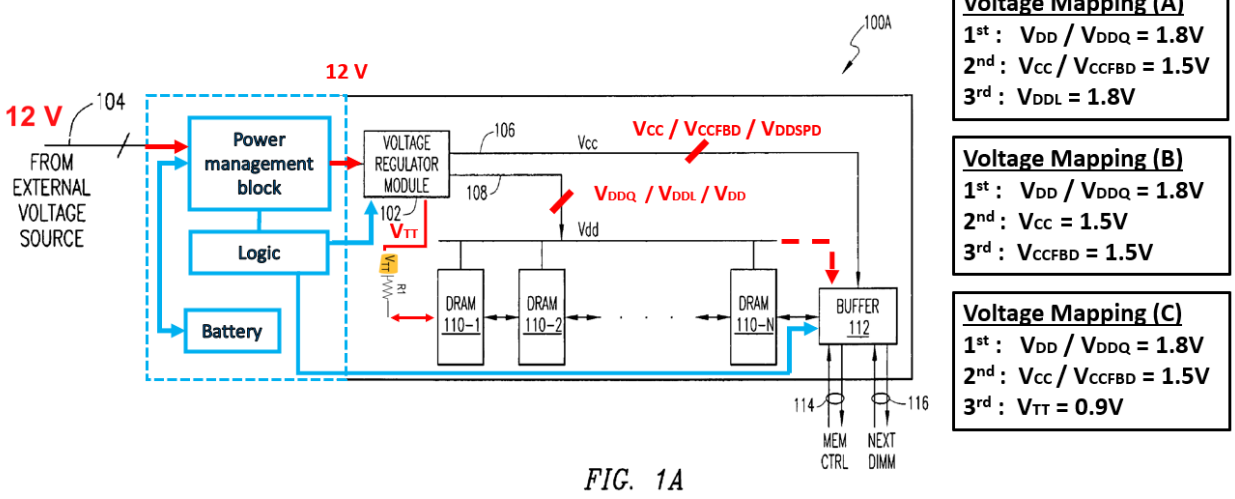


FIG. 1A

486. Indeed, a Skilled Artisan would have been motivated to include a power regulator in Amidi's Power management block to pre-regulate the input voltage of Harris's voltage regulator module if the external power source provides, or there is a chance it may provide, an unregulated input voltage, to ensure that the input of Harris's voltage regulator module remains within a tolerated interval around 12V. Ex. 1023 at [0013] ("tolerance (e.g., around +/−15%) can be accommodated"), [0014] ("It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages."). A Skilled Artisan would have also understood that such an additional voltage regulator in Amidi's power management block can be used to convert an input voltage other than 12V into 12V, thus allowing Harris's module to be adapted to a system which provides an input voltage other than 12V without altering other parts

of the module. Ex. 1023 (Harris) at [0020] ("voltage-independent embodiments disclosed herein can provide upgradeability and extensibility without changing system board power distribution"). A Skilled Artisan would have understood that such an additional voltage regulator can be a DC-DC switch-mode converter which provides a regulated voltage. Ex. 1032 (Mohan) at 161-162 (describing switch-mode converters as being used in "regulated switch-mode dc power supplies" where "the average dc output voltage must be controlled to equal a desired level").

487. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage*" limitation.

b) [18.b] Wherein, in the Second Operable State, Voltage Conversion Circuit Provides First Regulated Voltage to SDRAM Devices Using Second Pre-Regulated Voltage

488. Claim 18 further requires "*wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage*."

489. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

490. As discussed above with reference to claim element [4.c] and [16.e.2], the combination teaches a "*first operable state*" in which the memory module

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operates on the external voltage source when its amplitude is above a threshold and a "*second operable state*" in which the memory module operates on the battery backup when the external voltage source amplitude is below a threshold. *Supra* ¶¶315-319, 472-474.

491. In the "*second operable state*" that operates on the battery backup power, the combination discloses providing the VDD/VDDQ voltage supply to the SDRAM by converting the battery voltage (e.g., 4.2 volts) with a boost converter that steps-up the battery voltage to the 12-volt level ("*a second pre-regulated voltage*") to be input to Harris's Voltage Regulator Module. *Supra* ¶¶173-176; Ex. 1024 (Amidi) at 2:6-26, 4:14-60, Figs. 5-6, 15. A Skilled Artisan would have understood that such a boost converter provides a regulated voltage. Ex. 1032 (Mohan) at 161-162 (describing boost converters as being used in "regulated switch-mode dc power supplies" where "the average dc output voltage must be controlled to equal a desired level").

Ground 2: Ground 1 and Battery Backup of Amidi

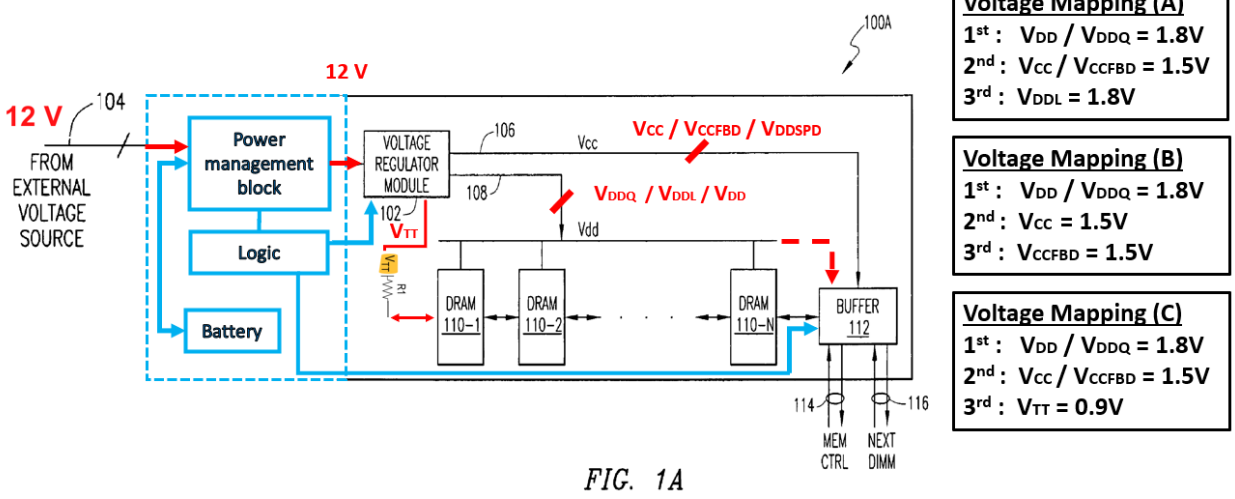


FIG. 1A

492. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage*" limitation.

19. Claim 19 is Unpatentable

493. Claim 19 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [19.a] Wherein, in the First Operable State, the First Pre-Regulated Voltage is Supplied to the Voltage Conversion Circuit Via a Circuit

494. Claim 19 requires "*[t]he memory module of claim 18, wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit*."

495. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

496. Amidi's Figure 7 discloses "*a circuit*," which is a power switch multiplexer for use in Amidi's power management block shown in Figure 5. *See* Ex. 1024 at 4:23-29, 4:56-63, Figs. 5, 7. As discussed for claim 18, in the "*first operable state*" that operates on the system power supply at 12 volts, a "*first pre-regulated voltage*" (710) from the system power supply is provided to the on-board voltage regulator module of Harris ("*voltage conversion circuit*") via circuitry that includes Amidi's power switch multiplexer (Fig. 7) ("*a circuit*") in the power management block (Fig. 5) of Amidi that is adapted to operate with a 12-volt external voltage source in the combination. *Supra* ¶¶479-492; *see, e.g.*, Ex. 1024 (Amidi) at Figs. 5 and 7 (reproduced below, annotated), *see also id*. at Fig. 6 (power management block details).

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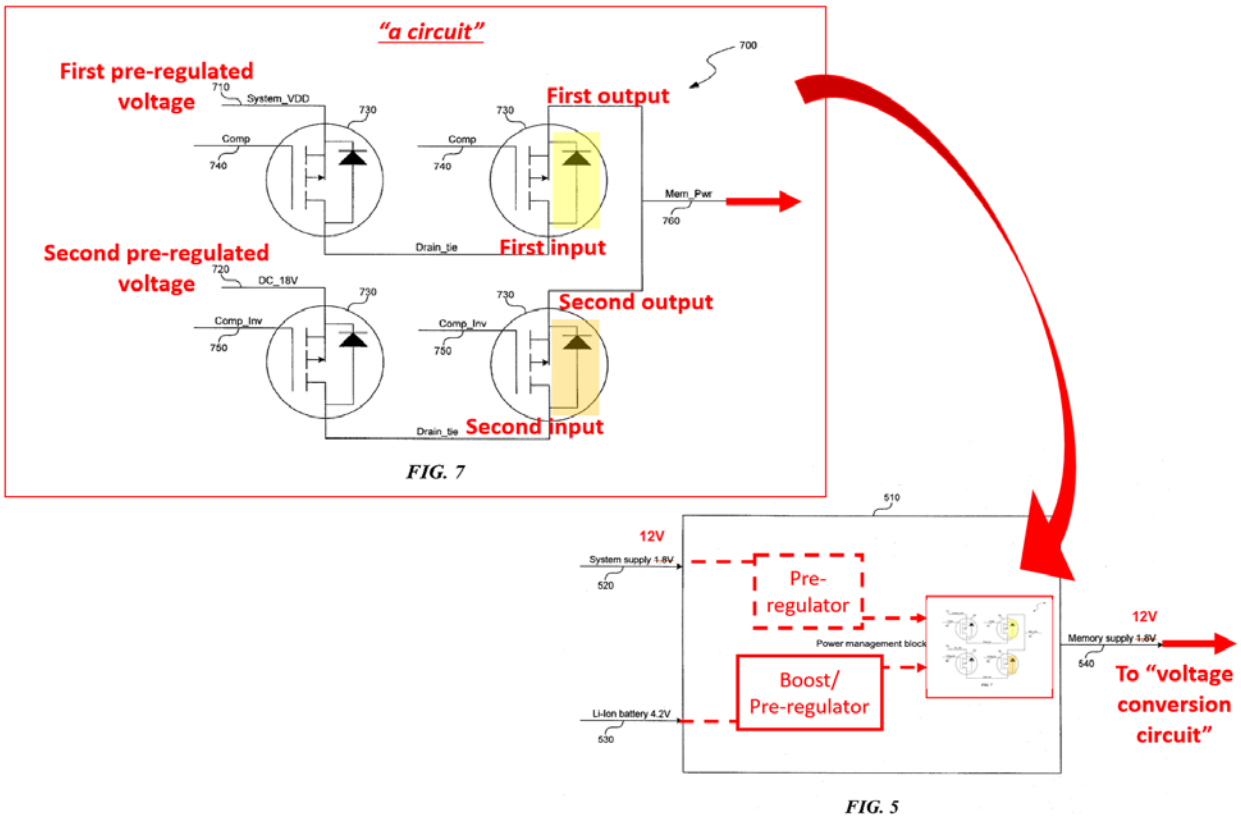


FIG. 7

FIG. 5

497. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit*" limitation.

b) [19.b] Wherein, in the Second Operable State, the Second Pre-Regulated Voltage is Supplied to the Voltage Conversion Circuit via the Circuit

498. Claim 19 further requires "*wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit.*"

499. As discussed for claim 18, in the "*second operable state*" that operates on the battery backup supply that is converted to the 12-volt level provides a

"*second pre-regulated voltage*" (720) which is supplied to Harris's on-board voltage regulator module ("*voltage conversion circuit*") via circuitry that includes Amidi's power switch multiplexer (Fig. 7) ("*a circuit*") in the power management block (Fig. 5) of Amidi. *Supra* ¶¶479-492; *see, e.g.*, Ex. 1024 (Amidi) at Figs. 5 and 7 (reproduced above for claim limitation [19.a]), Fig. 6 (showing same in power management block implementation).

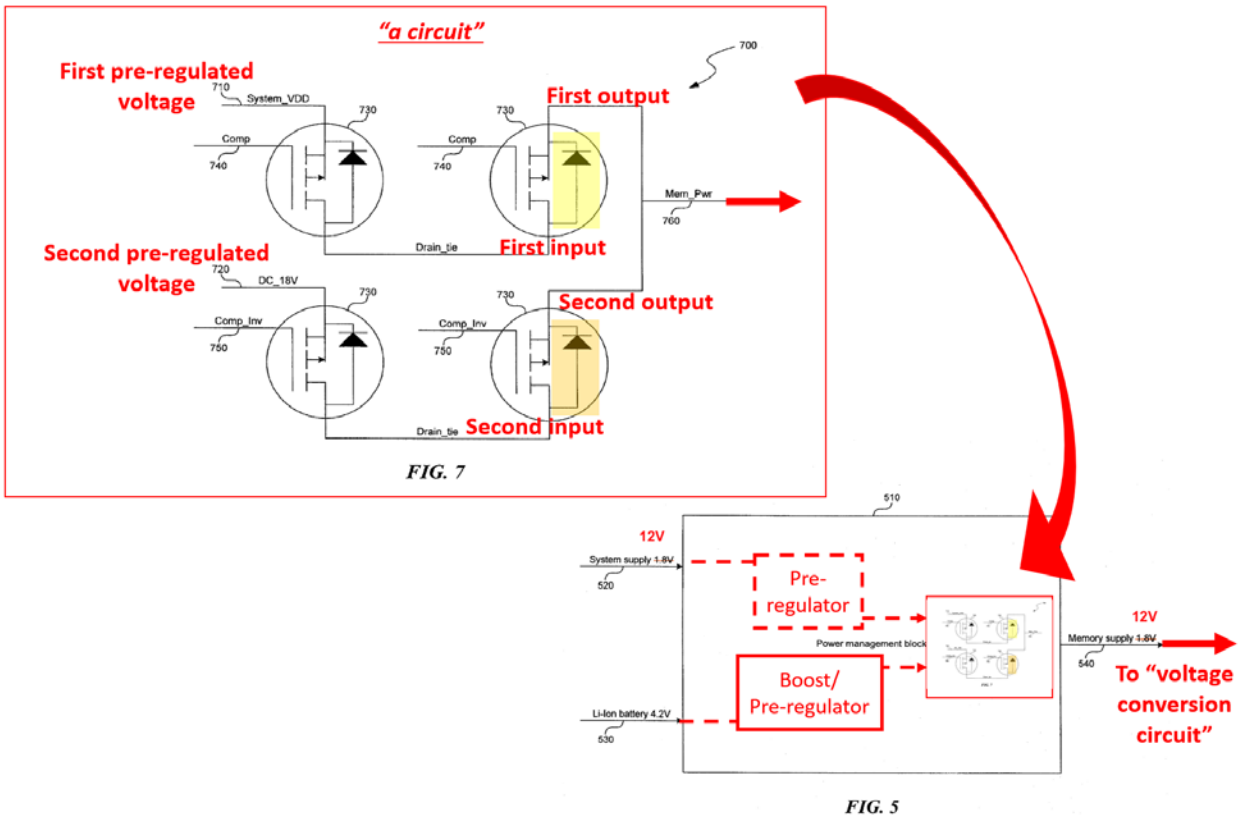


FIG. 7

FIG. 5

500. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit*" limitation.

20. Claim 20 is Unpatentable

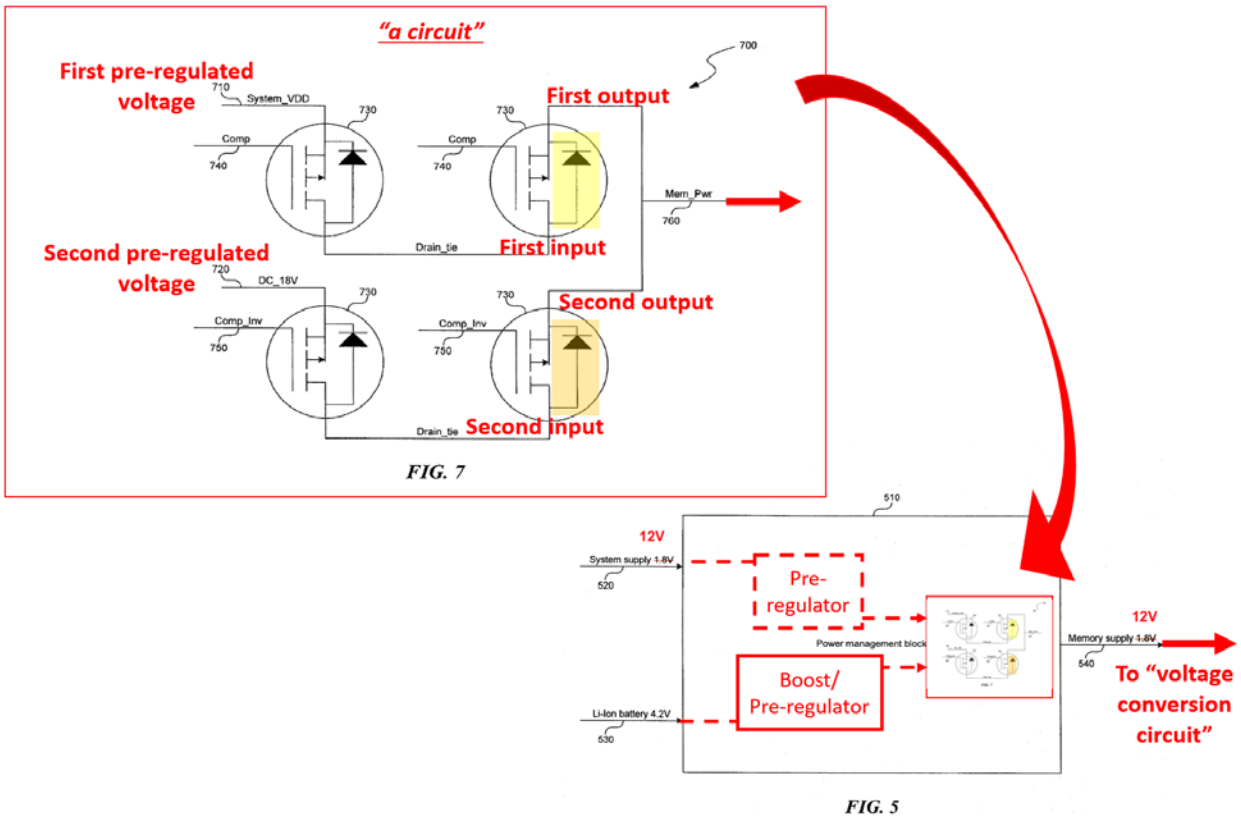
501. Claim 20 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [20.a] Wherein the Circuit Includes a First Diode

502. Claim 20 requires "*[t]he memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit*."

503. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

504. As discussed for claim 19, the first or second pre-regulated voltage is supplied to the on-board voltage regulator module ("*voltage conversion circuit*") via circuitry that includes the power switch multiplexer ("*a circuit*") in the power management block of Amidi that is adapted to operate with a 12-volt external voltage source, as disclosed by Harris. *Supra*, ¶¶493-500; *see, e.g.*, Ex. 1024 at Figs. 5 and 7 (reproduced and annotated below), Fig. 6 (showing same in power management block).



505. As shown here, the power switch multiplexer includes "*a first diode*" (yellow) having a "*first input*" coupled to the "*first pre-regulated voltage*" (710) from the system supply and "*a first output*" coupled to Harris's on-board voltage regulator module ("*voltage conversion circuit*") through the "Mem_Pwr" output (760) ("*having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit*"). *See* Ex. 1024 at 4:64-5:9.

506. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein the circuit includes a first diode having a first input and a*

first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit" limitation.

b) [20.b] Wherein the Circuit Includes a Second Diode

507. Claim 20 further requires "*wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit*."

508. The prior art references in each of Grounds 2 and 3 teach this limitation to a Skilled Artisan.

509. As discussed for claim 19, the first or second pre-regulated voltage is supplied to Harris's on-board voltage regulator module ("*voltage conversion circuit*") via circuitry that includes the power switch multiplexer ("*a circuit*") in the power management block of Amidi that is adapted to operate with a 12-volt external voltage source, as disclosed by Harris. *Supra*, ¶¶493-500; *see, e.g.*, Ex. 1024 at Figs. 5 and 7 (reproduced below), Fig. 6 (showing same in power management block).

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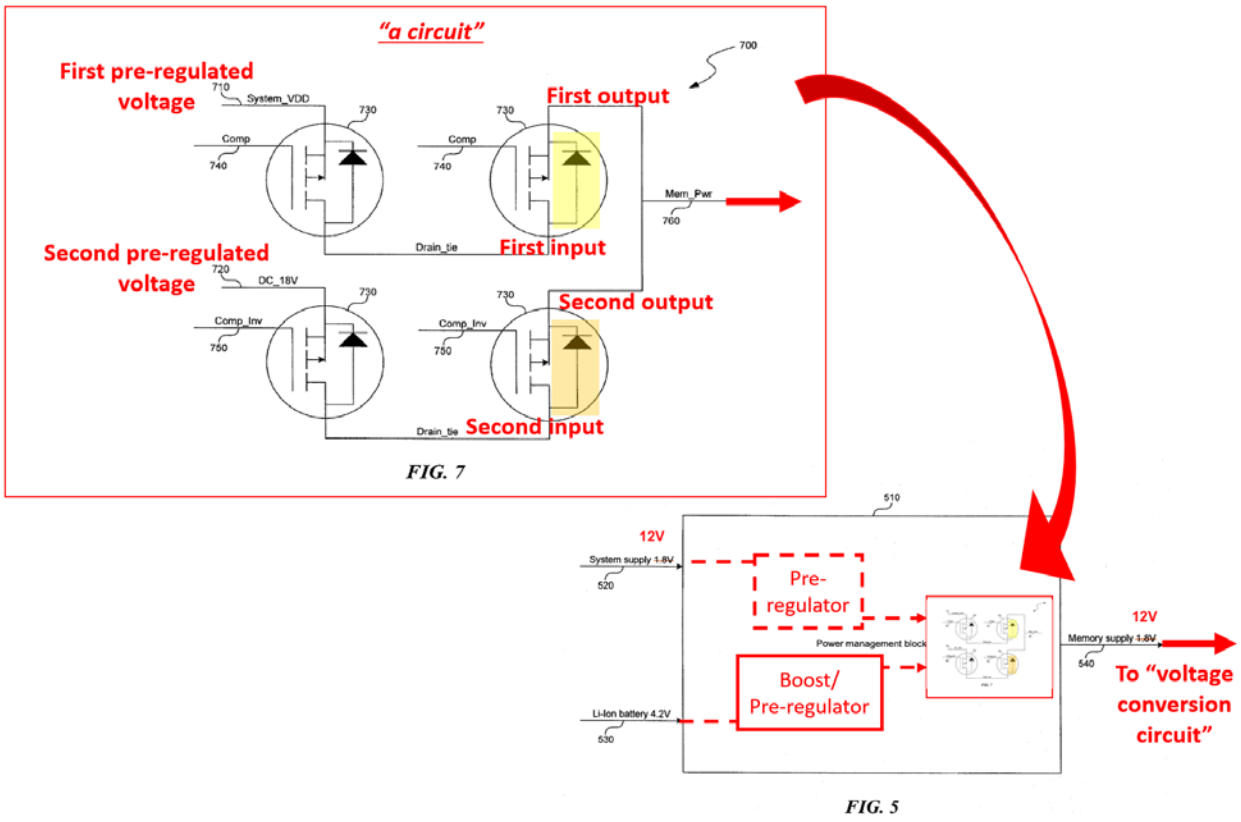


FIG. 7

FIG. 5

510. As shown, the power switch multiplexer includes "*a second diode*" (orange) having "*a second input*" coupled to the "*second pre-regulated voltage*" (720) from the battery backup power supply, and "*a second output*" coupled to "*the first output*" and to Harris's on-board voltage regulator module ("*voltage conversion circuit*") through the "Mem_Pwr" output (760) ("*having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit*"). *See* Ex. 1024 at 5:10-29.

511. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein the circuit includes a second diode having a second input*

and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit" limitation.

21. Claim 21 is Unpatentable

512. Claim 21 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [21.a] Preamble

513. The preamble of claim 21 requires that "*[t]he memory module of claim 16, further comprising*."

514. As discussed above with reference to claim 16, the prior art references in each of Grounds 2 and 3 satisfy "*[t]he memory module of claim 16*." *See* ¶¶ 450-474.

b) [21.b] A First Circuit with a First Input, Second Input, and an Output

515. Claim 21 requires "*a first circuit having a first input, a second input and an output, the first input coupled to a first pre-regulated voltage, the second input coupled to a second pre-regulated voltage, the output coupled to the voltage conversion circuit*."

516. As shown in the table below, claim element [21.b] is very similar to claim elements [20.a] – [20.b]:

Claim 20	**Claim 21**
[20.a] The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit [20.b] wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.	[21.b] a first circuit having a first input, a second input and an output, the first input coupled to a first pre-regulated voltage, the second input coupled to a second pre-regulated voltage, the output coupled to the voltage conversion circuit,

517. As discussed above with reference to claim elements [20.a] – [20.b], the prior art references in each of Grounds 2 and 3 satisfy this limitation. *See* ¶¶502-511.

c) [21.c] Wherein the Voltage Conversion Circuit Provides the First Regulated Voltage to the SDRAM devices

518. Claim 21 further requires "*wherein the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a supply voltage*."

519. As shown in the table below, claim element [21.c] is very similar to claim elements [18.a] – [18.b]:

Claim 18	**Claim 21**
[18.a] The memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and [18.b] wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.	[21.c] wherein the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a supply voltage,

520. As discussed above with reference to claim elements [18.a] – [18.b], the prior art references in each of Grounds 2 and 3 satisfy this limitation. *See* ¶¶480-492.

d) [21.d] Wherein, in the First Operable State, the First Circuit Provides the First Pre-Regulated Voltage to the Voltage Conversion Circuit

521. Claim 21 further requires "*wherein, in the first operable state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the first pre-regulated voltage*."

522. As shown in the table below, claim element [21.d] is very similar to claim element [19.a]:

Claim 19	**Claim 21**
[19.a] The memory module of claim 18, wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit, and	[21.d] wherein, in the first operable state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the first pre-regulated voltage,

523. As discussed above with reference to claim element [19.a], the prior art references in each of Grounds 2 and 3 satisfy this limitation. *See* ¶¶ 494-497.

e) [21.e] Wherein, in the Second State, the First Circuit Provides the Second Pre-Regulated Voltage to the Voltage Conversion Circuit

524. Claim 21 further requires "*wherein, in the second state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the second pre-regulated voltage*."

525. As shown in the table below, claim element [21.e] is very similar to claim element [19.b]:

Claim 19	**Claim 21**
[19.b] wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit.	[21.e] wherein, in the second state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the second pre-regulated voltage.

526. As discussed above with reference to claim element [19.b], the prior art references in each of Grounds 2 and 3 satisfy this limitation. *See* ¶¶ 498-500.

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22. Claim 22 is Unpatentable

527. Claim 22 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

528. Claim 22 requires "*[t]he memory module of claim 21, wherein the first circuit includes a first diode coupled between the first input and the output and a second diode coupled between the second input and the output*."

529. As shown in the table below, claim is very similar to claim elements [20.a] – [20.b]:

Claim 20	**Claim 22**
[20.a] The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and [20.b] wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.	[22] The memory module of claim 21, wherein the first circuit includes a first diode coupled between the first input and the output and a second diode coupled between the second input and the output.

530. As discussed above with reference to claim elements [20.a] – [20.b], the prior art references in each of Grounds 2 and 3 satisfy this limitation. *See* ¶¶502-511.

23. Claim 23 is Unpatentable

531. Claim 23 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [23.a] Wherein the Voltage Monitor Circuit is Configured to Produce a Trigger Signal

532. Claim 23 requires "*[t]he memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage*."

533. As shown in the table below, claim element [23.a] is very similar to claim elements [4.b] and [6.b]:

Claims 4, 6	**Claim 23**
[4.b] . . . the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, [6.b] . . . the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage,	[23.a] The memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and

534. As discussed above with reference to claim limitations [4.b] and [6.b], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *See* ¶¶306-314 (claim limitation [4.b]), ¶¶345-355 (claim limitation [6.b]).

b) [23.b] Wherein the Controller is Configured to Perform One or More Operations

535. Claim 23 further requires "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*."

536. As shown in the table below, claim element [23.b] is very similar to claim element [5.c]:

Claim 5	Claim 23
[5.c] wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.	[23.b] wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

537. As discussed above with reference to claim element [5.c], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶334-340.

24. Claim 24 is Unpatentable

538. Claim 24 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [24.a] Preamble

539. The preamble of claim 24 requires "*[a] memory module comprising*."

540. As shown in the table below, claim element [24.a] is identical to claim element [1.a]:

Claim 1	Claim 24
[1.a] A memory module comprising:	[24.a] A memory module comprising:

541. As discussed above with reference to claim element [1.a], to the extent the preamble of claim 1 is limiting, Harris alone, or in combination with the FBDIMM Standards, satisfies "[a] memory module." *Supra* ¶¶217-223.

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b) [24.b] A Printed Circuit Board (PCB) Having an Interface

542. Claim 24 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system*."

543. As shown in the table below, claim element [24.b] is very similar to claim element [1.b]:

Claim 1	**Claim 24**
[1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;	[24.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;

544. As discussed above with reference to claim element [1.b], Harris alone, or in combination with the FBDIMM Standards, satisfies this limitation. *Supra* ¶¶224-232.

c) [24.c] A Voltage Conversion Circuit

545. Claim 24 requires "*a voltage conversion circuit configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages*."

546. As shown in the table below, claim element [24.c] is very similar to claim element [1.c]:

Claim 1	**Claim 24**
[1.c] a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;	[24.c] a voltage conversion circuit configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

547. As discussed above with reference to claim element [1.c], the prior art in each of Grounds 1 through 3 satisfies this limitation. *Supra* ¶¶233-260.

d) [24.d] A Plurality of Components Coupled to the PCB

(1) [24.d.1] Plurality of components each coupled to at least one regulated voltage

548. Claim 24 requires "*a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages*."

549. As shown in the table below, claim element [24.d.1] is very similar to claim element [1.d.1]:

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Claim 1	**Claim 24**
[1.d.1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages,	[24.d.1] a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages,

550. As discussed above with reference to claim element [1.d.1], the prior art references in each of Grounds 1-3 satisfies this limitation. *Supra* ¶¶ 261-266.

(2) [24.d.2] Plurality of components includes SDRAM devices

551. Claim 24 requires "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices*."

552. As shown in the table below, claim element [24.d.2] is very similar to claim element [1.d.2]:

Claim 1	**Claim 24**
[1.d.2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and	[24.d.2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices,

553. As discussed above with reference to claim element [1.d.2], the prior art references in each of Grounds 1-3 satisfies this limitation. *Supra* ¶¶267-271.

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(3) [24.d.3] Wherein the SDRAM devices are coupled to the first regulated voltage

554. Claim 24 requires "*wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages*."

555. As shown in the table below, claim element [24.d.3] is very similar to claim element [1.d.5]:

Claim 1	**Claim 24**
[1.d.5] wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.	[24.d.3] wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages; and

556. As discussed above with reference to claim element [1.d.5], the prior art references in each of Grounds 1-3 satisfies this limitation. *Supra* ¶¶ 285-287.

e) [24.e] A Controller Coupled to the PCB

(1) [24.e.1] The Controller includes a voltage monitor circuit

557. Claim 24 requires "*a controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface of the PCB, the voltage monitor circuit configured to monitor the input voltage*."

558. As shown in the table below, claim element [24.e.1] is very similar to claim element [16.e.1]:

Claim 16	**Claim 24**
[16.e.1] a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage,	[24.e.1] a controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface of the PCB, the voltage monitor circuit configured to monitor the input voltage,

559. As discussed above with reference to claim element [16.e.1], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *See* ¶¶468-471. Because the PCB has the interface, receiving the input voltage from the host system via the interface also discloses receiving the input voltage from the host system via the interface of the PCB.

(2) [24.e.2] Wherein the controller is configured to perform one or more operations

560. Claim 24 further requires "*wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage*."

561. As shown in the table below, claim element [24.e.2] is very similar to claim elements [23.a] and [23.b]:

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Claim 23	**Claim 24**
[23.a] The memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and [23.b] wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.	[24.e.2] wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and

562. As discussed above with reference to claim elements [23.a] and [23.b], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶532-537.

(3) [24.e.3] Wherein the one or more operations include a write operation to transfer data into non-volatile memory

563. Claim 24 further requires "*wherein the one or more operations include a write operation to transfer data into non-volatile memory*."

564. As shown in the table below, claim element [24.e.3] is very similar to claim element [23.b]:

Claim 5	**Claim 24**
[23.b] wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.	[24.e.3] wherein the one or more operations include a write operation to transfer data into non-volatile memory.

565. As discussed above with reference to claim element [23.b], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶535-537.

25. Claim 25 is Unpatentable

566. Claim 25 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

567. Claim 25 requires "*[t]he memory module of claim 24, wherein, in response to the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state*."

568. As shown in the table below, claim 25 is very similar to claim element [16.e.2]:

Claim 16	**Claim 25**
[16.e.2] wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state	[25] The memory module of claim 24, wherein, in response to the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.

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569. As discussed above with reference to claim element [16.e.2], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶472-474.

26. Claim 26 is Unpatentable

570. Claim 26 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [26.a] Wherein, in the First Operable State, Voltage Conversion Circuit Provides First Regulated Voltage to SDRAM Devices Using First Pre-Regulated Voltage

571. Claim 26 requires "*[t]he memory module of claim 25, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage*."

572. As shown in the table below, claim element [26.a] is very similar to claim element [18.a]:

Claim 18	**Claim 26**
[18.a] The memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and	[26.a] The memory module of claim 25, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and

573. As discussed above with reference to claim element [18.a], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶480-487.

b) [26.b] Wherein, in the Second Operable State, Voltage Conversion Circuit Provides First Regulated Voltage to SDRAM Devices Using Second Pre-Regulated Voltage

574. Claim 26 further requires "*wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage*."

575. As shown in the table below, claim element [26.b] is very similar to claim element [18.b]:

Claim 18	**Claim 26**
[18.b] wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.	[26.b] wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.

576. As discussed above with reference to claim element [18.b], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶ 488-492.

27. Claim 27 is Unpatentable

577. Claim 27 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

578. Claim 27 requires "*[t]he memory module of claim 26, wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via a first diode*."

579. As shown in the table below, claim 27 is very similar to claim element [20.a]:

Claim 20	**Claim 27**
[20.a] The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and	[27] The memory module of claim 26, wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via a first diode.

580. As discussed above with reference to claim element [20.a], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶ 502-506.

28. Claim 28 is Unpatentable

581. Claim 28 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

582. Claim 28 requires "*[t]he memory module of claim 27, wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via a second diode*."

583. As shown in the table below, claim 28 is very similar to claim element [20.b]:

Claim 20	**Claim 28**
[20.b] wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.	[28] The memory module of claim 27, wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via a second diode.

584. As discussed above with reference to claim element [20.b], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *See* ¶¶ 507-511.

29. Claim 29 is Unpatentable

585. Claim 29 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

586. Claim 29 requires "*[t]he memory module of claim 24, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage or below a second predetermined threshold voltage*."

587. As shown in the table below, claim 29 is very similar to claim 17:

Claim 17	**Claim 29**
[17] The memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage.	[29] The memory module of claim 24, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage or below a second predetermined threshold voltage.

588. As discussed above with reference to claim 17, the prior art references in each of Grounds 2 and 3 satisfies this limitation. *See* ¶¶475-478.

30. Claim 30 is Unpatentable

589. Claim 30 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

590. Claim 30 requires "*[t]he memory module of claim 29, wherein the first predetermined threshold voltage is above a specified operating voltage, and the second predetermined threshold voltage is below the specified operating voltage*."

591. As shown in the table below, claim 30 is very similar to claim elements [9.b] and [11.b]:

Claims 9, 11	**Claim 30**
[9.b] wherein the first predetermined threshold voltage is above a specified operating voltage. [11.b] wherein the second predetermined threshold voltage is below the specified operating voltage, and	[30] The memory module of claim 29, wherein the first predetermined threshold voltage is above a specified operating voltage, and the second predetermined threshold voltage is below the specified operating voltage.

592. As discussed above with reference to claim elements [9.b] and [11.b], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶ 391-394, 407-410.

B. Claims 1-30 Are Unpatentable Over Grounds 4 and/or 5

593. As explained below claims 1-30 are unpatentable over Ground 4 (Spiers in view of Amidi) and Ground 5 (Ground 4 further in view of Hajeck).

1. Claim 1 is Unpatentable

594. Claim 1 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [1.a] Preamble

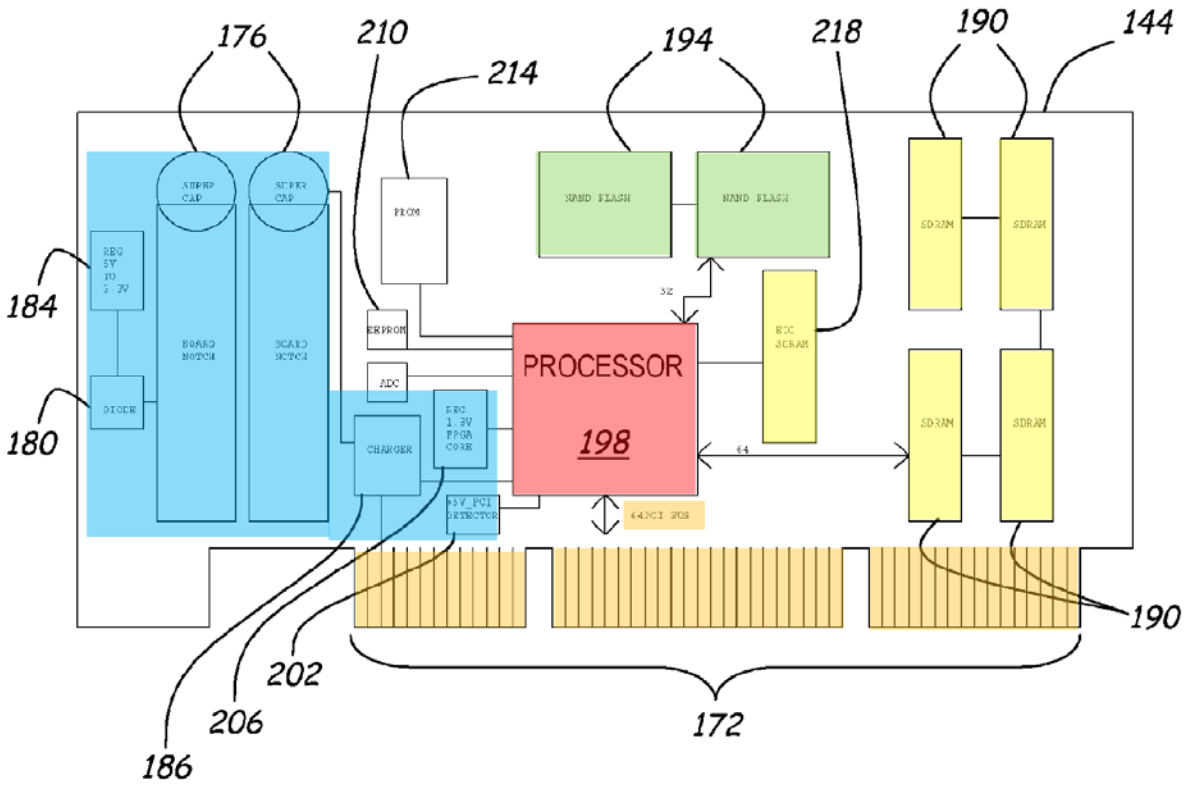
595. The preamble of claim 1 requires "*[a] memory module comprising.*"

596. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

597. As shown in the annotated figure below, Spiers discloses a "*memory module*" to a Skilled Artisan, such as backup device 144 implemented in a PCI

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card, and including volatile memory devices (*e.g.*, SDRAMs 190 annotated in yellow) and non-volatile memory devices (*e.g.*, NAND Flash 194 annotated in green).



Ex. 1025 at Fig. 5 (annotated). Spiers explains that, "[i]n this embodiment, the backup device is embodied in a PCI card having a 64-bit PCI connector 172 . . . the volatile memory comprises a number of SDRAM modules 190 . . . [and the] non-volatile memory in this embodiment comprises a number of NAND flash modules 194." *Id*. at [0037].

598. A Skilled Artisan would have understood that this backup device is a "*memory module*" because it includes a card (PCI card) with memories mounted

on it and configured to store data received from the system, as shown in Figure 3 of Spiers reproduced below.

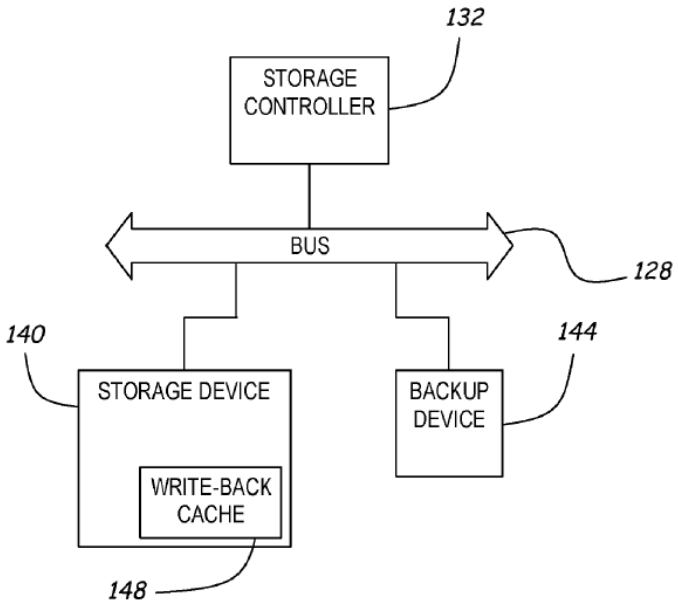


FIG.3

See id. at Fig. 3. For example, Spiers discloses that "the storage controller 132 stores a copy of the data in the backup device 144 as well as writing the data to the storage device 140. In this embodiment, if a failure occurs which results in the storage device 140 not storing the data to the storage media, a copy of the data is maintained in the backup device 144." *Id*. at [0034].

599. The backup device disclosed by Spiers is also consistent with how the 054 Patent describes a "*memory module*." For example, the 054 Patent states "[c]ertain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These

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memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the computer system to provide volatile memory to the computer system." Ex. 1001 (054 Patent) at 3:46-52.

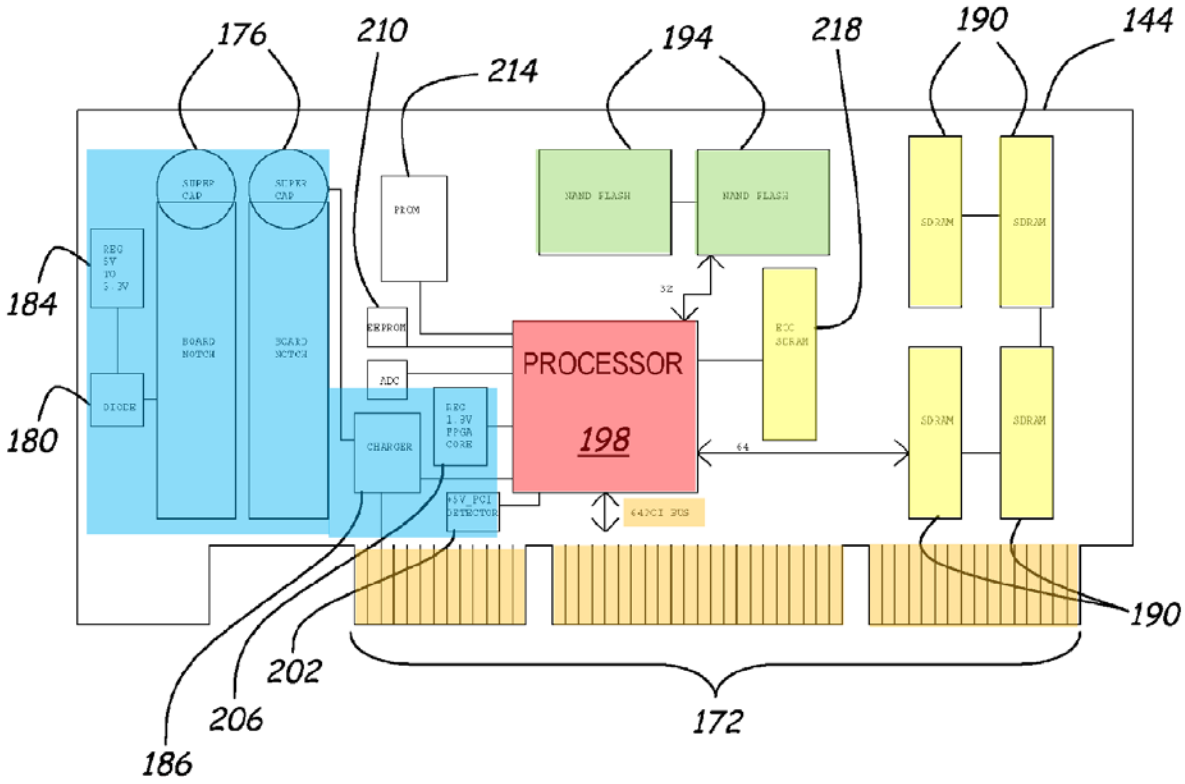
600. Accordingly, to the extent the preamble of claim 1 is limiting, the prior art references in each of Grounds 4 and 5 satisfy "*[a] memory module comprising*."

b) [1.b] Printed Circuit Board Having an Interface

601. Claim 1 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*"

602. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

603. Spiers discloses to a Skilled Artisan a printed circuit board (PCB), such as a PCB of a PCI card of backup device 144. Ex. 1025 at Fig. 5 (reproduced below, annotated).



See also, *e.g.*, Ex. 1031 at 298 (defining a PCI "expansion board" as a "circuit board that plugs into a mother board"), 152 (Section 4.4.3.2 describing routing for four-layer boards). Thus, Spiers satisfies a "*printed circuit board (PCB).*"

604. Spiers also discloses that the PCB has a 64-bit PCI connector 172 (orange). *See* Ex. 1025 at Fig. 5 (reproduced above, annotated). A Skilled Artisan would have understood that the PCI connector 172 is an interface that includes edge connections configured to fit into a corresponding slot connector on a PCI bus. For example, the figure below shows that a PCI board has a connecter with a keyway to fit into the corresponding slot on the motherboard.

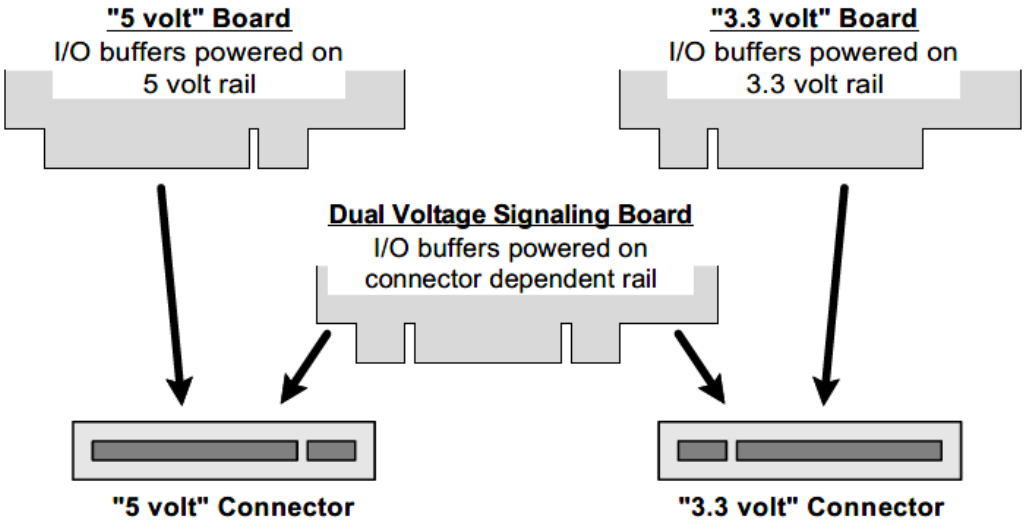


Figure 4-1: PCI Board Connectors

Ex. 1031 at 114, Fig. 4-1 (reproduced below), 3 ("Typical PCI Local Bus implementations will support up to four add-in board connectors . . . PCI extension cards use an edge connector and motherboards that allow a female connector . . . ."). Thus, Spiers satisfies the PCB "*having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections*."

605. Spiers also discloses edge connections of the interface "*configured to couple power, data, address and control signals between the memory module and the host system*." In particular, a Skilled Artisan would have understood that PCI connector 172 is for a dual-voltage signaling board since it has two notches or keyways that are configured to fit into a corresponding slot connector of a host system. *Id.* Accordingly, its "*edge connections* [are] *configured to couple power*,"

e.g., to a +5 volt power supply. *Id.* at 146-150 (describing pins of the board, including power pins for +5V power supply). For example, Spiers discloses receiving power at a 5-volt pin of the PCI card. Ex. 1025 at [0054] ("In the PCI card embodiment, this monitoring is performed by monitoring the voltage at a +5 volt pin.").

606. A Skilled Artisan would have also understood that, through the "64-bit PCI bus," Spiers's module receives address and data with corresponding read or write commands to store or retrieve the user data. Ex. 1025 at [0037]; Ex. 1031 at 1 ("The PCI Local Bus is a high performance 32-bit or 64 bit bus with multiplexed address and data lines"), 7 (Fig. 2-1, reproduced below, annotated, highlighting PCI pins including AD pins for address and data and C/BE pins for bus control signals); *see also id*. at 21-25 (describing C/BE commands for read and write operations).

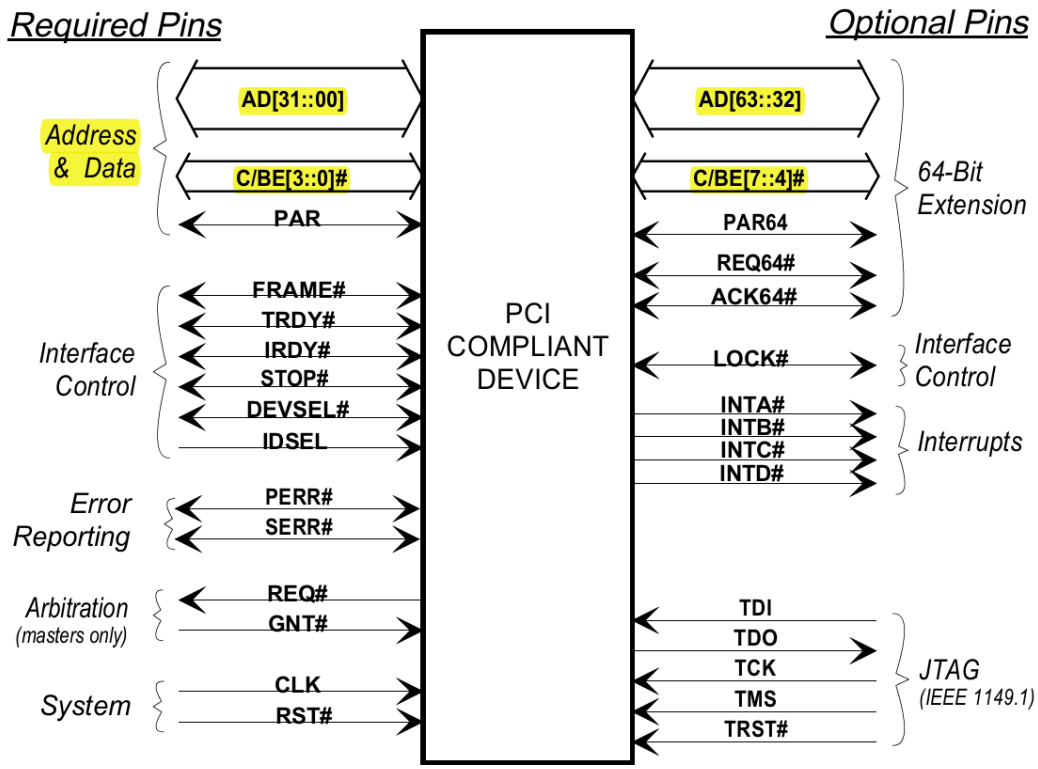


Figure 2-1: PCI Pin List

607. Spiers also discloses that "the backup device 144 utilizes a descriptor pointer queue contained within the FPGA processor 198 to receive commands from the storage controller." Ex. 1025 at [0039]; *see also id*. at Figs. 9, 10 and 11 (describing operational steps of the backup device processor when receiving commands and transferring data between the host memory and the SDRAMs on the module at corresponding addresses). Thus, Spiers satisfies the edge connections "*configured to couple power, data, address and control signals between the memory module and the host system*."

608. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a printed circuit board (PCB) having an interface configured to fit into a*

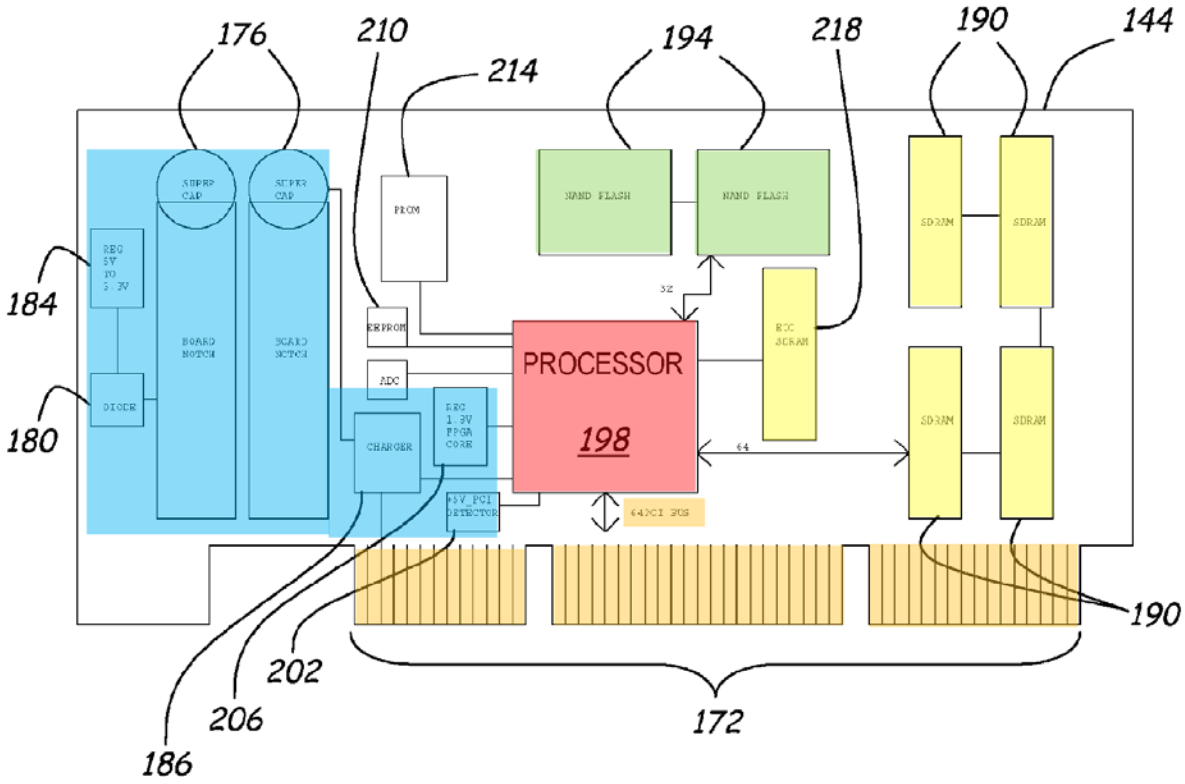
corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system."

c) [1.c] A Voltage Conversion Circuit

609. Claim 1 requires "*a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages.*"

610. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

611. Spiers discloses to a Skilled Artisan a "*voltage conversion circuit,*" including voltage regulator 206 (blue) providing power to the FPGA processor 198 and voltage converters providing power to other parts of backup device 144. Ex. 1025 at Fig. 5 (reproduced below, annotated). As shown in Fig. 5 of Spiers, the voltage conversion circuit is coupled to the PCB of the PCI card that converts a +5V power supply from the PCI bus to voltages required by the components of the PCI card, such as for the SDRAM devices 190 and 218 (yellow), the processor 198 (red), and the NAND Flash devices 194 (green).



612. Spiers discloses "monitoring the voltage at a +5 volt pin" of the PCI card to detect power failure. Ex. 1025 at [0054], Fig. 14. A Skilled Artisan would have understood from this disclosure that the PCI card uses the "+5 volt" power supply of the PCI bus to power components of the card, including the SDRAM devices 190 and 218, the processor 198, and the non-volatile memory 194. *See id.* at Fig. 5. Indeed, processor 198 transfers data from the (volatile) SDRAMs to the (non-volatile) NAND Flash devices in case of power failure detected at the "+5 volt" pin, indicating that Spiers's powers those components of its backup device 144 from the +5V power source in the PCI bus (when it is available). *See id.* at Abstract.

613. As discussed below in more detail, a Skilled Artisan would have understood that components of the backup device 144 require voltages that are less than 5V. For example, as expressly shown in Fig. 5 of Spiers, the backup memory 144 includes a voltage regulator 206 to provide 1.8V for the processor 198. Accordingly, a Skilled Artisan would have understood that the backup device 144 of Spiers includes "*a voltage conversion circuit coupled to the PCB*" of the PCI which converts the 5V power received through the "+5 volt pin" into voltages required by the components of the backup device 144 (including the voltage regulator 206 providing a regulated voltage for the FPGA core of the processor 198).

(1) First Regulated Voltage

614. The prior art references in each of Grounds 4 and 5 teach a first step-down converter "*configured to produce a* [first] *regulated voltage*" to a Skilled Artisan. As explained further below, it would have been obvious to implement this step-down converter as a "*buck converter*." *Infra* ¶¶649-660.

615. A Skilled Artisan would have understood that Spiers's module can be implemented with SDRAM memory devices, such as DDR2 or DDR3 memory devices that have been standardized by JEDEC at the time. *Supra* ¶¶189-207; *see also* Ex. 1025 at Fig. 4 (reproduced below annotated, showing power supply 168 providing regulated voltages to volatile memory 160 (yellow), non-volatile

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memory 164 (green) and processor 156 (red)), and [0036] ("The volatile memory 160, in one embodiment, is SDRAM utilized to store data from the storage controller 132 during typical write operations. The non-volatile memory 164, in one embodiment, is flash memory, and is utilized in the event of a power failure detection. As is understood, flash memory is a type of nonvolatile memory that may be erased and reprogrammed in units of memory referred to as blocks or pages. The processor 156, in this embodiment, upon detecting a power failure, switches the backup device 144 to the power supply 168, and moves the data in the volatile memory 160 to the non-volatile memory 164. After the data from the volatile memory 160 is stored in the non-volatile memory 164, the processor 156 shuts down the backup device 144.").

616. A Skilled Artisan would have recognized that SDRAM devices at the time required power supply voltages, such as VDD and VDDQ, that are less than, or stepped down from, 5 volts (and often even less than 3.3 volts, the other power supply in the PCI bus), and these power supply voltages need to be regulated to keep them within the limits, as required by the specification for those SDRAM devices. For example, the JEDEC DDR SDRAM standard, JESD79, requires a VDDQ supply of 2.5 volts +/- 0.2 volts and a VDD supply of, for example, 2.5 volts +/- 0.2 volts. Ex. 1045 (JESD79) at Cover, p.7. As another example, the JEDEC DDR2 SDRAM standard, JESD79-2B, requires VDD, VDDQ, and VDDL

supplies of 1.8 volts +/- 0.1V. Ex. 1026 at pp. 6-7. As a further example, the JEDEC DDR3 SDRAM standard, JESD79-3A, requires VDD and VDDQ supplies of 1.5 volts +/- 0.075V. Ex. 1046 at p.10.

617. For Grounds 4 and 5, there are two mappings for the "*regulated voltage[s],*" as shown in the figure below. While the figure below references Ground 4, the voltage mappings of Ground 5 are the same. These voltage mappings correspond to the implementation of Spiers's backup device with DDR3 (Voltage Mapping (A)) or DDR2 (Voltage Mapping (B)) DRAMs.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

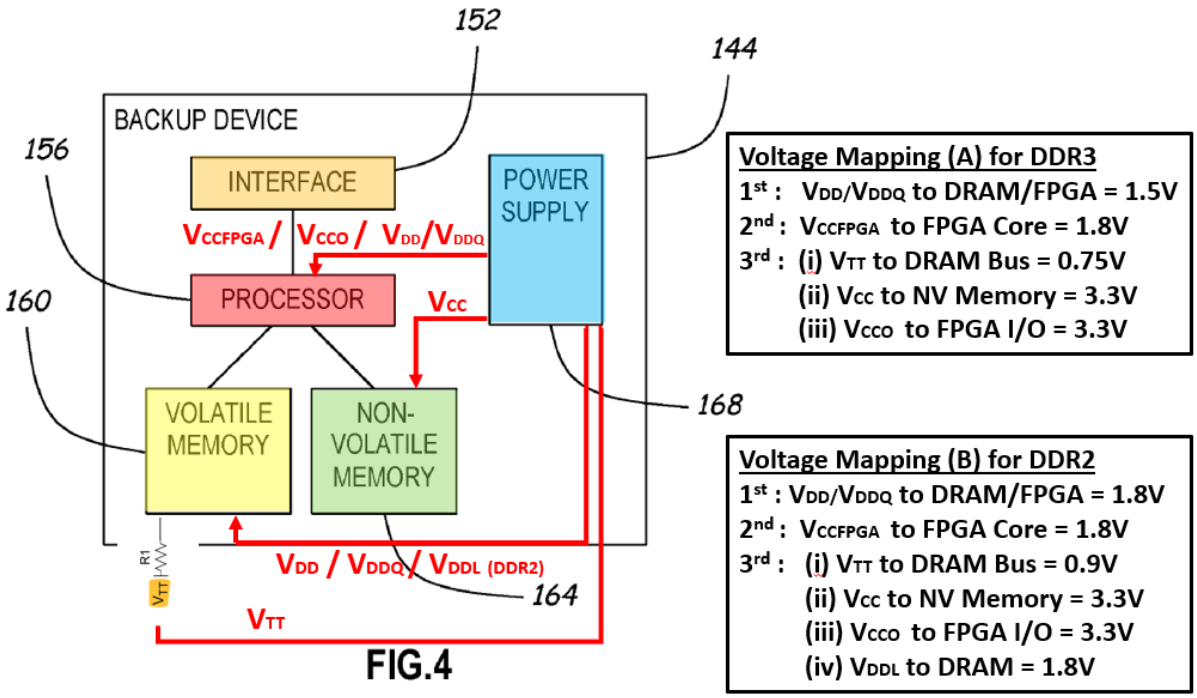


FIG.4

Ex. 1025 at Fig. 4 (annotated).

618. As previously explained, a Skilled Artisan would understand that JESD79-3A specifies a VDD power supply voltage of 1.5 volts for DDR3 DRAMs

(i.e., the "*first regulated voltage*" for Mapping A of Grounds 4 and 5). Ex. 1046 at p.10. Similarly, she would understand that JESD79-2B specifies a VDD of 1.8 volts for DDR2 DRAMs (i.e., the "*first regulated voltage*" for Mapping B of Grounds 4 and 5). Ex. 1026 at p.7.

619. Thus, for Mappings A and B of Grounds 4 and 5, Spiers teaches and discloses to a Skilled Artisan a first step-down converter "*configured to produce a* [first] *regulated voltage"* for the SDRAM devices from the +5 volt external power supply.

(2) Second Regulated Voltage

620. The prior art references in each of Grounds 4 and 5 teach a second step-down converter "*configured to produce a* [second] *regulated voltage*" to a Skilled Artisan. As explained further below, it would have been obvious to implement this step-down converter as a "*buck converter*." *Infra* ¶¶649-660.

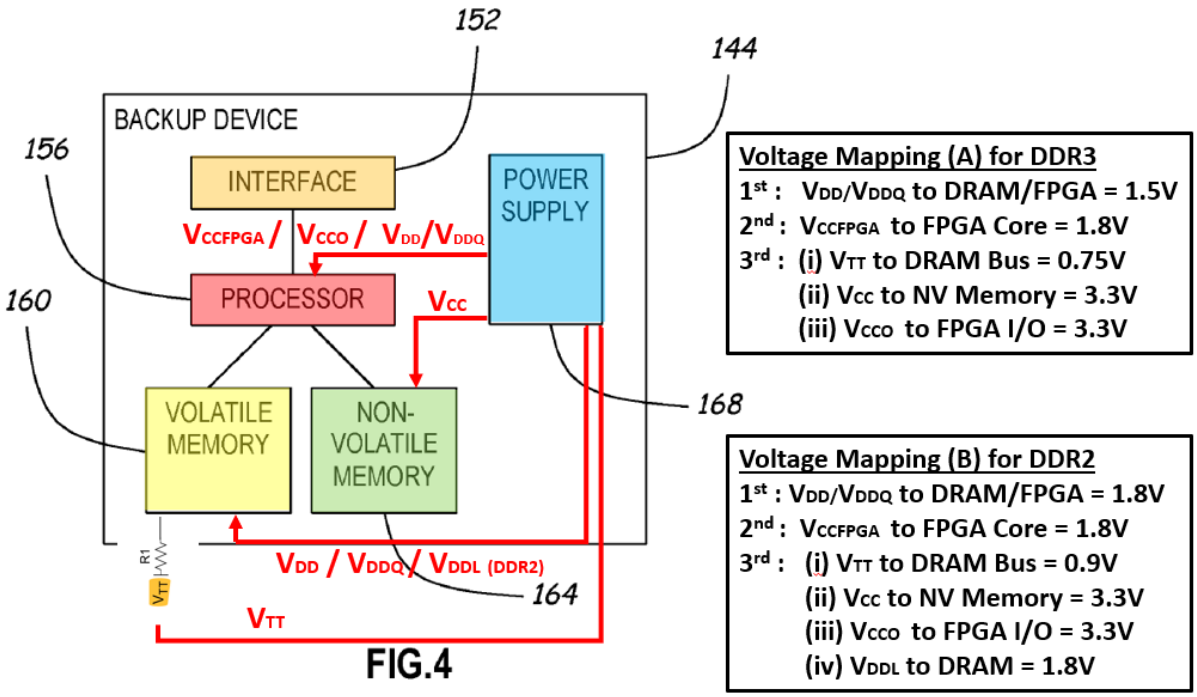
621. Spiers discloses that "[t]he FPGA processor receives power through a voltage regulator 206, which regulates the voltage required for the FPGA core." Ex. 1025 at [0037]. For the reasons discussed above, a Skilled Artisan would have understood, and it at least would have been obvious to her, that voltage regulator 206 includes a step-down converter to generate a supply voltage of, for example, 1.8 volts, as shown in Fig. 5 of Spiers (reproduced below in part, annotated), from the +5 volt external power supply. *Supra* ¶¶614-616; Ex. 1025 at Fig. 5.

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622. This understanding is reflected below in Voltage Mappings A and B of Grounds 4 and 5, where a VCCFPGA supply voltage of, for example, 1.8V is generated in the voltage regulator 206 (blue, below) and provided to processor 198 (red, below).

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



Ex. 1025 at Fig. 4 (annotated).

623. Thus, Spiers teaches and discloses to a Skilled Artisan that Spiers's voltage regulator 206 includes a second step-down converter "*configured to produce a* [second] *regulated voltage*," for example, VCCFPGA of 1.8 volts provided to the FPGA.

(3) Third Regulated Voltage

624. The prior art references in each of Grounds 4 and 5 teach a third step-down converter "*configured to produce a* [third] *regulated voltage*" to a Skilled Artisan. As explained further below, it would have been obvious to implement this step-down converter as a "*buck converter*." *Infra* ¶¶649-660.

625. As discussed above, Spiers discloses "monitoring the voltage at a +5 volt pin" of the PCI card to detect power failure. Ex. 1025 at [0054], Fig. 14. A Skilled Artisan would have understood from this disclosure that the PCI card uses the "+5 volt" power rail of the PCI bus to power the components coupled to the PCB, including the DRAM bus, non-volatile memory, and FPGA.

626. For Voltage Mapping A of Grounds 4 and 5, there are at least three possible voltage supplies produced by the third step-down converter (e.g., VTT to the DDR3 DRAM bus, VCC to the non-volatile memory, or VCCO to the FPGA).

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

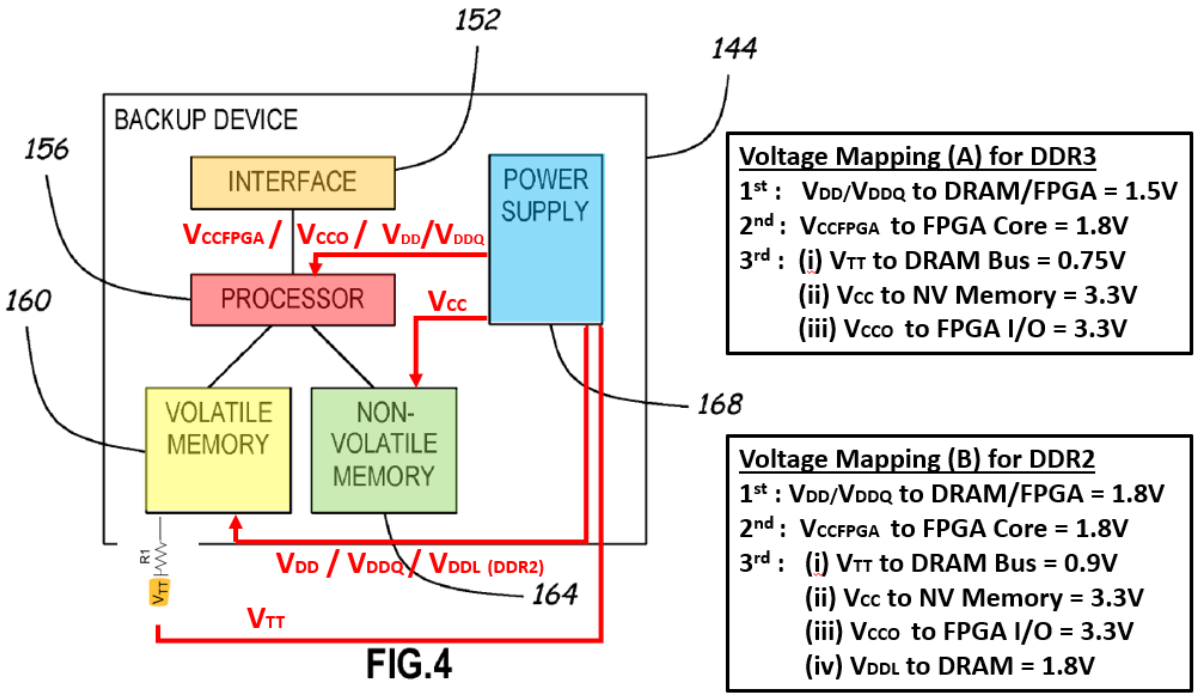


FIG.4

Ex. 1025 at Fig. 4 (annotated).

627. Regarding voltage supply VTT, a Skilled Artisan would have recognized that DRAM devices, at the time, required two supply voltages which are less than 5 volts. *See*, *e.g.*, Ex. 1046 (JESD79-3A) at 10 (disclosing VDD/VDDQ=1.5V for DDR3 devices), 15 (disclosing how to turn on supply voltages, including VTT), 109 (disclosing that VTT=VDDQ/2); Ex 1026 (JESD79-2B) at 6-7 (disclosing VDD/VDDQ/VDDL=1.8V for DDR2 devices), 9 (disclosing how to turn on supply voltages, including VTT), 49 (disclosing tolerances, including for VTT), 55 and 71 (disclosing that VTT=VDDQ/2); *see also* Ex. 1047 at 2:7-15 ("In a number of situations, it may be necessary to provide one or more operating voltages that are different from the available supply voltage on a single

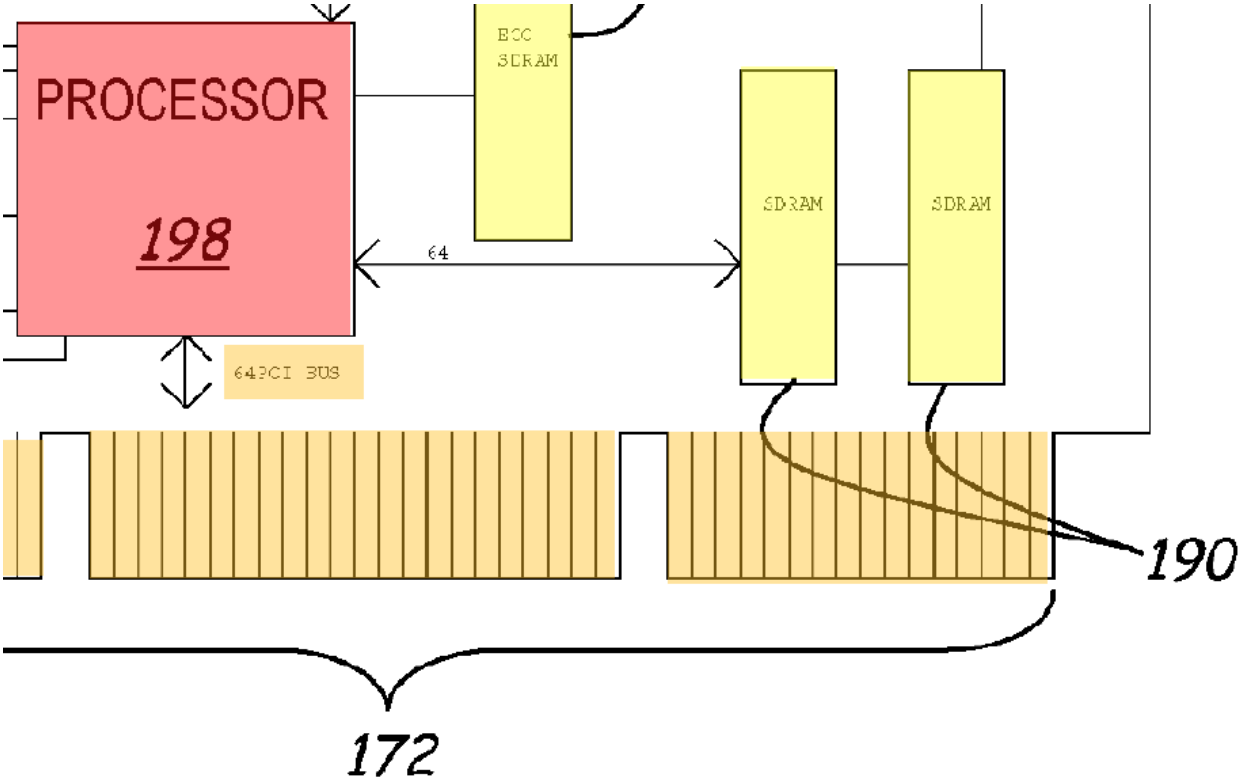
card. In at least one application, such as a dual-data-rate (DDR) memory system employing DDR random access memories (DRAMs), two supply voltages are required. Typically, a second supply voltage will be a prescribed fraction (e.g., one-half) of a first supply voltage, and generally may not exceed the first supply voltage."). For example, "a regulated voltage to a DDR DRAM, output voltage Vout2 may provide a VTT supply voltage to the DRAM." *Id*. at 5:56-59.

628. A Skilled Artisan would have also recognized that VTT is a termination voltage whose value is half of VDD/VDDQ (and the same voltage as a reference voltage, VREF) and that VTT is required for the proper operation of the DRAM devices, including DDR2, DDR3, and DDR4 DRAMs. *See, e.g.*, Ex. 1045 at pp. 8, 54, 60 ("VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the dc level of VREF."); Ex. 1026 at pp. 9, 49 (similar); Ex. 1046 at p.15 (similar).

629. Furthermore, a Skilled Artisan would have understood that the processor 198 of Spiers's module, similar to an AMB in a fully buffered memory module (FBDIMM), buffers address, command, and data signals for the SDRAM devices. *Supra* at ¶606. For example, Spiers discloses that processor 198 (red) receives read and write commands with corresponding address and data signals on a 64-bit PCI bus interface 172, buffers those in a FIFO, decodes the commands, and performs the corresponding read and write operations into the SDRAM

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devices on the SDRAM interface. Ex. 1025 (Spiers) at Fig. 5 (reproduced below in part, showing 64 bits of data to/from processor 198 and then to/from SDRAM 190).



See also id. at Fig. 9 (reproduced below and annotated) (showing the process of Spiers's processor 198 receiving read and write commands from the storage controller on a PCI bus and, in response, reading or writing corresponding data from and to SDRAMs 190 and 218 on an SDRAM bus), [0037] ("A FPGA processor 198 that provides PCI interfacing through a 64-bit PCI bus, is connected to the SDRAM modules 190 through a 64-bit bus, and is connected to the NAND flash modules 194 through a 32-bit bus."), [0046] ("At block 464 is it determined

if the command code indicates that the source of the data is the host and the destination of the data is the SDRAM. If so, the processor performs the operational steps for transferring data from the host memory to the SDRAM, as indicated at block 468.").

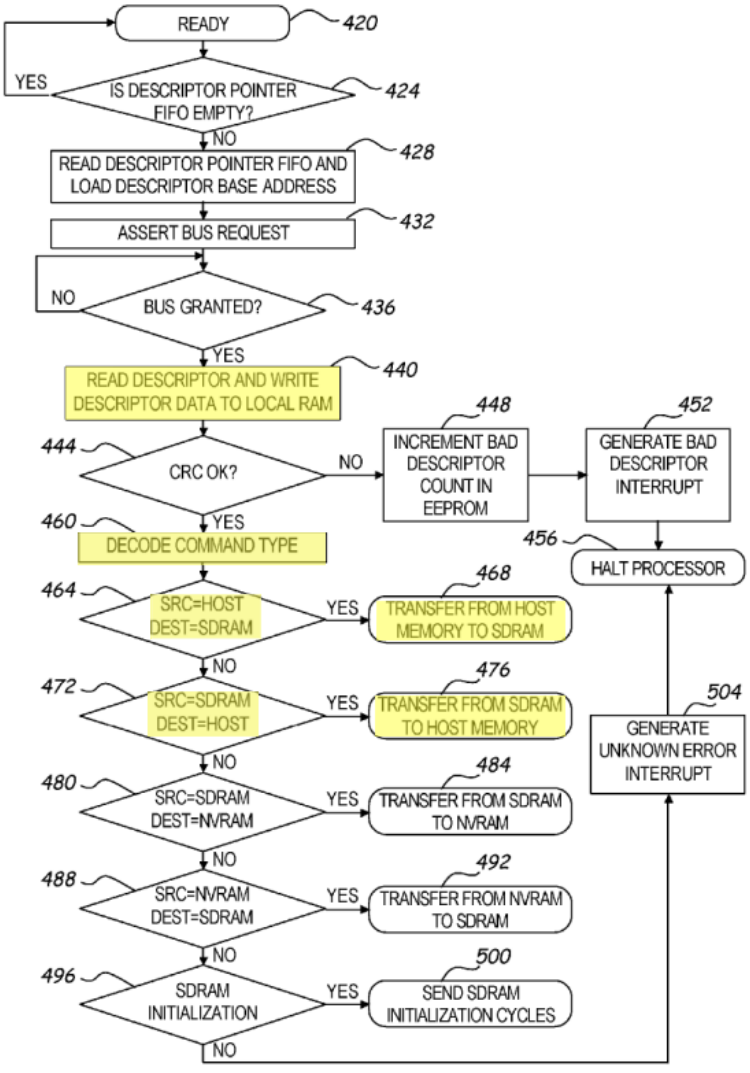
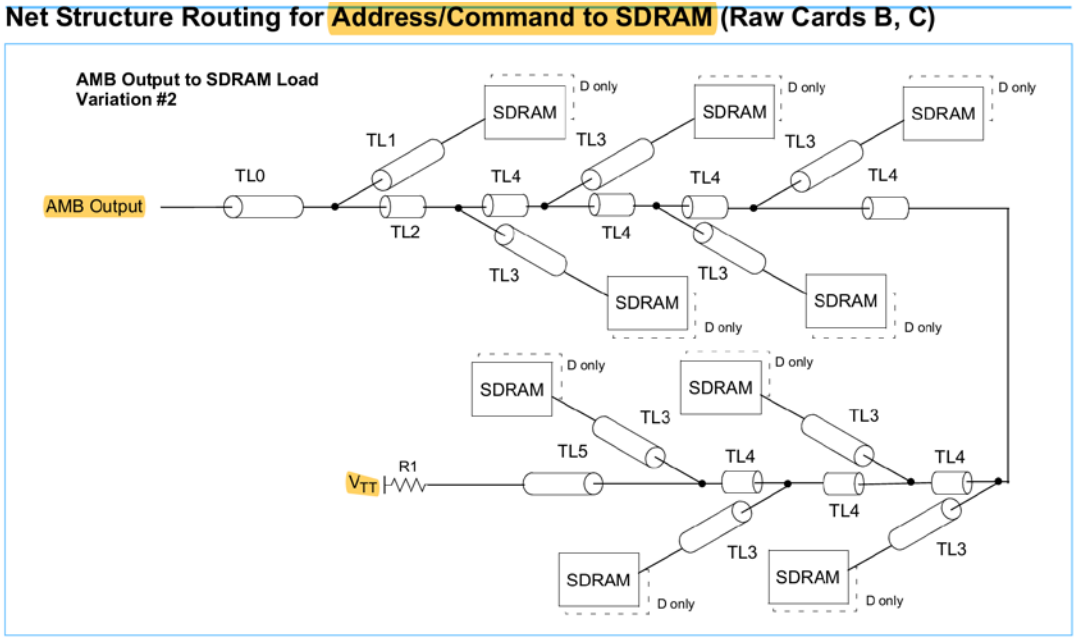


FIG.9

630. Therefore, a Skilled Artisan would have recognized that, in order to read and write the data from and to the SDRAMs, those SDRAM devices require proper termination voltages VTT. *See, e.g.*, Ex. 1046 (JESD79-3A) at 10

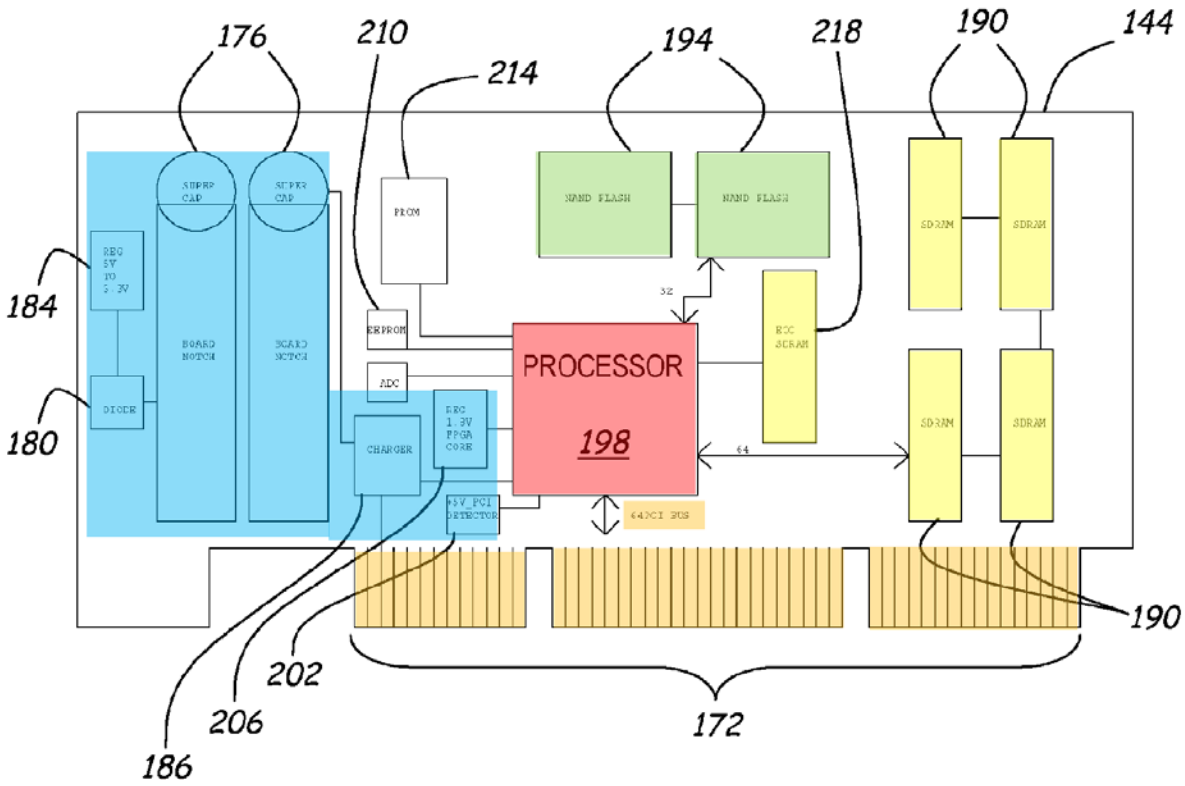
(disclosing VDD/VDDQ=1.5V for DDR3 devices), 15 (disclosing how to turn on supply voltages, including VTT), 109 (disclosing that VTT=VDDQ/2); Ex 1026 (JESD79-2B) at 6-7 (disclosing VDD/VDDQ/VDDL=1.8V for DDR2 devices), 9 (disclosing how to turn on supply voltages, including VTT), 49 (disclosing tolerances, including for VTT), 55 and 71 (disclosing that VTT=VDDQ/2). A Skilled Artisan would have also understood how to apply this VTT termination voltage on a memory module. *See, e.g.*, Ex. 1028 at 68 (reproduced below in part, annotated).

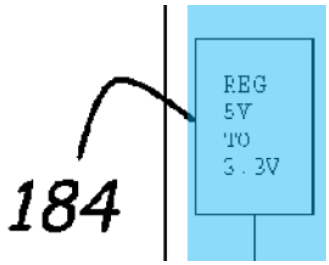


631. Thus, as reflected in Voltage Mapping A (above), a Skilled Artisan would have understood that, in order to properly terminate the clock, address, command and control signals for the DDR3 SDRAMs, the module of Spiers provides VTT of 0.75 volts (half of VDD) (i.e., the first of the three identified third

regulated voltages of Voltage Mapping A of Grounds 4 and 5) that is coupled to the DDR3 SDRAMs through termination resistors.

632. Regarding voltage supplies VCC to the non-volatile memory and VCCO to the FPGA, Spiers discloses to a Skilled Artisan that a converter, such as voltage regulator 184 or another, similar voltage converter, is configured to step down a 5 volt input supply to the 3.3 volt output supplies (e.g., VCC and VCCO) to be provided to the non-volatile memories 194 and processor 198. Ex. 1025 at Fig. 5 (reproduced below and annotated).





633. In particular, Spiers discloses to a Skilled Artisan that parts of its module are powered by 3.3 volts, as evidenced by a voltage regulator 184 that provides a 3.3-volt backup voltage. With regards to the backup voltage, Spiers explained that "the capacitors 176 are connected to a diode 180[,] a voltage regulator 184, and a charger 186. The charger 186 is utilized to charge the capacitors 176, and in the event of a power failure the capacitors are used as the power source to power the backup device 144 when moving data from the volatile memory to the non-volatile memory." Ex. 1025 at [0037].

634. Furthermore, as discussed above, a Skilled Artisan would have understood that Spiers uses the 5-volt power source from the PCI connector because its PCI detector 202 monitors a +5V pin to detect a power outage. *Supra* ¶¶611-613; Ex. 1025 at [0037] ("The FPGA processor 198 utilizes a power detection circuit that, in this embodiment, is a +5V PCI detector 202."). A Skilled Artisan would have also understood that, as disclosed by Spiers, the PCI standard allows the card (*e.g.*, backup device 144, "*memory module*") to use the 5-volt power source for all its power. Ex. 1031 at p.150 ("The expansion board may optionally draw all this power from either the +5V or +3.3V rail.").

635. To the extent one might argue that Spiers does not disclose using the 5-volt power source for all its power, it would have been obvious to a Skilled Artisan. For example, Spiers discloses using a +5V PCI detector to monitor a +5 volt rail of the PCI bus, Ex. 1025 at [0037], and a Skilled Artisan would have understood that all power can be drawn from this +5 volt rail, Ex. 1031 at p.150. Therefore, Spiers's express disclosure suggests to a Skilled Artisan to use the +5 volt rail for all of its power. A Skilled Artisan would have also understood and would have been motivated to use only the higher voltage source (5 volts) and convert that higher voltage locally on the board, because doing so would require smaller currents than receiving the same power on lower voltage rail.

636. Furthermore, using only the higher voltage source would allow mixing and upgrading different technologies requiring different voltage levels. *See, e.g.*, Ex. 1023 at [0011] ("Those skilled in the art should recognize upon reference hereto that by providing a tightly-controlled VRM as local voltage supply for on-board power requirements, a number of advantages may be obtained in the power supply design of an electronic component such as the memory module 100A. Since the Vdd and Vcc power supply rails are rendered independent from external voltage sources, the overall power supply interface to the memory module 100A is improved to better support large memory capacity scaling, hot-pluggability, DRAM technology independence (e.g., DDR2, DDR3, DDR4, and other DRAM

types), high DRAM device count (i.e., amenable to multi-ranking), as well as provide improved system-level cost sharing. Additionally, memory performance is also improved because of tighter voltage regulation.").

637. For example, a Skilled Artisan would have understood that Spiers's module uses a power converter which draws power from the +5 volt rail and converts that +5V down to 3.3 volts, similar to voltage regulator 184 which converts +5V down to 3.3V. A Skilled Artisan would have also understood that such a regulated 3.3V is provided to the processor 198, since FPGAs at the time used a 3.3V supply for VCCO, as shown in the figure below. *See also See* Ex. 1042 at 16 (showing the use of a commercially available dual buck converter, MPD4S014S, to supply VCCO of 3.3 volts). A Skilled Artisan would have also understood that the specific VCCO voltage value of 3.3 volts is just one example in a range of possibilities and that different FPGAs had different voltage requirements. *See, e.g.*, Ex. 1042 at 2 (reproduced below, in part, showing different FPGAs and their power requirements). Therefore, using the +5V rail and a down converter provides flexibility in selecting the VCCO value.

	Spartan™-3/3E/3L	Spartan™-IIE	Spartan™-II	Virtex™-5	Virtex™-4	Virtex-II Pro™	Virtex™-II
V_{CCINT}	1.2V @0.2A-5A	1.8V @0.2A-1.5A	2.5V @0.2A-1A	1.0V @0.2A-15A	1.2V @0.2A-20A	1.5V @0.2A-20A	1.5V @0.2A-20A
V_{CCO}	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-0.5A	1.5V-3.3V @50mA-0.5A	1.2V-3.3V @50mA-5A	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A
V_{CCAUX}	2.5V @50mA-0.3A	–	–	2.5V @50mA-0.7A	2.5V @50mA-0.7A	2.5V @50mA-0.3A	3.3V @50mA-0.3A

638. A Skilled Artisan would also have understood that some NAND Flash memory devices (194, annotated in green in Figure 5 of Spiers above) also use a power supply voltage of 3.3 volts at the time. *See, e.g.*, Ex. 1049 (NAND Flash Memory datasheet) at 1 ("VCC: 2.7V–3.6V"), 38 (recommending a VCC supply voltage of 3.3 volts, reproduced below in part and annotated).

Table 12: Recommended Operating Conditions

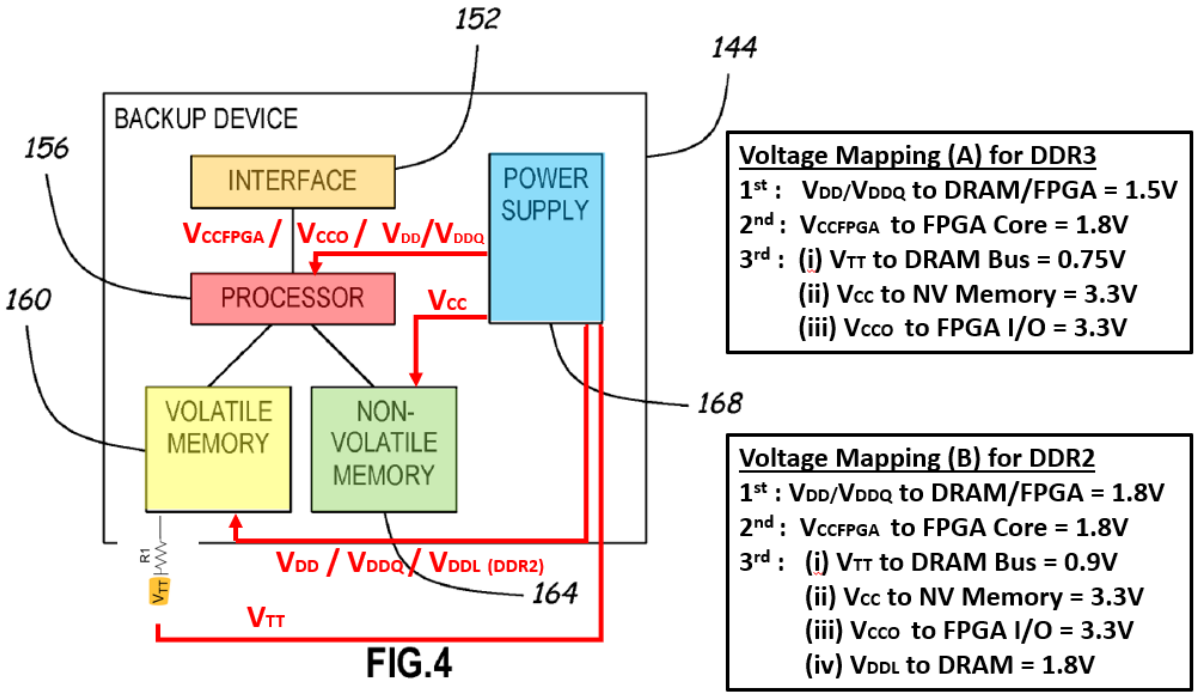
Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	^{t}A	0	–	+70	°C
	Extended	^{t}A	–40	–	+85	°C
Vcc supply voltage		Vcc	2.7	3.3	3.6	V
Supply voltage		Vss	0	0	0	V

639. A Skilled Artisan would have further understood that the 3.3-volt supply voltage is provided to both the processor (198, annotated in red in Figure 5 of Spiers above) and the Flash memories (194, green) when the processor transfers the data from the SDRAMs (190, yellow) to the Flash memories.

640. Thus, as reflected in Voltage Mapping A of Grounds 4 and 5, a Skilled Artisan would have understood that Spiers includes a step-down converter, such as voltage regulator 184 or another, similar voltage converter, that converts input supply voltage (e.g., 5 volts) down to 3.3 volts for the processor 198 (e.g., VCCO) and/or the non-volatile memories 194 (e.g., VCC) (i.e., the second and third of the three identified "[third] *regulated voltages*" of Voltage Mapping A of Grounds 4 and 5).

641. For Voltage Mapping B of Grounds 4 and 5, there are at least four possible voltage supplies produced by the third step-down converter (e.g., VTT to the DDR2 DRAM bus, VCC to the non-volatile memory, VCCO to the FPGA, or VDDL to the DDR2 DRAM).

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



Ex. 1025 at Fig. 4 (annotated).

642. As previously explained above, a Skilled Artisan would have recognized that VTT is a termination voltage whose value is half of VDD/VDDQ (and the same voltage as a reference voltage, VREF) and that VTT is required for the proper operation of the SDRAM devices, including DDR2 devices. *Supra* ¶¶627-631, *see, e.g.*, Ex 1026 (JESD79-2B) at 6-7 (disclosing VDD/VDDQ/VDDL=1.8V for DDR2 devices), 9 (disclosing how to turn on

supply voltages, including VTT), 49 (disclosing tolerances, including for VTT), 55 and 71 (disclosing that VTT=VDDQ/2). Applying this VTT signal was well within the level of skill at the time as evidenced by the similarities between Spiers's module and an FBDIMM. *See id.*

643. Thus, as reflected in Voltage Mapping B of Grounds 4 and 5 (above), a Skilled Artisan would have understood that, in order to properly terminate the clock, address, command and control signals, the module of Spiers includes a third step-down converter "*configured to provide a* [third] *regulated voltage*" VTT of, for example, 0.9V for DDR2 DRAMs.

644. For the reasons discussed above, a Skilled Artisan would have also understood that the module of Spiers includes a third step-down converter "*configured to provide a* [third] *regulated voltage*" VCC to the non-volatile memory 194 and/or VCCO to the processor 198. *Supra* ¶¶620-623.

645. Additionally, I understand that Patent Owner has indicated that the "*third regulated voltage*" can have the same voltage amplitude as the "*first regulated voltage*." Ex. 1073 at 59-61; *see also* Ex. 1071 at 43. Under Netlist's apparent claim construction, Spiers also discloses to a Skilled Artisan that a "*third regulated voltage*" VDDL is provided to the SDRAMs separately from VDD and VDDQ.

646. For example, the DDR2 standard expressly suggests to a Skilled Artisan to use a power source for VDDL that is separate from the voltage source(s) for VDD and VDDQ. Ex. 1026 at pp. 2 (NOTE 5) and 6-7 (reproduced below, annotated).

NOTE 5 VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ

NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**

Symbol	Type	Function
V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

See also id. at p.9 (disclosing order for applying VDDL separately from VDD and VDDQ; reproduced below, annotated).

2.2.1.1 Power-up and Initialization Sequence

The following sequence is required for POWER UP and Initialization.

1. Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.)

   - VDD, VDDL and VDDQ are driven from a single power converter output, AND
   - VTT is limited to 0.95 V max, AND
   - Vref tracks VDDQ/2.

   or

   - Apply VDD before or at the same time as VDDL.
   - Apply VDDL before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT & Vref.

   at least one of these two sets of conditions must be met.

647. Thus, a Skilled Artisan would have also understood that the module of Spiers includes a third step-down converter "*configured to provide a* [third] *regulated voltage*" VDDL of, for example, 1.8 volts to the DDR2 DRAMs.

648. For the reasons discussed above, a Skilled Artisan would have also understood that the module of Spiers includes a third step-down converter "*configured to provide a* [third] *regulated voltage*" VCC to the non-volatile memory 194 and/or VCCO to the processor 198. *Supra* ¶¶620-623.

(4) Implementing step-down converters with buck converters was obvious to a Skilled Artisan

649. Spiers in view of Amidi renders obvious to a Skilled Artisan that the voltage conversion circuit providing supply voltages to the components of the backup device 144 includes "*at least three buck converters*" to implement the step-down power converters from the +5V PCI supply voltage, as discussed above. *Supra* ¶¶609-648.

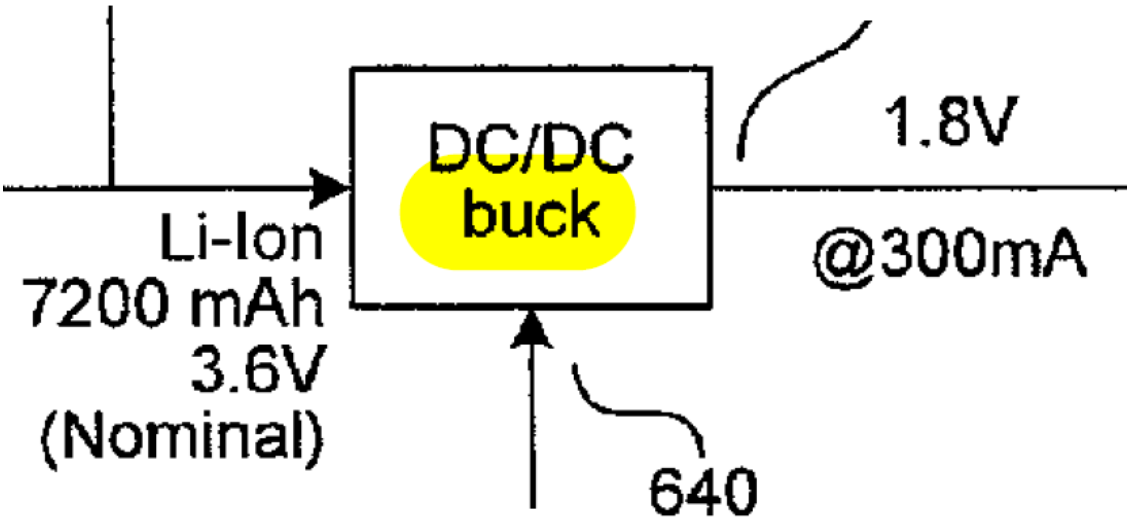
650. As discussed above, Spiers discloses to a Skilled Artisan that backup device 144 includes step-down voltage converters that provide regulated voltages for the SDRAM devices 190 and 218, the processor 198, and the flash memory devices 194 as required to power those devices. ***See id***. It would have been obvious to a Skilled Artisan to use a "*buck converter*" as the step-down converter to achieve high efficiency, reliable power conversion. *See, e.g.*, Ex. 1059 at 5:23-30 ("Switch mode buck converters have become popular due to two attractive

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features: first, they are more efficient than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, they can provide relatively high currents with lower power dissipation on chip than an LDO can."). A Skilled Artisan would have understood that the efficiency of power conversion is particularly important in implementations like Spiers, designed to handle power outages by transferring data from volatile to non-volatile memories using a temporary power supply, such as a capacitor, because any loss at the power conversion takes away time for this backup operation, risking its successful completion. *See, e.g.*, Ex. 1025 at Fig. 14 (step 752 checking if capacitors have sufficient charge to transfer data from volatile to non-volatile memory).

651. Indeed, it was well known at the time to use buck converters to power SDRAM devices. For example, Amidi discloses using a buck converter to convert backup battery power to a lower voltage for SDRAM memory devices. Ex. 1024 at Fig. 6 (buck converter 640), 4:38-41.

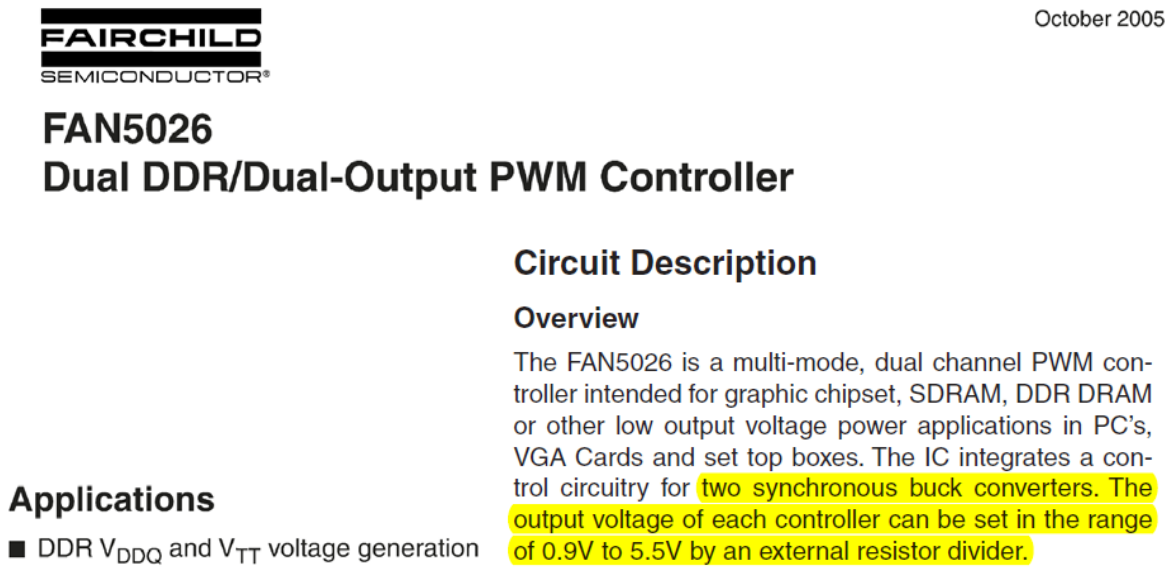
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Ex. 1069, p. 298



652. This was a well-known common practice at the time, as evidenced, for example, by Shearon (US7,023,187), which discloses "a multi (dual) voltage power supply architecture, in which an upstream buck converter stage is coupled in cascade with a downstream buck converter stage." Ex. 1047 at 2:47-55; *see also id.* at 5:56-59 (disclosing its buck converter for "supplying a regulated voltage to a DDR DRAM").

653. Such buck converters for SDRAMs were also commercially available at the time. *See id*. at 7:6-14 ("An embodiment of the dual buck mode power supply of the invention has been implemented in an integrated circuit, identified as part number ISL6530 by Intersil Corporation of Irvine, Calif., the assignee of the present application. Details regarding this part may be found in an advance data sheet, entitled 'Dual 5V Buck and Synchronous Buck Pulse-Width Modulator (PWM) Controller for DDRAM Memory VDDQ and VTT Termination', a copy of

which has been submitted as an Appendix."); *see also* Ex. 1041 at 1, 2 and 9 disclosing buck converters for SDRAM devices (reproduced below in part, annotated).



FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Applications

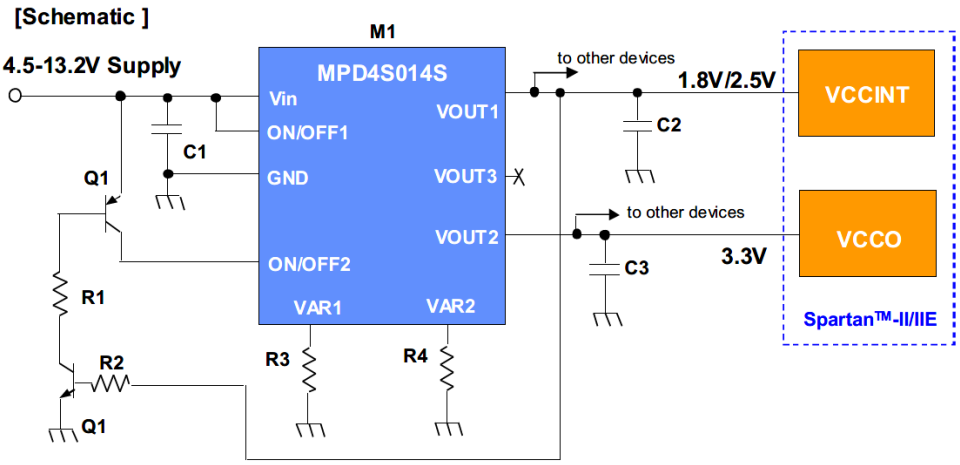
- DDR V_{DDQ} and V_{TT} voltage generation

Circuit Description

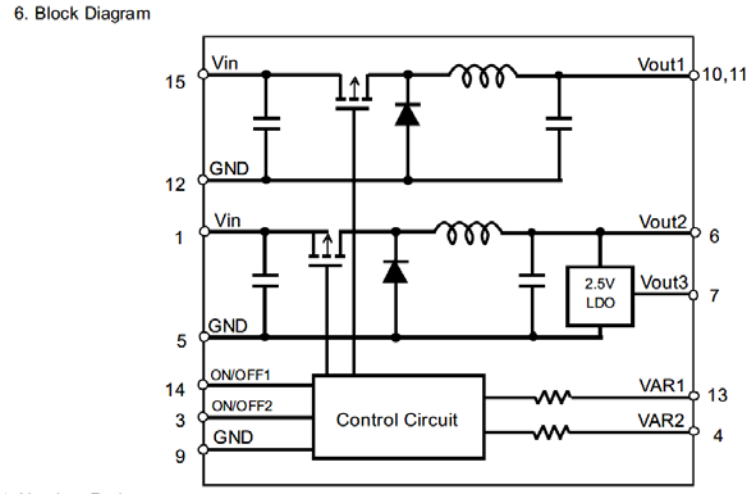
Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

654. Additionally, a Skilled Artisan would have understood that buck converters were commercially available to power FPGAs. *See* Ex. 1042 at 16 (reproduced below in part, showing the use of a commercially available dual buck converter, MPD4S014S, to supply those voltages, including 1.8 volts and 3.3 volts).



Compare Ex. 1048 at 2 (depicting internal structure of MPD4S014S with two typical buck converters, below) *with* Ex. 1058 at 5, Fig. 2 (illustrating a buck converter); Ex. 1032 at 164-165, Fig. 7-4(a) (same).

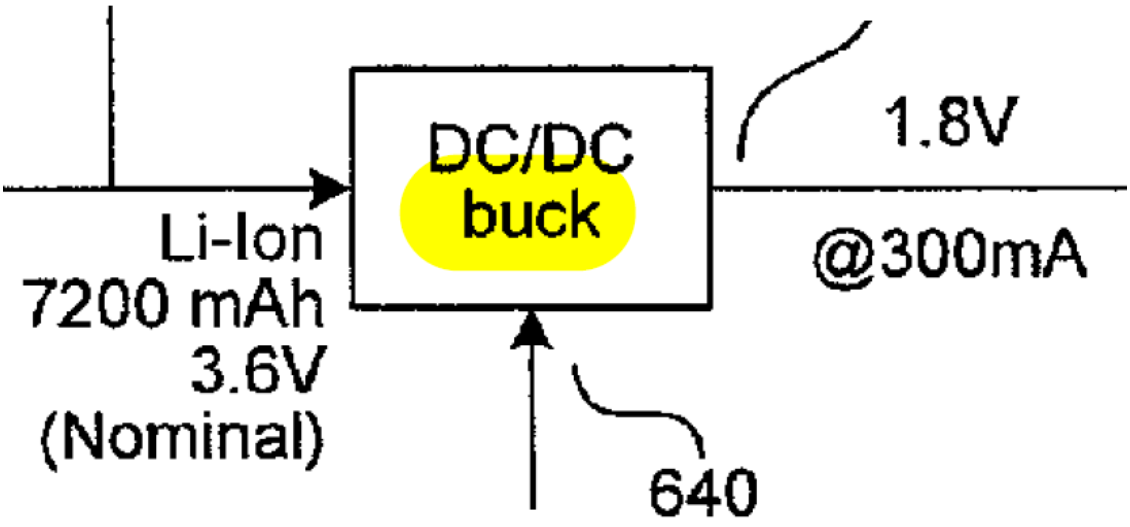


655. Therefore, a Skilled Artisan would have understood that using buck converters for powering (volatile and non-volatile) memory devices and FPGAs was a well-know, reliable technology providing nothing more than expected, namely efficient conversion providing regulated voltages as required by those components of the backup memory board 144 of Spiers.

656. Indeed, a Skilled Artisan would have understood that using a buck converter to convert a higher input voltage into a lower, regulated voltage was a readily available, reliable technology as taught by textbooks years before the 054 patent. *See, e.g.*, Ex. 1032 at p.161 (describing dc-dc switch-mode converters for regulated switch-mode dc power supplies, and identifying such a step-down converter as a "buck" converter), p.164 (in a Chapter entitled "Step-Down (Buck) Converter" explaining that, "[a]s the name implies, a step-down converter produces a lower average output voltage than the dc input voltage Vd. Its main application is in regulated dc power supplies and dc motor speed control."). A Skilled Artisan would have also understood that "only the step-down and the step-up are the basic converter topologies" although there are three more variations "of the two basic topologies." *Id*. at p.161 (also listing "Step-down/step-up (buck-boost) converter, "Cuk converter," and "Full-bridge converter").

657. Therefore, a Skilled Artisan would have understood that the "basic converter topology" for a dc-dc switch-mode converter that steps down the voltage is a "buck converter," and she would have been motivated to use this basic, reliable design for the step-down converters of backup device 144 because its "main application is in regulated dc power supplies." *Id*. at p.164. Indeed, Amidi also discloses using a buck converter to convert a higher voltage to a lower voltage in its memory module. *See, e.g.*, Ex. 1024 at Fig. 6 (showing a DC/DC buck

converter 640 to step down a higher voltage to a lower one, reproduced below in part, annotated).



658. A Skilled Artisan would have also understood that buck converters were more efficient and can provide higher currents with lower power dissipation than other alternatives, such as LDOs. *See, e.g.*, Ex. 1059 at 5:23-30 ("Switch mode buck converters have become popular due to two attractive features: first, they are more efficient than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, they can provide relatively high currents with lower power dissipation on chip than an LDO can.").

659. Therefore, a Skilled Artisan would have understood that each of the "*at least three regulated voltages*" can be produced by a respective one of "*at least three buck converters*" and using such buck converters would have been obvious because they were well-known reliable and efficient voltage converters to generate

the required tightly controlled voltage levels required for the memory devices and the processor 198 on Spiers's module.

660. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages*."

d) [1.d] A Plurality of Components Coupled to the PCB

(1) [1.d.1] Plurality of components each coupled to at least one regulated voltage

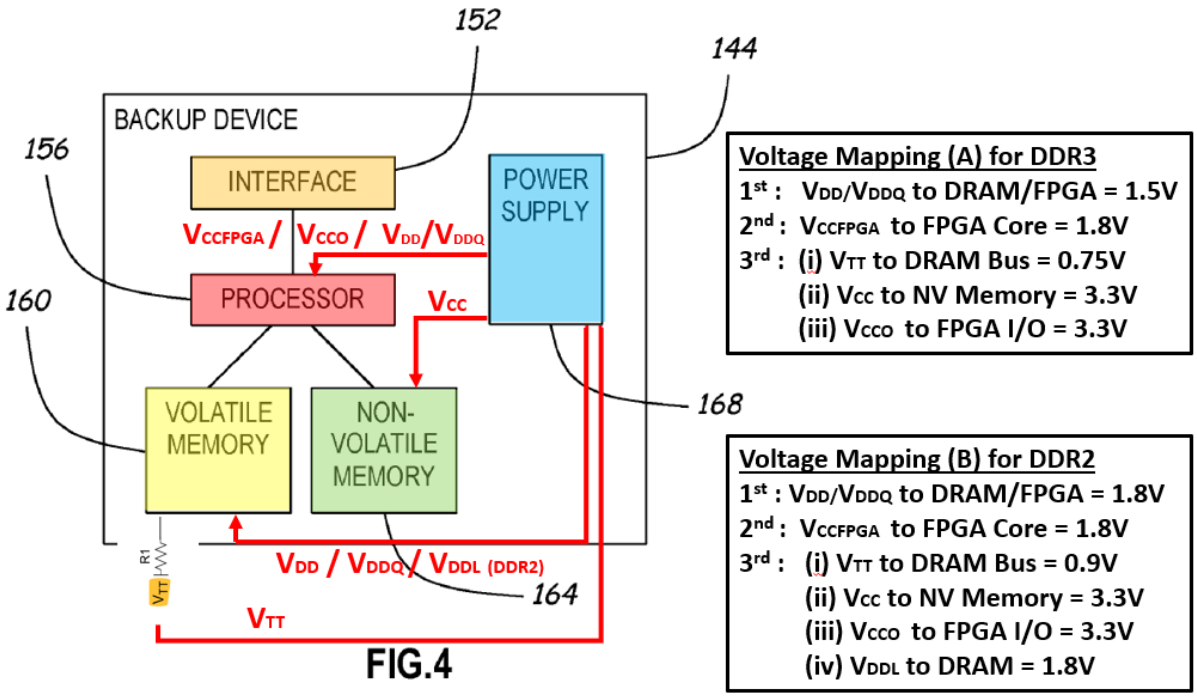
661. Claim 1 requires "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages.*"

662. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

663. As explained above for claim limitation [1.b], Spiers discloses to a Skilled Artisan using "*a printed circuit board (PCB)*" to implement a memory module. *Supra* ¶¶601-608. Further, as explained above for claim limitation [1.c], a plurality of components, including SDRAM 190 and 218, processor 198, termination resistors, and NAND flash memory 194, are coupled to the PCB and

each component is coupled to at least one of the "at least three regulated voltages." *Supra* ¶¶609-660; *see also* Ex. 1025 at Fig. 4 (annotated, reproduced below).

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



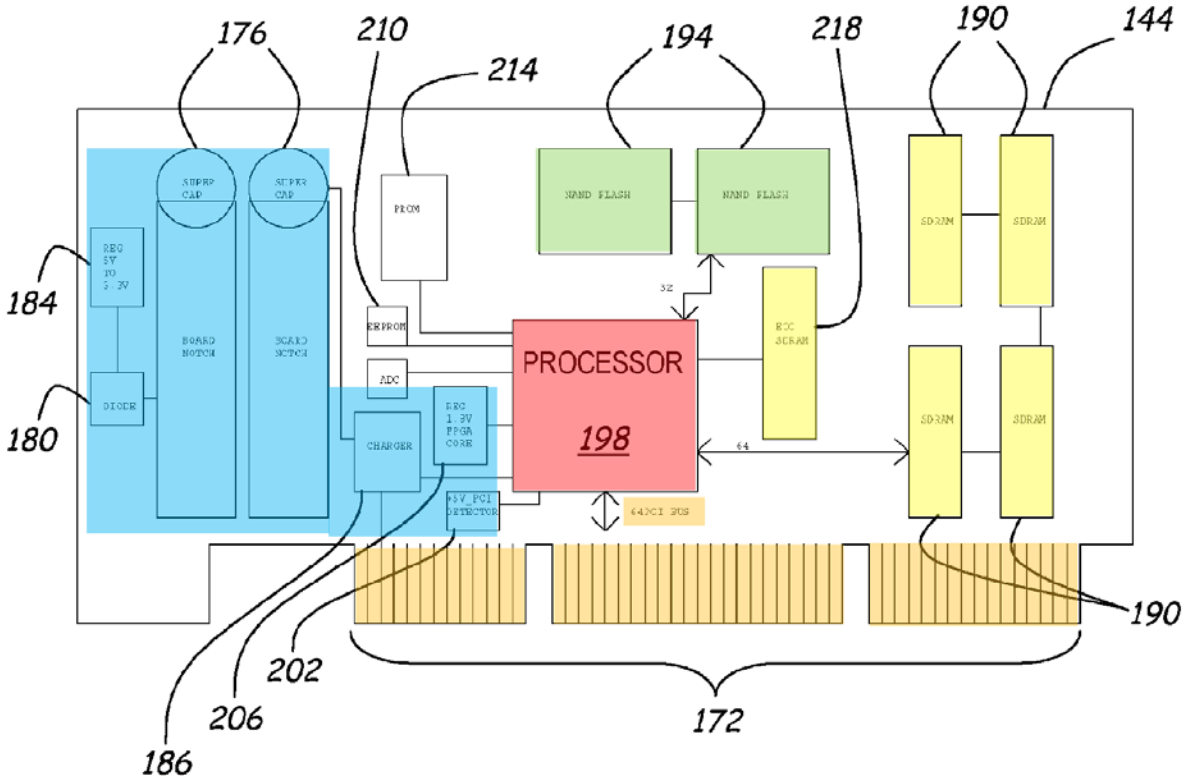
664. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages*."

(2) [1.d.2] Plurality of components including SDRAM devices

665. Claim 1 requires "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices*."

666. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

667. As discussed above for claim limitation [1.c], Spiers discloses "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices*." *Supra* ¶¶609-660; *see also* Ex. 1025 at [0036] ("The volatile memory 160, in one embodiment, is SDRAM utilized to store data from the storage controller 132 during typical write operations."), [0037-38] (describing SDRAMs 190 and 218 in Fig. 5), Fig. 5 (reproduced below and annotated).



668. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices*."

(3) [1.d.3] A first circuit coupled to the SDRAM devices and first set of edge connections

669. Claim 1 requires "*a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections*."

670. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

671. As discussed above for claim limitation [1.b], Spiers satisfies "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system*." *Supra* ¶¶601-608.

672. Spiers discloses processor 198 ("*a first circuit*") that is coupled between a first portion of the plurality of edge connections in PCI connector 172 and the plurality of SDRAM devices 190 and 218. *See, e.g.*, Ex. 1025 at Fig. 5, [0037] ("A FPGA processor 198 that provides PCI interfacing through a 64-bit PCI bus, is connected to the SDRAM modules 190 through a 64-bit bus, and is connected to the NAND flash modules 194 through a 32-bit bus"); *see also* Ex. 1031 at p.1 ("The PCI Local Bus is a high performance 32-bit or 64 bit bus with multiplexed address and data lines"), p.7 (Fig. 2-1, reproduced below, describing PCI pins AD for address and data signals and pins C/BE for bus control signals).

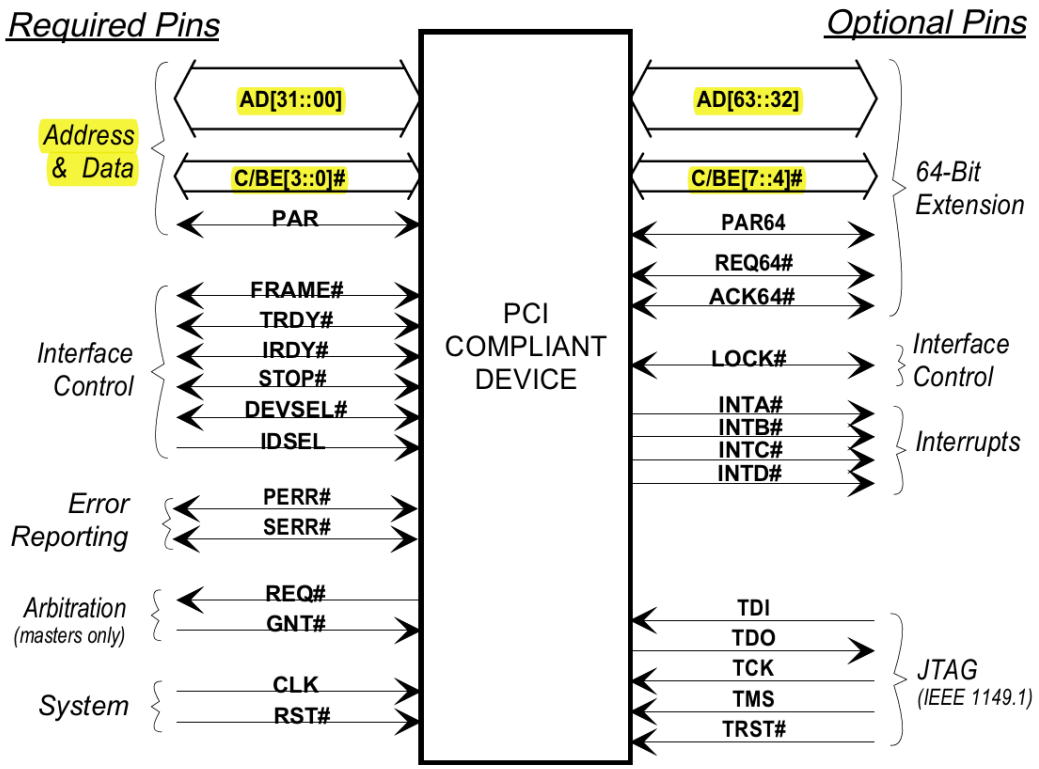


Figure 2-1: PCI Pin List

See also id. at p.21 (listing C/BE commands, including commands for read and write operations), p.172 (showing edge connections of 5V/64-bit PCI bus).

3.1.1. Command Definition

PCI bus command encodings and types are listed below, followed by a brief description of each. Note: The command encodings are as viewed on the bus where a "1" indicates a high voltage and "0" is a low voltage. Byte enables are asserted when "0".

C/BE[3::0]#	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

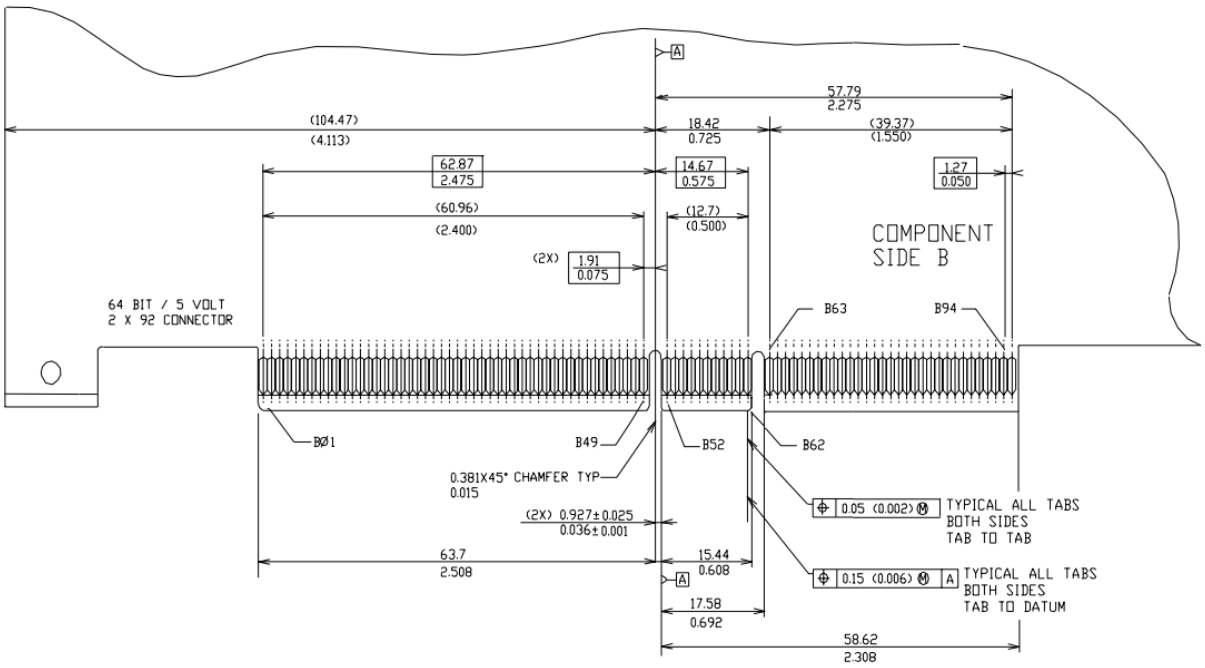


Figure 5-27: 5V/64-bit Card Edge Connector Dimensions and Tolerances

673. Accordingly, the prior art references in each of Grounds 4 and 5 "*a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections*."

(4) [1.d.4] Wherein the first circuit is coupled to first and second regulated voltages

674. Claim 1 requires "*wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages*."

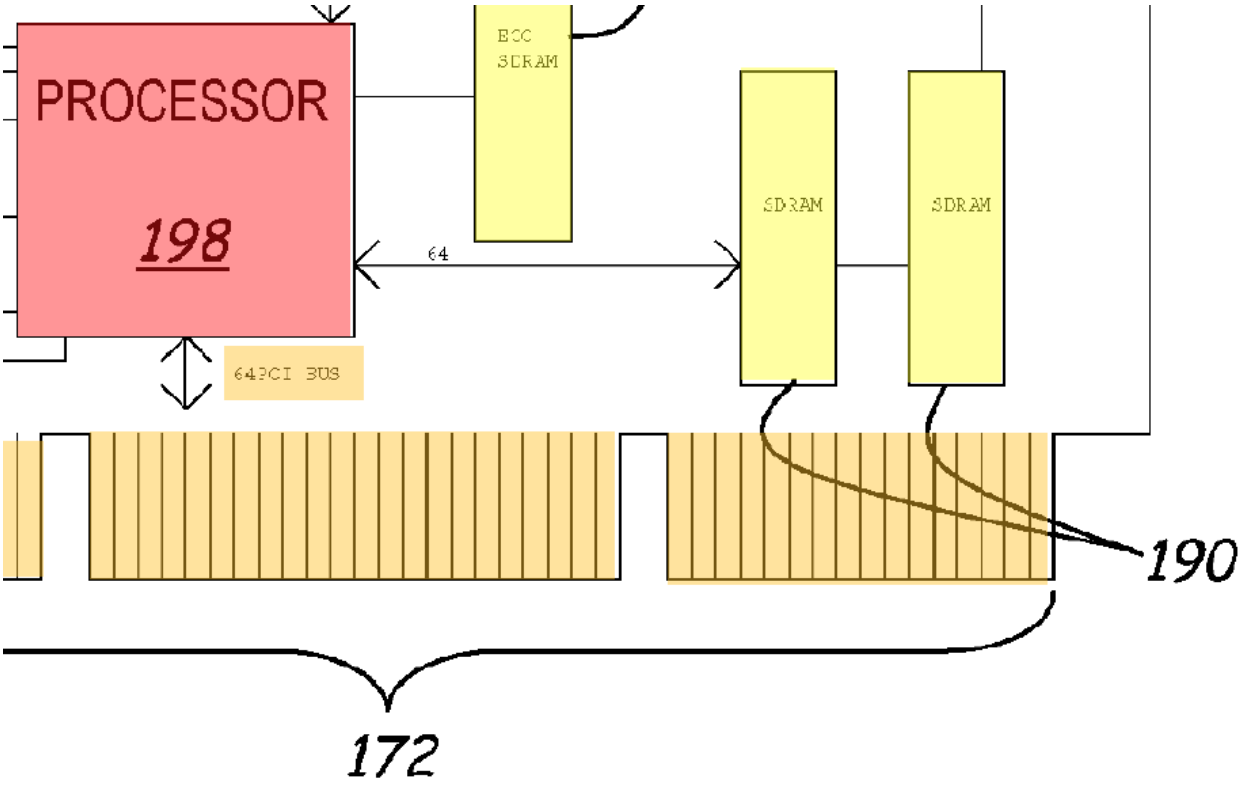
675. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

676. As explained above, the prior art references in each of Grounds 4 and 5 satisfy "*a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages*." *Supra* ¶¶609-660. For the reasons discussed above with reference to claim element [1.c], in each voltage mapping of Grounds 4 and 5, Spiers discloses to a Skilled Artisan that the processor 198 (i.e., "*the first circuit*") is coupled to a "*first regulated voltage*," for example, VDD/VDDQ of the SDRAMs in order to communicate with those memories, and a "*second regulated voltage*," for example, VCCFPGA for the FPGA core. *See id.*

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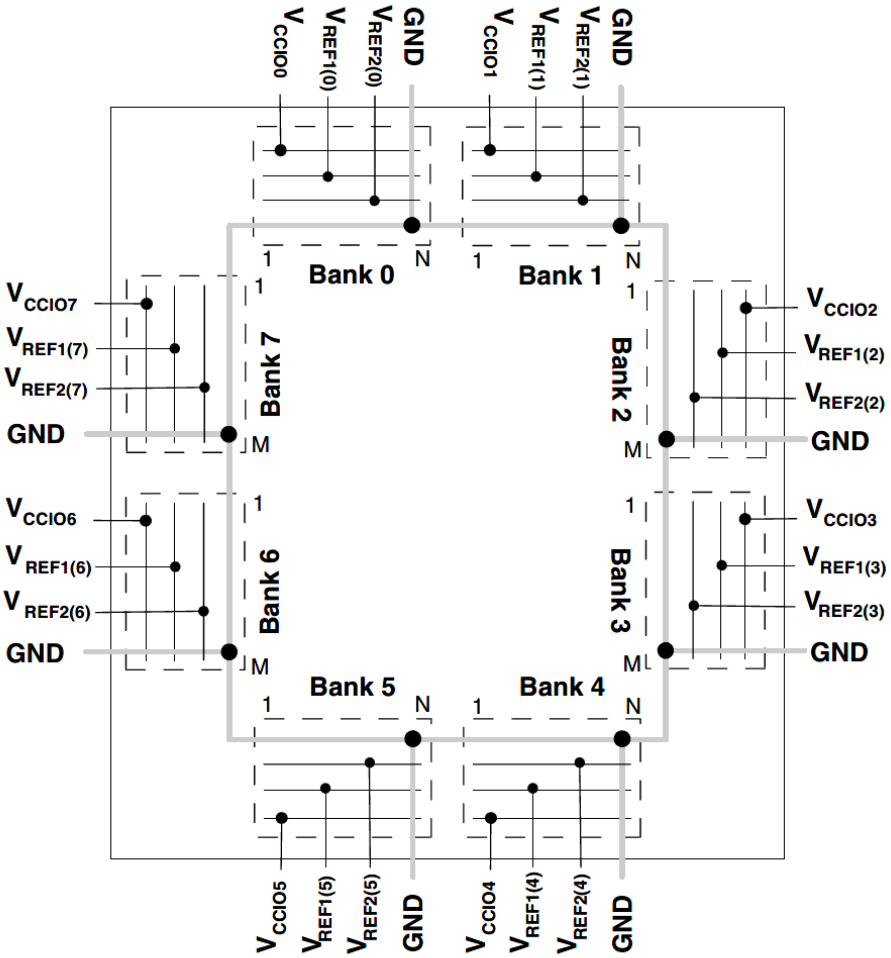
677. For example, Spiers discloses that its processor 198 receives a supply voltage for its FPGA core. Ex. 1025 at [0037] ("The FPGA processor receives power through a voltage regulator 206, which regulates the voltage required for the FPGA core"). Spiers also discloses that its processor 198 interfaces with the SDRAM devices. *Id*. ("A FPGA processor 198 that provides PCI interfacing through a 64-bit PCI bus, is connected to the SDRAM modules 190 through a 64-bit bus, and is connected to the NAND flash modules 194 through a 32-bit bus.").

678. A Skilled Artisan would have understood from this disclosure of Spiers that processor 198, like the AMB in the FBDIMM standards, receives the same VDD/VDDQ voltage as the SDRAMs in order to interface with the SDRAMs. *See, e.g.*, Ex. 1025 at Fig. 5 (reproduced below in part, showing a 64-bit bus between the processor 198, red, and the SDRAMs 190, yellow).



679. Indeed, a Skilled Artisan would have understood at the time that FPGAs, like the FPGA processor 198 of Spiers, were configured to receive a separate voltage to interface with devices that use a voltage for communication other than the FPGA core. *See*, *e.g.*, Ex. 1067 (LatticeXP FPGA datasheet), 2-23 (Fig. 2-27, reproduced below showing separate voltages VCCIO0-VCCIO7, one for each interface of the FPGA); 2-24 through 2-25 (Table listing different communication standards supported by the FPGA).

Figure 2-27. LatticeXP Banks



Note: N and M are the maximum number of I/Os per bank.

680. To the extent one might argue that Spiers does not sufficiently disclose that processor 198 receives the power supply (VDD/VDDQ) that is used by the SDRAMs to communicate data, it would have been obvious. A Skilled Artisan would have understood from the JEDEC standards that SDRAM devices require certain voltages for communicating data. *See, e.g.*, Ex. 1045 at pp.7, 54 (describing VDDQ as power supply for input/output); Ex. 1026 (JESD79-2B) at pp.6, 49 (same); Ex. 1046 at pp.10, 114 (same). Spiers discloses that the data is

transferred to and from the SDRAM devices through processor 198. *See, e.g.*, Ex. 1025 at [0037] ("A FPGA processor 198 that provides PCI interfacing through a 64-bit PCI bus, is connected to the SDRAM modules 190 through a 64-bit bus…."). Therefore, a Skilled Artisan would have been motivated to provide the proper voltages, including VDD/VDDQ, to processor 198 to communicate data to and from the SDRAM memory devices.

681. A Skilled Artisan would have also understood that devices which interface with SDRAM devices also received the VDD/VDDQ voltage of the SDRAMs in addition to their own power supply of VCC in order to meet the specific SDRAM voltage requirements for signaling. *See, e.g.*, Ex. 1026 (JESD79-2B) at 49-91 (AC & DC operating conditions); Ex. 1046 (JESD79-3A) at 100-126 (Chapters 7-9, including AC & DC Operating Conditions, AC and DC Input Measurement Levels, AC and DC Output Measurement Levels); Ex. 1067 (LatticeXP FPGA datasheet), 2-23 (Fig. 2-27, reproduced above showing separate voltages VCCIO0-VCCIO7, one for each interface of the FPGA); 2-24 through 2-25 (Table listing different communication standards supported by the FPGA); Ex. 1027 at pp.7, 29 (describing a power supply of an AMB as "I/O buffer voltage for DDR2 buffers" and "Supply voltage DRAM Interface"). Implementing such an SDRAM interface in processor 198 was well within the level of skill at the time, as FPGA's were allowed to receive different supply voltages for output. *See, e.g.*, Ex.

1067 (LatticeXP FPGA datasheet), 2-23 through 2-25 (programming interfaces of commercially available FPGA according to different voltage requirements); Ex. 1042 at p.2 (showing different FPGAs and their power requirements, allowing output drive voltages in the range of 1.2V to 3.3V).

682. Therefore, this limitation would have been at least obvious to a Skilled Artisan.

683. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages*."

(5) [1.d.5] Wherein the SDRAM devices are coupled to the first regulated voltage

684. Claim 1 requires "*wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages*."

685. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

686. For the reasons discussed above with reference to claim limitation [1.c], Spiers's discloses that the SDRAM devices 190 and 218 are coupled to the "*first regulated voltage*" VDD/VDDQ. *Supra* ¶¶609-660.

687. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages*."

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2. Claim 2 is Unpatentable

688. Claim 2 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mapping A) render the claim obvious

a) [2.a] Wherein the First and Second Regulated Voltages Have Respective First and Second Voltage Amplitudes

689. Claim 2 requires "*[t]he memory module of claim 1, wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude*."

690. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

691. As explained above with reference to claim limitation [1.c], Spiers discloses that the "*first regulated voltage*" is VDD, which has a "*first voltage amplitude*" of, for example, 1.5V for DDR3 (Voltage Mapping A of Grounds 4 and 5). *Supra* ¶¶609-660.

692. As also explained above for claim limitation [1.c], for each Voltage Mapping in Grounds 4 and 5, Spiers discloses that the "*second regulated voltage*" is VCCFPGA, which has a "*second voltage amplitude*" of, for example, 1.8V, which is different from the "first voltage amplitude" such as 1.5V for DDR3 (Voltage Mapping A of Grounds 4 and 5). *Supra* ¶¶609-660.

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693. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude*" limitation.

b) [2.b] Wherein One of the First and Second Voltage Amplitudes is Less Than the Other

694. Claim 2 requires "*wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes*."

695. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

696. As explained above with reference to claim limitations [1.c] and [2.a], for Voltage Mapping A of Grounds 4 and 5 the "*first voltage amplitude*" is 1.5V (VDD to DDR3 DRAM) and the "*second voltage amplitude*" is 1.8V (VCCFPGA to FPGA Core). *Supra* ¶¶609-660 (claim limitation [1.c]); ¶¶689-693 (claim limitation [2.a]). Thus, the *first voltage amplitude* (1.5V) is less the *second voltage amplitude* (1.8V).

697. Accordingly, the prior art references in each of Grounds 4 and 5 (Voltage Mapping A) satisfy the "*wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes*" limitation.

3. Claim 3 is Unpatentable

698. Claim 3 is unpatentable as the prior art references in Grounds 4 and 5 (Voltage Mapping B) render the claim obvious.

699. Claim 3 requires "*[t]he memory module of claim 1, wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts*."

700. The prior art references in Grounds 4 and 5 teach this limitation to a Skilled Artisan.

701. As discussed above with reference to claim limitation [1.c], for Voltage Mapping B of Grounds 4 and 5, Spiers discloses to a Skilled Artisan that the "*third regulated voltage*" can be mapped to VDDL that is provided to the SDRAMs separately from VDD and VDDQ, which has a voltage amplitude of 1.8V for DDR2 SDRAMs. *Supra* ¶¶609-660.

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Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

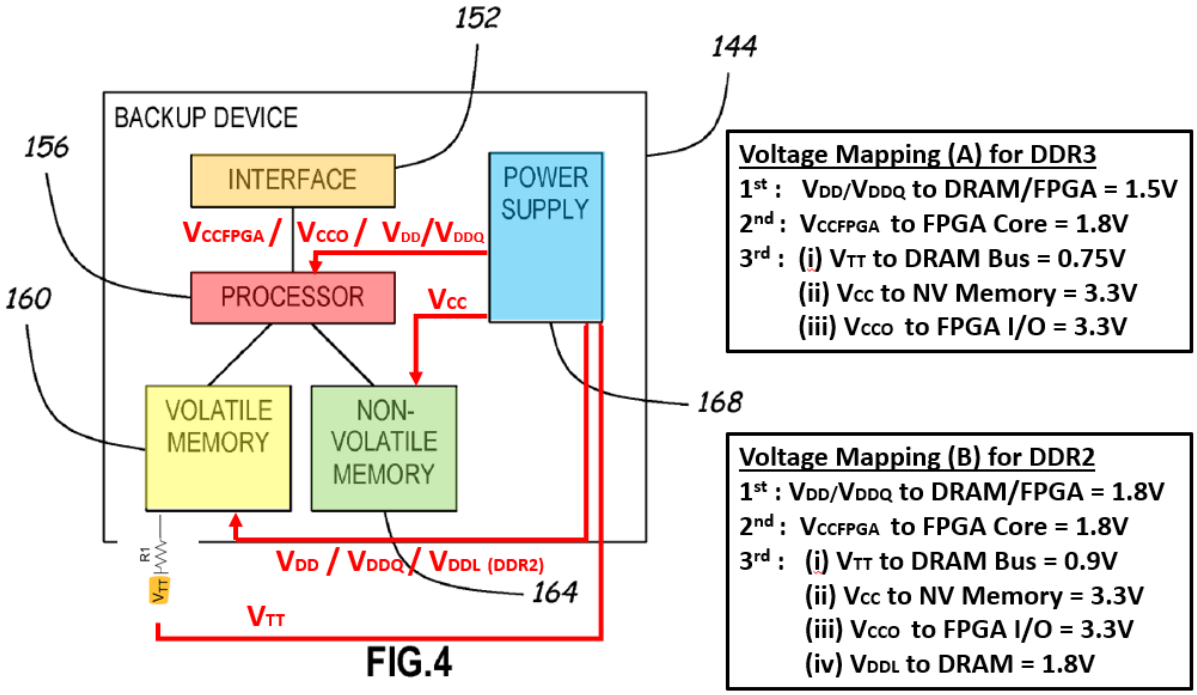


FIG.4

See Ex. 1025 at Fig. 4 (annotated). For example, the DDR2 standard expressly suggests to a Skilled Artisan to use a power source for VDDL that is separate from the voltage source(s) for VDD and VDDQ. JESD79-2B at p.2 (NOTE 5) and pp.6-7 (reproduced below, annotated).

NOTE 5 VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ

NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**

Symbol	Type	Function
V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

See also id. at p.9 (disclosing order for applying VDDL separately from VDD and VDDQ; reproduced below, annotated).

a) Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.) The power voltage ramp time must be no greater than 20mS; and during the ramp, VDD>VDDL>VDDQ and VDD-VDDQ<0.3 volts.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2.

or

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

at least one of these two sets of conditions must be met.

702. To the extent the amplitude of the "*third regulated voltage*" must be different than the amplitude of the "*first*" and "*second*" regulated voltages, the above Voltage Mapping A can be modified such that the "*third regulated voltage*" can be V_{CCFPGA} of 1.8V to the FPGA core and the "*second regulated voltage*" can be V_{CCO} of 3.3V to the interface of Spiers's processor (156/198) with the non-volatile memory (164/194). As required by claim limitations [1.d.4] and [1.d.5], the "*first regulated voltage*" of VDD/VDDQ=1.5V (for DDR3) is coupled to the SDRAMs (164/190) and to the processor (156/198), and the "*second regulated voltage*" of V_{CCO}=3.3V is also coupled to the processor (156/198). *Supra* ¶¶609-660.

703. Therefore, for this modified Voltage Mapping A of Grounds 4 and 5, V_{CCFPGA} to the FPGA core with a voltage amplitude of 1.8V can be considered as the "*third regulated voltage*," rendering this claim invalid.

704. Accordingly, the prior art references in Grounds 4 and 5 satisfy the "*wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts*" limitation.

4. Claim 4 is Unpatentable

705. Claim 4 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [4.a] Preamble

706. The preamble of claim 4 requires "*[t]he memory module of claim 1, further comprising*."

707. As explained above for claim 1, the prior art references in each of Grounds 4 and 5 satisfy the limitations of claim 1. *Supra* ¶¶594-687.

708. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory module of claim 1, further comprising*."

b) [4.b] Voltage Monitor Circuit

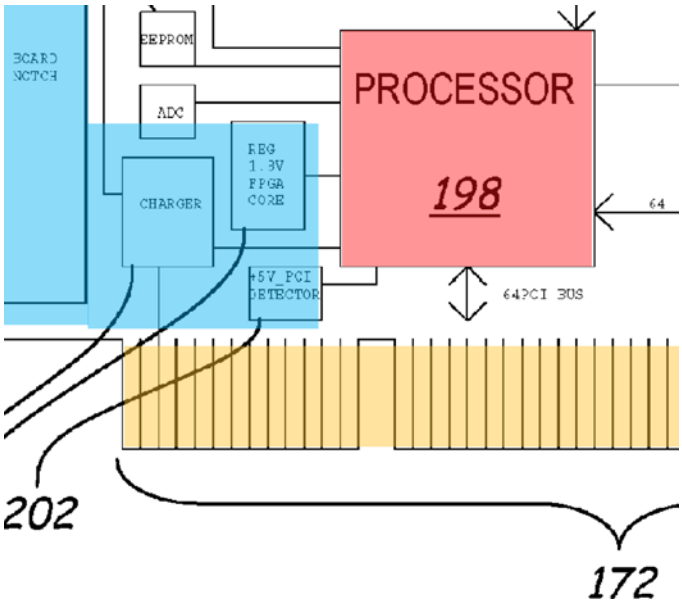
709. Claim 4 requires "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger*

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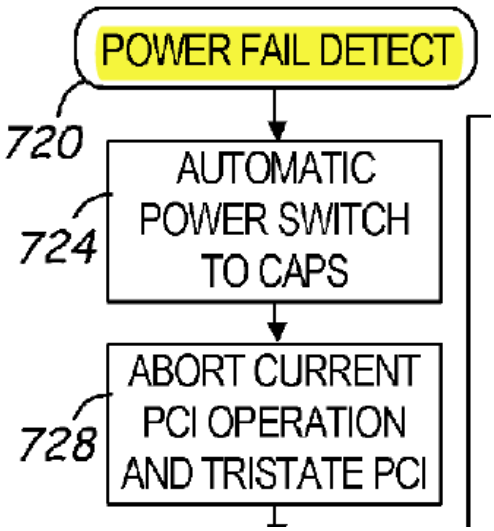
signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage."

710. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

711. It would have been obvious to a Skilled Artisan that the prior art in each of Grounds 4 and 5 teaches and discloses "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections*." Spiers discloses a power detection circuit 202 ("*a voltage monitor circuit*") coupled to the PCB and a second set of edge connections that is configured to monitor the +5 volt supply voltage at a +5 volt pin of PCI connector 172 ("*an input voltage received from the second set of edge connections*"). *See* Ex. 1025 at Figs. 5, 14 (reproduced below in part, annotated), [0037] ("The FPGA processor 198 utilizes a power detection circuit that, in this embodiment, is a +5V PCI detector 202."), [0054] ("Referring now to FIG. 14, the operational steps performed by the backup device upon detection of a power failure are now described. As discussed previously, the backup device monitors the primary power supply. In the PCI card embodiment, this monitoring is performed by monitoring the voltage at a +5 volt pin.").



Ex. 1025 at Fig. 5 (excerpted and annotated).



Id. at Fig. 14 (excerpted and annotated).

712. A Skilled Artisan would have understood that a PCI bus includes "*a second set of edge connections*" that carry the +5V power supply. *See*, *e.g.*, Ex.

1031 at p.149 (showing that the number of pins carrying the +5V supply in a PCI card, reproduced below).

Table 4-14: Pin Summary - 32-bit Expansion Board

Pin Type	5V Board	Universal Board	3.3V Board
Ground	22	18 (Note)	22 (Note)
+5 V	13	8	8
+3.3 V	12	12	17
I/O pwr	0	5	0
Reserv'd	4	4	4

NOTE:

If the **M66EN** pin is implemented, the number of ground pins for a Universal board is 17 and the number of ground pins for a 3.3V board is 21.

Table 4-15: Pin Summary - 64-bit Board (incremental pins)

Pin Type	5V Board	Universal Board	3.3V Board
Ground	16	16	16
+5 V	6	0	0
+3.3 V	0	0	6
I/O pwr	0	6	0
Reserv'd	5	5	5

713. Therefore, Spiers discloses "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections*" to a Skilled Artisan.

714. In addition, it would have been obvious to a Skilled Artisan that the prior art in each of Grounds 4 and 5 teaches "*the voltage monitor circuit* [is] *configured to produce a trigger signal in response to the input voltage having a*

voltage amplitude below a predetermined threshold voltage." Spiers alone and in view of Amidi renders obvious to a Skilled Artisan that the +5V voltage detector 202 is "*configured to produce a trigger signal*" to switch power to capacitors and disconnect from the PCI bus "*in response to the input voltage having a voltage amplitude below a predetermined threshold voltage*," indicating an anomaly in the external power source. *See* Ex. 1025 at Figs. 5, 14 (reproduced above in part, annotated).

715. For example, Spiers explains that, "[i]nitially, at block 720, a power failure is detected. At block 724, the backup device processor switches the power to the capacitors. At block 728, the processor aborts any current PCI operation and tristates the PCI." Ex. 1025 at [0054]. A Skilled Artisan would have understood from Spiers's disclosure that the voltage monitor circuit 202 produces a "*trigger signal*" when it detects a power failure. The backup device processor (198, red) receives this "*trigger signal*" (*see* connection between voltage detector 202 (blue) and processor 198 (red)), switches the power source from the PCI connector pin to the capacitors, and disconnects ("tristates") the PCI bus. *See id.* at Fig. 5 (reproduced above in part, annotated).

716. Spiers further describes the function of its "+5V PCI detector 202." In particular, Spiers discloses that the "FPGA processor 198 utilizes a power detection circuit" such as "+5V PCI detector 202." Ex. 1025 at [0037]. In relation

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to the detector, Spiers explains that "[t]he non-volatile memory 164 . . . is utilized in the event of a power failure detection." *Id.* at [0036]. Although Spiers does not expressly disclose the details of how that function is performed, a Skilled Artisan would have understood that such a voltage detector operation includes comparing the input voltage to a "*predetermined threshold voltage*." *See, e.g.*, Ex. 1024 at Fig. 6 (disclosing a voltage supervisory block 665 comparing the system supply voltage 605 to a reference voltage 675, defining a threshold, and generating a "trigger signal" 670 as a result of the comparison).

717. A Skilled Artisan would have also understood, and it would have been at least obvious to her, that Spiers's "+5V PCI detector 202" can detect a power failure when the input voltage is outside of a preset interval about +5V, defined by an upper and a lower limit, which the backup device 144 can tolerate without losing data or damaging the circuits. *See, e.g.*, Ex. 1023 at [0013] ("Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated.").

718. For example, U.S. Patent Publication No. 2009/0034354 to Resnick ("Resnick") describes generating "an alarm signal if the difference between the operating voltage and the reference voltage indicates the operating voltage is outside of a normal operating range" for a memory device. Ex. 1065 at Abstract,

[0014], Fig. 1. Resnick describes that the alarm signal is generated when "the operating voltage [is] above an upper threshold or below a lower threshold." *Id.* at Fig. 5 (block 530). Resnick explains that a "voltage sensor 110 may be configured to signal an alarm in the case where the operating voltage is outside of a range" which relates to the "magnitude of the voltage [going] beyond a predetermined threshold level, which may be an upper or lower level relative to an expected, or normal operating voltage." *Id.* at [0018]. Further, "[i]f the operating voltage is above or below the relevant threshold, voltage sensor 110 may indicate the voltage failure by sending a flag such as alarm signal 112 to a pin on semiconductor memory device 100 for signaling the alarm externally." *Id.* at [0019]; *see also id.* at [0031], [0033], Figs. 1-3. Thus, by way of example, Resnick shows that, at the time, a Skilled Artisan would have understood that a voltage detection circuit could be implemented to detect different types of anomalies on a memory module, including the amplitude of the voltage going above or below predetermined levels, and to indicate a voltage failure by sending a flag such as an alarm signal.

719. Similarly, Hajeck discloses a voltage detection circuit 48 which monitors an input voltage to a memory module for both under-voltage and over-voltage anomalies. *Supra* at ¶138; Ex. 1038 at Fig. 1.

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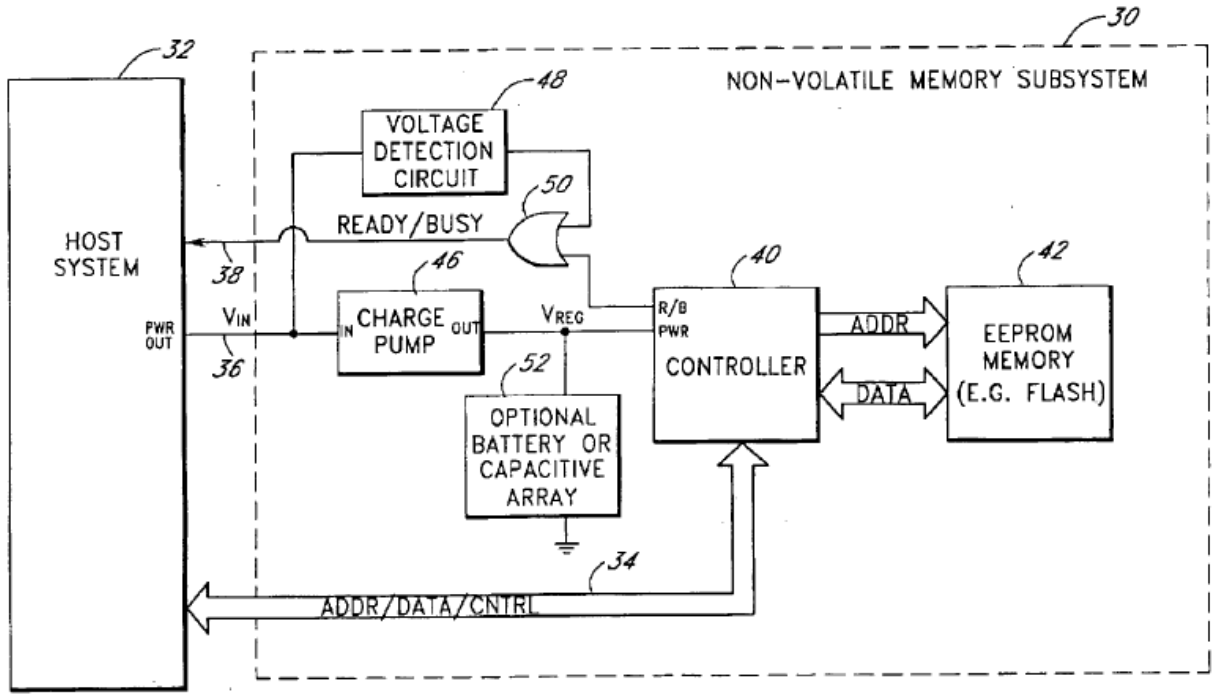


FIG. 1

Hajeck explains that a "conventional voltage detection circuit" is "responsible for detecting anomalies in the power signal V_{IN}," including "whenever V_{IN} falls below a certain level" and "when the voltage exceeds a certain level." *Id.* at 3:30-39. Therefore, a Skilled Artisan would have understood that conventional voltage detection circuits monitored over-voltage and under-voltage conditions.

720. As another example, a National Semiconductor datasheet for LMC6953, a PCI Local Bus Power Supervisor, describes a voltage monitor circuit for PCI cards like Spiers's and discloses an under-voltage threshold of 4.4 volts for

a 5-volt power supply. *See* Ex. 1063 at 1-2 (reproduced below and annotated for both over-voltage and under-voltage).

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

721. As yet another example, an Analog Devices datasheet for ADM1066 describes programmable circuits to "detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out-of-window fault (undervoltage or overvoltage)." Ex. 1061 at 15; *see also* Ex. 1062 at 15 ("Two comparators are dedicated to each input so that undervoltage and overvoltage detection can be implemented . . . .").

722. Accordingly, it would have been obvious for a Skilled Artisan to implement Spiers's "+5V PCI detector 202" to detect voltage anomalies and switch to the backup power based on detection of an undervoltage or overvoltage

condition. As described above, implementing Spiers's +5V PCI detector 202 in this manner was well within the level of skill at the time. *See, e.g.*, Ex. 1024 (Amidi) at 5:35-43, 8:23-29, 9:8-12, Figs. 6, 14; Ex. 1065 at Abstract, [0014], [0018], Fig. 5 (block 530); Ex. 1063 at 1-2; Ex. 1061 at 15; Ex. 1062 at 15. Thus, Spiers alone and in view of Amidi renders obvious this limitation in view of the knowledge of a Skilled Artisan.

723. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage*."

c) [4.c] Wherein the memory module transitions from a first operable state to a second operable state

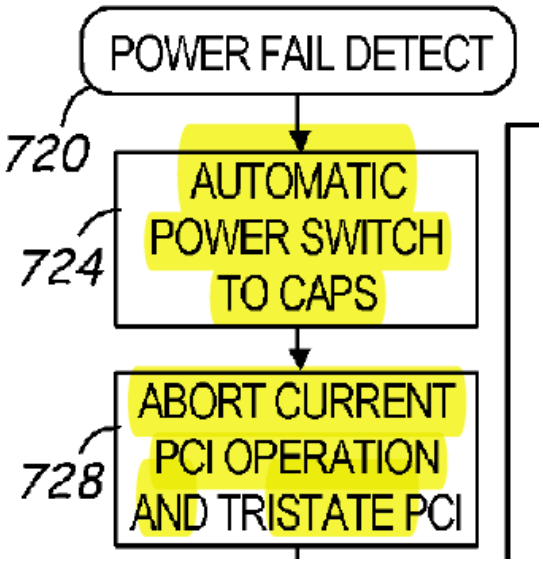
724. Claim 4 requires "*wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal*."

725. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

726. Spiers discloses that its memory module "*transitions from a first operable state*" that relies on the PCI +5V power "*to a second operable state*" that

disconnects the PCI bus and uses capacitor power for backup operations, including read and write operations for moving data from the volatile SDRAMs to the non-volatile NAND Flash memories, in response to the trigger signal indicating a power failure.

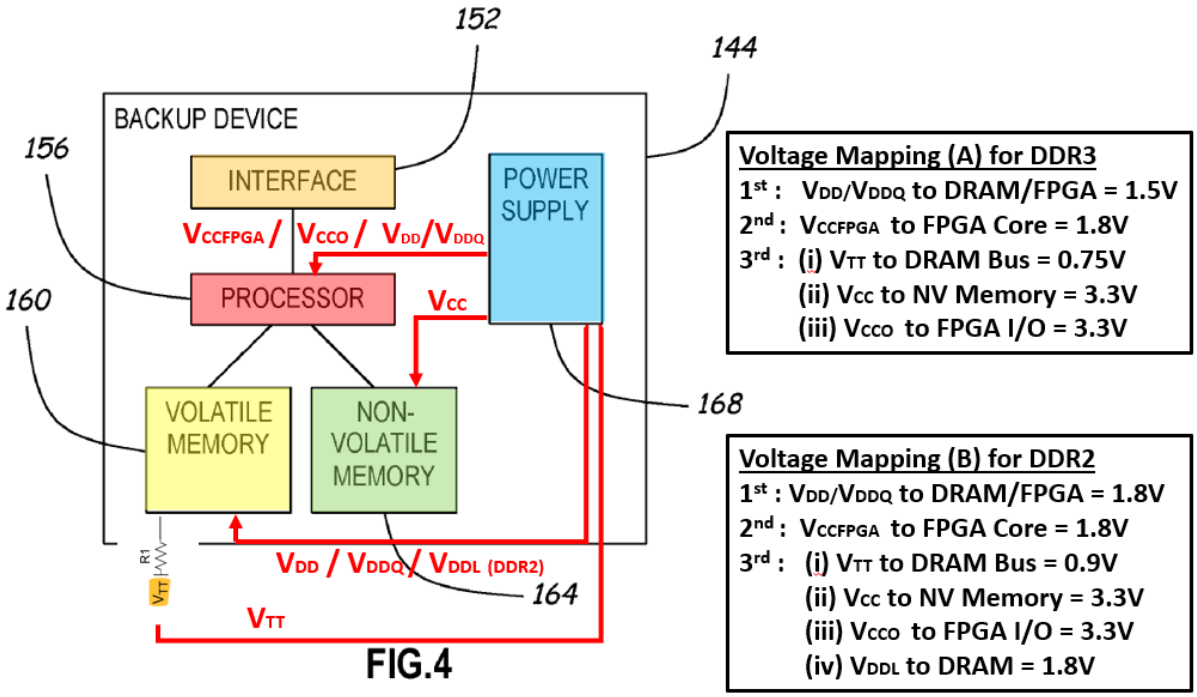
727. For example, Spiers discloses that, if a power failure is detected, the backup device processor switches the power from the PCI bus to the capacitors and "aborts any current PCI operation and tristates the PCI." Ex. 1025 at [0054], Fig. 14 (reproduced below in part, annotated).

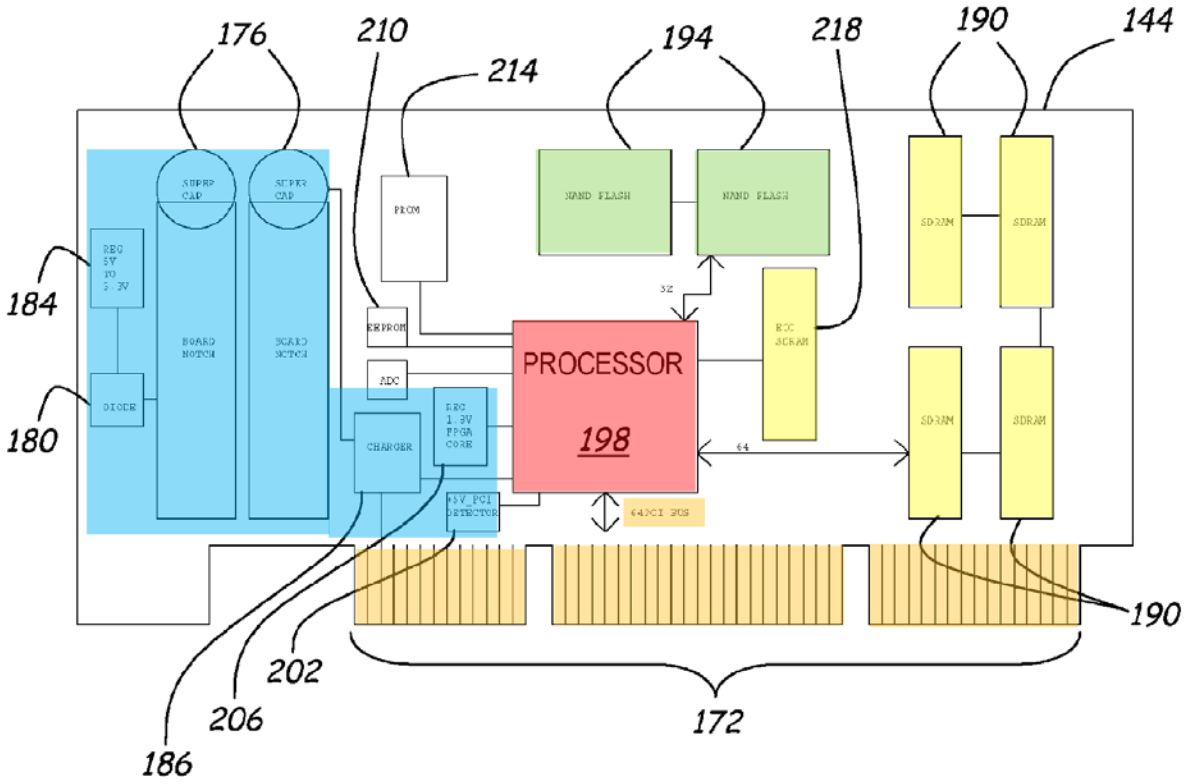


728. A Skilled Artisan would have also understood that the backup power from the capacitor is provided for the SDRAM, NAND Flash, and EEPROM devices of Spiers while data is transferred from the volatile SDRAM devices to the non-volatile NAND flash devices and corresponding information is stored in EEPROM 210. For example, Spiers discloses that "the backup device 144 includes

a volatile memory, and a non-volatile memory into which data is moved in the event of a power failure." Ex. 1025 at [0034]. Moreover, in this embodiment, the processor "upon detecting a power failure, switches the backup device 144 to the power supply 168, and moves the data in the volatile memory 160 to the non-volatile memory 164." *Id.* at [0036]. Spiers also describes that "in the event of a power failure the capacitors are used as the power source to power the backup device 144 when moving data from the volatile memory to the non-volatile memory." *Id.* at [0037]; *see also id.*, Fig. 4 (reproduced below, annotated), Fig. 6 (reproduced below, annotated).

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs





729. Annotated Figure 14 below depicts this data transfer process.

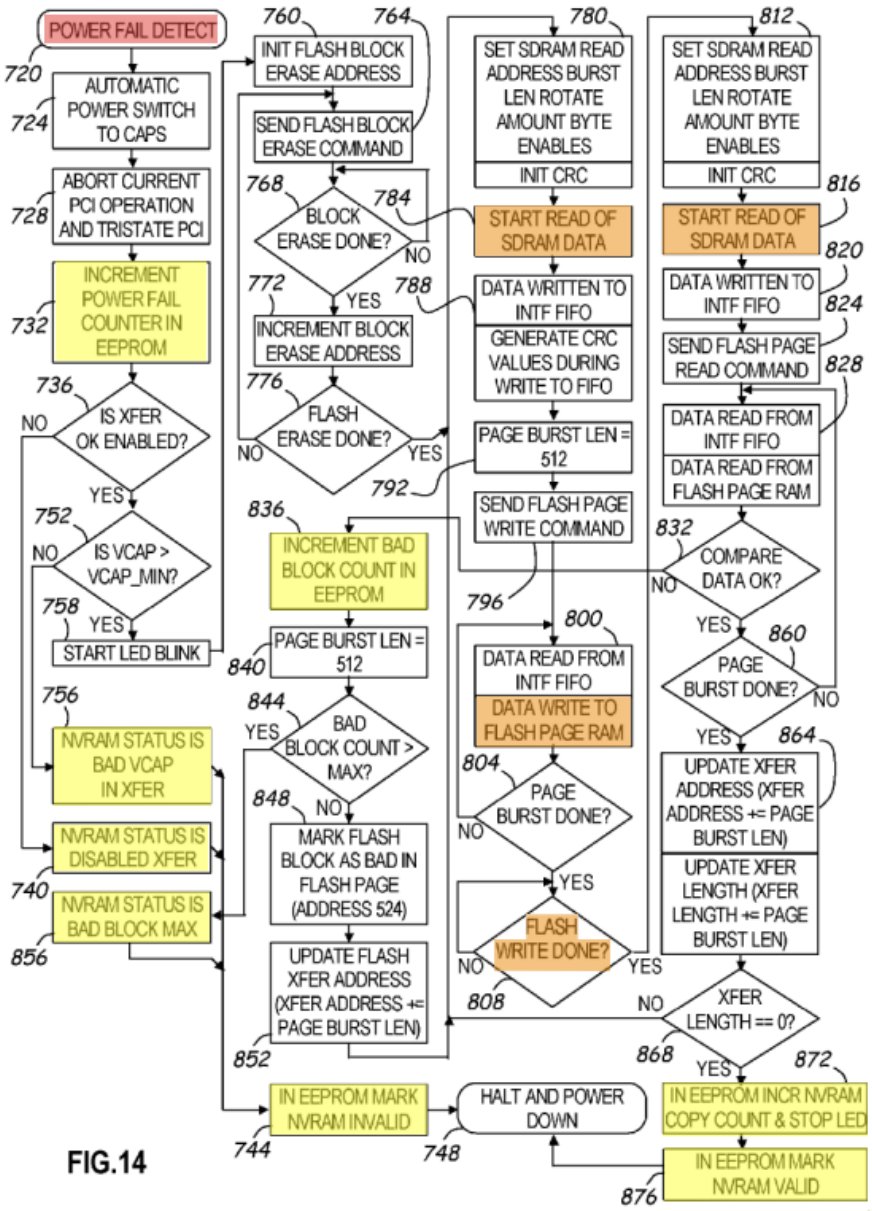


FIG.14

Id. at Fig. 14 (reproduced above with annotations, red indicating the power failure detection, yellow indicating examples of storing information in a non-volatile memory, and orange indicating data transfer from the volatile SDRAM devices to the non-volatile NAND flash devices); *see also id.* at [0054-56] ("The power fail counted in the EEPROM is incremented, according to block 732 … If the transfer

is not enabled, the NVRAM status is set as 'disabled transfer,' as noted at block 740. At block 744, the EEPROM is marked to indicate that the NVRAM is invalid . . .. At block 784, the backup device processor starts the read of SDRAM data. . .. At block 796, the backup device processor sends a flash page write command. The data is then read from the FIFO, and written to the flash page RAM, as noted by block 800….If the comparison indicates that the data is not the same, the backup device processor increments a bad block count in the EEPROM, at noted by block 836. …If the transfer length is zero, the backup device processor increments the NVRAM copy count in the EEPROM and stops the LED blink, as noted at block 872. At block 876, the backup device processor marks the EEPROM to indicate that the NVRAM is valid.")

730. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal*."

5. Claim 5 is Unpatentable

a) [5.a] Preamble

731. The preamble of claim 5 requires "*[t]he memory module of claim 4, further comprising*."

732. As explained above for claim 4, the prior art references in each of Grounds 4 and 5 satisfy the limitations of claim 4. *Supra* ¶¶705-730.

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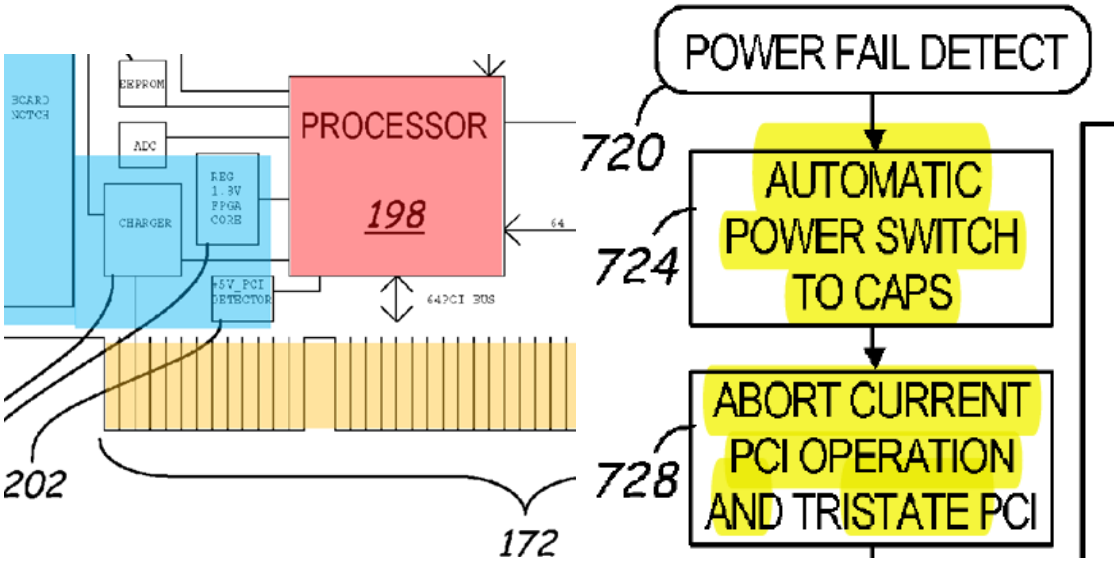
733. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory module of claim 4, further comprising*."

b) [5.b] Controller Coupled to the Voltage Monitor Circuit

734. Claim 5 requires "*a controller coupled to the voltage monitor circuit*."

735. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

736. Spiers discloses to a Skilled Artisan "*a controller*" including logic implemented in processor 198 to carry out operations in case of a power failure as discussed above for claim limitation [4.c] and with reference to Fig. 14. *Supra* ¶¶724-730; *see* Ex. 1025 at Fig. 14 (reproduced below in part, annotated). This controller is coupled to the +5V PCI detector (i.e., "*the voltage monitor circuit*"). *See* Ex. 1025 at Fig. 5 (reproduced below in part, annotated).



737. For example, Spiers explains that, "[i]nitially, at block 720, a power failure is detected. At block 724, the backup device processor switches the power to the capacitors. At block 728, the processor aborts any current PCI operation and tristates the PCI." Ex. 1025 at [0054]. A Skilled Artisan would have understood from Spiers's disclosure that the voltage monitor circuit 202 produces a "*trigger signal*" when it detects a power failure. The backup device processor (198, red) receives this "*trigger signal*" (*see* connection between voltage detector 202 (blue) and processor 198 (red)), switches the power source from the PCI connector pin to the capacitors, and disconnects ("tristates") the PCI bus. *See id.* at Fig. 5 (reproduced above in part, annotated).

738. Accordingly, the prior art references in each of Grounds 4 and 5 the "*a controller coupled to the voltage monitor circuit*" limitation.

c) [5.c] Wherein the Controller is Configured to Perform One or More Operations

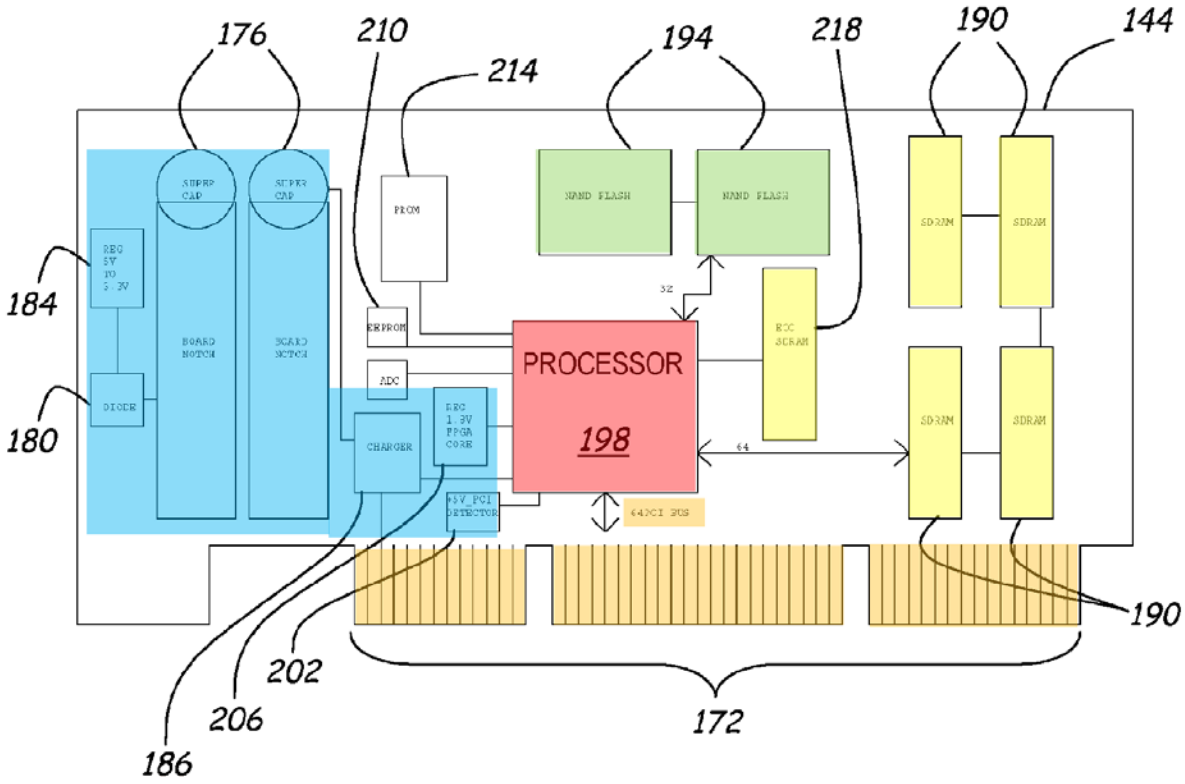
739. Claim 5 requires "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*."

740. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

741. As discussed above with reference to claim limitation [4.c], Spiers discloses that in response to an indication of power failure (i.e., "*the trigger*

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signal"), "*the controller,*" including logic implemented in processor 198 to carry out operations in case of a power failure as disclosed with reference to Fig. 14, is configured to move data from volatile SDRAMs (yellow) to non-volatile NAND Flash memory (green) (i.e., "*perform one or more operations including a write operation to transfer data to non-volatile memory*"). *Supra* ¶¶724-730.



Ex. 1025 at Fig. 5 (reproduced above, annotated); *see also id.* at Abstract ("The backup data storage device further includes a backup power source such as a capacitor, a battery, or any other suitable power source, and upon detection of a power interruption, switches to the backup power source and receives power from

the backup power source while moving the data from the backup volatile memory to the backup non-volatile memory.").

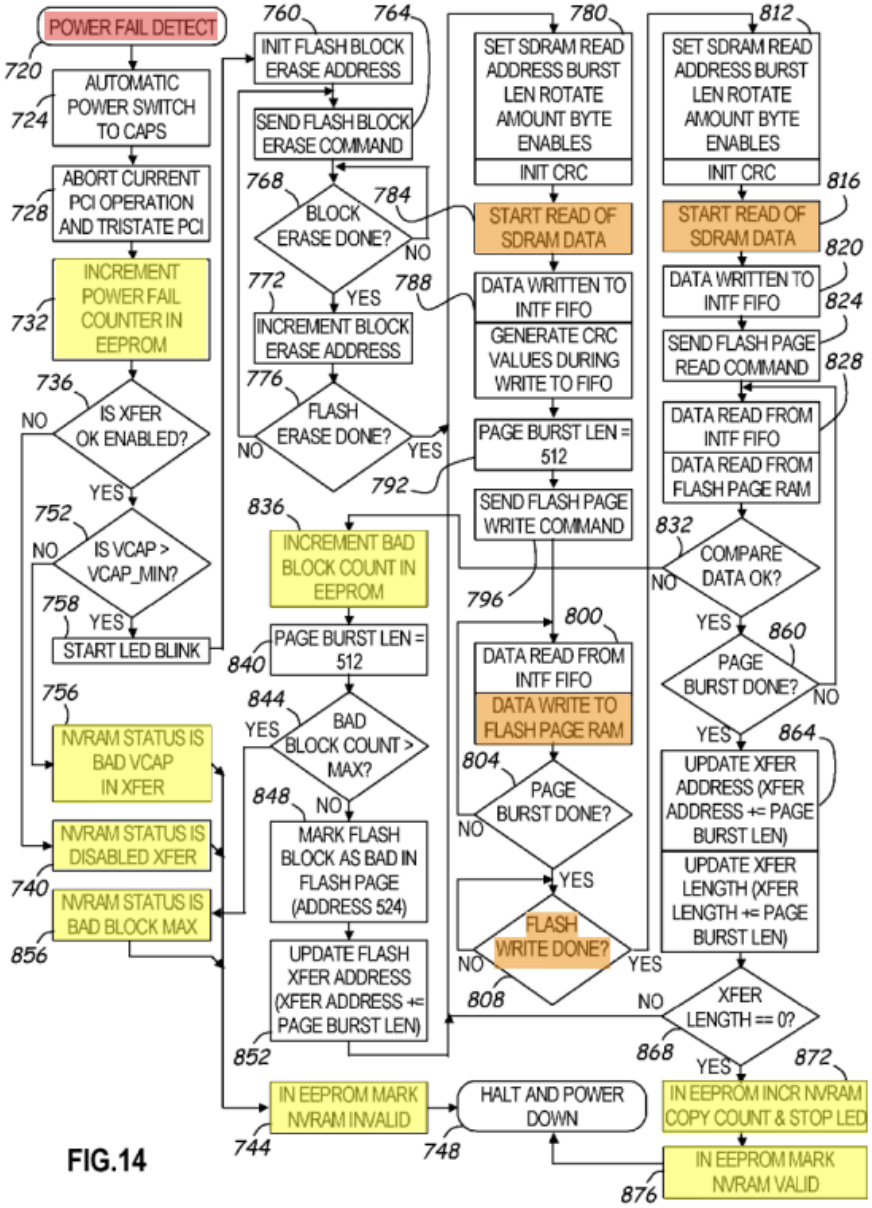


FIG.14

Annotated Figure 14 above depicts this data transfer process. *Id.* at Fig. 14 (reproduced above with annotations, red indicating the power failure detection, yellow indicating examples of storing information in a non-volatile memory, and

orange indicating data transfer from the volatile SDRAM devices to the non-volatile NAND flash devices); *see also id.* at [0055] ("At block 784, the backup device processor starts the read of SDRAM data. At block 788, the data is written to the data FIFO, and CRC values are generated during the write to the FIFO. At block 792, the page burst length is set to 512, indicating that 512 bytes of data are included in each page when writing to the NVRAM. At block 796, the backup device processor sends a flash page write command. The data is then read from the FIFO, and written to the flash page RAM, as noted by block 800.").

742. A Skilled Artisan would have understood that, through the "64-bit PCI bus," Spiers's module receives address and data with corresponding read or write commands to store or retrieve the user data. Ex. 1025 at [0037]; Ex. 1031 at 1 ("The PCI Local Bus is a high performance 32-bit or 64 bit bus with multiplexed address and data lines"), 7 (Fig. 2-1, reproduced below, describing PCI pins including AD pins for address and data and C/BE pins for bus control signals); *see also id*. at 21-25 (describing C/BE commands for read and write operations).

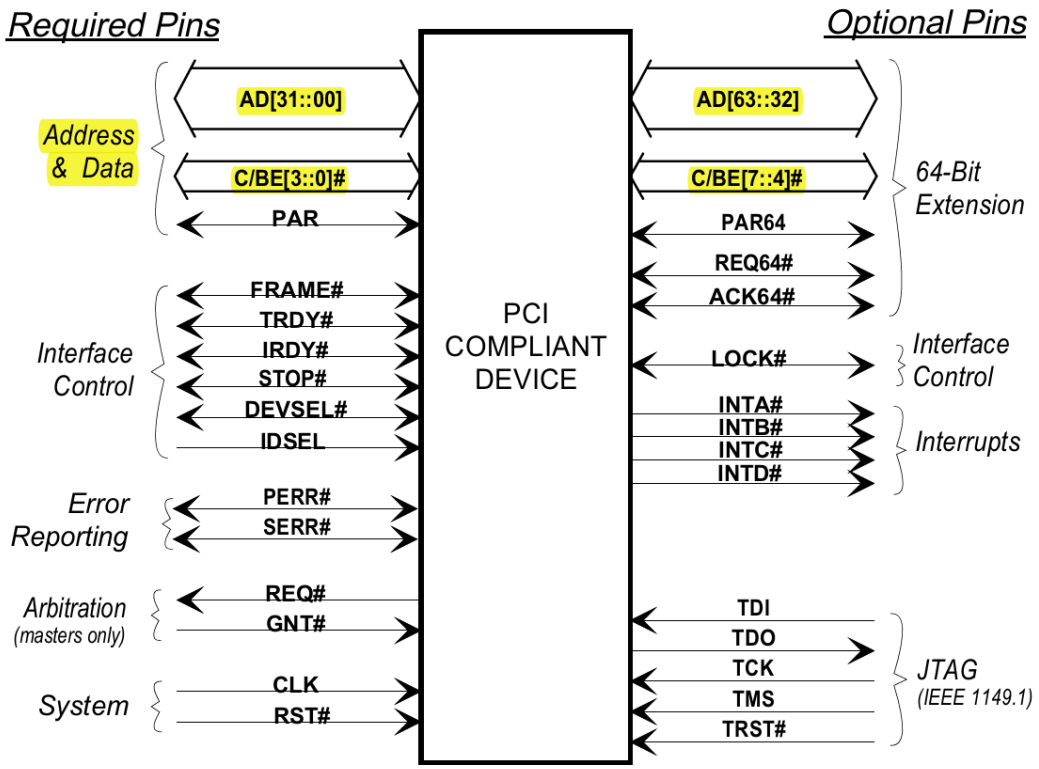


Figure 2-1: PCI Pin List

743. Spiers also discloses that "the backup device 144 utilizes a descriptor pointer queue contained within the FPGA processor 198 to receive commands from the storage controller." Ex. 1025 at [0039]; *see also id*. at Figs. 9, 10 and 11 (describing operational steps of the backup device processor when receiving commands and transferring data between the host memory and the SDRAMs on the module at corresponding addresses). Further, unlike devices that merely use a storage cache that cannot preserve data in the event of a failure, Spiers teaches that the backup device (144) includes both volatile and nonvolatile memory "into which data is moved in the event of a power failure." *Id.* at [0034]. Thus, Spiers alone and in combination with the references in Grounds 4 and 5 teaches that the

processor 198 (includes "*the controller*") performs write operations of user data to the NAND flash 194 ("*perform one or more operations including a write operation to transfer data to non-volatile memory*").

744. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*" limitation.

6. Claim 6 is Unpatentable

745. Claim 6 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [6.a] Preamble

746. The preamble of claim 6 requires "*[t]he memory module of claim 1, further comprising*."

747. As explained above for claim 1, the prior art references in each of Grounds 4 and 5 satisfy the limitations of claim 1. *Supra* ¶¶594-687.

748. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory module of claim 1, further comprising*."

b) [6.b] Voltage Monitor Circuit

749. Claim 6 requires "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second*

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set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage."

750. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

751. For the reasons discussed above with reference to claim limitation [4.b], the prior art references in each of Grounds 4 and 5 disclose and render obvious "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections*" to a Skilled Artisan. *Supra* ¶¶709-723.

752. In addition, as discussed above with reference to claim limitation [4.b], the prior art references in each of Grounds 4 and 5 render obvious to a Skilled Artisan that Spiers's +5V voltage detector 202 is "*configured to produce a trigger signal*" to switch power to capacitors and disconnect from PCI bus "*in response to the input voltage having a voltage amplitude above a predetermined threshold voltage*." *See id.*

753. As discussed above, a Skilled Artisan would have understood, and it would have been at least obvious to her, that Spiers's "+5V PCI detector 202" can detect a power anomaly when the input voltage is outside of a preset interval about

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+5V, defined by an upper and a lower limit, which the backup device 144 can tolerate without losing data or damaging the circuits. *Supra* ¶¶709-723; *see, e.g.*, Ex. 1023 at [0013] ("Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated").

754. Indeed, as previously discussed, in addition to undervoltage detection, implementing overvoltage detection was well within the level of skill of a Skilled Artisan at the time. *See supra* ¶¶709-723. For example, Resnick shows that, at the time, a Skilled Artisan would have been able to design a voltage detection circuit that detects different types of anomalies on a memory module, including the amplitude of the voltage going beyond a predetermined level, and that indicates a voltage failure by sending a flag such as an alarm signal. *See* Ex. 1065 (Resnick) at Abstract, [0014], [0018], [0031], [0033], Figs. 1-3, 5. As another example, a National Semiconductor datasheet for LMC6953, a PCI Local Bus Power Supervisor, describes a voltage monitor circuit for PCI cards like Spiers's and discloses an over-voltage threshold of 5.6 volts for a 5-volt power supply. *See* Ex. 1063 at 1-2 (describing both over-voltage and under-voltage). As yet another example, an Analog Devices datasheet for ADM1066 describes programmable circuits to "detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a

preprogrammed value), or an out-of-window fault (undervoltage or overvoltage)." Ex. 1061 at 15; *see also* Ex. 1062 at 15 ("Two comparators are dedicated to each input so that undervoltage and overvoltage detection can be implemented . . . .").

755. Accordingly, it would have been obvious for a Skilled Artisan to implement Spiers's "+5V PCI detector 202" to detect voltage anomalies and switch to the backup power based on detection of not only an undervoltage condition, but also an overvoltage condition. Thus, the prior art references in each of Grounds 4 and 5 renders obvious this limitation in view of the knowledge of a Skilled Artisan.

756. To the extent one might argue that overvoltage detection was not obvious in light of Ground 4, it would have been obvious in light of Hajeck, as part of Ground 5. As explained above, a Skilled Artisan would have been motivated to combine Ground 4 with Hajeck. *See supra* ¶¶208-213. Hajeck describes the operation of a "conventional voltage detection circuit." Ex. 1038 at 3:33-34; *see also id.* at Abstract, 1:62-2:7, 3:30-4:9. Hajeck discloses:

> "[A] voltage detection circuit 48 [that] is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line 36, and for driving the ready/busy signal to the 'busy' state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit 48 may be designed to generate a 'busy' signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. **The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected**. To inhibit rapid transitions between the 'ready' and 'busy' states, the **voltage detection circuit may be designed to provide a degree of**

> **hysteresis, and/or to hold its output for a particular time period after a state transition**."

Id. at 3:30-43 (emphasis added).

757. Thus, Hajeck shows that, at the time, a Skilled Artisan would have been able to design a voltage detection circuit that detects multiple types of anomalies, including when the voltage exceeds a certain level, and that provides hysteresis and holds its output for a period of time after a state transition. In light of Hajeck's and Amidi's teachings, a Skilled Artisan would have understood and been motivated to implement Spiers's "+5V PCI detector 202" to detect voltage anomalies and switch to the backup power not only if an undervoltage is detected, such as taught in Amidi (Ex. 1024 at 4:44-53 ("[i]f system supply 605 has a magnitude lower than reference voltage 675"), but also "when the voltage exceeds a certain level" as taught by Hajeck (Ex. 1038 at 3:30-40). Indeed, as discussed above, the problems caused by such overvoltage conditions, and solutions to detect and protect against them, were well known at the time. Accordingly, Skilled Artisan would have understood that, to avoid these well-known problems, Hajeck's "conventional voltage detection circuit" teachings on detecting both under- and over-voltage conditions were readily available at the time. Ex. 1038 at 3:30-40.

758. Accordingly, the prior art references in Ground 5 (Ground 4 in view of Hajeck) also satisfies "*a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage*

monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage."

c) [6.c] Wherein the Memory Module Transitions from a First Operable State to a Second Operable State

759. Claim 6 requires "*wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal*."

760. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

761. For the reasons discussed above with reference to claim limitation [4.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶724-730.

762. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal*."

7. Claim 7 is Unpatentable

763. Claim 7 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

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a) [7.a] Preamble

764. The preamble of claim 7 requires "[t]he memory module of claim 6, further comprising."

765. As explained above for claim 6, the prior art references in each of Grounds 4 and 5 satisfy the limitations of claim 6. *Supra* ¶¶745-762.

766. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "[t]he memory module of claim 6, further comprising."

b) [7.b] Controller Coupled to the Voltage Monitor Circuit

767. Claim 7 requires "*a controller coupled to the voltage monitor circuit*."

768. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

769. For the reasons discussed above with reference to claim limitation [5.b], Spiers discloses and renders obvious "*a controller coupled to the voltage monitor circuit*" to a Skilled Artisan. *Supra* ¶¶734-738.

770. Accordingly, prior art references in each of Grounds 4 and 5 satisfy the "*a controller coupled to the voltage monitor circuit*" limitation.

c) [7.c] Wherein the Controller is Configured to Perform One or More Operations

771. Claim 7 requires "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*."

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772. For the reasons discussed above with reference to claim limitation [5.c], Spiers discloses and renders obvious "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*" to a Skilled Artisan. *Supra* ¶¶739-744.

773. Accordingly, prior art references in each of Grounds 4 and 5 satisfy the "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*" limitation.

8. Claim 8 is Unpatentable

774. Claim 8 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [8.a] Preamble

775. The preamble of claim 8 requires "*[t]he memory module of claim 1, further comprising*."

776. As explained above for claim 1, the prior art references in each of Grounds 4 and 5 satisfy the limitations of claim 1. *Supra* ¶¶594-687.

777. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory module of claim 1, further comprising*."

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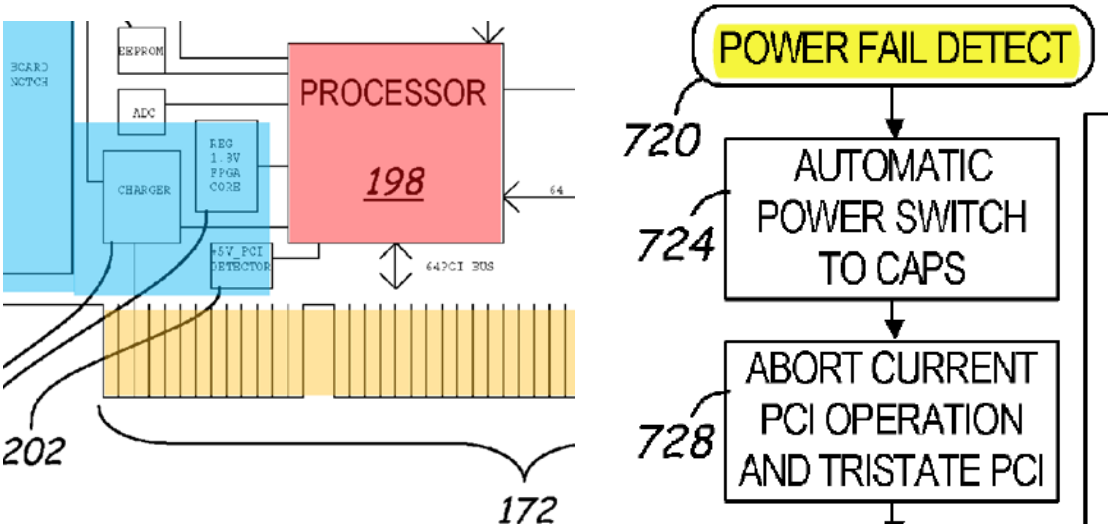
b) [8.b] A Controller, Including a Voltage Monitor Circuit, Coupled to the PCB

778. Claim 8 requires "*a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections*."

779. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

780. For the reasons discussed above with reference to claim limitations [4.b], [5.b], and [6.b], Spiers discloses and renders obvious "*a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections*" to a Skilled Artisan. *Supra* ¶¶709-723 (claim limitation [4.b]), ¶¶734-738 (claim limitation [5.b]), ¶¶749-758 (claim limitation [6.b]).

781. For example, Spiers discloses "*a controller*" including logic in processor 198 (red, below) and "*a voltage monitor circuit"* such as power detection circuit 202 (blue, below), both "*coupled to the PCB"* of the PCI card, the +5V PCI detector monitoring a +5V power received from the respective +5V PCI edge connections *"of the plurality of edge connections*" (orange, below).



Ex. 1025 at Figs. 5, 14 (reproduced above in part, annotated); *see also id.* at [0037] ("The FPGA processor 198 utilizes a power detection circuit that, in this embodiment, is a +5V PCI detector 202."), [0054] ("Referring now to FIG. 14, the operational steps performed by the backup device upon detection of a power failure are now described. As discussed previously, the backup device monitors the primary power supply. In the PCI card embodiment, this monitoring is performed by monitoring the voltage at a +5 volt pin.").

782. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections*."

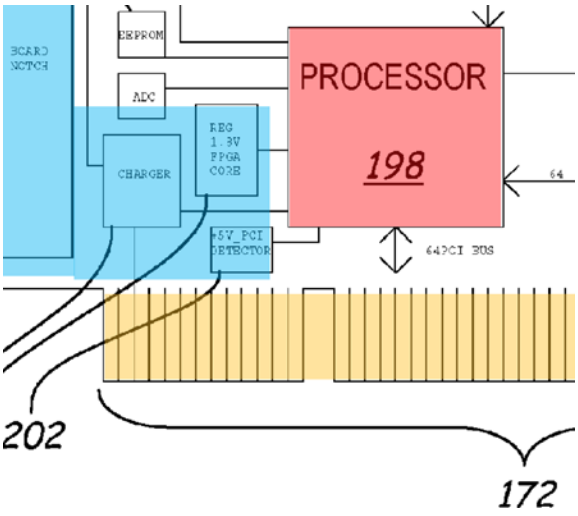
c) [8.c] Wherein the Voltage Monitor Circuit Transmits a Signal to Portion(s) of the Controller

783. Claim 8 requires "*wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller*."

784. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

785. For the reasons discussed above with reference to claim limitations [4.b] and [6.b], Spiers discloses and renders obvious "*wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller*" to a Skilled Artisan. *Supra* ¶¶709-723 (claim limitation [4.b]), ¶¶749-758 (claim limitation [6.b]). For example, Spiers discloses that a +5V PCI detector 202 is connected to processor 198, and a Skilled Artisan would have understood that this connection is used to transmit a signal to the processor ("*one or more portions of the controller*") when a power failure is detected (as indicated by the input voltage being out of range as defined by lower and upper thresholds), and the processor switches the power to the capacitors. Ex. 1025 at Fig. 5 (reproduced below in part, annotated, showing the connection between the +5V PCI detector 202 and processor 198) and Fig. 14, [0054] ("Referring now to FIG. 14, the operational steps performed by the backup device upon detection of a power failure are now described. As discussed

previously, the backup device monitors the primary power supply. In the PCI card embodiment, this monitoring is performed by monitoring the voltage at a +5 volt pin. In another embodiment, the backup device monitors the PCI bus for a power failure indication. Initially, at block 720, a power failure is detected. At block 724, the backup device processor switches the power to the capacitors.").



786. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller*."

9. Claim 9 is Unpatentable

787. Claim 9 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [9.a] Wherein the Voltage Monitor Circuit Detects an Amplitude of the Input Voltage Being Above a First Predetermined Threshold Voltage

788. Claim 9 requires "*[t]he memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage*."

789. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

790. As discussed above with reference to claim limitation [8.c], Spiers discloses and renders obvious "*wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller*" to a Skilled Artisan. *Supra* ¶¶783-786.

791. For the reasons discussed above with reference to claim limitations [4.b] and [6.b], Spiers discloses and renders obvious "*wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage*" to a Skilled Artisan. *Supra* ¶¶709-723 (claim limitation [4.b]), ¶¶749-756 (claim limitation [6.b]).

Samsung Electronics Co., Ltd.
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792. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage*" limitation.

b) [9.b] Wherein the First Predetermined Threshold Voltage is Above a Specified Operating Voltage

793. Claim 9 requires "*wherein the first predetermined threshold voltage is above a specified operating voltage*."

794. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

795. For the reasons discussed above with reference to claim limitations [4.b] and [6.b], Spiers in view of Amidi renders obvious to a Skilled Artisan that the "*first predetermined threshold voltage*" corresponds to a tolerance the module can safely handle in the external voltage during operation. *Supra* ¶¶709-723 (claim limitation [4.b]), ¶¶749-756 (claim limitation [6.b]). Furthermore, Spiers discloses a +5V PCI detector 202, and a Skilled Artisan would have understood that +5V represents a "*specified operating voltage*" for the input voltage the backup device 144 uses. Ex. 1025 (Spiers) at Figs. 5, 14, [0037].

796. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the first predetermined threshold voltage is above a specified operating voltage*" limitation.

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10. Claim 10 is Unpatentable

797. Claim 10 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

798. Claim 10 requires "*[t]he memory module of claim 9, wherein the first predetermined threshold voltage is ten percent above the specified operating voltage*."

799. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

800. For the reasons discussed above with reference to claim limitations [4.b] and [6.b], Spiers in view of Amidi renders obvious to a Skilled Artisan that the "*first predetermined threshold voltage is ten percent above the specified operating voltage*." *Supra* ¶¶709-723 (claim limitation [4.b]), ¶¶749-756 (claim limitation [6.b]).

801. As discussed above with reference to claim limitations [4.b] and [6.b], Spiers alone and in combination with Amidi renders obvious to a Skilled Artisan that a "*predetermined threshold voltage*" corresponds to a tolerance the module can safely handle in the external voltage. *Supra* ¶¶709-723 (claim limitation [4.b]), ¶¶749-756 (claim limitation [6.b]).

802. In Spiers (like in Harris), the external voltage (5V) is stepped down by voltage regulators to the voltages used by the parts in the module, including the

memory devices. Thus, a Skilled Artisan would have understood that, just like in Harris, the tolerance on the input voltage (+/-15%) can be larger than the tolerance of the memory devices (e.g., roughly 5% for DDR2 SDRAMs). Ex. 1023 at [0013] (describing +/- 15% tolerance); Ex. 1026 at pp.6-7 (describing +/- 0.1V tolerance for 1.8V supply voltage to DDR2 SDRAM devices); *see also* Ex. 1024 at Fig. 6 (showing a VREF 5% below nominal value when the external voltage is directly used by the memory devices).

803. Therefore, a Skilled Artisan would have understood and been motivated to select a tolerance between 5% and 15% for the module of Spiers, where the specific value selected would be nothing more than an obvious design choice. A Skilled Artisan would have also understood that allowing too high a tolerance carries the risk of losing data or damaging the devices on the memory module, while setting too low a tolerance carries the risk of unnecessary interruptions of operation. In particular, a Skilled Artisan would have understood that the choice of a 10 percent tolerance provided a reasonable compromise between the risks associated with too high a tolerance and too low a tolerance. *See, e.g.*, Ex. 1063 at 1-2 (reproduced below in part, annotated, describing an Over-Voltage Threshold of about 5.6V and an Under-Voltage Threshold of about 4.4V for a +5V power supply).

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

A Skilled Artisan would have also understood that such a PCI voltage detector can be implemented on a PCI card. *Id.* at 1 (describing typical application, including on Add-in Cards).

804. For example, Amidi discloses an alternative implementation for monitoring a power rail of 3.3V and comparing it to a 3.0V reference voltage, corresponding to a "*predetermined threshold voltage*" of about 10 percent below the power rail's nominal voltage. *See* Ex. 1024 at Fig. 14 (reproduced below, annotated), 8:23-36; *see also* Ex. 1027 at 32 (stating VDDSPD has a typical voltage of 3.3 volts with a minimum voltage 10 percent below the typical voltage, or 3.0 volts, and a maximum voltage 10 percent above the typical voltage, or 3.6 volts).

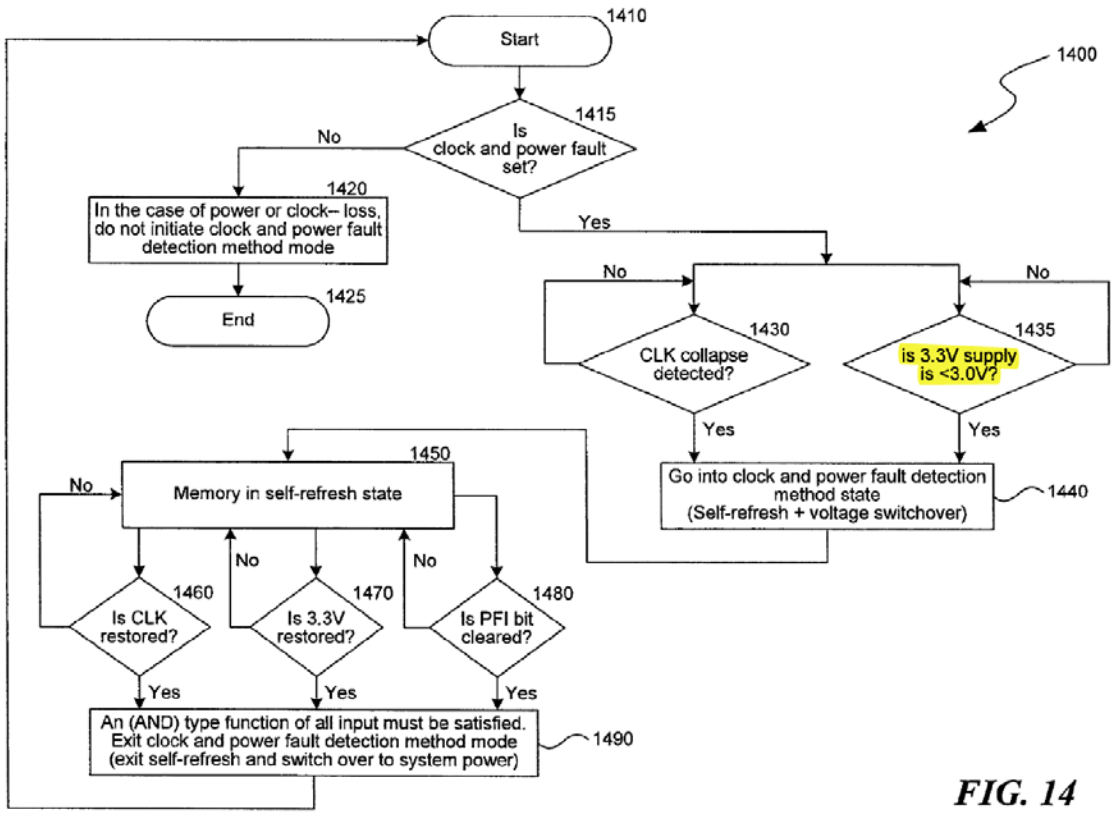


FIG. 14

805. Therefore, a Skilled Artisan would have understood that a tolerance of 10% was an obvious choice for a "*predetermined threshold voltage*."

806. As discussed for claim limitation [6.b], to the extent one were to argue that overvoltage detection was not obvious in light of Ground 4, it would have been obvious in light of Hajeck, as part of Ground 5. *Supra* ¶¶756-758.

807. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the first predetermined threshold voltage is ten percent above the specified operating voltage*" limitation.

11. Claim 11 is Unpatentable

808. Claim 11 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [11.a] Wherein the Voltage Monitor Circuit Detects an Amplitude of the Input Voltage Being Below a Second Predetermined Threshold Voltage

809. Claim 11 requires "*[t]he memory module of claim 9, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage*."

810. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

811. For the reasons discussed above with reference to claim limitations [4.b] and [6.b], the prior art references in each of Grounds 4 and 5 renders obvious to a Skilled Artisan "*wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage*." *Supra* ¶¶709-723 (claim limitation [4.b]), ¶¶749-756 (claim limitation [6.b]).

812. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the voltage monitor circuit detecting a power threshold*

condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage" limitation.

b) [11.b] Wherein the Second Predetermined Threshold Voltage is Below the Specified Operating Voltage

813. Claim 11 requires "*wherein the second predetermined threshold voltage is below the specified operating voltage*."

814. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

815. For the reasons discussed above with reference to claim limitations [4.b], [6.b], [9.b], the prior art references in each of Grounds 4 and 5 renders obvious to a Skilled Artisan "*wherein the second predetermined threshold voltage is below the specified operating voltage*." *Supra* ¶¶709-723 (claim limitation [4.b]), ¶¶749-756 (claim limitation [6.b]), ¶¶793-796 (claim limitation [9.b]).

816. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the second predetermined threshold voltage is below the specified operating voltage*" limitation.

c) [11.c] Wherein the Memory Module Transitions from a First Operable State to a Second Operable State

817. Claim 11 requires "*wherein the memory module transitions from a first operable state to a second operable state in response to the signal*."

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818. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

819. For the reasons discussed above with reference to claim limitation [4.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶724-730.

820. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the memory module transitions from a first operable state to a second operable state in response to the signal*" limitation.

12. Claim 12 is Unpatentable

821. Claim 12 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

822. Claim 12 requires "*[t]he memory module of claim 11, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage*."

823. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

824. As discussed for claim 10, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the first predetermined threshold voltage is ten percent above the specified operating voltage*" limitation. *Supra* ¶¶797-807. For the same reasons why the "*first predetermined threshold voltage*" is "*ten percent*

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above the specified operating voltage," the same combinations render obvious that "*the second predetermined threshold voltage is ten percent below the specified operating voltage*."

825. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory module of claim 11, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage*."

13. Claim 13 is Unpatentable

826. Claim 13 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

827. Claim 13 requires "*[t]he memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage*."

828. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

829. For the reasons discussed above with reference to claim limitation [4.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶709-723.

830. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the voltage monitor circuit detecting a power threshold*

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Ex. 1069, p. 363

condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage" limitation.

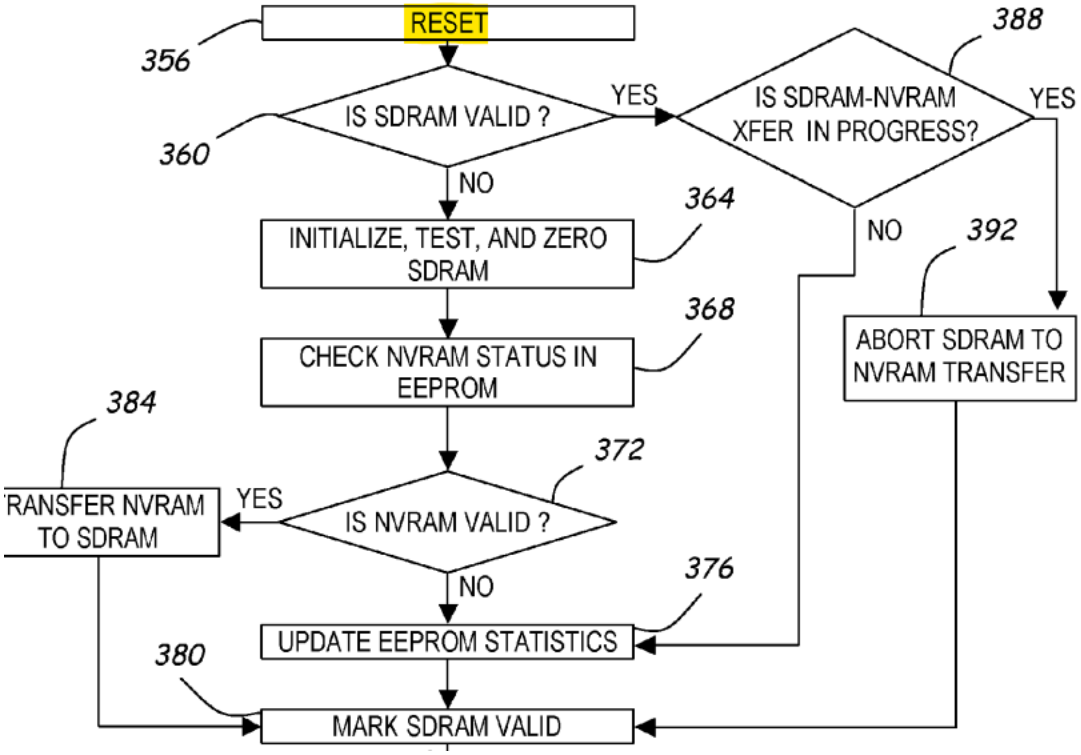
14. Claim 14 is Unpatentable

831. Claim 14 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

832. Claim 14 requires "*[t]he memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system.*"

833. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

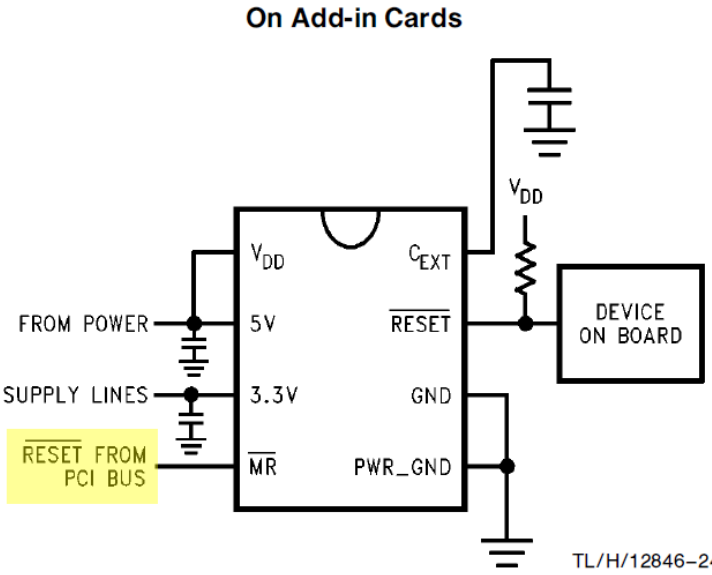
834. For example, as discussed above with reference to claims 4 and 8, Spiers discloses to a Skilled Artisan "*a voltage monitor circuit detecting a power threshold condition,*" including power detection circuit 202 monitoring the +5 volt supply voltage at a +5 volt pin of PCI connector 172, and detecting a power interruption. Spiers also discloses to a Skilled Artisan that such a power-failure detection "*includes the voltage monitor circuit detecting a request* [such as a Reset] *by the host system*." *See* Ex. 1025 at Fig. 8 (reproduced below in part, annotated).



835. For example, Spiers discloses detecting a reset request by the host system when data is transferred from the volatile SDRAM to the non-volatile NAND Flash. *Id*. at [0043] ("If, at block 360, it is determined that the SDRAM is valid, it is then determined if a SDRAM to NVRAM transfer was in progress at the time the backup device was reset, as indicated at block 388."). Spiers also discloses that such a SDRAM to NVRAM transfer happens following the voltage monitor circuit detecting a power failure. *See, e.g.*, *id.* at Abstract ("The backup data storage device further includes a backup power source such as a capacitor, a battery, or any other suitable power source, and upon detection of a power interruption, switches to the backup power source and receives power from the

backup power source while moving the data from the backup volatile memory to the backup non-volatile memory.").

836. A Skilled Artisan would have understood from this disclosure that the host can issue a Reset request while the SDRAM-to-NVRAM transfer happens following a power failure. A Skilled Artisan would have also understood that the host can reset the PCI voltage detector. For example, a Skilled Artisan would have understood that a "+5V PCI detector" at the time included such a reset functionality. *See* Ex. 1063 at 1 (reproduced below in part, annotated, showing RESET from PCI Bus); *see also* Ex. 1031 at 133 (PCI standard requiring, "The system must assert RST# [Reset] … in the event of a power failure.").



837. Thus, it would have been obvious to a Skilled Artisan that, in Spiers, the functionality of "*detecting a power threshold condition*" includes detecting a reset request by the voltage monitor circuit. Indeed, a Skilled Artisan would have

understood that, when the host issues a Reset request as disclosed by Spiers, the host can also reset the PCI voltage detector. A Skilled Artisan would have been motivated to issue such a reset of the PCI voltage detector in order to make sure that the different parts of the module, including the PCI voltage detector, are properly reset and correctly operate following a power failure.

838. Accordingly, the prior art references in each of Grounds 4 and 5 invalidate the "*wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system*" limitation.

15. Claim 15 is Unpatentable

839. Claim 15 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

840. Claim 15 requires "*[t]he memory module of claim 1, wherein two of the at least three buck converters are configured to operate as a dual-buck converter*."

841. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

842. The prior art references in each of Grounds 4 and 5 renders obvious to a Skilled Artisan that "*two of the at least three buck converters are configured to operate as a dual-buck converter*."

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843. As explained above for claim limitation [1.c], the prior art references in each of Ground 4 (Spiers in view of Amidi) and Ground 5 (Ground 4 in view of Hajeck) render obvious to a Skilled Artisan that "*two of the at least three buck converters are configured to operate as a dual-buck converter*." *Supra* ¶¶609-660. As previously discussed for Voltage Mapping A and B of Grounds 4 and 5, the first of the "*at least three buck converters*" provides, for example, VDD/VDDQ as the first of the "*regulated voltages*" to the memory devices, such as DDR2 or DDR3 DRAMs. *See id.* In addition, the second of the "*at least three buck converters*" provides, for example, VCCFPGA as the second of the "*regulated voltages*" to the FPGA implementing the processor. *See id.* Further, the third of the "*at least three buck converters*" provides, for example, VTT as the third of the "*regulated voltages*" to the memory devices, such as DDR2 or DDR3 DRAMs. *See id.*

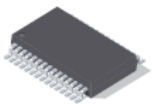
844. For Mappings A and B of Grounds 4 and 5, where the first, second, and third regulated voltages are VDD/VDDQ, VCCFPGA, and VTT, a Skilled Artisan would have been motivated, for example, to use a dual buck converter to have VTT follow the fluctuations of VDD/VDDQ, thus maintaining the fixed ratio between VTT and VDD/VDDQ. *See id.* In each of these cases, a Skilled Artisan would have been motivated to use a "*dual buck converter*" to provide the first and third "*regulated voltages*" because using a dual buck converter would use fewer

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integrated circuits, pins, and interconnections on the module, therefore simplifying its design. Further, in each of the voltage mappings above, a Skilled Artisan would have been motivated with a reasonable expectation of success to use a "*dual buck converter*" to provide the second and third "*regulated voltages*," for example to reduce input "ripple" and improve performance, as discussed below.

845. A Skilled Artisan would have understood that such "*dual buck converters*" were designed and readily available on the market at the time for this very functionality. *Id.*; Ex. 1040 at 1 (reproduced below in part), 11 ("TPS51020 gives a complete function set required for the DDR termination supply such as VDDQ/2 tracking V_{TT}"); *see also supra* ¶¶653-654.

TEXAS INSTRUMENTS



TPS51020

SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

APPLICATIONS

- **Notebook Computers System Bus and I/O**
- **DDR I or DDR II Termination**

See also Ex. 1041 at 1, 2 (reproduced below in part, annotated), 9 (disclosing how using different phases for the two converters can reduce ripples); Ex. 1047 at 3:49-

50, 4:7-10, 4:37-56, 5:4-13, 5:46-59 & Fig.2 (illustrating dual buck converter with Vout1=V_{DDQ} and Vout2=V_{TT} and phase shifting).

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Applications

■ DDR V_{DDQ} and V_{TT} voltage generation

Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

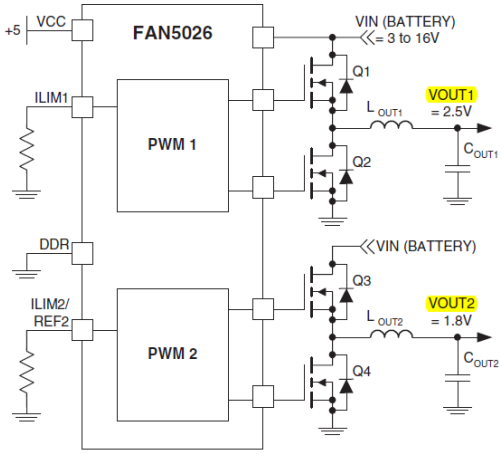


Figure 1. Dual Output Regulator

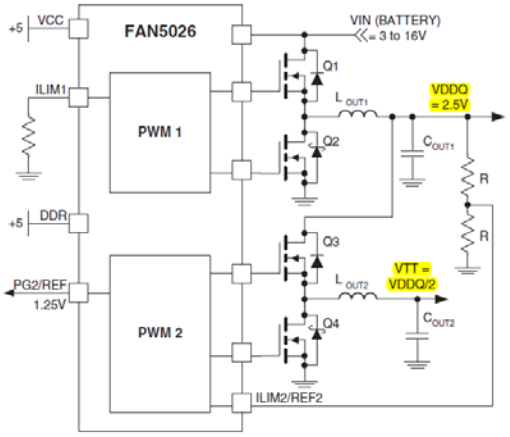


Figure 2. Typical Application

846. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*wherein two of the at least three buck converters are configured to operate as a dual-buck converter*."

16. Claim 16 is Unpatentable

847. Claim 16 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [16.a] Preamble

848. The preamble of claim 16 requires "*[a] memory module comprising*."

849. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

850. As shown in the table below, the preamble of Claim 16 is identical to the preamble Claim 1:

Claim 1	**Claim 16**
[1.a] A memory module comprising:	[16.a] A memory module comprising:

851. As discussed above with reference to claim element [1.a], to the extent the preamble of claim 1 is limiting, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶595-600.

b) [16.b] Printed Circuit Board

852. Claim 16 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system*."

853. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

854. As shown in the table below, claim element [16.b] is very similar to claim element [1.b]:

Claim 1	**Claim 16**
[1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;	[16.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;

855. As discussed above with reference to claim limitation [1.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶601-608.

c) [16.c] Voltage Conversion Circuit

856. Claim 16 requires "*a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages*."

857. As shown in the table below, claim element [16.c] is very similar to claim element [1.c]:

Claim 1	Claim 16
[1.c] a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;	[16.c] a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

858. As discussed above with reference to claim limitation [1.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶609-660.

d) [16.d] A Plurality of Components Coupled to the PCB

(1) [16.d.1] Plurality of components each coupled to at least one regulated voltage

859. Claim 16 requires "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages*."

860. As shown in the table below, claim element [16.d.1] is very similar to claim element [1.d.1]:

Claim 1	Claim 16
[1.d.1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages,	[16.d.1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages,

861. As discussed above with reference to claim limitation [1.d.1], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶661-664.

(2) [16.d.2] Plurality of components includes SDRAM devices

862. Claim 16 requires "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices*."

863. As shown in the table below, claim element [16.d.2] is very similar to claim elements [1.d.2]:

Claim 1	**Claim 16**
[1.d.2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and	[16.d.2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices

864. As discussed above with reference to claim elements [1.d.2], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶665-668.

(3) [16.d.3] The SDRAM devices are coupled to the first regulated voltage

865. Claim 16 requires "*the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages*."

866. As shown in the table below, claim element [16.d.3] is very similar to claim element [1.d.5]:

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Claim 1	**Claim 16**
[1.d.5] wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.	[16.d.3] the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages

867. As discussed above with reference to claim element [1.d.5], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶684-687.

e) [16.e] A Controller Coupled to the PCB

(1) [16.e.1] The Controller Includes a Voltage Monitor Circuit

868. Claim 16 require "*a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage*."

869. As shown in the table below, claim element [16.e.1] is very similar to claim limitations [1.b], [8.b], and [9.a]:

Claims 1, 8, 9	**Claim 16**
[8.b] a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections, [1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system; [9.a] The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage,	[16.e.1] a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage

870. As discussed above with reference to claim limitations [1.b], [8.b], and [9.a], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶601-608 (claim limitation [1.b]), ¶¶778-782 (claim limitation [8.b]), ¶¶788-792 (claim limitation [9.a]).

871. Furthermore, a Skilled Artisan would have understood that Spiers's +5V PCI detector 202 (part of the "*voltage monitor circuit*") is "*configured to*

detect an amplitude change in the input voltage," for example, when the input voltage changes by crossing the reference voltage.

(2) [16.e.2] Wherein the Memory Module Transitions from a First Operable State to a Second Operable State

872. Claim 16 requires "*wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state*."

873. As shown in the table below, claim element [16.e.2] is very similar to claim element [4.c]:

Claim 4	**Claim 16**
[4.c] wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.	[16.e.2] wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state

874. As discussed above with reference to claim element [4.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶724-730.

17. Claim 17 is Unpatentable

875. Claim 17 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

876. Claim 17 requires "*[t]he memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first*

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predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage."

877. As shown in the table below, claim 17 is very similar to claim limitations [4.b] and [6.b]:

Claims 4, 6	**Claim 17**
[4.b] . . . the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, [6.b] . . . the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage,	[17] The memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage.

878. As discussed above with reference to claim elements [4.b] and [6.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶709-723 (claim limitation [4.b]), ¶¶749-756 (claim limitation [6.b]).

18. Claim 18 is Unpatentable

879. Claim 18 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

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a) [18.a] Wherein, in the First Operable State, Voltage Conversion Circuit Provides First Regulated Voltage to SDRAM Devices Using First Pre-Regulated Voltage

880. Claim 18 requires "*[t]he memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage*." The "*first pre-regulated voltage*" is in addition to the "*input voltage*" from [16.e.2].

881. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

882. As discussed above with reference to claim element [4.c] and [16.e.2], the combination teaches a "*first operable state*" in which Spiers's memory module operates on PCI +5V power when its amplitude is above a threshold and a "*second operable state*" in which the memory module operates on capacitor power when the PCI +5V power is below a threshold. *Supra* ¶¶726-729, 872-874.

883. Spiers discloses that when the backup device is relying on the system power (i.e., "in the first operable state"), the voltage conversion circuit provides the first regulated voltage VDD to the plurality of SDRAM devices using the system supply voltage of +5V.

884. I understand that Patent Owner has indicated the "*pre-regulated voltage*" as recited in the claims of the related 918 Patent is satisfied by an input voltage which has pre-determined tolerances or limits. *See* Ex. 1073 at 49-50

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(pointing to input voltage received from "Power edge connection"). Under such an apparent claim construction, Spiers discloses that the input voltage can be the PCI +5V supply voltage which a Skilled Artisan understood was provided within a +/- 5% tolerance. Ex. 1025 at [0037] ("The FPGA processor 198 utilizes a power detection circuit that, in this embodiment, is a +5V PCI detector 202."); Ex. 1031 at p.117 (allowing +/-0.25 V tolerance, reproduced below in part).

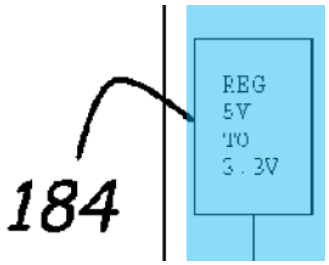
Table 4-1: DC Specifications for 5V Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{CC}	Supply Voltage		4.75	5.25	V	

885. Therefore, Spiers discloses a "*first pre-regulated voltage*" to a Skilled Artisan under Patent Owner's apparent claim interpretation.

886. To the extent the claimed "*pre-regulated input voltage*" requires "pre-regulating" the input voltage on the memory module, *see* Ex. 1001 at 28:53-58, it would have been obvious to a Skilled Artisan at the time to convert the +5V from the PCI bus into a 3.3V "pre-regulated" voltage in light of the disclosure of Spiers.

887. For example, Spiers discloses that the power from the capacitors is provided by a voltage regulator 184 that converts the voltage from the capacitors into a 3.3V regulated voltage.



Ex. 1025 at Fig. 5 (reproduced above in part); [0037] ("The power supply comprises two super capacitors 176, which, in this embodiment, are 50 F each and connected in parallel. The capacitors 176 are connected to a diode 180 a voltage regulator 184, and a charger 186. The charger 186 is utilized to charge the capacitors 176, and in the event of a power failure the capacitors are used as the power source to power the backup device 144 when moving data from the volatile memory to the non-volatile memory.").

888. A Skilled Artisan would have been motivated to add a power regulator to convert the +5V PCI voltage to a 3.3V regulated voltage, similar to voltage regulator 184 converting the 5V backup voltage from the capacitors to a 3.3V regulated voltage. Such a 5V to 3.3V pre-regulator would stabilize the power on the module if the external power source provides—or there is a chance it may provide—an unregulated input voltage, so that the additional power regulator ensures that the input of Spiers's voltage converters remains within a tolerated interval. *See, e.g.*, Ex. 1023 (Harris) at [0014] ("It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even

including variable voltages."). A Skilled Artisan would have also understood that such an additional voltage regulator can be used to convert an input voltage other than 5V into 3.3V, thus allowing Spiers's module to be adapted to a system which provides an input voltage other than 5V without replacing other parts of the module. *See, e.g.*, Ex. 1023 (Harris) at [0020] ("voltage-independent embodiments disclosed herein can provide upgradeability and extensibility without changing system board power distribution"). A Skilled Artisan would have understood that such an additional voltage regulator can be a DC-DC switch-mode converter which provides a regulated voltage. Ex. 1032 (Mohan) at 161-162 (describing switch-mode converters as being used in "regulated switch-mode dc power supplies" where "the average dc output voltage must be controlled to equal a desired level"). Therefore, a Skilled Artisan would have been motivated to convert the +5V PCI voltage from the PCI +5V supply to 3.3V as well and provide this pre-regulated 3.3V to the buck converters powering the SDRAMs. In such an implementation, these buck converters would receive the same pre-regulated voltage of 3.3V during normal operation and also when powered from the capacitors, thus avoiding large transients when changing from +5V PCI power to the capacitors. Ex. 1025 at Fig. 14, [0054] ("At block 724, the backup device processor switches the power to the capacitors.").

889. Therefore, Spiers in view of Amidi renders obvious the claimed "*first pre-regulated voltage*" (down-converted from the +5V PCI voltage to 3.3V before using buck converters to provide the supply voltages to the SDRAM devices) under such an interpretation as well.

890. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage*" limitation.

b) [18.b] Wherein, in the Second Operable State, Voltage Conversion Circuit Provides First Regulated Voltage to SDRAM Devices Using Second Pre-Regulated Voltage

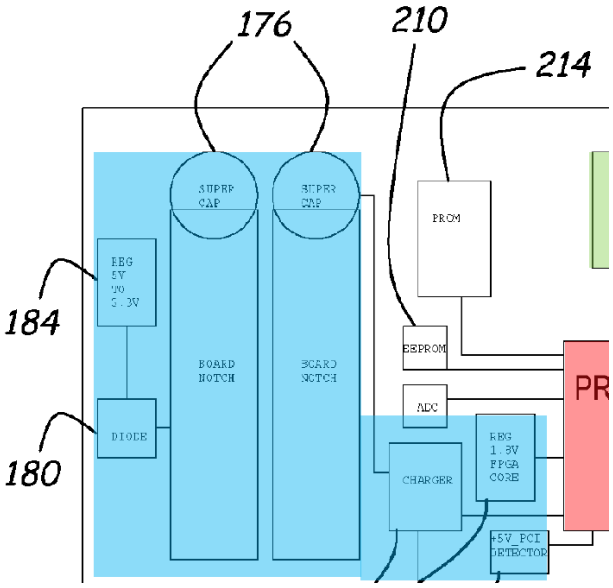
891. Claim 18 further requires "*wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage*."

892. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

893. As discussed above with reference to claim element [4.c] and [16.e.2], the combination teaches a "*first operable state*" in which Spiers's memory module operates on PCI +5V power when its amplitude is above a threshold and a "*second operable state*" in which the memory module operates on capacitor power when the PCI +5V power is below a threshold. *Supra* ¶¶726-729, 872-874.

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894. Spiers discloses that when the backup device is relying on capacitor power (i.e., "*in the second operable state*"), the voltage conversion circuit provides the first regulated voltage VDD to the plurality of SDRAM devices using a voltage produced by power regulator 184 by converting the voltage of the capacitor to 3.3V (i.e., "*a second pre-regulated voltage*").



Ex. 1025 at Fig. 5 (reproduced below in part), [0037] ("The power supply comprises two super capacitors 176, which, in this embodiment, are 50 F each and connected in parallel. The capacitors 176 are connected to a diode 180 a voltage regulator 184, and a charger 186. The charger 186 is utilized to charge the capacitors 176, and in the event of a power failure the capacitors are used as the power source to power the backup device 144 when moving data from the volatile memory to the non-volatile memory.").

895. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage*" limitation.

19. Claim 19 is Unpatentable

896. Claim 19 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [19.a] Wherein, in the First Operable State, the First Pre-Regulated Voltage is Supplied to the Voltage Conversion Circuit Via a Circuit

897. Claim 19 requires "*[t]he memory module of claim 18, wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit*."

898. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

899. As discussed above with reference to claim limitation [18.a], Spiers discloses that when the backup device is relying on the system power (i.e., "*in the first operable state*"), the voltage conversion circuit provides the first regulated voltage VDD to the plurality of SDRAM devices using "*a first pre-regulated voltage*." *Supra* ¶¶880-890.

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900. Spiers in view of Amidi renders obvious to a Skilled Artisan in view of Amidi that when the backup device is relying on the system power (i.e., "*in the first operable state*"), "*the first pre-regulated voltage is supplied to the voltage conversion circuit,*" including voltage converters to power the SDRAMs, the NAND Flash memories and the processor 198, "*via a circuit*" such as the Power switch multiplexer of Amidi. *See, e.g.*, Ex. 1024 at Fig. 7 (reproduced below); *see also id*. at Figs. 5-6 (showing details in Power management block).

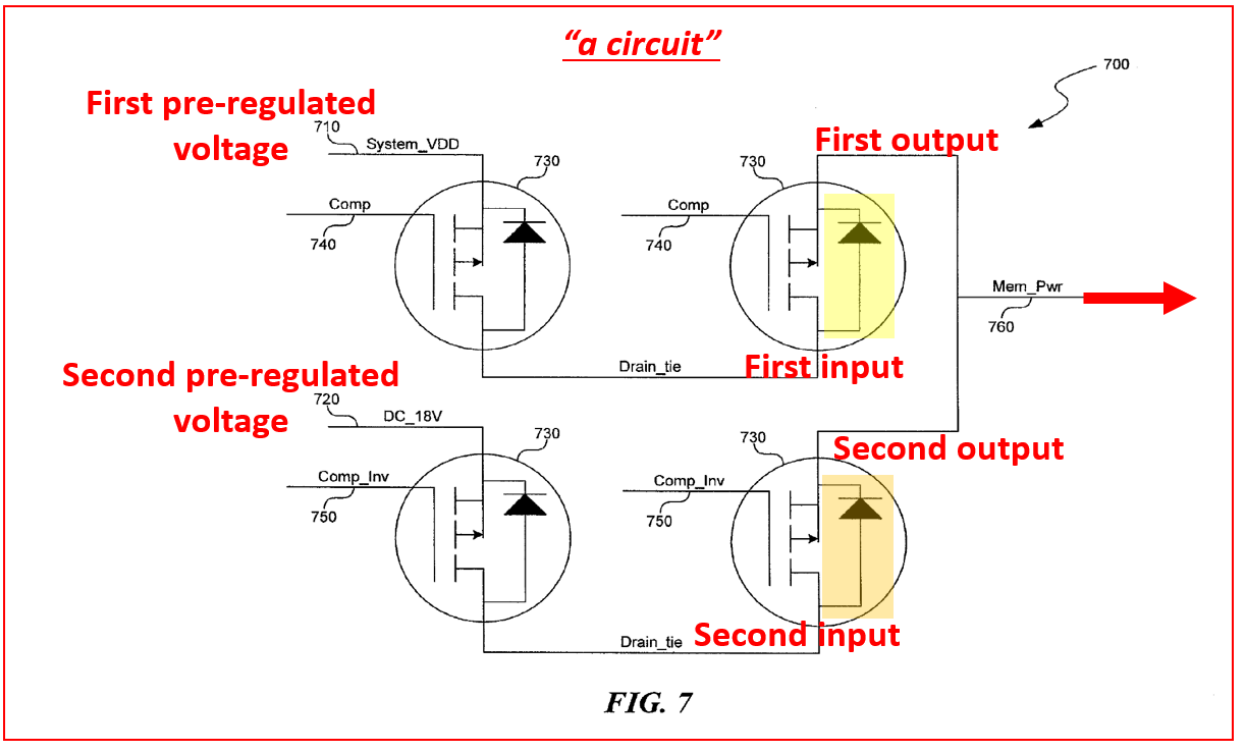


FIG. 7

901. Spiers discloses that, in case of power failure, "the backup device processor switches the power to the capacitors." Ex. 1025 at [0054]; *see also id*. at Abstract ("The backup data storage device further includes a backup power source such as a capacitor, a battery, or any other suitable power source, and upon

detection of a power interruption, switches to the backup power source and receives power from the backup power source while moving the data from the backup volatile memory to the backup non-volatile memory.").

902. A Skilled Artisan would have understood from this disclosure that Spiers's module includes a power switch to select either the external power from the PCI bus or the backup power from the capacitors. Although Spiers does not expressly disclose a specific structure for performing this functionality to switch to the secondary power source of capacitors, it would have been obvious to a Skilled Artisan to use a structure like Amidi's power switch 700 for this fuctionality, since it discloses "an embodiment of a power switch multiplexer." Ex. 1024 at Fig. 7 (reproduced above); 4:56-63. A Skilled Artisan would be particularly motivated to use a power switch like Amidi's because "when the path between system supply 710 and memory supply 760 is shutoff, even parasitic conductance should be minimal or zero." *Id*. at 5:6-9. In particular, "the opposing parasitic diodes of the transistors 730 in each conduction path should essentially block parasitic current when a given conduction path is turned off." *Id*. at 5:16-19. A Skilled Artisan would have understood that getting rid of parasitic currents advantageously saves power.

903. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit*" limitation.

b) [19.b] Wherein, in the Second Operable State, the Second Pre-Regulated Voltage is Supplied to the Voltage Conversion Circuit via the Circuit

904. Claim 19 further requires "*wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit.*"

905. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

906. As discussed above with reference to claim limitation [18.b], Spiers discloses that when the backup device relies on capacitor power (i.e., "*in the second operable state*"), the voltage conversion circuit provides the first regulated voltage VDD to the plurality of SDRAM devices using "*a second pre-regulated voltage*." *Supra* ¶¶891-895.

907. For the reasons discussed above with reference to claim limitation [19.a], Spiers in view of Amidi renders obvious to a Skilled Artisan that when the backup device relies on capacitor power (i.e., "*in the second operable state*"), *the second pre-regulated voltage is supplied to the voltage conversion circuit,* including voltage converters to power the SDRAMs, the NAND Flash memories

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and the processor 198, *via a circuit* such as the Power switch multiplexer of Amidi. *Supra* ¶¶897-903.

908. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit*" limitation.

20. Claim 20 is Unpatentable

909. Claim 20 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [20.a] Wherein the Circuit Includes a First Diode

910. Claim 20 requires "*[t]he memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit*."

911. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

912. The Spiers-Amidi combination discloses that "*the circuit* [including the Power switch multiplexer of Amidi] *includes a first diode* [(yellow)] *having a first input and a first output, the first input is coupled to the first pre-regulated voltage* [710, from the system] *and the first output is coupled to the voltage*

conversion circuit [through Mem_Pwr output 760]." *See, e.g.*, Ex. 1024 at Fig. 7 (reproduced below, annotated).

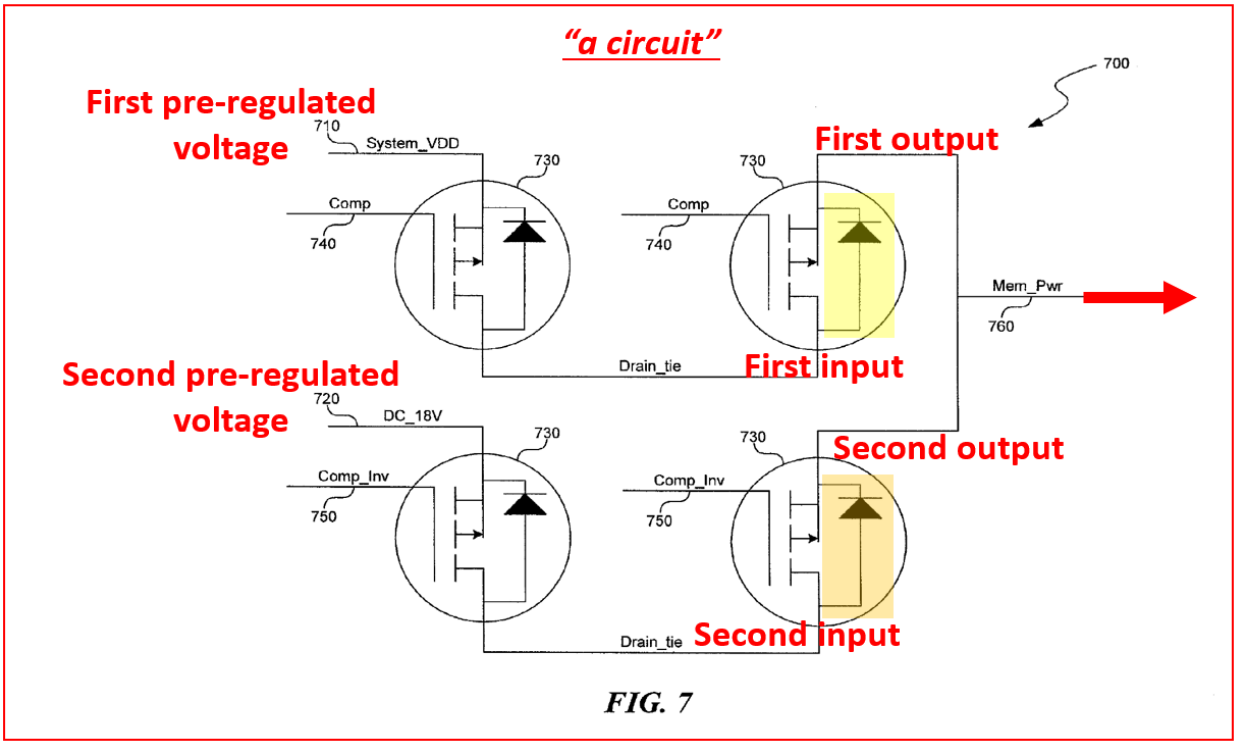


FIG. 7

913. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit*" limitation.

b) [20.b] Wherein the Circuit Includes a Second Diode

914. Claim 20 further requires "*wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.*"

915. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

916. The Spiers-Amidi combination discloses that "*the circuit* [including the Power switch multiplexer of Amidi] *includes a second diode* [(orange)] *having a second input and a second output, the second input is coupled to the second pre-regulated voltage* [720, from backup power] *and the second output is coupled to the first output and to the voltage conversion circuit* [through Mem_Pwr output 760]." *See, e.g.*, Ex. 1024 at Fig. 7 (reproduced below, annotated).

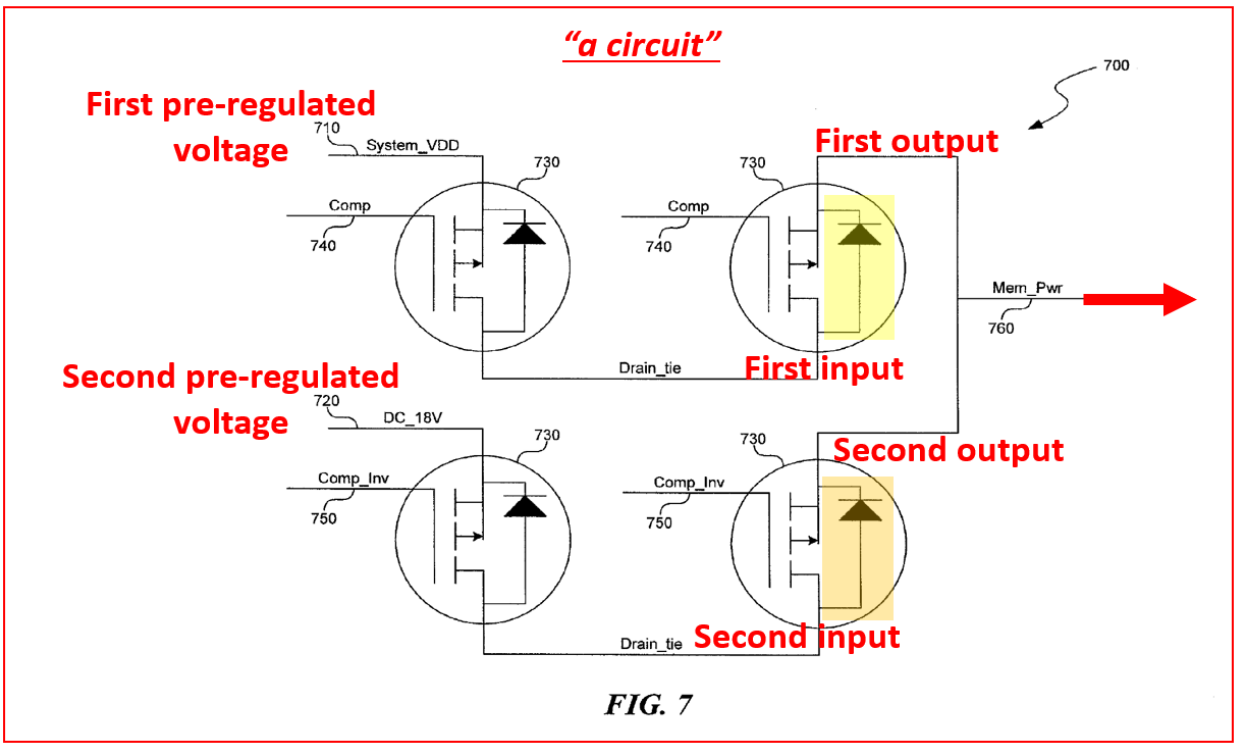


FIG. 7

917. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage*

and the second output is coupled to the first output and to the voltage conversion circuit" limitation.

21. Claim 21 is Unpatentable

918. Claim 21 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [21.a] Preamble

919. The preamble of claim 21 requires that "*[t]he memory module of claim 16, further comprising*."

920. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

921. As discussed above with reference to claim 16, the prior art references in each of Grounds 4 and 5 satisfy the "*[t]he memory module of claim 16*." *Supra* ¶¶847-874.

b) [21.b] A First Circuit with a First Input, Second Input, and an Output

922. Claim 21 requires "*a first circuit having a first input, a second input and an output, the first input coupled to a first pre-regulated voltage, the second input coupled to a second pre-regulated voltage, the output coupled to the voltage conversion circuit*."

923. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

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924. As shown in the table below, claim element [21.b] is very similar to claim elements [20.a] – [20.b]:

Claim 20	**Claim 21**
[20.a] The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit [20.b] wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.	[21.b] a first circuit having a first input, a second input and an output, the first input coupled to a first pre-regulated voltage, the second input coupled to a second pre-regulated voltage, the output coupled to the voltage conversion circuit,

925. As discussed above with reference to claim elements [20.a] – [20.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶910-917.

c) [21.c] Wherein the Voltage Conversion Circuit Provides the First Regulated Voltage to the SDRAM devices

926. Claim 21 further requires "*wherein the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a supply voltage*."

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927. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

928. As shown in the table below, claim element [21.c] is very similar to claim elements [18.a] – [18.b]:

Claim 18	**Claim 21**
[18.a] The memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and [18.b] wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.	[21.c] wherein the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a supply voltage,

929. As discussed above with reference to claim elements [18.a] – [18.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶880-895.

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d) [21.d] Wherein, in the First Operable State, the First Circuit Provides the First Pre-Regulated Voltage to the Voltage Conversion Circuit

930. Claim 21 further requires "*wherein, in the first operable state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the first pre-regulated voltage*."

931. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

932. As shown in the table below, claim element [21.d] is very similar to claim element [19.a]:

Claim 19	**Claim 21**
[19.a] The memory module of claim 18, wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit, and	[21.d] wherein, in the first operable state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the first pre-regulated voltage,

933. As discussed above with reference to claim element [19.a], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶897-903.

e) [21.e] Wherein, in the Second State, the First Circuit Provides the Second Pre-Regulated Voltage to the Voltage Conversion Circuit

934. Claim 21 further requires "*wherein, in the second state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the second pre-regulated voltage*."

935. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

936. As shown in the table below, claim element [21.e] is very similar to claim element [19.b]:

Claim 19	**Claim 21**
[19.b] wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit.	[21.e] wherein, in the second state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the second pre-regulated voltage.

937. As discussed above with reference to claim element [19.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶904-908.

22. Claim 22 is Unpatentable

938. Claim 22 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

939. Claim 22 requires "*[t]he memory module of claim 21, wherein the first circuit includes a first diode coupled between the first input and the output and a second diode coupled between the second input and the output*."

940. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

941. As shown in the table below, claim is very similar to claim elements [20.a] – [20.b]:

Claim 20	**Claim 22**
[20.a] The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and [20.b] wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.	[22] The memory module of claim 21, wherein the first circuit includes a first diode coupled between the first input and the output and a second diode coupled between the second input and the output.

942. As discussed above with reference to claim elements [20.a] – [20.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶910-917.

23. Claim 23 is Unpatentable

943. Claim 23 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [23.a] Wherein the Voltage Monitor Circuit is Configured to Produce a Trigger Signal

944. Claim 23 requires "*[t]he memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage*."

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945. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

946. As shown in the table below, claim element [23.a] is very similar to claim elements [4.b] and [6.b]:

Claims 4, 6	**Claim 23**
[4.b] . . . the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, [6.b] . . . the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage,	[23.a] The memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and

947. As discussed above with reference to claim limitations [4.b] and [6.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶709-723 (claim limitation [4.b]), ¶¶749-756 (claim limitation [6.b]). Furthermore, as discussed above with reference to claim limitation [16.e.1], a Skilled Artisan would have understood that Spiers's +5V PCI detector 202 (i.e., "*voltage monitor circuit*") is "*configured to detect an amplitude change in the input voltage,*" for example, when the input voltage changes by crossing the reference voltage. *Supra* ¶¶868-871.

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b) [23.b] Wherein the Controller is Configured to Perform One or More Operations

948. Claim 23 further requires "*wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory*."

949. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

950. As shown in the table below, claim element [23.b] is very similar to claim element [5.c]:

Claim 5	**Claim 23**
[5.c] wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.	[23.b] wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

951. As discussed above with reference to claim element [5.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶739-744.

24. Claim 24 is Unpatentable

952. Claim 24 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [24.a] Preamble

953. The preamble of claim 24 requires "*[a] memory module comprising*."

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954. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

955. As shown in the table below, claim element [24.a] is identical to claim element [1.a]:

Claim 1	**Claim 24**
[1.a] A memory module comprising:	[24.a] A memory module comprising:

956. As discussed above with reference to claim element [1.a], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *See* ¶¶595-600.

b) [24.b] A Printed Circuit Board (PCB) Having an Interface

957. Claim 24 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system*."

958. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

959. As shown in the table below, claim element [24.b] is very similar to claim element [1.b]:

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Claim 1	**Claim 24**
[1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;	[24.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;

960. As discussed above with reference to claim element [1.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶601-608.

c) [24.c] A Voltage Conversion Circuit

961. Claim 24 requires "*a voltage conversion circuit configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages*."

962. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

963. As shown in the table below, claim element [24.c] is very similar to claim element [1.c]:

Claim 1	**Claim 24**
[1.c] a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;	[24.c] a voltage conversion circuit configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

964. As discussed above with reference to claim element [1.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶609-660.

d) [24.d] A Plurality of Components Coupled to the PCB

(1) [24.d.1] Plurality of components each coupled to at least one regulated voltage

965. Claim 24 requires "*a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages*."

966. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

967. As shown in the table below, claim element [24.d.1] is very similar to claim element [1.d.1]:

Claim 1	Claim 24
[1.d.1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages,	[24.d.1] a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages,

968. As discussed above with reference to claim element [1.d.1], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶661-664.

(2) [24.d.2] Plurality of components includes SDRAM devices

969. Claim 24 requires "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices*."

970. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

971. As shown in the table below, claim element [24.d.2] is very similar to claim element [1.d.2]:

Claim 1	Claim 24
[1.d.2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and	[24.d.2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices,

972. As discussed above with reference to claim element [1.d.2], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶665-668.

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(3) [24.d.3] Wherein the SDRAM devices are coupled to the first regulated voltage

973. Claim 24 requires "*wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages*."

974. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

975. As shown in the table below, claim element [24.d.3] is very similar to claim element [1.d.5]:

Claim 1	**Claim 24**
[1.d.5] wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.	[24.d.3] wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages; and

976. As discussed above with reference to claim element [1.d.5], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶684-687.

e) [24.e] A Controller Coupled to the PCB

(1) [24.e.1] The Controller includes a voltage monitor circuit

977. Claim 24 requires "*a controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface of the PCB, the voltage monitor circuit configured to monitor the input voltage*."

978. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

979. As shown in the table below, claim element [24.e.1] is very similar to claim element [16.e.1]:

Claim 16	**Claim 24**
[16.e.1] a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage,	[24.e.1] a controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface of the PCB, the voltage monitor circuit configured to monitor the input voltage,

980. As discussed above with reference to claim element [16.e.1], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶868-871. Because the PCB has the interface, receiving the input voltage from the host system via the interface also discloses receiving the input voltage from the host system via the interface of the PCB.

(2) [24.e.2] Wherein the controller is configured to perform one or more operations

981. Claim 24 further requires "*wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage*."

982. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

983. As shown in the table below, claim element [24.e.2] is very similar to claim elements [23.a] and [23.b]:

Claim 23	**Claim 24**
[23.a] The memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and [23.b] wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.	[24.e.2] wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and

984. As discussed above with reference to claim limitations [23.a] and [23.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *See* ¶¶944-951.

(3) [24.e.3] Wherein the one or more operations include a write operation to transfer data into non-volatile memory

985. Claim 24 further requires "*wherein the one or more operations include a write operation to transfer data into non-volatile memory*."

986. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

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987. As shown in the table below, claim element [24.e.3] is very similar to claim element [23.b]:

Claim 23	**Claim 24**
[23.b] wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.	[24.e.3] wherein the one or more operations include a write operation to transfer data into non-volatile memory.

988. As discussed above with reference to claim element [23.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶948-951.

25. Claim 25 is Unpatentable

989. Claim 25 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

990. Claim 25 requires "*[t]he memory module of claim 24, wherein, in response to the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state*."

991. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

992. As shown in the table below, claim 25 is very similar to claim element [16.e.2]:

Claim 16	Claim 25
[16.e.2] wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.	[25] The memory module of claim 24, wherein, in response to the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.

993. As discussed above with reference to claim limitation [16.e.2], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶872-874.

26. Claim 26 is Unpatentable

994. Claim 26 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

a) [26.a] Wherein, in the First Operable State, Voltage Conversion Circuit Provides First Regulated Voltage to SDRAM Devices Using First Pre-Regulated Voltage

995. Claim 26 requires "*[t]he memory module of claim 25, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage*."

996. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

997. As shown in the table below, claim element [26.a] is very similar to claim element [18.a]:

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Claim 18	Claim 26
[18.a] The memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and	[26.a] The memory module of claim 25, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and

998. As discussed above with reference to claim element [18.a], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶880-890.

b) [26.b] Wherein, in the Second Operable State, Voltage Conversion Circuit Provides First Regulated Voltage to SDRAM Devices Using Second Pre-Regulated Voltage

999. Claim 26 further requires "*wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage*."

1000. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1001. As shown in the table below, claim element [26.b] is very similar to claim element [18.b]:

Claim 18	Claim 26
[18.b] wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.	[26.b] wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.

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1002. As discussed above with reference to claim element [18.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶891-895.

27. Claim 27 is Unpatentable

1003. Claim 27 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

1004. Claim 27 requires "*[t]he memory module of claim 26, wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via a first diode*."

1005. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1006. As shown in the table below, claim 27 is very similar to claim element [20.a]:

Claim 20	**Claim 27**
[20.a] The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and	[27] The memory module of claim 26, wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via a first diode.

1007. As discussed above with reference to claim element [20.a], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶910-913.

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28. Claim 28 is Unpatentable

1008. Claim 28 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

1009. Claim 28 requires "*[t]he memory module of claim 27, wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via a second diode*."

1010. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1011. As shown in the table below, claim 28 is very similar to claim element [20.b]:

Claim 20	**Claim 28**
[20.b] wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.	[28] The memory module of claim 27, wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via a second diode.

1012. As discussed above with reference to claim element [20.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶914-917.

29. Claim 29 is Unpatentable

1013. Claim 29 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

1014. Claim 29 requires "*[t]he memory module of claim 24, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage or below a second predetermined threshold voltage*."

1015. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1016. As shown in the table below, claim 29 is very similar to claim 17:

Claim 17	**Claim 29**
[17] The memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage.	[29] The memory module of claim 24, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage or below a second predetermined threshold voltage.

1017. As discussed above with reference to claim 17, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶875-878.

30. Claim 30 is Unpatentable

1018. Claim 30 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A and B) render the claim obvious.

1019. Claim 30 requires "*[t]he memory module of claim 29, wherein the first predetermined threshold voltage is above a specified operating voltage, and the second predetermined threshold voltage is below the specified operating voltage*."

1020. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1021. As shown in the table below, claim 30 is very similar to claim elements [9.b] and [11.b]:

Claims 9, 11	**Claim 30**
[9.b] wherein the first predetermined threshold voltage is above a specified operating voltage. [11.b] wherein the second predetermined threshold voltage is below the specified operating voltage, and	[30] The memory module of claim 29, wherein the first predetermined threshold voltage is above a specified operating voltage, and the second predetermined threshold voltage is below the specified operating voltage.

1022. As discussed above with reference to claim elements [9.b] and [11.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶793-796 (claim limitation [9.b]), ¶¶813-816 (claim limitation [11.b]).

* * *

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: May 16, 2022



Andrew Wolfe

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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 11,232,054
1002	File History of U.S. Patent No. 11,232,054
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	File History of U.S. Provisional Application No. 60/941,586
1006	File History of U.S. Patent Application No. 12/131,873
1007	File History of U.S. Patent Application No. 12/240,916
1008	File History of U.S. Provisional Application No. 61/512,871
1009	File History of U.S. Patent Application No. 13/559,476
1010	File History of U.S. Patent Application No. 14/489,269
1011	File History of U.S. Patent Application No. 14/840,865
1012	File History of U.S. Patent Application No. 15/934,416
1013	File History of U.S. Patent Application No. 17/138,766
1014	*SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper No. 1 (PTAB June 20, 2014) (833 Patent IPR Petition)
1015	*SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper No. 8 (PTAB December 16, 2014) (833 Patent Institution Decision)
1016	*Smart Modular Techs. Inc. v. Netlist, Inc.*, IPR2014-01370, Paper No. 8 (PTAB September 22, 2014) (833 Patent IPR Corrected Petition)
1017	*Smart Modular Techs. Inc. v. Netlist, Inc.*, IPR2014-01370, Paper No. 13 (PTAB March 13, 2015) (833 Patent Institution Decision)

Exhibit #	Description
1018	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00649, Paper No. 1 (PTAB January 13, 2017) (833 Patent IPR Petition)
1019	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00649, Paper No. 7 (PTAB July 24, 2017) (833 Patent Institution Decision)
1020	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00692, Paper No. 1 (PTAB January 17, 2017) (831 Patent IPR Petition)
1021	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00692, Paper No. 25 (PTAB July 5, 2018) (831 Patent Final Written Decision)
1022	*Micron Tech., Inc. et al. v. Netlist, Inc.*, IPR2022-00418, Paper No. 2 (PTAB January 14, 2022) (831 Patent IPR Petition)
1023	U.S. Patent Application Publication No. 2006/0174140 to Harris *et al.*
1024	U.S. Patent No. 7,724,604 to Amidi *et al.*
1025	U.S. Patent Application Publication No. 2006/0080515 to Spiers *et al.*
1026	JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (January 2005) (“JESD79-2B”)
1027	JEDEC Standard, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20 (March 2007) (“JESD82-20”)
1028	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification, JESD205 (March 2007) (“JESD205”)
1029	Declaration of Julie Carlson for JESD82-20 and JESD205
1030	U.S. Patent No. 7,719,866 to Boldo
1031	PCI Local Bus Specification Revision 2.2 (1998)

Exhibit #	Description
1032	Mohan et al., Power Electronics: Converters, Applications, and Design (2d Ed. 1995)
1033	U.S. Patent No. 7,721,130 to Prete *et al.*
1034	U.S. Patent No. 6,798,709 to Sim *et al.*
1035	[Intentionally Omitted]
1036	[Intentionally Omitted]
1037	U.S. Patent Application Publication No. 2008/0238536 to Hayashi *et al.*
1038	U.S. Patent No. 6,856,556 to Hajeck
1039	U.S. Patent Application Publication No. 2010/0257304 to Rajan *et al.*
1040	Texas Instruments, TPS51020 Datasheet (December 2003)
1041	Fairchild Semiconductor, FAN5026 Datasheet (October 2005)
1042	Murata Power Supply Reference Guide for Xilinx FPGAs (September 2006)
1043	Murata Power Supply Reference Guide for Altera FPGAs (February 2008)
1044	U.S. Patent Application Publication No. 2010/0205470 to Moshayedi *et al.*
1045	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) ("JESD79")
1046	JEDEC Standard, DDR3 SDRAM, JESD79-3C (September 2007) ("JESD79-3A")
1047	U.S. Patent No. 7,023,187 to Shearon *et al.*

Exhibit #	Description
1048	Murata, DC-DC Converter Specification (DRAFT), MPD4S014S Datasheet (January 21, 2008)
1049	Micron, NAND Flash Memory Datasheet (January 2006)
1050	U.S. Patent No. 7,692,938 to Petter
1051	[Intentionally Omitted]
1052	[Intentionally Omitted]
1053	[Intentionally Omitted]
1054	U.S. Patent No. 11,016,918
1055	U.S. Patent Application Publication No. 2008/0101147 to Amidi
1056	U.S. Patent No. 5,563,839 to Herdt *et al.*
1057	U.S. Patent No. 6,693,840 to Shimada *et al.*
1058	Lenk, John D., *Simplified Design of Switching Power Supplies* (1995)
1059	U.S. Patent No. 7,061,214 to Mayega *et al.*
1060	U.S. Patent No. 5,630,096 to Zuravleff *et al.*
1061	Analog Devices, ADM1066 Datasheet (2006)
1062	Alan Moloney, *Power-Supply Management—Principles, Problems, and Parts*, Analog Dialogue (May 2006)
1063	National Semiconductor, LMC6953 PCI Local Bus Power Supervisor Datasheet (October 1996)
1064	U.S. Patent Application Publication No. 2007/0136523 to Bonella *et al.*
1065	U.S. Patent Application Publication No. 2009/0034354 to Resnick

Exhibit #	Description
1066	U.S. Patent No. 10,672,458 to Shaeffer *et al.*
1067	LatticeXP Family Data Sheet (March 2006)
1068	Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
1069	First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Jan. 18, 2022)
1070	Netlist's motion to dismiss the First Amended Complaint, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Feb. 16, 2022)
1071	Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
1072	Answer in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Apr. 12, 2022)
1073	Amended Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed May 3, 2022)

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A memory module comprising:
1.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
1.c	a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;
1.d	[1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and [3] a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections, [4] wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and [5] wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.
2.a	2. The memory module of claim 1, wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude; and
2.b	wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes.
3	3. The memory module of claim 1, wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts.
4.a	4. The memory module of claim 1, further comprising:

Ref. #	Listing of Challenged Claims
4.b	a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage,
4.c	wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.
5.a	5. The memory module of claim 4, further comprising:
5.b	a controller coupled to the voltage monitor circuit;
5.c	wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.
6.a	6. The memory module of claim 1, further comprising:
6.b	a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage,
6.c	wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.
7.a	7. The memory module of claim 6, further comprising:
7.b	a controller coupled to the voltage monitor circuit;
7.c	wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.
8.a	8. The memory module of claim 1, further comprising:
8.b	a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections,
8.c	wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller.

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Ref. #	Listing of Challenged Claims
9.a	9. The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage, and
9.b	wherein the first predetermined threshold voltage is above a specified operating voltage.
10	10. The memory module of claim 9, wherein the first predetermined threshold voltage is ten percent above the specified operating voltage.
11.a	11. The memory module of claim 9, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage, and
11.b	wherein the second predetermined threshold voltage is below the specified operating voltage, and
11.c	wherein the memory module transitions from a first operable state to a second operable state in response to the signal.
12	12. The memory module of claim 11, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage.
13	13. The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage.
14	14. The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system.
15	15. The memory module of claim 1, wherein two of the at least three buck converters are configured to operate as a dual-buck converter.
16.a	16. A memory module comprising:
16.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;
16.c	a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

Ref. #	Listing of Challenged Claims
16.d	[1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, [3] the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages; and
16.e	[1] a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage, [2] wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.
17	17. The memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage.
18.a	18. The memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and
18.b	wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.
19.a	19. The memory module of claim 18, wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit, and
19.b	wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit.
20.a	20. The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and

Ref. #	Listing of Challenged Claims
20.b	wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.
21.a	21. The memory module of claim 16, further comprising:
21.b	a first circuit having a first input, a second input and an output, the first input coupled to a first pre-regulated voltage, the second input coupled to a second pre-regulated voltage, the output coupled to the voltage conversion circuit,
21.c	wherein the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a supply voltage,
21.d	wherein, in the first operable state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the first pre-regulated voltage, and
21.e	wherein, in the second state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the second pre-regulated voltage.
22	22. The memory module of claim 21, wherein the first circuit includes a first diode coupled between the first input and the output and a second diode coupled between the second input and the output.
23.a	23. The memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and
23.b	wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.
24.a	24. A memory module comprising:
24.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;
24.c	a voltage conversion circuit configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

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Ref. #	Listing of Challenged Claims
24.d	[1] a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, [3] wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages; and
24.e	[1] a controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface of the PCB, the voltage monitor circuit configured to monitor the input voltage, [2] wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and [3] wherein the one or more operations include a write operation to transfer data into non-volatile memory.
25	25. The memory module of claim 24, wherein, in response to the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.
26.a	26. The memory module of claim 25, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and
26.b	wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.
27	27. The memory module of claim 26, wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via a first diode.
28	28. The memory module of claim 27, wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via a second diode.
29	29. The memory module of claim 24, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage or below a second predetermined threshold voltage.

Ref. #	Listing of Challenged Claims
30	30. The memory module of claim 29, wherein the first predetermined threshold voltage is above a specified operating voltage, and the second predetermined threshold voltage is below the specified operating voltage.

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