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Paper 30
Entered: August 28, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00418
Patent 8,301,833 B1

Before GEORGIANNA W. BRADEN, SHEILA F. McSHANE, and KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

SZPONDOWSKI, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

We instituted *inter partes* review of claims 1, 3–17, and 19–30 of U.S. Patent 8,301,833 B1, issued on October 30, 2012 (Ex. 1001, "the '833 patent") in response to a Petition (Paper 2, "Pet.") filed by Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively "Petitioner"). Paper 14 ("Inst. Dec."). During the trial, Netlist, Inc. ("Patent Owner") filed a Response to the Petition (Paper 19, "PO Resp."), Petitioner filed a Reply (Paper 22, "Reply"), and Patent Owner filed a Sur-reply (Paper 23, "Sur-reply").

An oral hearing was held on June 7, 2023, and a copy of the transcript was entered into the record. Paper 29 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This Decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of the claims on which we instituted trial. Based on the complete record, Petitioner has shown by a preponderance of the evidence that claims 1, 3–17, and 19–30 of the '833 patent are unpatentable.

II. BACKGROUND

A. Real Parties-in-Interest

Petitioner identifies itself as the real party-in-interest. Pet. 64. Patent Owner also identifies itself as the real party-in-interest. Paper 3 ("Patent Owner's Mandatory Disclosure"), 1.

B. Related Matters

The parties advise that the '833 patent is the subject of *Netlist, Inc. v. Micron Technology, Inc., et al.*, 6:21-cv-00430 (W.D. Tex.). Pet. 64; Paper 3, 2. Petitioner also advises that the '833 patent has been the subject of the following three *inter partes* review proceedings: IPR2014-00994,

IPR2014-01370, and IPR2017-00649. Pet. 64. Additionally, Petitioner advises that "a nearly identical claim to the '833 Patent's claim 15 was invalidated as obvious in IPR2017-00692." *Id.* at 65.

C. The '833 Patent (Ex. 1001)

The '833 patent is titled "Non-Volatile Memory Module" and is generally directed to "a memory system which can communicate with a host system such as a disk controller of a computer system." Ex. 1001, codes (54), (57).

The '833 patent states that "[n]on-volatile memory can generally maintain stored information while power is not applied to the non-volatile memory," so, "[i]n certain circumstances, it can therefore be useful to backup volatile memory using non-volatile memory." *Id.* at 1:28–31. The invention in the '833 patent relates to a configuration of hybrid memory systems that "can include volatile and non-volatile memory and a controller which are configured such that the controller backs up the volatile memory using the non-volatile memory in the event of a trigger condition," such as a power failure or power reduction. *Id.* at code (57), 3:65–67, 17:66–18:1. "[T]he volatile memory system can be operated at a reduced frequency during backup and/or restore operations which can improve the efficiency of the system and save power." *Id.* at 4:41–44.

Figure 9, which depicts a flowchart of an example method of a volatile memory subsystem operating at a reduced rate in back-up mode, is reproduced below:

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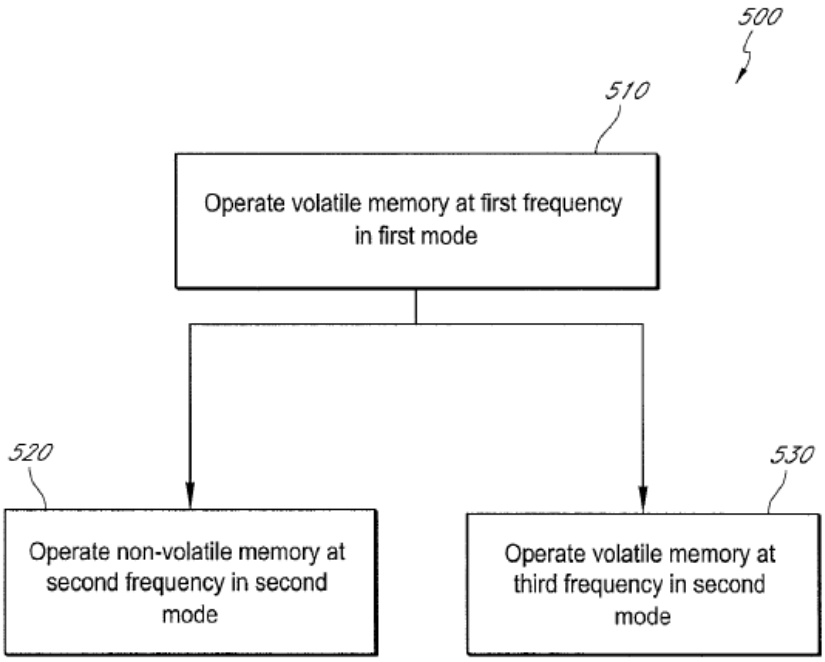

FIG. 9

Id. at 3:45–48. Figure 9 depicts block 510, "[o]perate volatile memory at first frequency in first mode," block 520, "[o]perate non-volatile memory at second frequency in second mode," and block 530, "[o]perate volatile memory at third frequency in second mode." The memory system "may switch from the first mode of operation to the second mode of operation in response to a trigger condition," such as "a power failure condition." *Id.* at 17:64–18:1. The second mode of operation may include, for example, backup and/or restore operations. *Id.* at 18:1–7. The '833 patent also describes that "[t]he third frequency can be less than the first frequency," and "can be approximately equal to the second frequency." *Id.* at 18:8–10.

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D. Illustrative Claims

Among the challenged claims, claims 1 and 15 are independent. Independent claim 15 is representative and is reproduced below.

15. A memory system operatively coupled to a host system, the memory system comprising:

> a volatile memory subsystem operable at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;
>
> and a non-volatile memory subsystem operable at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem,
>
> the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

Ex. 1001, 21:61–22:11.

E. Prior Art and Asserted Challenge to Patentability

Petitioner asserts that claims 1, 3–17, and 19–30 are unpatentable on the following challenge (Pet. 2):[1]

[1] Petitioner also asserts, as a separate challenge, that Patent Owner is collaterally estopped from re-litigating the issue of validity of claims 1 and 15 of the '833 patent based upon the Final Written Decision in IPR2017-00692, where claim 15 of U.S. Patent No. 8,874,831, which is a continuation-in-part of the '833 patent, was determined invalid over the combination of Best, Bonella, and Mills. Pet. 18–24; IPR2017-00692, Paper 25 at 31–40. Petitioner asserts that claim 15 of the '831 patent is substantively identical to claims 1 and 15 of the '833 patent. Pet. 18. As we

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Claim(s) Challenged	35 U.S.C. §[2]	Reference(s)/Basis
1, 3–17, 19–30	§ 103(a)	Best,[3] Bonella,[4] Mills[5]

In support of its proposed challenge, Petitioner relies on the Declaration of Ron Maltiel. *See* Ex. 1003. Patent Owner relies on the Declaration of Dr. Steven Przybylski. Ex. 2004. Deposition transcripts have been submitted for both witnesses. Exs. 1025 (deposition of Dr. Przybylski), 2005 (deposition of Mr. Maltiel).

III. ANALYSIS

A. Legal Standards

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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stated in our Institution Decision, collateral estoppel is not an appropriate *separate* ground for *inter partes* review. Inst. Dec. 19 (citing 35 U.S.C. § 311(b), "A petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent *only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications*."). Additionally, even if had been presented appropriately (i.e., as an argument prohibiting Patent Owner from contesting the unpatentability of claims 1 and 15 over Best, Bonella, and Mills rather than as a separate ground), because we determine that Petitioner has established that claims 1 and 15 are unpatentable based upon the combination of Best, Bonella, and Mills, it is not necessary to consider Petitioner's arguments regarding collateral estoppel.

[2] Because the '833 patent issued from a patent application that was filed before March 16, 2013, patentability is governed by the version of 35 U.S.C. § 103 preceding the Leahy-Smith America Invents Act ("AIA"), Pub L. No. 112–29, 125 Stat. 284 (2011).

[3] US 2010/0110748 A1, published May 6, 2010 (Ex. 1006).

[4] US 2007/0136523 A1, published June 14, 2007 (Ex. 1008).

[5] US 6,026,465, issued Feb. 15, 2000 (Ex. 1009).

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invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see KSR*, 550 U.S. at 418. Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418; *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine "must be supported by a 'reasoned explanation'").

B. Level of Ordinary Skill in the Art

Petitioner asserts a person of ordinary skill in the art "would have been a person with a bachelor's degree in materials science, electrical engineering, computer engineering, computer science, or in a related field

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and at least one year of experience with the design or development of semiconductor non-volatile memory circuitry or systems." Pet. 4 (citing Ex. 1003 ¶¶ 48–52).

Patent Owner "disputes Petitioners' definition of the level of a person of ordinary skill in the art . . . [but] resolution of such dispute is not necessary for the Board to determine the validity of the Challenged Claims." PO Resp. 13. Dr. Przybylski testifies that he does not take exception to the education and years of experience identified by Mr. Maltiel, however, he believes that "an individual with that level of experience would have less knowledge and familiarity than Mr. Maltiel presumes, as described herein." Ex. 2004 ¶ 42. We do not discern any further explanation of that statement in the testimony nor does Patent Owner propose any alternative qualifications of a person of ordinary skill in the art.

In our Institution Decision, we preliminarily adopted Petitioner's unopposed[6] proposed level of ordinary skill in the art. Inst. Dec. 17–18. Nothing in the full record persuades us that our preliminary finding as to the level of ordinary skill in the art was incorrect. Accordingly, we maintain our adoption of Petitioner's proposed level of ordinary skill in the art, as consistent with the level of ordinary skill in the art reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

C. Claim Construction

Petitioner provides the parties' proposed constructions from the related district court litigation, but asserts that "[t]hese construction disputes from the related litigations do not affect the outcome of this Petition with

[6] Patent Owner did not challenge the proposed level of ordinary skill in the art in the Preliminary Response. *See generally* Paper 11.

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respect to any claim." Pet. 9 (citing Exs. 1012, 1013). Petitioner also asserts that the term "clock frequency" was construed in IPR2014-00994, Paper 8 at 6 as "identification of a clock running at a particular frequency," which Petitioner contends is consistent with the '833 patent's Specification. *Id.* (citing Ex. 1001, 17:25–18:13; Ex. 1003 ¶ 136). Petitioner states that it has applied this construction of "clock frequency" in its analysis. *Id.*

Patent Owner asserts that "a first mode of operation" and "a second mode of operation," as recited in independent claims 1 and 15, require construction. PO Resp. 15–27. Patent Owner contends that Petitioner improperly interprets "a first mode of operation" as "the operation of the system when no write-back trigger is detected," and "a second mode of operation" as "the operation of the system when a power-loss event write-back trigger is detected." *Id.* at 15.

1. "a first mode of operation"

a) The Parties' Contentions

Patent Owner contends that "a first mode of operation" should be construed as "a mode of operation wherein no backup or restore operations are performed, wherein the non-volatile memory subsystem does not communicate with the volatile memory subsystem or the host system." PO Resp. 16.

According to Patent Owner, the '833 patent describes the first mode of operation as having "three key features." PO Resp. 16 (citing Ex. 2004 ¶¶ 45–46).

First, Patent Owner contends that during a first mode of operation, "data is communicated between the volatile memory subsystem and the host

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system." PO Resp. 16 (citing Ex. 1001, 2:18–22, 2:35–37, 2:63–66, 15:6–10, Figs. 6, 7; Ex. 2004 ¶ 47).

Second, Patent Owner contends that during the first mode of operation, "memory system 10 is not performing a backup or restore operation," and cites to disclosure from the '833 patent allegedly supporting this assertion. PO Resp. 16–17 (citing Ex. 1001, 16:43–48, 9:15–17, 19:41–44). Patent Owner asserts, a person of ordinary skill in the art "would understand that no backup or restore operations are occurring during the 'first mode of operation.'" *Id.* (citing Ex. 2004 ¶ 48).

Third, Patent Owner contends that during the first mode of operation, "the non-volatile memory subsystem does not communicate with the volatile memory subsystem or the host." PO Resp. 17 (citing Ex. 2004 ¶ 49). Patent Owner argues that "the specification expressly touts the importance of isolating the non-volatile memory subsystem during the first mode of operation as advantageous." *Id.* (citing Ex. 1001, 4:5–9, 8:57–62; Ex. 2004 ¶¶ 49–50). Patent Owner argues "[b]ecause of the importance of isolating the non-volatile memory subsystem during the first mode of operation, the '833 Patent discloses multiple examples of 'isolation devices' used to isolate the data bus and address busses of the host system and the volatile memory system when the volatile memory is interacting with the host system." *Id.* at 18. In support, Patent Owner cites to the embodiments disclosed in Figures 3, 4A, and 4B, and their associated circuit 52, which is described as a "switch" or "isolation device." *Id.* at 18–21.

In Reply, Petitioner contends that Patent Owner's proposed construction is improper and seeks "to fundamentally modify the claim language." Reply 1–2. Petitioner contends that this term is clear on its face

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because the claim language recites the requirements for the "first mode of operation," and, therefore, this term need not be construed. *Id.* at 2–4. Petitioner also argues that some dependent claims already recite the limitations Patent Owner proposes for the independent claims. *Id.* at 4–5. Petitioner further argues that Dr. Przybylski's testimony is unreliable because, among other things, it cites to portions of the Specification that refer to embodiments or to portions of the Specification that do not use the term "first mode of operation" and omit embodiment language, such as "for example," from the cited portions of the Specification. *Id.* at 5–6.

In Sur-reply, Patent Owner argues that Petitioner's application of Best to the "first mode of operation" defines the term with respect to backup or restore operations. Sur-reply 2. Patent Owner contends that the Specification and both experts support its proposed construction. *Id.* at 3–5. Regarding Petitioner's claim differentiation argument, Patent Owner argues that Petitioner ignores claim scope differences between the independent and dependent claims. *Id.* at 3–4. For example, Patent Owner argues that "decouple from," as recited in claim 16, conveys a narrower claim scope than "does not communicate with." *Id.* at 3. Patent Owner also reiterates that the '833 patent "consistently and repeatedly teaches the importance of not allowing the non-volatile memory to communicate in the first mode in order to preserve the memory system's integrity and ensure its operation is not adversely affected." *Id.* at 6; *see also id.* at 7–8.

b) Analysis

We construe each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent," the same

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standard used to construe the claim in a civil action. 37 C.F.R. § 42.100(b) (2019). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–1317 (Fed. Cir. 2005) (en banc)). "]T]he claims themselves provide substantial guidance as to the meaning of particular claim terms," but "do not stand alone." *Phillips*, 415 F.3d at 1314–1315. They are part of "'a fully integrated written instrument,' consisting principally of a specification that concludes with the claims," and must therefore "be read in view of the specification." *Id.* at 1315 (quoting *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 978–79 (Fed. Cir. 1995)). There is a "heavy presumption," however, that a claim term carries its ordinary and customary meaning. *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002) (citation omitted). "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips*, 415 F.3d at 1313.

Independent claim 15 recites, in part, "the memory system is in *a first mode of operation* in which data is communicated between the volatile memory subsystem and the host system." Ex. 1001, 21:64–22:2 (emphasis added). We agree with Petitioner that the plain language of the claim clearly recites the requirements for the "first mode of operation," i.e., data is communicated between the volatile memory subsystem and the host system. *See* Reply 3. This language replicates the first of the "three key features"

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that Patent Owner contends is part of the "first mode of operation." PO Resp. 16.

Patent Owner's proposed construction seeks to limit "a first mode of operation" to particular embodiments disclosed in the Specification, which are themselves exemplary embodiments. Patent Owner supports its contentions that "no backup or restore operations are performed" in the "first mode of operation" with citations from the '833 patent, but each of Patent Owner's citations explicitly refers to examples and "certain embodiments."[7] *See* Ex. 1001, 16:43–48 ("*For example*, when the memory system 10 is not performing a backup or restore operation and is communicating with the host system (e.g., normal operation), the volatile memory system clock signal 420 may be provided by the multiplexer 422 to the volatile memory PLL block 424.") (emphasis added), 9:15–17 ("*In certain embodiments*, the memory system 10 is in the first state when no trigger condition . . . is present") (emphasis added), 19:41–44 ("*For example*, the memory system 10 may be in the first mode of operation when no trigger condition has occurred and the memory system is not performing a backup and/or restore operation") (emphasis added).

Patent Owner similarly provides citations to exemplary embodiments in support of its contention that the "non-volatile memory subsystem does not communicate with the volatile memory subsystem or the host system" during a "first mode of operation." Patent Owner asserts that "the specification expressly touts the importance of isolating the non-volatile memory subsystem during the first mode of operation as advantageous," (PO

[7] In its citations, Patent Owner omits the language from the Specification referring to "for example" or "certain embodiments."

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Resp. 17) but Patent Owner's citations to the '833 patent again are directed to "certain embodiments." *See* Ex. 1001, 4:5–9 ("*In certain embodiments*, the memory system can be configured such that the operation of the volatile memory is not adversely affected by the non-volatile memory or by the controller when the volatile memory is interacting with the host system. For example . . . .") (emphasis added); 8:22–23, 8:57–62 ("The memory system 10 *of certain embodiments* is configured to be operated in at least two states . . . The isolation or operational decoupling of the volatile memory subsystem 30 from the on-volatile memory subsystem in the first state can preserve the integrity of the operation of the memory system 10 during periods of operation in which signals (e.g., data) are transmitted between the host system and the volatile memory subsystem 30") (emphasis added).

Patent Owner's reliance on switch 52 in the Figure 3, 4A, and 4B embodiments, and supporting citations is similarly unavailing. *See, e.g.*, Ex. 1001, 4:61–64 ("*In certain embodiments*, the memory system 10 includes at least one circuit 52 configured to selectively operatively decouple the controller 62 from the volatile memory subsystem 30") (emphasis added); 6:63–7:4 ("*In certain embodiments*, the at least one circuit 52 comprises one or more switches coupled to the volatile memory subsystem 30, to the controller 62, and to the host computer (e.g., via the interface 22)") (emphasis added); 7:4–6 ("In addition, *in certain embodiments* the at least one circuit 52 selectively operatively couples and decouples the volatile memory subsystem 30 and the host system") (emphasis added); 7:11–16 ("*In certain such embodiments*, the at least one circuit 52 can comprise one or more switches 172 coupled to the controller 62 (e.g., logic element 70) and to the volatile memory subsystem 30 . . .") (emphasis added).

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We are not persuaded that the proper interpretation of "a first mode of operation" requires that we read in the unclaimed features of these embodiments. Claims are not limited to specific embodiments described in the specification. *See Phillips*, 415 F.3d at 1323.

> Though understanding the claim language may be aided by explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim. For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment.

SuperGuide Corp. v. DirecTV Enterprises, Inc., 358 F.3d 870, 875 (Fed Cir. 2004) (citing *Electro Med. Sys. S.A. v. Cooper Life Sci., Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994)); *see also Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1366 (Fed. Cir. 2012) ("It is likewise not enough that the only embodiments, or all of the embodiments, contain a particular limitation. We do not read limitations from the specification into claims; we do not redefine words."). The mere description of a preferred embodiment is not a limiting definition for a claim term. *See E-Pass Techs., Inc. v. 3Com Corp.*, 343 F.3d 1364, 1369 (Fed. Cir. 2003); *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 908–09 (Fed. Cir. 2004).

Patent Owner's contention that the '833 patent includes "numerous and consistent teachings describing the importance of the structures used to perform the claimed functions" is not supported by the '833 patent. Although the specification's emphasis of a particular feature's importance to the invention can indicate "what the patentee had claimed and disclaimed," *see SafeTCare Mfg., Inc. v. Tele-Made, Inc.*, 497 F.3d 1262, 1269–70 (Fed. Cir. 2007), Patent Owner has not shown that here. The

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Federal Circuit has acknowledged "the difficulty in drawing the 'fine line between construing the claims in light of the specification and improperly importing a limitation from the specification into the claims.'" *Continental Circuits LLC v. Intel Corp.*, 915 F.3d 788, 797 (Fed. Cir. 2019) (citing *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1305 (Fed. Cir. 2011)). To avoid improperly importing limitations into the claims, "it is important to keep in mind that the purposes of the specification are to teach and enable those of skill in the art to make and use the invention and to provide a best mode for doing so." *Phillips*, 415 F.3d at 1323.

The written description includes embodiments with a switch that may operate to isolate the non-volatile memory subsystem from the volatile memory subsystem or the host system, but does not indicate that this is an important or essential part of the invention, or that it is important or essential in distinguishing the prior art. Patent Owner focuses on the following two statements from the Specification: (1) "In certain embodiments, the memory system can be configured such that the operation of the volatile memory is not adversely affected by the non-volatile memory or by the controller when the volatile memory is interacting with the host system"; and (2) "The isolation or operational decoupling of the volatile memory subsystem 30 from the non-volatile memory subsystem in the first state can preserve the integrity of the operation of the memory system 10 during periods of operation in which signals (e.g., data) are transmitted between the host system and the volatile memory subsystem 30." *See* PO Resp. 17 (citing Ex. 1001, 4:5–9, 8:57–62); Sur-reply 6. However, as discussed above, these statements are limited to "certain embodiments" and are not statements clearly limiting or expressly requiring that the claimed "first

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mode of operation" include this functionality, or setting forth its importance. *See, e.g.*, *Continental Circs.*, 915 F.3d at 797; *Hill-Rom Services, Inc. v. Stryker Corp.*, 755 F.3d 1367, 1372–1373 (Fed. Cir. 2014). Indeed, the '833 patent expressly states that "[a]lthough this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting." Ex. 1001, 20:64–67. Nothing in the language of the Specification suggests that the "first mode of operation" should be limited to operations when "no backup or restore operations are performed" and "the non-volatile memory subsystem does not communicate with the volatile memory subsystem or the host system." Thus, there is no reason to depart from the plain and ordinary meaning of a "first mode of operation," as recited in the claim language.

Moreover, we find Patent Owner's assertions that Mr. Maltiel agrees with its interpretation of this term to be disingenuous. *See* Sur-reply 4–6. Patent Owner cites to testimony on pages 58 and 59 of Mr. Maltiel's deposition in support of its assertions that Mr. Maltiel testified that the non-volatile memory does not communicate with the volatile memory in the first mode (*id.* at 4–5), but when Mr. Maltiel's testimony is read in context, it is clear that Mr. Maltiel was being questioned about certain passages in the '833 patent, not about the interpretation of a "first mode of operation" as recited in the claims. *See* Ex. 2005, 53:3–54:20 (asking Mr. Maltiel to read aloud the sentences beginning at Ex. 1001, 2:18, and 2:34); *see also id.* at 59:5–8 ("Q. And isn't it true that *neither of those passages* discuss the communication of data between the volatile memory and the nonvolatile memory in the first mode of operation?") (emphasis added); *see* Tr. 38:9–16.

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As discussed above, there is no dispute that during a first mode of operation "data is communicated between the volatile memory subsystem and the host system." PO Resp. 16; Ex. 2005, 56:20–57:1. This is precisely what the claim language recites. For the reasons explained above, we decline to import limitations into the claim, as Patent Owner urges. *See, e.g.*, *SuperGuide Corp.*, 358 F.3d at 875 ("Though understanding the claim language may be aided by explanations contained in the written description, it is important not to import into a claim limitations that are not a part of the claim.")

Accordingly, we agree with Petitioner that the term "a first mode of operation" does not require construction, and its meaning is evident from the claim language, i.e., "a first mode of operation in which data is communicated between the volatile memory subsystem and the host system."

2. "a second mode of operation"

a) The Parties' Contentions

Patent Owner contends that "a second mode of operation" should be construed as "a backup or restore mode of operation wherein the host system does not communicate with the volatile memory subsystem." PO Resp. 23.

According to Patent Owner, the '833 patent "makes clear that the second mode of operation is a mode in which backup or restore operations are performed." PO Resp. 23 (citing Ex. 1001, 7:41–48, 10:33–58, 18:1–7; Ex. 2004 ¶ 61). Patent Owner also contends that Mr. Maltiel agrees with this interpretation. *Id.* (citing Ex. 2005, 68:5–8). As with the "first mode of operation," Patent Owner similarly relies on circuit 52 (switch) and switch 174 as shown in Figures 3, 4A and 4B, respectively, which show

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"that the host system may be isolated from the volatile memory subsystem using isolation devices, such as switches." *Id.* at 24–26 (citing Ex. 1001, 7:20–22, 7:26–29, 8:22–35, 10:19–23, Figs. 3, 4A, 4B; Ex. 2004 ¶¶ 62–64, 66). Similarly, Patent Owner contends that Mr. Maltiel agrees that "in the second mode of operation, when backup or restore operations are performed, the volatile memory does not communicate with the host." *Id.* at 26 (citing Ex. 2005, 68:13–19).

In Reply, Petitioner contends that Patent Owner's proposed construction is improper and seeks "to fundamentally modify the claim language." Reply 1–2. Petitioner contends that this term is clear on its face because the claim language clearly recites the requirements for the "second mode of operation," and, therefore, this term need not be construed. *Id.* at 2–4. Petitioner also argues that some dependent claims already recite the limitations Patent Owner proposes for the independent claims. *Id.* at 4–5. Petitioner also argues that Dr. Przybylski's testimony is unreliable because, among other things, it cites to portions of the Specification that refer to embodiments or do not use the term "second mode of operation" and omits embodiment language, such as "for example," from the cited portions of the Specification. *Id.* at 5–6.

In Sur-reply, Patent Owner argues that Petitioner's application of Best to the "second mode of operation" defines the term with respect to backup or restore operations. Sur-reply 2. Patent Owner contends that the Specification and both experts support its proposed construction. *Id.* at 3–5. Regarding Petitioner's claim differentiation argument, Patent Owner argues that Petitioner ignores claim scope differences between the independent and dependent claims. *Id.* at 3–4. For example, Patent Owner argues that the

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language in dependent claim 28, which recites "wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem," conveys a narrower claim scope than the language in claim 15. *Id.* Patent Owner also reiterates that the '833 patent "consistently and repeatedly teaches the importance of not allowing the non-volatile memory to communicate in the first mode in order to preserve the memory system's integrity and ensure its operation is not adversely affected." *Id.* at 6; *see also id.* at 7–8.

b) Analysis

Independent claim 15 recites, in part, "the memory system is in *a second mode of operation* in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem." Ex. 1001, 22:4–7 (emphasis added). We agree with Petitioner that the plain language of the claim clearly recites the requirements for the second mode of operation, i.e., data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem. Reply 3.

We do not adopt Patent Owner's proposed construction for the same reasons as discussed above for "a first mode of operations." For example, we find that Patent Owner's proposed construction seeks to limit "a second mode of operation" to particular embodiments disclosed in the Specification, which are themselves exemplary embodiments. *See* Ex. 1001, 7:41–48 ("*Certain embodiments* described herein utilize the non-volatile memory subsystem 40 as a flash 'mirror' to provide backup of the volatile memory subsystem 30 . . .") (emphasis added); 10:33–58 (*In certain embodiments*, the memory system 10 protects the operation of the volatile memory when

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communicating with the host-system and provides backup and restore capability in the event of a trigger condition such as a power failure") (emphasis added); 18:1–7 ("*In certain embodiments*, the second mode of operation includes both backup and restore operations as described herein. *In other embodiments*, the second mode of operation includes backup operations but not restore operations. *In yet other embodiments*, the second mode of operation includes restore operations but not backup operations") (emphasis added). We note that the '833 patent supports that the "second mode of operation" could be a backup and restore operation, but not that it is *limited to* a backup and restore operation, as Patent Owner argues.

Patent Owner's reliance on switch 52 in the Figure 3, 4A, and 4B embodiments, and supporting citations, to support that the host system may be isolated from the volatile memory subsystem, are similarly unavailing, for the same reasons set forth above. *See, e.g.,* Ex. 1001, 7:20–29 (referring to "*certain embodiments*"), 8:22–35 ("The memory subsystem 10 *of certain embodiments* is configured to be operated in at least two states . . . a second state in which the volatile memory subsystem 30 is operatively coupled to the controller 62 to allow data to be communicated between the volatile memory subsystem 30 and the non-volatile memory subsystem 40 via the controller 62") (emphasis added).

Moreover, we again find Patent Owner's assertions that Mr. Maltiel agrees with its interpretation of this term to be disingenuous. *See* PO Resp. 23, 26; Sur-reply 4–6. Patent Owner cites to testimony on page 68 of Mr. Maltiel's deposition in support of its assertions that Mr. Maltiel agrees that backup or restore operations are performed in the second mode and testified that the non-volatile memory does not communicate with the host in

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the second mode (PO Resp. 23, 26; Sur-reply 4–5), but when Mr. Maltiel's testimony is read in context, it is clear that Mr. Maltiel was being questioned about certain passages in the '833 patent, not about the interpretation of a "second mode of operation" as recited in the claims. *See* Ex. 2005, 63:5–21 (asking Mr. Maltiel to read the paragraph beginning at Ex. 1001, 6:63).

There appears to be no dispute that during a second mode of operation "data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem," as recited in the claim language. For the reasons explained above, we decline to import limitations into the claim, as Patent Owner urges. *See, e.g.*, *SuperGuide Corp.* 58 F.3d at 875. Accordingly, we agree with Petitioner that the term "a second mode of operation" does not require construction, and its meaning is evident from the claim language, i.e., "a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem."

D. Alleged Obviousness Over Best, Bonella, and Mills

Petitioner contends claims 1, 3–17, and 19–30 would have been obvious over the combination of Best, Bonella, and Mills. Pet. 24–60. After reviewing the entire record developed at trial, we determine that Petitioner has shown by a preponderance of the evidence that claims 1, 3–17, and 19–30 are unpatentable over Best, Bonella, and Mills.

1. Best (Ex. 1006)

Best is titled "Hybrid Volatile and Non-Volatile Memory Device" and is generally directed to a "composite, hybrid memory device including a first storage die having an array of volatile storage cells and a second storage die having an array of non-volatile storage cells disposed within an integrated

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circuit package." Ex. 1006, codes (54), (57). "The hybrid memory device includes a shared interface circuit to receive memory access commands directed to the first storage die and the second storage die and to convey read and write data between an external data path and the first and second storage dice." *Id.* at code (57).

Figure 2 of Best, which illustrates an embodiment of a hybrid, composite memory device, is reproduced below.

FIG. 2

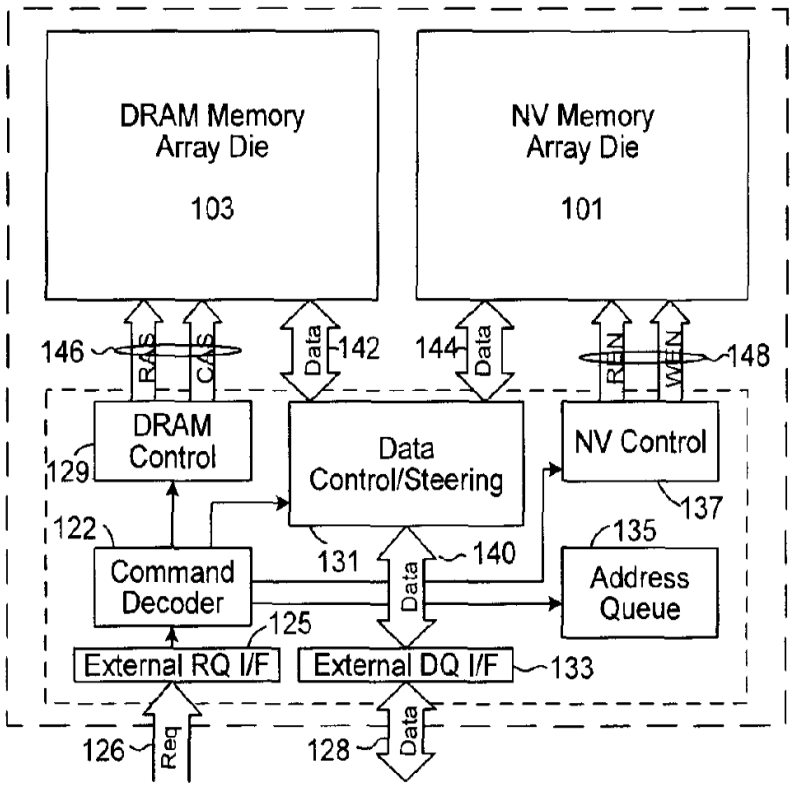

Figure 2, depicted above, illustrates an embodiment of a hybrid, composite memory device with shared interface circuitry, volatile memory implemented with DRAM die 103, and non-volatile memory implemented with Flash memory die 101. *Id.* ¶ 17. "[T]he shared interface circuitry

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includes an external request interface 125, external data interface 133, command decoder 122, address queue 135, DRAM control circuit 129, Flash control circuit 137, and data control/steering circuit 131." *Id.* "[I]ncoming control signals and addresses . . . are received in the external request interface 125 via control/address (CA) path 126, reformatted as necessary (e.g., deserialized to form a parallel command word and one or more address values) and then forwarded to the command decoder 122." *Id.* "The command decoder 122 in turn forwards address to the address queue 135 and stores memory access commands." *Id.* "[M]emory access operations may be automatically directed to either the volatile storage die or non-volatile storage die according to the memory address to be accessed." *Id.* "[C]ommand decoder 122 outputs, from the head of the command queue, an enable signal and corresponding memory access control signals to the DRAM control circuit 129 and NV control circuit 137." *Id.* ¶ 18. "[D]ata control/steering circuit 131 is used to control the transfer of data between a shared internal data bus and dedicated internal data buses associated with the volatile and non-volatile storage dice, respectively." *Id.* ¶ 20.

Figure 3 of Best, which illustrates an embodiment of a data control/steering circuit, is reproduced below.

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FIG. 3

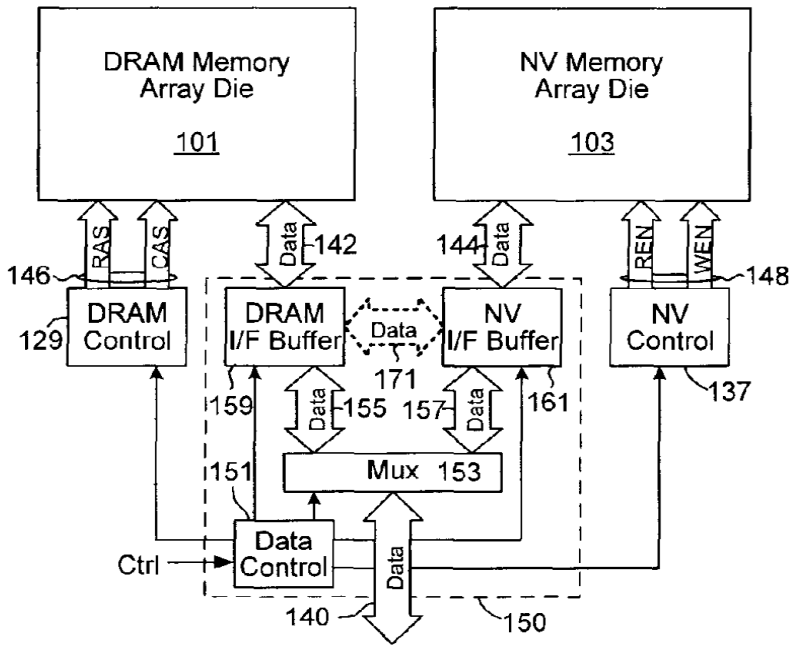

Figure 3, depicted above, illustrates an embodiment of a data control/steering circuit 150 that may be used to implement the data control/steering circuit 131 of Figure 2. *Id.* ¶ 21. "[D]ata control circuit 151 receives control signals from the command decoder that indicate the direction of data flow during a memory access operation (read or write) and whether the volatile or non-volatile storage die is the target of the memory access." *Id.*

2. Bonella (Ex. 1008)

Bonella is titled "Advanced Dynamic Disk Memory Module Special Operations" and is generally directed to "[a] memory module including a volatile memory, a non-volatile memory, and a controller that provides address, data, and control interfaces to the memories and to a host system." Ex. 1008, codes (54), (57). Bonella states that "[r]eduction of power in the

DRAM can be accomplished" by "reduc[ing] the frequency in which the DRAM is operating," which "reduces power and, in general, produces no noticeable decrease in system performance." *Id.* ¶ 49; *see id.* ¶ 50.

3. Mills (Ex. 1009)

Mills is titled "Flash Memory Including a Mode Register for Indicating Synchronous or Asynchronous Mode of Operation" and is generally directed to a "flash memory chip that can be switched into four different read modes." Ex. 1009, codes (54), (57). Mills describes several interfaces for a FLASH memory device, one of which is a synchronous FLASH interface, i.e. "a synchronous flash interface (SFI) flash memory integrated circuit 600 that incorporates a complete synchronous flash interface in a single flash memory chip." *Id.* at 16:60–63. The synchronous FLASH interface includes a clock input such that all the external operations of the device are synchronized to the rising edge of the clock. *Id.* at 17:10–25. Mills teaches that this synchronous operation is used for both read operations and write operations: "When SFI is enabled, interlace control 670 and [bank] select logic 674 operate to interlace read (and write) operations between flash bank A 610 and a flash bank B 620 . . . ." *Id.* at 17:33–39. Because "the device is interleaved internally," it "creates an average access time for sequential read accesses that is significantly less than the access time of an asynchronous flash device." *Id.* at 17:1–9.

4. Analysis of Independent Claims 1 and 15

Petitioner contends that Best, Bonella, and Mills, alone or in combination, teach each limitation of independent claims 1 and 15. Pet. 24–38. In support, Petitioner identifies certain passages and figures in the references and explains their significance with respect to the corresponding

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claim limitation. *Id.* Petitioner also provides reasons, supported by the testimony of Mr. Maltiel, why it would have been obvious to one of ordinary skill in the art to combine Best, Bonella, and Mills. *Id.* Petitioner analyzes claims 1 and 15 together.[8] *Id.* Claims 1 and 15 are substantially similar, although claim 1 is a method claim and claim 15 is a system claim. *See, e.g.*, Ex. 1001, 21:6–22, 21:61–22:11. We select claim 15 as representative.

a) "A memory system operatively coupled to a host system, the memory system comprising:"

Petitioner relies on Best to teach the preamble. Pet. 25–26. Specifically, Petitioner contends that Best's memory device (as shown in Fig. 2) is "operatively coupled to a host system" because it "includes an interface that 'receive[s] commands from a controller device.'" *Id.* at 25 (citing Ex. 1006 ¶ 14; Ex. 1003 ¶ 142). According to Petitioner, "Best discloses techniques for using the shared interface to control access by the controller device to the non-volatile and/or volatile memories." *Id.* at 25–26 (citing Ex. 1006 ¶¶ 12–17, Fig. 2; Ex. 1003 ¶¶ 140–142).

Patent Owner does not specifically respond to these arguments. *See generally* PO Resp.

After considering the evidence and arguments of the complete record, and for the reasons set forth by Petitioner, we determine that Petitioner has shown, by a preponderance of the evidence, that Best teaches the preamble.[9]

b) "a volatile memory subsystem operable at a first clock frequency when the memory system is in a first mode of

[8] Patent Owner also addresses claims 1 and 15 together. PO Resp. 35 n.3.
[9] Neither party argues whether the preamble limits claim 1 or claim 15. Because we find that the evidence supports that the prior art teaches the preamble, we need not make a determination whether the preamble of claim 1 and claim 15 is limiting.

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> *operation in which data is communicated between the volatile memory subsystem and the host system;"*

Petitioner relies on Best to teach this limitation. Pet. 26–29. Specifically, Petitioner contends that Best's DRAM teaches "a volatile memory subsystem." *Id.* at 26 (citing Ex. 1006 ¶¶ 17, 21; Ex. 1003 ¶ 145).

Petitioner further contends that Best's volatile memory (DRAM) die can be synchronous or asynchronous, and that Best "explains that a conventional synchronous DRAM interface relies on 'clock and clock-enable signals.'" *Id.* at 26–27 (citing Ex. 1006 ¶ 14). According to Petitioner, a person of ordinary skill in the art would understand this "to mean that a synchronous DRAM is '*operable at a first clock frequency*' because it is operated synchronously by a clock signal." *Id.* at 27 (citing Ex. 1003 ¶¶ 146–147). Petitioner contends that "[t]his corresponds to the usual operation of DRAM memory, as would have been well-known by a" person of ordinary skill in the art. *Id.*

Petitioner further contends that Best teaches "a first mode of operation in which data is communicated between the volatile memory subsystem and the host system" because "Best discloses a 'Shadow Operation'[10] embodiment where a portion of the DRAM is used as a write buffer for the non-volatile memory." Pet. 27 (citing Ex. 1006 ¶ 24; Ex. 1003 ¶ 148). In this embodiment, "[d]ata is stored in a fast access volatile storage die," and

[10] Best states: "In memory shadowing, memory accesses are directed first to the non-volatile storage device to enable relatively high-speed, non-degrading memory accesses, with the data eventually being written-back (retired or recorded) within the non-volatile storage in response to a triggering event referred to herein as a write-back trigger. Applications of memory shadowing include non-volatile DRAM, and rapid-access non-volatile memory." Ex. 1006 ¶ 24.

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later "a write-back trigger is detected within the shared interface circuitry," such as a "power-loss" event. *Id.* (citing Ex. 1006 ¶¶ 25–26). According to Petitioner, "[o]nce the power-loss event is detected, 'internal data transfer operations are performed to transfer data . . . from the DRAM to . . . the NV memory.'" *Id.* (citing Ex. 1006 ¶¶ 25–26; Ex. 1003 ¶ 148) (second two alterations in original). Petitioner, therefore, asserts that Best "describes at least two modes of operation: (1) the operation of the system when no write-back trigger is detected ('*a first mode of operation*'), and (2) the operation of the system when a power-loss event write-back trigger is detected such as a power-loss ('*a second mode of operation*')." *Id.* at 28 (citing Ex. 1006 ¶¶ 25–26; Ex. 1003 ¶¶ 148–150).

According to Petitioner, Best's "*first mode of operation*" "is one in which '*data is communicated between the volatile memory subsystem and the host system*' because initially 'data is stored in a fast-access volatile storage die' and only later after a write-back trigger is written to non-volatile memory." Pet. 28 (citing Ex. 1006 ¶ 25; Ex. 1003 ¶¶ 148–150).

Petitioner further contends that it would have been obvious to operate Best's DRAM at any of the frequencies described by the DDR DRAM and DDR2 DRAM standards because it "would have been merely the use of a known structure (a standard DRAM module and clock frequency) for its known use (operating as a DRAM module) to achieve a predictable result (operating a DRAM module at a standard clock frequency in Best's system)." *Id.* at 28–29 (citing Ex. 1003 ¶¶ 151–152).

Patent Owner argues that Best's "Shadow Operation" does not disclose "*a first mode of operation*." PO Resp. 35–36. Specifically, Patent Owner argues that during Best's normal operation, when no write-back

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trigger is detected, "the host communicates with ***both*** the volatile memory and the non-volatile memories." *Id.* at 36 (citing Ex. 2004 ¶ 83). According to Patent Owner, Best "repeatedly and consistently emphasizes the host's ability to communicate with both the volatile and non-volatile memories, even during 'Shadow Operation.'" *Id.* at 37 (citing Ex. 2004 ¶ 86).

We agree with Petitioner (Reply 17) that Patent Owner's arguments are based upon its proposed claim construction for a "first mode of operation." As discussed above, we decline to adopt Patent Owner's proposed construction that interprets the "first mode of operation" to *require* that the "the non-volatile memory subsystem does not communicate with the volatile memory subsystem or the host system." Rather, the claim simply recites that "in a first mode of operation . . . data is communicated between the volatile memory subsystem and the host system." Patent Owner does not appear to dispute that in Best, data is communicated between the volatile memory subsystem and the host system. *See* PO Resp. 36 ("Best teaches that during normal operation, when no write-back trigger is detected, the host communicates with both the volatile memory and the non-volatile memories.").

Therefore, after considering the evidence and arguments of the complete record, and for the reasons set forth by Petitioner, we determine that Petitioner has shown, by a preponderance of the evidence, that Best teaches this limitation.

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c) *"and a non-volatile memory subsystem operable at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem,"*

Petitioner relies on the combination of Best and Mills to teach this limitation. Pet. 29–34. Specifically, Petitioner contends that Best's Flash memory teaches "a non-volatile memory subsystem." *Id.* at 30 (citing Ex. 1006 ¶¶ 13, 17; Ex. 1003 ¶ 155). Petitioner relies on Best's "Shadow Operation" embodiment, discussed above, to teach "a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem." *Id.* (citing Ex. 1006 ¶¶ 24–26; Ex. 1003 ¶ 156). According to Petitioner, Best's "'*second mode of operation*' (i.e., the operation of the system when a power-loss write-back trigger is detected) involves '*a non-volatile memory subsystem operable*' (Best's 'NV' memory) such that '*data is communicated between the volatile memory subsystem and the non-volatile memory subsystem*,' e.g. when 'internal data transfer operations are performed to transfer data . . . from the DRAM to . . . the NV memory.'" *Id.* at 31 (citing Ex. 1006 ¶¶ 25–26; Ex. 1003 ¶¶ 156–158).

Petitioner contends that "Best does not explicitly disclose 'operating the non-volatile memory subsystem' (the Flash memory) 'at a second clock frequency' during this second mode, but it would have been obvious to include that functionality in the system of Best." *Pet.* 31 (citing Ex. 1003 ¶ 159). Petitioner, therefore, relies on a Flash implementation in Mills, which Petitioner asserts describes a synchronous flash interface that causes the Flash memory to "*opera[te] at a second clock frequency*." *Id.* at 31–32

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(citing Ex. 1009, 16:60–63, 17:10–25; Ex. 1003 ¶ 160) (alteration in original). According to Petitioner, "Mills teaches that this synchronous operation is used for both read operations and write operations." *Id.* at 32.

Petitioner asserts that Best and Mills are analogous art to the '833 patent. Pet. 32. Petitioner further asserts that the combination (i.e., employing a synchronous flash memory as described in Mills in the system of Best) would have been obvious to a person of ordinary skill in the art because it "would have been merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement, i.e. the non-volatile storage of data." *Id.* at 32–33 (citing Ex. 1003 ¶ 163). Petitioner contends that, as combined, Best's Flash memory would operate "at a second clock frequency." *Id.* at 33 (citing Ex. 1003 ¶ 164). Petitioner contends that one of ordinary skill in the art would have been motivated to make the combination because "restoring data from the non-volatile flash memory would therefore have been faster by use of a synchronous flash memory, and reduced sequential read access times during other operations or uses of Best's Flash memory." *Id.* at 33–34 (citing Ex. 1003 ¶ 165). Petitioner also asserts that a person of ordinary skill in the art would have understood Best to work with any known Flash interface, including Mills' synchronous Flash interface. *Id.* at 34 (citing Ex. 1003 ¶ 166).

Patent Owner argues that Best's "Shadow Operation" does not disclose "*a second mode of operation*." PO Resp. 38–40. Specifically, Patent Owner contends that "Best does not teach that the host system does not communicate with the volatile memory subsystem as part of the 'Shadow Operation' embodiment when a power-loss event write-back

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trigger is detected." *Id.* at 38; *see id.* at 40–41. According to Patent Owner, "Best teaches away from isolating the host system from the volatile memory subsystem when a power-loss event write-back trigger is detected by emphasizing that the volatile and non-volatile memories can be accessed simultaneously even during 'Shadow Operation.'" *Id.* at 38–39 (citing Ex. 1006 ¶¶ 18, 29; Ex. 2004 ¶ 91)).

We agree with Petitioner (Reply 17) that Patent Owner's arguments are based upon its proposed claim construction for a "second mode of operation." As discussed above, we decline to adopt Patent Owner's proposed construction that interprets the "second mode of operation" to require that the "the host system does not communicate with the volatile memory subsystem." Rather, the claim recites "a second mode of operation in which data is communicated between the volatile memory subsystem and the nonvolatile memory subsystem." We agree with Petitioner that Best teaches this limitation. *See, e.g.*, Ex. 1006 ¶ 25 ("Some time after one or more write operations have been performed, a write-back trigger is detected within the shared interface circuitry and, in response, one or more internal data transfer operations are performed *to transfer data* from the locations indicated by the write-back table to be dirty . . . *from the DRAM to corresponding locations (e.g., 205) within the NV memory*") (emphasis added).

Therefore, after considering the evidence and arguments of the complete record, and for the reasons set forth by Petitioner, we determine that Petitioner has shown, by a preponderance of the evidence, that the combination of Best and Mills teaches this limitation.

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d) "the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency."

(1) The Parties' Contentions

Petitioner relies on the combination of Best and Bonella to teach this limitation. Pet. 34–38. Petitioner asserts that Best does not explicitly disclose this limitation, but it would have been obvious for two reasons: "(1) reducing power during volatile to non-volatile flush operations prompted by a power loss was a well-known technique, and (2) one known way to reduce the power consumption of DRAM devices was to reduce their frequency of operation." *Id.* at 35 (citing Ex. 1003 ¶ 170). According to Petitioner, it would have been obvious to operate Best's DRAM "*at a third clock frequency*" that is "*less than the [first clock] frequency*" when performing Best's flush operation (i.e., "*when the memory system is in the second mode of operation.*"). *Id.*

Petitioner contends that the first reason and its advantages were well known in the art, and cites to Ashmore[11] and Long[12] in support of this assertion. Pet. 35–36 (citing Ex. 1010 ¶ 9; Ex. 1011, 4:54–64; Ex. 1003 ¶¶ 171–172). Petitioner contends that a person of ordinary skill in the art "would have been motivated to reduce the power consumption during Best's write flushing in response to a power loss" (1) for all the reasons that were known in the art, such as decreasing the risk of data loss due to insufficient backup power and enabling the use of a smaller-sized backup power source; and (2) because it would have been the arrangement of old elements, each

[11] US 2006/0212651 A1, published Sep. 21, 2006 (Ex. 1010).
[12] US 7,421,552 B2, issued Sep. 2, 2008 (Ex. 1011).

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performing the same function it had been known to perform, in a way that yields no more than what would be expected from such an arrangement, i.e., reducing power consumption during a power loss event, as suggested by Long and Ashmore. *Id.* at 36 (citing Ex. 1010 ¶ 7; Ex. 1011, 4:54–64; Ex. 1003 ¶ 173).

Petitioner relies on Bonella in support of the second reason, asserting that Bonella "explains that one way to reduce the power consumption of the memory module is to slow or reduce the operating frequency of the DRAM." Pet. 37 (citing Ex. 1008 ¶¶ 49–50; Ex. 1003 ¶ 174). Petitioner contends that Best and Bonella are analogous art to the '833 patent because both are from the field of memory systems. *Id.* Petitioner contends that a person of ordinary skill in the art "would also have found it obvious to reduce power consumption during Best's write flushing in response to a power loss using any known or conventional means, and would have also considered power consumption reduction techniques other than those of Ashmore and Long to obtain the same benefits, including those described in Bonella." *Id.* According to Petitioner, a person of ordinary skill in the art "would have found it obvious to perform Bonella's power reduction technique (DRAM operational frequency reduction) during the performance of Best's write flushing in response to a power loss, in view of the specific motivations evidenced by Ashmore and Long." *Id.* (citing Ex. 1003 ¶ 176). Petitioner also argues that Bonella itself provides motivation because "it results in 'major power savings.'" *Id.* (citing Ex. 1008 ¶ 50). Petitioner contends that "[u]sing Bonella's power reduction technique during Best's write flushing would also have been the arrangement of old elements, each performing the same function it had been known to perform, in a way that

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yields no more" than would be expected from such an arrangement. *Id.* at 37–38.

Patent Owner argues that a person of ordinary skill in the art would not have been motivated to combine Bonella with Best. PO Resp. 45. Specifically, Patent Owner argues that "[r]educing the DRAM frequency, as taught by Bonella, reduces DRAM performance" and "Best emphasizes the need to maintain high-speed, non-degraded DRAM performance, including during write-back operations." *Id.* at 49; *id.* at 45–46 (citing Ex. 2004 ¶ 109; Ex. 1006 ¶ 12); *see id.* at 46 (citing Ex. 1006 ¶ 18; Ex. 2004 ¶ 110). Patent Owner argues that "Best teaches away from reducing DRAM performance during write-back operation." *Id.* at 45 (citing Ex. 2004 ¶ 109).

Patent Owner argues that "Best neither teaches nor suggests . . . that the hybrid memory device behaves differently during a write-back operation depending on the write-back trigger." PO Resp. 47 (citing Ex. 2004 ¶ 112). Patent Owner argues that "all of Best's potential write-back triggers would occur during normal operation during which, Best teaches, the performance of the hybrid memory device should not be degraded." *Id.* (citing Ex. 2004 ¶ 112). Patent Owner also argues that "Best teaches away from reducing the DRAM's clock frequency, and thus its performance, during write-back operations, because the host may access the DRAM during such operations." *Id.* at 48 (citing Ex. 2004 ¶ 113).

Patent Owner argues that "Best's write-back operations triggered by a power-loss event are the same as write-back operations initiated by other triggers." PO Resp. 49 (citing Ex. 1006 ¶ 26; Ex. 2004 ¶ 117). Therefore, according to Patent Owner, the "same teaching away applies to write-back operations that are triggered by a power-loss event." *Id.* at 48 (citing

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Ex. 2004 ¶ 114). Patent Owner contends that "Best's power-loss trigger indicates that power will be unavailable soon, not that power is already unavailable." *Id.* (citing Ex. 1006 ¶ 26). Patent Owner argues that "other operations within the host system would need to be performed prior to the loss of power . . . [and a person of ordinary skill in the art] would understand that these common shutdown tasks, which would be performed by the host system, should not be delayed by artificially reducing the frequency of—and, thus, the performance of—Best's DRAM." *Id.* (citing Ex. 2004 ¶ 114).

In Reply, Petitioner argues that Patent Owner "fails to show that Best ever discloses or teaches that the DRAM must maintain high-speed and high-performance communication with the host even after it has lost power or is powering down." Reply 19. Petitioner contends that Best does not support Patent Owner's assertions that write-back operations can be triggered by "a power-loss trigger [that] indicates that power will be unavailable soon, not that power is already unavailable." *Id.* (alteration in original). Rather, Petitioner contends that Best "discloses that the trigger that initiates the write-back flush operations is the actual detection of 'a power-loss or power-down signal or event,' . . . not the near-future unavailability of power, as [Patent Owner] suggests." *Id.* at 20. Petitioner further argues that "[t]here is no disclosure or teaching [in Best] that the DRAM must maintain, or is even capable of maintaining, high-speed and high-performance read/write communications with the host during a power-loss event when 'dirty data' is being written to Flash." *Id.*

In Sur-reply, Patent Owner cites to paragraph 26 of Best, and argues that a person of ordinary skill in the art "would understand that Best teaches performing write-backs as part of a power down procedure, prior to the

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removal of power to the system." Sur-reply 22 (emphasis omitted). According to Patent Owner, a person of ordinary skill in the art "would understand that the ability to perform any module operation after the removal or failure of system power would require an alternate power source such as a battery or capacitor," and Best "does not disclose a secondary power source." *Id.* Patent Owner repeats its contention that "Best does not teach that his device performs differently depending on the write-back trigger source." *Id.* at 23.

(2) Analysis

On this record, we are persuaded that Petitioner has provided an articulated reasoning with rational underpinning for the combination of Best and Bonella. *See KSR*, 550 U.S. at 418. We are not persuaded that Best's description of "relatively high-speed, non-degrading memory accesses" teaches away from the proposed combination with Bonella. *See* Ex. 1006 ¶ 24; *see also id.* ¶ 12 ("in one application of the hybrid memory device, a DRAM memory is provided for relatively high-speed memory access and degradation-free performance"); *id.* ¶ 18 ("accesses may be overlapped at least in part to enable multiple accesses to the DRAM to be carried out while awaiting a memory read or programming operation (memory write) within the slower non-volatile die"). In an exemplary description of the memory shadowing operation, Best states that "Initially . . . data is stored in a fast-access volatile storage die." *Id.* ¶ 25. Best goes on to describe that "some time after one or more write operations have been performed, a write-back trigger is detected within the shared interface circuitry and, in response, one or more internal data transfer operations are performed to transfer data from the locations indicated by the write-back

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table to be dirty . . . from the DRAM to the corresponding locations . . . within the NV memory." *Id.* Best states that the write-back trigger may be "detecting a power-loss or power-down signal or event (i.e., performing all necessary write-backs–an operation referred to herein as flushing the write-back table–as part of power down)." *Id.* ¶ 26. According to Patent Owner, Best teaches away from reducing DRAM performance (i.e., by reducing DRAM frequency) during this "power-loss trigger [that] indicates that power will be unavailable soon, not that power is already unavailable." *See* PO Resp. 49.

We are not persuaded that the foregoing description of a "power-loss" or "power-down signal" or event exclusively refers to an indication that "power will be unavailable soon," (PO Resp. 49) as opposed to the actual detection of a power-loss. *See* Reply 19–20. Even taking into account Best's description of "relatively high-speed, non-degrading memory accesses," we are not persuaded that this teaches away from the combination of Best and Bonella. As the Federal Circuit has explained, "[a] reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." *Galderma Labs. LP v. Tolmar Inc.*, 737 F.3d 731, 738 (Fed. Cir. 2013). It is not sufficient for "teaching away" if the reference "merely expresses a general preference for an alternative invention but does not criticize, discredit, or otherwise discourage investigation into the invention claimed." *Id.* We agree with Petitioner that there is "no disclosure or teaching [in Best] that the DRAM must maintain, or is even capable of maintaining, high-speed and high-performance read/write communications

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with the host during a power-loss event when 'dirty data' is being written to Flash." *See* Reply 20. We are persuaded that a person of ordinary skill in the art would be motivated to use Bonella's power reduction technique (DRAM operational frequency reduction) during the performance of Best's write flushing for the reasons set forth by Petitioner.

After considering the evidence and arguments of the complete record, and for the reasons set forth by Petitioner, we determine that Petitioner has shown, by a preponderance of the evidence, that the combination of Best and Bonella teaches this limitation and Petitioner has provided a sufficient reason for combining the references.

e) Conclusion for Independent Claims 1 and 15

Based on our review and consideration, we determine that Petitioner has demonstrated that the combination of Best, Bonella, and Mills teaches the limitations in claims 1 and 15, and provided sufficient reasoning for combining the references. We determine that the information presented in the Petition demonstrates, by a preponderance of the evidence, that claims 1 and 15 are unpatentable under 35 U.S.C. § 103(a) over Best, Bonella, and Mills.

5. Dependent Claim 16

Claim 16 depends from claim 15 and recites "a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation." Ex. 1001, 22:12–17.

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Petitioner contends that Best discloses a "*controller*" in the form of a shared interface circuit. Pet. 39 (citing Ex. 1006 ¶ 12; Ex. 1003 ¶ 181); *see also id.* (citing Ex. 1006 ¶¶ 17, 21, Figs. 2–3).

Petitioner contends that Best's shared interface circuitry is "*configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation*" because when no write-back trigger is detected (i.e., the *first mode of operation*), the Flash memory is decoupled from the DRAM. Pet. 39–40 (Ex. 1006 ¶¶ 17, 21, 25–26; Ex. 1003 ¶¶ 182–183). In particular, Petitioner contends that "access to only one of the DRAM or Flash memory is enabled, and when access to one is enabled access to the other is not enabled." *Id.* at 40 (citing Ex. 1006 ¶¶ 17, 21, 22, 25; Ex. 1003 ¶ 183). In particular, Petitioner identifies that the data control circuit 151 may switch multiplexer 153 to convey data from the shared internal path 140 to secondary data path 155 (volatile) or secondary data path 157 (non-volatile). *Id.* at 40 (citing Ex. 1006 ¶ 21); *see* Ex. 1006, Figs. 2, 3.

Petitioner further contends that Best's shared interface circuitry is configured "*to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation*" because Best discloses that during a power-loss event write-back trigger event (i.e., a second mode of operation), "the Flash memory is coupled to the DRAM so that 'the data read out of the volatile storage die may be transferred from the volatile-die interface buffer 159 to the non-volatile-die interface buffer 161 via the inter-die data path 171.'" Pet. 41 (citing Ex. 1006 ¶ 21); *see* Ex. 1006, Fig. 3. Petitioner contends that "Best therefore discloses that at least the following elements of the shared interface circuitry couple the Flash memory to the

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DRAM: volatile-die interface buffer 159, non-volatile-die interface buffer 161, and inter-die data path 171." Pet. 41–42 (citing Ex. 1006 ¶ 21; Ex. 1003 ¶ 187).

Patent Owner argues that Petitioner has not shown that Best's shared interface circuitry is "*configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation*" because Petitioner relies on data paths between the host system and the Flash or DRAM, which do not "ha[ve] anything to do with decoupling Best's volatile memory from the non-volatile memory (or coupling, for that matter)." PO Resp. 43. Patent Owner cites to testimony from Mr. Maltiel that it asserts supports the conclusion that Petitioner's position has nothing to do with coupling or decoupling the non-volatile and volatile memories from each other. *Id.* at 44 (citing Ex. 2005, 174:8–12; 144:13–17; Ex. 2004 ¶¶ 104, 105).

In Reply, Petitioner contends that showing that the non-volatile and volatile memories are coupled in a second mode of operation via inter-die data path 171 renders obvious that they are decoupled during the first mode of operation. Reply 18–19 (citing Ex. 1003 ¶¶ 185, 188).

In Sur-reply, Patent Owner argues that Petitioner did not argue that inter-die data path 171 is disabled while data paths 155 and 157 are enabled, as Petitioner contends in the Reply, so this new argument should be rejected as untimely. Sur-reply 21. Patent Owner argues that "Best teaches that data may flow via inter-die data path 171 from non-volatile memory to volatile memory, and vice versa," but "Best does not disclose that inter-die data path is ever disabled." *Id.* (citing Ex. 1006 ¶ 21).

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We disagree that Petitioner's evidence does not support that Best's shared interface circuitry is "*configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation*." Figure 3 of Best is reproduced below.

FIG. 3

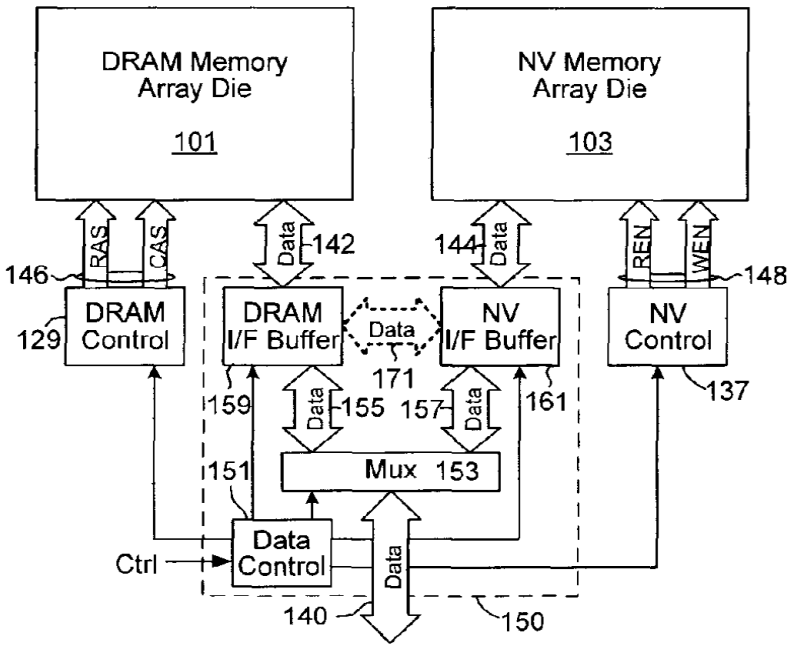

Figure 3, depicted above, illustrates an embodiment of a data control/steering circuit 150 that includes control circuit 151, multiplexer 153, secondary volatile and non-volatile data paths 155 and 157, volatile-storage-die interface buffer 159, non-volatile-storage-die interface buffer 161, and inter-die data path 171. *Id.* ¶ 21.

Best describes that:

> In a memory write operation, *data received via shared internal data path 140 is passed, via multiplexer 153, to one of the secondary data paths 155, 157 according to the memory access target* (e.g., indicated by memory-select signal MSel as described in reference to FIG. 4). If the volatile storage die 103

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> is the target of the memory write, the data control circuit 151 *switches the multiplexer 153* to convey data from the shared internal path 140 to secondary data path 155, and signals the DRAM interface buffer 159 to enable the data to be buffered (or queued) therein for eventual transfer to the DRAM die via data path 142.

Id. (emphasis added). We agree with Petitioner that this disclosure, describing use of a multiplexer 153 to convey data to one of paths 155 or 157 depending on the memory access target (i.e., volatile storage die or non-volatile storage die), teaches "*decoupl[ing] the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation.*" That is, "during Best's first mode of operation, the non-volatile and volatile memory subsystems are ***decoupled*** because the only memory paths that are enabled originate from the host to either volatile or non-volatile memory." *See* Reply 18; *see* Pet. 40–41. Patent Owner's argument that Petitioner's cited evidence "has nothing to do with coupling or decoupling the non-volatile and volatile memories from each other" (Sur-reply 21) is not persuasive, given Best's disclosure above.

We also disagree that Petitioner's evidence does not support that Best teaches that its shared interface circuitry is configured "*to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation.*" This is supported by Best's disclosure of an alternative embodiment during the memory shadow operation, where data may be transferred from the volatile-die interface buffer 159 to the non-volatile-die interface buffer 161 and vice versa *via the inter-die data path 171*, depicted

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above in Figure 3.[13] Ex. 1006 ¶ 21. We agree with Petitioner that "Best's disclosure of ***coupling*** the non-volatile and volatile memory subsystems during the second mode of operation renders obvious that the memory systems are ***decoupled*** during the first mode of operation." *See* Reply 18–19; *see also* Pet. 41–42. For example, there does not appear to be, and Patent Owner does not identify, any path by which the volatile and non-volatile memories are coupled in Figure 3, aside from inter-die data path 171, which is described in context of the memory shadowing operation described above.

Accordingly, we determine that the information presented in the Petition demonstrates, by a preponderance of the evidence, that claim 16 is unpatentable under 35 U.S.C. § 103(a) over Best, Bonella, and Mills.

6. Dependent Claims 3–14, 17, and 19–30

Petitioner contends that dependent claims 3–14, 17, and 19–30, which depend directly or indirectly from independent claims 1 and 15, would have been obvious over Best, Bonella, and Mills, and provides explanation as to how the prior art teaches each claim limitation. Pet. 38–60.

For example, claim 17 depends from claim 15 and recites "a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation." Ex. 1001, 22:18–22. Petitioner contends that these features were "well-known in the art" and are disclosed by Bonella's standard and backup power

[13] Petitioner explicitly referred to inter-die data path 171 twice on page 40 of the Petition, so Patent Owner's contention that Petitioner did not identify inter-die data path 171 in the Petition is not persuasive.

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sources. Pet. 42–43 (citing Ex. 1008 ¶¶ 29–31, 33, 101; Ex. 1003 ¶ 192). Petitioner contends that it would have been obvious to a person of ordinary skill in the art "to include Bonella's power supplies and associated selective power switching functionality/circuitry, including the power transistors, in Best's hybrid memory devices because to do so would have been merely an arrangement of old elements . . . each performing the same function it had been known to perform . . . in a way that yields no more than a [person of ordinary skill in the art] would expect from such an arrangement." *Id*. at 43–44 (citing Ex. 1006 ¶¶ 25, 26; Ex. 1008 ¶¶ 29–31, 33, 101; Ex. 1003 ¶ 194).

Claims 3 and 19 depend from claims 1 and 15, respectively, and recite "wherein the memory system is not powered by a battery when it is in the second mode of operation." Ex. 1001, 21:25–27, 22:25–27. Petitioner contends that Bonella discloses that a power loss event is powered by either a battery or capacitors, so "when Bonella's capacitors power the memory module for emergency shutdown operations . . . the memory module 'is not powered by a battery.'" Pet. 44–45 (citing Ex. 1008 ¶ 29; Ex. 1003 ¶ 198). According to Petitioner, "as combined, Best's system would use Bonella's power techniques/capacitors to power Best's hybrid memory device system when Best's hybrid memory device system is also operating in a state similar to Bonella's 'emergency shutdown operations,' such as Best's operation in response to 'power-loss'/'power-down' events." *Id.* at 45–46 (citing Ex. 1006 ¶¶ 25–26; Ex. 1008 ¶¶ 29–31, 33, 101; Ex. 1003 ¶ 199).

Claims 4 and 20 depend from claims 1 and 15, respectively, and recite "wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition." Ex. 1001, 21:28–30, 22:28–30. Petitioner relies on Best to teach this limitation,

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specifically, Best's detection of the power-loss event write-back trigger. Pet. 46–47 (citing Ex. 1006 ¶¶ 25–26; Ex. 1003 ¶ 202).

Claims 5 and 21 depend from claims 4 and 20, respectively, and recite "wherein the trigger condition comprises a power failure condition." Ex. 1001, 21:31–32, 22:32–33. Petitioner relies on Best's write-back trigger detecting a power-loss or power-down signal or event to teach this limitation. Pet. 47 (citing Ex. 1006 ¶ 26).

Claims 6 and 22 depend from claims 1 and 15, respectively, and recite "wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board." Ex. 1001, 21:33–36, 22:33–36. Petitioner relies on Figure 1A of Best, and Best's disclosure that "the DRAM and Flash are typically implemented in separate integrated circuit devices having distinct control and data interfaces and disposed in distinct regions of an integrated circuit board." Pet. 47–48 (citing Ex. 1006 ¶¶ 2, 13, Fig. 1A).

Claims 7 and 23 depend from claims 1 and 15, respectively, and recite "wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation." Ex. 1001, 21:37–40, 22:37–40. Petitioner relies on Mills to teach this limitation, specifically Mills' saving of intermediate results generated during the course of execution of the program. Pet. 49 (citing Ex. 1009, 3:21–26; Ex. 1003 ¶ 207). Petitioner contends that, "as combined, Best's system would operate as usual such that when 'a write-back trigger is detected,' such as a power-loss event, shadowing operations are performed, e.g., 'internal data transfer operations are performed to

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transfer data . . . from the DRAM to . . . the NV memory,' where the data being transferred in Best's system includes the 'intermediate results' disclosed by Mills." *Id.* at 50 (alterations in original). According to Petitioner a person of ordinary skill in the art would be motivated to make such a combination "to prevent the loss of all data forever, especially because prevention of data loss is a goal of both Best and Mills." *Id.* at 51 (citing Ex. 1006 ¶¶ 25–26; Ex. 1009, 3:21–26; Ex. 1003 ¶ 212).

Claims 8 and 24 depend from claims 1 and 15, respectively, and recite "wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation." Ex. 1001, 21:41–44, 22:41–44. Petitioner relies on Best's memory shadowing operations to teach this limitation. Pet. 52 (citing Ex. 1006 ¶¶ 24–25; Ex. 1003 ¶¶ 215, 216, 218, 219).

Claims 9 and 25 depend from claims 8 and 24 and recite "wherein the backup operation is conducted at repeating time intervals." Ex. 1001, 21:44–45, 22:45–46. Petitioner relies on Best to disclose this limitation, for example, that Best teaches "[t]he write-back trigger itself may include . . . periodically performing write-back." Pet. 52–53 (citing Ex. 1006 ¶¶ 25, 26; Ex. 1003 ¶ 220) (alteration in original).

Claims 10 and 26 depend from claims 9 and 25, respectively, and recite "wherein the backup operation is initiated in response to a trigger event." Ex. 1001, 21:46–47, 22:47–48. Petitioner relies on Best to teach this limitation, for example, that Best's "write-back operations" occur "in response" to when a "write-back trigger" is detected. Pet. 53 (citing Ex. 1006 ¶¶ 25–26; Ex. 1003 ¶ 221).

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Claims 11 and 27 depend from claims 1 and 15, respectively, and recite "wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem." Ex. 1001, 21:48–51, 22:50–53. Petitioner relies on Best's memory shadow operation to teach this limitation. Pet. 54 (citing Ex. 1006 ¶¶ 25, 26; Ex. 1003 ¶ 223).

Claims 12 and 28 depend from claims 1 and 15, respectively, and recite "wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem." Ex. 1001, 21:52–55, 22:54–57. Petitioner relies on Best to teach this limitation, for example, that Best discloses that communication between the volatile memory and non-volatile memory includes the performance of restore operations in which data is "transferred . . . from the non-volatile die 101 to the volatile storage die 103 . . . to restore the state of the volatile storage die 103 to a pre-power-down or pre-sleep condition." Pet. 55 (citing Ex. 1006 ¶ 21; Ex. 1003 ¶ 226).

Claims 13 and 29 depend from claims 1 and 15, respectively, and recite "wherein the one or more of the first, second, or third clock frequencies is configurable by the memory system." Ex. 1001, 21:56–58, 22:58–60. Petitioner relies on Bonella to teach this limitation, for example, that Bonella teaches that the memory module has power management features that are "user configured and/or system configured" and that at least the primary operating frequency of the DRAM is configurable by the memory system based on the user configuration. Pet. 56 (citing Ex. 1008 ¶¶ 36, 45, 48–50; Ex. 1003 ¶¶ 230, 231). Petitioner contends that a person of ordinary skill in the art would have been motivated to modify Best to

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obtain the benefit of configurability and power savings. *Id.* at 57 (citing Ex. 1003 ¶ 234).

Claims 14 and 30 depend from claims 1 and 15, respectively, and recite "wherein one or more of the first, second or third clock frequencies is configurable by a user." Ex. 1001, 21:59–60, 22:60–62. Petitioner relies on Bonella to teach this limitation, for many of the same reasons set forth for claims 13 and 29. Pet. 58–60.

Patent Owner does not specifically respond to Petitioner's contentions, but instead relies on the arguments presented for claim 15. PO Resp. 45.

Based on our review and consideration of the record, we determine that Petitioner has demonstrated that the combination of Best, Bonella, and Mills teach the limitations in claims 3–14, 17, and 19–30 and provided sufficient reasoning for combining the references. We determine that the information presented in the Petition demonstrates, by a preponderance of the evidence, that claims 3–14, 17, and 19–30 are unpatentable under 35 U.S.C. § 103(a) over Best, Bonella, and Mills.

7. Summary

We find that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 3–17, and 19–30 are unpatentable under 35 U.S.C. § 103(a) over Best, Bonella, and Mills.

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IV. CONCLUSION

For the foregoing reasons, we are persuaded that Petitioner established by a preponderance of the evidence that claims 1, 3–17, and 19–30 of the '833 patent are unpatentable.[14]

In summary:

Claims	35 U.S.C. §	Reference(s)/Basis	Claims Shown Unpatentable	Claims Not shown Unpatentable
1, 3–17, 19–30	103(a)	Best, Bonella, Mills	1, 3–17, 19–30	

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1, 3–17, and 19–30 of the '833 patent have been shown to be unpatentable under 35 U.S.C. § 103(a); and

FURTHER ORDERED that, because this is a final written decision, parties to this proceeding seeking judicial review of our Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

[14] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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