UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner

Case PGR2026-00001
Case IPR2026-00018
Patent 12,373,366

DECLARATION OF DR. ANDREW WOLFE REGARDING U.S. PATENT NO. 12,373,366

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd. ("Samsung") as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 12,373,366 ("the '366 Patent") (EX1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. My professional qualifications, experience, publications and presentations, and a listing of previous cases in which I have provided expert testimony are set forth in my CV, attached as Exhibit 1004.

3. I am the founder and sole employee of Wolfe Consulting. Through Wolfe Consulting, I provide technical and business analytics to businesses on processor technology, computer systems, consumer electronics, software, design tools, data security, cryptography and intellectual property issues. I have more than thirty years' experience developing products, researching, consulting, and teaching in those fields. In that time, I have worked as a computer architect, computer system designer, and as an executive in the PC and electronics business. I have also taught at some of the world's leading institutions in those fields, including

Stanford University, Princeton University, Carnegie Mellon University, and Santa Clara University.

4. In 1985, I earned the B.S.E.E. degree in Electrical Engineering and Computer Science from the Johns Hopkins University. In 1987, I received the M.S. degree in Electrical and Computer Engineering from Carnegie Mellon University and in 1992, I received the Ph.D. degree in Computer Engineering from Carnegie Mellon University. My doctoral dissertation proposed a new approach for the architecture of a computer processor.

5. I have more than 35 years of experience as a computer architect, computer system designer, personal computer graphics designer, educator, and executive in the electronics industry.

6. In 1983, I began designing touch sensors, microprocessor-based computer systems, and I/O (input/output) cards for personal computers as a senior design engineer for Touch Technology, Inc. During the course of my design projects with Technology, I designed I/O cards for PC-compatible computer systems, including the IBM PC-AT, to interface with interactive touch-based computer terminals that I designed for use in public information systems. I continued designing and developing related technology as a consultant to the Carroll Touch division of AMP, Inc., where in 1986 I designed one of the first custom touch-screen integrated circuits. I designed the touch/pen input system for

the Linus WriteTop, which many believe to be the first commercial tablet computer.

7. From 1986 through 1987, I designed and built a high-performance computer system as a student at Carnegie Mellon University. From 1986 through early 1988, I also developed the curriculum, and supervised the teaching laboratory, for processor design courses.

8. In the latter part of 1989, I worked as a senior design engineer for ESL-TRW Advanced Technology Division. While at ESL-TRW, I designed and built a bus interface and memory controller for a workstation-based computer system and also worked on the design of a multiprocessor system.

9. At the end of 1989, I (along with some partners) reacquired the rights to the technology I had developed at Touch Technology and at AMP, and founded The Graphics Technology Company. Over the next seven years, as an officer and a consultant for The Graphics Technology Company, I managed the company's engineering development activities and personally developed dozens of touch screen sensors, controllers, and interactive touch-based computer systems.

10. I have consulted, formally and informally, for a number of fabless semiconductor companies. In particular, I have served on the technology advisory boards for two processor design companies: BOPS, Inc., where I chaired the board, and Siroyan Ltd., where I served in a similar role for three networking chip

companies – Intellon, Inc., Comsilica, Inc., and Entridia, Inc. – and one 3D game accelerator company, Ageria, Inc.

11. I have also served as a technology advisor to Motorola and to several venture capital funds in the U.S. and Europe. Currently, I am a director at Turtle Beach Corporation, providing guidance in its development of premium audio peripheral devices for a variety of commercial electronic products.

12. From 1991 through 1997, I served on the Faculty of Princeton University as an Assistant Professor of Electrical Engineering. At Princeton, I taught undergraduate and graduate-level courses in Computer Architecture, Advanced Computer Architecture, Display Technology, and Microprocessor Systems, and conducted sponsored research in the area of computer systems and related topics. From 1999 through 2002, I taught a Computer Architecture course to both undergraduate and graduate students at Stanford University multiple times as a Consulting Professor. At Princeton, I received several teaching awards, both from students and from the School of Engineering. I have also taught advanced microprocessor architecture to industry professionals in IEEE and ACM sponsored seminars. I am currently an Asst. Teaching Professor at Santa Clara University teaching courses on Microprocessor Systems, Advanced Logic Design, Real-Time Computing, and Mechatronics. I teach about memory, including DDR SDRAM

and flash memory, in several of my classes and rely on the JEDEC specifications as industry standards.

13. From 1997 through 2002, I held a variety of executive positions at a publicly held fabless semiconductor company originally called S3, Inc. and later called Sonicblue Inc. I held the positions of Chief Technology Officer, Vice President of System Integration Products, Senior Vice President of Business Development, and Director of Technology, among others.

14. In the roles listed above, I worked with and managed architecture and design teams responsible for the development of SRAM and DRAM memories, graphics chip memory controllers, and CPU memory controllers. I also worked with memory vendors and memory standards bodies, directly and through my staff, on the development of memory technology and standards. I have been involved with interpreting and understanding JEDEC memory standards since at least 1997. For many years, I had a direct-report staff member who would attend JEDEC meetings and bring me both proposed and final standards for review and comment. I also have used proposed and final JEDEC standards for chips, modules, and protocols to guide product decisions and to facilitate technical discussions with corporate partners and with consulting clients. I supervised design teams that implemented memory controllers for successful commercial products that interoperated with JEDEC-compliant DDR memory chips and memory modules.

15. My teams also developed the Rio MP3 players and a music delivery platform and webstore backend service for selling music. In 1999, this music delivery system was spun out as a separate company called RioPort.com. I served on the RioPort.com board of directors and became involved in their product and technology strategy. I also managed engineering and marketing for the Rio product line for a period of time as an interim general manager. The Rio MP3 players were among the first consumer products to incorporate large quantities of NAND flash memory. I worked with CEOs and General Managers at several leading flash memory suppliers on strategic planning for the flash market. I also worked with my engineering teams to evaluate and implement flash memory protocols and select flash memory form factors. During my time at SonicBlue we launched more than 30 new consumer electronics products.

16. I served as a board member and technical advisor as KBGear Inc. from 1999-2001. KBGear Inc. designed and produced digital cameras and music players.

17. I have published more than fifty peer-reviewed papers in computer architecture and computer systems and IC design. I have also chaired IEEE and ACM conferences in microarchitecture and integrated circuit design and served as an associate editor for IEEE and ACM journals. I served on the IEEE Computer Society Awards committee. I am an IEEE Fellow and a Member of ACM. I am a

named inventor on at least fifty-seven U.S. patents and thirty-seven foreign patents.

18. I have been the invited keynote speaker at the ACM/IEEE International Symposium on Microarchitecture and at the International Conference on Multimedia. I have also been an invited speaker on various aspects of technology or the PC industry at numerous industry events including the Intel Developer's Forum, Microsoft Windows Hardware Engineering Conference, Microprocessor Forum, Embedded Systems Conference, Comdex, and Consumer Electronics Show as well as at the Harvard Business School and the University Illinois Law School. I have been interviewed on subjects related to technology and the electronics industry by publications such as the Wall Street Journal, New York Times, LA Times, Time, Newsweek, Forbes, and Fortune as well as CNN, NPR, and the BBC. I have also spoken at dozens of universities including MIT, Stanford, University of Texas, Carnegie Mellon, UCLA, University of Michigan, Rice University, and Duke University.

C. Compensation and Prior Testimony

19. I am being compensated at a rate of $750.00 per hour for my study and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

20. My CV, attached as Exhibit 1004, lists all other cases in which, during the previous 4 years, I have testified as an expert at trial or by deposition.

D. Information Considered

21. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Exhibit List at the end of this declaration.

22. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

23. My analysis of the materials produced in this matter is ongoing and I will continue to review any new materials as it is provided. This declaration represents only those opinions I have formed to date.

II. LEGAL STANDARDS FOR PATENTABILITY

24. In expressing my opinions and considering the subject matter of the claims of the ’366 Patent, I am relying upon certain basic legal principles that have been explained to me.

A. 35 U.S.C. §§ 102 and 103

25. I understand that for an invention claimed in a patent to be found patentable under 35 U.S.C. §§ 102 and 103, it must be, among other things, new and not obvious from what was known before the invention was made.

26. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

27. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the '366 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

28. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

29. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below

compares the claims to patents and printed publications that are prior art to the claims.

30. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. In this declaration I focus on "obviousness." My understanding of the legal standard for "obviousness" is set forth below.

31. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

32. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the claims of the '366 Patent would have been considered obvious as of the priority date of the patent.

34. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

35. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

36. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being

associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors" suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

37. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

38. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a Skilled Artisan would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

39. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that does no more than yield predictable results, which are inferences and creative steps that a Skilled Artisan would employ.

40. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

41. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or

derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

42. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

43. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art

references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

44. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

45. I understand that a person of ordinary skill is also a person of ordinary creativity.

46. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was

obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

B. 35 U.S.C. § 112

47. I understand that under 35 U.S.C. § 112, the specification for the patent must (a) contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and (b) conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor(s) regard(s) as the invention.

48. I understand that a claim that lacks "written description" in the specification of the patent is invalid.

49. I understand that the written description inquiry looks to the four corners of the specification to discern the extent to which the inventor(s) had possession of the invention as broadly claimed. I understand that to the extent the specification purports to incorporate by reference, there must be a clear intent to

incorporate by reference that clearly identifies the referenced patent, application, or publication, and that "Essential material" (e.g., material necessary to provide written description) may only be incorporated by reference to a U.S. patent or U.S. patent application publication.

50. I understand that a specification that merely renders the invention ***obvious*** does ***not*** satisfy the written description requirement.

51. I understand that a patent that provides a "laundry list" disclosure does not provide adequate written description of every possible combination because such a disclosure would not reasonably lead those skilled in the art to any particular species. I understand that following a maze-like path, each step providing multiple alternative paths, is not a written description of what might have been described if each of the optional steps had been set forth as the only option.

52. I understand that hindsight (e.g., working backward from the knowledge of the claims) is not permitted to satisfy the written description requirement, and thus a patent lacks written description for a claim—even where the patent provides formal textual support for each individual limitation recited in the claims—if the patent nowhere describes the actual functioning invention that those limitations together define.

53. I understand that a patent owner cannot show written description support by picking and choosing claim elements from different embodiments that are never linked together in the specification. Thus, I understand that the written description requirement is not met when the specification provides at best disparate disclosures that an artisan might have been able to combine in order to make the claimed invention. I understand that one cannot disclose a forest in the original application, and then later pick a tree out of the forest and say here is my invention.

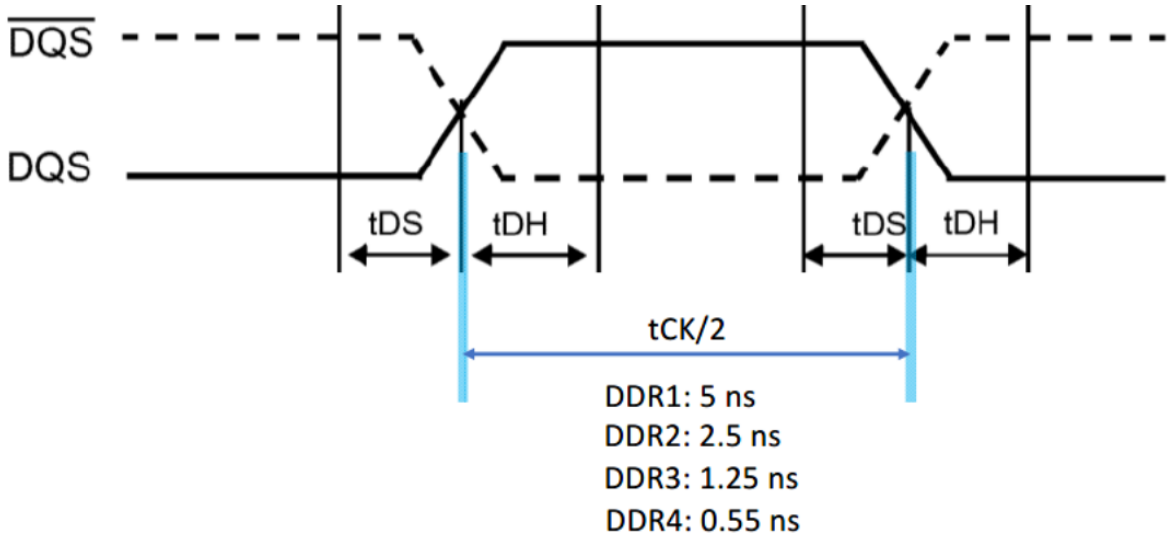
54. I understand that, for a negative claim limitation, silence is generally not disclosure. If it were, then every later-added negative limitation would be supported so long as the patent makes no mention of it. I understand that while a negative limitation need not be recited in the specification verbatim, there generally must be something in the specification that conveys to a skilled artisan that the inventor intended the exclusion, such as a discussion of disadvantages or alternatives. However, I understand that it is possible that the written description requirement may be satisfied when a skilled artisan would understand the specification as inherently disclosing a limitation. Thus, if a patent owner could establish that a particular limitation would always be understood by skilled artisans as being necessarily excluded from a particular claimed method or apparatus if that limitation is not mentioned, the written description requirement would be satisfied despite the specification's silence.

III. BACKGROUND ON THE '366 PATENT

A. Background Technology

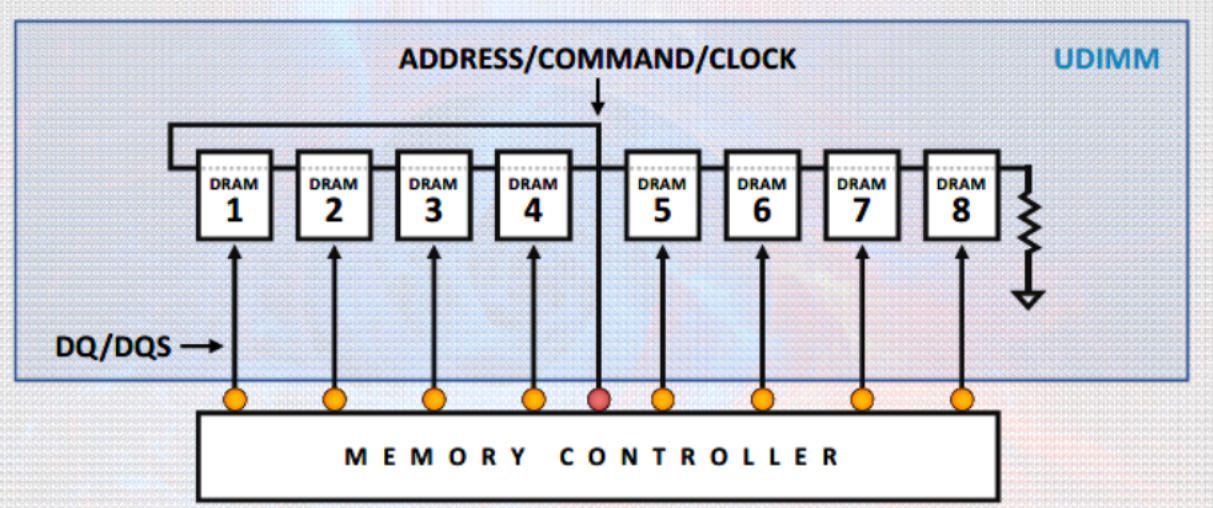
1. JEDEC Standards

55. A Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory devices and memory modules at the time. *See infra* ¶71. The Joint Electron Device Engineering Council (JEDEC) has played a central role in standardizing DRAM technologies, including the various generations of double data rate (DDR) DRAM devices and the different types of memory modules used in servers and workstations. EX1077, 3; EX1105, ¶¶4-5. JEDEC standards have defined the progression of DRAM technology from SDRAM through DDR, DDR2, DDR3, and beyond, with each generation essentially doubling the data transfer rate of its predecessor.



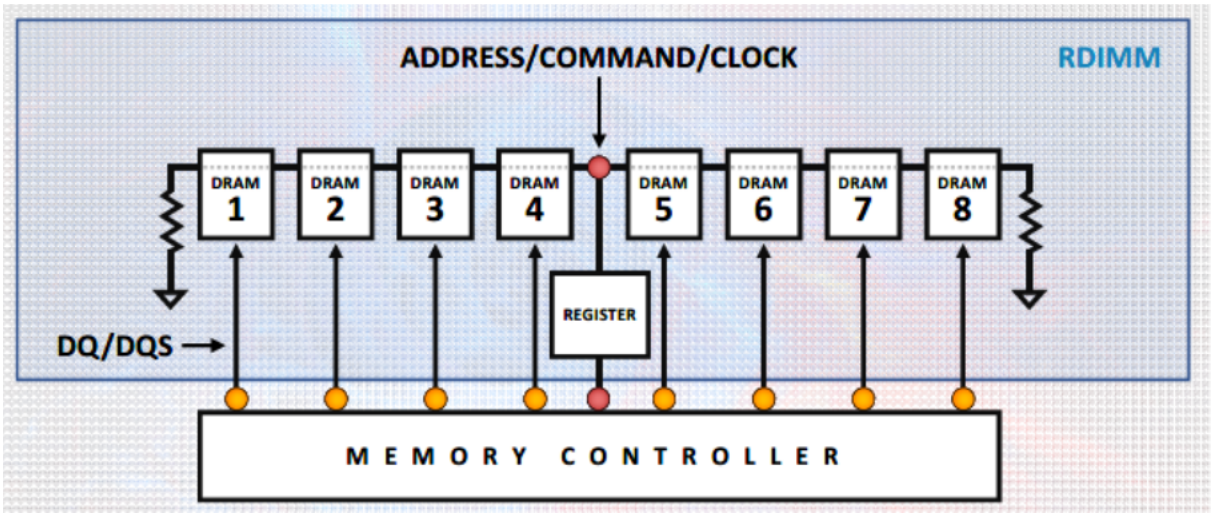
EX1077 at 6 (showing decrease in nominal clock cycle speed over consecutive DRAM generations); EX1045 at 58 (DDR1); EX1026 at 66 (DDR2); EX1046 at 144-48 (DDR3). For example, the Harris reference in Ground 2 discloses Double Data Rate (DDR) memory devices, including DDR2, DDR3 and DDR4 memories. *See* EX1023 at [0009], [0011]. A Skilled Artisan would have understood that at the time of the '336 priority date these memories were either already standardized, such as DDR, DDR2 and DDR3, or were in the process of being standardized by JEDEC, such as DDR4. *See, e.g., infra* at ¶¶59-61; EX1077 at 3-6. Harris also discloses Dual In-Line Memory Modules (DIMMs), including unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), and fully-buffered DIMMs (FBDs or FBDIMMs), illustrated below. *See* EX1023 at [0009]. A Skilled Artisan would have understood that some of these memory modules and their components were also standardized by JEDEC, including the Advanced Memory Buffers (AMB) for FBDIMMs as discussed below, *infra* ¶¶62-65; EX1077 at 2, 7-11.

56. UDIMMs—as pictured below—connect DRAM devices directly to the memory controller (at the bottom).



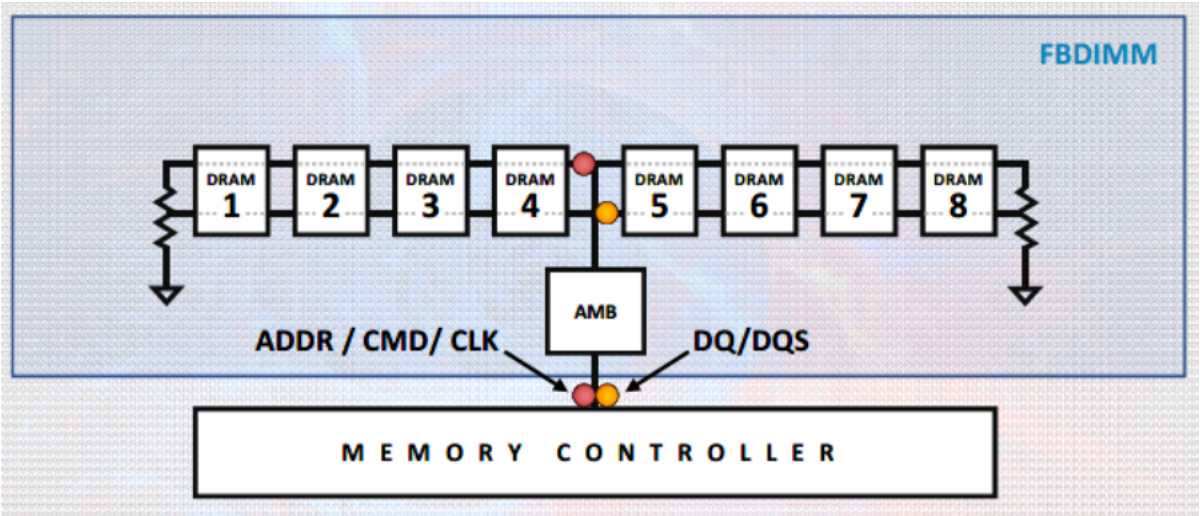
EX1077 at 7. This gives low latency but means the memory controller must drive the full electrical load of all DRAM chips, limiting the number of modules per channel at high speeds.

57. RDIMMs (as below) insert a *register* between the DRAM chips and the memory controller for address and control lines (red).



EX1077 at 8. This register buffers these signals, reducing the electrical load on the memory controller and allowing more DIMMs per channel.

58. FBDIMMs (below) go further by replacing the parallel DQ/DQS data lines to the memory module with a high-speed link through an Advanced Memory Buffer (AMB) on each module.



EX1077 at 9. The AMB handles address/control and also re-drives and buffers data signals, completely isolating DRAM loading from the memory controller. This enables very large memory capacities.

a) DDR SDRAM Specification (JESD79) (EX1045)

59. I understand that JEDEC published the standard DDR SDRAM Specification in June 2000 ("JESD79"). EX1045 at Cover. JESD79 specifies multiple voltages for operating DDR SDRAM devices, including supply voltage VDD, I/O supply voltage VDDQ, reference voltage VREF, and I/O termination voltage VTT, as shown in the table below.

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6
I/O Termination Voltage (system)	VTT	VREF–0.04	VREF+0.04	V	7

Id. at p.54 (excerpt of "Electrical Characteristics and DC Operation Conditions"). In particular, the nominal supply voltage VDD is 2.5 volts or 3.3 volts (both are supported). The nominal input/output (I/O) supply voltage VDDQ is 2.5 volts, which is the average of the minimum voltage at 2.3 volts and maximum voltage at 2.7 volts. The nominal I/O reference voltage VREF is half of VDDQ or 1.25 volts, as is the nominal I/O termination voltage VTT. *Id.*

b) DDR2 SDRAM Specification (JESD79-2B) (EX1026)

60. I understand that JEDEC published the standard DDR2 SDRAM Specification in January 2005 ("JESD79-2B"). EX1026 at Cover-1. JESD79-2B specifies multiple voltages for operating DDR2 SDRAM devices, including supply voltage VDD, supply voltage VDDL for DLL, supply voltage VDDQ for output, input reference voltage VREF, and termination voltage VTT, as shown in the table below.

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	2. 3
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	4

NOTE 1 There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.
NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
NOTE 4 VTT of transmitting device must track VREF of receiving device.
NOTE 5 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

EX1026 at p.49 (Table 16). In particular, there are five supply voltages specified at two different voltage amplitudes. VDD is a supply voltage typically at 1.8 volts, VDDL is a supply voltage for a delay-locked loop (DLL) typically at 1.8 volts, VDDQ is a supply voltage for output typically at 1.8 volts, VREF is an input reference voltage typically at one-half of VDDQ or 0.9 volts, and VTT is a termination voltage that is typically at VREF, or one-half of VDDQ (i.e., 0.9 volts). As I noted above, Harris explicitly references standard DDR2 memory technology. *Supra* ¶55.

c) DDR3 SDRAM Specification (JESD79-3A) (EX1046)

61. I understand that JEDEC published revision A of the standard DDR3 SDRAM Specification in September 2007 ("JESD79-3A"). EX1046 at Cover. JESD79-3A specifies multiple supply voltages for operating DDR3 SDRAM devices, including power supply voltages V_{DDQ} and V_{DD} of 1.5V, and reference voltages VREFDQ and VREFCA, as shown in the table below. *Id.* at p.10. DDR3

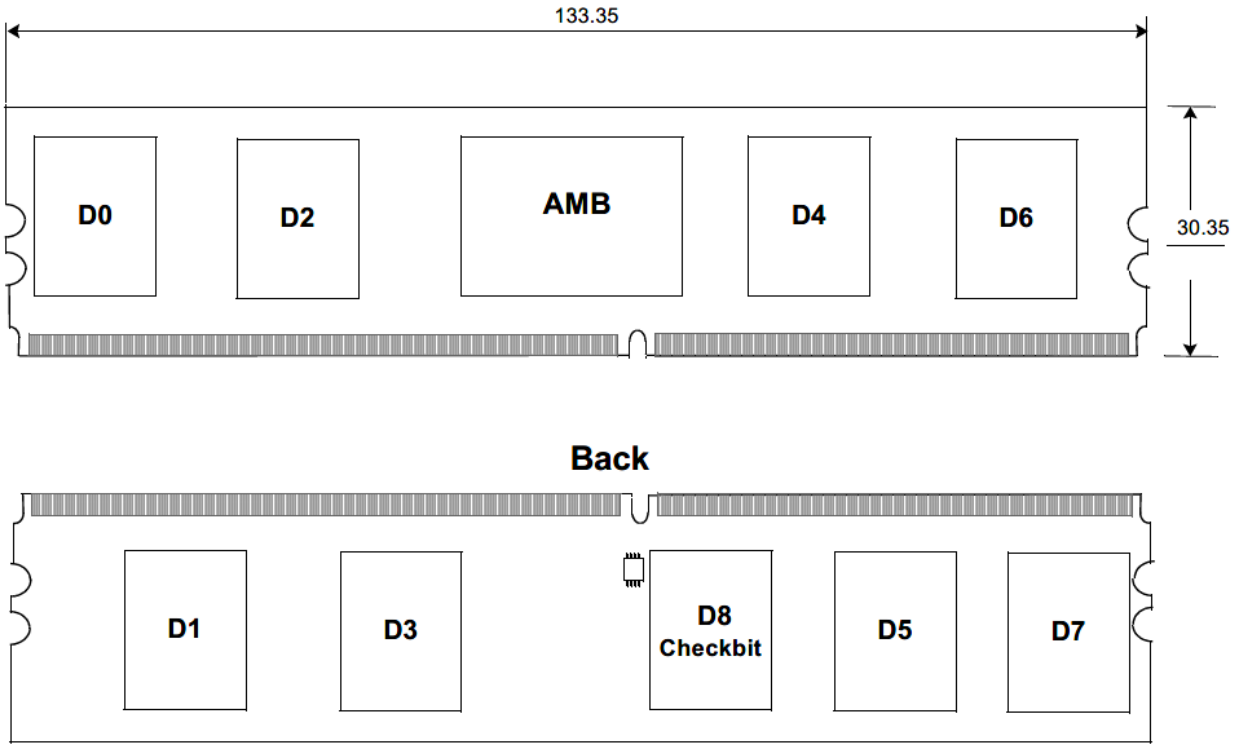
operation also requires a termination voltage VTT. *Id*. at p. 15 ("Power-up initialization … Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.")

V_{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage

d) DIMM Standards (EX1027, EX1028)

62. As mentioned above, Harris expressly states that its memory module can be implemented as a DIMM, such as un-buffered DIMM (UDIMM), registered DIMM (RDIMM), or a fully-buffered DIMM (FBD or FB-DIMM). *Supra* ¶¶55-58. A Skilled Artisan would have understood that some of these DIMMs were standardized. For example, JEDEC standardized registered DIMMs with DDR SDRAM and DDR2 SDRAM devices. *See*, *e.g.*, EX1104 (DDR SDRAM RDIMM); EX1106 (DDR2 SDRAM RDIMM).

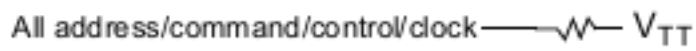
63. JEDEC also standardized fully-buffered DIMMs with DDR2 SDRAM devices. *See, e.g.*, EX1027 (JESD82-20); EX1028 (JESD205). A Skilled Artisan would have understood that an FBDIMM includes an advanced memory buffer (AMB) which interfaces with the DDR2 SDRAM devices on the module. EX1027 (FBDIMM Advanced Memory Buffer); EX1028 at 37 (example DDR2 SDRAM FBDIMM below); *see also id.* at 9, 13-16, 38-40.



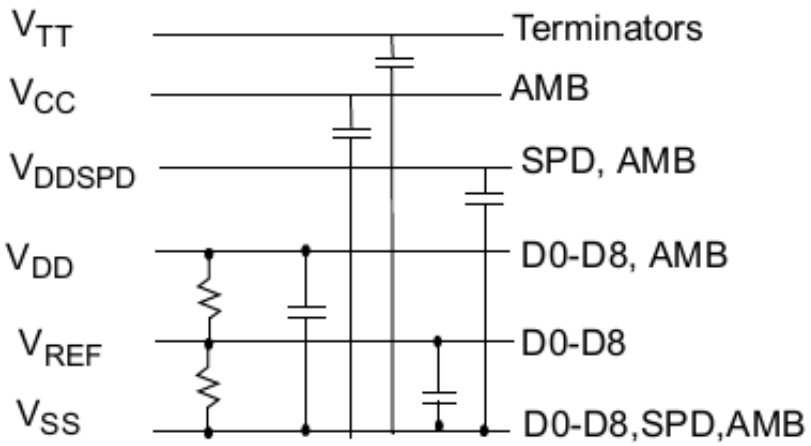
64. The FBDIMM receives supply voltages for the DRAM devices (V_{DD}/V_{DDQ}), the AMB (V_{CC}/V_{CCFBD}), the DRAM interface (V_{TT}), and an SPD device (V_{DDSPD}). EX1028 at p.9 (below), 105 ("The Serial Presence Detect (SPD) function MUST be implemented on the …DDR2 SDRAM FB-DIMM").

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})

All address/command/control/clock signal lines of the DRAM interface are terminated at V_{TT} on the FBDIMM. *Id.* at 9 (above), 13 (below, in part).



The AMB uses the V_{CC} voltage for its core, and it also uses the V_{DD} and V_{DDSPD} voltages to communicate with the memory devices and the SPD device, respectively. *Id*. at 13 (below, in part, illustrating supply voltage V_{DD} coupled to memory devices (D0-D8); supply voltage V_{DDSPD} coupled to the SPD; supply voltages V_{CC}, V_{DDSPD} and V_{DD} coupled to AMB; and termination voltage V_{TT} coupled to Terminators).



65. When the host system provides operating voltages as discussed above, DRAM devices on the DIMM perform normal read/write operations in response to address/command signals received from the host system. *See* EX1077, 7-9 (DRAMs on various types of DIMMs communicating "DQ/DQS" signals with the memory controller in response to "ADDRESS/COMMAND/CLOCK" signals). To increase bandwidth for the normal read/write operations, some DIMMs provide

a rank operation, where a group of DRAM devices, typically called a "rank," are enabled together by the same chip select signal ("CS") from the host system to concurrently communicate data signals. *See, e.g.*, EX1077 at 5; EX1026 at 6 ("Chip Select…provides for external Rank selection"); EX1106, 9 ("CS"). For example, in the case of standard DDR2 RDIMMs, one rank includes nine DRAM devices (eight for main data and one for ECC error correction), each having a x8 data width, and those DRAM devices are enabled together to concurrently communicate 72 bits (9x8) of data and ECC signals for normal read/write operations. *See, e.g.*, EX1106, 4 ("DIMM organization" is "x72 ECC"), 6 ("S[3:0]" for "Chip Selects"), 7 (similar), 9 ("x72 DIMM, populated as one physical rank of x8 DDR2 SDRAMs," showing nine x8 DRAM devices (D0-8) are enabled by the same chip select signal (RS0) to concurrently communicate 64-bit data (DQ0-63) and 8-bit ECC (CB0-7) signals for rank operations).

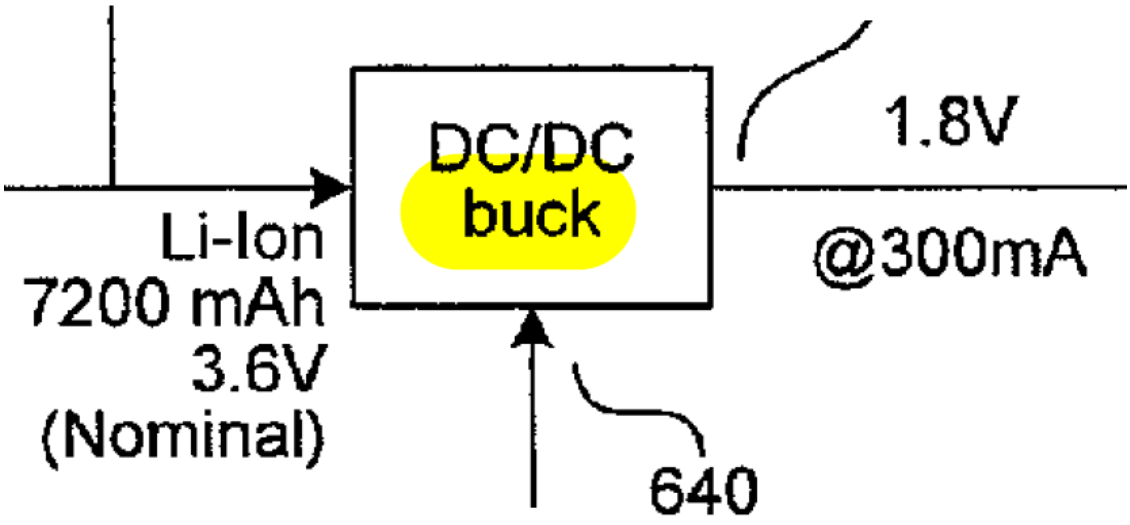
2. Buck Converters (EX1032, EX1058)

66. At the time of the '366 Patent, buck converters were well-known switching power supplies used to step down a higher input voltage to a lower output voltage. In fact, buck converters were one of "the most basic building blocks in power electronics." EX1050 at 1:21-23. A textbook entitled Simplified Design of Switching Power Supplies by John D. Lenk ("Lenk") from the mid-90s explained that a "buck circuit is used when the input voltage is always greater than

the desired output voltage (and is also known as a *step-down* converter)." EX1058 at 3 (describing Fig. 1-3), 5 (Fig. 1-3). In particular, the duty cycle of the switching converter determines the output voltage relative to the input voltage. *Id.* at 5 ("1.3 Switching-Regulatory Theory") ("The output voltage V_O is always equal to the input voltage V_{IN}, times the duty cycle D, or $V_O = DV_{IN}$."). Lenk also shows that the configurations and waveforms for a theoretical buck converter were well-known to a Skilled Artisan. *See id.* at 12-15 ("1.5.4. Buck or Step-Down").

67. Another textbook entitled Power Electronics: Converters, Applications, and Design by Ned Mohan et al. ("Mohan") also from the mid-90s explains that a step-down or buck converter is one of the "basic converter topologies." EX1032 at 161. Mohan also explains that, "[a]s the name implies, a step-down converter produces a lower average output voltage than the dc input voltage V_d." *Id.* at 164. Similar to Lenk, Mohan explains that the output voltage can be controlled "[b]y varying the duty ratio" of the switching cycle. *Id.*

68. As a further example, the Amidi reference in Ground 2 discloses using a buck converter on a memory module to convert a higher input voltage to a lower output voltage. *See, e.g.*, EX1024 at Fig. 6 (showing a DC/DC buck converter 640 to step down a higher voltage to a lower one, reproduced below in part, annotated).



69. In fact, buck converters providing V_{DDQ} and V_{TT} voltages specifically to operate DDR and DDR2 memory devices were commercially available at the time. EX1040 at p.1 (TPS51020 step-down controller for "DDR I or DDR II" devices "provides a one chip solution for all switching applications"); EX1041 at p.1 (FAN5026 PWM controller for "DDR V_{DDQ} and V_{TT} voltage generation" which "Supports DDR-II").

70. A Skilled Artisan would have understood at the time that using a "buck converter" was (and still is) a very efficient way to provide a step-down regulated voltage compared to a non-switching, linear regulator, such as a low-dropout regulator (LDO). *See, e.g.*, EX1058 (Lenk) at p.5 ("The high efficiency of switching regulators is the result of operating the series transistor in a switching mode."); EX1059 (Mayega) at 5:23-30 ("Switch mode buck converters have become popular due to two attractive features: first, they are more efficient than

traditional low drop out regulators (LDO) (e.g., up to 95%) and second, they can provide relatively high currents with lower power dissipation on chip than an LDO can."); EX1075 at 112:12-114:8 (LDOs may have an efficiency of only 10%). A buck converter would be the obvious choice for a high-speed circuit like a DDR memory.

B. Person of Ordinary Skill in the Art

71. The '366 Patent claims priority, at least in part, back to a non-provisional application filed on June 2, 2008 (EX1006), and a provisional application filed on June 1, 2007 (EX1005). The '366 Patent identifies the relevant field of art as follows: "The present disclosure relates generally to computer memory devices, and more particularly, to devices that employ different types of memory devices such as combinations of Flash and random access memories." EX1001 at 2:6-9. Based on that description of the field of art, my experience, and the prior art I discuss herein, I believe a person of ordinary skill in the art in the field of the '366 Patent in 2007 and 2008 ("Skilled Artisan" or "POSITA") would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person

would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system, including standard communication busses and protocols, such as PCI and SMBus busses and protocols. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers. Such a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry.

72. My description of a POSITA above is consistent with the description I provided previously in my expert declarations about the related U.S. Patents Nos. 11,232,054 (the ’054 Patent) (EX1053) and 11,016,918 (the ’918 Patent) (EX1054). *See* EX1069, ¶61; EX1068, ¶67. I understand that the Board, in its Final Written Decisions finding the ’054 and ’918 Patents invalid, agreed with my description of a POSITA “with the exception of the open-ended language ‘at least’ which introduces ambiguity and may encompass skill levels beyond ordinary.” EX1071 at 11-12; EX1070 at 11-13.

C. Overview of the '366 Patent

73. The '366 Patent states that it describes "a memory system having a volatile memory subsystem, a non-volatile memory subsystem, a controller coupled to the non-volatile memory subsystem, and a circuit coupled to the volatile memory subsystem, to the controller, and to a host system." EX1001 at 8:11-15. The '366 Patent explains that "[i]n a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system." *Id*. at 8:15-20. The '366 Patent further explains that "[i]n a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem to allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, and the circuit is operable to selectively isolate the volatile memory subsystem from the host system." *Id*. at 8:20-26.

74. The '366 Patent describes embodiments wherein "[t]he controller backs up the volatile memory using the non-volatile memory in the event of a trigger condition." EX1001 at 20:34-35. It lists "trigger conditions" including "a power failure, power reduction, request by the host system, etc." *Id*. at 20:36-37. It further describes that the trigger condition can occur when the memory system

detects that the system voltage is above or below a certain threshold. *Id*. at 24:38-47.

75. Figure 12 of the ’366 Patent depicts an exemplary memory system of the invention:

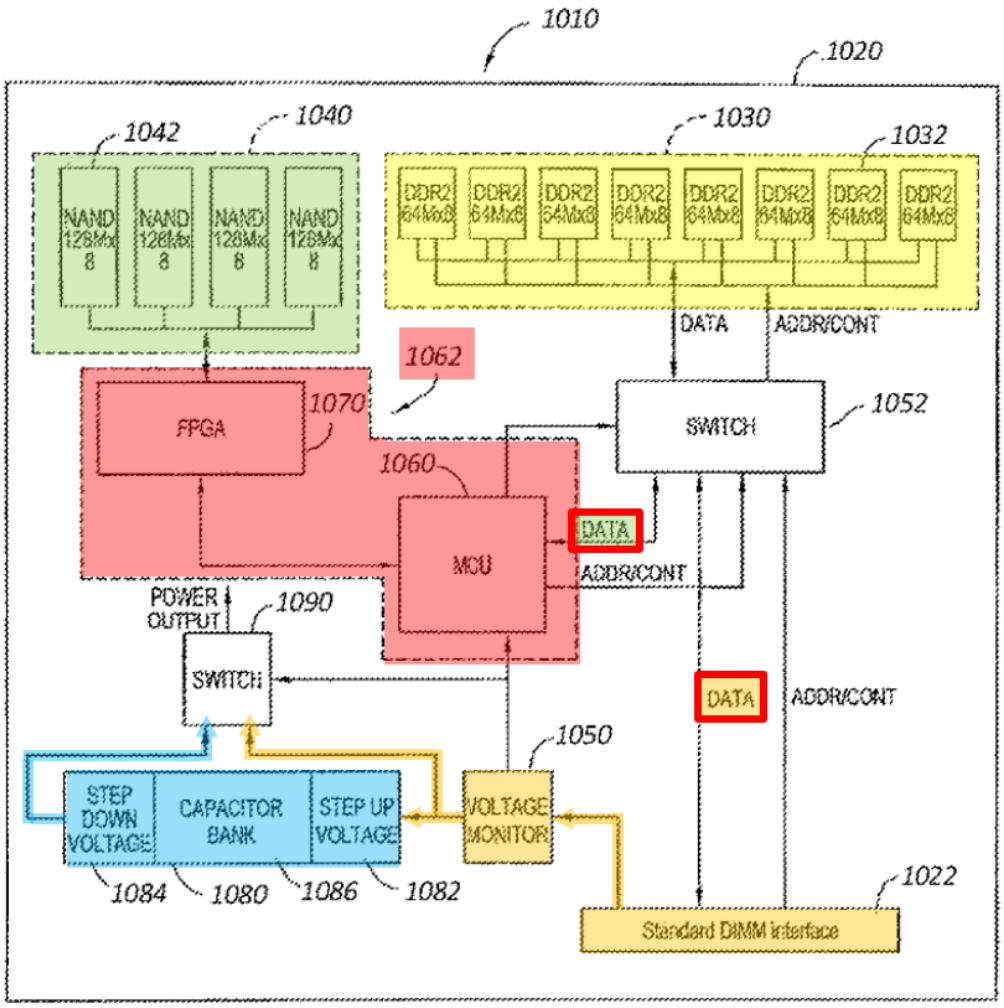


FIG. 12

EX1001 at Fig. 12 (annotated). With reference to Figure 12, the ’366 Patent describes that “[t]he memory system 1010 can be coupled to a host computer system and can include a volatile memory subsystem 1030 [yellow], a non-volatile memory subsystem 1040 [green], and a controller 1062 [red] operatively coupled

to the non-volatile memory subsystem 1040 [green]." *Id*. at 21:31-34. The system includes a "second power supply 1080 [blue]" comprising either "capacitors" or a "battery" to supply power during a power disruption. *Id.* at 26:1-39.

76. The volatile memory subsystem 1030 [yellow] "comprises a plurality of volatile memory elements 1032." EX1001 at 22:24-25. The volatile memory elements 1032 can comprise "dynamic random-access memory (DRAM) elements" including, but not limited to, "DDR, DDR2, DDR3, and synchronous DRAM (SDRAM)" elements. *Id*. at 22:31-37. The volatile memory elements 1032 may also comprise "other types of memory elements such as static random-access memory (SRAM)." *Id*. at 22:39-41.

77. The controller 1062 [red] "may comprise a microcontroller unit (MCU) 1060 and a logic element 1070." EX1001 at 24:51-52. The MCU 1060 "provides memory management for the non-volatile memory subsystem 1040 [green] and controls data transfer between the volatile memory subsystem 30 [*sic*, 1030, yellow] and the nonvolatile memory subsystem 1040 [green]." *Id*. at 24:53-56. The logic element 1070 in Figure 12 is labeled as an FPGA (field-programmable gate array). *Id*. at Fig. 12, 23:16-18.

78. The non-volatile memory subsystem 1040 [green] "comprises a plurality of non-volatile memory elements 1042." EX1001 at 22:25-27. The non-volatile memory elements 1042 can comprise "one or more flash elements"

including, but not limited to, "NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC)." *Id*. at 22:50-55. The '366 Patent describes that the non-volatile memory subsystem 1040 [green] may be used "as a flash 'mirror' to provide backup of the volatile memory subsystem 1030 [yellow] in the event of certain system conditions," i.e. trigger conditions. *Id*. at 24:24-31.

79. As shown in Figure 12, the above-described components of the memory system 1010 reside on "a printed-circuit board (PCB) 1020." EX1001 at 21:40-41. The PCB 1020 can "comprise an interface 1022 [orange] that is configured to be in electrical communication with the host system." *Id*. at 22:14-16. The interface 1022 [orange] can further "comprise a plurality of edge connections" that connect to the host system. *Id*. at 22:16-18. The interface 1022 on the memory module "provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system." *Id*. at 22:18-21.

80. The '366 Patent further describes that, in some embodiments, "the memory system 1010 includes at least one circuit 1052 configured to selectively operatively decouple the controller 1062 [red] from the volatile memory subsystem 1030 [yellow]." EX1001 at 21:35-38. It further describes that, in some embodiments, "the at least one circuit 1052 comprises one or more switches coupled to the volatile memory subsystem 1030 [yellow], to the controller 1062

[red], and to the host computer." *Id*. at 23:43-46. These switches "respon[d] to signals (e.g., from the controller 1062) to selectively operatively decouple the controller 1062 [red] from the volatile memory subsystem 1030 [yellow] and to selectively operatively couple the controller 1062 to the volatile memory subsystem 1030 [yellow]." *Id*. at 23:47-52.

81. As depicted in Figure 12, the memory system 1010 may also include a "voltage monitor 1050" which "monitors the voltage supplied by the host system via the interface 1022 [orange]." EX1001 at 25:23-25. The '366 Patent describes that "upon detecting a low voltage condition," the voltage monitor 1050 "may transmit a signal to the controller 1062 [red] indicative of the detected condition." *Id*. at 25:26-29. The controller 1062 (red) can then respond to the signal by "transmitting a signal to the at least one circuit 1052 to operatively couple the controller [(1062)] to the volatile memory system 1030 [yellow], such that the memory system 1010 enters the second state." *Id*. at 25:29-34. This process can result in the execution of a write cycle whereby "data is read from the volatile memory subsystem 1030 [yellow] and is transferred to the non-volatile memory subsystem 1040 [green] via the MCU 1060 [red]." *Id*. at 25:34-41. In some embodiments, such a write operation to the non-volatile memory subsystem 1040 (green) during power failures may involve "transfer[ring] data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 [yellow] of a

memory system 1010 to a controller 1062 [red] of the memory system 1010." *Id.* at 35:38-42, 36:17-20, Fig. 21 (annotated below). During the transfer of sliced data, the "two DRAM segments 1630, 1640" may receive respective chip select signals, CS#1 and CS#2, from the controller 1062. *Id.* at 35:51-54, Fig. 21. The '366 Patent further describes that "[t]he volatile memory subsystem 1030 [yellow] may normally be run at a higher frequency (e.g., DRAM running at 400 MHz)" during normal operations "when communicating with the host system (e.g., when no trigger condition is present)," but "the volatile memory subsystem 1030 [yellow] may be operated at a reduced frequency (e.g., at twice the frequency of the non-volatile memory subsystem 1040 [green]) … during backup operation and/or restore operations" to "advantageously reduce overall power consumption of the memory system 1010." *Id.*, 33:44-57, 35:5-32, Fig. 20.

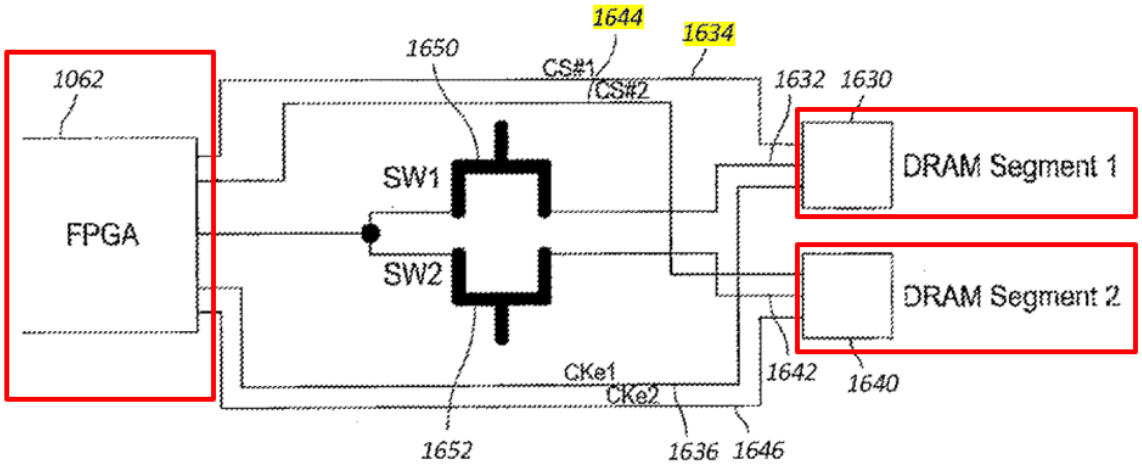


FIG. 21

82. Figure 16 of the '366 Patent depicts an exemplary power module of the memory system:

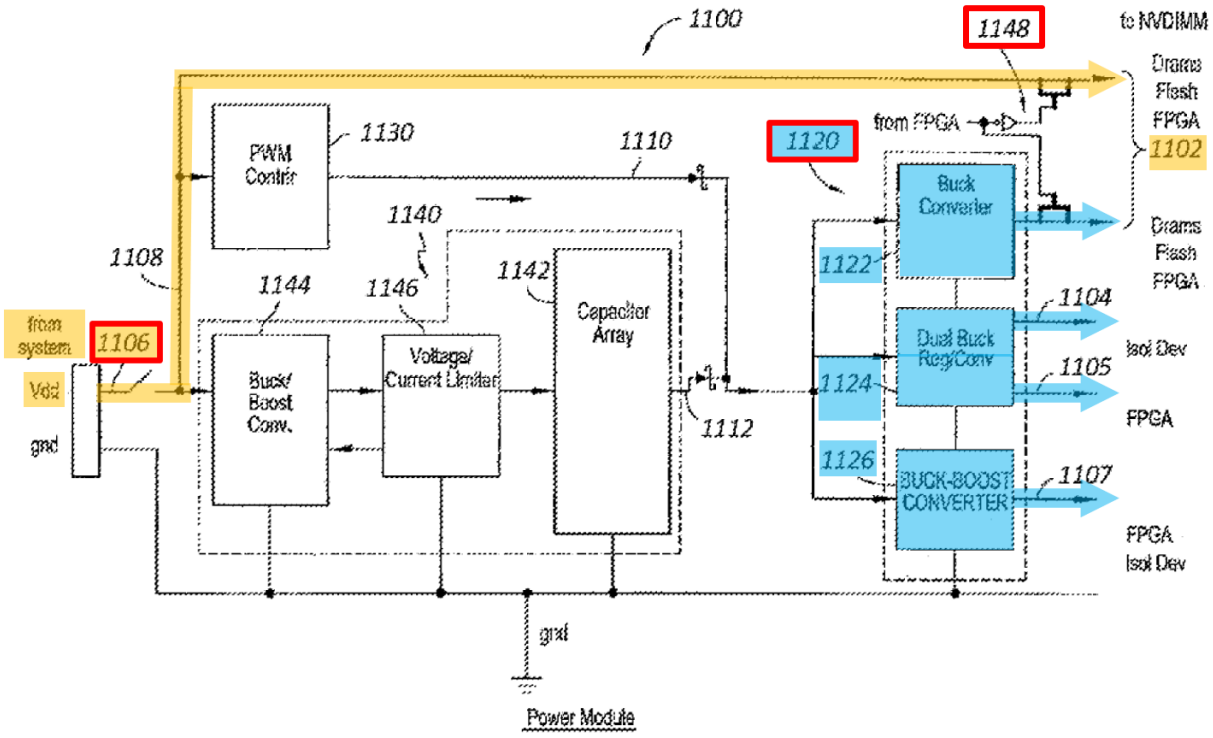


FIG. 16

EX1001 ('366 Patent) at Fig. 16 (annotated). The power module 1100 depicted in Figure 16, "provides power to the various components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition." *Id*. at 28:8-12. Specifically, the '366 Patent describes that "[t]he power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040." *Id*. at 28:17-19. It states that "[t]he plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104." *Id*. at 28:19-21.

83. The ’366 Patent describes generally that “[t]he conversion element 1120” can comprise “one or more buck converters and/or one or more buck-boost converters.” EX1001 at 29:34-35. The conversion element 1120 receives as voltage input “either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100.” *Id*. at 29:49-54. The conversion element 1120 then “reduces the input to an appropriate amount for powering various components of the memory system.” *Id*. at 29:54-55.

84. The ’366 Patent explains that the power module 1100 may provide power to the components on the memory module from different sources depending on the system power situation. EX1001 at 28:40-61. For example, during normal operations (“first state”), when there is no power failure, *id*. at 28:53-61, “the first voltage 1102 is provided to the memory system 1010 from the [system] input 1106,” and thus the components on the memory module receive power from the host system, *id*. at 28:41-45. When “a power failure is about to occur” (“second state”) or “has occurred” (“third state”), *id*. at 28:53-61, “the first voltage 1102 [or 1104] is provided to the memory system 1010 from the conversion element 1120,” and thus the components on the memory module receive power generated on the module by the conversion element 1120, *id*. at 28:45-52.

D. The Prosecution History of The '366 Patent

85. The '366 Patent is the last of several continuation and continuation-in-part applications dating back to June 2, 2008, and a provisional application filed June 1, 2007, as shown below:

Related U.S. Application Data

(63) Continuation of application No. 17/328,019, filed on May 24, 2021, now Pat. No. 11,232,054, which is a continuation of application No. 17/138,766, filed on Dec. 30, 2020, now Pat. No. 11,016,918, which is a continuation of application No. 15/934,416, filed on Mar. 23, 2018, now abandoned, which is a continuation of application No. 14/840,865, filed on Aug. 31, 2015, now Pat. No. 9,928,186, which is a continuation of application No. 14/489,269, filed on Sep. 17, 2014, now Pat. No. 9,158,684, which is a continuation of application No. 13/559,476, filed on Jul. 26, 2012, now Pat. No. 8,874,831, which is a continuation-in-part of application No. 12/240,916, filed on Sep. 29, 2008, now Pat. No. 8,301,833, which is a continuation of application No. 12/131,873, filed on Jun. 2, 2008, now abandoned.

(60) Provisional application No. 61/512,871, filed on Jul. 28, 2011, provisional application No. 60/941,586, filed on Jun. 1, 2007.

EX1001 at 1-2.

86. In my previous expert declarations on the related U.S. Patents Nos. 11,232,054 (the ’054 Patent) and 11,016,918 (the ’918 Patent), I summarized the prosecution histories of all of the applications shown above. *See* EX1068, ¶¶ 82-127; EX1069, ¶¶ 76-127; *see also* EX1005 to EX1013, and EX1052 (prosecution histories).

87. Since then, on August 28, 2023, the Board invalidated all challenged claims of the ’833 Patent, which have since been cancelled. *See* EX1088; EX1089, 26. Furthermore, on December 5 and 6, 2023, the Board invalidated all claims of the ’054 and ’918 Patents, consistent with the opinions I offered about those patents in my previous expert declarations. EX1070; EX1071; EX1072. Specifically, for the ’918 Patent, the Board (1) found Claims 1-3, 8, 14, 18, and 23 unpatentable because they were obvious over U.S. Patent Pub. No. 2006/0174140 A1 to Harris (“Harris”) (EX1023) and the JEDEC standards JEDS82-30 and JESD205 for Fully Buffered DIMM (“FBDIMM Standards”) (EX1027, EX1028); (2) found Claims 1-30 unpatentable because they were obvious over Harris, the FBDIMM Standards, and U.S. Patent No. 7,724,604 to Amidi (“Amidi”) (EX1024); and (3) found Claims 1-30 unpatentable because they were obvious over Harris, the FBDIMM Standards, Amidi, and U.S. Patent No. 6,856,556 to Hajeck (“Hajeck”) (EX1038). EX1070, 90. For the ’054 Patent, the Board (1) found Claims 1-3, 15 unpatentable because they were obvious over Harris and the

FBDIMM Standards; (2) found Claims 1-30 unpatentable because they were obvious over Harris, the FBDIMM Standards, Amidi; and (3) found Claims 1-30 unpatentable because they were obvious over Harris, the FBDIMM Standards, Amidi, and Hajeck. EX1071, 79. I understand that Netlist has appealed the Board's decisions invalidating the claims of the '054 and '918 Patents. EX1073; EX1074.

88. Below is a summary of the prosecution history of the '366 Patent (Application No. 17/582,797), which was filed as a continuation of the most recent application shown above (Application No. 17/328,019 resulting in the '054 Patent).

89. Application No. 17/582,797 was filed on January 24, 2022, as a continuation of the applications shown above. EX1002, 1, 3, 9-10.

90. On October 12, 2022, the Examiner rejected the pending claim for double patenting against claim 1 in the '918 Patent. EX1002, 168-75.

91. On April 12, 2023, the applicant responded to the rejection by cancelling pending claim 1 and submitting a new set of 14 claims. EX1002, 298-304.

92. On July 13, 2023, the Examiner issued a Final Rejection, rejecting all pending claims for failure to comply with the written description requirement of 35 U.S.C. Section 112(a) or 35 U.S.C. Section 112 (pre-AIA). EX1002, 345-350. In particular, the Examiner pointed out that the reference to a "fourth buck converter"

and "fourth regulated voltages" was not supported by the specification. *Id*., 348-49. This rejection was discussed in an Examiner interview on September 13, 2023. *Id.* at 373-75.

93. On October 13, 2023, the applicant submitted a Request for Continued Examination with amendments to the claims and arguments responding to the written description issue raised by the Examiner. EX1002, 389-90, 425-32. The applicant identified "buck-boost converter 1126" in the specification as the "4th buck converter," based on counting the "dual buck converter 1124" as both the 2nd and 3rd buck converters. *Id*., 430-31. The applicant further pointed to the statement in the paragraph [00149] of the specification that "there may be more or less sub-blocks [in conversion element 1120] which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values." *Id*., 431 (brackets added by applicant); *see also id.*, 441-48 (Supplemental Response making same arguments).

94. On November 8, 2023, the Examiner issued a Notice of Allowance, agreeing with the applicant's arguments about the previous written description rejection. EX1002, 479-86.

95. On December 5 and 6, 2023, the Board invalidated all claims of the parent '054 and '918 Patents, consistent with the opinions I offered about those patents in my previous expert declarations. EX1070; EX1071; EX1072

96. Despite the prior claim set being allowed, on February 8, 2024, the applicant submitted a Request for Continued Examination with extensive amendments and new claims. EX1002, 491-503, 510-11. The applicant did not discuss the Final Written Decisions invalidating all claims of the ’054 and ’918 Patents, *see id.*, and instead submitted them in an Information Disclosure Statement without explanation, *see id.* at 507, 523.

97. Without issuing any substantive rejection to the new claims, and without discussing the Final Written Decisions invalidating all claims of the ’054 and ’918 Patents, on February 28, 2024, the Examiner issued a second Notice of Allowance, noting that the amended and new claims contained the previously allowed subject matter. EX1002, 528-35.

98. On May 28, 2024, the applicant submitted another Request for Continued Examination with remarks specifically identifying the Final Written Decisions invalidating all claims of the’054 and ’918 Patents, but with no discussion of those Final Written Decisions or any explanation why the pending claims would be allowable in light of those Final Written Decisions. EX1002, 565-71.

99. On August 8, 2024, the Examiner issued a rejection finding the pending claims unpatentable over Harris in view of the FBDIMM Standards and Amidi, and the Board’s Final Written Decision on the related ’918 Patent.

EX1002, 645-62. The rejection was discussed in an Examiner interview on September 6, 2024. *Id.* at 663-83.

100. On October 1, 2024, the applicant responded by amending pending claim 2, cancelling the remaining pending claims, and submitting forty-one new claims numbered 28-68, along with remarks attempting to distinguish Harris in view of the FBDIMM Standards and Amidi, and the Board's Final Written Decision on the related '918 Patent. EX1002, 1122-66. The applicant included a chart attempting to identify written description support in the specification for the proposed amendments. *Id.* at 1169-1236.

101. On January 24, 2025, the Examiner issued a Final Rejection rejecting all pending claims for failure to comply with the written description requirement of 35 U.S.C. Section 112(a) or 35 U.S.C. Section 112 (pre-AIA), and rejecting three pending claim as indefinite, and finding "not…persuasive" the applicant's remarks attempting to distinguish Harris in view of the FBDIMM Standards and Amidi and the Board's Final Written Decision on the related '918 Patent. EX1002, 1261-74. The Examiner identified the following limitations as lacking written description support:

- "the memory-socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits"

- "a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board"
- "wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines"
- "in response to the detected trigger condition, the logic element is configured to perform a plurality of write operations, including: a first write operation to write a first set of data bits into a first portion of the data storage element; a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations"
- "the trigger condition occurs when the input voltage goes above both the first and second threshold voltages"
- "wherein: a specified operating voltage value is within a range of operating voltage values of the DIMM, the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value"

- "each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the system board"
- "wherein, when the system power is provided to the DIMM from the system board: the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and wherein: a specified operating voltage value is within a range of operating voltage values of the DIMM, the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value"
- "when the system power is provided to the DIMM from the system board: the first and second groups of DDR SDRAM packages are configured to be **accessible and not in self-refresh mode**; the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and the 40 1-bit wide DDR data signals

include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits."

EX1002, 1264-66 (emphasis in original).

102. On March 5, 2025, the applicant initiated an interview with the Examiner, to discuss the Section 112(a) written description rejection. EX1002, 1277-1390. The applicant agreed in the interview to provide a table that maps claim limitations to supporting portions of the specification. *Id.* at 1276.

103. On March 24, 2025, the applicant submitted another Request for Continued Examination, with a response to the prior Final Rejection. EX1002, 1393-94. In addition, the applicant heavily amended the pending claims — removing numerous limitations and adding new limitations — and included remarks attempting to distinguish the Harris reference (without addressing the Final Written Decisions for the '918 and '054 Patents finding claims of those patents obvious in light of Harris in view of the FBDIMM Standards and Amidi). *Id*., 1398-1432, 1482-96. As agreed during the prior interview, the applicant also provided a chart purporting to show where the specification provided written description support for the limitations of the claims. *Id*., 1433-81. However, as

discussed below, the applicant's arguments in the chart purporting to identify support in the written description improperly engaged in hindsight by picking and choosing from a laundry list of options in the specification without identifying a disclosure of the specific combination of all limitations recited in each claim (*infra*, ¶¶ 117-118), and also improperly mixed distinct modes of operation described in the specification (*infra*, ¶¶119-125), and also failed to adequately justify negative limitations (*infra*, ¶¶126-130), and also improperly relied on unsupported interpretations (*infra*, ¶¶131-135).

104. On April 7, 2025, the applicant filed a "Petition to Make Special" based on the age of the inventor being over 65, EX1002 at 1500, which was granted the same day, *id.* at 1497. My understanding is that a "Petition to Make Special" can cause the Examiner to act more quickly during examination.

105. On April 17, 2025, the applicant submitted a supplemental amendment following Examiner interviews on April 10, 16, and 17. EX1002, 1503-21. The record does not include any indication why the Examiner believed (contrary to his previous rejections) that the claims had written description support or why the claims were non-obvious over Harris in view of the FBDIMM Standards and Amidi and the Board's Final Written Decision on the related '918 Patent.

106. On April 28, 2025, the Examiner issued a Notice of Allowance, with a minor Examiner Amendment to a dependent claim. EX1002, 1531-40. The Examiner stated, without explanation, that "[i]n the previous office action mailed 01/24/2025, the claims were rejected under the 35 USC 112, first paragraph as not complying with the written description requirement. The Application has overcome the 112 rejection." *Id.* at 1536. The Examiner did not specifically distinguish any particular prior art but instead provided the following conclusion why the claims were "patentably distinct from the prior art of record":

> ***the pending claims, in light of the specification, the Examiner finds the claimed invention to be patentably distinct from the prior art of record. The prior art of record neither anticipates, nor renders obvious the recited combination as a whole, including the limitation of*** "wherein the plurality of DDR SDRAM devices includes: a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal: a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

> • the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
>
> • the at least 40 1-bit DDR data signals include 32 1-bit wide-DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals: and wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits."
>
> *7. Independent claims **29-39, 41-43, 45, 47-57, and 60-67** are allowable at least for reasons recited above including all the limitations of the allowable independent base claim upon which they depend..*

Id. at 1538-39. However, as explained below, in my opinion the claim limitations identified by the Examiner above for distinguishing the prior art concern features found in the DDR5 standard dated approximately 10 years ***after*** the effective filing date of the '366 Patent, and there is no written description for those features in the application for the '366 Patent. *See infra* ¶¶116-125. In other words, in my opinion, the Examiner distinguished the prior art based on claim limitations not properly supported by the written description of the '366 Patent.

107. On May 19, 2025, the applicant submitted a further Request for Continued Examination with additional amendments to the claims, and new claims 69-77, without explanation of the reason for the amendments or any support in the written description for the amendments. EX1002, 1544-66.

108. On June 3, 2025, the applicant submitted a Supplemental Response reverting the claim language substantially back to the previously allowed claim language on April 28, 2025, based on feedback from the Examiner that US Patent Publication 2004/0193777 (LaBerge) and US Patent Publication 2004/0143773 (Chen) "may be used to reject the currently pending claims, filed on May 19, 2025" but that "if the claims were restored to their previously allowed form, as of April 17, 2025 (Supplemental Amendment), and allowed by the Examiner in the Notice of Allowance of April 28, 2025, then they would again be allowed." EX1002, 1570-85, 1589-1606.

109. On June 18, 2025, the Examiner issued another Notice of Allowance. EX1002, 1606, 1609, 1617-25. Similar to the previous Notice of Allowance on April 28, 2025 discussed above, *supra* ¶ 106, the Examiner provided no explanation as to why the claims had written description support. Nor did the Examiner specifically distinguish any particular prior art. Instead the Examiner provided the following conclusion why the claims were "patentably distinct from the prior art of record":

The reason for allowance of the independent claim 2 are the following: in interpreting the pending claims, in light of the specification, the Examiner finds the claimed invention to be patentably distinct from the prior art of record. The prior art of record neither anticipates, nor renders obvious the recited combination as a whole, including the limitation of: "wherein each component of the set of components: (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and wherein the plurality of DDR SDRAM devices includes: a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode: the first group of DDR SDRAM

devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 32 1-bit DDR data signals in parallel via at least 32 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and wherein the sum of the at least 32 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 64 data conduits."

Independent claims 44 and 58 include similar limitations as claim 1 and are allowed for the reasons recited above with respect to claim 1.

*6. Independent claims **29-39, 41-43, 45, 47-57, and 60-67** are allowable at least for reasons recited above including all the limitations of the allowable independent base claim upon which they depend.*

EX1002, 1623-24. I note that the claim language quoted by the Examiner above does not actually match the claim language in issued claim 1 (or dependent claim 2). Furthermore, as explained below, in my opinion the claim limitations identified by the Examiner above for distinguishing the prior art concern features found in the DDR5 standard dated approximately 10 years ***after*** the effective filing date of the '366 Patent, and there is no written description for those features in the application for the '366 Patent. *See infra* ¶¶116-130. In other words, in my

opinion, the Examiner distinguished the prior art based on claim limitations not properly supported by the written description of the ’366 Patent.

110. On June 24, 2025, the applicant paid the Issue Fee. EX1002, 1630.

111. On July 29, 2025, the application issued as U.S. Patent No. 12,373,366 with 38 claims. EX1002, 1643-46; EX1001, 1 and 50.

E. Construction of Terms Used in the ’366 Patent Claims

112. I understand that claim terms should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. For purposes of my analysis below, I do not believe that any of the claims of the ’366 Patent require an explicit claim construction. While I understand that Patent Owner appears to have interpreted the claims of the ’366 Patent broadly for purposes of infringement against DDR5 products, *see, e.g.*, EX1100 at 13-25; EX1101 at 14-26, and that a narrower interpretation may be more reasonable, in my opinion the claims are both invalid under § 112 and obvious in light of the prior art regardless of the precise interpretation of their plain and ordinary meaning, as shown by my analysis below.

113. I also understand that in district court litigation involving the related ’918 and ’054 Patents, the district court provided the following claim constructions for terms in those patents:

"dual buck converter" ('918 Patent, Claims 2, 17, 28) "dual-buck converter" ('054 Patent, Claim 15)	"a buck converter with two regulated voltage outputs"
"pre-regulated input voltage" ('918 Patent, Claims 16, 30)	Plain and ordinary meaning
"first" / "second" / "third" / "fourth" "regulated voltages" / first"; "second" / "third" / "fourth" "voltage amplitude" ('918 Patent, Claim 1 and most other claims)	Plain and ordinary meaning.
"at least three regulated voltages" ('054 Patents, Claims 1–15)	Plain and ordinary meaning.

"plurality of regulated voltages" ('054 Patents, Claims 16, 24)	Plain and ordinary meaning.
"a second plurality of address and control signals" ('918 Patent, Claims 1, 21)	Plain and ordinary meaning.
"a memory module" ('918 Patent, all claims; '054 Patent, all claims)	Limiting.

EX1083, 34-35; *see also id.* at 17-28. Except for "memory module," "first" / "second" / "third" / "fourth" "regulated voltage[s]," and "address and control signals," none of these terms appear in the '366 Patent claims. The term "memory module" in the preamble was treated as "[l]limiting," which does not change my analysis below, because the prior art teaches a "memory module," and the other terms that appear in the '366 Patent were given their "[p]lain and ordinary

meaning," consistent with my analysis below. As such, my analysis below is consistent with the claim constructions above and is not affected by the appeal from the district court litigation involving the '918 and '054 Patents. *See generally* EX1095, EX1096, EX1097.

114. In the Final Written Decisions involving the related '918 and '054 Patents, I understand that the Board applied the following claim constructions, which were consistent with the expert opinions about obviousness that I offered in those proceedings and that the Board ultimately agreed with:

- "*memory module*": "[W]e agree with Petitioner that the term 'memory module' is not limited to '*main* memory modules . . . designed to connect to the *primary* memory controller.' We agree with Patent Owner that the 'memory module' includes structure to connect with a 'host system' including its memory controller." EX1070, 17 (internal citations omitted); *see also* EX1071, 16-17 (similar).
- "*pre-regulated input voltage*": "Under its ordinary and plain meaning in the context of the '918 patent, we understand 'pre-regulated input voltage' to mean that the voltage is regulated before conversion to a stepped up or down level by the voltage converters. […] This is consistent with Patent Owner's proposed construction." EX1070, 18 (internal citations omitted).

My analysis below is consistent with the claim constructions above, with the understanding that the term "pre-regulated input voltage" does not appear in the claims of the '366 Patent.

IV. WRITTEN DESCRIPTION (Ground 1)

115. In my opinion, all claims of the '366 Patent fail to satisfy the written description requirements as explained below. I refer to this as Ground 1. My understanding of the legal requirements for written description is provided above. *Supra* ¶¶ 47-54.

116. Fundamentally, the '366 Patent appears to be trying to claim as its invention specific requirements in the new DDR5 standard for DDR SDRAM memory — which was released a decade after the priority date of the '366 Patent — even though the '366 Patent does not disclose any of those DDR5 requirements. *See, e.g.*, EX1086 (overview of DDR5 dated 2020). Furthermore, the claims of the '366 Patent purport to distinguish the prior art based on these requirements of the DDR5 standard that are not disclosed by the '366 Patent. *See, e.g.*, limitations [1.i.2], [16.i.2], [29.i.2]. For example, the new DDR5 standard includes distinctive features, such as "***two*** independent subchannels," each 40 bits wide, between the memory module and the host computer, as shown below. *See* EX1086, 1 ("key difference of the DDR5 module as compared to a DDR4 module"); EX1101, ¶¶31, 49, 69-78; EX1100, ¶¶31, 69-78. "Each subchannel has up to two physical

package ranks," and thus, in the DDR5 configuration, each subchannel can be independently selected by the respective chip select signal. EX1086, 1.

Module Layout and Data Access

A key difference of the DDR5 module as compared to a DDR4 module is the presence of subchannels (Figure 1). A standard DDR5 module has two independent subchannels. Each subchannel has up to two physical package ranks. Each DRAM package can be configured in a primary/secondary topology to enable additional logical ranks for increased density.

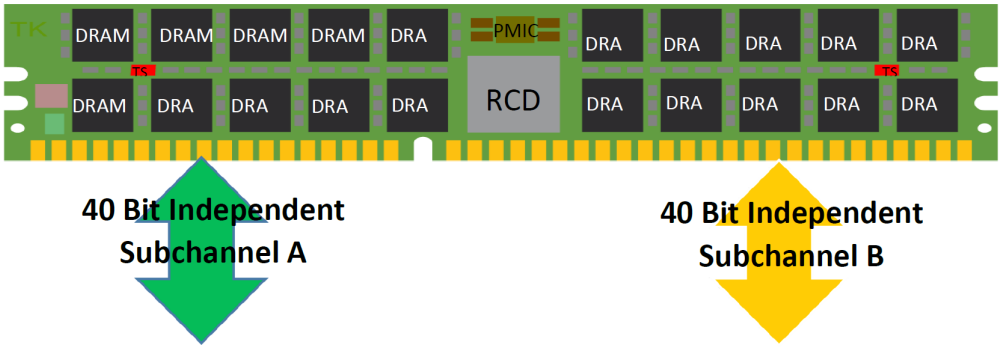


Figure 1: DDR5 2Rx4 RDIMM module illustrating two independent subchannels

The DDR5 standard thus differs from the previous standards (DDR1 to DDR4) that disclosed a ***single*** 72-bit-wide channel controlled by a ***single*** chip-select signal from the host computer. *See, e.g.*, EX1104, 10 ("x72", "CS: SDRAMs D0-D8"). But the '366 Patent does not provide any written description for these new features of the DDR5 standard.

117. In my opinion, the '366 Patent fails to disclose the ***specific combination*** of ***all*** limitations recited in each independent claim. As shown in the table below, each independent claim of the '366 Patent requires an extraordinarily long combination of limitations, reflected in the word count below, which is not actually described in the '366 Patent:

Independent Claim No.	**Words in claim**
1	910
16	915
29	933

See infra p.174 (reprinting the claim language). In the sections below, I identify specific limitations in the claims of the '366 Patent that lack written description, but there is also no disclosure of the ***combination*** of ***all*** the limitations below (along with all of the other limitations in each claim reflected in the word count above). To the contrary, the '366 Patent repeatedly states, over 100 times, that certain features "may" (or may not) be included in "certain" embodiments, *see generally* EX1001 — without ever identifying ***any*** particular embodiment that actually ***combines*** all the limitations in the manner ***required*** by the claims. In doing so, the specification provides a laundry list of possibilities, discussed in isolation and introduced as merely optional, which I understand is insufficient to support written description under the law. *Supra* ¶¶47-54. With this disclosure, a Skilled Artisan would not have understood that the inventor actually possessed the specific combination of limitations now recited in the challenged claims.

A. "at least" (all claims)

118. Each independent claim of the '366 Patent uses the claim language "at least" in order to encompass infinite possible combinations, including the requirements of the new DDR5 standard, *supra* ¶116 — such as two groups of five

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Ex. 1003, p. 61

DDR5 SDRAM, each group 40-bits wide, resulting in a total width of 80 bits — which is not actually described in the '366 Patent. *Compare* EX1001, 35:60-36:1 (40+32=72 bits); EX1104, 5 ("64/72 bit-wide"), *with* limitations [1.h.3], [16.h.3], [29.h.3] ("at least four"), [1.i.3], [16.i.3], [29.i.3] ("at least 40" and "at least 32"), [1.j.2], [16.j.2], [29.j.2] ("at least 72"). For example, the claims try to encompass 80 bits (as in the DDR5 standard) by broadly claiming "at least 72," but there is no upper limit to "at least 72" and no disclosure in the '366 Patent for either 80 bits or "at least 72" bits with no upper limit.

B. During normal operation, enabling a first group of DDR SDRAM "in response to the first chip select signal…independently of whether the second group of DDR SDRAM devices is enabled" (all claims)

119. There is also no written description for the requirement in each independent claim of splitting DDR SDRAM memory devices on a DIMM memory module into two groups — such as two 40-bit-wide subchannels — that are enabled "***independently***" by two separate chip select signals, similar to the DDR5 standard discussed above, *supra* ¶116. *See* limitations [1.i.2], [16.i.2], [29.i.2]; *see also* limitations [1.i.2] ("first group of DDR SDRAM devices…receive or output…via at least 40 data lines"), [1.j.2] ("the total number of data conduits is at least 72 data conduits"), [16.i.2], [16.j.2], [29.i.2], [29.j.2] (similar). Critically, the claims require the use of independent chip select signals during what the specification calls "***normal operation***" (or the "first state"

operation). The specification distinguishes normal operations from backup/restore operations and explains that "normal operation" is when the "memory system 1010 is ***not*** performing a ***backup or restore*** operation [between the volatile DDR SDRAM memory (yellow below) and the non-volatile memory (green below), due to a power failure] and [instead the volatile DDR SDRAM memory (yellow below)] is communicating with the host system [via the orange "Standard DIMM Interface" 1022 below]," EX1001, 33:64-66; *see also id*. 20:30-41 ("The controller backs up the volatile memory using the non-volatile memory in the event of a trigger condition. Trigger conditions can include, for example, a power failure, power reduction, request by the host system, etc."), 25:8-22 ("The at least two states can comprise a first state in which the controller 1062 and the non-volatile memory subsystem 1040 are operatively decoupled (e.g., isolated) from the volatile memory subsystem 1030 by the at least one circuit 1052 and a second state in which the volatile memory subsystem 1030 is operatively coupled to the controller 1062 to allow data to be communicated between the volatile memory subsystem 1030 and the nonvolatile memory subsystem 1040 via the controller 1062."), Fig.12 (below annotated).

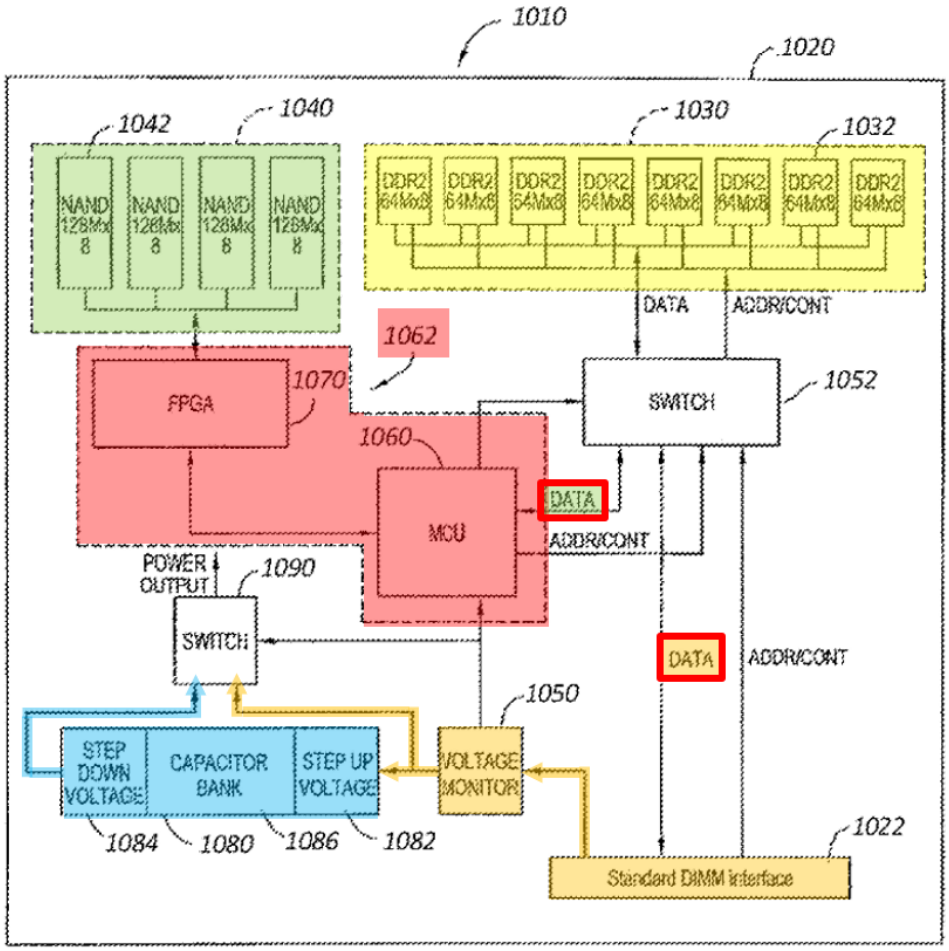


FIG. 12

120. The difference between ***normal*** and ***backup/restore*** operations is significant because they use different pathways for each respective purpose. For normal operations, the memory module uses "Standard DIMM Interface 1022" (orange) above to communicate data signals (orange) with the system memory controller. EX1001, 22:13-23. In contrast, during backup/restore operations, the "Standard DIMM Interface 1022" is disabled and data from the memory devices (yellow) is transferred to the non-volatile memory (green). *Id*., 25:8-22. Also, the two operations are performed at different ***frequencies***, so that power consumption

can be optimized: "The volatile memory subsystem 1030 may ***normally*** be run at a ***higher*** frequency (e.g., DRAM running at 400 MHz)…when communicating with the host system (e.g., when no trigger condition is present)…[T]he volatile memory subsystem 1030 may be operated at a ***reduced*** frequency…during ***backup operation and/or restore*** operations….[which] may advantageously reduce overall power consumption of the memory system 1010." EX1001, 33:44-57. During normal operations, the non-volatile memory (green) is "isolate[ed]" by the "SWITCH" (1052) to reduce "capacitive load" on the volatile memory (yellow) so that the volatile memory (yellow) can perform "high-speed" operations with the host computer (across the "Standard DIMM Interface" in orange). *Id*. 20:42-55, 25:8-22, 25:46-62 (isolating and reducing "capacitive load" is "particularly advantageous in relatively high-speed memory systems where loading effects can be significant.").

121. In the claims, the requirement that two groups of DDR SDRAM devices are enabled "***independently***" by two separate chip select signals ***during normal operation*** is shown by the limitation requiring "power from the power rails on the system board is provided to the DIMM [via the orange 'Standard DIMM Interface' 1022 above] and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode" ([1.i.1], [16.i.1], [29.i.1]) and by the limitation requiring each group of DDR SDRAM devices on the DIMM is

"enabled…to receive or output…data signals…via…the set of data lines" that are "electrically connected to the second set of edge connections [part of the orange 'Standard DIMM Interface' 1022 above]" leading to the host computer ([1.i.2], [1.b.1], [1.b.7], [16.i.2], [16.b.1], [16.b.7], [29.i.2], [29.b.1], [29.b.7]). *See* EX1001, 22:13-23, 25:8-22, 26:1-5, 26:57-65, 32:43-45, 33:64-66, 37:2-15, 38:5-9. This combination of "***independent***" chip select signals for two groups of DDR SDRAM devices during ***normal operations*** is nowhere described in the specification of the '366 Patent.

122. During prosecution, to try to show written description for the claim language requiring independent chip select signals during ***normal operations***, Netlist pointed to the "slicing" operation that is performed during slower ***backup/restore operations***, where the volatile memory (yellow above) transfers data (green above) to the non-volatile memory (green above) internally on the DIMM for backup. *See* EX1002, 1441-42 ("The method 1600 may generally be referred to as 'slicing' the volatile memory during a backup operation" (quoting EX1001, 37:31-33)). This "slicing" operation during ***backup/restore operations*** does not provide written description for the claims, which require "independently" controlling the two groups of DDR SDRAM (i.e., volatile memory) with two different chip select signals during ***normal operations*** (i.e., with the host computer via the orange "Standard DIMM Interface" 1022).

123. In fact, the only discussion of chip select signals in the '366 Patent are chip select signals 1634 and 1644 depicted in Figure 21 (below) in the context of slower ***backup/restore*** operations with the non-volatile memory via the FPGA controller 1062 (red above and below), which does ***not*** output data or control signals to the host computer during faster normal operations (via the orange "Standard DIMM Interface" 1022 above):

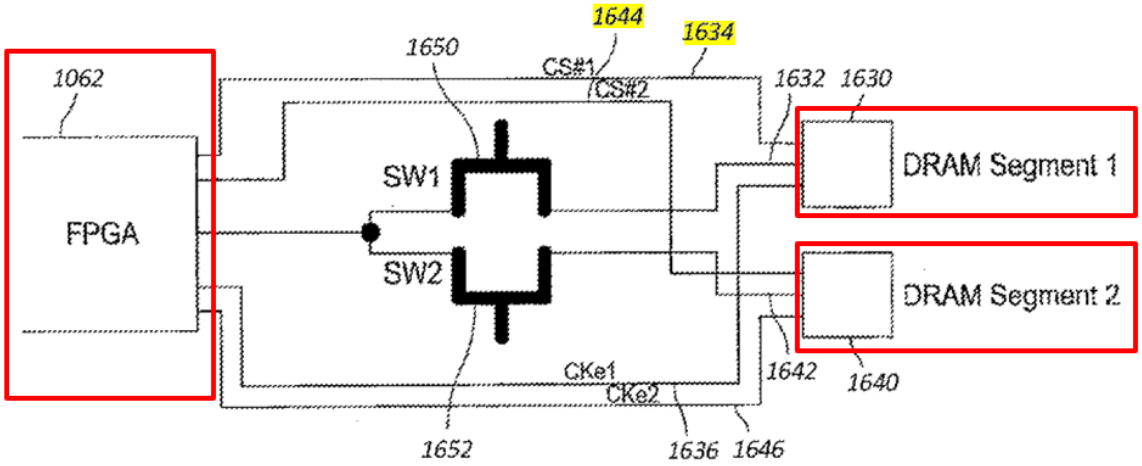


FIG. 21

EX1001, 35:38-42, 36:3-47, Fig.21. As shown above and described in the specification, these chip select signals (1634, 1644) come ***from the FPGA controller*** 1062 to independently select "DRAM Segment" 1/2, and they are part of the "connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030…to ***a controller 1062***." EX1001, 35:38-41. Thus, the chip select signals 1634 and 1644 in Figure 21 are not typical chip select

signals coming ***from the host computer*** (using "Standard DIMM Interface" 1022) during normal operations. Indeed, as shown by Figure 12 (reprinted again below), the controller 1062 does not interface with the host computer (via the orange "Standard DIMM Interface" 1022 used for faster normal operations), and instead only interfaces with the non-volatile memory (green) used for slower backup/restore operations. *See* EX1001, 33:44-57, 36:42-47, 37:31-33, Fig.22 (explaining that after receiving data from DRAM segments, the controller 1062 "writes each complete word or block of words to the non-volatile [i.e., backup] memory subsystem 1040").

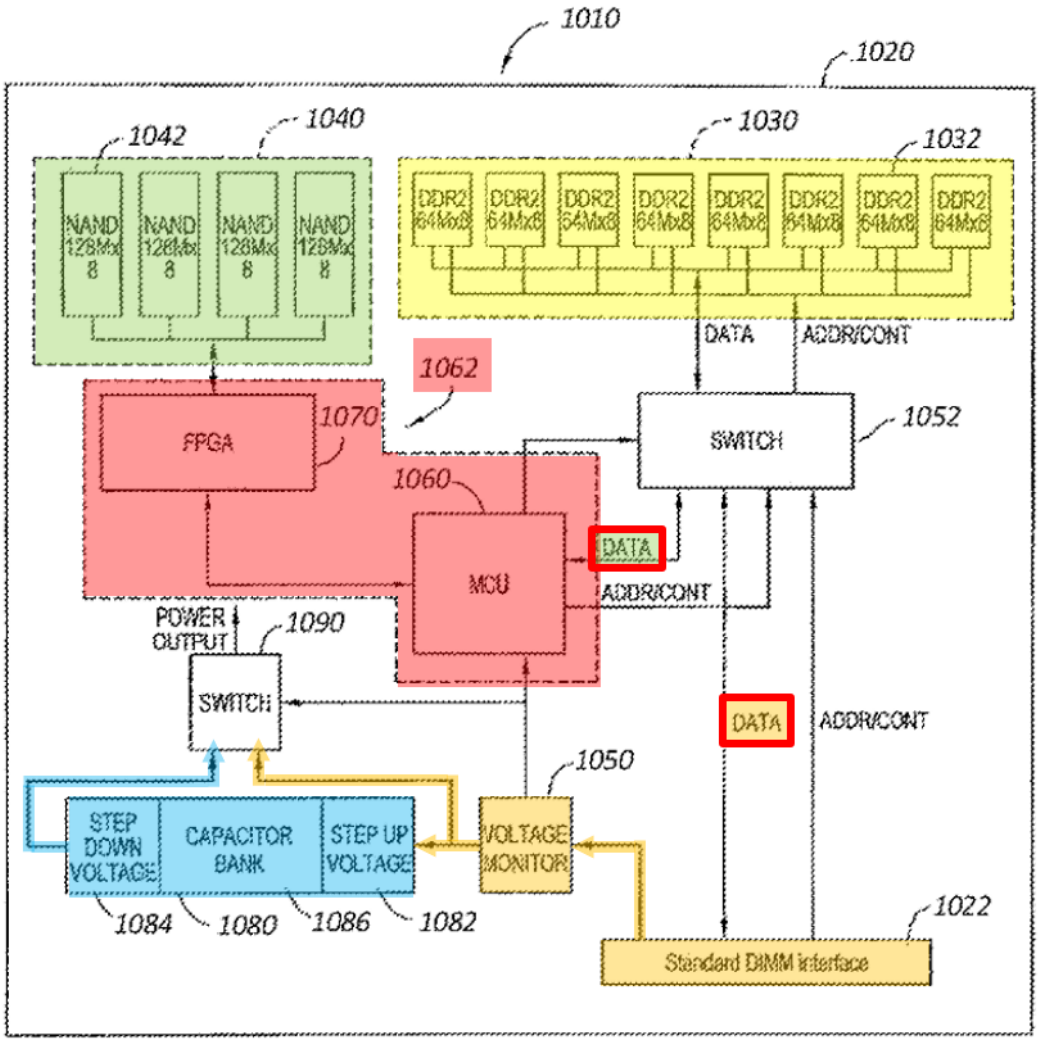


FIG. 12

124. Thus, the "slicing" operations during backup/restore with the non-volatile memory (green above) do not provide written description for the claims. The chip select signals 1634 and 1644 in Figure 21 ***from the controller 1062*** (red above) to independently select a "DRAM Segment" and transfer data to the nonvolatile memory are ***different*** from chip select signals ***from the host computer*** to enable the "DDR SDRAM devices [yellow above]…to receive or output…data signals…via…the set of data lines" that are "electrically connected to the second

set of edge connections [part of the orange 'Standard DIMM Interface' 1022 above]" leading to ***the host computer***, as required by limitations [1.i.2], [1.b.7], [16.i.2], [16.b.7], [29.i.2], [29.b.7]. In the claims, "the set of data lines" refers to data lines that connect the DDR SDRAM memory devices (yellow above) to the host system via edge connectors (orange above). *See* limitations [1.a.3] ("***data signals*** are transferred between ***the system board*** and the DIMM ***via the set of data conduits***"), [1.b.4] ("***a second set of edge connections*** configured to be electrically ***connected to the set of data conduits***"), [1.b.7] ("***a set of data lines*** electrically ***connected to the second set of edge connections***"), [1.d.2], [16.a.3], [16.b.4], [16.b.7], [16.d.2], [29.a.3], [29.b.4], [29.b.7], [29.d.2]. However, as shown by the green "DATA" going from "SWITCH" 1052 to the FPGA controller 1062 (red) in Figure 12 above, and as shown by Figure 21 above (data lines 1632, 1642), the data lines associated with chip select signals 1634 and 1644 connect "DRAM Segment[s]" 1630, 1640 to the FPGA controller 1062 for backing up or restoring data to/from the non-volatile memory (green in Figure 12 above), and those data lines are not connected to the edge connections (orange in Figure 12 above) leading to the host computer as required by the claim language. Such backup and restore operations, which occur when the host computer fails, are entirely internal to the DIMM memory module, and thus they do not utilize the data lines

connecting to the host computer via the edge connections as required by the claim language.

125. Figure 22 (below left) further distinguishes between normal operations (1610 below) and backup operations (1620 below). EX1001, 36:59-37:48, Fig.22. As shown below, Figure 22 delineates between a "first [normal] mode of operation" (1610) that involves "communicating data words between the volatile memory subsystem 1030 and the host system," EX1001, 35:7-9, and "second [backup] mode of operation" (1620) that involves "transferring data words from the volatile memory subsystem 1030 to the non-volatile [i.e., backup] memory subsystem 1040," EX1001, 35:12-16. The first mode corresponds to normal operations—e.g., "when no trigger condition has occurred and the memory system is not performing a backup and/or restore operation or is not being powered by a secondary power supply," EX1001, 37:3-6 — and the second mode corresponds to backup operations "when a trigger condition (e.g., a power failure) occurs," EX1001, 37:14-15.

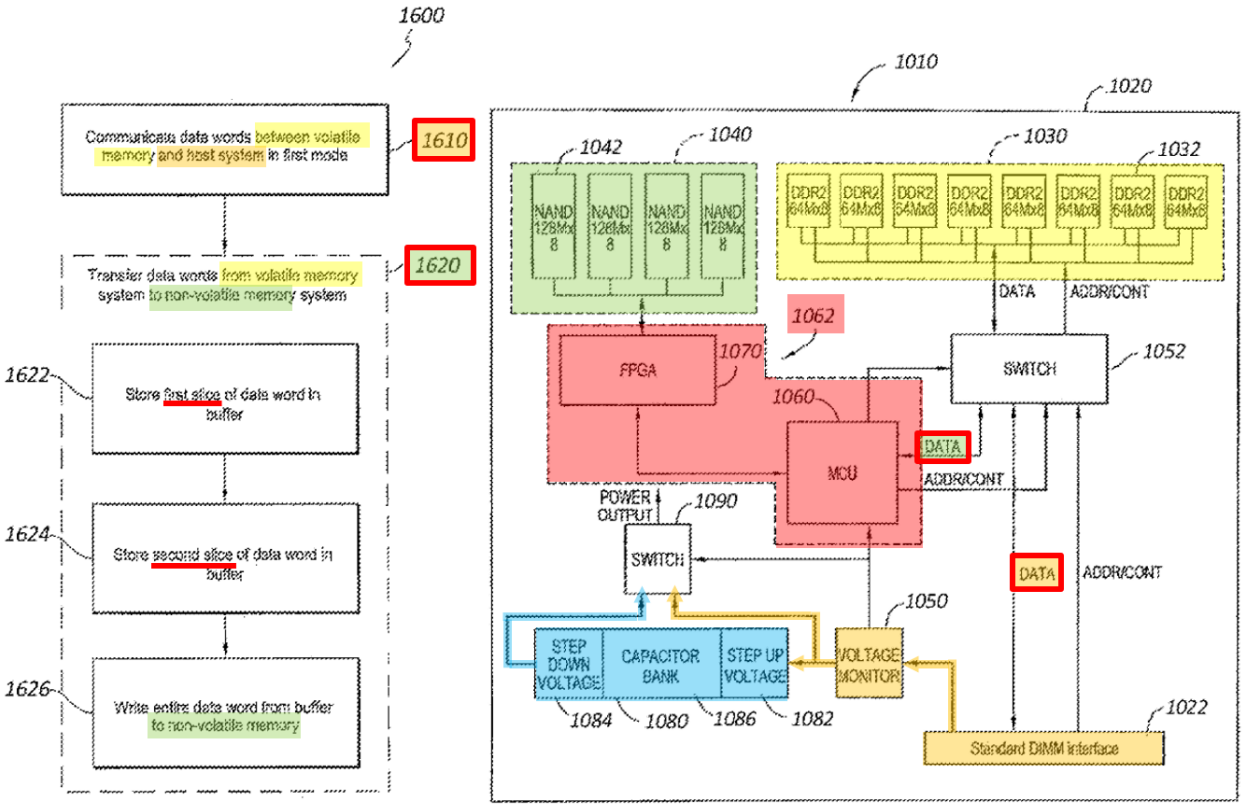


FIG. 22

Figure 22 (above left) further confirms that the "slicing" operations (1622, 1624) disclosed in the specification only occur in the second (backup) mode (1620), and ***not*** during normal operations when data is communicated with the host system (1610). And because the '366 Patent does not teach "slicing" the volatile memory (using internally generated chip select signals 1634 and 1644) during faster normal operations with the host computer, there are no disclosed embodiments in the specification that use independent chip select signals during normal operations as claimed.

C. <u>"each component of the set of components…receives power only via the one or more of the first, second, third, and fourth regulated voltage lines" (all claims)</u>

126. There is also no support in the specification that "the set of components" on the DIMM memory module (including the volatile DDR SDRAM memory) "receives power ***only*** via the one or more of the first, second, third, and fourth regulated voltage lines," *see* limitations [1.g.3], [16.g.3], [29.g.3], and certainly not during normal operations (when no power failure is detected) as required by the claims as discussed above, *supra* ¶¶119-125. Because "only" excludes features, I understand that this is properly characterized as a negative limitation, meaning that the specification generally must describe a reason to exclude the feature in order to satisfy the written description requirement. *See supra* ¶ 54.

127. During prosecution, Netlist mapped the four "regulated voltage" lines to those highlighted in blue in Figure 16 below:

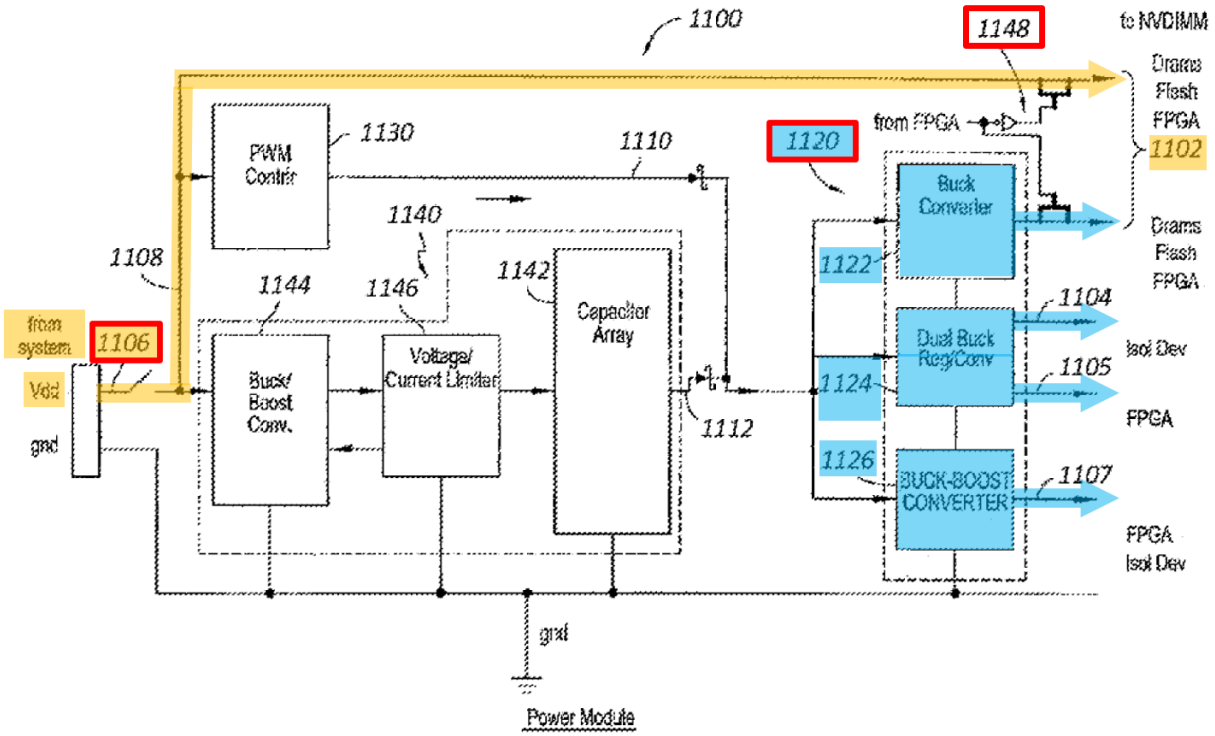


FIG. 16

See EX1002, 1437-38 (citing EX1001, Figs.12, 16, 29:33-30:3 ("The conversion element 1120 can comprise one or more buck converters….")); *see also* limitations [1.e], [16.e], [29.e]. But as shown by the orange highlighting in Figure 16 above, the '366 Patent teaches that during normal operation (when there is ***not*** a power failure) the power to 1102 (in the upper right, connecting to "FPGA," "Flash," and to "Drams," which is part of the claimed "set of components" according to [1.d.1], [1.f.1]-[1.f.2], [16.d.1], [16.f.1]-[16.f.2], [29.d.1], [29.f.1]-[29.f.2]) comes "from system" (as shown by 1106 on the left in orange) and ***not*** from the four "regulated voltage" lines highlighted in blue, which are used during backup operations when there is a power failure: "The power module 1100 can be configured to selectively

provide the first voltage 1102 to the memory system 1010 ***either*** from the conversion element 1120 [blue above] ***or*** from the input 1106 [orange above]." EX1001, 28:36-39. In particular, during a power failure, "a switch 1148 [red above] can be toggled to provide the first voltage 1102 from the conversion element 1120 [blue above] ***rather than from*** the input power supply [orange above]." EX1001, 30:38-41; *see id*. at 30:14-61 ("During a first condition [normal operation], the method 1200 comprises providing the first voltage 1102 to the memory system 1010 from an input power supply 1106."). Thus, the '366 Patent discloses precisely the ***opposite*** of what the claims require ("receiv[ing] power ***only*** via the one or more of the first, second, third, and fourth regulated voltage lines"), because the '366 Patent discloses that the claimed "set of components" (including the DRAM connected to 1102) does ***not*** receive power "***only***" from the "first, second, third, and fourth regulated voltage lines" highlighted in blue above during normal operations. The components directly receive power from the input system supply (orange above) when no power failure is detected. There is no written description for "only" receiving power from the blue lines above ("one or more of the first, second, third, and fourth regulated voltage lines"), and never from the orange line above, as required by the claims.

128. Figure 17 (below) further confirms that, contrary to the claim language, power is supplied during normal operations (at step 1210 below) from

the "input power supply" (1106 to 1102 above in orange) and ***not*** from the four regulated voltage lines (1120 in blue above). *See* EX1001, 30:14-61, Fig.17. In particular, "[d]uring a first condition, the method 1200 comprises providing the first voltage 1102 to the memory system 1010 from an input power supply 1106 [orange above]…in operational block 1210 [of Figure 17 below]." EX1001, 30:21-25. It is only when there is about to be a power failure — after step 1220 in Figure 17 below — that power switches from the input power supply to the backup power supply (1120 in blue above): "The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. During the second condition….a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 [blue above] rather than from the input power supply [orange above]….[T]he trigger condition comprises a power reduction, power failure, or system hang-up." EX1001, 30:31-61. But there is no written description for using the backup power supply (via 1120 in blue above) during normal operations — let alone ***only*** using the backup power supply (and thus the four regulated voltages) at all times.

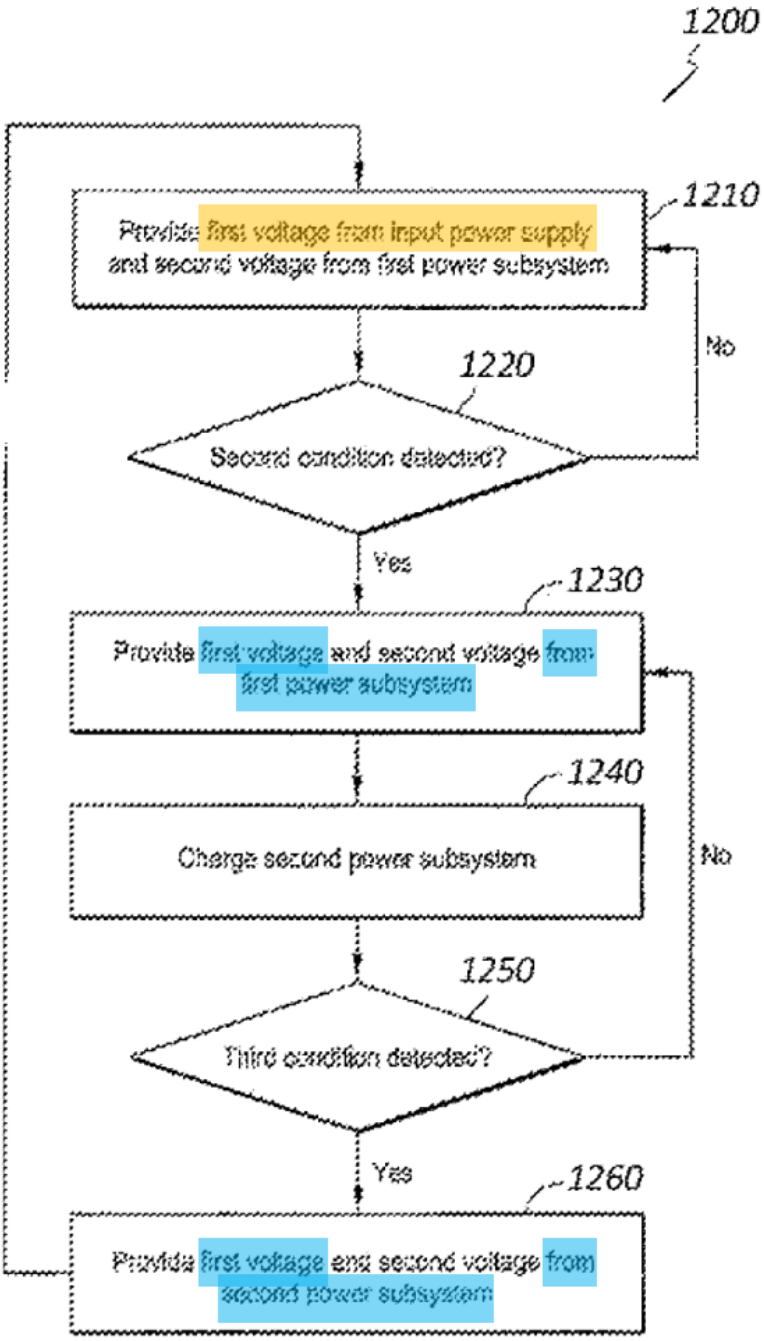


FIG. 17

129. Figure 12 (reprinted again below) also confirms that the '366 Patent does not provide written description for the claim language requiring "each

component of the set of components" to "receive[] power ***only*** via the one or more of the first, second, third, and fourth regulated voltage lines" (highlighted in blue below). As shown in the figure below, the power for the components on the memory module can be supplied from the input power supply (highlighted in orange below) via switch 1090 (in red):

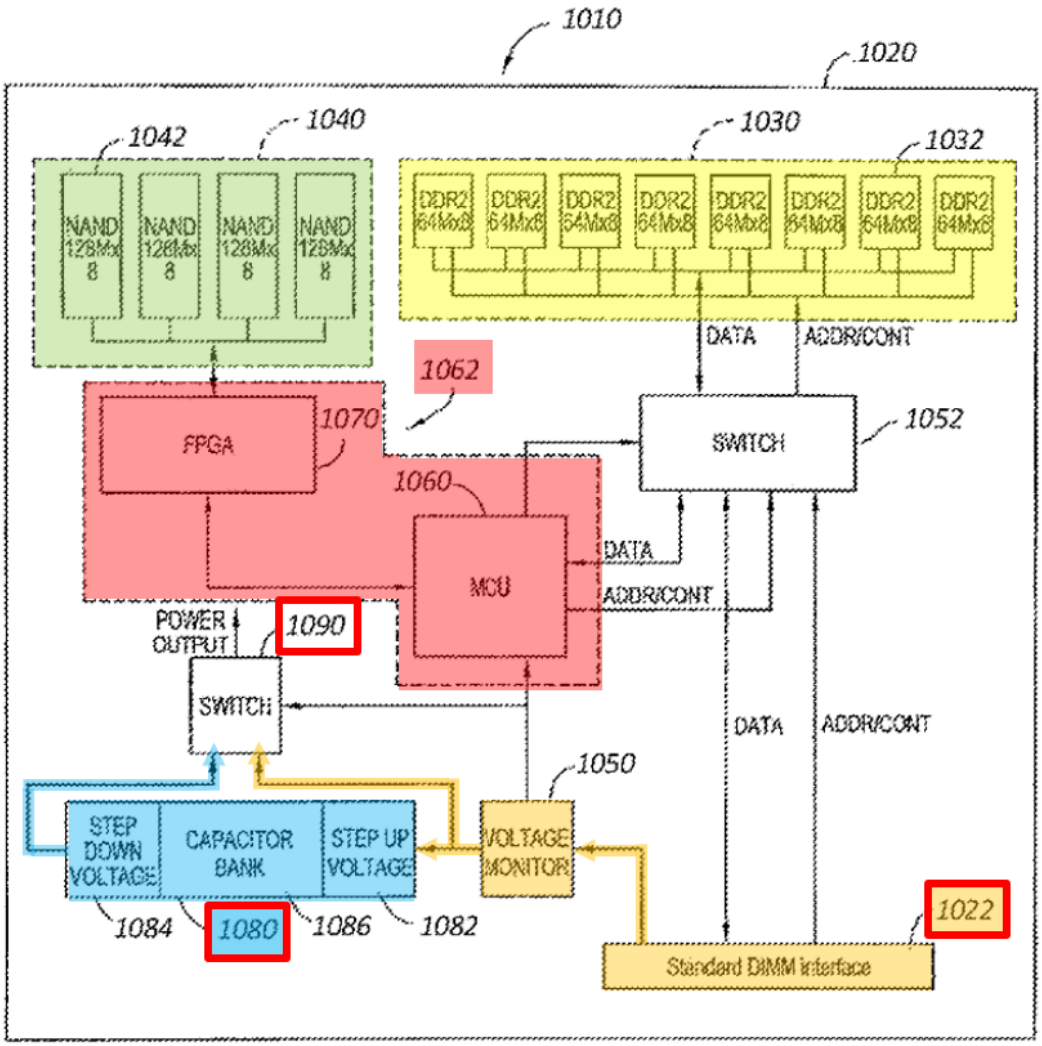


FIG. 12

In particular, the '366 Patent explains, "a switch 1090 (e.g., FET switch)…switches power provided to the controller 1062 [red], the volatile

memory subsystem 1030 [yellow], and the non-volatile memory subsystem 1040 [green], between the power from the second power supply 1080 [blue] and the power from the first power supply (e.g., system power) received via the interface 1022 [orange]." EX1001, 26:59-65. Power provided directly from the first power supply (orange above) is from the external host system, not from the internal "first, second, third, and fourth regulated voltage lines" (blue) as required by the claim language.

130. For the foregoing reasons, the '366 Patent does not provide written description for these claim limitations requiring each component to receive power only via one of the four regulated voltage lines. Furthermore, based on my understanding of the written description requirement, *supra* ¶¶47-54, Netlist cannot rely on hindsight or obviousness to pick and choose from disclosures about backup operations to try to provide written description for normal operations.

D. <u>"an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold" [13.a.1], [28.a], [34.a]</u>

131. Under at least Netlist's interpretation of the claims during prosecution, there is also no support in the specification for the requirement that "an additional trigger condition occurs when the input voltage is ***above the first*** threshold ***and***

below the second threshold." *See* limitations [13.a.1],[1] [28.a], [34.a]; *see also* limitations [1.c.6], [11], [26], [32].

132. The '366 Patent explains that "a trigger [] condition, such as…a power failure or power reduction" initiates backup operations. EX1001, 24:27-31. The patent teaches "the trigger condition occurs when…the system [input] voltage is ***below*** a certain threshold voltage [such as]…10 percent below a specified operating voltage" ***or*** "the voltage goes ***above*** a certain threshold value, such as, for example, 10 percent above a specified operating voltage." EX1001, 24:38-45; *see also id*. 24:45-47 ("[A] trigger condition occurs when the voltage goes ***below*** a threshold ***or above*** another threshold."); EX1002, 1428-29 ("'[A] threshold' can be considered…lower threshold, and 'another threshold' can be considered…upper threshold," citing EX1002, 62-63, ¶[0130] (same as EX1001, 24:45-47)). A POSITA would understand these to be exclusive conditions in this context. Thus, according to the '366 Patent, "a trigger condition" occurs when the input voltage falls ***outside*** a normal operating range defined by a lower (e.g., "10 percent below a specified operating voltage") and an upper (e.g., "10 percent above a specified

[1] The "second threshold" in claim 13 also lacks antecedent basis. *See* claims 1, 12; *cf.* limitations [11], [26], [32].

operating voltage") limit. This trigger condition is also consistent with "a power failure or power reduction," which triggers backup operations.

133. As explained below, there are three possible ways to interpret the claim language in limitations [13.a.1], [28.a], and [34.a] requiring that "an ***additional*** trigger condition occurs when the input voltage is ***above the first*** threshold ***and below the second*** threshold." In my opinion the claims are invalid for lack of written description and/or obvious under each possible interpretation,

134. ***First Interpretation***: If the "first [lower] threshold is the upper limit of a normal operating range (e.g., 13.2 volts, "10 percent above" +12 volts), above which backup operations occur, as claim 1 (which claim 13 depends from via claim 12) requires, *see* limitations [1.c.2]-[1.c.6] ("the trigger condition occurs when the input voltage ***exceeds*** a first threshold voltage"), [12], [13], then the "second [upper] threshold" must be an even higher upper limit (e.g., 15 volts), in which case the claimed "***additional*** trigger condition" would occur within the same range (e.g., between 13.2 and 15 volts in this example) as the initial "trigger condition" (e.g., above 13.2 volts in this example, *see* limitation [1.c.6]). But the '366 Patent does not provide any written description for this interpretation of the claims, where the same voltage could result in both a "trigger condition" and an "additional trigger condition."

135. ***Second Interpretation***: During prosecution, in response to an indefiniteness rejection concerning other claims, Netlist explained that the "first threshold" is a lower threshold, and the "second threshold" is an "upper threshold." EX1002, 1428-29. Thus, under Netlist's interpretation, the issued claim language in limitations [13.a.1], [28.a], [34.a] — which requires an additional trigger condition when the input voltage is "***above*** the first [***lower***] threshold ***and below*** the second [***upper***] threshold" — would define a certain voltage range, and the "additional trigger condition" would "occur[] when the input voltage" falls ***within*** that range. As explained above, however, *supra* ¶ 132, the '366 Patent does ***not*** disclose any range ***within*** which a "trigger condition" occurs. *Id*. The specification only discloses a "trigger condition" occurring when the input voltage goes ***outside*** a normal operating range, e.g., when the system power fails, and a backup operation kicks in. Thus, under Netlist's interpretation, limitations [13.a.1], [28.a], and [34.a] lack written description. Furthermore, under this Second Interpretation, the claims are also obvious as discussed below. *Infra* ¶224.

136. ***Third Interpretation***: Finally, if not bound by Netlist's interpretation and if the "first threshold" can be higher than the "second threshold," then the limitation may be interpreted consistent with the specification of the '366 Patent. Namely, "an additional trigger condition" occurs in response to ***both*** overvoltage ("when the input voltage is above the first threshold [the upper limit of a normal

operating range]") ***and*** undervoltage ("when the input voltage is…below the second threshold [the lower limit]") — i.e., upon detecting the input voltage going ***outside*** that normal range. Under this Third Interpretation, while the claims may have written description, they are still obvious as discussed below. *Infra* ¶225.

V. OVERVIEW OF THE PRIOR ART

A. U.S. Patent No. 7,363,422 to Perego *et al*. ("Perego") (EX1035)

137. U.S. Patent Application No. 10/766,131 by Perego *et al*. ("Perego"), titled "Configurable Width Buffered Module," was filed on January 28, 2004, and was published as U.S. Patent Pub. No. 2004/0186956 on September 23, 2004. EX1035 (Perego), 1. Perego issued as U.S. Patent No. 7,363,422 on April 22, 2008. *Id*. Perego was not cited or discussed during prosecution of the '366 Patent, *see* EX1002, and as explained below, Perego discloses features similar to those found in the DDR5 standard that the Examiner erroneously believed distinguished the claims of the '366 Patent from the prior art, *supra* ¶¶ 106, 109.

138. Because Perego was filed and published more than one year before the earliest claimed priority date of the '366 Patent (June 1, 2007), I understand that Perego is prior art to the '366 Patent under at least 35 U.S.C. § 102(a), (b), and (e) (pre-AIA). Alternatively, because the claims of the '366 Patent lack written description and are not entitled to claim priority before the application for the '366 Patent was filed on January 24, 2022, as explained above, *see supra* ¶¶115-136, I

understand that Perego, filed and published before that date, is also prior art to the '366 Patent under 35 U.S.C. § 102(a)(1) and (2) (post-AIA).

139. Similar to the DDR5 standard discussed above, *see supra* ¶116, Perego discloses a memory module (below) where "two channels 415c and 415d" may "transfer information simultaneously," such as 32 bits from the 4 memory devices in channel 415c, and 40 bits from the 5 memory devices (including ECC) in channel 415d:

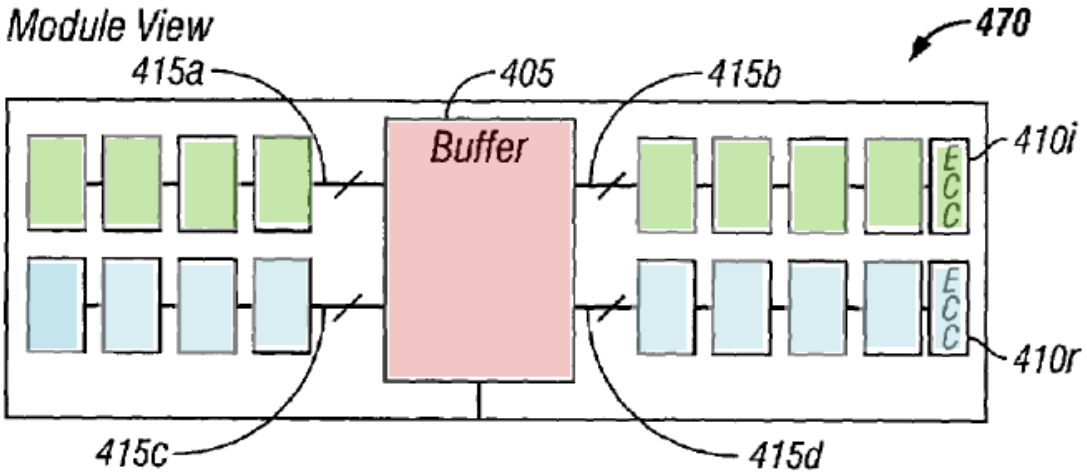


FIG. 4C

EX1035 at 21:16-20, Fig.4C; *see also id.* at 10:54-59 (disclosing DDR memory devices, which can be 8-bits wide, *see* EX1026 at 2 ("x8")); EX1090 at 28-32 (Final Written Decision finding Perego compatible with JEDEC standards); EX1091 at 32-37 (same).

140. Perego discloses a memory module, e.g., 340, that includes a buffer device 350 (red below), an edge connector 390, and multiple groups of memory

devices 360 (green and blue). EX1035 (Perego), Fig. 3B (below, annotated). The edge connector of such memory modules 330a-330c can fit into sockets 380a-380n on a common substrate (not shown) that also includes a memory controller 310. *Id*., 5:56-6:11.

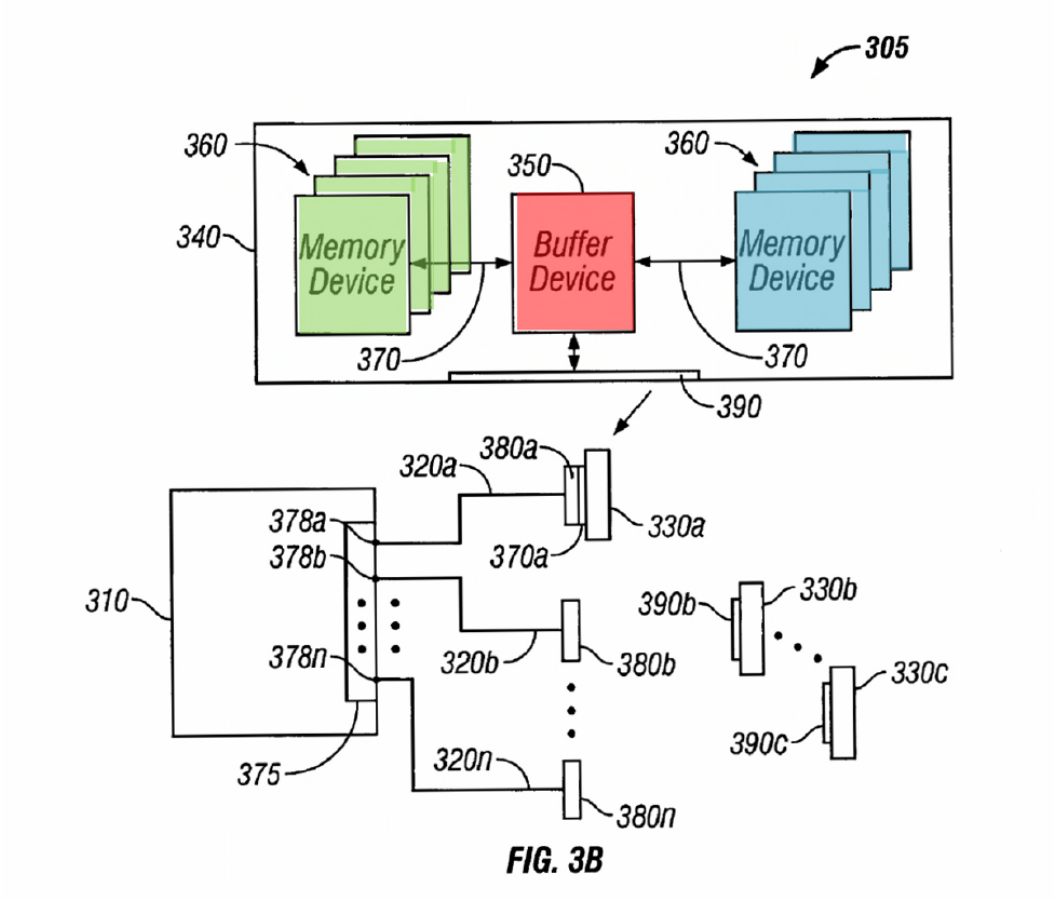


FIG. 3B

141. Perego's "[b]uffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be

phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices." *Id*., 6:34-43.

142. To achieve this flexibility, Perego's buffer device (red) includes programmable interfaces, e.g., 520a and 520b, which can accommodate different number and types of memory devices. EX1035 (Perego), Fig. 5B (below, annotated), 13:60-14:15.

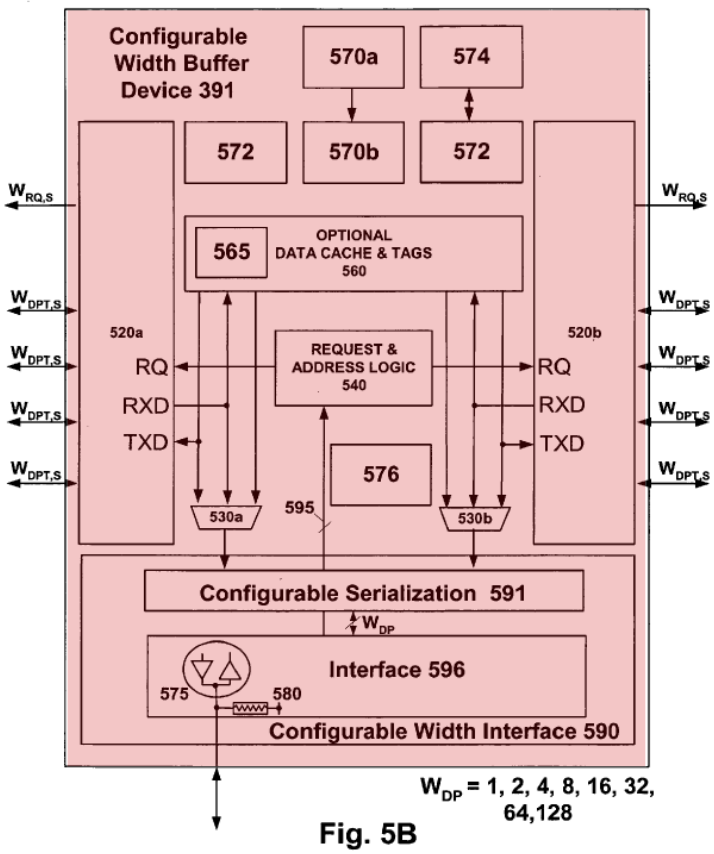


Fig. 5B

For example, Perego's buffer may "translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation," such as

SDRAM or DDR2 memory devices, thus "render[ing] the type of memory device transparent to the system." *Id*., 10:54-67.

B. U.S. Patent Publication No. 2006/0174140 by Harris *et al*. ("Harris") (EX1023)

143. U.S. Patent Application No. 11/047,304 by Harris *et al*. ("Harris"), titled "Voltage Distribution System and Method for a Memory Assembly," was filed on January 31, 2005, and was published as U.S. Patent Pub. No. 2006/0174140 on August 3, 2006. EX1023 (Harris), 1. Harris was one of the references used by the Board to invalidate the related '054 and '918 Patents. *See supra* ¶87. During prosecution of the '366 Patent, Harris was discussed by the applicant, but the Examiner disagreed with the applicant's arguments about Harris, and the Examiner did not specifically distinguish Harris in the reasoning for allowance. *See supra* ¶¶ 95-109.

144. Because Harris was filed and published before the earliest claimed priority date of the '366 Patent (June 1, 2007), I understand that Harris is prior art to the '366 Patent under at least 35 U.S.C. § 102(a) and (e) (pre-AIA). Alternatively, because the claims of the '366 Patent lack written description and are not entitled to claim priority before the application for the '366 Patent was filed on January 24, 2022, as explained above, *see supra* ¶¶115-136, I understand that Harris, filed and published before that date, is also prior art to the '366 Patent under 35 U.S.C. § 102(a)(1) and (2) (post-AIA).

145. Harris is "directed to a voltage distribution system for a memory board." EX1023, ¶[0003]. Harris explains that "industry standard memory modules, e.g., Dual In-line Memory Modules (DIMMS) populated with dynamic random access memory (DRAM) devices, are provided with power supply rails (on a relatively large number of pins) that are powered from system board or main board voltage sources, and are specific to the memory technology. … Furthermore, each generation of DIMM/DRAM technology requires a different power supply which keeps getting lower (e.g., 3.3V, 2.5V, 1.8V, 1.5V and beyond), thereby making it difficult to mix memory technologies on a system board, or provide upgrades to next generation DRAM technology in a cost-effective manner." *Id*., ¶[0002].

146. To deal with the different voltage requirements of different memory technologies, Harris discloses a memory module, e.g., 100A, that includes an on-board voltage regulator module 102 to convert an externally supplied voltage 104 to "appropriate local voltage levels" on the module. EX1023 (Harris), Fig. 1A (below), ¶¶[0009-10].

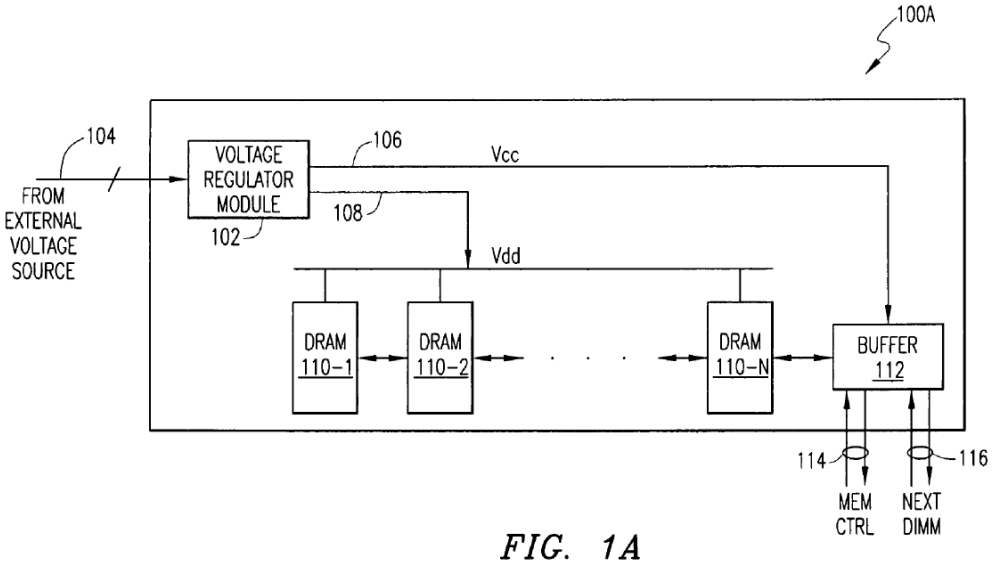


FIG. 1A

In particular, voltages on Vdd path 108 "depend[] on the type, functionality, and design of the memory devices" 110-1 to 110-N, and voltages on Vcc path 106 "depend[] on the buffer and DIMM technology." *Id*. "Since the Vdd and Vcc power supply rails are rendered independent from external voltage sources, the overall power supply interface to the memory module 100A is improved to better support large memory capacity scaling, hot-pluggability, DRAM technology independence (e.g., DDR2, DDR3, DDR4, and other DRAM types), high DRAM device count (i.e., amenable to multi-ranking), as well as provide improved system-level cost sharing." *Id*., ¶[0011].

C. U.S. Patent No. 7,724,604 to Amidi *et al*. ("Amidi") (EX1024)

147. U.S. Patent Application No. 11/552,949 by Amidi *et al*. ("Amidi"), titled "Clock and Power Fault Detection for Memory Modules," was filed on October 25, 2006, and was published as U.S. Patent Pub. No. 2008/0101147 on

May 1, 2008. EX1024 (Amidi), 1. Amidi issued as U.S. Patent No. 7,724,604 on May 25, 2010. *Id*. Amidi was one of the references used by the Board to invalidate the related '054 and '918 Patents. *See supra* ¶87. During prosecution of the '366 Patent, Amidi was discussed by the applicant, but the Examiner disagreed with the applicant's arguments about Amidi, and the Examiner did not specifically distinguish Amidi in the reasoning for allowance. *See supra* ¶¶ 95-109.

148. Because Amidi was filed before the earliest claimed priority date of the '366 Patent (June 1, 2007), I understand that Amidi is prior art to the '366 Patent under at least 35 U.S.C. § 102(e) (pre-AIA). Alternatively, because the claims of the '366 Patent lack written description and are not entitled to claim priority before the application for the '366 Patent was filed on January 24, 2022, as explained above, *see supra* ¶¶122-137, I understand that Amidi, filed and published before that date, is also prior art to the '366 Patent under 35 U.S.C. § 102(a)(1) and (2) (post-AIA).

149. Amidi is directed to a memory module with a "power fault detection" functionality. EX1024 (Amidi), Abstract. Amidi explains that computer systems operate in part using volatile memory, which requires periodic refresh and loses data when power is not supplied. *Id*. at 1:6-18. Nonetheless, data is often stored in volatile memory for fast access, even irreplaceable data in mission critical systems. *Id*., 1:19-27. Amidi further explains that system information for failure analysis

and for restarting the system would also be useful after a power failure. *Id*. Thus, a Skilled Artisan would have understood at the time that there was a need to keep data in volatile memory for short or medium-term time periods even when the surrounding system loses power. *Id*., 1:28-35.

150. To avoid loss of critical data and important system information stored in volatile memory in the event of a power fault of the surrounding system, Amidi teaches a memory module that includes a power management block 510 to monitor the system supply voltage 520 and to switch to a battery supply 530 "to ensure a stable power supply even in the face of disruptions in system supply." EX1024 (Amidi), 4:14-23, Fig. 5 (below), *see also id*., Fig. 14, 8:23-36.

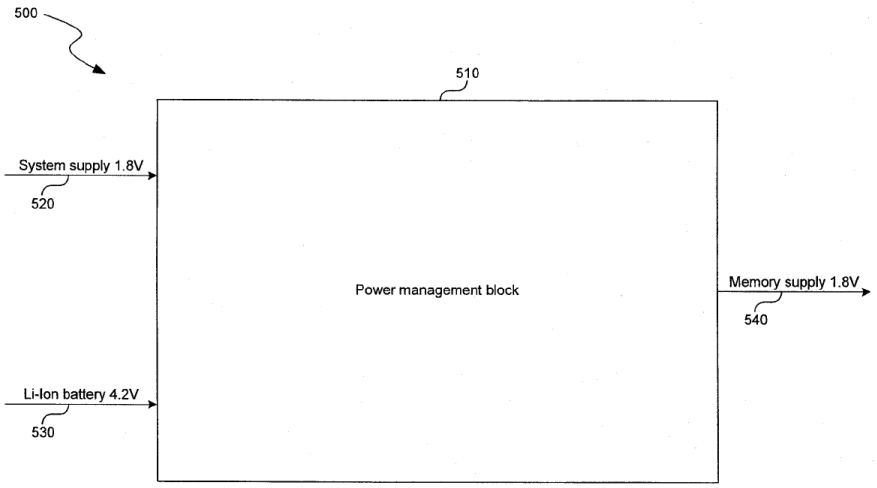


FIG. 5

151. Amidi teaches that its power management technique can be implemented by using well-known components, such as boost, buck, and

boost/buck DC/DC converters (610, 640, and 680/690, blue) as illustrated in Fig. 6. *Id*., Fig. 6 (below, annotated), 4:23-55.

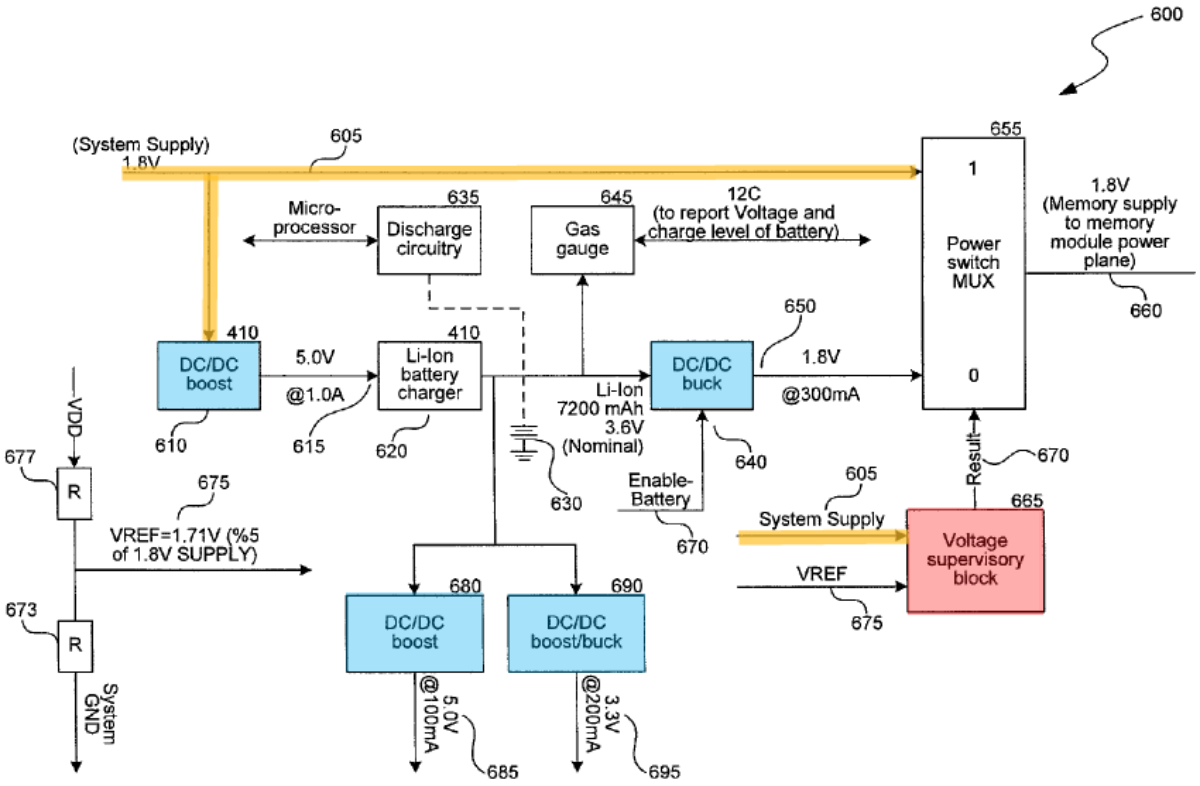


FIG. 6

In this implementation, a boost converter 610 and a Li-ion battery charger 620 use the system supply power 605 (orange) to charge a Li-ion battery 630. *Id*. A voltage supervisory block 665 (red) monitors the system supply voltage and controls a power switch 655 to select the system supply 605 or the battery power 650 for the memory module power plane. *Id*. Amidi teaches that its power management technique can be implemented on a memory card. *Id*., Figs. 3, 4 (below).

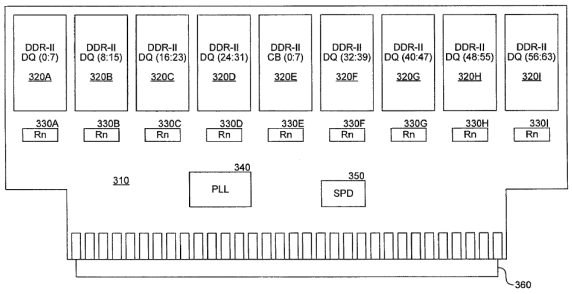


FIG. 3

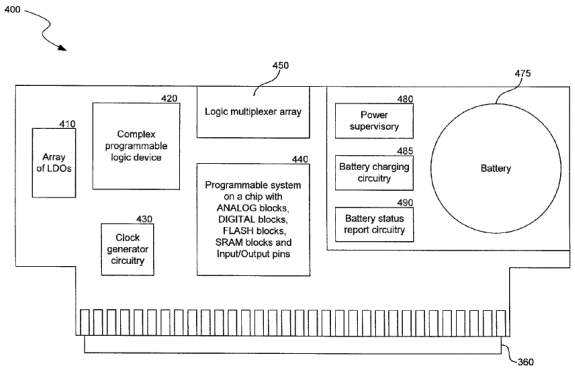


FIG. 4

VI. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE '366 PATENT

152. My analysis below is based on my understanding of the law and other information discussed above.

A. Ground 2 combination: Perego (EX1035) and Harris (EX1023) further in view of Amidi (EX1024)

153. A Skilled Artisan would have been motivated to combine the teachings of Perego and Harris and had a reasonable expectation of success in doing so as discussed below. In the combination, Harris's power distribution techniques power the components in Perego's memory module, including the memory devices 360 and the buffer 391, as schematically illustrated below in Figure 3C of Perego as modified to illustrate the combination:

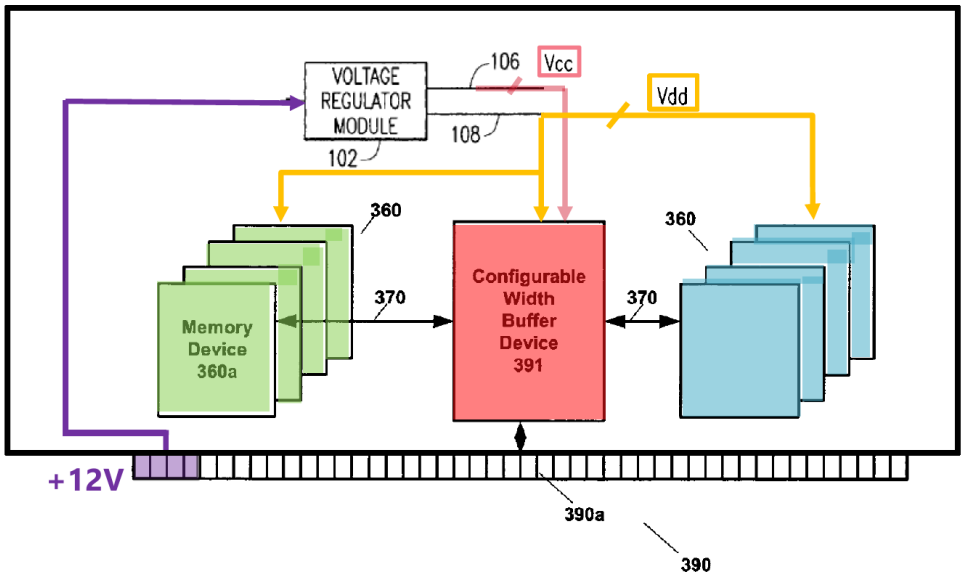


Fig. 3C

In the combination, Perego's memory module includes the functionality of Harris's voltage regulator module 102 receiving a 12V power supply (purple) from which it provides the required voltages Vdd (orange) to the memory devices 360 and voltages Vcc (pink) to the buffer device 391.

154. Perego and Harris are analogous art to the '366 Patent, each being directed to memory modules and memory systems, and pertinent to the problem of allowing the use of different types of memory devices in a memory system, including techniques to power these devices. EX1001 (the '366 Patent), 2:6-9 ("The present disclosure relates generally to computer memory devices, and more particularly, to devices that employ different types of memory devices."), 20:56-60 ("[A] power module…provides power to the various components of the memory

system from different sources based on a state of the memory system."); EX1035 (Perego), 1:12-17 ("This invention relates to memory systems, memory subsystems, memory modules or a system having memory devices."), 10:54-67 ("Different types of memory devices may be included on different modules within a memory system."), 20:41-47 ("[S]ubsets of available memory devices…are…powered-on during various modes of operation…to achieve power savings."); EX1023 (Harris), ¶¶[0003] ("One embodiment is directed to a voltage distribution system for a memory board assembly."), [0020] ("Because voltage-independent embodiments disclosed herein can provide upgradeability and extensibility without changing system board power distribution, transitioning to newer DRAM technologies (e.g., at lower operating voltages) is more cost-effective as well as simpler to implement.").

155. Perego teaches a memory module including a "buffer device…for flexible system configurations, and several performance benefits." EX1035 (Perego), 3:23-25. Perego's buffer device is "isolating data, control, and address signals of the memory devices from the connector interface." *Id*., 4:38-42, 6:12-15. Thus, Perego's buffer device can "render the type of memory device transparent to the system," and "translate protocols employed by [the system's memory] controller…to the protocol utilized in a particular memory device implementation," so that "[d]ifferent types of memory devices may be included on

different modules within a memory system." *Id*., 10:59-67. Perego specifically mentions DDR2 and SDRAM devices as exemplary memory types, *id*., 10:56-59, and teaches that its techniques can be applied to newer generations of memory devices and controllers, *id*, 6:34-43 ("Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in. … Backward compatibility…may also be preserved. Similarly, new generations of controllers may be phased in.").

156. A Skilled Artisan would have understood at the time that allowing the use of different types and generations of memory and buffer devices on Perego's module required different power supplies. Harris teaches that "each generation of DIMM/DRAM technology requires a different power supply which keeps getting lower (e.g., 3.3V, 2.5V, 1.8V, 1.5V and beyond), thereby making it difficult to mix memory technologies on a system board, or provide upgrades to next generation DRAM technology in a cost-effective manner." EX1023 (Harris), ¶[0002]. Harris solves these generational power-supply problems by a "voltage distribution system for a memory board assembly," which is "locally converting the voltage by an on-board voltage regulator module to generate appropriate local voltage levels for powering…memory devices of the memory board assembly." *Id*., ¶[0003]. Therefore, a Skilled Artisan would have been motivated to implement Harris's "voltage distribution" functionality in Perego's memory systems in order to

provide a simple, cost effective, and advantageous power supply to Perego's modules.

157. For example, Harris teaches that its "voltage-independent embodiments disclosed herein can provide upgradeability and extensibility without changing system board power distribution," and allows "transitioning to newer DRAM technologies (e.g., at lower operating voltages)." EX1023 (Harris), ¶[0020]. Harris further teaches that its techniques are "more cost-effective as well as simpler to implement" than other approaches. *Id*. By using Harris's "local voltage supply for on-board power requirements, a number of advantages may be obtained," including that "the overall power supply interface to the memory module…is improved to better support large memory capacity scaling, hot-pluggability, DRAM technology independence (e.g., DDR2, DDR3, DDR4 and other DRAM types), high DRAM device count (i.e., amenable to multi-ranking), as well as provide improved system level cost sharing. Additionally, memory performance is also improved because of tighter voltage regulation." *Id*., ¶[0011].

158. Harris further teaches that, by using its "technology-independent voltage distribution scheme…, power supply design's complexity as well as the cost of memory-specific power distribution are reduced. Cost savings may include, for example, elimination of system-board-specific power supply or regulator output, associated bypass capacitor arrangements, heavy etch or power planes.

Also, under the technology-independent voltage distribution scheme disclosed herein, cost of memory power regulation scales with populated memory devices, rather than being pre-provisioned for maximum memory capacity as is typically the case in existing systems. Additionally, one or more of the following advantages may be realized in an exemplary voltage distribution embodiment: provision of tighter, lower inductance regulation which decreases voltage variability and increases timing margins; reduction in the pin count on DIMM connector to system board or memory riser card (whereby a smaller connector or wider pin spacing may be accommodated); improved signal integrity due to reduced crosstalk on the same size connector; and reservation of extra pins for implementing additional standard or proprietary functions." EX1023 (Harris), ¶[0019].

159. Realizing any one or more of the advantages and benefits taught by Harris would have further motivated a Skilled Artisan to implement Harris's power distribution teachings in Perego's memory system.

160. Such a combination would have been well within the level of skill at the time as evidenced by the teaching of Perego and Harris and the knowledge of a Skilled Artisan. For example, Harris teaches that "Dual In-line Memory Modules (DIMMS)…are provided with power supply rails…that are powered from system board or main board voltage sources." EX1023 (Harris), ¶[0002]. Harris further teaches that its "embodiments are amenable to dual +12V power supply rail

implementations." *Id.*, ¶[0020]. A Skilled Artisan would have understood that such "+12V power supply rail implementations" were provided on commercially available motherboards at the time. EX1085 (ATX12V Power Supply Design Guide), 8 ("power supplies…for motherboards") ("ATX12V power supplies should be designed to accommodate…increased +12 VDC currents."), 13 (Table 2, DC Output Voltage Regulation including two 12V outputs).

161. Converting the 12V power supply locally to the voltages required on a specific module was also well known. For example, buck converters converting a 12V power supply to a voltage "from about 0.5V to 3.5V or more" were commercially available at the time. *See e.g.*, EX1023 (Harris), ¶[0009]; EX1062 (Analog Dialogue), 15; EX1078 (ADP1821), 1; EX1048 (MPD4S014S), 1. Voltage converters designed specifically to provide voltages (V_{DDQ} and V_{TT}) to operate DDR memories were also commercially available. *See e.g.*, EX1041 (FAN5026), 1. Thus, a Skilled Artisan would have known how to implement the combination, where Perego's memory module receives 12V power supply from the motherboard as it was known at the time, and Harris's on-board voltage regulator module uses known buck converters to provide the appropriate voltage levels that are required on the module.

162. As discussed above, it would have been obvious to a Skilled Artisan to combine the teaching of Perego and Harris in order to generate appropriate

voltages for the components of Perego's module on the module itself from a 12V system supply as taught by Harris. *Supra* ¶¶153-161. A Skilled Artisan would have also been motivated to use Amidi's power monitoring and backup techniques in a memory module according to the combination of Perego and Harris in order to provide power to the memory module during a system power fault and avoid data loss, as schematically illustrated below in annotated Figure 3C of Perego (functionalities from Amidi's teaching are indicated by light blue):

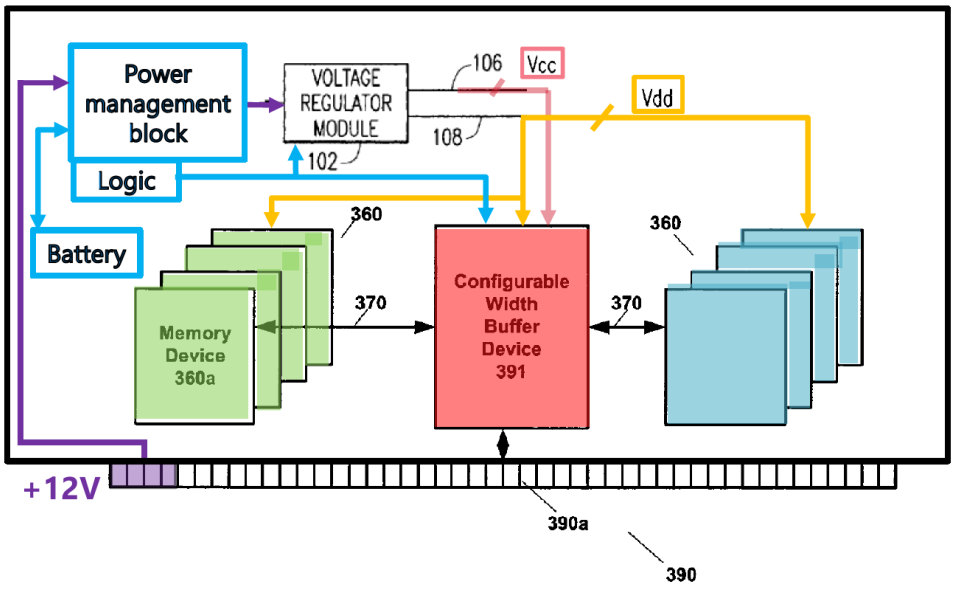


Fig. 3C

In the combination, Amidi's Logic and Power management functionalities (light blue) are configured to detect faults in Harris's +12V system power (purple) and, in case of a fault, switch to on-board battery power and put the memory devices 360 into self-refresh mode to save battery power while preserving their data.

163. In prior Final Written Decisions involving the '054 parent and '918 grandparent patents (which have the same specification), the Board already found that a Skilled Artisan would have been motivated to combine Harris and Amidi with a reasonable expectation of success and rejected Netlist's arguments to the contrary. EX1070 (FWD for '918 Patent), 72-75; EX1071 (FWD for '054 Patent), 56-60. For example, Netlist argued that "Harris provides alternate voltage sources … [which is] a solution for the alleged problem that Amidi addresses." EX1070, 74. The Board, however, found that "Amidi provides power supply on the memory module that is independent from the host, and that a person of ordinary skill in the art would have seen the value of adding a redundant power supply onboard Harris's memory module at least for some practical applications." *Id*., 74-75 (citing EX1024 (Amidi), 1:28-35, 2:6-26). The Board also found that "memory modules with battery backup were known in the art and readily available." *Id*., 75. Netlist also argued that "substituting Amidi's battery backup solution for Harris's redundant power sources would require substantial space," *id*., 74, but the Board agreed that "even if the battery backup occupies one side of an FBDIMM board, the other side still can include one rank or two ranks using stacked memory devices," *id*., 75. I agree with the Board's conclusion (which relied on my prior testimony) for the reasons discussed below.

164. Amidi, like Perego and Harris, is analogous art to the '366 Patent, each being directed to memory modules and memory systems, and pertinent to the problem of allowing the use of different types of memory devices, including techniques to power these devices. *Supra* ¶154; EX1024 (Amidi), Abstract ("…power fault detection for a memory module is provided…"), 2:11-26 ("Clock and power fault detection for a memory module may be provided in a variety of ways. … Providing such a system and process within a memory module can be very helpful, as it avoids the need for system circuitry … which can maintain a memory module from outside the memory module. Moreover, such a system and process may be tuned to the specific memory module, instead of requiring the overhead to deal with many different types of memory modules, for example.").

165. A Skilled Artisan would have been motivated to implement Amidi's power monitoring and backup techniques in a memory module of the Perego-Harris combination and had a reasonable expectation of success in doing so. For example, Amidi teaches that "it may be useful to provide an option for keeping data in volatile memory even when a surrounding system loses power." EX1024 (Amidi), 1:28-30. The data in the volatile memory may be "irreplaceable," or "useful for restarting a system after a failure" or for "failure analysis." *Id*., 1:19-27. Harris also recognizes the importance of reliable power and proposes a "redundant" power source. EX1023 (Harris), ¶¶[0012-14], [0016], Figs. 1B, 2.

Amidi teaches that power fault detection and supplying backup power "within a memory module can be very helpful, as it avoids the need for system circuitry … which can maintain a memory module from outside the memory module. Moreover, such a system and process may be tuned to the specific memory module, instead of requiring the overhead to deal with many different types of memory modules, for example." EX1024 (Amidi), 2:11-26. Thus, a Skilled Artisan would have been motivated to implement Amidi's teaching of power-fault detection and redundant power source on the memory module itself for maintaining data during a power disruption. *Id.*, Abstract, 1:28-35, 2:6-26, 4:14-60, Figs. 4-6.

166. Such a combination would have been well within the level of skill at the time as evidenced by the teaching of Amidi and Harris and the knowledge of a Skilled Artisan. For example, the "power management block" of Amidi could be modified easily to work with the memory module of Perego-Harris combination, as shown in the annotated version of Figure 5 of Amidi below:

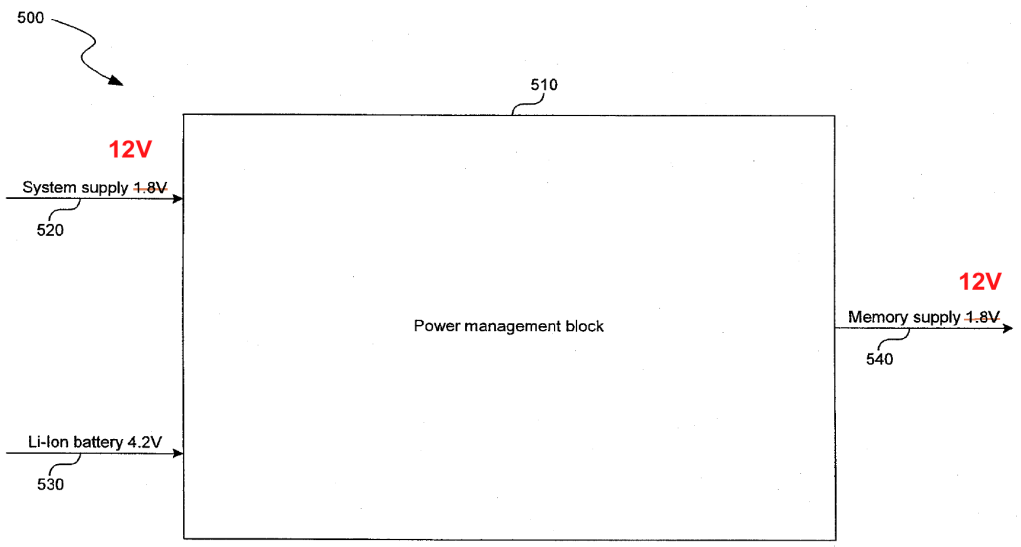


FIG. 5

EX1024 (Amidi) at Fig.5 (annotated with teachings of Harris). Harris teaches using a 12V supply voltage, EX1023 (Harris), ¶[0012], thus it would have been obvious to a Skilled Artisan that, in a combination with Harris, Amidi's power management block also uses the 12-volt supply voltage as the system supply (520, above left). A Skilled Artisan would have also understood that Harris's 12-volt supply can be stepped-down with a buck converter (instead of using Amidi's boost converter 610) to a 5-volt supply which can be used by Amidi's lithium-ion battery charger 620 to charge the Li-ion battery 630 from the 12-volt system power. EX1024 (Amidi), Fig. 6 (below), 4:25-27 ("FIG. 6 illustrates an embodiment of the internals of a power management block.").

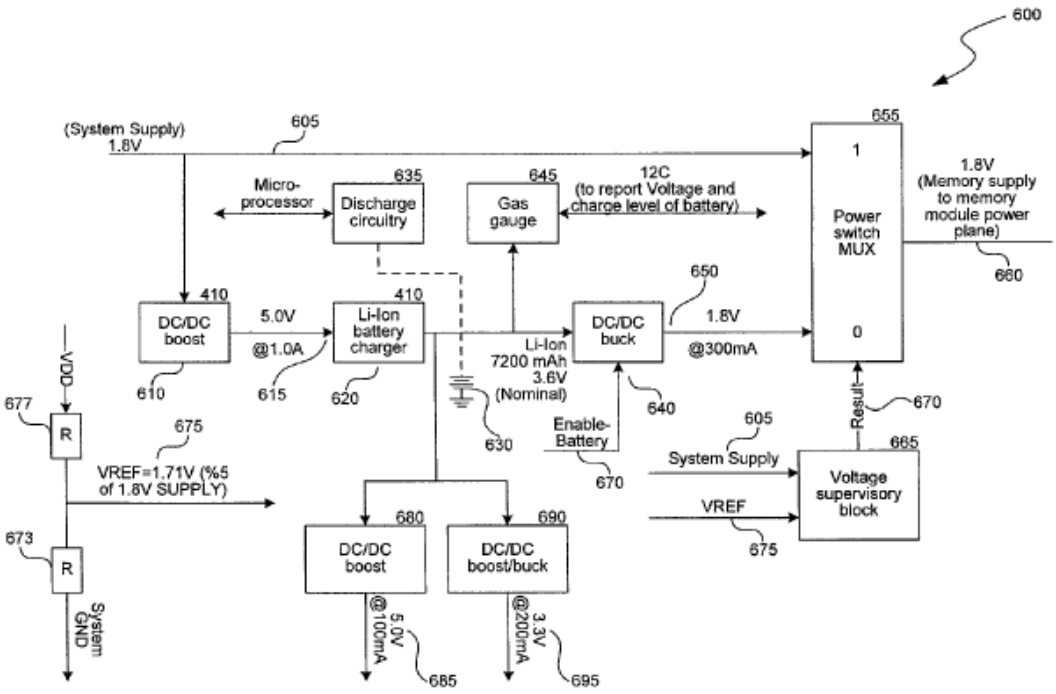


FIG. 6

167. Similarly, a Skilled Artisan would have understood that Amidi's battery voltage can be stepped-up with a boost converter (instead of using a buck converter 640) to the 12-volt level used by Harris's memory module (via 660 in Fig. 6 and 540 in Fig. 5 above). Indeed, Amidi expressly discloses that his "power management block" (Fig. 5 above) uses "buck" converters to step-down voltages as needed, *see, e.g.*, EX1024 (Amidi), 4:38-40 & Fig. 6 (640 "buck"), and "boost" converters to step-up voltages as needed, *id.*, 4:27-32 & Fig. 6 (610 "boost"). Boost converters and buck converters were well-known and widely used at the time and had long been taught in textbooks. *See, e.g.*, *supra* ¶¶66-70; EX1058

(Lenk), 3-5 (switching converter circuits include, "buck," "boost," and "buck-boost" converters); EX1032 (Mohan), 161 (similar).

168. A Skilled Artisan would have also understood how to control the volatile memory devices and have them perform self-refresh operations to maintain their data while saving power in the combination. For example, Amidi discloses that "one may provide a process which operates to … maintain memory (through refresh, for example)." EX1024 (Amidi), 2:16-19, 6:40-52 ("State machine 1100 may be used to refresh SDRAM of a memory module … without benefit of other parts of a system."), Figs. 11, 13 (control of self-refresh operations). Such self-refresh operations to save power while keeping the stored data were available on standard memory devices at the time. *See, e.g.*, EX1026 (JESD79-2B), 39-40 ("The Self Refresh command can be used to retain data in the DDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR2 SDRAM retains data without external clocking."); EX1046 (JESD79-3A), 70-71 (similar for DDR3 memories).

169. Furthermore, a Skilled Artisan would have understood that Amidi's battery backup mode is similar to the well-known S3 power-saving mode in memory modules, such as FBDIMMs. *See, e.g.*, EX1027 (JESD82-20), 39 ("S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode."). Amidi, like the S3 mode, puts the DRAMs in a

self-refresh state to preserve data while saving battery power in order to extend the time while the data is preserved without external power. EX1024 (Amidi), 6:40-52. Accordingly, a Skilled Artisan would have been motivated to follow relevant, known S3 power saving techniques when implementing Amidi's techniques in the module of Perego and Harris. For example, "in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low [i.e., they are not used]… 1.8V supply is on [i.e., for VDD to the DRAMs]. 1.5V [i.e., for VCC/VCCFBD to the input-output of the Buffer], Vtt [i.e., VTT for DRAM Interface termination] and 3.3V [i.e., for VDDSPD to SPD] are off. DRAMs are in self refresh [i.e., still powered on with VDD], and the CKE signals must be driven low." EX1027 (JESD82-20), 21; EX1028 (JESD205), 9 ("Supply voltages" including VDD, VCC/VCCFBD, VTT, and VDDSPD).

170. Thus, a Skilled Artisan would have been motivated to implement the memory module of the Perego-Harris combination with the functionality of Amidi's power management and logic for detecting power faults and switching over to battery backup when needed. This straightforward modification of the memory module of the Perego-Harris combination in view of the teaching of Amidi and the knowledge of a Skilled Artisan simply uses a known technique (e.g., Amidi's battery backup techniques) to improve a similar device (e.g., the

memory module of the Perego-Harris combination) in the same way (e.g., to provide a backup power supply using a battery). In addition, the combination merely applies a known technique (e.g., providing a backup power supply) to a known device (e.g., a memory module) that is ready for improvement to yield predictable results (e.g., redundancy when the system supply or clock fails).

B. Claims 1-38 Are Unpatentable Over Ground 2

171. In my opinion, claims 1-38 of the '366 Patent are obvious in light of Ground 2. I have compared each and every limitation in claims 1-38 to Ground 2 and I have prepared a claim chart showing why each and every limitation is obvious in light of Ground 2. *See* EX1113. In the paragraphs below, I focus on providing context and technical explanations related to specific limitations.

1. [1.a.2] Conduits

172. Ground 2 discloses "*the memory slot connector* [e.g., "mating connectors 380a-380n"] *including a set of power conduits* [e.g., receiving power supplies from the system], *a set of data conduits* [e.g., interfacing "DQ" data signals], *and a set of address and control conduits* [e.g., interfacing "RQ" address/control signals]." EX1035, Fig.4B (below, annotated).

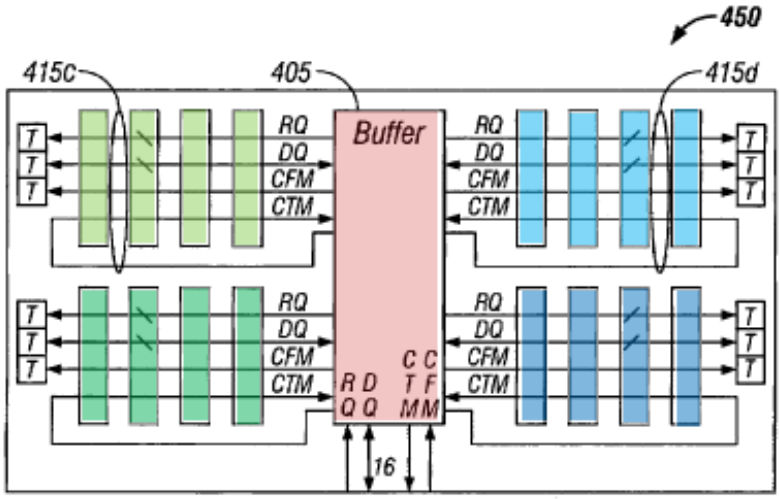


FIG. 4B

173. As shown in Fig. 4B above, Perego discloses that channels (415) on the module "include control lines (RQ), [and] data lines (DQ)." EX1035, 9:43-45. "[C]ontrol lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines." *Id.*, 9:58-60. The "row address strobe" and "column address strobe" lines are standard JEDEC control lines abbreviated as "RAS" and "CAS," respectively. EX1026 (JESD79-2B), p.6 ("Command Inputs: RAS, CAS and WE (along with CS) define the command entered."); EX1107 (Jacob paper), p.4 ("DRAM's RAS pin (row address strobe) … DRAM's CAS pin (column address strobe)"); EX1090 at 24-32 (finding Perego compatible with JEDEC standards); EX1091 at 28-37 (same). Perego's memory module receives the DQ data signals and RQ address/control signals from the system controller via "edge connectors" 390, which fit into corresponding memory slot connectors 380. EX1035, Figs. 3C (below), 4 (above showing the

buffer 405 having "RQ" and "DQ" ports leading to the edge of the module), 13:13-17 ("to provide electrical connections between interface 596 [in the buffer 405] and connector 390 (FIG. 3C)")."

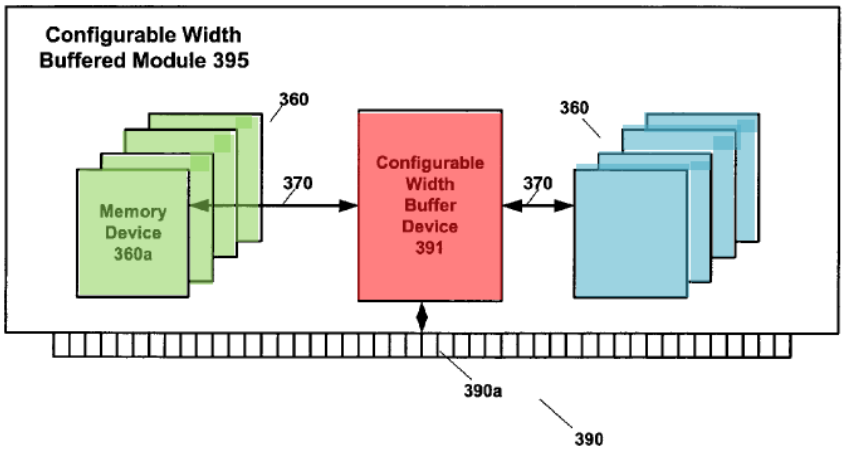


Fig. 3C

174. Similarly, Harris and Amidi disclose edge connectors by which the memory module communicates data and address/control signals with the system controller, as was common at the time for DIMMs. EX1023, ¶¶[0013] ("compatible with … (JEDEC) standards"), [0009] ("buffer/logic component 112 … buffering command/address (C/A) … as well as data"), Fig.3 (showing the buffer 112 receiving data and address/control signals via edge connectors); EX1024, Figs. 3, 4, 3:58-62 ("a set of printed conductors on an edge"), 4:1-2 ("Card interface 360 is present on this side as well, providing connectivity."); EX1108 (Dell), Figs.1-4. Edge connector pins for data signals and those for address/control signals were commonly separate from one another, consistent with

the JEDEC standards at the time. *See, e.g.*, EX1108 (Dell), Fig.3 (showing "168 PIN SDRAM DIMM" including separate data (DQ0-DQ79) and control/address (A0-A13, CS0-CS4, etc.) pins).

175. Perego also discloses that the DQ data lines and RQ control lines on the memory module—which deliver data signals and control/address signals received from the edge connectors 390—"may equally apply" to links 320 between the memory module and the system controller. EX1035, 9:43-49 ("Signal lines of channels 415a and 415b include control lines (RQ), data lines (DQ) and clock lines (CFM, CTM). The varieties of interconnect topologies, interconnect types, clocking methods, signaling references, signaling methods, and signaling apparatus described above in reference to point-to-point links 320a–320n may equally apply to channels 415a and 415b."). Perego further discloses that "mating connectors 380a-380n interface with [edge] connectors 390" for the module to communicate with the system controller. *Id*., 6:1-11; *see also* EX1024, 3:58-62 ("a set of printed conductors on an edge … mat[ing] with a slot or socket … to which memory module 300 is connected"). Thus, the "mating connectors 380a-380n" ("*memory slot connector*") include "*a set of data conduits*" electrically coupled with the data edge connectors to interface data and "*a set of address and control conduits*" electrically coupled with the address/control edge connector pins to interface address/control signals.

176. Ground 2 further discloses that the "mating connectors 380a-380n" also includes "*a set of power conduits*" to interface with power supplies from the system. For example, Perego's edge connectors 390 on the memory module include power connectors to receive power supplies from the system through "mating connectors 380a-380n." *See* EX1035, FIG. 3B (below, annotated).

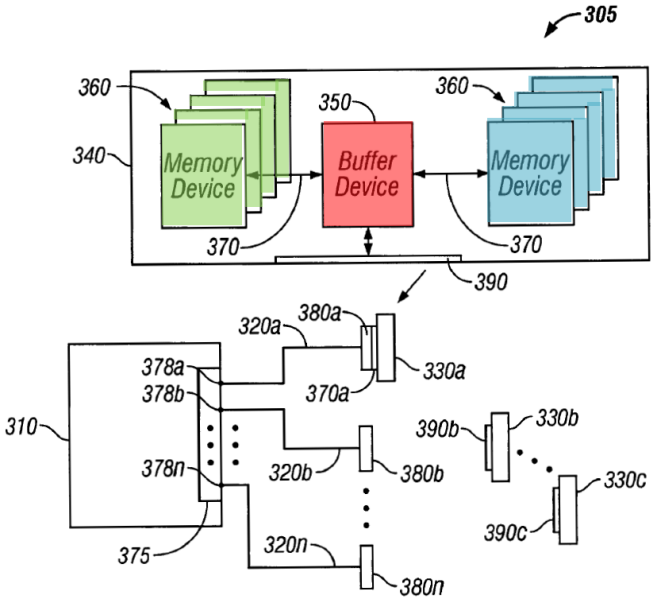


FIG. 3B

Indeed, it was well known at the time that DIMMs receive power through their edge connectors. *See, e.g.*, EX1108 (Dell), 1:65-2:20 ("A SIMM generally is easily inserted into a connector within the computer system, the SIMM thereby deriving all necessary power, ground, and logic signals therefrom. … A DIMM essentially comprises a SIMM …"), Fig.3 (DIMM having Power Supply and Ground pins); EX1051 (Doblar) at [0043-47] and Figs. 1-5 (DIMMs with edge connector pins and mating connector sockets including pins for power); EX1104

(JESD21-C), 4.20.4-1 ("DDR SDRAM Registered DIMM Design Specification"), 4.20.4-6 ("Pin Description […] V_{DD} SDRAM positive power supply [] V_{DDQ} SDRAM I/O Driver positive power supply [] V_{REF} SDRAM I/O reference supply [] V_{DDSPD} Serial EEPROM positive power supply "); EX1028 (JESD205), p.1 ("DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification"), p.11 ("DIMM Connector Pin Description […] V_{CC} AMB Core Power and AMB Channel Interface Power (1.5 Volt) […] V_{DD} DRAM Power and AMB DRAM I/O Power (1.8 Volt) […] V_{TT} DRAM Address/Command/Clock Termination Power ($V_{DD/2}$) […] V_{DDSPD} SPD Power …").

177. Harris further discloses that standard DIMMs have "a relatively large number of pins" coupled to "power supply rails … powered from system board or main board voltage sources, and are specific to the memory technology." EX1023, ¶[0002]; *see also id*., ¶[0012] ("a standard FBD module requires 28 Vdd pins (for DRAM devices) and 8 Vcc pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface"); EX1108 (Dell), Fig. 3 (168 Pin SDRAM DIMM having 17+2 Power Supply pins and 18 Ground pins). Harris's "technology-independent voltage distribution scheme" is "replacing these power supply interface pins [for receiving voltages specific to the memory technology on the module] with as few as six +12V pins." EX1023, ¶¶[0002], [0012], [0019]. As discussed above, *supra* ¶¶153-161, the 12V

power rails were readily available on motherboards at the time to provide 12V power supply for a memory module under Harris's voltage distribution scheme. EX1023, ¶¶[0014] ("It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages."), [0020] ("Further, the embodiments are amenable to dual +12V power supply rail implementations so that industry-standard form factors can be advantageously accommodated."). Harris also explains that, in its Fig. 3, "each memory board … receives a supply voltage that … may be sourced from the memory controller 302." *Id*., Fig. 3 (below), ¶[0017] ("Although not explicitly shown in this FIGURE, each memory board also receives a supply voltage that is locally converted by an on-board VRM for powering the DRAM and buffer components therein. In one arrangement, the supply voltage may be sourced from the memory controller 302 or from a separate voltage source."). Thus, Harris discloses that the module receives its supply voltage through their expressly shown edge connectors to interface with the power supply. *Id*.

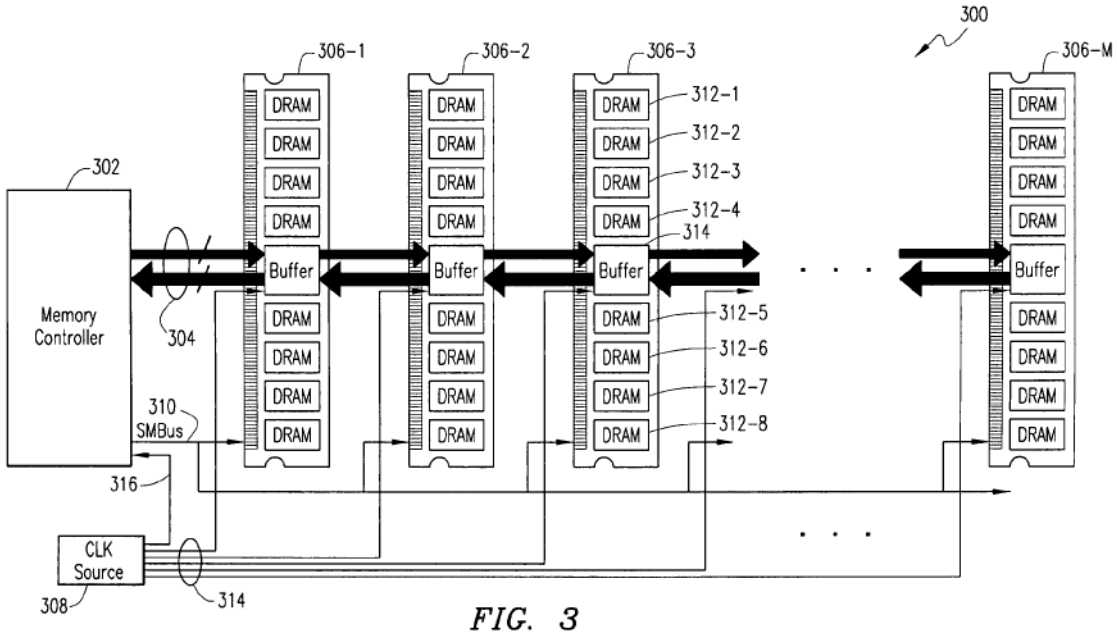


FIG. 3

178. In prior IPRs, involving related patents with the same specification as the '366 Patent, Netlist argued that Harris does not disclose that the module's edge connections are "configured to couple power … between the memory module and the host system," but the Board already considered and rejected those arguments. EX1070 (FWD of the 918IPR), 42-50; EX1071 (FWD of the 054IPR), 37-39. For example, the Board found that Harris discloses that DRAM devices may be "powered from system board or main board voltage sources." EX1070, 49. The Board further found that Harris's teaching of "replacing … power supply interface pins with as few as six +12V pins" means that those six pins take the place of the power pins in the prior art interface, "implying that power still comes from the interface with the host system." *Id.* (citing EX1023, ¶¶[0012], [0017]). The Board also found that Harris's teaching that "external voltage sources may comprise any

combination of known or heretofore unknown voltage supplies" means that the voltage supply "may be the host system," which was known to provide 12V supply. *Id*., 50 (citing EX1023, ¶[0014]). The Board credited Samsung's expert testimony explaining that Harris's statement that "system board power supply and associated voltage plane(s) are eliminated" means that "supplies such as the memory VDD and memory VCC that are specific to a particular generation of memory chips … can be supplied on the DIMM rather than being supplied from the motherboard." *Id*. (citing EX1076 (Samsung's expert testimony), 116:25-117:6). The Board also relied on the undisputed fact and supporting evidence that commercially available DIMMs derive their power from the host. *Id*. (citing EX1076, 92:9-95:8 ("Lots of computer systems had 12-volt power rails"); EX1075 (Netlist's expert testimony), 180:14-183:3 ("Q. … this document indicates that the power supply on the [ATX] is 12 volts; correct? A. It indicates that … there has to be a 12-volt output, that has to be provided by the power supply, yeh.")).

179. Accordingly, the memory module under Ground 2 includes edge connectors not only to communicate data and address/control signals, *supra* ¶¶173-174, but also to receive a power supply from the host system, such as Harris's +12V power supply, as illustrated in the annotated Fig.3 below. *Supra* ¶¶153-170; EX1035, Fig. 3C (below, annotated). Thus, the "mating connectors 380a-380n," which "interface with [edge] connectors 390," EX1035, 6:1-11, further include "*a*

set of power conduits" electrically coupled to the power supply edge connectors to deliver the system power to the module.

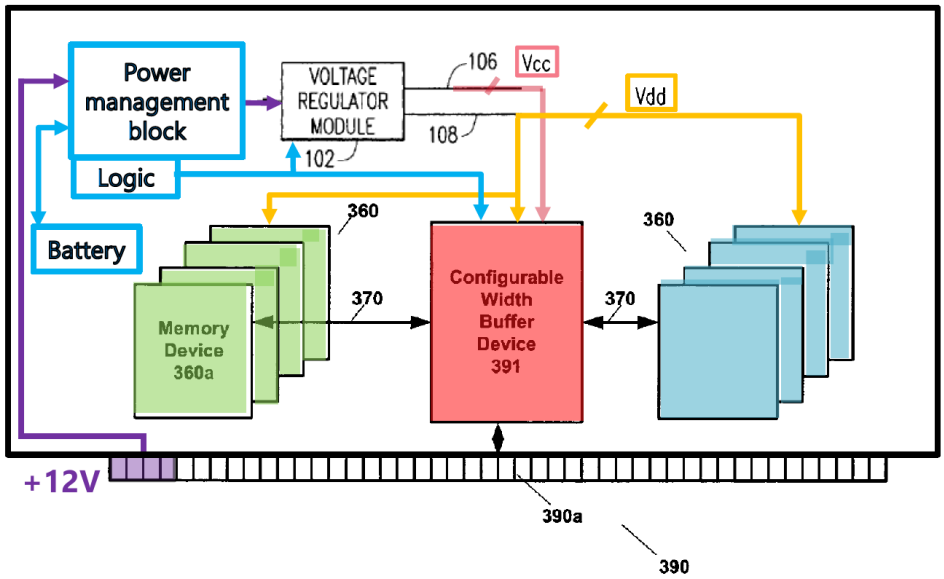


Fig. 3C

2. [1.b.3] Power Delivered to the DIMM

180. Ground 2 discloses "*the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM*" as explained above for [1.a.2] and as shown in the annotated Fig.3C below. *Supra* ¶¶172-179, 153-170; EX1035, Fig.3C (below).

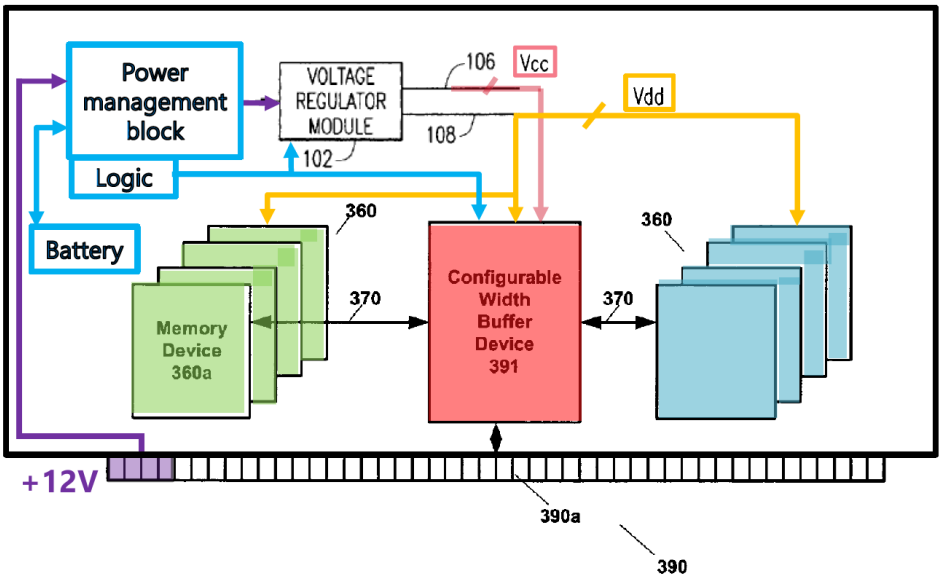


Fig. 3C

181. It was common practice at the time to have "*the power delivered to the DIMM from the power rails of the system board*." Harris, for example, discloses that "Dual In-line Memory Modules (DIMMS) populated with dynamic random access memory (DRAM) devices, are provided with power supply rails … that are powered from system board or main board voltage sources" and specifically teaches that its "embodiments are amenable to dual +12V power supply rail implementations." EX1023, ¶¶[0002], [0020]. Harris does not disclose any power source for delivering power to the DIMM other than the power supply rails of the system board.

182. Furthermore, "deriving all necessary power" from the DIMM's connector was common practice at the time. EX1108 (Dell, cited by Perego (EX1035) at 2:4-6), 1:65-2:20 ("A SIMM generally is easily inserted into a

connector within the computer system, the SIMM thereby deriving all necessary power, ground, and logic signals therefrom. … A DIMM essentially comprises a SIMM …"). Thus, the combination of Perego and Harris discloses that "*the power delivered to the DIMM from the* [12V] *power rails of the system board is the only power received by the DIMM*."

183. Amidi also teaches delivering power to the DIMM from the power rails of the system board only. For example, Amidi teaches that its module includes an on-board battery charger (620) that uses the same system supply (605) to charge the battery (630) than what provides power to the rest of the module. EX1024, Fig. 6 (below), 4:23-43 ("System supply 605 provides a system power supply to a boost power converter 610 … Boost converter 610 provides a power output 615 which powers battery charger 620—which in turn supplies battery 630.").

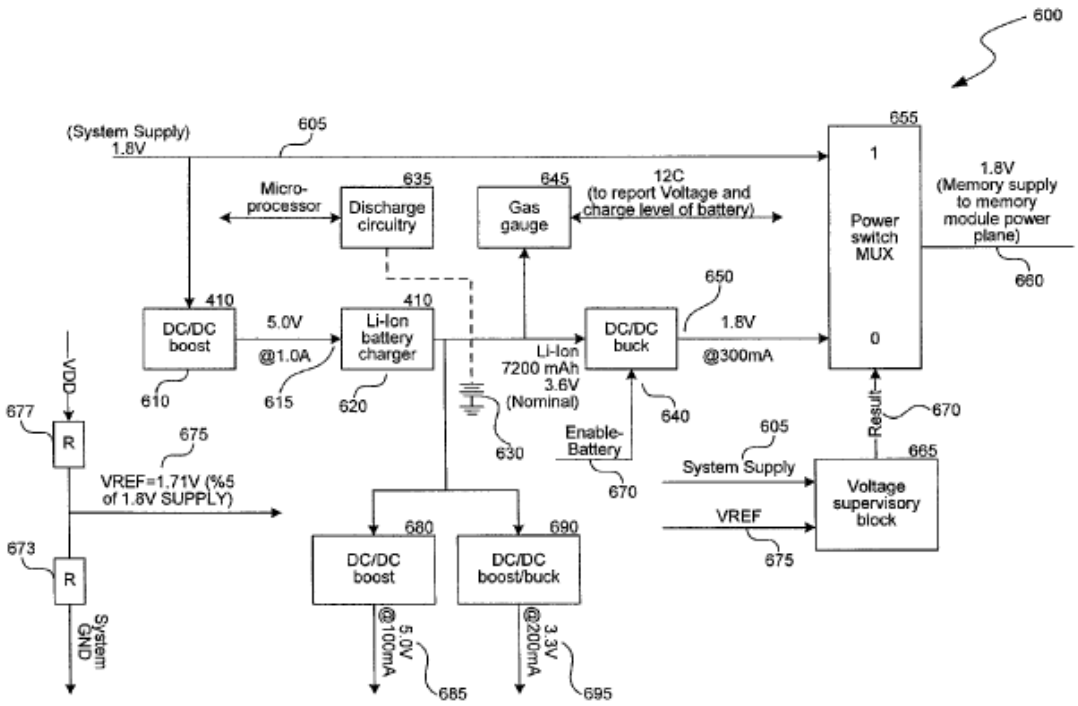


FIG. 6

As illustrated in Fig. 4 of Amidi, the battery charger (485) and the battery (475) are part of Amidi's memory module. EX1024, Fig. 4, 3:64-4:13.

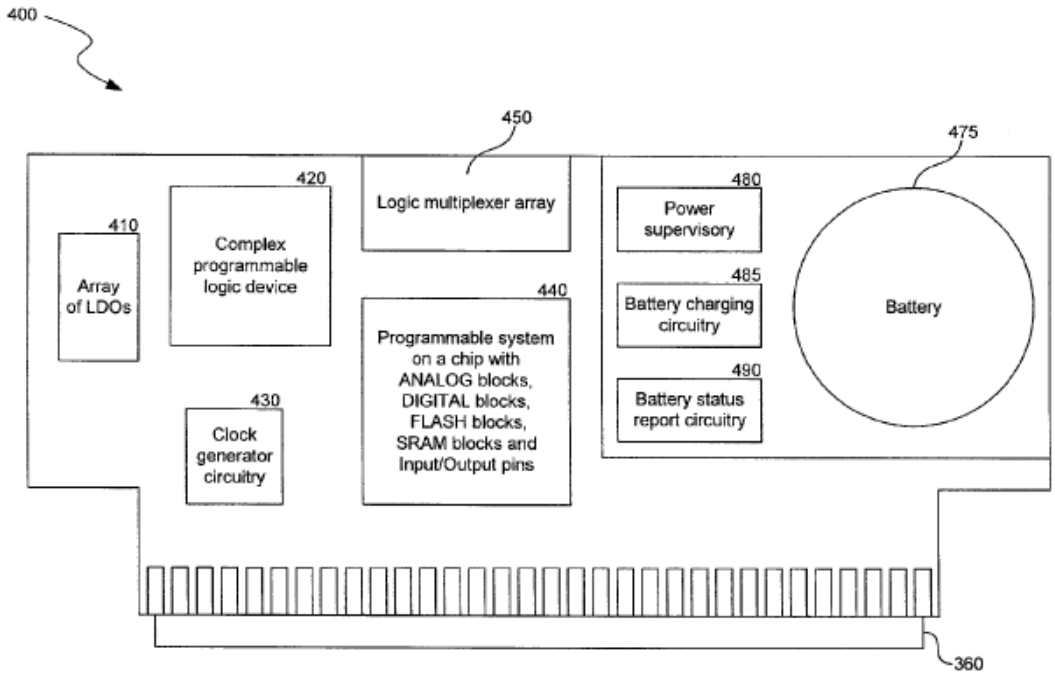


FIG. 4

Thus, Amidi also teaches "deriving all necessary power," including the power required to charge the battery, from the memory PCB connector, as was common practice at the time. EX1108 (Dell, cited by Perego (EX1035) at 2:4-6), 1:65-2:20 ("A SIMM generally is easily inserted into a connector within the computer system, the SIMM thereby deriving all necessary power, ground, and logic signals therefrom…").

184. Amidi's chargeable battery operates substantially the same way as the secondary power source of the '366 Patent, including the use of power from the system board to charge the secondary power source. EX1001, 20:63-67 ("For example, when no power failure is detected, the power module may provide power

to certain components, such as the volatile memory, from system power while charging a secondary power source (e.g., a capacitor array).”). The ’366 specification suggests that capacitors may be better than batteries for the second (backup) power supply, but these concerns are limited to batteries that “need to be replaced” and, in any event, do not support excluding batteries in general. EX1001, 26:19-35. Rather, the ’366 Patent discusses some known advantages of using capacitors (which are like rechargeable batteries) over non-rechargeable batteries. Indeed, the ’366 Patent expressly teaches that, “in certain embodiments, the second power supply … may comprise a battery.” EX1001, 26:35-39. Using either a capacitor or a battery as a secondary power source on a memory module were well-known, and obvious, alternatives at the time. EX1025 (Spiers), [0009] (“The secondary power source may comprise a capacitor, a battery, or any other suitable power source.”).

185. Accordingly, in the combination of Ground 2, a Skilled Artisan would have understood that power was readily available to the DIMM from the power rails of the system board and thus been motivated to implement the combination of Ground 2 such that “*the power delivered to the DIMM from the* [12V] *power rails of the system board is the only power received by the DIMM*.”

Samsung Electronics Co., Ltd.
Ex. 1003, p. 122

3. [1.c.3] Trigger Signal

186. Ground 2 discloses "*the voltage monitor circuit* [e.g., Amidi's "voltage supervisory block 665"] *configured to:…(ii) generate a trigger signal* [e.g., "signal 670 caus[ing] power switch multiplexer 655 to choose battery power 650"] *upon detecting a trigger condition* [e.g., "[i]f system supply 605 has a magnitude lower than reference voltage 675"]." EX1024, 4:44-55 ("Signal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two. If system supply 605 has a greater magnitude than reference voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660. If system supply 605 has a magnitude lower than reference voltage 675, then signal 670 causes power switch multiplexer 655 to choose battery power 650 for memory supply 660."), Fig.6 (below, annotated).

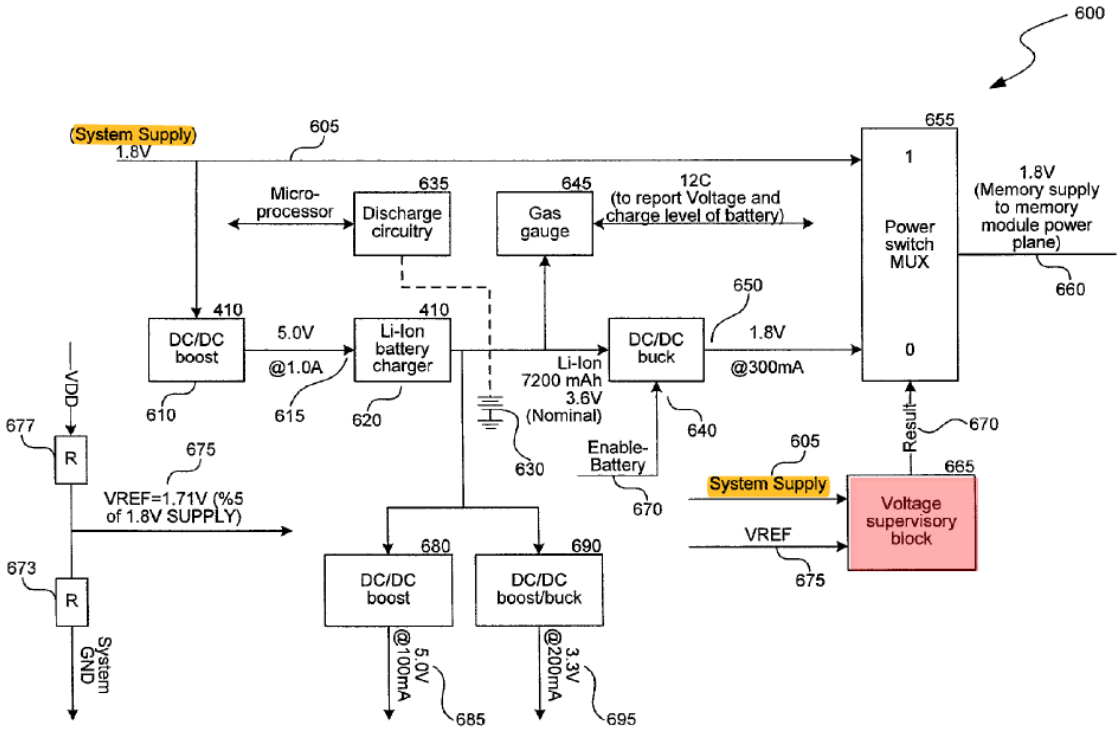


FIG. 6

187. In the combination, the voltage monitor circuit may also detect both overvoltage (when the input voltage exceeds the upper threshold of the operating range) and undervoltage (when the input voltage goes below the lower threshold of the operating range) as "*a trigger condition*," such as when the system voltage is outside "a wide tolerance" of "around +/-15%" of +12V. EX1023, ¶[0013]. The Board has also found that the combination of Harris and Amidi discloses substantially similar limitations, specifically finding that the combination teaches detecting both over- and under-voltage. EX1070 (918 FWD), 79 ("Harris discloses that its +12V power supply has a tolerance of '+/-15%' which indicates it would be

a concern if the power supply was greater than 15% …[and] Amidi indicates concern with 'power fault[s]' … [thus] a person of ordinary skill in the art considering these teachings would have considered it obvious to detect overvoltage and generate a trigger signal in response to the detection."), 83 ("Amidi provides the teaching of generating the trigger signal ***onboard the memory module*** in response to detecting a 'power fault.'") (emphasis in original); EX1071 (054 FWD), 65 (similar).

4. [1.c.5] Write Operation

188. Ground 2 discloses "*the controller is configured to perform, in response to the trigger signal* [e.g., Amidi's "signal 670" indicating a power failure], *a write operation to write data* [e.g., configuration/status information used for restoration, EX1024, 1:23-25, 8:62-9:2, or information about the power failure to be used for failure analysis, EX1024, 1:21-22] *into the nonvolatile memory* [e.g., Perego's "operations circuit 572" or "SPD device," EX1035, 15:46-16:12]."

189. In particular, Amidi teaches that "one may expect that SDRAM will be properly refreshed when system power is present and a system operates normally, but if SDRAM is to retain memory in a power fail situation, refresh operations must be implemented without benefit of other parts of a system, requiring that the memory module trigger SDRAM refresh operations itself." EX1024, 6:40-52. Thus, as part of its power fault detection and switching to

backup power, Amidi "provide[s] a process which operates to detect voltage … signals, initiate backup operations, maintain memory (through refresh, for example), and detect a recovery status." *Id*., 2:11-26. For maintaining memory, Amidi teaches putting the memories into a "self refresh state." *Id*., 6:53-7:8, Fig. 11 (finite state machine including commands to self-refresh memory), Fig. 14 (below, showing memory in self-refresh state 1450 after power fault detection 1440).

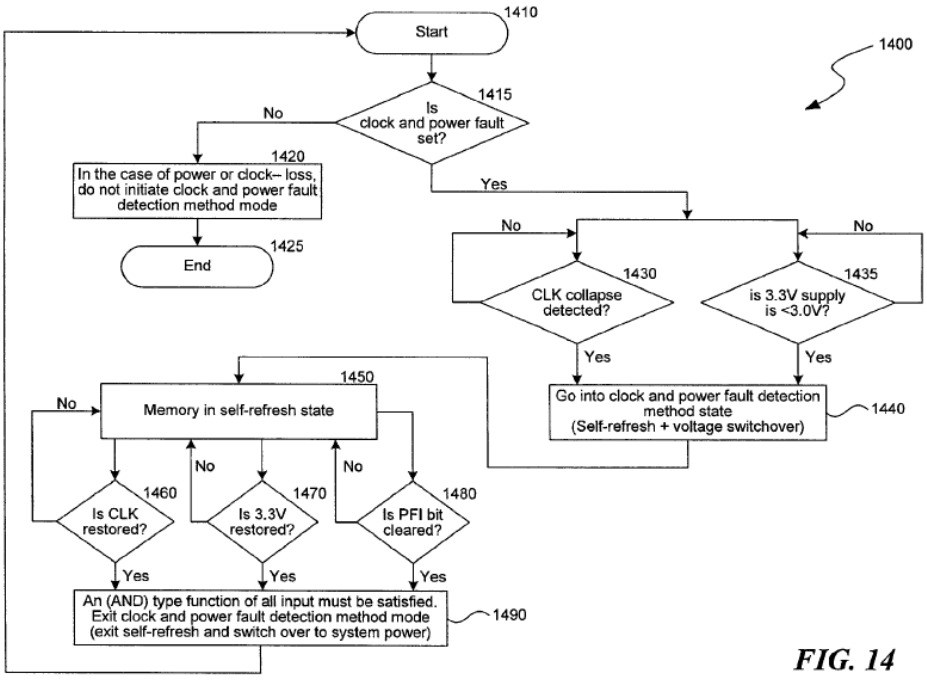


FIG. 14

190. Putting memory into a self-refresh state while using lower power as taught by Amidi was also known as "S3 sleeping state." EX1109 (ACPI), p.229 ("The S3 state is defined as a low wake-latency sleep state … [in which] some devices may be in a lower power state…."). For example, an S3 sleeping state

transition can include "[p]lacing the memory into a low-power auto-refresh or self-refresh state" and "[d]evices that are maintaining memory isolating themselves from other devices in the system" such that "only devices supporting memory are powered (possibly partially powered)." *Id*. The S3 sleeping state was also used in "a standard FBD module," i.e., a standard fully buffered DIMM, which Harris expressly references. EX1023, ¶[0012]. For example, one of the FBD standards explains that "S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode." EX1027 (JESD82-20), 39.

191. Amidi also discloses that its memory module returns to normal operation after the power is restored and the system is ready for controlling the normal operation. EX1024, Fig. 15 (below), 8:62-9:2 ("Process 1500 includes initiating monitoring, detecting a fault, initiating a backup system, maintaining memory, detecting potential restoration, checking whether a system is ready, and restoring control to the system."). Amidi explains that "some data may be useful for restarting a system after a failure." *Id*., 1:23-25. For example, in order to wake up from the S3 sleeping state properly, "the BIOS needs to store the pre-sleeping state or initial boot state configuration in a non-volatile memory area … to enable it to restore the values during the waking process." EX1109 (ACPI), p.229. Similarly, Amidi's teaching of "restoring control to the system" would also require

"to store the pre-sleeping state … in a non-volatile memory area … to enable it to restore the values during the waking process." *Id*.

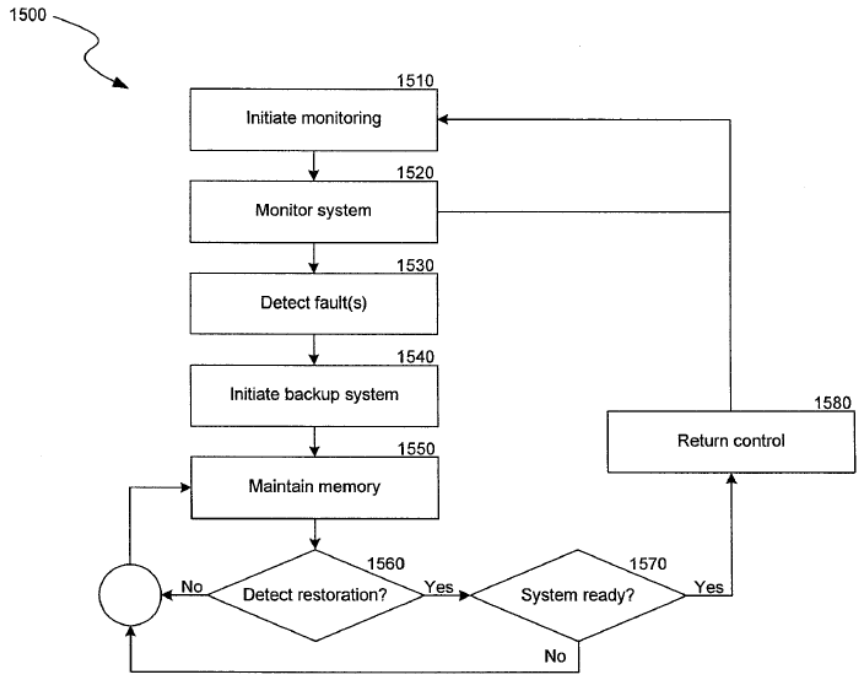


FIG. 15

192. The standard FBD referenced by Harris also requires that S3 recovery configuration registers "should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin." EX1027 (JESD82-20), 25. For example, "S3RESTORE … registers contain implementation dependent state needed to recover connections to DRAMs left in self refresh without destroying data in the DRAMs … [such as] calibration information for DDR IO drivers. BIOS will copy these registers into some form of stable storage prior to system standby then restore these registers after system wakes up." *Id*., 141. Perego also discloses parameters needed to restore system

control, including Perego's state storage 576 which "may store … the desired width of configurable width interface 590, and … the desired width of one or more of interfaces 520a and 520b" which can be used "to establish the desired configuration" of these interfaces. EX1035, 16:13-21.

193. Thus, restoring system control after a power failure as taught by Amidi includes or at least renders obvious using the known techniques for restoring memory operations after an S3 sleeping state, including writing configuration information before the sleeping state into non-volatile memory, such as operations circuit 572 or an SPD device of Perego, and using the stored configuration information for restoring normal operation. *See*, *e.g.*, EX1024, 1:23-25 ("[S]ome data may be useful for restarting a system after a failure."). In addition, Amidi also discloses that "failure analysis can be much simpler if information about the state of a system is available after a failure occurs." EX1024, 1:21-22. The "information about the state of a system is available after a failure occurs" if such failure information (along with the configuration information for recovery) is written into the non-volatile memory, such as Perego's "operations circuit 572" or an "SPD device" in the proposed combination. EX1035, 15:46-16:12. Indeed, storing failure information into non-volatile memory was a well-known technique at the time. *See*, *e.g.*, EX1025 (Spiers), ¶¶[0038] ("An EEPROM 210 is connected to the FPGA processor 198, and is

utilized to store various status indicators and counters, which may be utilized during operations."), [0042] ("[T]he backup device includes an EEPROM that contains various status indicators as well as other statistics.").

194. The Board also agreed that the S3 sleep mode would be used to conserve power during Amidi's battery backup mode and that the S3 sleep mode requires writing S3 configuration information into the non-volatile memory in the SPD before going to sleep. EX1070 (FWD of the 918 IPR), 80-81 (considering the limitations of "in response to the trigger signal, the logic element writes information into the non-volatile memory," the Board agreeing that "the features of these claims are taught or at least suggested by the combination of Harris, the FBDIMM Standards, and Amidi"); EX1071 (FWD of the 054 IPR), 61-63 (similar).

5. [1.d.2] Receiving or Outputting Data

195. Ground 2 discloses "*the DDR SDRAM devices being operable to receive or output data signals* [e.g., "stor[ing]" and "retriev[ing]" data, EX1035, 3:64-65] *via the set of data lines* [e.g., DQ data lines, EX1035, Fig.4B (below, annotated)] *based on address and control signals* [e.g., "associated with a particular address provided…as part of a write or read command," EX1035, 3:65-66] *received from the system board via the set of address and control lines* [e.g., RQ address/control lines, EX1035, Fig.4B (below, annotated)]," as was typical for

DDR SDRAM memory devices. *See, e.g.*, EX1035, 3:64-4:12 ("A memory device stores data (which may be retrieved) associated with a particular address provided, for example, as part of a write or read command. Examples of types of memory devices include dynamic random access memory (DRAM), static random access memory (SRAM), and double data rate SDRAM (DDR). A memory device typically includes request decode and array access logic that, among other functions, decodes request and address information, and controls memory transfers between a memory array and routing path. A memory device includes a transceiver for transmitting and receiving data in an embodiment of the present invention."); EX1026, 20-30 (Bank Activate followed by Read and write access modes), Figure 20 (p.21, reproduced below, Bank activate with row address followed by Read command with column address), Figure 21 (p.22, reproduced below, showing data transfer for read and write commands).

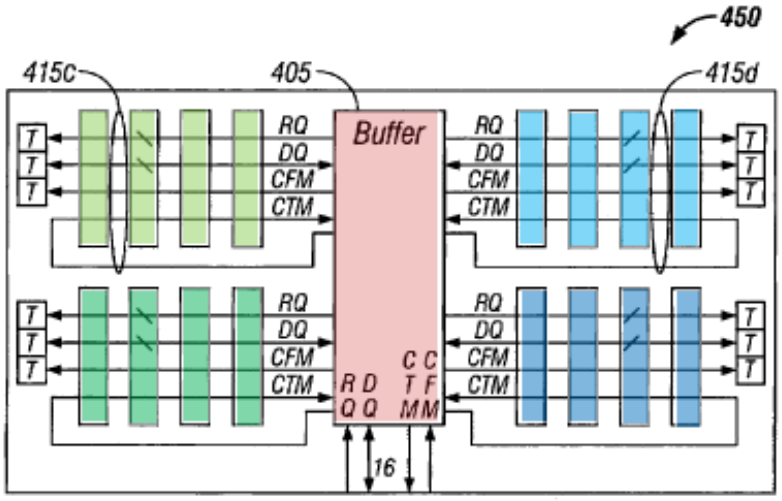


FIG. 4B

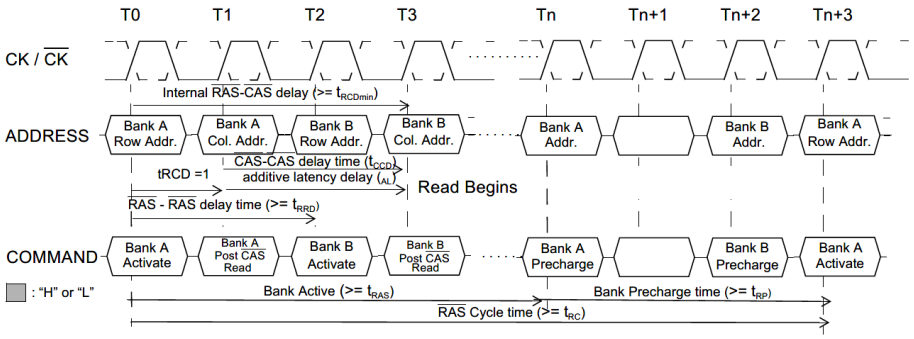
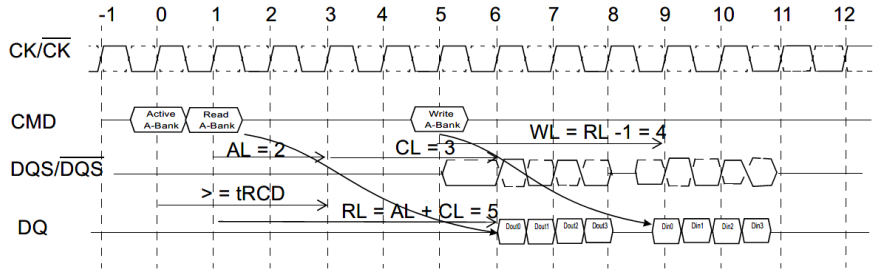


Figure 20 — Bank activate command cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2



[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]

Figure 21 — Example 1: Read followed by a write to the same bank, where AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4

196. Perego also discloses that the address and control signals for memory operations like read and write are received from the system board. EX1035, Fig. 3B (below), 6:12-27 ("In a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370. One or more of memory devices 360 may respond by transmitting data to Buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a. Controller 310 receives the signals corresponding to the data at corresponding ports 378a-378n.").

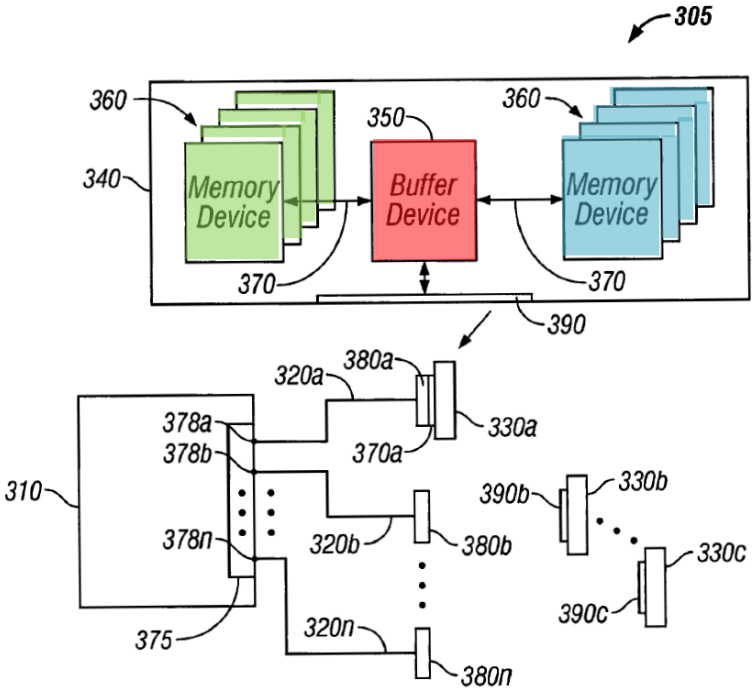


FIG. 3B

6. [1.e] Converter Circuits

197. Ground 2 discloses "*first, second, third, and fourth converter circuits* [e.g., in Harris's Voltage Regulator Module 102 in Fig.3C below] *coupled to the PCB and to the input voltage supply line* [e.g., purple line in Fig.3C providing +12V input supply], *and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines* [e.g., for delivering, respectively, (i) V_{dd} to the memory devices 360 and to the buffer device 391 in Fig. 3C, (ii) V_{cc} to the buffer device 391 in Fig.3C, (iii) V_{tt} to on-board "termination elements 420" in Fig.4A below, and (iv) V_{DDSPD} to the non-volatile memory in "operations circuit 572" or SPD in the buffer device 391 in Fig.3C]." Ex1035, Figs. 3C, 5B, 4A (below, annotated); *supra* ¶¶153-170.

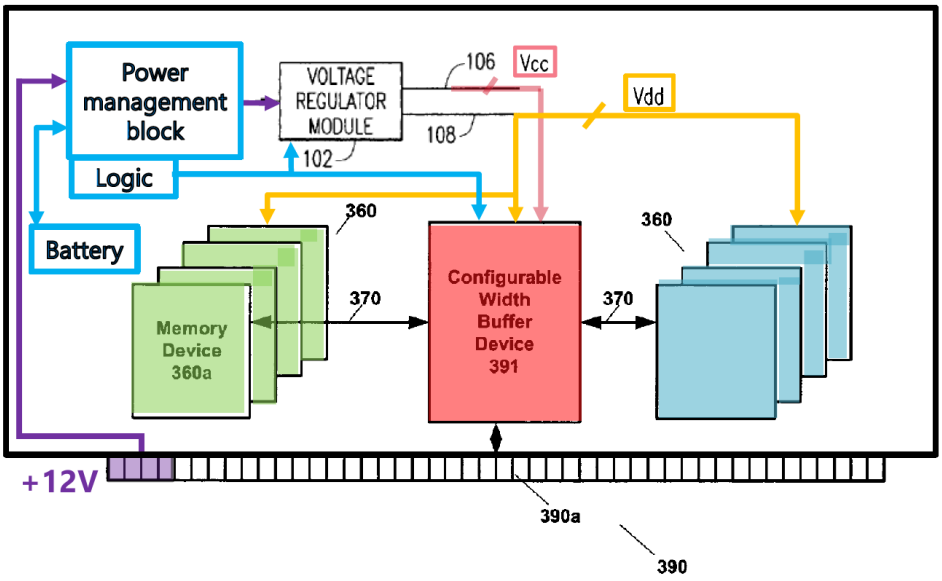

Power management block
Logic
Battery
VOLTAGE REGULATOR MODULE
102
106
Vcc
108
Vdd
360
370
Memory Device 360a
Configurable Width Buffer Device 391
360
370
+12V
390a
390

Fig. 3C

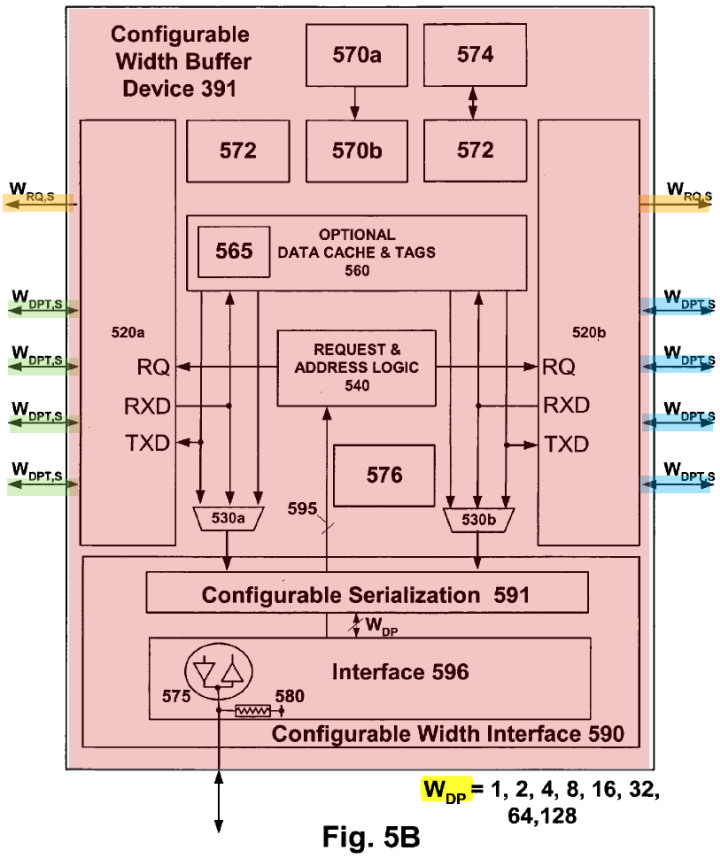

Configurable Width Buffer Device 391
570a
574
572
570b
572
565
OPTIONAL DATA CACHE & TAGS 560
520a
520b
RQ
RXD
TXD
REQUEST & ADDRESS LOGIC 540
576
595
530a
530b
Configurable Serialization 591
Interface 596
575
580
Configurable Width Interface 590
W_DP = 1, 2, 4, 8, 16, 32, 64,128

Fig. 5B

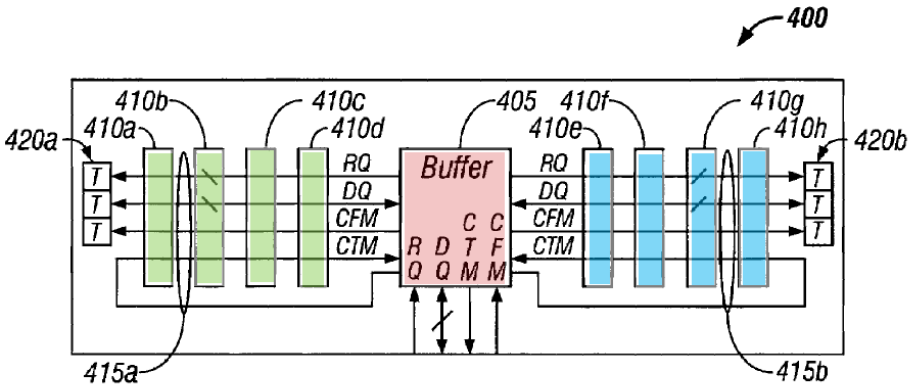


FIG. 4A

198. Harris teaches that its on-board Voltage Regulator Module (VRM 102) includes "*converter circuits coupled to the PCB*" which provide regulated voltages with "tightly controlled voltage levels" for the components of the module. EX1023, ¶[0010] ("In accordance with the teachings of the present patent disclosure, at least one on-board voltage regulator module (VRM) is provided as part of the memory board assembly module 100A for converting an externally supplied voltage level available on external source path 104 into appropriate local voltage levels that power the first and second voltage paths, i.e., the Vdd and Vcc paths 108, 106, respectively. Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM 102 for purposes of the present patent disclosure."). Harris also teaches "a first voltage path 108, typically referred to as a V_{dd} path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices, e.g., from about 0.5V to

3.5V or more." EX1023, ¶[0009]. Perego discloses using DDR2 SDRAM memory devices, EX1035, 10:56-59, and Harris teaches that "the memory devices can be of any known or heretofore unknown DDR type, e.g., DDR2 (operable with 1.8 V), DDR3 (operable with 1.35V to 1.5V), and the like," EX1023, ¶[0009]. Thus, in a DDR2 implementation, the V_{dd} path would include "*first … regulated voltage lines*" and the Voltage regulator module would include a "*first … converter circuit*" to convert the +12V input voltage to 1.8V regulated voltage to power DDR2 memories. Perego's buffer would also receive the regulated V_{dd} voltage (1.8V for DDR2 technology) in order to communicate with those memory devices (e.g., DDR2 memories). *Id*., ¶[0002] ("As the performance of the DRAM technology goes up, and timing margins shrink, it is becoming increasingly more difficult for the system board sources to provide tightly regulated power for the DRAM cores as well as input/output (I/O) interface buffers.").

199. Harris also discloses that "bidirectional memory controller interface path 114 as well as a second voltage path 106, typically referred to as a V_{cc} path, are provided with respect to the buffer component 112, wherein the V_{cc} path may be energized to appropriate voltage levels depending on the buffer and DIMM technology, e.g., from about 0.5V to 3.5V or more." EX1023, ¶[0009]. Similar to Harris, Perego also discloses that its DIMM uses a buffer device interfacing with memories on one side and with the memory controller on the other side. *See, e.g.*,

EX1035, 10:54-67 ("Utilizing buffer device 405 between the memory devices and controller in accordance with the present invention (e.g., see FIG. 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation."). Thus, in the combination with Perego, Harris's V_{cc} path would include "*second … regulated voltage lines*" and the Voltage regulator module would include a "*second … converter circuit*" to convert the +12V input voltage to a regulated voltage level as required to power the specific implementation of the buffer device and the DIMM's memory controller interface of Perego.

200. Perego also discloses that signals to the memory devices are terminated by termination elements (420). EX1035, Fig. 4A (below, annotated), 9:34-38 ("The plurality of signal lines may be controlled impedance transmission lines that are terminated using respective termination elements 420a and 420b.").

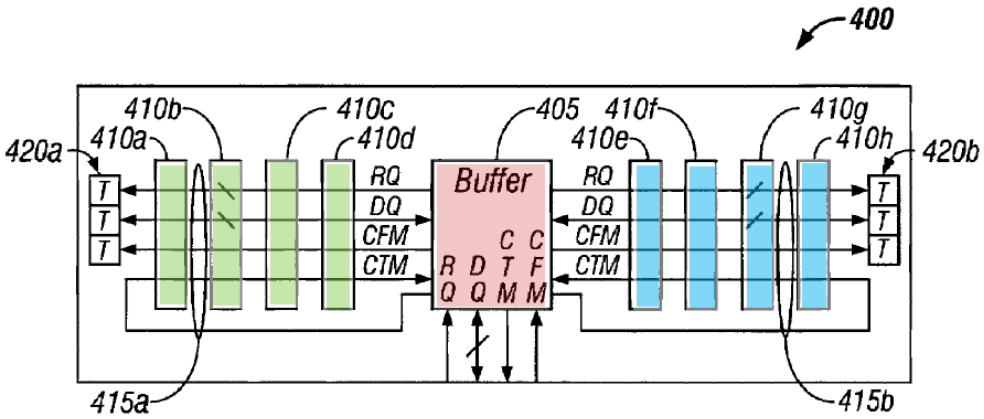


FIG. 4A

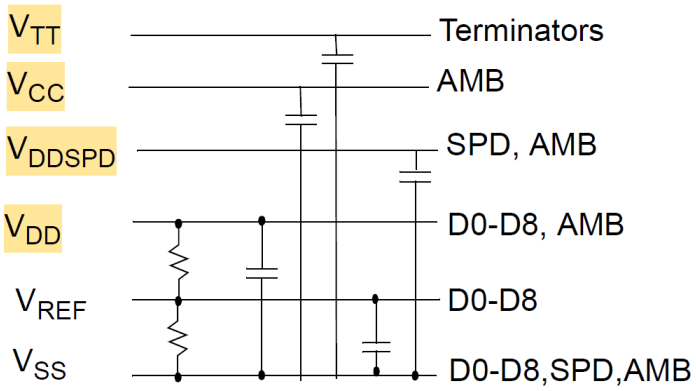
Perego further explains that such "terminator(s) connect to a termination voltage, such as ground or a reference voltage." *Id.*, 9:1-12. Thus, in the combination with Harris, the Voltage Regulator Module also includes a converter to provide the proper "termination voltage" V_{tt} to terminate signal lines to the memory devices. The Board has already found that it would be obvious in light of Harris to generate Vtt on the module using a buck converter. EX1070 (918 FWD), pp.34-38; EX1071 (054 FWD), pp.30-34. In the case of DDR2 memory devices, the address and command lines are terminated by a V_{tt} voltage which is half (i.e., 0.9V) of the memories' operating voltage V_{dd} (1.8V). EX1026 (JESD79-2B), 9 (Power-up and initialization sequence includes applying V_{tt}), 49 (operating condition require V_{tt} to track the reference voltage VREF of 0.5*1.8V). Thus, in a DDR2 implementation, the paths would include "*third … regulated voltage lines*" and the Voltage regulator module would include a "*third … converter circuit*" to convert the +12V

input voltage to 0.9V regulated voltage to properly terminate address and command lines to the DDR2 memories.

201. Perego also discloses that operations circuit 572 in its buffer device or a separate SPD device includes non-volatile memory. EX1035, 15:46-16:12 ("Operations circuit 572 (similarly, as described above) is included in configurable width buffer device 391 in an embodiment of the present invention. Operations circuit 572 includes storage circuit to store information used by the system in which the configurable width buffer device 391 is situated in, for example, to perform configuration operations. … The functionality of operations circuit 572 may be included on an SPD device for example, an EEPROM device …."). Such a non-volatile memory also requires power with a proper voltage for its operation, including power to write information into its non-volatile storage, as discussed above with reference to claim element [1.c.5]. *Supra* ¶¶188-194. For example, SPD devices at the time used a voltage of 3.3V. EX1027 (JESD82-20), 32 (V_{DDSPD} typical value of 3.3.V). Thus, in the combination with Perego, Harris's Vcc path would also include "*fourth … regulated voltage lines*" and the Voltage regulator module would include a "*fourth … converter circuit*" to convert the +12V input voltage to a regulated voltage level as required to power the non-volatile memory in the operations circuit 572 in Perego's buffer device or a separate SPD device.

202. As Harris explained, the specific values of the voltages that are provided by the voltage regulator module depend on the type of the memory module and the technologies used. *See, e.g.*, EX1023, ¶[0009] ("Further, the DIMM configuration of an exemplary memory module may include unbuffered DIMMs, registered DIMMs (RDIMMs), or fully buffered DIMMs (FBDs), and may be configured as having one or more ranks (e.g., 2, 4, 8, or more)."). Taking the example of the FBDs, the corresponding JEDEC standards specify the required voltage levels. *See, e.g.*, EX1027 (JESD82-20), 32 (Advanced Memory Buffer requiring a VCC voltage of 1.5V for its link and core functions, a VDD voltage of 1.8V for interfacing with the DDR2 memories, a VDDSPD voltage of 3.3V for operating the SPD, and "[t]here will also be a VTT termination supply at VDD/2 available on the DIMM"); EX1028 (JESD205), 9 (listing supply voltages, below annotated), 13 (reproduced below in part annotated, showing power line connections).

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})



Perego's memory module can use DDR2 memories and a buffer device which interfaces with those memories on one hand and with the system's memory controller on the other, similar to the fully buffered DIMM (FBD) discussed by Harris. *Compare*, *e.g.*, EX1023, Fig. 1A, *with* EX1035, Fig. 3C.

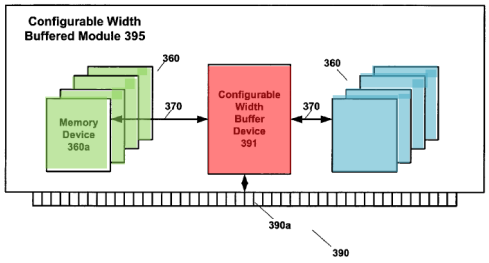


Fig. 3C

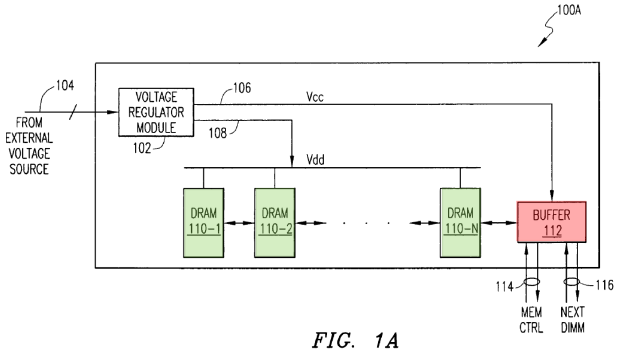


FIG. 1A

Thus, like Harris's FBD, Perego's module in combination with Harris requires the Voltage Regulator Module to include at least four converter circuits to provide at least four voltages: V_{DD} for the memories, V_{CC} for the buffer, V_{TT} to terminate the address and control lines from the buffer to the memories, and V_{DDSPD} for the non-volatile memory, like SPD.

203. The Board has already considered the issues related to the converter circuits in Harris and Netlist's counter-arguments in detail and found that Harris, in light of the JEDEC standards, renders obvious a memory module having at least four converters, EX1070 (FWD of the 918 IPR), 24-29, including separate converters to generate $V_{DD}/V_{DDQ}/V_{DDL}$ or V_{CC}/V_{CCFBD}, *id*., 30-34, a buck converter for the termination voltage V_{TT}, *id*., 34-38, and a buck converter to provide V_{DDSPD} for the non-volatile memory, *id*., 38-41. The Board also found that the four buck converters provide four respective regulated voltages. *Id*., 56-59. Since Perego's module requires the same or similar voltages as Harris's FBD implementation, the Board's reasons equally apply to the combination of Harris and Perego.

7. [1.h.1]-[1.h.2] First Group of DDR SDRAM

204. Ground 2 discloses "*wherein the plurality of DDR SDRAM devices includes: a first group of at least five DDR SDRAM devices* [e.g., five memory devices in channel 415b or 415d below in Fig.4C] *that are each connected to a first chip select line configured to electrically conduct a first chip select signal* [e.g., to select memory devices in the channel for read/write operations]." EX1035, Fig. 4C (below, annotated), 21:16-20 ("Any number of channels 415a-415d, for example…two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b

remain in a ready or standby state until called upon to perform memory access operations.").

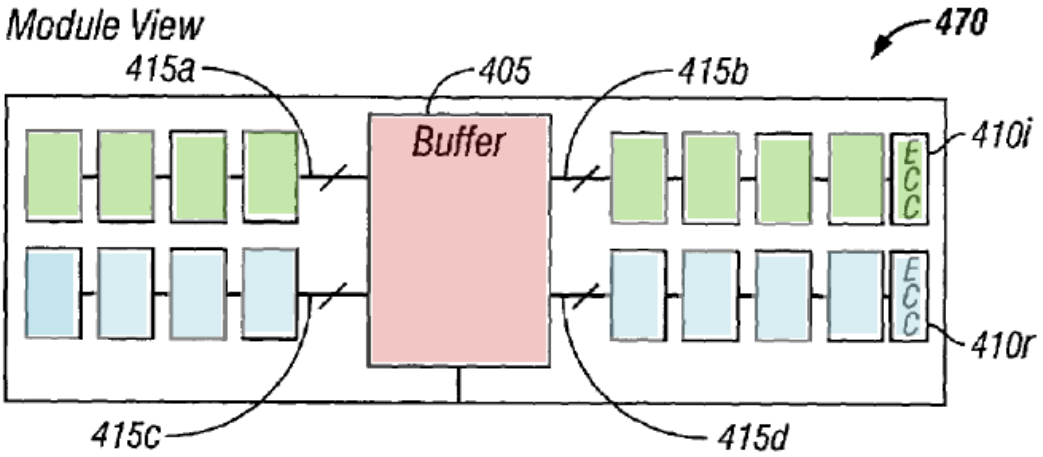


FIG. 4C

205. Perego explains that, "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320 a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." EX1035, 6:15-24. Perego also discloses using DDR2 memory devices. *Id*., 10:54-59. For a "normal memory read operation" from such DDR2 memory devices, the signals "corresponding" to "control, and address information" include a "chip select signal" which selects the memory devices to perform the operation, as taught by Amidi. EX1024, 7:55-56 ("Truth table 1300 represents the values of signals to memory components of a DDR2 SDRAM"), Fig.13 & n.4 ("Write" and "Read" commands require "CS" chip-select signal asserted Low); EX1026 (JESD79-2B), pp.6 ("Chip Select: All

commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code."), 46-47 & n.1 (Command truth table including chip select (CS) signal asserted low for read and write operations); EX1107 (Jacob paper) at 2-3 ("chip-select…is essential"). The chip select signal is required for other memory operations, including write operations, as well. *Id*.

206. Perego further discloses that "[o]ne or more of memory devices 360 may respond [to the read command] by transmitting data to Buffer device 350 which receives the data via one or more of channels 370," making clear that memory devices in one channel can carry out the read operation. EX1035, 6:15-24. Since receiving a chip select signal is needed for the DDR SDRAMs to carry out the read operation and transmit data to the buffer, as discussed directly above, Perego discloses that the "*at least five DDR SDRAM devices* [in channel 415b or in channel 415d] … *are each connected to a first chip select line configured to electrically conduct a first chip select signal*."

8. [1.i.1] Not in Self-Refresh Mode

207. Ground 2 discloses "*when power from the power rails of the system board is provided to the DIMM* [in normal mode when power from the system is available] *and each group of the first and second groups of DDR SDRAM devices is* [being normally accessed or in a ready or standby state thus] *not in self-refresh*

mode [which Amidi discloses being used other times, when power from the system is not available]."

208. For example, Amidi discloses that "[d]uring normal operation of the system with proper power and/or clock operation the system control and command bus input … will be chosen," and the memory module operates according to that "system control and command bus input." EX1024, 7:35-38. Amidi teaches putting the DDR SDRAM devices into self-refresh mode only when the power (or the system clock) fails, as discussed above for element [1.c.5], *supra* ¶¶188-194, and as shown by Figure 14 of Amidi below.

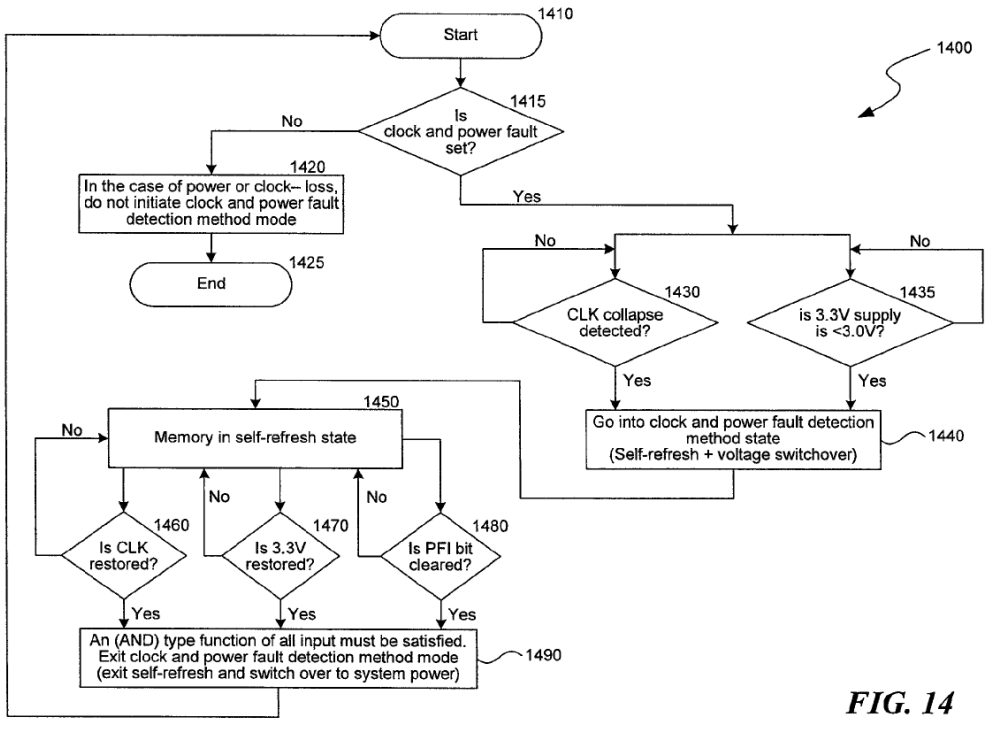


FIG. 14

209. Perego also discloses that, during normal operations, the memories are accessed or they are in a ready or standby state. EX1035, 21:16-20 ("Any number of channels 415a-415d, for example…two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations."). For DDR SDRAMs, the "ready or standby state" is different from the self-refresh mode, because the self-refresh mode disables all but CKE inputs (thus preventing normal read/write commands), turns off ODT, and requires a sequence of commands to exit from, followed by a preset time (e.g., tXSRD) after which other memory operations (e.g., read) can be performed. EX1026 (JESD79-2B), pp.6 ("Input buffers, excluding CKE, are disabled during self-refresh"), 16 ("ODT is turned off and not supported in SELF REFRESH mode."), 39 ("When the DDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are 'don't care'. … The procedure for exiting Self Refresh requires a sequence of commands."), 68 (Exit self refresh to a read command time tXSRD has a minimum of 200 clock cycle tCK). Thus, self-refresh mode is not a "ready or standby state," because the memory in self-refresh mode is not ready to receive and execute memory commands like a read or write command. Thus, Ground 2 discloses a normal mode "*when power from the power rails of the*

system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode."

9. [1.i.2] First Group of DDR SDRAM Enabled

210. Ground 2 discloses, during normal operations, "*the first group of DDR SDRAM devices* [e.g., including 5 memory devices in channel 415b or in channel 415d in Fig. 4C below] *is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines* [e.g., when each of the 5 memory devices in one channel is 8-bits wide, including four x8 memories for data and one x8 memory for ECC] *independently of whether the second group of DDR SDRAM devices* [e.g., including 4 memory devices in channel 415a or in channel 415c in Fig. 4C] *is enabled, in response to the second chip select signal, to receive or output an integer number of* [e.g., 32 = 4 memories each 8 bits wide] *1-bit DDR data signals in parallel via an integer number of* [e.g., 32=4x8] *data lines of the set of data lines* [e.g., when each of the 4 memory devices in one channel is 8-bits wide]" for the reasons discussed for [1.h.1]-[1.h.2], *supra* ¶¶204-206, and further discussed below. EX1035, Fig. 4C (below), 10:48-53 ("Other features may also be incorporated to enhance module 400 in high capacity memory systems, for example, additional memory devices and interface signals for error correction code

storage and transport (ECC). Referring to FIG. 4C, memory devices 410i and 410r intended for ECC are disposed on module 470.").

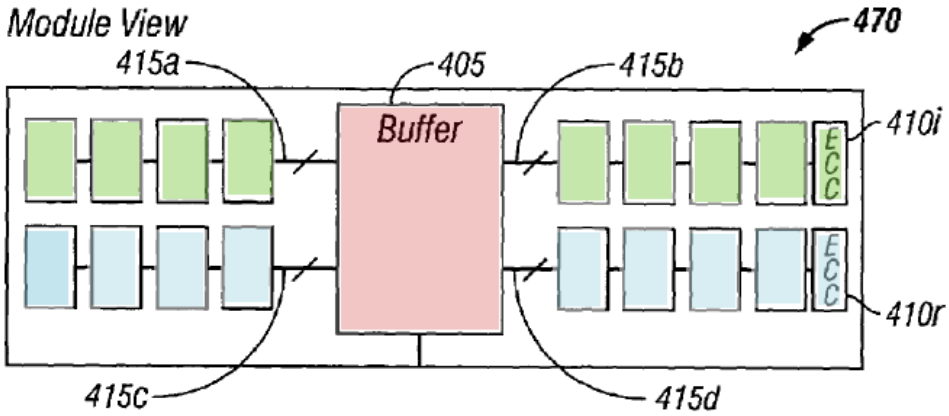


FIG. 4C

211. Perego discloses that "[a]ny number of channels 415a-415d, for example…two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations." EX1035, 21:16-20. As another example, "[b]uffer device 350 [or 391] … receives the data via one … of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a." *Id*. 6:15-24, Fig. 3C (below).

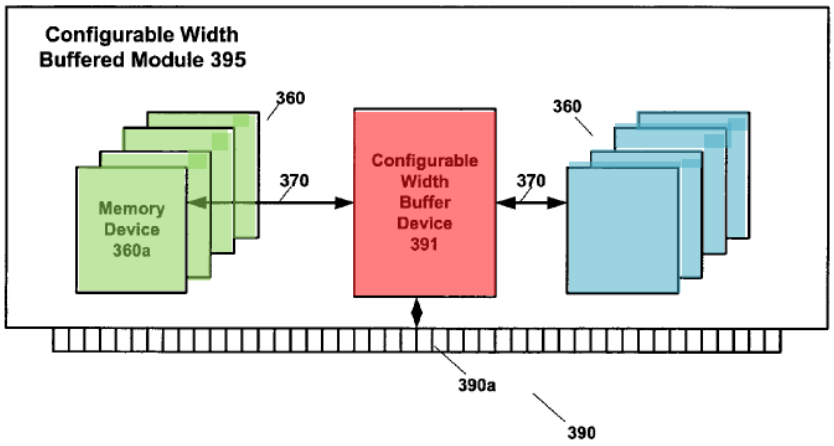


Fig. 3C

212. Thus, Perego teaches that the memory devices in each of the channels are enabled to output data in response to read commands independent of whether the memory devices in another channel are enabled or not. Also, as discussed above, *supra* ¶205, the memory devices are enabled for read and write operations by chip select signals. Therefore, Perego discloses that "*the first group of* [five] *DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output … DDR data signals … independently of whether the second group of* [four] *DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output … DDR data signals*."

213. Perego further discloses that each of the memory devices can be 8-bits wide ("x8"). EX1035, 14:10-15 ("For example, interfaces 520a and 520b may be programmed to connect to 16'x4' width memory devices, 8'x8' width memory devices or 4"x16" width memory devices."). In fact, 8-bit wide DDR SDRAM

memory devices were standardized. *See*, *e.g.*, EX1026 (JESD79-2B), pp.2 (DDR2 SDRAM x8 ballout), 7-8 (DDR2 SDRAM addressing for x4, x8 and x16 devices). Accordingly, when the five 8-bit wide memory devices in one channel, for example in channel 415b or 415d (FIG. 4C above), are enabled to output data by the "*first chip select signal*," they provide a total of 5x8 = "*40 1-bit DDR data signals in parallel*." EX1035, FIG. 4C (above). Similarly, when the four 8-bit wide memory devices in one channel, for example in channel 415a or 415c, are enabled by "*the second chip select signal*," they provide 4x8=32 "*1-bit DDR data signals in parallel*." *Id*.

214. In the implementation where "two channels 415c and 415d … transfer information simultaneously," the total number of data bits received by the buffer device is 72 bits (= 40 bits + 32 bits). EX1035, 21:16-20. Perego also discloses that the "Memory Device Access Width" (W_A) can be the same as the "Buffer Device Interface Width" (W_{DP}), which corresponds to a serialization ratio of one-to-one (R_S=W_A:W_{DP}). *Id*., 14:32-51, 17:26-28 ("For the embodiment illustrated by FIG. 5C, the serialization ratio is 1:1."). For example, when channels 415c and 415d are accessed simultaneously and channel 415c has four x8 memories and channel 415d has five x8 memories, the 40 bits of data from channel 415d are output to the controller "*via at least 40 data lines of the set of data lines*," and the 32 bits of data from channel 415c are output to the controller "*via an integer*

Samsung Electronics Co., Ltd.
Ex. 1003, p. 150

number of [32] *data lines of the set of data lines*"—a total of 72 data lines. *Id*., Fig. 4C (above). Such 72-bit wide memory modules with 8-bit wide DDR2 SDRAMs were standard at the time. *See, e.g.*, EX1106, 10; EX1090, 24-32 (finding Perego compatible with JEDEC standards); EX1091, 28-37 (same).

10. [2.a.1]-[2.a.2] Data Storage Element

215. Ground 2 discloses "*the controller further includes: a data storage element* [e.g., a FIFO or similar buffer for writing data to nonvolatile memory] *configured to store a plurality of data bits* [e.g., corresponding to one or more pages to be written to nonvolatile memory]."

216. As discussed above with reference to claim element [1.c.5], *supra* ¶¶188-194, the proposed combination discloses that "*the controller is configured to perform, in response to the trigger signal, a write operation to write* [configuration/status] *data into the nonvolatile memory*." To perform such "*a write operation to write* [configuration/status] *data into the nonvolatile memory*" in an efficient way, a Skilled Artisan would have been motivated to implement in Ground 2 a temporary "*data storage element*," such as a FIFO or similar buffer, to organize the configuration/status data into blocks or pages which the nonvolatile memory was typically organized into, and to write those blocks or pages as units from that FIFO or similar buffer into the nonvolatile memory. Using such page

write operations reduces the number of write operations into the nonvolatile memory thereby increasing speed and efficiency as discussed below in detail.

217. A feature of "nonvolatile memory" is that it "may be erased and reprogrammed in units of memory referred to as blocks or pages." *See*, *e.g.*, EX1025 (Spiers), ¶[0036]; *see also* EX1110 (EEPROM datasheet), p.1 ("64 byte page"), p.6 ("Up to 64 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Note: Page write operations are limited to writing bytes within a single physical page."). "When writing a page of data, having a page address, the page is first erased and then data is written to the page." EX1025, ¶[0049]. Thus, a page write operation writes "*a plurality of data bits*" as a unit corresponding to the size of the page into the nonvolatile memory. *Id*. In Ground 2, the data to be stored in nonvolatile memory is about the status and configuration of the memory module and is meant for recovery and/or failure analysis. Thus, there is no need to store or access each byte of data separately—the status/configuration data can be stored and accessed more efficiently in pages for recovery and/or failure analysis. Organizing configuration/status data into pages requires temporary storage, such as a FIFO or similar buffer, before the pages are written as units into the nonvolatile memory. For example, Spiers teaches that, in case of a power failure, a "backup device processor writes the data to the FIFO," which is "*a data storage element*"

organized as a first-in-first out buffer having a size corresponding to the size of the page of the nonvolatile memory. *Id*., ¶¶[0036], [0050]. After collecting the configuration/status data into the FIFO, "the backup device processor reads the data from the FIFO" and writes the one or more pages of data into the non-volatile memory. *Id*.

218. A Skilled Artisan at the time would have been particularly motivated to write data into non-volatile memory in units of pages and to organize the data into such pages before the write operation, because a page write operation was a known, reliable technique to efficiently write a block of data into nonvolatile memory. *See*, *e.g.*, EX1025, ¶¶[0049]-[50]; EX1110, p.6. A Skilled Artisan would have also been motivated to implement a FIFO or similar buffer to collect configuration/status data that needs to be stored in nonvolatile storage in case of a power failure and use one or more page write operations to move entire pages of the collected data into nonvolatile storage instead of writing the data byte-by-byte individually into the nonvolatile storage which would require more write operations, thus more time, and would use more power. EX1025, ¶¶[0054]-[55] ("Referring now to FIG. 14, the operational steps performed by the backup device upon detection of a power failure are now described. … At block 788, the data is written to the data FIFO, and CRC values are generated during the write to the FIFO. At block 792, the page burst length is set to 512, indicating that 512 bytes of

data are included in each page when writing to the NVRAM. At block 796, the backup device processor sends a flash page write command. The data is then read from the FIFO, and written to the flash page RAM, as noted by block 800.").

219. Thus, Ground 2 discloses writing configuration and status data into nonvolatile memory in case of a power failure for the reasons discussed above with reference to claim element [1.c.5], and a Skilled Artisan would have been motivated to write such data into the nonvolatile memory by the well-known and efficient page write operations, which includes collecting the configuration/status data into "*a data storage element*," such as a FIFO or similar buffer, and writing one page of data at a time from the FIFO to the nonvolatile memory.

11. Claim 8

220. Ground 2 discloses "*claim 7, wherein the logic element is configured to perform a first read operation of the one or more read operations* [of claim 7] *by reading the first* [from [2.a.5], e.g., a first set of configuration/status information for recovery or fault analysis, such as "a first value that represents the desired width of [Perego's] configurable width interface 590 [coupled to the system memory controller]," EX1035, 16:13-21] *and second sets of data bits* [from [2.a.6], e.g., a second set of configuration/status information for recovery or fault analysis, such as "a second value that represents the desired width of [Perego's] interfaces 520a and 520b [coupled to the memory devices]," EX1035, 16:13-21, or

driver settings for these interfaces, EX1027 (JESD82-20), 141] *from the first and second groups of DDR SDRAM devices*" for the reasons discussed above for [1.c.5], *supra* ¶¶188-194, and because it would have been obvious to store configuration/status information in "*the first and second groups of DDR SDRAM devices*" of Perego before and in preparation for potential backup operations, and read that configuration/status information from the DDR SDRAM devices and write them into nonvolatile memory in case of a backup operation, as discussed below in detail.

221. For example, Amidi explains that "as systems become more mission critical, the possibility of irreplaceable data being stored in volatile memory increases. Similarly, failure analysis can be much simpler if information about the state of a system is available after a failure occurs. Moreover, some data may be useful for restarting a system after a failure, even though that information is not otherwise vital for external purposes. Also, some data may simply be desirable for retention purposes, but may also be most useful in volatile memory." EX1024, 1:19-27. Thus, Amidi teaches that, at least some data about the configuration/status of a system for recovery and failure analysis may be stored in volatile memory, which includes "*the first and second groups of DDR SDRAM devices*" of Perego in the proposed combination. Also, Perego's DDR SDRAM devices provide a large capacity and fast storage to collect and store efficiently

even larger amount of configuration/status data for recovery and failure analysis at a single location which can be readily accessed in the proposed combination in case of power failure. The configuration/status data are read from the DDR SDRAM devices and then written into nonvolatile memory, such as those in Perego's operations circuit (572) or SPD memory, in case of a power failure for the reasons discussed above with reference to claim elements [1.c.5]. *Supra* ¶¶188-194.

222. Furthermore, "*the first and second sets of data bits*" are stored in "*the first and second groups of DDR SDRAM devices, respectively*" because storing different pieces of configuration/status information in respective locations of the memory device is a simple design choice.

12. Claim 13

223. Ground 2 discloses "*when* [+12V] *power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold* [e.g., under the ***Second Interpretation*** discussed above, *supra* ¶135, when the input voltage is ***within*** a normal operating range, e.g., +/−15% of the +12V; or, under the ***Third Interpretation*** above, *id*. ¶136, when the input voltage is ***outside*** a normal operating range]*; and wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and*

transmit a second trigger signal [e.g., a signal similar to Amidi's "signal 670" causing to select "system supply 605" under the ***Second Interpretation*** or to select "battery power 650" under the ***Third Interpretation***, *see* EX1024, 4:44-55]."

224. Under the ***Second Interpretation*** (consistent with Netlist's reading) discussed above, *supra* ¶135, the "first" and "second threshold" may represent the lower and upper limit of a normal operating range, respectively, in which case "an additional trigger condition" occurs when the input voltage is ***within*** the normal range (i.e., ***above*** *the first threshold* [**the lower** limit] ***and below*** *the second threshold* [**the upper** limit]). Under this interpretation, Ground 2 discloses this limitation for the reasons discussed above with reference to claim elements [1.c.3] and [1.c.5]. *Supra* ¶¶186-187, 188-194. For example, in the combination, a normal operating range for the purpose of detecting a power failure can be set as "+/−15%" of the 12V input supply as discussed above. *Supra* ¶¶186-187. And Amidi teaches that the memory module restarts normal operations once the power is restored. EX1024, 1:23-25 ("some data may be useful for restarting a system after a failure"), Fig.15 (below), 8:62-9:2 ("Process 1500 includes…detecting potential restoration, checking whether a system is ready, and restoring control to the system."), 9:8-10, 4:44-55 ("Signal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two. If system supply 605 has a greater magnitude than reference

voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660."), Fig.6; EX1023, ¶[0013].

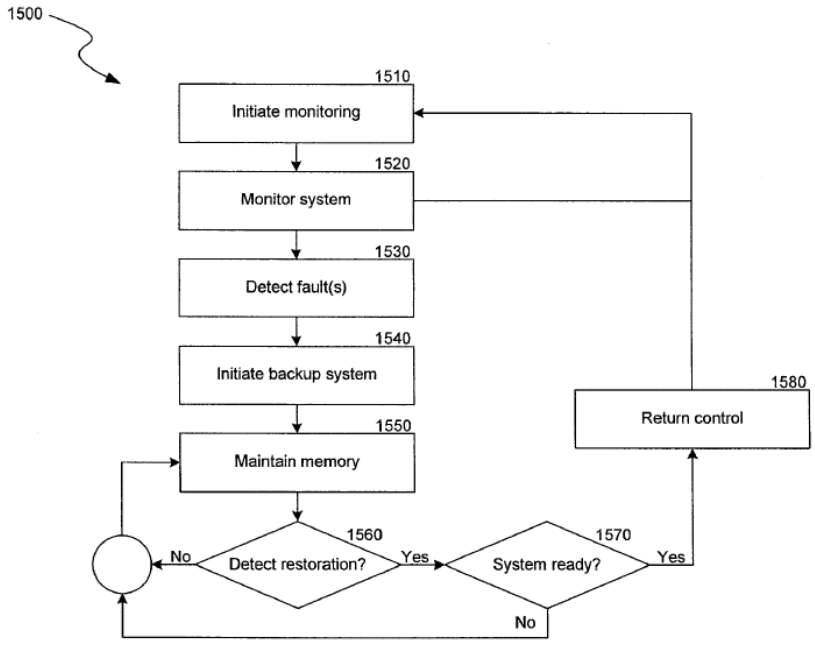


FIG. 15

In the proposed combination, detecting "potential restoration" happens after the voltage monitor circuit detects the return to normal voltage levels and generates a "*second trigger signal*" to indicate to the rest of the module that control can be returned to the system. EX1024, Fig.15 (above), 8:62-9:2.

225. Under the ***Third Interpretation*** (consistent with the specification) discussed above—where "*an additional trigger condition*" occurs when the input voltage is ***outside*** a normal operating range, *supra* ¶136—Ground 2 discloses this limitation for the reasons discussed above with reference to claim elements [1.c.3] and [1.c.5]. *Supra* ¶¶186-187, 188-194; *see, e.g.*, EX1023, ¶[0013] ("Further,

since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated"); EX1024, 9:8-10 ("the system is monitored, with power … signals checked for proper levels"); 4:44-55 ("If system supply 605 has a magnitude lower than reference voltage 675, then signal 670 causes power switch multiplexer 655 to choose battery power 650 as a source for memory supply 660."), Fig.6.

13. [16.c.5]

226. Claim limitation [16.c.5] requires "*wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element*."

227. Claim limitation [16.c.5] is very similar to claim limitations [1.c.5], [2.a.4], and [2.a.5] as shown by the comparison below:

Claims 1, 2	Claim 16
[1.c.5] wherein the controller is configured to perform, in response to the trigger signal, a write operation …, and **[2.a.4]** wherein the write operation conducted by the controller in response to the trigger signal includes: **[2.a.5]** a first write operation to write a first set of data bits into a first portion of the data storage element;	**[16.c.5]** wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

228. Furthermore, as explained below, Ground 2 discloses using a FIFO or similar buffer of the size of one page in the nonvolatile memory, and to have the "*controller … configured to periodically perform, at regular intervals of time* [corresponding to a time interval, such as an "Internal Write Cycle Time," required to write one page of data before writing a next page into the nonvolatile memory from the FIFO or similar buffer], *a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element* [e.g., including write operations to collect one page of configuration/status data into the FIFO or similar buffer and the page write operation of writing the collected one page of data into the nonvolatile memory]."

229. As discussed above with reference to claim 2, *supra* ¶¶215-219, Ground 2 discloses using a temporary "*data storage element*" such as a FIFO or

similar buffer to organize the configuration/status data into blocks or pages which the nonvolatile memory was organized into, and to write those blocks or pages as units from that FIFO or similar buffer into the nonvolatile memory. Furthermore, as discussed above, *supra* ¶¶215-219, the size of the FIFO or similar buffer would correspond to one page of the nonvolatile memory, and one page at a time would be written from the FIFO to the non-volatile memory, because that allows using the efficient page writing feature of the nonvolatile memory without a large sized FIFO or similar buffer.

230. Also, a page write operation into the nonvolatile memory would take a predefined time interval before a subsequent write operation could be started. *See*, *e.g.*, EX1049 (Flash datasheet), p.1 ("Write performance: Page program: 300µs (TYP)"), p.41 ("Page program time tPROG 300 [Typ] 700 [Max] µs"); EX1110 (EEPROM datasheet), p.1 ("Self-timed ERASE and WRITE cycles (5ms max.)"), p.4 ("TWC Internal Write Cycle Time – 5 ms [Max]"). Therefore, when writing multiple pages of configuration/status data into the nonvolatile memory, Ground 2 discloses writing one page at a time into the nonvolatile memory periodically at a regular interval of time which corresponds to the internal write cycle of the nonvolatile memory, and refilling the FIFO or similar buffer with the next page of configuration/status data during that time interval.

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231. Thus, for the same reasons as with claim limitations [1.c.5], [2.a.4], and [2.a.5], Grounds 2 discloses this limitation.

14. [19.a.3]

232. Claim limitation [19.a.3] requires "*wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.*"

233. Claim limitation [19.a.3] is very similar to claim limitations [16.c.5], [2.a.6], and [2.a.7] as shown by the comparison below:

Claims 2 and 16	**Claim 19**
[16.c.5] wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element; **[2.a.6]** a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently **[2.a.7]** a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory,	**[19.a.3]** wherein, in response to the detected trigger condition, the logic element [included in the controller of claim 17] is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

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234. Furthermore, as discussed above with reference to claim element [16.c.5] and claim 2, *supra* ¶¶226-231, 215-219, the proposed combination teaches "*to periodically perform, at regular intervals of time, a plurality of write operations*" in order to write multiple pages of configuration/status data into the nonvolatile memory one page at a time, each page of data being collected into a FIFO or similar buffer having a size of one-page. Thus, each page write cycle includes "*the first and second write operations* [of configuration/status data pieces into the FIFO or similar buffer] *followed by the third write operation* [of the entire page from the FIFO or similar buffer into the nonvolatile memory]." As also discussed above with reference to claim element [16.c.5], *supra* ¶¶226-231, the "*regular intervals of time*" corresponds to the page write cycle of the nonvolatile memory, which is on the order of one millisecond depending on the specific implementation (e.g., between 300 µs and 5 ms). *See, e.g.*, EX1049 (Flash datasheet), p.1 ("Write performance: Page program: 300µs (TYP)"), p.41 ("Page program time tPROG 300 [Typ] 700 [Max] µs"); EX1110 (EEPROM datasheet), p.1 ("Self-timed ERASE and WRITE cycles (5ms max.)"), p.4 ("TWC Internal Write Cycle Time – 5 ms [Max]"). It would have been a simple design choice to choose a specific nonvolatile memory and a corresponding write cycle time that allows "*to periodically perform every millisecond*" a page write operation into the nonvolatile memory, because nonvolatile memories with page write cycle around

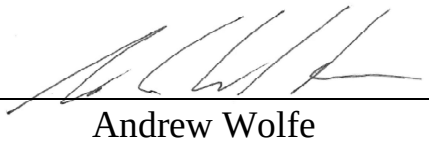
one millisecond were available. For example, a page write operation can be safely performed "*every millisecond*" into a nonvolatile memory with a write cycle time somewhat less than 1 ms in order to allow for potential timing issues, such as delays and skews.

235. Thus, for the same reasons as with claim limitations [16.c.5], [2.a.6], and [2.a.7], Grounds 2 discloses this limitation.

* * *

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: November 7, 2025



Andrew Wolfe

EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 12,373,366
1002	File History of U.S. Patent No. 12,373,366 (Application No. 17/582,797), *available at* <https://patentcenter.uspto.gov/applications/17582797/ifw/docs?application=>
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	File History of U.S. Provisional Application No. 60/941,586
1006	File History of U.S. Patent Application No. 12/131,873
1007	File History of U.S. Patent Application No. 12/240,916
1008	File History of U.S. Provisional Application No. 61/512,871
1009	File History of U.S. Patent Application No. 13/559,476
1010	File History of U.S. Patent Application No. 14/489,269
1011	File History of U.S. Patent Application No. 14/840,865
1012	File History of U.S. Patent Application No. 15/934,416
1013	File History of U.S. Patent Application No. 17/138,766
1014	*SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper No. 1 (PTAB June 20, 2014) (833 Patent IPR Petition)
1015	*SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper No. 8 (PTAB December 16, 2014) (833 Patent Institution Decision)
1016	*Smart Modular Techs. Inc. v. Netlist, Inc.*, IPR2014-01370, Paper No. 8 (PTAB September 22, 2014) (833 Patent IPR Corrected Petition)

Exhibit #	Description
1017	*Smart Modular Techs. Inc. v. Netlist, Inc.*, IPR2014-01370, Paper No. 13 (PTAB March 13, 2015) (833 Patent Institution Decision)
1018	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00649, Paper No. 1 (PTAB January 13, 2017) (833 Patent IPR Petition)
1019	*SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00649, Paper No. 7 (PTAB July 24, 2017) (833 Patent Institution Decision)
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1023	U.S. Patent Application Publication No. 2006/0174140 to Harris *et al.*
1024	U.S. Patent No. 7,724,604 to Amidi *et al.*
1025	U.S. Patent Application Publication No. 2006/0080515 to Spiers *et al.*
1026	JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (January 2005) ("JESD79-2B")
1027	JEDEC Standard, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20 (March 2007) ("JESD82-20")
1028	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification, JESD205 (March 2007) ("JESD205")
1029	Declaration of Julie Carlson for JESD82-20 and JESD205
1030	U.S. Patent No. 7,719,866 to Boldo

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1032	Mohan et al., Power Electronics: Converters, Applications, and Design (2d Ed. 1995)
1033	U.S. Patent No. 7,721,130 to Prete *et al.*
1034	U.S. Patent No. 6,798,709 to Sim *et al.*
1035	U.S. Patent No. 7,363,422 to Perego *et al.*
1036	U.S. Patent No. 7,155,627 to Matsui
1037	U.S. Patent Application Publication No. 2008/0238536 to Hayashi *et al.*
1038	U.S. Patent No. 6,856,556 to Hajeck
1039	U.S. Patent Application Publication No. 2010/0257304 to Rajan *et al.*
1040	Texas Instruments, TPS51020 Datasheet (December 2003)
1041	Fairchild Semiconductor, FAN5026 Datasheet (October 2005)
1042	Murata Power Supply Reference Guide for Xilinx FPGAs (September 2006)
1043	Murata Power Supply Reference Guide for Altera FPGAs (February 2008)
1044	U.S. Patent Application Publication No. 2010/0205470 to Moshayedi *et al.*
1045	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) (“JESD79”)
1046	JEDEC Standard, DDR3 SDRAM, JESD79-3A (September 2007) (“JESD79-3A”)
1047	U.S. Patent No. 7,023,187 to Shearon *et al.*

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1048	Murata, DC-DC Converter Specification (DRAFT), MPD4S014S Datasheet (January 21, 2008)
1049	Micron, NAND Flash Memory Datasheet (January 2006)
1050	U.S. Patent No. 7,692,938 to Petter
1051	U.S. Patent Application Publication No. 2003/0090879 to Doblar *et al.*
1052	File History of U.S. Patent No. 11,232,054 (EX1002 in IPR2022-00999)
1053	U.S. Patent No. 11,232,054 (EX1001 in IPR2022-00999)
1054	U.S. Patent No. 11,016,918
1055	U.S. Patent Application Publication No. 2008/0101147 to Amidi
1056	U.S. Patent No. 5,563,839 to Herdt *et al.*
1057	U.S. Patent No. 6,693,840 to Shimada *et al.*
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1061	Analog Devices, ADM1066 Datasheet (2006)
1062	Alan Moloney, *Power-Supply Management—Principles, Problems, and Parts*, Analog Dialogue (May 2006)
1063	National Semiconductor, LMC6953 PCI Local Bus Power Supervisor Datasheet (October 1996)
1064	U.S. Patent Application Publication No. 2007/0136523 to Bonella *et al.*

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1065	U.S. Patent Application Publication No. 2009/0034354 to Resnick
1066	U.S. Patent No. 10,672,458 to Shaeffer *et al.*
1067	LatticeXP Family Data Sheet (March 2006)
1068	Declaration of Dr. Andrew Wolfe in IPR2022-00996 (EX1003 in IPR2022-00996)
1069	Declaration of Dr. Andrew Wolfe in IPR2022-00999 (EX1003 in IPR2022-00999)
1070	Final Written Decision, *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00996, Paper 49 (PTAB Dec. 6, 2023) (U.S. Patent No. 11,016,918)
1071	Final Written Decision, *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00999, Paper 51 (PTAB Dec. 5, 2023) (U.S. Patent No. 11,232,054)
1072	Order Denying Director Review, *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00996 and -00999 (PTAB Mar. 18, 2024)
1073	Notice of Docketing, *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 2024-1859 (Fed. Cir. May 23, 2024) (appeal from IPR2022-00996 of U.S. Patent No. 11,016,918)
1074	Notice of Docketing, *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 2024-1863 (Fed. Cir. May 23, 2024) (appeal from IPR2022-00999 of U.S. Patent No. 11,232,054)
1075	Transcript of deposition of William Mangione-Smith, Ph.D. in IPR2022-00996 and -00999 (June 12, 2023)
1076	Transcript of deposition of Andrew Wolfe, Ph.D. (March 16–17, 2023) (EX2030 in IPR2022-00996 and EX2060 in IPR2022-00999)
1077	Netlist's Technology Tutorial
1078	Datasheet for ADP1821 Step-Down DC-to-DC Controller

Exhibit #	Description
1079	Petitioner's Demonstratives for Oral Argument on September 11, 2023 in IPR2022-00996 and IPR2022-00999
1080	Romo, Joaquin, *DDR Memories: Comparison and overview*, NXP technical note, downloaded from https://www.nxp.com/docs/en/supporting-information/BeyondBits2article17.pdf (last access 09/08/2022). As downloaded the file shows the following meta data: (EX2012 in IPR2022-00996 and IPR2022-00999)
1081	EURESYS, PCI Bus Variation Technical Note (2006), downloaded from https://documentation.euresys.com/Products/MULTICAM/MULTICAM/Content/MultiCam_6_7_HTML_Documentation/PCI_Bus_Variation.pdf (last accessed 09/08/2022) (EX2016 in IPR2022-00996 and IPR2022-00999)
1082	PCI Technology Overview (Feb. 2003) downloaded from https://web.archive.org/web/20040721012143/http://www.cs.unc.edu/Research/stc/FAQs/pci-overview.pdf (Wayback Machine (archive.org)) (last visited 09/08/2022) (EX2029 in IPR2022-00996 and IPR2022-00999)
1083	Claim Construction Order, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463, ECF No. 114 (E.D. Tex. Dec. 14, 2022) (EX2032 in IPR2022-00996 and IPR2022-00999)
1084	Netlist Presentation (excerpt) (EX2035 in IPR2022-00996 and IPR2022-00999)
1085	Intel, ATX12V, Power Supply Design Guide, Version 2.2 (March 2005), downloaded from https://web.archive.org/web/20070403181612/http://www.formfactors.org/developer/specs/ATX12V_PSDG_2_2_public_br2.pdf (EX2038 in IPR2022-00996 and IPR2022-00999)

Exhibit #	Description
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1087	Wolfe Deposition exhibit, FB-DIMM Design Considerations (Feb. 18, 2004) (EX2101 in IPR2022-00996 and IPR2022-00999)
1088	Final Written Decision, *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00418, Paper 30 (PTAB Aug. 28, 2023) (U.S. Patent No. 8,301,833)
1089	U.S. Patent No. 8,301,833
1090	Final Written Decision, *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00454, Paper 45 (PTAB July 30, 2024) (U.S. Patent No. 11,093,417)
1091	Final Written Decision, *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00455, Paper 45 (PTAB July 30, 2024) (U.S. Patent No. 9,858,215)
1092	Order Denying Director Review, *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00454 and -00455 (PTAB Oct. 8, 2024)
1093	Notice of Docketing, *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 2025-1286 (Fed. Cir. Dec. 16, 2024) (appeal from IPR2023-00455 of U.S. Patent No. 9,858,215)
1094	Notice of Docketing, *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 2025-1296 (Fed. Cir. Dec. 17, 2024) (appeal from IPR2023-00454 of U.S. Patent No. 11,093,417)
1095	Samsung's Principal Brief, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2024-2203 (Fed. Cir. Dec. 16, 2024)
1096	Netlist's Responsive Brief, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2024-2203 (Fed. Cir. Mar. 28, 2025)

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1097	Samsung's Reply Brief, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2024-2203 (Fed. Cir. May 19, 2025)
1098	Proposed Amended Complaint in *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:25-cv-00626 (D. Del. filed Aug. 1, 2025) (U.S. Patent No. 12,373,366)
1099	Complaint in *Micron Technology, Inc. et al. v. Netlist, Inc.*, No. 1:25-cv-00942 (D. Del. Filed July 29, 2025) (U.S. Patent No. 12,373,366)
1100	Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:25-cv-00748 (E.D. Tex. July 28, 2025) (U.S. Patent No. 12,373,366)
1101	Complaint in *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:25-cv-00749 (E.D. Tex. July 28, 2025) (U.S. Patent No. 12,373,366)
1102	[omitted]
1103	[omitted]
1104	JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002)
1105	Declaration of Julie Carlson re: JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002)
1106	JEDEC JESD21-C design specification for DDR2 SDRAM Registered DIMM, Rev. 3.2 (Oct. 4, 2005), *available at* <http://web.archive.org/web/20060912004633/http://www.jedec.org:80/Catalog/display.cfm>, <http://web.archive.org/web/20061002003035/http://www.jedec.org/download/search/4_20_10R15.pdf>, <http://web.archive.org/web/20061002003035if_/http://www.jedec.org/download/search/4_20_10R15.pdf>
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1108	U.S. Patent. No. 5,513,135 to Dell *et al.*

Exhibit #	Description
1109	Advanced Configuration and Power Interface (ACPI) Specification, Revision 2.0 (2000), *available at* <https://web.archive.org/web/20030921001001fw_/http://www.o3one.org/hwdocs_index.html>, <https://web.archive.org/web/20030921001001fw_/http://www.o3one.org/hwdocs/acpi/ACPIspec20.pdf>, <https://uefi.org/sites/default/files/resources/ACPI_2.pdf>
1110	Microchip 25LC256 EEPROM datasheet (2003), *available at* <https://web.archive.org/web/20041130175640/http://www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=1335&dDocName=en010846>, <https://web.archive.org/web/20040805021246/http://ww1.microchip.com/downloads/en/DeviceDoc/21822c.pdf>, <https://web.archive.org/web/20040805021246if_/http://ww1.microchip.com:80/downloads/en/DeviceDoc/21822c.pdf>
1111	[omitted]
1112	Complaint, *In the Matter of Certain Dynamic Random Access Memory (DRAM) Devices, Products Containing the Same, and Components Thereof*, Inv. No. 337-TA-3854 (USITC filed Sept. 30, 2025) (U.S. Patent No. 12,373,366)
1113	Invalidity claim chart by Dr. Andrew Wolfe

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a.1	A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,
1.a.2	the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,
1.a.3	wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and
1.a.4	address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:
1.b.1	a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:
1.b.2	a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits,
1.b.3	wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;
1.b.4	a second set of edge connections configured to be electrically connected to the set of data conduits, and
1.b.5	a third set of edge connections configured to be electrically connected to the set of address and control conduits,
1.b.6	a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,
1.b.7	a set of data lines electrically connected to the second set of edge connections, and
1.b.8	a set of address and control lines electrically connected to the third set of edge connections;
1.c.1	a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:
1.c.2	(i) monitor an input voltage supplied via the input voltage supply line;

Ref. #	Listing of Challenged Claims
1.c.3	(ii) generate a trigger signal upon detecting a trigger condition; and
1.c.4	(iii) transmit the trigger signal to at least one other portion of the controller,
1.c.5	wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and
1.c.6	wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;
1.d.1	a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,
1.d.2	the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and
1.e	first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,
1.f.1	wherein the set of components includes:
1.f.2	a first component configured to receive power via at least the first regulated voltage line;
1.f.3	a second component configured to receive power via at least the second regulated voltage line;
1.f.4	a third component configured to receive power via at least the third regulated voltage line; and
1.f.5	a fourth component configured to receive power via at least the fourth regulated voltage line;
1.g.1	wherein each component of the set of components:
1.g.2	(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
1.g.3	(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines,
1.h.1	wherein the plurality of DDR SDRAM devices includes:

Ref. #	Listing of Challenged Claims
1.h.2	a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;
1.h.3	a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;
1.i.1	wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:
1.i.2	the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;
1.i.3	the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and
1.j.1	wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and
1.j.2	the total number of data conduits is at least 72 data conduits.
2.a.1	The DIMM of claim 1, wherein the controller further includes:
2.a.2	a data storage element configured to store a plurality of data bits and
2.a.3	a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and
2.a.4	wherein the write operation conducted by the controller in response to the trigger signal includes:
2.a.5	a first write operation to write a first set of data bits into a first portion of the data storage element;
2.a.6	a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

Ref. #	Listing of Challenged Claims
2.a.7	a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory,
2.a.8	wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.
3	The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations.
4	The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.
5	The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.
6	The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.
7	The DIMM of claim 2, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger signal, one or more read operations.
8	The DIMM of claim 7, wherein the logic element is configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.
9.a.1	The DIMM of claim 2, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and

Ref. #	Listing of Challenged Claims
9.a.2	wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.
10	The DIMM of claim 2, wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.
11	The DIMM of claim 1, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.
12	The DIMM of claim 1, wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when power from the power rails of the system board is provided to the DIMM.
13.a.1	The DIMM of claim 12, wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and
13.a.2	wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.
14	The DIMM of claim 1, wherein, when power from the power rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.
15	The DIMM of claim 1, wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.
16.a.1	A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,
16.a.2	the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,
16.a.3	wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and
16.a.4	address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

Ref. #	Listing of Challenged Claims
16.b.1	a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:
16.b.2	a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the system board via the set of power conduits,
16.b.3	wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,
16.b.4	a second set of edge connections configured to be electrically connected to the set of data conduits,
16.b.5	a third set of edge connections configured to be electrically connected to the set of address and control conduits,
16.b.6	a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,
16.b.7	a set of data lines electrically connected to the second set of edge connections, and
16.b.8	a set of address and control lines electrically connected to the third set of edge connections;
16.c.1	a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:
16.c.2	(i) monitor an input voltage supplied via the input voltage supply line;
16.c.3	(ii) generate a trigger signal upon detecting a trigger condition; and
16.c.4	(iii) transmit the trigger signal to at least one other portion of the controller,
16.c.5	wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

Ref. #	Listing of Challenged Claims
16.d.1	a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,
16.d.2	the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and
16.e	first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,
16.f.1	wherein the set of components includes:
16.f.2	a first component configured to receive power via the first regulated voltage line;
16.f.3	a second component configured to receive power via the second regulated voltage line;
16.f.4	a third component configured to receive power via the third regulated voltage line; and
16.f.5	a fourth component configured to receive power via the fourth regulated voltage line;
16.g.1	wherein each component of the set of components:
16.g.2	(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines;
16.g.3	(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and
16.h.1	wherein the plurality of DDR SDRAM devices includes:
16.h.2	a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;
16.h.3	a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

Ref. #	Listing of Challenged Claims
16.i.1	wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:
16.i.2	the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and
16.i.3	the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and
16.j.1	wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and
16.j.2	the total number of data conduits is at least 72 data conduits.
17	The DIMM of claim 16, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.
18	The DIMM of claim 17, wherein the logic element is configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.
19.a.1	The DIMM of claim 18, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory,
19.a.2	wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and
19.a.3	wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

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20	The DIMM of claim 19, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.
21.a.1	The DIMM of claim 19, wherein the logic element is configured to perform the third write operation by writing the third set of data bits from the data storage element into the nonvolatile memory, and
21.a.2	wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.
22	The DIMM of claim 19, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on the groups of data bits stored in the data storage element.
23.a.1	The DIMM of claim 19, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and
23.a.2	wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.
24	The DIMM of claim 18, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.
25	The DIMM of claim 16, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.
26	The DIMM of claim 16, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

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27	The DIMM of claim 26, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.
28.a	The DIMM of claim 26, wherein when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and
28.b	wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.
29.a.1	A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,
29.a.2	the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,
29.a.3	wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and
29.a.4	address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:
29.b.1	a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector, the PCB including:
29.b.2	a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits,
29.b.3	wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,
29.b.4	a second set of edge connections configured to be electrically connected to the set of data conduits,
29.b.5	a third set of edge connections configured to be electrically connected to the set of address and control conduits,
29.b.6	a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

Ref. #	Listing of Challenged Claims
29.b.7	a set of data lines electrically connected to the second set of edge connections, and
29.b.8	a set of address and control lines electrically connected to the third set of edge connections,
29.b.9	wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection,
29.b.10	wherein each data line of the set of data lines is configured to electrically conduct a 1-bit DDR data signal;
29.c.1	a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:
29.c.2	(i) monitor an input voltage supplied via the input voltage supply line;
29.c.3	(ii) generate a trigger signal upon detecting a trigger condition; and
29.c.4	(iii) transmit the trigger signal to at least one other portion of the controller,
29.c.5	wherein the controller is configured to perform, in response to the trigger signal, one or more write operations to write data into the data storage element;
29.d.1	a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,
29.d.2	the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and
29.e	first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,
29.f.1	wherein the set of components includes:
29.f.2	a first component configured to receive power via the first regulated voltage line;
29.f.3	a second component configured to receive power via the second regulated voltage line;

Ref. #	Listing of Challenged Claims
29.f.4	a third component configured to receive power via the third regulated voltage line; and
29.f.5	a fourth component configured to receive power via the fourth regulated voltage line;
29.g.1	wherein each component of the set of components:
29.g.2	(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
29.g.3	(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines;
29.h.1	wherein the plurality of DDR SDRAM devices includes:
29.h.2	a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; and
29.h.3	a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal, and
29.i.1	wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:
29.i.2	the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and
29.i.3	the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and
29.j.1	wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and
29.j.2	the total number of data conduits is at least 72 data conduits.

Ref. #	Listing of Challenged Claims
30	The DIMM of claim 29, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.
31	The DIMM of claim 29, wherein when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.
32	The DIMM of claim 29, when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.
33	The DIMM of claim 32, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.
34.a	The DIMM of claim 32, wherein, when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and
34.b	wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.
35.a.1	The DIMM of claim 29, wherein the controller further includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and
35.a.2	the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to wire a second set of data bits into a second portion of the data storage element.
36.a.1	The DIMM of claim 35, wherein the logic element is configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and
36.a.2	wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

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37	The DIMM of claim 35, wherein the logic element is configured to perform, prior to the first and second write operations, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.
38	The DIMM of claim 29, wherein each of the first, second, and third converter circuits is a buck converter.

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Ex. 1003, p. 187