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Paper 48
Date: February 9. 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00639
Patent 10,949,339 B2

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

JURGOVAN, *Administrative Patent Judge*.

DECISION
Denying Patent Owner's Request on Rehearing of Final Written Decision
37 C.F.R. 42.71(d)

[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00204 and have been joined as petitioners to this proceeding. *See* Paper 33.

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Samsung") filed a Petition (Paper 1, "Pet.") for *inter partes* review of claims 1–35 ("challenged claims") of U.S. Patent 10, 949,339 B2 (Ex. 1001, "the '339 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7) to the Petition. Samsung filed an authorized Preliminary Reply (Paper 13), and Patent Owner filed an authorized Preliminary Sur-Reply (Paper 14). We instituted *inter partes* review under 35 U.S.C. § 314(a). Paper 15 ("Inst. Dec.").

During the trial, Patent Owner filed a Response (Paper 27, "PO Resp."), Petitioner filed a Reply (Paper 31, "Pet. Reply"), and Patent Owner filed a Sur-Reply (Paper 36, "PO Sur-Reply"). We joined Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC as petitioners in this proceeding, and we refer to Samsung and these entities collectively as "Petitioner." *See* Paper 33.

We entered a Final Written Decision determining all challenged claims unpatentable. Paper 45 ("Final Dec."). Patent Owner filed a Request for Rehearing (Paper 47, "Req. Reh'g") pursuant to 37 C.F.R. § 42.71(d), which we now consider.

A party is permitted to file a single request for rehearing of a final written decision. 37 C.F.R. § 42.71(d). "The burden of showing a decision should be modified lies with the party challenging the decision." *Id.* "The request must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed." *Id.*

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We determine that Patent Owner's assertions do not show that the Board misapprehended or overlooked any matters, and we deny Patent Owner's Request for Rehearing for the following reasons.

II. ANALYSIS

Patent Owner alleges that the Final Written Decision misapprehended or overlooked the following: (A) Ellsberry "activates" and "disables" one port by disabling devices, not data paths (Req. Reh'g 1–4); (B) Halbert and the general knowledge of JEDEC do not fix this gap in Ellsberry (*id.* at 4–8); (C) Patent Owner's arguments for why the prior art did not teach using a latency parameter to enable a write data path (*id.* at 8–11); and (D) there is no motivation to enable data paths during a write (*id.* at 11–15). We address Petitioner's arguments sequentially below.

A. Ellsberry's Alleged Enabling and Disabling of Devices and Not Data Paths

Patent Owner argues that Ellsberry's switch ASICs are always enabled, contrary to the claims. Req. Reh'g 1. Patent Owner contends that the Board misread Ellsberry's so-called "one port disabled" embodiment as using the switch ASICs to enable or disable data paths to respective banks of memory devices. *Id.* (citing Final Dec. 39–40; Pet. 73–74; Ex. 1005 ¶¶ 30–31, 40, Figs. 2, 4). According to Patent Owner, the Board overlooked Patent Owner's argument that Ellsberry says nothing about disabling or enabling data paths in the cited paragraphs. *Id.* (citing PO Resp. 13, 21, 41–43; PO Sur-Reply 17–21).

At the outset, we note that a rehearing request is not an opportunity for the requesting party to reargue its case, present new arguments, or express disagreement with the Final Written Decision. We considered

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Patent Owner's arguments and evidence in rendering the Final Written Decision. PO Resp. 13, 21, 41–43; PO Sur-Reply 11–15, 17–21; Final Dec. 39–40; Ex. 1005 ¶¶ 30–31, 40, Figs. 2, 4; Ex. 1003 ¶¶ 231, 358. Even considering Patent Owner's repeat and new arguments in the Request for Rehearing, we are not swayed to modify our Final Written Decision.

Patent Owner's arguments confuse and selectively consider different Ellsberry embodiments. In the so-called "one port disabled" embodiment, the control unit controls the memory bank switches (switch ASICS) to enable one port and disable the other so that data is written to the correct memory bank. Ex. 1005 ¶¶ 31, 40. As we explained in our Final Written Decision, enabling a port means that the data path through the port is enabled, and disabling a port means that the data path through that port is disabled. Final Dec. 39–40. Thus, Patent Owner's argument that the data paths through the switch ASICs are always enabled is incorrect concerning Ellsberry's "one port disabled" embodiment. Req. Reh'g 1.

Distinct from the "one port disabled" embodiment, Ellsberry has an "always on" or "no ports disabled" embodiment with two modes of operation. Ex. 1005 ¶ 33. Column mode operation sends write-data to both ports of the memory bank switch and the control unit uses a data mask signal to select the target memory device. *Id.* Row/bank mode sends read or write commands only to the targeted memory device and sends a NOP (no-operation) to the non-targeted memory device. *Id.* ¶¶ 33, 40. Ellsberry explains that in these two modes "the control unit and switch architecture can control data to and from the memory banks without the delays caused by otherwise disabling the banks." *Id.* ¶ 42. As described in Ellsberry, the

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"always on" or "no ports enabled" embodiment is distinct from the "one port disabled" embodiment.

Accordingly, Patent Owner's and Dr. Brogioli's explanations of how Ellsberry operates with a memory bank switch (switch ASIC) with "always on" enabled ports may be correct for the embodiment with column and row/bank modes of operation (Req. Reh'g 1–4), but it is not for the "one port disabled" embodiment, which enables or disables data paths through the ports under control of the control unit. Although Patent Owner argues about what exactly is inside of Ellsberry's switch ASICs that performs enabling and disabling (e.g., pin drivers, FET switches, etc.), we clearly indicated that the evidence at trial showed that the signal drivers 402, 404 perform this function. Final Dec. 40–42. Patent Owner also focuses on its attacks on Ellsberry individually and loses sight of Petitioner's combination of Ellsberry with Halbert, which discloses a bidirectional buffer 122 and bi-directional data registers 126, 128 with tristate buffers to perform these functions. *Id.* at 42.

Patent Owner presents several other repeat and new arguments that are manifestly incorrect. Patent Owner erroneously equates ports of the memory bank switch (switch ASIC) with physical memory banks. Req. Reh'g 2. Ellsberry clearly shows Ports A and B as parts of the switch ASICs, not the physical memory banks. Ex. 1005, Fig. 2. Patent Owner argues that the control unit does not communicate with the switch ASICs. Req. Reh'g 2. Ellsberry discloses that the control unit communicates with the switch ASICs via control bus 210. Ex. 1005 ¶ 29, Fig. 2. Patent Owner argues that deactivating is not the same as disabling the data path through the switch ASIC as required by the claims. Req. Reh'g 2–3. Patent Owner

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made no such argument in its briefings, and, in any case, Ellsberry discloses disabling. PO Resp. 13 (Patent Owner stating that a port is disabled by deactivating it); Ex. 1005 ¶¶ 40–42. Nor do we agree with Patent Owner's repeated argument that disabling a port means disabling memory banks. Req. Reh'g 3–4. Disabling a port means disabling the data path through the memory bank switch (switch ASIC) that is connected to those memory banks. Ex. 1005 ¶ 31.

For at least the foregoing reasons, Patent Owner's arguments concerning Ellsberry's enabling or disabling of data paths are incorrect and unavailing.

B. Board's Alleged Gap Filling of Ellsberry with Halbert and JEDEC

Maintaining its erroneous argument that Ellberry's memory bank switches (switch ASICs) do not enable or disable data paths, Patent Owner repeats its argument during trial that, while Halbert has the capability to enable and disable data paths with its bidirectional buffer 122 and bidirectional data registers 126 and 128, it does not actually teach doing so because Halbert has "don't care" states before its write operations. Req. Reh'g 4–6. Patent Owner argues that "gap-filling" a reference with general knowledge in a JEDEC standard (Ex. 1011, 6, 22) is improper, that Petitioner did not rely on that general knowledge in its briefings, and that general knowledge is not a patent or printed publication under 35 U.S.C. § 311(b). Req. Reh'g 6–7.

Petitioner relied upon Ellsberry to teach enabling and disabling ports. *See, e.g.*, Pet. 73–75 (citing Ex. 1005 ¶¶ 31, 40, Fig. 2), 119, 134, 139–140. It would have been clear to a person of ordinary skill in the art considering

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Ellsberry that a port may be disabled before it is enabled during a write operation to the extent that is required in the claims. Pet. 79–81; Reply 23–26 (citing Ex. 1009, 17, 26; Ex. 1011, 22; Ex. 2007, 57:2–10, 28:15–29:2; Ex. 2010, 2; Ex. 1003 ¶¶ 352, 362). Ellsberry's memory bank switch (or switch ASIC) is after all a "switch" that enables one port and disables the other, and vice versa. Ex. 1005 ¶ 31. Thus, Ellsberry had no deficiency that required "gap-filling" by Petitioner.

Halbert's "don't care" state does not preclude disabling data paths before enabling them in a write operation according to Ellsberry. Pet. 80 (citing Ex. 1006, Fig. 6). Patent Owner relies on an application note (Ex. 2010) and datasheet (Ex. 2011) to show "don't care" states prior to a write operation. Req. Reh'g 6 (citing PO Resp. 46; Ex. 2010 3, 5–8; Ex. 2011, 13, Table 3). As Petitioner explained, however, when viewed in their entireties, the application note, datasheet, and the JEDEC standards all teach that the data paths should be placed in high-impedance states (disabled) when not performing a read or write operation. Pet. Reply 23–24 (citing Ex. 2010, 2; Ex. 1009, 17, 26; Ex. 1011, 22; Ex. 1003 ¶¶ 352, 362; Pet. 79–80; Ex. 1006, Figs. 3, 5, 6). The general knowledge reflected in the JEDEC standards relied on in the Petition, as well as the application note and datasheet, reinforce Petitioner's contention that the data paths would be disabled before they are enabled during a write operation. *See, e.g.*, Pet. 3, 16, 36, 54, 63, 76–77, 100, 103, 105, 116–117, 123, 144 (citing Ex. 1011, 6, 22). And contrary to Patent Owner's argument, the JEDEC standard (Ex. 1011) is a "printed publication" under 35 U.S.C. § 311(b). Ex. 1011, 1–2. It is clearly a printed document and it is published. *Id.*

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Even if Petitioner had needed to "gap-fill" with the general knowledge of the JEDEC standard, Patent Owner misapprehends *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1363–64 (Fed. Cir. 2016), which does not prohibit gap-filling with the general knowledge of a person of ordinary skill in the art. So long as supported by a reasoned explanation and evidence, the use of general knowledge is not only proper, it is required under *Graham*. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (background knowledge of skilled artisan may provide motivation to combine); *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337–38 (Fed. Cir. 2020) (holding that general knowledge of skilled artisan may supply missing limitation and that obviousness analysis "necessarily depends on such artisan's knowledge").

Patent Owner next argues that the JEDEC standard (Ex. 1011) pertains to the operation of DDR2 SDRAMs and not the internal operation of the data buffers to which they are connected. Req. Reh'g 7 (citing Final Dec. 42, 49; Ex. 1011, 6, 22; PO Resp. 3, 49–52 & n.9, 54; Ex. 2005 ¶¶ 91–93; Ex. 2009, 27). Patent Owner's argument overlooks that, when enabled, a data buffer (corresponding to Ellsberry's memory bank switch with Halbert's tristate buffers in Petitioner's combination) is connected to the SDRAMs (Ellsberry's "SDRAM DDR devices") so what is output from the data buffer is what is input to the SDRAM. *See, e.g.*, Ex. 1005 ¶¶ 26, 31, 40, Fig. 2. Nor does Patent Owner explain why the JEDEC standard must disclose the internal workings of the switch ASIC when Petitioner's combination of Elbert and Halbert discloses these features. *See, e.g.*, Pet. 79, 85.

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For the foregoing reasons, Patent Owner's arguments are unpersuasive.

C. The Board's Alleged Overlooking of Patent Owner's Arguments for Why the Prior Art Did Not Teach Using a Latency Parameter to Enable a Write Data Path

Patent Owner argues that the Board improperly shifted the burden to prove validity to Patent Owner by faulting Patent Owner for not explaining why Ellsberry's memory bank switch (switch ASIC) would store the Posted CAS_n latency (or additive latency (AL)) parameter if it did not use it for some purpose. Req. Reh'g 8 (citing Final Dec. 44). Patent Owner argues that Ellsberry is silent on what the memory bank switch does with the Posted CAS_n latency (AL) parameter. *Id.* Patent Owner further argues that the Board, while stating that the skilled artisan would have implemented Ellsberry to budget one clock cycle to account for the delay through the data buffers, overlooked that the Posted CAS_n latency (AL) parameter has "nothing to do with operation of the data buffers." *Id.* at 9 (citing Final Dec. 46–47).

As we explained in the Final Written Decision, the read and write latencies RL and WL depend on the CAS latency (CL) and Posted CAS latency (or additive latency) (AL) (RL=AL+CL; WL=AL+CL–1). Final Dec. 45 (citing Ex. 1011, 10–11; Ex. 1003 ¶ 352). Petitioner contends that the Posted CAS latency (AL) parameter accounts for the time needed for data to traverse the data buffer (corresponding to Ellsberry's memory bank switch modified with Halbert's tristate buffers). Pet. 36–37, 75–78; Pet. Reply 10 (citing Ex. 1005, Fig. 8B, note 1; Ex. 2007, 181:9–182:22, 204:11–205:24, 230:25–234:16). In the Final Written Decision, we agreed with Petitioner that U.S. Patent No. 7,532,537 B2 (Ex. 1014, "the '537

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patent"), which constitutes general knowledge of a skilled artisan, teaches to budget one clock cycle to account for delay through the data buffer, and the skilled artisan would have understood that Ellsberry's Posted CAS latency parameter would have been useful for this purpose. Final Dec. 46–47 (citing Ex. 1014, 21:28–53; Ex. 1003 ¶ 363; Ex. 2007, 182:16–22; Ex. 1092, 174:8–175:21, 179:14–181:6).

Patent Owner contends that Petitioner's reliance on the '537 patent in its Reply was "improper sandbagging" because it was not set forth in a challenge ground in the Petition. Req. Reh'g 10. We disagree. Petitioner's reliance on the '537 patent's teaching in support of its contention that it would have been obvious to add one clock cycle to account for the data buffer (corresponding to Ellsberry's memory bank switch modified with Halbert's tristate buffers) has a nexus to Patent Owner's argument that Ellsberry never disclosed enabling or disabling the data path in accordance with a latency parameter (PO Resp. 33–40), and it is a fair extension of Petitioner's contention that the combination of Ellsberry and Halbert in view of the general knowledge of a skilled artisan taught the claimed enabling of the data path in accordance with the latency parameter (Pet. 36–37, 73–81). Thus, Petitioner's reliance on the '537 patent in the Reply is not a new argument but an extension of what Petitioner had contended in the Petition. Accordingly, Petitioner's Reply argument was not improper. *Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1385 (Fed. Cir. 2023). Patent Owner had the opportunity to address Petitioner's contentions concerning the '537 patent in its Sur-Reply, and Patent Owner availed itself of this opportunity. PO Sur-Reply 13.

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D. Allegation That There is No Motivation to Enable Data Paths During a Write

Patent Owner contends that the Board overlooked that "Petitioner never provided an independent reason for further modifying Ellsberry and Halbert to disable and then enable the otherwise always-on data paths and use latency parameters." Req. Reh'g 11–12 (citing Final Dec. 19, 22–23).

Patent Owner's arguments are premised on the incorrect assumption that all of Ellsberry's embodiments have "always on" data paths when, as explained, that is not the case. *See* Sect. II.A, *supra*. Ellsberry's "one port disabled" embodiment does not use "always on" data paths but selectively enables and disables them. *Id.*

Patent Owner further misapprehends that Ellsberry teaches to use the Posted CAS (AL) latency parameter, as does the JEDEC standard, which is used to avoid bus conflicts by accounting for the time necessary for signals to traverse a data buffer (corresponding to Ellsberry's memory bank switch with Halbert's tristate buffers). *See* Sect. II.C, *supra*.

Contrary to Patent Owner's assertion, Petitioner did provide reasons for using Ellsberry's Posted CAS (AL) latency parameter in the combination of Ellsberry and Halbert—to avoid bus conflicts, reduce load, and save power. Pet. 31–36, 44–47, 80–81; Final Dec. 17–19 (motivation), 19–21 (bus conflicts), 21–23 (reducing load), 23–26 (saving power).

Patent Owner argues that the Board relied on an "obvious to try" rationale based on "a finite number of identified, predictable solutions" that was not raised by Petitioner. Req. Reh'g 12 (citing Final Dec. 49–50). However, the issue was raised by the parties' arguments. Patent Owner argued that the "don't care" state in Halbert's Figure 6 means that the write

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path is enabled even when there are no memory operations. PO Resp. 45. Petitioner argued that Halbert's data lines can be in a high-impedance (disabled) state in the "don't care" state. Pet. Reply 23. Patent Owner's and Petitioner's arguments presented the possibility that Halbert's "don't care" encompassed the two options of enabled and high-impedance states, thereby raising the issue of "obvious to try," which we were compelled to address in the Final Written Decision. Final Dec. 49–50; *KSR*, 550 U.S. at 421.

Patent Owner argues that "don't care" and "high impedance" are mutually exclusive states. Req. Reh'g 12. We do not agree. The "don't care" state does not preclude a data path from being disabled in the high-impedance state. Final Dec. 49 (citing Ex. 1005 ¶ 50; Ex. 1006, 9:55–65; Ex. 1009, 17, 26; Ex. 1011, 22).

Patent Owner argues that the Board applied the wrong legal analysis and that the "obvious to try" rationale requires identification of a problem and predictable solution. Req. Reh'g 12–13. Petitioner identified the problems of bus conflicts, excessive loading, and excessive power consumption. Pet. 31–36, 44–47, 80–81. Petitioner showed that disabling the data paths was a predictable solution to those problems. Pet. 47, 78, 80–81.

Even setting aside the "obvious to try" rationale, in Ellsberry's "one port disabled" embodiment, the memory bank switch disables the port connected to memory device for which a memory operation is not underway, and Halbert's "don't care" state does not preclude disabling the port and its associated data path according to Ellsberry's teaching. Ex. 1005 ¶¶ 31, 40, Fig. 2. Petitioner showed by a preponderance of the evidence that a person of ordinary skill in the art would have had motivation to combine Ellsberry

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and Halbert to avoid bus conflicts, reduce load, and save power even without the "obvious to try" rationale. Pet. 31–36, 44–47, 80–81.

Patent Owner argues that neither the Board nor Petitioner ever explained the underlying and necessary reasoning for the rationales to combine Ellsberry and Halbert in the Institution Decision. Req. Reh'g 13 & n.2. We do not agree with this assertion. The Institution Decision (Inst. Dec. 20, 28) merely recognized that the showing that Petitioner made in the Petition (Pet. 31–36, 44–47, 80–81) fits into rationales identified in *KSR* as sufficient to establish a motivation to combine. 550 U.S. at 416–417.

Patent Owner argues that "bus conflicts are indisputably not a concern for write operations, and the Board never found otherwise." Req. Reh'g 14 (citing Final Dec. 20; PO Resp. 55–58; PO Sur-Reply 21, 27). We addressed this argument in the Final Written Decision and decided that bus conflicts are a concern. Final Dec. 20 (citing Pet. 78; Ex. 1035, 89–90; Ex. 1003 ¶¶ 239–240, 264, 366, 373). We are not inclined to change our view, as explained below.

Dr. Subramanian stated that, in order to drive data on shared, bidirectional data busses in read and write operations, "each driver has to be able to turn off to avoid bus conflicts." Ex. 1003 ¶ 373. Dr. Subramanian refers to Dr. Harold Stone's textbook (*id.* (citing Ex. 1035, 89–90, 133 (Fig. 4.7))), which explains that, on a shared data bus, a conflict between read and write drivers "creates a low impedance path from V_{CC} to ground through the output stages of the conflicting gates" and that the "high current through this path can burn out both driving gates." Ex. 1035, 89–90. Hence, the evidence of record showed that bus conflicts are a concern not only for read operations, but also for write operations.

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Patent Owner asserts that Dr. Subramanian, Dr. Wolfe, and Dr. Brogioli testified that bus conflicts are not a concern for write operations. PO Resp. 55–58, 66 (citing Ex. 2006, 188:17–189:2, 189:5–17, 189:22–190:16; Ex. 2007, 68:16–20, 69:16–19, 70:20–23, 72:19–22, 114:9–22, 117:19–21, 117:25–118:2; Ex. 2005 ¶ 128); PO Sur-Reply 21, 27. This testimony, however, does not address the driver "burn out" type of bus conflict that Dr. Subramanian discussed in Dr. Stone's textbook. Req. Reh'g 14 (citing PO Resp. 55–58; PO Sur-Reply 21, 27); Ex. 1003 ¶¶ 373–374; Ex. 1035, 89–90, 133; *see also* Pet. Reply 31 (citing, *inter alia*, Ex. 1003 ¶¶ 373–374 and asserting that "if Ellsberry's or Halbert's *write* drivers were enabled while data is *read* from the coupled memories, that could cause devastating bus conflicts" (emphases omitted)). Also, Dr. Wolfe's testimony was given in the context of Ellsberry's "always on" embodiment which does not disable ports, unlike its "one port disabled" embodiment, which selectively enables and disables its ports. Ex. 2006, 186:23–189:3. Dr. Subramanian's testimony with respect to Halbert indicated that even if it is not necessary to disable read direction drivers outside of a write operation, it is still beneficial to do so in order to reduce power consumption and loading, and to prevent loopback conflicts. Ex. 2007, 68:5–22, 69:7–21, 70:20–23, 73:13–16, 114:9–115:7.

Patent Owner further argues that "whether a skilled artisan might have sought to avoid bus conflicts for unclaimed reasons (i.e., read operations) . . . is irrelevant." Req. Reh'g 14 (citing Final Dec. 19–20). We disagree with Patent Owner's suggestion that the reasoning to combine is limited to claimed features. *See Outdry Techs. Corp. v. Geox S.p.A.*, 859 F.3d 1364, 1370 (Fed. Cir. 2017) ("The Board was not required to limit its motivation to

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combine inquiry to the problem faced by the inventor . . .”). Rather, “[a]ny motivation to combine references, whether articulated in the references themselves or supported by evidence of the knowledge of a skilled artisan, is sufficient to combine those references to arrive at the claimed” subject matter. *Id.* at 1370–71; *see also Intel Corp. v. PACT XXP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. 2023) (“It’s enough for Intel to show that there was a known problem of cache coherency in the art, that Bauman’s secondary cache helped address that issue, and that combining the teachings of Kabemoto and Bauman wasn’t beyond the skill of an ordinary artisan.”). Furthermore, Patent Owner’s argument overlooks that some claims of the ’339 patent are directed to read operations. Ex. 1001, 20:56–21:22 (claim 10), 22:64–23:28 (claim 18), 23:29–24:29 (claim 19), 25:29–26:31 (claim 27), 26:38–49 (claim 29), 26:50–27:9 (claim 30), 27:10–21 (claim 31), 27:26–28:22 (claim 33).

The ’339 patent also discusses data collisions, i.e., bus conflicts, power dissipation, and loading as concerns. *See, e.g.*, Ex. 1001, 2:5–12, 4:27–47, 7:37–43. Likewise, Ellsberry mentions loading and bus conflicts (i.e., activating and disabling ports of memory bank switch to write data to the correct memory bank) as concerns. Ex. 1005 ¶¶ 12, 27, 31, 50, claim 2. Halbert seeks to reduce loading, and describes timing that avoids bus conflicts in successive write operations. Ex. 1006, 3:67–4:8, 6:66–7:30, Fig. 6. Thus, the ’339 patent addresses the same or similar problems as Ellsberry and Halbert. Pet. 14–15, 20, 31–38, 44–47, 80–81. “[A]ny need or problem known in the field of endeavor at the time of the invention and addressed by the patent” may provide a motivation to combine. *KSR*, 550 U.S. at 420–21.

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Patent Owner argues that, in the Final Written Decision, the Board "fell back to unargued and unsupported known-problems-with-predictable-solutions and familiar-elements-combined-using known methods-with-predictable-results rationales" which "violated the APA and lacks any explanation of the underlying predicates." Req. Reh'g 14 (citing *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016) ("*Magnum*")). Here, as we explained in the Final Written Decision, Petitioner presented contentions that amounted to rationales recognized in *KSR* as establishing a reason to combine Ellsberry and Halbert. Final Dec. 19–20 (citing Pet. 78; Ex. 1035, 89–90; Ex. 1003 ¶¶ 239–240, 264, 366, 373). Thus, Patent Owner's reliance on *Magnum* is misplaced.

Patent Owner next argues that, since "Ellsberry and Halbert were redundant in presenting a single load already," "there is no 'reduction' in load to support this motivation." Req. Reh'g 14 (citing Final Dec. 22; PO Resp. 68; PO Sur-Reply 29–30). As we explained, a person of ordinary skill in the art considering Ellsberry would naturally be curious how others solved the loading problem and would have looked to Halbert's solution of using tristate buffers. Final Dec. 22 (citing *Intel*, 61 F.4th at 1380). Patent Owner further argues that the rationale does not teach how to configure Halbert's tristate buffers. Req. Reh'g 15. However, Halbert teaches how to configure the tristate buffers (*see, e.g.*, Halbert's Figure 4), so we do not find this argument persuasive.

Patent Owner argues that "there is no evidence of power concerns in Ellsberry solved by Halbert or by not disabling data paths on write commands" and that "Halbert leaves the data path enabled during write commands, suggesting that power savings is negligible and of no concern."

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Req. Reh'g 15 (citing Final Dec. 23–26; Ex. 2007, 72:5–8). Patent Owner contends that the Board overlooked this argument in its Final Written Decision, and invoked a predictable-solutions-to-a-known-problem rationale that was never argued and unproven. *Id.* (citing PO Resp. 4, 47; Ex. 2005 ¶¶ 107–108; PO Sur-Reply 28–29; Final Dec. 25; *In re Magnum Oil Tools*, 829 F.3d at 1381).

We considered Patent Owner's arguments concerning power consumption and did not agree with them. Final Dec. 23–26 (citing PO Resp. 4, 47; PO Sur-Reply 28–29). Patent Owner incorrectly premises its arguments on equating Halbert's "don't care" state with the enabled state when, as explained, it encompasses both enabled and disabled states. Also, the expert testimony in this case established that power savings would be an important priority in at least some applications and that it was a known problem in the art. *Id.* at 25–26 (citing Ex. 1003 ¶¶ 366, 422, 662; Ex. 2007, 18:8–18, 37:20–24, 57:1–10; Ex. 1092, 123:16–125:11; Ex. 2013, 5; Ex. 2010, 2). The record further established that Halbert's tristate buffers in the high-impedance state would have been effective in saving power when a memory module was not actively conducting a read or write operation. *Id.* (citing Ex. 1003 ¶ 366; Ex. 1009, 1; Ex. 1035, 135; Ex. 2007, 18:8–18, 27:21–25, 37:20–24, 57:1–10, 60:4–8; Ex. 1092, 114:7–115:1, 123:16–125:11; Ex. 2013, 5; Ex. 2010, 2).

III. CONCLUSION

We have considered Patent Owner's arguments in its Request for Rehearing but they do not persuade us to modify our Final Written Decision.

IV. ORDER

In consideration of the foregoing, it is hereby:

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ORDERED that Patent Owner's Request for Rehearing of our Final Written Decision is *denied*.

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Samsung Electronics Co., Ltd. v. Netlist, Inc., PGR2026-00001

In summary:

Outcome of Decision on Rehearing:

Claim(s)	35 U.S.C §	Reference(s)/Basis	Denied	Granted
1–35	103	Ellsberry, Halbert	1–35	

Final Outcome of Final Written Decision after Rehearing:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not Shown Unpatentable
1–35	103	Ellsberry, Halbert	1–35	

Samsung Ex. 1119, p. 19
Samsung Electronics Co., Ltd. v. Netlist, Inc., PGR2026-00001

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