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Paper 96
Entered: April 17, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00615
Patent 7,619,912 C1

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Challenged Claim Unpatentable
Dismissing Patent Owner's Motion to Submit Supplemental Information
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00203 and have been joined as petitioners in this proceeding. *See* Paper 58.

I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co., Ltd. ("Samsung") filed a Petition (Paper 1, "Pet.") for *inter partes* review of claim 16 ("challenged claim") of U.S. Patent 7,619,912 C1 (Ex. 1001, "the '912 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7) to the Petition. Samsung filed an authorized Preliminary Reply (Paper 14), and Patent Owner filed an authorized Preliminary Sur-Reply (Paper 15). The Board instituted *inter partes* review under 35 U.S.C. § 314(a). Paper 20 ("Institution Decision" or "Inst. Dec.").

Patent Owner requested Rehearing and Precedential Opinion Panel review of the Institution Decision. Paper 25. While that request was pending, the Board authorized Patent Owner to file a motion seeking additional discovery on the issue of whether Google was a real party in interest, which would bar the Petition under 35 U.S.C. § 315(b). Paper 32. Patent Owner then filed the Motion for Additional Discovery (Paper 34), Petitioner opposed (Paper 36), and Patent Owner replied in support of its Motion (Paper 37).

The Director granted *sua sponte* review (Paper 38) of the Institution Decision, entered a stay of the proceeding, and dismissed the Request for Rehearing and Precedential Opinion Panel Review (Paper 39). The Director then issued a Decision (Paper 40) denying Patent Owner's Request for Rehearing, granting-in-part and denying-in-part Patent Owner's Motion for Additional Discovery, lifting the stay, and remanding the case to the panel for further proceedings consistent with the Director's Decision.

We entered an Order for Petitioner to complete the additional discovery as authorized by the Director, and for the parties to propose a briefing schedule for the additional discovery. Paper 42. Petitioner filed the authorized additional discovery as exhibits and a Summary of Responses to the Additional Discovery (Paper 46) along with a Motion to Seal (Paper 43), which we granted (Paper 49). We then authorized a schedule for the parties to brief the applicability of the additional discovery to the issue of whether Google was a real party in interest and the Petition thus time-barred under 35 U.S.C. § 315(b). Papers 51–57. After consideration of the evidence, we determined by Order on Remand from the Director (Paper 62 (parties and Board), Paper 64 (public)) that Google was not a real party in interest and that this proceeding thus was not time-barred.

After briefing on the additional discovery but before our Order on Remand from the Director, Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC ("the Micron entities") filed a petition and requested joinder to this proceeding. IPR2023-00203, Papers 1, 3. We granted the Micron entities' petition for *inter partes* review and joined them as parties on the petitioner side of this case. *Id.* at Paper 8. A copy of that institution decision was entered in this proceeding. Paper 58. We refer to Samsung and the Micron entities together as "Petitioner" in this Decision.

Under authority delegated by the Director, due to the joinder, we adjusted the one-year period for issuing the Final Written Decision to April 19, 2024 and modified the due dates applicable to this proceeding. Paper 63.

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During the trial, Patent Owner filed a Response (Paper 67) ("PO Resp."), Petitioner filed a Reply (Paper 77) ("Pet. Reply"), and Patent Owner filed a Sur-Reply (Paper 80) ("PO Sur-Reply").

Patent Owner also requested authorization to submit supplemental information from parallel litigation concerning the deposition of Micron's corporate representative who had allegedly taken inconsistent positions impacting the merits of this *inter partes* review. Ex. 3017. We issued an Order (Paper 71) authorizing Patent Owner to file a Motion to Submit Supplemental Information. Patent Owner filed the Motion (Paper 72), Petitioner opposed (Paper 75), and Patent Owner replied in support of its Motion (Paper 76). We dismiss Patent Owner's Motion to Submit Supplemental Information for reasons explained later in this Decision.

Patent Owner then contended that Petitioner's Reply contained new arguments, and Petitioner contended that Patent Owner's Sur-Reply contained new arguments, and each requested authorization to file a motion to strike new arguments in the other's briefing. Ex. 3020. We denied these requests (*id.*) but permitted the parties to file one-page statements identifying new arguments in the other party's briefings, which they did. Papers 86 and 87.

Petitioner and Patent Owner requested oral argument. Papers 84 and 85. A hearing was conducted on January 31, 2024, and the transcript is in the record. Paper 95.

Petitioner objected to evidence (Papers 45, 68, 83) and filed a Motion to Exclude (Paper 89). Patent Owner opposed Petitioner's Motion to Exclude (Paper 90), then amended its opposition (Paper 91), and Petitioner replied (Paper 92) in support of its Motion to Exclude.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). Having reviewed the complete trial record, we determine that Petitioner has shown, by a preponderance of the evidence, that the challenged claim is unpatentable.

B. Real Parties in Interest

Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC are the identified real parties in interest on the petitioner side. Pet. 1; IPR2023-00203, Paper 3, 1.

Patent Owner identifies itself as the sole real party in interest. Paper 4, 1.

C. Related Matters

The parties advise that the '912 patent is related to the following pending matters:

- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, 2:21-cv-00293 (E.D. Tex. filed Aug. 1, 2022)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00294 (E.D. Tex. filed Aug. 1, 2022)
- *Netlist, Inc. v. Google LLC*, 3:09-cv-05718 (N.D. Cal. filed Dec. 4, 2009)
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2023-00203 (PTAB filed Nov. 18, 2022)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00454 (U.S. Patent 11,093,417)

- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00455 (U.S. Patent 9,858,215)
- U.S. Patent Application No. 17/403,832.

Petitioner contends that the ’912 patent is related to the following matters, which are no longer pending:

- *Netlist, Inc. v. Inphi Corporation*, No. 2-09-cv-06900 (C.D. Cal. filed September 22, 2009)
- *Inter Partes* Reexamination 95/000,578 (U.S. Patent 7,619,912);
- *Inter Partes* Reexamination 95/000,579 (U.S. Patent 7,619,912);
- *Inter Partes* Reexamination 95/001,339 (U.S. Patent 7,619,912)
- *Inter Partes* Reexamination 95/000,546 (U.S. Patent 7,289,386)
- *Inter Partes* Reexamination 95/000,577 (U.S. Patent 7,289,386)
- *Inter partes* Reexamination 95/001,337 (U.S. Patent 7,636,274)
- IPR2014-00882 (U.S. Patent 7,881,150)
- IPR2014-00883 (U.S. Patent 8,081,536)
- IPR2015-01021 (U.S. Patent 8,081,536)
- IPR2017-00549 (U.S. Patent 8,756,364)
- IPR2017-00667 (U.S. Patent 7,532,537)
- IPR2017-00668 (U.S. Patent 7,532,537)

Paper 79, 2–3 (Petitioner’s Updated Mandatory Notices); Paper 81, 1–2 (Patent Owner’s Third Updated Mandatory Notice).

D. Overview of the '912 Patent (Ex. 1001)

The '912 patent is titled "Memory Module Decoder" and is directed to a memory module that is connectable to a computer system. Ex. 1001, codes (54), (57). Figure 1A of the '912 patent is reproduced below.

Figure 1A:

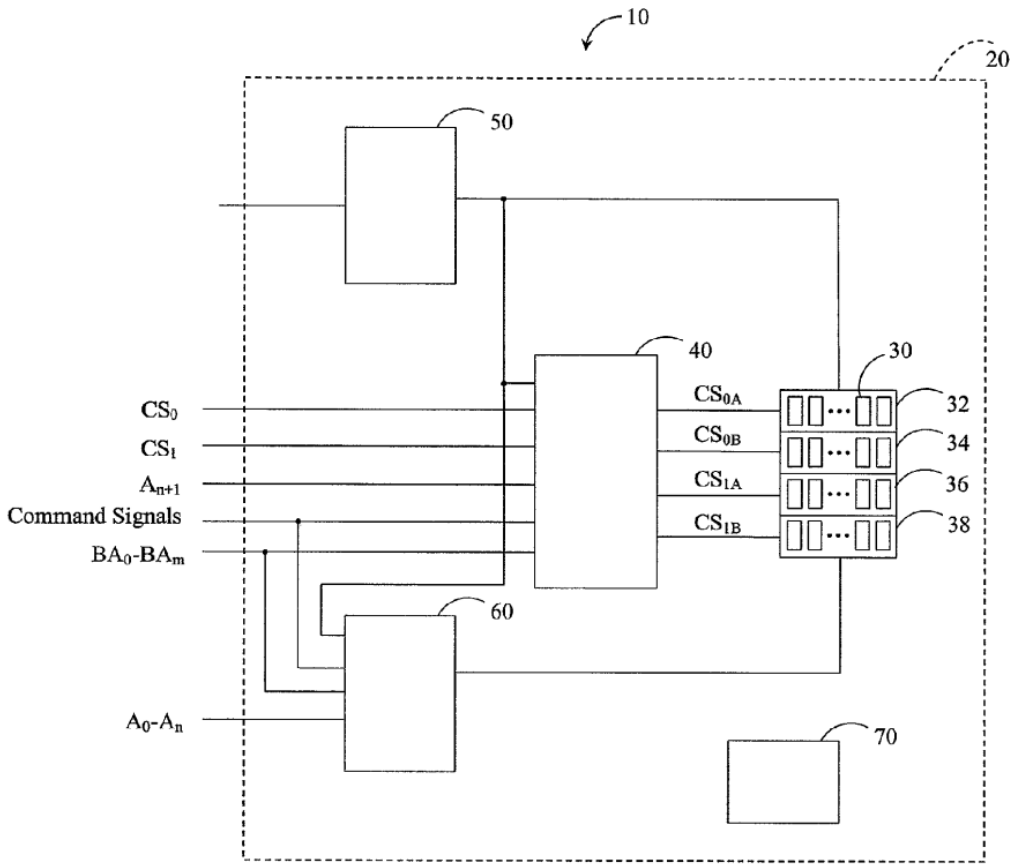

Figure 1A shows a memory module 10 with printed circuit board 20 and memory devices 30 connected to the printed circuit board. *Id.* at 5:9–11. Memory devices 30 are arranged in ranks 32, 34, 36, 38. *Id.* at 22:35–37. The memory devices 39 may be double-data rate (DDR) dynamic random-access memory (DRAM) devices. *Id.* at 6:12–16. The memory module 10 further comprises logic element 40 coupled to the printed circuit board 20. *Id.* at 5:13–14. Logic element 40 receives a set of input control signals and

generates output control signals for select memory devices 30. *Id.* at 5:14–21. Phase-lock loop device 50 and register 60 are also mounted on printed circuit board 20. *Id.* at 5:25–27. The phase-lock loop device 50 generates clock signals to memory devices 30, logic element 40, and register 60. *Id.* at 5:28–31. Register 60 receives and buffers control signals including address signals, and transmits corresponding signals to appropriate memory devices 30. *Id.* at 5:31–36.

In Figure 1A, logic element 40 receives a set of input control signals from the computer system that include chip-select signals CS_0–CS_1, address signal A_{n+1}, and bank address signals BA_0–BA_m. *Id.* at 7:35–53. To the computer system, the memory module has only two ranks selectable with either CS_0 or CS_1. *Id.* at 6:55–7:19. However, logic element 40 generates a set of output control signals CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B} corresponding to the four ranks 32, 34, 36, 38 of memory devices 30. *Id.* at 6:61–63. Logic element 40 also receives command signals (e.g., read or write) from the computer system and transmits the command signal to memory devices on the selected rank of the memory module. *Id.* at 6:55–61, 7:43–53.

E. Claim 16 of the ’912 Patent

Claim 16 of the ’912 patent is an independent claim, and the only claim that is challenged in this proceeding. Claim 16 is reproduced below with Petitioner’s identifiers shown in bold brackets.

> **[16.pre]** A memory module connectable to a computer system, the memory module comprising:
>
> **[16.a]** a printed circuit board;
>
> **[16.b]** a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, **[16.b.i]** the plurality

of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

[16.c] a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, **[16.c.i]** the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal**, [16.c.ii]** the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, **[16.c.iii]** the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, **[16.c.iv]** wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

[16.d] a phase-lock loop device coupled to the printed circuit board, **[16.d.i]** the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,

[16.e] wherein the command signal is transmitted to only one DDR memory device at a time.

Ex. 1001, *Inter Partes* Reexamination Certificate, 3:9–43.

A. Evidence

Petitioner relies on the following references:

Reference		Date	Exhibit No.
Perego-422[2,3]	US 7,363,422 B2	Apr. 22, 2008	1035
Amidi[4]	US 2006/0117152 A1	Jun. 1, 2006	1036
Ellsberry[5]	US 2006/0277355 A1	Dec. 7, 2006	1037

Pet. 4, 14–22.

Petitioner further relies upon the Declaration of Dr. Andrew Wolfe (Ex. 1003). Patent Owner relies on the Declaration of Dr. Michael C. Brogioli (Ex. 2062). The parties deposed each other's experts and rely on those depositions in their arguments (Ex. 1101; Ex. 2103). The parties submitted other evidence into the record, which we will address herein as necessary.

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[2] Although the Petition refers to this reference as "Perego," we refer to it as "Perego-422" to distinguish it from another reference of record by the same inventor, U.S. Patent 7,356,639 ("Perego-639") (Ex. 1061).

[3] Petitioner contends that Perego-422 is prior art under 35 U.S.C. §§ 102(a) and (e). Pet. 14.

[4] Petitioner contends that Amidi is prior art under 35 U.S.C. §§ 102(a) and (e). Pet. 18.

[5] Petitioner contends that Ellsberry is prior art under 35 U.S.C. §§ 102(a) and (e). Pet. 20.

B. Asserted Challenges to Patentability

Ground	Claim Challenged	35 U.S.C. §	Reference(s)/Basis
1	16	§ 103(a)	Perego-422
2	16	§ 103(a)	Perego-422, Amidi
3	16	§ 103(a)	Ellsberry

Pet. 4.

II. ANALYSIS

A. Principles of Law

In an *inter partes* review, a petitioner bears the burden of persuasion to prove "unpatentability by a preponderance of the evidence." *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (quoting 35 U.S.C. § 316(e)); *see* 37 C.F.R. § 42.1(d) (2021).

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

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B. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include "(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Env't Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). "Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case." *Id.* at 696–97.

Petitioner contends that a person of ordinary skill in the art ("POSITA") in the field of memory module design in 2004 or 2005 would have an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Pet. 5. Petitioner contends such person would have been familiar with various standards of the day, including JEDEC industry standards, and would have been knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id.* at 6.

Patent Owner applies the skill level of a POSITA proposed by Petitioner for this proceeding. PO Resp. 4.

On this record, we accept Petitioner's statement of the level of ordinary skill in the art except that we omit the qualifiers "at least" before years of education and experience because they render the level ambiguous

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and may encompass levels that are beyond ordinary. Otherwise, we find Petitioner's statement of the level of ordinary skill in the art consistent with the '912 patent and the applied prior art references. *Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (the applied prior art may reflect an appropriate level of skill).

C. Claim Construction

We construe claim terms "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)." 37 C.F.R. § 42.100(b). There is a presumption that claim terms are given their ordinary and customary meaning, as would be understood by a POSITA in the context of the specification. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Nonetheless, if the specification "reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor's lexicography governs*."* *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17). Only disputed claim terms must be construed, and then only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner contends that "rank" refers to "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module." Pet. 12 (citing Ex. 1003 ¶ 74).

Patent Owner argues that "rank" should be construed as "a predetermined set of DRAMs on a memory module that act together to send or receive a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other DRAMs on the memory module." PO Resp. 4.

Patent Owner argues that the parties' dispute over claim construction can be narrowed to the following issue: "whether 'rank' can include just 'one memory device.'" *Id.* Petitioner agrees that this is the dispositive issue for claim construction. Pet. Reply 1. For the following reasons, we determine that the intrinsic evidence of the '912 patent shows that the claim term "rank" may include only one memory device.

Starting with the intrinsic evidence, we begin our analysis by observing that claim 16 of the '912 patent recites "a plurality of double-data-rate (DDR) memory devices." Ex. 1001, 3:13–14 (reexamination certificate). The claim further recites "a first number of DDR memory devices arranged in a first number of ranks" and "a second number of DDR memory devices arranged in a second number of ranks." *Id.* at 3:15–16, 3:23–24 (reexamination certificate). The only restrictions in the claim on the first and second numbers of memory devices and ranks are that "the second number of DDR memory devices [is] smaller than the first number of DDR memory devices" and "the second number of ranks is less than the first number of ranks." *Id.* at 3:25–28 (reexamination certificate). Hence, the

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language of claim 16 does not preclude the possibility that a rank could have a single memory device.

Claim 55 of the ’912 patent depends from claim 1 and recites “each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages.” *Id.* at 5:56–59 (reexamination certificate); *see also* Pet. Reply 7. This implies that each of the ranks recited in claim 1 could include a single memory device. Ex. 1001, 1:29–31 (reexamination certificate). Otherwise, the limitation would be superfluous. Claim 55 informs how “rank” should be understood in claim 16.

The specification of the ’912 patent similarly describes its memory module without restriction on the specific number of memory devices that can be included in each rank (except that the second number of memory devices or ranks must be less than the first number of memory devices or ranks). *Id.* at 3:3–14 (summary), 6:64–7:18.

During the trial, the parties disputed at length the meaning of the “Logic Tables” section of the ’912 patent. *Id.* at 7:55–9:21; Pet. 12–13; PO Resp. 6–10; Pet. Reply 9–10. The disputed paragraph from this section is shown below.

> The “Command” column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. *In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory* devices

> *to ensure that the memory content of the memory devices remains valid over time.* Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

Ex. 1001, 8:44–64 (emphasis added). Patent Owner argues that the ’912 patent consistently describes memory devices as part of multi-device ranks and thus that a POSITA would understand this passage as referencing a memory module with at least two ranks, each rank having at least two memory devices. PO Resp. 7 (citing Ex. 1001, 6:31–38, 20:64–65, 22:34–35; Figs. 1A, 1B, 2A, 3A; Ex. 2062 ¶¶ 106–107). Petitioner contends that the language emphasized in the block quoted paragraph above means that the selected rank has only one memory device. Pet. Reply 9–10 (citing Ex. 1001, 8:48–60; Ex. 1100, 11–12; Ex. 1098/2063, 5–6).

The disputed paragraph may be better understood with reference to Table 1, shown below, and Figure 1A (*see* § I.D).

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1

TABLE 1-continued

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

Ex. 1001, 7:60–8:18.

In Table 1, states 1, 2, 4, 5 select only one rank with chip select signals CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}, which are active low ("0") and inactive high ("1"). *See id.* at 8:19–42 (describing what is selected in each logic state). States 3 and 6, however, pair the ranks together so that when CS_{0A} and CS_{0B} are activated, CS_{1A} and CS_{1B} are deactivated, and vice versa. States 3 and 6 permit two smaller memory devices to emulate a larger one.

The first two emphasized sentences above (*id.* at 8:47–54) could be interpreted both as Petitioner and Patent Owner propose. Under Patent Owner's interpretation, the "selected rank" includes the "one memory device or the other memory device" each in multi-device ranks. Under Petitioner's interpretation, the "selected rank" may be the one memory device connected to C_{S1A} of the pair of memory devices connected to chip select signals CS_{1A} and CS_{1B}.

However, the subsequent emphasized sentences (*id.* at 8:54–60) could only be understood in favor of Petitioner's interpretation. If "the command signal is passed through to both associated ranks" and "the command signal is sent to both memory devices," each rank must have only one memory device. Thus, we agree with Petitioner that this passage means that a rank may have only one memory device.

Patent Owner argues that this paragraph of the '912 patent (*id.* at 8:44–64) must be read in conjunction with its Figures which show multiple memory devices per rank. PO Resp. 7 (citing Ex. 1001, 6:31–38, 20:64–65, 22:34–35, Figs. 1A, 1B, 2A, 3A; Ex. 2062 ¶¶ 106–107). However, the disputed paragraph refers to "certain embodiments" which do not necessarily correspond exactly to what the Figures depict, and the Figures are described as "exemplary" and "compatible with" or "in accordance with certain embodiments described herein." *See, e.g.*, Ex. 1001, 3:32–48. We find no statement here or elsewhere in the '912 patent that a rank must include multiple memory devices, and cannot include a single memory device.

The "Back-to-Back Adjacent Read Commands" section of the '912 patent provides another example of single-device ranks. Ex. 1001, 23:26–25:67; *see* Pet. Reply 7–13. This section relates to solving a problem that occurs when back-to-back read commands cross the memory boundaries between ranks of memory devices, and memory controllers must take measures to avoid data collisions or interference. Ex. 1001, 23:60–67. Back-to-back adjacent read commands are referred to as "BBARX" in the '912 patent. *Id.* This section explains that the circuit of Figure 6B of the '912 patent uses isolation device 120 to avoid collisions between memory

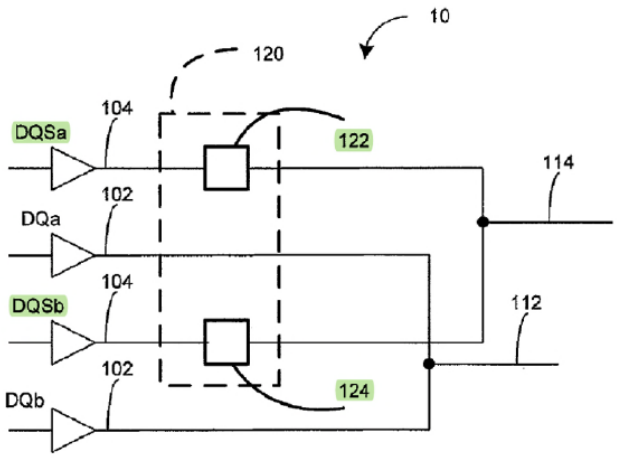
devices "a" and "b" of different ranks. *Id.* at 24:1–58. This section thus supports that a rank may have only one memory device.

The '912 patent provides Examples 1 and 2 of Verilog code relating to the operation of field-effect transistor (FET) switches used to avoid conflicts during back-to-back read operations (which the '912 patent refers to as "BBARX"). *Id.* at 14:24–20:53, 23:60–67. Patent Owner argues that Example 2 of this code shows that FET switches are used to send a command to a single memory device in a rank of multiple memory devices and shows that the ranks discussed in the "Logic Tables" section of the '912 patent include multiple memory devices. PO Resp. 26 (citing Ex. 1003 ¶¶ 36–43). Petitioner disagrees, contending that code relates to FET switches on the DQS[6] strobe lines, not the command lines, and thus does not relate to the "Logic Tables" section which discusses the command signal, not the DQS strobe lines. Pet. Reply 11–13.

We agree with Petitioner that the Verilog code of Example 2 relates to enabling and disabling FET switches on the DQS strobe lines, not the command lines. Petitioner provides an annotated version of Figure 6B shown below.

[6] The JEDEC DDR standards refer to data signals as "DQ", data strobe signals as "DQS", control signals as "RQ", and clock signal as "CK". Pet. 30 (citing Ex. 1003 ¶ 124).

Figure 6B:



Id. at 11 (citing Ex. 1001, 24:39–58, Fig. 6B). Figure 6B shows isolation device 120 connected between logic element 40 and memory devices 30 (e.g., memory devices "a" and "b"). Ex. 1001, 3:65–67, 24:1–58. Isolation device 120 comprises switches 122, 124 (e.g., FETs), which control when respective DQSa and DQSb strobe signals are output to memory devices "a" and "b" on common strobe line 114. *Id.* at 24:31–38.

Petitioner also provides an annotated version of an excerpt from Example 2 of the Verilog code at Exhibit 1001, 19:1–53, shown below:

```
always @(posedge clk_in)
 begin
 if (
    (rd0_o_R2 & ~rd1_o_R4)                                  // pre-am rd if no ped on rnk 1
   | rd0_o_R3                                               // 1st cyc of rd brst
   | rd0_o_R4                                               // 2nd cyc of rd brst
   | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                     // post-rd cyc if no ped on rnk 1
   | (wr0_o_R1)                                             // pre-am wr
   | wr0_o_R2 | wr0_o_R3                                    // wr brst 1st & 2nd cyc
   | (wr0_o_R4)                                             // post-wr cyc (chgef9)
   | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4 // rank 1 (chgef9)
   )
                 en_fet_a <= 1'b1;                          // enable fet
 else
                 en_fet_a <= 1'b0;                          // disable fet
 end
```

Pet. Reply 13. Petitioner contends that the code highlighted in green indicates when to enable/disable the same FET switches on the DQS strobe lines (not the command lines) to switch the strobe line between data bursts, as stated in the comments section of the code, to avoid problems due to BBARX. *Id.* at 12–13. The highlighted code is followed on the same lines by comments "//1st cyc of rd brst" and "//2nd cyc of rd brst" which refer to a first read cycle followed by a second read cycle, i.e., which is a BBARX situation that presents the possibility of a collision of DQS data strobe signals for the memory devices 'a' and 'b' sharing common strobe line 114 shown in the '912 patent's Figure 6B above. The code stating "en_fet_a <= 1'b1" and "en_fet_a <= 1'b0" refers to enabling and disabling, respectively, the FET 122 for the DQS signal for memory device 'a' shown in Figure 6B. Ex. 2062 ¶ 40. From inspection of Figure 6B and the code of Example 2, we agree with Petitioner that the code of Example 2 relates to enabling and disabling a FET 122 on the DQS data strobe line, not the command line discussed in the "Logic Tables" section of the '912 patent.

Dr. Brogioli offers testimony explaining the Verilog code in the '912 patent and, specifically, contrasting Verilog code Examples 1 and 2. Ex. 2062 ¶¶ 36–43. Dr. Brogioli testifies that, in Example 2, "[s]ignal 'en_fet_a' is used to enable or disable the FET switch for memory device 'a' in physical rank 0 (rnk0), and 'en_fet_b' is used to enable or disable FET switch for memory device 'b' from physical rank 1 (rnk1)." *Id.* ¶ 40. According to Dr. Brogioli, "[b]y providing for the selective enabling or disabling of the FET switch associated with memory device 'a' or memory device 'b,' Example 2 teaches how to transmit a command to a single memory device on a physical rank of multiple memory devices." *Id.*

Dr. Brogioli testifies that

> Example 1 provides for the generation of ***multiple*** control signals to control ***multiple*** DQS signals from ***multiple*** memory devices in each rank. This is achieved by using multiple FET switches: fet1a, fet2a, and fet3a to control DQS signals from three different memory devices belonging to the same physical rank (rnk0); and fet1b, fet2b, and fet3b to control DQS signals from 3 different memory devices belonging to the same physical rank (rnk1).

Id. ¶ 42. Dr. Brogioli annotates a portion of the Verilog Example 1 as shown below.

```
// DQ FET enables
assign        enq_fet1 = dq_cyc | dq_ncyc
assign        enq_fet2 = dq_cyc | dq_ncyc ;
assign        enq_fet3 = dq_cyc | dq_ncyc
assign          enq_fet4 = dq_cyc | dq_ncyc ;
assign          enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign        ens_fet1a = dqs_cyc_a | dqs_ncyc_a ;
assign        ens_fet2a = dqs_cyc_a | dqs_ncyc_a ;
assign        ens_fet3a = dqs_cyc_a | dqs_ncyc_a ;
assign        ens_fet1b = dqs_cyc_b | dqs_ncyc_b ;
assign        ens_fet2b = dqs_cyc_b | dqs_ncyc_b ;
assign        ens_fet3b = dqs_cyc_b | dqs_ncyc_b ;
```

Memory devices in rnk0

Memory devices in rnk1

Id. In the annotated Verilog code above, Dr. Brogioli notes that the code for fet1a, fet2a, and fet3a corresponds to "Memory devices in rnk0" and that the code for fet1b, fet2b, and fet3b corresponds to "Memory devices in rnk1." *Id.* Dr. Brogioli opines that

> Example 1 teaches enabling or disabling the DQ and DQS lines for a plurality of memory devices in each corresponding rank, not a single memory device. But as explained above, Example 2, teaches selectively enabling or disabling of the FET switch associated with memory device "a" or memory device "b" in each corresponding rank.

Id. ¶ 43.

Even if we were to accept Dr. Brogioli's testimony that the FETs control transmission of commands (*id.* ¶ 40), we do not agree with

Dr. Brogioli's conclusion that Example 2 involves multiple memory devices in each rank. As his testimony for Example 1 makes clear, the Verilog code specifically identifies multiple FETs when there are multiple memory devices in each rank. *Id.* ¶ 42. Example 2, however, identifies commands for two FETs, which Dr. Brogioli acknowledges are in separate ranks. *Id.* ¶ 40. Thus, "en_fet_a" would appear to pertain to memory device a, which is the memory device of rank 0 just as "en_fet_b" pertains to memory device b, which is the memory device of rank 1. Dr. Brogioli does not identify Verilog code in Example 2 that controls other memory devices in each rank, suggesting that Example 2 pertains to single-device ranks, as opposed to Example 1. Thus, we find the Verilog code in the '912 patent supports Petitioner's position that a rank may be only one device.

We previously explained that the prosecution history of the examination and reexamination do not elucidate the proper construction of "rank." Inst. Dec. 31–32. Nothing that has transpired during the trial changes our view of the prosecution history.

We consider claim constructions from district courts in our analyses if they are timely made of record. 37 C.F.R. § 42.100(b). Petitioner contends that the District Court for the Eastern District of Texas considering the '912 patent and its related '215 patent concluded that "rank" can include a single memory device. Paper 79, 2 (Petitioner's Updated Mandatory Notices) (citing Ex. 1117, 11–14). This is consistent with our discussion of the intrinsic record above.

Based on the foregoing, we conclude that "rank" as used in the '912 patent can include only "one memory device." Because the intrinsic record is clear, we need not resort to extrinsic evidence to determine the scope of

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the term "rank." *See Seabed Geosolutions (US) Inc. v. Magseis FF LLC*, 8 F.4th 1285, 1287 (Fed. Cir. 2021) ("If the meaning of a claim term is clear from the intrinsic evidence, there is no reason to resort to extrinsic evidence."); *Intel Corp. v. VIA Techs., Inc.*, 319 F.3d 1357, 1367 (Fed. Cir. 2003) ("When an analysis of *intrinsic* evidence resolves any ambiguity in a disputed claim term, it is improper to rely on extrinsic evidence to contradict the meaning so ascertained."); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) (*en banc*) (noting that extrinsic evidence is "in general . . . less reliable than the patent and its prosecution history in determining how to read claim terms"). With this construction, we proceed to address the challenge grounds asserted by Petitioner.

D. Obviousness of Claim 16 Over Ellsberry (Ground 3)

We now address the parties' contentions concerning whether Ellsberry is prior art to the '912 patent under their respective priority dates and whether Ellsberry qualifies as a "printed publication"; and Petitioner's contention that Ellsberry teaches or suggests each limitation of claim 16. We conclude that claim 16 is obvious notwithstanding Patent Owner's arguments to the contrary.

1. Priority

Petitioner bears the initial burden of production on priority. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1379 (Fed. Cir. 2015). Petitioner satisfies that burden by arguing that Ellsberry, having publication and filing dates before the filing date of the '912 patent, renders claim 16 of the '912 patent obvious under § 103(a). *Id.*; Pet. 63–111. The burden of production on the issue of priority then shifts to Patent Owner to show that Ellsberry is not prior art. *Dynamic Drinkware*, 800 F.3d at 1380.

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Patent Owner must show that each application in a priority chain leading back to an application predating Ellsberry complies with the written description requirement of § 112 and reasonably conveys to those skilled in the art that the inventors had possession of the subject matter of claim 16 as of the earlier filing date. *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1571 (Fed. Cir. 1997); *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). Patent Owner does not satisfy its burden of production for the reasons that follow.

The ’912 patent was filed on September 7, 2007, as U.S. Application 11/862,931 (“the ’931 application”), and issued November 17, 2009. Ex. 1001, codes (21), (22), 1:3–16. The ’912 patent indicates that it is a continuation of U.S. Application 11/173,175, filed on July 1, 2005, which issued as U.S. Patent 7,289,386 (“the ’386 patent”). *Id.* at code (63). The ’386 patent claims priority to U.S. Provisional 60/588,244 (“the ’244 provisional”), filed July 15, 2004. *Id.* at code (60), 1:6–11.

The ’912 patent further indicates that the ’386 patent is a continuation-in-part of U.S. Application 11/075,395, filed March 7, 2005, which issued as U.S. Patent 7,286,436 (“the ’436 patent”). *Id.* at code (63), 1:11–13. The ’436 patent claims priority to U.S. Provisional 60/550,668 (“the ’668 provisional”) filed March 5, 2004, and U.S. Provisional 60/575,595 (“the ’595 provisional”) filed May 28, 2004. *Id.* at code (60).

Petitioner contends that the ’668, ’595, and ’244 provisionals and the ’436 patent do not provide written description support under § 112 ¶ 1 for claim 16 of the ’912 patent. Pet. 63–69. Accordingly, Petitioner contends that the priority date for the ’912 patent is July 1, 2005. *Id.* at 20–21. Ellsberry was filed on June 1, 2005 as U.S. Application 11/142,989.

Ex. 1037, codes (21), (22). Petitioner contends that Ellsberry constitutes prior art to claim 16 of the ’912 patent under §§ 102(a) and (e) and that Ellsberry renders claim 16 obvious under § 103(a). Pet. 20–21 (citing *id.* at § VI.B.1; Ex. 1003 ¶¶ 189–196).

More specifically, Petitioner contends that the ’668 and ’595 provisionals do not disclose the claimed “logic element” or that such a “logic element” receives “at least one row/column address signal, bank address signals, and at least one chip-select signal.” *Id.* at 63 (citing Ex. 1003 ¶ 189). Patent Owner does not dispute Petitioner’s contentions concerning the ’668 and ’595 provisionals.

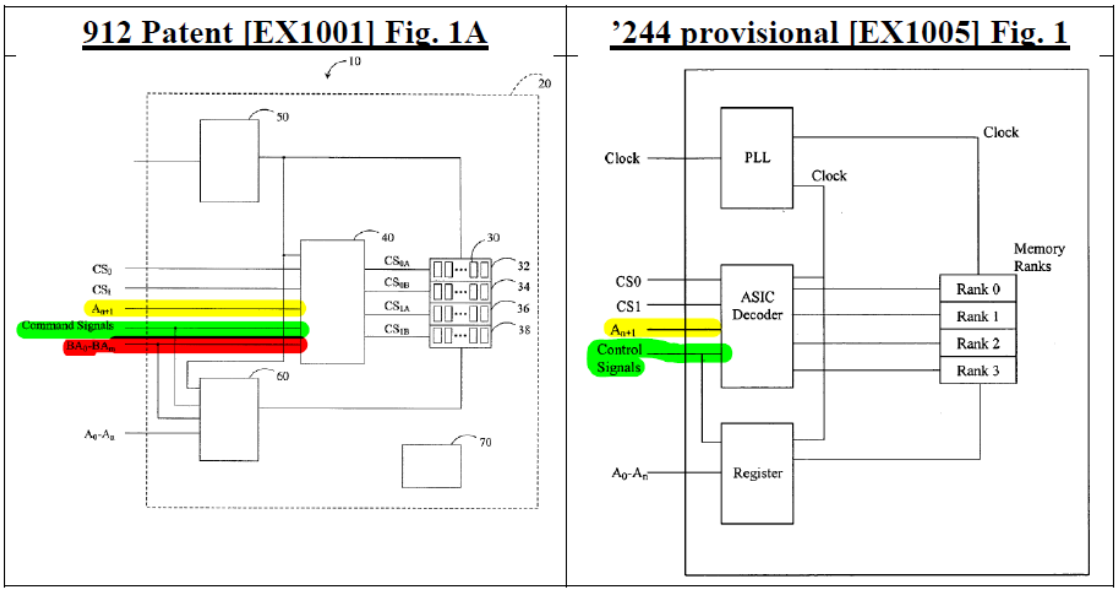
Instead, Patent Owner relies on the ’244 provisional and ’436 patent as providing written description support for claim 16 of the ’912 patent. PO Resp. 54–75; PO Sur-Reply 21–40. Petitioner contends that the ’244 provisional has no disclosure of “bank address” signals as required by claim 16. Pet. 63. Petitioner further contends that the ’436 patent, which is in a separate priority chain from the ’244 provisional, lacks any embodiment including “a circuit” comprising “a logic element” and “a register” as required by claim 16 and as shown in Figure 1A of the ’912 patent (elements 40 and 60, respectively). *Id.* at 64 (citing Ex. 1003 ¶ 190). Petitioner, therefore, contends that Ellsberry is not prior art because it predates the earliest effective filing date of the ’912 patent. *Id.* at 68–69 (citing Ex. 1003 ¶¶ 188, 196).

a) ’244 Provisional

Patent Owner argues that the ’244 provisional provides written description support for the “bank address” signals that Petitioner contends are missing. PO Resp. 62–70. Specifically, Patent Owner asserts that a

POSITA would have understood "control signals" to include "bank address" signals under the JEDEC DRAM standards of the day. *Id.* at 63 (citing Ex. 2062 ¶¶ 62–66). Patent Owner asserts that Petitioner's expert, Dr. Wolfe, acknowledged that personal computers would send bank address signals (*id.* at 64); that Figure 1 of the '244 provisional would be understood to be a JEDEC-style memory module because of its chip select signals (*id.* at 64–65); that the JEDEC standards required bank address signals (*id.* at 65–68); and that the '244 provisional mentions "one control signal (such as an address signal)," which would be understood as an "address signal" that would include the bank address signal "BA2" (*id.* at 69–70).

Petitioner replies that the '244 provisional does not provide support for the "bank address" signals and provides the following diagram to explain.



Pet. Reply 34–35. The diagram shows that Figure 1A of the '912 patent includes bank address signals BA_0–BA_m whereas Figure 1 of the '244 provisional does not show any bank address signals, but does show control

signals. Petitioner further asserts that Patent Owner's argument that the control signals contain the bank address signals is belied by the fact that all other address signals are set out in separate lines in the figures. *Id.* at 35 (citing PO Resp. 63–68). In addition, Petitioner contends that Patent Owner's argument that commands would include bank address signals is incorrect because those commands would go to the memory devices, and not to the logic performing rank multiplication. *Id.* (citing Ex. 2103, 109:3–110:8, 111:3–13, 112:15–113:23, 114:23–116:4). Rank multiplication is achieved by the logic element using two input chip select signals to generate one of four output chip select signals to select one of the four ranks of memory devices. *See, e.g.*, Pet. 6–7; Ex. 1003 ¶¶ 173, 190; PO Resp. 1–3; Ex. 2062 ¶¶ 31–35.

Petitioner further notes that Patent Owner argued during reexamination that rank multiplication can be performed by row or column address and not bank address signals. Pet. 7; Pet. Reply 35. For the same reason, Petitioner argues that the '244 provisional's reference to using "an address signal" is not a disclosure of using a "bank address signal" for rank multiplication. *Id.* at 35–36 (citing PO Resp. 69, 72; Ex. 1005 ¶ 10, Fig. 1 ("A_{n+1}")).

Petitioner further contends that Patent Owner asserted that "bank address" signals were known for "DDR" memory devices, but argues that this is an obviousness argument, and obviousness is insufficient to show an actual disclosure of the '244 provisional that would demonstrate that the inventors had possession of how to use "bank address signals" for rank multiplication. *Id.* at 36 (citing *Ariad*, 598 F.3d at 1352; *Rivera v. ITC*, 857 F.3d 1315, 1322 (Fed. Cir. 2017)). Petitioner further argues that the '244

provisional does not even disclose "DDR memory devices" and that Patent Owner makes another obviousness argument based on "DRAM" devices, many of which were not capable of double-data-rate (DDR) operation. *Id.* (citing Ex. 1034, 5–6). Petitioner argues that the '244 patent mentions "data" only once, but does not explain or illustrate the data strobe lines (DQS) for DDR transactions, or how to avoid BBARX collisions for DDR devices. *Id.* at 36–37 (citing Ex. 1034, 6–7 (Figs. 12, 13); Ex. 1101, 80:4–81:16).

Patent Owner replies that the written description requirement does not require the exact terms appearing in the claim to be used *in haec verba* and asserts that Petitioner's arguments fail to consider what a POSITA would have recognized as opposed to what the specification states verbatim. PO Sur-Reply 22. Patent Owner reiterates that the control signals mentioned in the '244 provisional would include bank address signals. *Id.* at 22–28. Patent Owner further asserts that DDR or DDR2 SDRAMs were the most commonly available DRAM devices at the time of the '244 provisional and that a POSITA would have understood that its teachings pertained to such devices. *Id.* at 23–28.

We agree with Petitioner that the '244 provisional does not provide written description support under § 112 ¶ 1 for claim 16 of the '912 patent. There is no mention of "bank address" signals in the '244 provisional. In order to find that "bank address" signals are present, according to Patent Owner's arguments and the evidence presented, one would have to (1) assume at least that the '244 provisional pertains to DDR memory modules (when there is no mention of DDR and there were other types of DRAM devices on the market) because Figure 1 suggests them by its use of

chip select signals and the term "rank," and because they were the most common at the time; (2) understand that DDR DRAMs use bank address signals according to the JEDEC standards; (3) recognize that bank address signals are not mentioned in the '244 provisional; (4) infer that bank address signals would be included as part of the control signals (even though the other address signals are explicitly mentioned and set out separately); and (5) infer that the bank address signals are used for rank multiplication (when row/ and column/address could have been used for this purpose). This is a chain of inferences too long and speculative to show that the '244 provisional demonstrates that the inventors had possession of the subject matter of claim 16.

b) '436 Patent

Petitioner also contends that the '436 patent fails to disclose a "circuit" comprising "a logic element" and "a register" as required by limitation [16.c] of claim 16 of the '912 patent. Pet. 64 (citing Ex. 1003 ¶ 190).

Patent Owner argues that the '436 patent teaches that "the logic element [] 640 comprises a programmable-logic device (PLD) 642" that "uses sequential and combinatorial logic procedures" to produce gated CAS signals or gated chip-select signals for each of the four ranks in Figure 11A of the '436 patent. PO Resp. 55 (citing Ex. 1009, 17:41–45, 18:3–11) (emphasis omitted). Patent Owner argues that Petitioner's expert, Dr. Wolfe, establishes that a POSITA would understand that PLD 642 includes a logic element to perform sequential and combinatorial logic, and that the sequential logic would include a register to store state values. *Id.* at

55–56 (citing Ex. 2103, 117:16–119:18; Ex. 1009, 17:41–45, 18:3–11; Ex. 2062 ¶ 78).

Patent Owner's arguments are not persuasive to demonstrate that the '436 patent provides written description support for claim 16 of the '912 patent. First, the '436 patent teaches that in certain embodiments its logic element 640 comprises a PLD 642 that uses sequential and combinatorial logic procedures. Ex. 1009, 17:41–45, 18:3–11. Under Patent Owner's arguments, a POSITA would have had to infer that "sequential procedures" requires a register when there is no mention of this in the '436 patent, and when other types of devices, such as flip-flops and memory, could hold state as well.[7] For example, Dr. Brogioli recognizes that devices other than a register could be used when he refers to a "*storage* or register" as holding state (Ex. 2062 ¶ 78 (emphasis added)), as does Dr. Wolfe when he refers to a "register or an *equivalent*" (Ex. 2103, 118:16–20 (emphasis added)).

Furthermore, even assuming Patent Owner is correct that a "sequential procedure" implies the existence of a register, that register would be, according to the '436 patent, part of logic element 640. Ex. 1009, 17:41–45, 18:3–11. In contrast, claim 16 recites that "the circuit comprises a logic

[7] Sequential Logic Circuits and the SR Flip-flop (electronics-tutorials.ws) https://www.electronics-tutorials.ws/sequential/seq_1.html (last viewed 4/12/2024) ("Unlike **Combinational Logic** circuits that change state depending upon the actual signals being applied to their inputs at that time, **Sequential Logic** circuits have some form of inherent 'Memory' built in. . . . bistable latches and flip-flops are the basic building blocks of sequential logic circuits. Sequential logic circuits can be constructed to produce either simple edge-triggered flip-flops or more complex sequential circuits such as storage registers, shift registers, memory devices or counters"). Ex. 3021.

element and a register." Ex. 1001, 3:17–18 (reexamination certificate). In other words, claim 16 recites that the "logic element" and "register" are two different things whereas the '436 patent describes the register as included in the logic element.

Moreover, Petitioner argues that Patent Owner did not show that the '436 patent provides written description support for limitation [16.e] requiring that "the command signal is transmitted to only one DDR memory device at a time." Pet. Reply 29 (citing Ex. 1101, 107:24–108:12, 113:1–114:8, 115:16–116:24, 118:6–119:10) (emphasis omitted). Patent Owner argues that this is a new argument. Paper 87, 1. Petitioner alleged, however, that the '436 patent lacked written description support and provided specific examples in the Petition. Pet. 64. In its Response, Patent Owner argued that the '436 patent supports claim 16 of the '912 patent. PO Resp. 54–62. Petitioner's argument in its Reply has nexus and was responsive to Patent Owner's argument in its Response, and was a fair extension of the previously raised Petition argument that the '436 patent lacks support for claim 16 and providing examples to explain why. *Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1385 (Fed. Cir. 2023) (petitioner's reply argument is not new if it has nexus and is responsive to patent owner's response argument, and is a fair extension of argument raised in petition). In any event, Patent Owner had the opportunity to respond to Petitioner's Reply arguments, and availed itself of that opportunity. PO Sur-Reply 28–40.

Patent Owner further argues that, under Petitioner's theory, the '436 patent's reference to "[o]ther numbers of memory components 610 in each of the ranks 620, 625, 630, 635 are compatible with embodiments described

herein" means that there could be only one memory device per rank, and that a command signal would thus be sent to only one device at a time, which would satisfy limitation [16.e]. PO Sur-Reply 39–40 (citing Ex. 1009, 17:11–13) (alteration in original).

Even if we accept Patent Owner's argument as correct and assume it does not constitute a new argument as Petitioner alleges (*see* Paper 86), this would not negate the other discussed deficiencies in the '436 patent's written description.

Furthermore, to antedate Ellsberry based on the '436 patent, Patent Owner must show that the '436 patent provides written description support for all of the limitations of claim 16. Patent Owner, however, only addresses in its Response how the '436 patent allegedly provides written description support for "each disputed limitation," i.e., those raised by Petitioner. PO Resp. 54–62. This is insufficient because, "to gain the benefit of the filing date of an earlier application under 35 U.S.C. § 120, each application in the chain leading back to the earlier application must comply with the written description requirement of 35 U.S.C. § 112." *Zenon Env't, Inc. v. U.S. Filter Corp.*, 506 F.3d 1370, 1378 (Fed. Cir. 2007) (quoting *Lockwood*, 107 F.3d at 1571); *see also In re Hogan*, 559 F.2d 595, 609 (CCPA 1977) ("[T]here has to be a continuous chain of copending applications each of which satisfies the requirements of § 112 with respect to the subject matter presently claimed." (quoting *In re Schneider*, 481 F.2d 1350, 1356 (CCPA 1973)) (alteration in original).

To show that claim 16 is entitled to the benefit of the March 7, 2005, filing date of the '436 patent, Patent Owner had "to show not only the existence of the earlier application [the '436 patent], but why the written

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description in the earlier application supports the claim." *Tech. Licensing Corp. v. Videotek, Inc.*, 545 F.3d 1316, 1327 (Fed. Cir. 2008). "In the context of the allegedly anticipating [Ellsberry] prior art, that means producing sufficient evidence and argument to show that an ancestor to the ['912] patent, with a filing date prior to the [Ellsberry] date, contains a written description that supports all the limitations of claim [16]." *Id.* Patent Owner did not endeavor to do this as to all limitations of claim 16 with respect to the '436 patent, and, therefore, Patent Owner's attempt to gain the benefit of the filing of the '436 patent fails for this additional reason.

For the foregoing reasons, we determine that the '668, '595, and '244 provisionals and the '436 patent do not provide written description support under § 112 ¶ 1 for claim 16 of the '912 patent. Thus, we do not reach the parties' remaining arguments such as whether the '436 patent describes that row and/or bank address signals are used to generate output signals, or whether the '244 provisional or '436 patent address BBARX collisions. PO Resp. 56–62, Pet. Reply 29–34.

2. Printed Publication

Petitioner contends that Ellsberry is prior art to claim 16 of the '912 patent under §§ 102(a) and (e), and renders the claim obvious under § 103(a). Pet. 4, 20–21 (citing § VI.B.1; Ex. 1003 ¶¶ 189–196). Patent Owner argues that Ellsberry was not published until December 2006, after the invention date of the '912 patent, and thus is not a "printed publication" under § 311(b). PO Resp. 54. Petitioner replies that Patent Owner's argument that Ellsberry is not prior art as of its pre-AIA § 102(e) date is legally incorrect, as the Board has repeatedly held. Pet. Reply 16 (citing

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Exs. 1098 and 2063 (same), 7–10; Ex. 1099, 27–29; Ex. 1100, 29; MPEP § 2217).

We agree with Petitioner on this issue, which is currently on appeal before the Court of Appeals for the Federal Circuit. *Lynk Labs, Inc. v. Samsung Electronics Co., Ltd.*, Appeal No. 23-2346, Doc. 14, page 15 (Fed. Cir. Jan. 10, 2024).

In an *inter partes* review, a petitioner "may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or ***printed publications***." 35 U.S.C. § 311(b).

Ellsberry is a printed publication, having been published in December 2006, as Patent Owner acknowledges. *See* Ex. 1037, code (43) (publication date of Dec. 7, 2006); *see also* PO Resp. 54 (acknowledging publication in December 2006). Ellsberry is prior art at least under 35 U.S.C. § 102(e)(1), being "an application for patent, ***published*** under section 122(b), by another filed in the United States before the invention by the applicant for patent." *See* Ex. 1037, code (22) (filing date of June 1, 2005). Thus, Petitioner asserts a permissible ground of unpatentability under 35 U.S.C. § 311(b) because it argues that claim 16 is unpatentable under 35 U.S.C. § 103(a) on the basis of prior art (Ellsberry), which is a printed publication.

Accordingly, we determine that Ellsberry is prior art to the '912 patent at least under pre-AIA 35 U.S.C. § 102(e)(1).

3. Ellsberry (Ex. 1037)

Ellsberry is titled "Capacity-Expanding Memory Device." Ex. 1037, code (54). "A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from

memory devices communicatively coupled to the memory bank switch." *Id.* at code (57). "By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system." *Id.*

Figure 2 of Ellsberry is shown below.

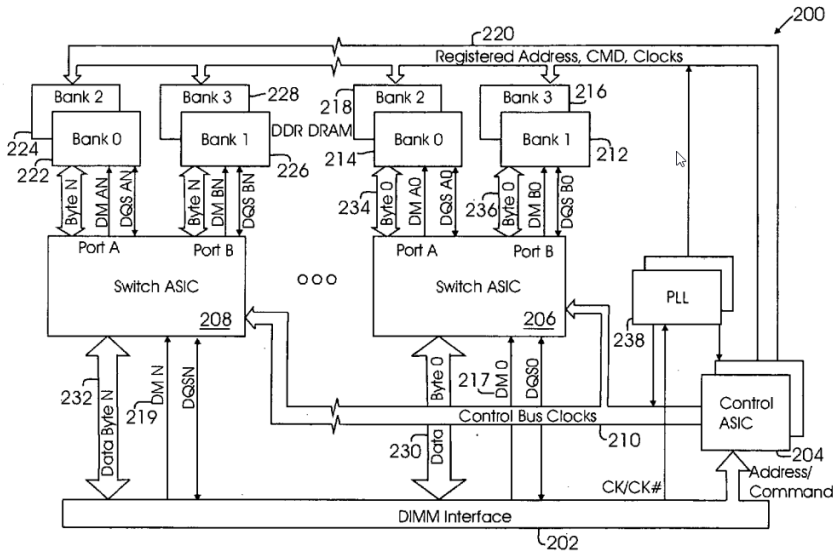

Fig. 2

Figure 2 "illustrates a block diagram of a capacity-expanding memory system 200 according to one embodiment." *Id.* ¶ 28. In Figure 2, system 200 has a DIMM interface 202 that couples to a "memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted." *Id.* "The capacity-expanding feature of the invention is accomplished by a combination of control unit 204 and one or more memory bank switches 206 & 208." *Id.* Figure 2 of Ellsberry illustrates system 200 with control ASIC 204 that receives addresses and commands from DIMM interface 202 and generates corresponding control signals on bus 210 and addresses on bus 220 to selectively connect memory banks 212–228 to DIMM interface 202 via switch ASICs 206, 208. *Id.* ¶¶ 28–29.

Figure 12 of Ellsberry is shown below.

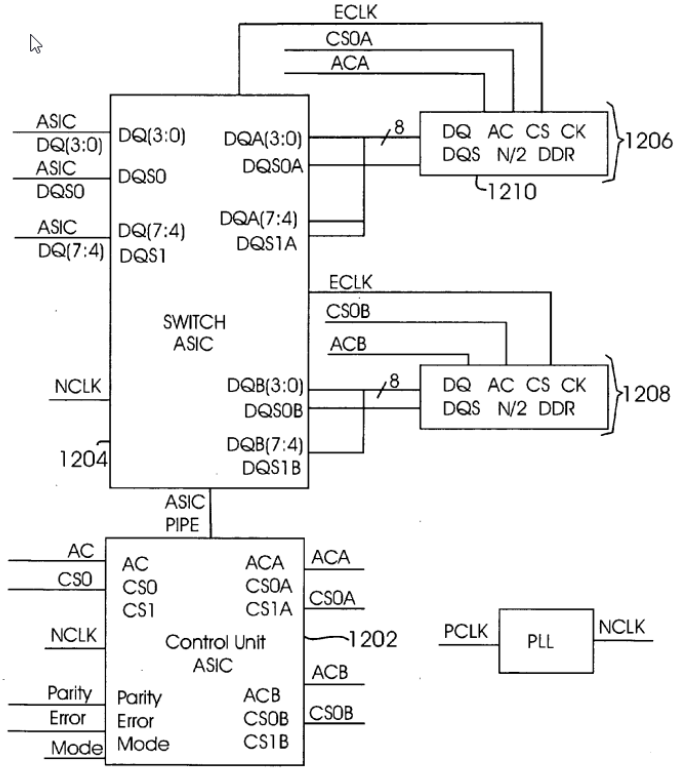

Fig. 12

Figure 12 of Ellsberry shows another configuration of the control unit and bank switch. *Id.* ¶ 52. In Figure 12, a single chip-select memory configuration includes one control unit 1202 and one bank switch 1204 which are used to control two memory banks 1206, 1208, each memory bank having one memory device 1210. *Id.* ¶ 55.

4. Correspondence of Ellsberry to Claim 16

Petitioner contends that Ellsberry teaches or suggests all limitations of claim 16. Pet. 69–111.

The preamble limitation [16.pre] of claim 16 recites "memory module connectable to a computer system." Ex. 1001, 3:9–11 (reexamination certificate). Petitioner contends that Ellsberry describes a memory module 106 with a capacity expanding device 108, connected to a computer system

100 that includes a processing unit 102 and I/O controller 104. Pet. 69 (citing Ex. 1037 ¶¶ 23, 27, Fig. 1; Ex. 1003 ¶¶ 198–199).

Patent Owner does not dispute that Ellsberry discloses the preamble limitation [16.pre].

Petitioner shows that the preamble limitation [16.pre] of claim 16 is taught by Ellsberry. It is thus unnecessary for us to determine whether the preamble is limiting.

Claim 16 further recites limitation [16.a] as "a printed circuit board." Ex. 1001, 3:12 (reexamination certificate). Petitioner contends that Ellsberry teaches a memory module with a printed circuit board. Pet. 72–73 (citing Ex. 1037 ¶ 2, Fig. 5).

Patent Owner does not dispute that Ellsberry discloses limitation [16.a].

Petitioner shows that limitation [16.a] of claim 16 is taught by Ellsberry.

Claim 16 further recites limitation [16.b] as "a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board." Ex. 1001, 3:13–16 (reexamination certificate). Petitioner contends that Ellsberry teaches DDR and DDR 2 memory devices mounted on a circuit board. Pet. 73–74 (citing Ex. 1037 ¶¶ 3, 23, 26, 46; Ex. 1038, 4, 23; Ex. 1003 ¶¶ 209–213).

Claim 16 further recites limitation [16.b.i] as "the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks." Ex. 1001, 3:14–16 (reexamination certificate). Petitioner contends that Ellsberry discloses a memory module with two memory devices arranged in two single device ranks controlled by separate

chip select signals (CS_{0A}, CS_{0B}). Pet. 74–76 (citing Ex. 1037 ¶¶ 3, 26, 30, 32, Fig. 12; Ex. 1003 ¶¶ 215, 218–221). Petitioner thus contends "a first number of DDR memory devices" is two and the "first number of ranks" is two. *Id.* Alternatively, Petitioner contends "a first number of DDR memory devices" is four and the "first number of ranks" is four. *Id.* at 76 (citing Ex. 1037, Fig. 13; Ex. 1003 ¶ 216). Petitioner's expert states that "bank" (as used in Ellsberry) and "rank" were interchangeable terms at the time. Ex. 1003 ¶ 76. Both terms are mentioned in Ellsberry. *See, e.g.*, Ex. 1037, code (57), Fig. 9.

Patent Owner contends that limitation [16.b.i] of claim 16 requires multiple-device ranks. PO Resp. 75–82. For the reasons discussed in § II.C, *supra*, and addressed further with respect to limitation [16.e], *infra*, we determine that "rank" can include only "one memory device." Thus, we disagree with Patent Owner's attempted distinction over the art.

Petitioner shows that limitations [16.b] and [16.b.i] of claim 16 are taught by Ellsberry.

Limitation [16.c] of claim 16 recites "a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register." Ex. 1001, 3:17–18 (reexamination certificate). Petitioner contends that Ellsberry teaches this limitation. Pet. 77–80 (citing Ex. 1003 ¶¶ 224–225). Specifically, Petitioner contends that Ellsberry teaches that the "circuit" is a control unit ASIC, that the "logic element" is a control block, and that the "register" corresponds to register 302. *Id.* at 77.

Petitioner contends that Ellsberry discloses limitation [16.c.i] of claim 16 reciting "the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one

row/column address signal, bank address signals, and at least one chip-select signal." *Id.* at 75–78; Ex. 1001, 3:18–22 (reexamination certificate). Specifically, Petitioner contends that Ellsberry teaches a command processing system 300 with a control block possessing address/command decode logic 304, configuration decode logic 306, and bank switch state machine 308. Pet. 78–79 (citing Ex. 1037, Fig. 3). Petitioner notes that Ellsberry describes memory addresses and command information are received from DIMM interface 202, buffered in register 302, decoded in logic 304, and that a bank switch state machine 308 determines which memory bank should be activated or accessed. *Id.* at 79 (citing Ex. 1037 ¶ 39). Petitioner contends that a person of ordinary skill in the art would have understood that Ellsberry's control block includes a "logic element" and "register" receiving row/column address signal, bank address signals, and chip-select signals. *Id.* (citing Ex. 1003 ¶ 224).

Petitioner contends that Ellsberry teaches limitation [16.c.ii] of claim 16 reciting "the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks." Pet. 86–95 (citing Ex. 1003 ¶¶ 232–243); Ex. 1001, 3:22–28 (reexamination certificate). Specifically, Petitioner contends that Ellsberry teaches that the "set of input signals" corresponding to a single DDR2 memory device and the memory module uses two DDR2 memory devices to simulate a larger memory device. *Id.* at 87–88 (citing Ex. 1037, Figs. 7D, 12 [signals AC, C0]; Ex. 1003 ¶ 233). Petitioner contends that Ellsberry teaches that the "set of input signals" includes bank address, row address,

and column address signals consistent with the JEDEC standard. *Id.* at 87–95 (citing Ex. 1037, Figs. 7D, 8A).

Petitioner further contends the "second number of DDR memory devices" is one, which is less than the "first number of DDR memory devices," which is two, and that the "second number of ranks" is one which is less than the "first number of ranks," which is two. *See* Ex. 1037, Fig. 12. According to Petitioner, these relations would also be satisfied for the alternative when the "first number of DDR memory devices" is four and the "first number of ranks" is four. *See* Pet. 76 (citing Ex. 1037, Fig. 13).

Patent Owner contends that limitation [16.c.ii] of claim 16 requires multiple-device ranks. PO Resp. 75–82. As discussed above in § II.C, *supra*, and addressed further regarding limitation [16.e], *infra*, we determine that "rank" can include only one memory device. Thus, we disagree with Patent Owner's attempted distinction over the art.

Petitioner contends that Ellsberry teaches the limitation [16.c.iii] of claim 16 reciting "the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks." Pet. 95–99 (citing Ex. 1037, Figs. 12, 13; Ex. 1003 ¶¶ 244–246); Ex. 1001, 3:28–31 (reexamination certificate). Petitioner contends that Ellsberry teaches that "the circuit" corresponds to the Control Unit ASIC and that the "set of output signals" corresponds to Ellsberry's signals ACA, CS0A, ACB, CS0B that are responsive to the "set of input signals" corresponding to Ellsberry's signals AC, CS0. Pet. 95–96 (citing Ex. 1037, Fig. 12). Petitioner contends that Ellsberry teaches that the "circuit generat[es] the set of output signals in response to the set of input signals" because the

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relationship between the input signals and output signals is described in Ellsberry. *Id.* at 97–99 (citing Ex. 1037 ¶¶ 37, 42, 40, Figs. 7D, 8A; Ex. 1003 ¶¶ 232–243, 246). Petitioner further contends that "the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks" corresponds to single device ranks 1206, 1208 corresponding to chip-select signals CS0A, CS0B. *Id.* at 95–96 (citing Ex. 1037, Fig. 12). In addition to this embodiment with two single-device ranks, Petitioner contends similar mappings apply to Ellsberry's embodiment with four-single device ranks. *Id.* (citing Ex. 1037, Fig. 13).

Petitioner contends that Ellsberry teaches the limitation [16.c.iv] of claim 16 reciting "wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks." Pet. 99–103 (citing Ex. 1003 ¶¶ 248–254); Ex. 1001, 3:32–37 (reexamination certificate). Petitioner contends that the "command signal" corresponds to a read or write command under the JEDEC standard. Pet. 99 (citing Ex. 1029, 6, 49). Petitioner further contends that Ellsberry selects "one" rank and transmits the command signal to the selected "one" rank. *Id.*

Furthermore, Petitioner notes that Ellsberry states "[t]he control unit maps a received logical address to a physical address corresponding to the particular memory bank configuration employed. It also directs commands to the memory banks to indicate which memory bank should be operational and which one should be passive (do nothing)."

Id. at 100 (quoting Ex. 1037 ¶ 11). Petitioner further notes that Ellsberry states that the control unit may send either the same command to both memory banks or different commands to each memory bank with a "no operation" command to the other memory bank. *Id.* at 100–01 (citing Ex. 1037 ¶ 42, Fig. 8A; Ex. 1029, 48, 49; Ex. 1003 ¶¶ 229, 233–235, 249, 250). Petitioner contends this Ellsberry disclosure is similar to Example 1 of the Verilog code in the '912 patent. *Id.* at 102 (citing Ex. 1003 ¶ 251). Petitioner contends another embodiment of Ellsberry selects a target rank based on a row address bit that is bank specific, like Example 2 of the Verilog code in the '912 patent. *Id.* (citing Ex. 1003 ¶ 252).

Patent Owner does not dispute that Ellsberry teaches limitations [16.c], [16.c.i], [16.c.iii], and [16.c.iv].

Petitioner has shown that Ellsberry teaches limitations [16.c], [16.c.i]. [16.c.ii], [16.c.iii], and [16.c.iv] of claim 16.

Claim 16 recites a limitation [16.d] as "a phase-lock loop device coupled to the printed circuit board." Petitioner contends that Ellsberry teaches limitation [16.d]. Pet. 103–06 (citing Ex. 1037 ¶ 2, Figs. 12, 13; Ex. 1003 ¶¶ 255–257). Specifically, Petitioner contends that Ellsberry teaches a "phase lock loop (PLL) 238 [(yellow)] regenerates a clock signal that can be used by the components on the memory system 200." *Id.* at 104 (citing Ex. 1037 ¶ 30, Fig. 2; Ex. 1003 ¶ 256) (alteration in original). Petitioner further contends that Ellsberry's PLL is coupled to the circuit board. *Id.* at 105 (citing Ex. 1037 ¶ 48, Fig. 5). In particular, Petitioner contends that Ellsberry teaches that external phase lock loop (PLL) 514 receives a clock signal from the edge interface 506 and provides a clock

signal to the memory module components. *Id.* (citing Ex. 1037 ¶¶ 39, 45, 48, 49, Figs. 2–4, 12; Ex. 1003 ¶ 257).

Claim 16 recites the limitation [16.d.i] as "the phase-lock loop device is operatively coupled to the plurality of DDR memory devices, the logic element, and the register." Ex. 1001, 3:39–41 (reexamination certificate). Petitioner contends that Ellsberry discloses limitation [16.d.i]. Pet. 106–09 (citing Ex. 1003 ¶¶ 259–263). Specifically, Petitioner contends Ellsberry's PLL receives a clock signal PCLK and generates a clock signal NCLK that is provided to the Control Unit ASIC and Switch ASIC. *Id.* at 106 (citing Ex. 1037 ¶ 30, Figs. 2–5, 12, 13; Ex. 1003 ¶¶ 255–257). Petitioner contends the Switch ASIC then uses the clock NCLK to derive the clock ECLK provided to the memory devices. *Id.* Petitioner thus contends Ellsberry's PLL is also operatively coupled to the plurality of DDR memory devices. *Id.* at 106–07 (citing Ex. 1037, Fig. 12; Ex. 1003 ¶ 260).

Petitioner contends Control Unit ASIC uses the clock signal NCLK from the PLL to derive its own local clocks that are provided to both the Control Block and register 302 in the Control Unit ASIC. *Id.* at 108 (citing Ex. 1037, Figs. 3, 12, 13; Ex. 1003 ¶ 261).

Petitioner contends that, to the extent Ellsberry does not sufficiently disclose a local clock of the Control Unit ASIC is provided to the register 302, a person of ordinary skill in the art would have understood that register 302 is clocked by a local clock signal as indicated by the small triangle at the bottom of the register 302. *Id.* at 108–09 (citing Ex. 1003 ¶ 262). Petitioner notes that Ellsberry states that the PLL "regenerates a clock signal that can be used by the components on the memory system 200." *Id.* at 109 (quoting Ex. 1037 ¶ 30). Thus, Petitioner contends that Ellsberry's PLL provides a

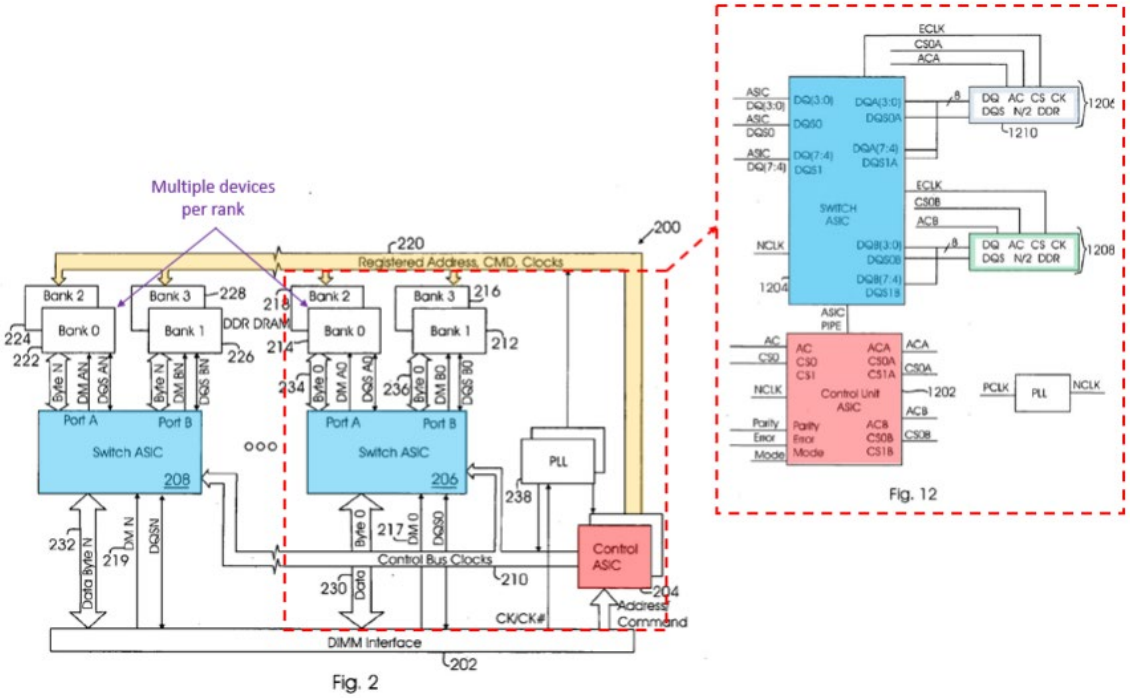
clock to the Control Unit ASIC, which can be used to operate its components, including the register 302, and that a person of ordinary skill in the art "would have understood and been motivated to use the local clock in the Control Unit ASIC to operate the register 302." *Id.* (citing Ex. 1003 ¶ 262).

Patent Owner does not dispute that Ellsberry teaches limitations [16.d] and [16.d.i].

Petitioner has shown that Ellsberry teaches limitations [16.d] and [16.d.i] of claim 16.

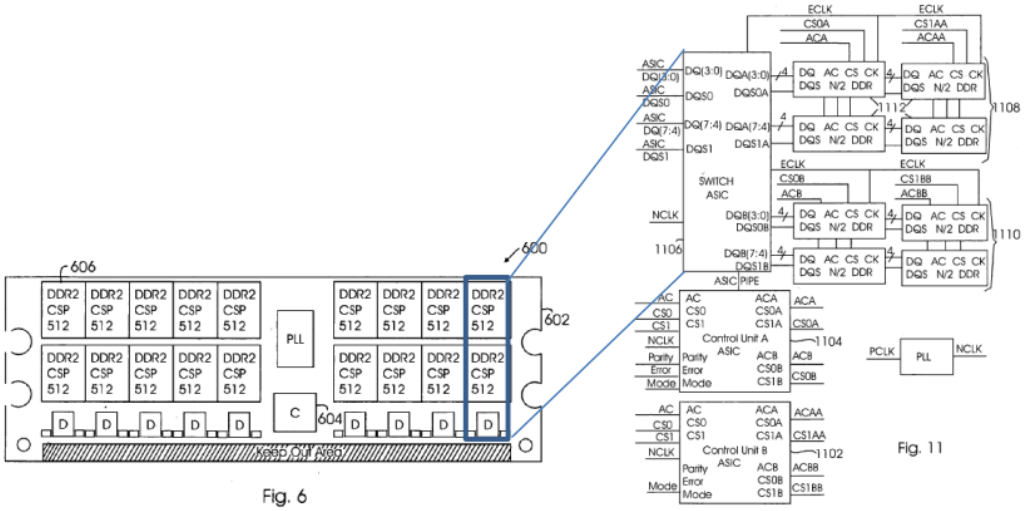
Petitioner contends that Ellsberry discloses limitation [16.e] of claim 16 reciting "wherein the command signal is transmitted to only one DDR memory device at a time." Pet. 109–11 (citing Ex. 1003 ¶¶ 264–265); Ex. 1001, 3:42–43 (reexamination certificate). Specifically, Petitioner contends that Ellsberry teaches that an Activate, Write or Read command signal is transmitted to only the selected memory device and the other memory device receives a no-operation command. Pet. 109–11 (citing Ex. 1037 ¶¶ 10, 33, 42, Figs. 8A, 12; Ex. 1003 ¶ 264).

Patent Owner argues that the Board's prior decision in IPR2023-00203 that Ellsberry's Figure 12 discloses a complete memory module was incorrect. PO Resp. 75 (citing Ex. 2063, 10–11; Ex. 2062 ¶ 239). Patent Owner argues that Ellsberry's Figures 10–13 each depict one data group of a memory module, not the entire memory module. *Id.* at 75–76 (citing Ex. 2062 ¶ 240). In support of its argument, Patent Owner provides the following figure, which is an annotated composite of Ellsberry's Figures 2 and 12.



Id. at 76 (citing Ex. 1037, Figs. 2, 12). Patent Owner contends that Ellsberry's Figure 12 shows a data group which is a part of the entire memory module shown in Ellsberry's Figure 2 which has multiple memory devices per rank. *Id.* at 76–77.

Patent Owner also argues that Ellsberry's Figures 6 and 11, shown below, support its argument that each rank includes multiple memory devices.



Id. at 77. Patent Owner asserts that Figure 6 shows multiple data groups per rank even though Figure 11, like Figure 12, shows only a single bank switch and one data group. *Id.* (citing Ex. 1037 ¶ 51; Ex. 2062 ¶¶ 242–243). Patent Owner argues that "a POSITA would understand that Figures 10–13 are used to illustrate how each data group and switch on the memory module can be implemented, and not how many data groups the memory modules are to have." *Id.* at 77–78 (citing Ex. 1038, 50–51, 57, 77, 81; Ex. 2061, 40 n.11; Ex. 1037 ¶ 52; Figs. 2, 5–6; Ex. 2062 ¶ 244).

Patent Owner further argues that Petitioner's experts, Dr. Wolfe and Dr. Subramanian, testified that they had never used or known of a memory module with DDR or newer generations of DRAMs that was 16 or fewer bits wide. *Id.* at 78 (citing Ex. 2103, 146:2–12, 155:13–25; Ex. 2104, 258:3–259:7). Patent Owner asserts that from a POSITA's perspective there were no known 8-bit-wide memory modules, especially JEDEC-style ones, and that 8-bit-wide memory modules would be going against the industry trend of increasing module data width. *Id.* at 79 (citing Ex. 2103, 146:2–12, 155:13–25; Ex. 2104, 258:3–259:7; Ex. 1034, 20–21; Ex. 2062 ¶¶ 245–246).

Patent Owner further argues that the Board questioned why Ellsberry needed to comply with JEDEC, and asserts that Ground 3 relies on implementations that follow the JEDEC standard but there is no substantial evidence that a JEDEC-compliant memory module would have a single device per rank. *Id.* at 79–80 (citing Ex. 2063, 12; Pet. 93; Ex. 1037 ¶¶ 50, 57; Ex. 1029, 1–3; Pet. 69–111; Ex. 1032, 4.20.4-5; Ex. 2062 ¶ 247; Ex. 2103, 46:3–15; Ex. 2112, 1; Ex. 1090, 86:19–87:17).

Patent Owner further criticizes Petitioner's contention that it would have been obvious to make a module with only a single data group because it would have been simpler to make, would require fewer parts, and would present fewer error sources. *Id.* at 81 (citing Pet. 76; *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016)). Patent Owner argues that there is no evidence that a POSITA had ever thought of constructing an 8-bit wide DDR memory module. *Id.* at 81–82 (citing Ex. 2062 ¶ 251; Ex. 2103, 146:2–12, 155:13–25; Ex. 2104, 258:3–259:13). Patent Owner further asserts this does not make any technical or economic sense, and "[i]f simplicity is desired, Ellsberry would just couple a 1Gbx8 (or 512Mbx8) device directly with the CPU, as the cost saved by removing PCB, PCB routing, costly switch ASIC and control ASIC would more than offset any potential price difference between a single 1Gbx8/512Mbx8 and two 512Mbx8/256Mbx8 devices." *Id.* at 82 (citing Ex. 2062 ¶ 252). Patent Owner concludes that Petitioner is using the claim as a roadmap to piece together the modifications, and is engaging in hindsight. *Id.*

Petitioner argues that Ellsberry does not require multiple switches. Pet. Reply 38 (citing PO Resp. 75–78; Pet. 74–77; Ex. 2103, 157:1–161:3, 164:6–15, 177:13–178:3; Ex. 1037 ¶ 28). Petitioner further contends that

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Ellsberry describes Figure 12 as a memory module and not just part of a module, and makes clear that a memory module just requires one or more memory devices. *Id.* (citing Ex. 1037 ¶¶ 21, 23, 52). Petitioner further states that Ellsberry specifically claims a "memory module" with "one or more memory bank switches." *Id.* (citing Ex. 1037, claims 6, 8).

In addition, Petitioner argues that claim 16 does not exclude memory modules that are 8- or 16-bits wide. *Id.* at 39 (citing *id.* at 5; PO Resp. 78–82). Petitioner contends that the JEDEC SPD standards for memory modules specifically permitted those widths. *Id.* (citing *id.* at 14–15). Moreover, Petitioner asserts that Perego-422 specifically taught those widths. *Id.* (citing *id.* at 18, 21–22, where W_A=W_{DP}). Furthermore, Petitioner states that the Board explained that memory modules such as Ellsberry's Figure 12 could still "expand the capacity" of the memory module with multiple ranks. *Id.* (citing Exs. 1098 and 2063 (same), 12).

In Sur-Reply, Patent Owner asserts that JEDEC specifications do not permit memory modules below 32-bits wide. PO Sur-Reply 40–42 (citing Ex. 1006, 8; Ex. 1107, 8). Patent Owner further asserts that Perego-422 and Ellsberry are "completely different architectures." *Id.* at 42 (citing Ex. 1035; Ex. 1037). Patent Owner contends that while Perego-422 can program WA for different access cycles, Ellsberry's data access width is fixed. *Id.* Patent Owner contends there is a lack of any known examples of x8 or x16 DDR1 or DDRs SDRAM modules and that a POSITA would not have found it obvious to construct such a memory module. *Id.* (citing Pet. 81–86).

The parties' disputes concerning limitation [16.e] can be resolved by inspection of Ellsberry. Ellsberry states

> FIGS. 10, 11, 12 and 13 illustrate different configurations of *memory modules* (e.g., DIMMs) that can be built using *combinations of the control unit and bank switch* according to various embodiments of the invention.

Ex. 1037 ¶ 10. We understand this to mean that Figures 10–13 are memory modules notwithstanding that they could also be used as parts of a larger memory module according to Figure 2's configuration. That they are combinations of the control unit and bank switch (singular) means there could be only one bank switch in the memory module.

Ellsberry further states

> [t]he capacity-expanding feature of the invention is accomplished by a combination of a control unit 204 and ***one*** or more memory bank switches 206 & 208.

Id. ¶ 28. This confirms that a memory module may include only one memory bank switch, as shown in Figures 10–13.

Ellsberry's Figure 12 shows a memory module with

> one control unit 1202 and one bank switch 1204 [that] are used to control two memory banks 1206 & 1208, each memory bank having one memory device 1210.

Id. ¶ 55. Petitioner is correct that Ellsberry discloses transmitting a command (Activate, Write or Read) to only the selected one of the two memory devices in Figure 12, and a no-operation (NOP) command to the other memory device. Pet. 109–11 (citing Ex. 1037 ¶¶ 10, 33, 42, Figs. 8A, 12; Ex. 1003 ¶¶ 264–265).

Accordingly, we determine that Ellsberry discloses limitation [16.e] of claim 16 reciting "wherein the command signal is transmitted to only one DDR memory device at a time."

Thus, we do not agree with Patent Owner's arguments that Ellsberry's Figures 10–13 do not constitute respective memory modules, but are only parts of the memory module shown in Figure 2. As to Patent Owner's arguments concerning bit width, claim 16 does not require any particular bit width, so Patent Owner is arguing a feature that is not commensurate in scope with the claim. *In re Self*, 671 F.2d 1344, 1348 (CCPA 1982). Nor does claim 16 recite that the memory module is compliant with a JEDEC standard. Patent Owner also does not explain why a POSITA could not have drawn on teachings in JEDEC standards without fully complying with them as needed for a particular application.

Furthermore, Petitioner directs us to evidence that JEDEC standards permitted 8-bit and 16-bit wide modules. Pet. Reply 14–15 (citing Ex. 1107, 7–8, 13; Ex. 1106, 7–8, 13; Ex. 1101, 141:11–19, 144:10–147:25, 149:10–18, 151:3–153:22); *see* Ex. 1107, 8 (disclosing that "[b]yte 6 is used to designate the module's data width" and including a table indicating values from 0–255). Patent Owner cites this disclosure and asserts that "JEDEC specifications do not permit memory modules below 32-bit wide." PO Sur-Reply 40–42 (reproducing disclosure from Ex. 1107, 8 and Ex. 1106, 8). The cited portions, however, show that the data width can be defined below 32 bits given that a byte can represent 255 values as in Exhibit 1107. *See also* Ex. 1106, 8 (disclosing a "16 bit width identifier").

Moreover, we do not agree with Patent Owner's argument that claim 16 requires sending a command to a single device that is in a multi-device rank. A rank may have only one device for reasons explained in § II.C.

We determine that Petitioner has shown by a preponderance of the evidence that Ellsberry teaches or suggests each limitation of claim 16.

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5. Secondary Considerations

Patent Owner does not present objective evidence of non-obviousness other than to respond to Petitioner's assertion of evidence of "simultaneous invention." PO Resp. 82–83. As discussed, Ellsberry teaches all of the limitations of claim 16, and there is no objective evidence of non-obviousness in the record.

6. Conclusion

Petitioner has shown by a preponderance of the evidence that Ellsberry teaches or suggests each limitation of claim 16 of the '912 patent. Accordingly, Petitioner has shown by a preponderance of the evidence that claim 16 of the '912 patent is unpatentable as obvious over Ellsberry.

E. Obviousness of Claim 16 Over Perego-422 (Ground 1)

Our determination that claim 16 is obvious over Ellsberry (Ground 3) is dispositive. Therefore, we need not reach Petitioner's contention that claim 16 is obvious over Perego-422.

F. Obviousness of Claim 16 Over Perego-422 and Amidi (Ground 2)

Our determination that claim 16 is obvious over Ellsberry (Ground 3) is dispositive. Therefore, we need not reach Petitioner's contention that claim 16 is obvious over the combination of Perego-422 and Amidi.

G. Supplemental Information

Patent Owner sought to submit supplemental information in the form of testimony from a Micron representative concerning the meaning of the term "rank." Paper 72. As we determined that the intrinsic evidence is clear that a "rank" may include only one memory device, we do not and need not

resort to extrinsic evidence on this topic. Therefore, we dismiss Patent Owner's motion to introduce this extrinsic evidence.

H. Motion to Exclude

Petitioner sought to exclude Exhibits 1090, 2056, 2058, 2059, 2104, 2107, 2108, 2112, 2113, 2117 and portions of Exhibit 1101. Paper 89. Because we do not rely on any of these Exhibits in a manner adverse to Petitioner, we dismiss the Motion to Exclude as moot.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner establishes by a preponderance of the evidence that claim 16 of the '912 patent is unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claim 16 of the '912 patent has been shown to be unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Submit Supplemental Information is dismissed;

FURTHER ORDERED that Petitioner's Motion to Exclude is dismissed; and

FURTHER ORDERED that any party seeking judicial review must comply with the notice and service requirements of 37 C.F.R. § 90.2.[8]

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[8] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this

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Decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
16	103(a)	Perego-422		
16	103(a)	Perego-422, Amidi		
16	103(a)	Ellsberry	16	
Overall Outcome			16	

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