**IN THE UNITED STATES DISTRICT COURT**
**FOR THE EASTERN DISTRICT OF TEXAS**
**MARSHALL DIVISION**

| | | |
|---|---|---|
| **NETLIST, INC.**<br><br>Plaintiff,<br><br>v.<br><br>**SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC.**<br><br>Defendants. | )<br>)<br>)<br>)<br>)<br>)<br>)<br>)<br>)<br>)<br>)<br>)<br>)<br>)<br>)<br>) | Civil Action No.2:21-cv-463<br><br>JURY TRIAL DEMANDED |

**COMPLAINT**

1. Plaintiff Netlist, Inc. ("Netlist"), by its undersigned counsel, for its Complaint against defendants Samsung Electronics Co., Ltd. ("SEC"), Samsung Electronics America, Inc. ("SEA"), and Samsung Semiconductor, Inc. ("SSI") (collectively, "Samsung" or "Defendants"), states as follows, with knowledge as to its own acts, and on information and belief as to the acts of others:

2. This action involves three of Netlist's patents: U.S. Patent Nos. 10,860,506 (the "'506 Patent," Ex. 1), 10,949,339 (the "'339 Patent," Ex. 2), and 11,016,918 (the "'918 Patent," Ex. 3) (collectively, the "Patents-in-Suit").

## I. THE PARTIES

3. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Drive, Suite 100, Irvine, CA 92617.

4. On information and belief, SEC is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129 Samsung-ro, Yeongtong-gu, Suwon, Gyeonggi, 16677, Republic of Korea. On information and belief, SEC is the worldwide parent corporation for SEA and SSI, and is responsible for the infringing activities identified in this complaint. On information and belief, SEC's Device Solutions division is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, SEC is also involved in the design, manufacture, and provision of products sold by SEA.

5. On information and belief, SEA is a corporation organized and existing under the laws of the State of New York. On information and belief, SEA, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. Defendant SEA maintains facilities at 6625 Excellence Way, Plano, Texas 75023. SEA may be served with process through its registered agent for service in Texas: CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, Texas 75201. SEA is a wholly owned subsidiary of SEC.

6. On information and belief, SSI is a corporation organized and existing under the laws of the State of California. On information and belief, SSI, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined


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below. Defendant SSI maintains facilities at 6625 Excellence Way, Plano, Texas 75023. Defendant SSI may be served with process through its registered agent National Registered Agents, Inc., 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136. On information and belief, SSI is a wholly owned subsidiary of SEA.

7. On information and belief, Defendants have used, sold or offered to sell products and services, including the Accused Instrumentalities, in this judicial district.

## II. JURISDICTION AND VENUE

8. Subject matter jurisdiction is based on 28 U.S.C. § 1338, in that this action arises under federal statute, the patent laws of the United States (35 U.S.C. §§ 1, *et seq.*).

9. Each Defendant is subject to this Court's personal jurisdiction consistent with the principles of due process and/or the Texas Long Arm Statute.

10. Personal jurisdiction exists generally over the Defendants because each Defendant has sufficient minimum contacts and/or has engaged in continuous and systematic activities in the forum as a result of business conducted within the State of Texas and the Eastern District of Texas. Personal jurisdiction also exists over each Defendant because each, directly or through subsidiaries, makes, uses, sells, offers for sale, imports, advertises, makes available, and/or markets products within the State of Texas and the Eastern District of Texas that infringe one or more claims of the Patents-in-Suit. Further, on information and belief, Defendants have placed or contributed to placing infringing products into the stream of commerce knowing or understanding that such products would be sold and used in the United States, including in this District.

11. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b). For example, SEC maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district. As another example, SEA maintains a regular and established place of


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business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district. Venue is also proper for SSI because it maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district.

12. Defendants have not contested proper venue in this District. *See, e.g.*, Answer at ¶ 10, *Arbor Global Strategies LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-333, Dkt. 43 (E.D. Tex. Apr. 27, 2020); Answer at ¶ 29, *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-347, Dkt. 14 (E.D. Tex. Feb. 12, 2020).

## III. FACTUAL ALLEGATIONS

### Background

13. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

14. Netlist has a long history of being the first to market with disruptive new products such as the first load-reduced dual in-line memory module ("LR-DIMM"), HyperCloud®, based on Netlist's distributed buffer architecture later adopted by the industry for DDR4 LRDIMM. Netlist was also the first to bring NAND flash to the memory channel with its NVvault® NVDIMM. These innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate (DDR) technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory.


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15. Generally speaking, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard.

16. Memory modules are designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications. The structure, function, and operation of memory modules is defined, specified, and standardized by the JEDEC Solid State Technology Association ("JEDEC"), the standard-setting body for the microelectronics industry. Memory modules are typically characterized by, among other things, the generation of DRAM on the module (*e.g.*, DDR5, DDR4, DDR3) and the type of module (*e.g.*, RDIMM, LRDIMM).

**The Asserted Netlist Patents**

**<u>The '506 Patent</u>**

17. The '506 Patent is entitled "Memory Module With Timing-Controlled Data Buffering." Netlist owns the '506 Patent by assignment from the listed inventors Hyun Lee and Jayesh R. Bhakta. The '506 Patent was filed as Application No. 16/391,151 on April 22, 2019, issued as a patent on December 8, 2020, and claims priority to, among others, a utility application filed on July 27, 2013 (No. 13/952,599) and a provisional application filed on July 27, 2012 (No. 61/676,883).

18. Samsung had knowledge of the '506 Patent no later than August 2, 2021 via its access to Netlist's patent portfolio docket.

19. As described in the '506 Patent, in conventional memory modules, the "distribution of control signals and a control clock signal in the memory module is subject to strict constraints"

to ensure that memory devices on the memory module can be properly accessed. Ex. 1 at 2:16-17. For example, in some conventional memory modules, "control wires are routed so there is an equal length to each memory component, in order to eliminate variation of the timing of the control signals and the control clock signal between different memory devices in the memory modules." *Id.* at 2:20-24. But as noted in the '506 Patent, "[t]he balancing of the length of the wires to each memory devices compromises system performance, limits the number of memory devices, and complicates their connections." *Id.* at 2:24-27. In yet other conventional memory systems, the memory controller includes mechanisms for compensating for unbalanced wire lengths on the memory module. *Id.* at 2:30-32. However, with increasing memory operating speed and memory density "such leveling mechanisms are also insufficient to ensure proper timing of the control and/or data signals received and/or transmitted by the memory modules." *Id.* at 2:32-36.

20. The '506 Patent discloses a memory module operable in a memory system with a memory controller that includes memory devices, a module control circuit, and a plurality of buffer circuits coupled between respective sets of data signal lines in a data bus and respective sets of the memory devices. As summarized in the Abstract, "[e]ach respective buffer circuit is configured to receive the module control signals and the module clock signal, and to buffer a respective set of data signals in response to the module control signals and the module clock signal. Each respective buffer circuit includes a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals." *Id.*, Abstract.

21. The buffer circuits (118, highlighted below) are associated with respective groups of memory devices and are distributed across the memory module at positions corresponding to the respective groups of memory devices as illustrated in the exemplary configuration of Figure 2A.


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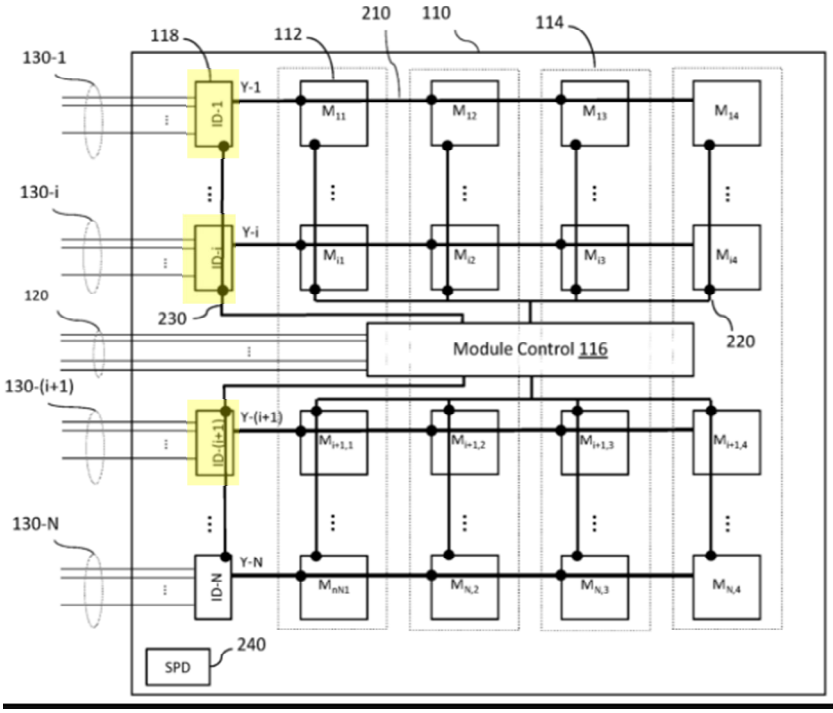


FIG. 2A

'506 Patent, Figure 2A. However, because the buffer circuits—or "isolation devices"—are distributed across the memory module, at high speeds of operation, the same set of module control signals may reach different buffer circuits at different times across one cycle of the system clock. *Id.* at 9:51-62 ("Because the isolation devices 118 are distributed across the memory module 110, during high speed operations, it may take more than one clock cycle time of the system clock MCK for the module control signals to travel along the module control signals lines 230 from the module control device 116 to the farthest positioned isolation devices 118, such as isolation device ID-1 and isolation device ID-(n−1) in the exemplary configuration shown in FIG. 2."). The '506 Patent discloses an embodiment wherein "each isolation devices includes signal alignment circuits that determine, during a write operation, a time interval between a time when one or more module control signals are received from the module control circuit 116 and a time when a write strobe or write data signal is received from the MCH 101. This time interval is used during a subsequent read operation to time the transmission of read data to the MCH 101, such that the read data follows a read command by a read latency value associated with the system 100." *Id.* at 10:11-21.

**The '339 Patent**

22. The '339 Patent is entitled "Memory Module With Controlled Byte-Wise Buffers." Netlist owns the '339 Patent by assignment from the listed inventors Hyun Lee and Jayesh R. Bhakta. The '339 Patent was filed as Application No. 15/470,856 on March 27, 2017, issued as a patent on March 16, 2021, and claims priority to U.S. Patent Application No. 12/504,131 filed on July 16, 2009, U.S. Patent Application No. 12/761,179 filed on April 15, 2010 and U.S. Application No. 13/970,606 filed on August 20, 2013.

23. Samsung had knowledge of the '339 Patent no later than August 2, 2021 via its access to Netlist's patent portfolio docket.

24. As described in the '339 Patent, in optimizing performance of memory subsystems (e.g. memory modules) "consideration is always given to memory density, power dissipation (or thermal dissipation, speed, and cost." Ex. 2 at 2:5-7. The '339 Patent further explains that "[g]enerally, these attributes are not orthogonal to each other, meaning that optimizing one attribute may detrimentally affect another attribute. For example, increasing memory density typically causes higher power dissipation, slower operational speed, and higher costs." *Id.* at 2:7-12. The '339 Patent is generally directed to a memory module optimized to reduce the load experienced by a system memory controller via the use of configurable data transmission circuits.

25. The '339 Patent discloses a memory module configured to communicate with a memory controller that includes DDR DRAM devices arranged in multiple ranks each of the same width as the memory module, and a module controller configured to receive and register input control signals for a read or write operation from the memory controller and to output registered address and control signals. As summarized in the Abstract, "[t]he registered address and control signals selects one of the multiple ranks to perform the read or write operation. The module controller further outputs a set of module control signals in response to the input address and

control signals. The memory module further comprises a plurality of byte-wise buffers controlled by the set of module control signals to actively drive respective byte-wise sections of each data signal associated with the read or write operation between the memory controller and the selected rank." *Id.*, Abstract.

26. Figure 3A illustrates an example of a memory subsystem consistent with embodiments disclosed in the '339 patent.

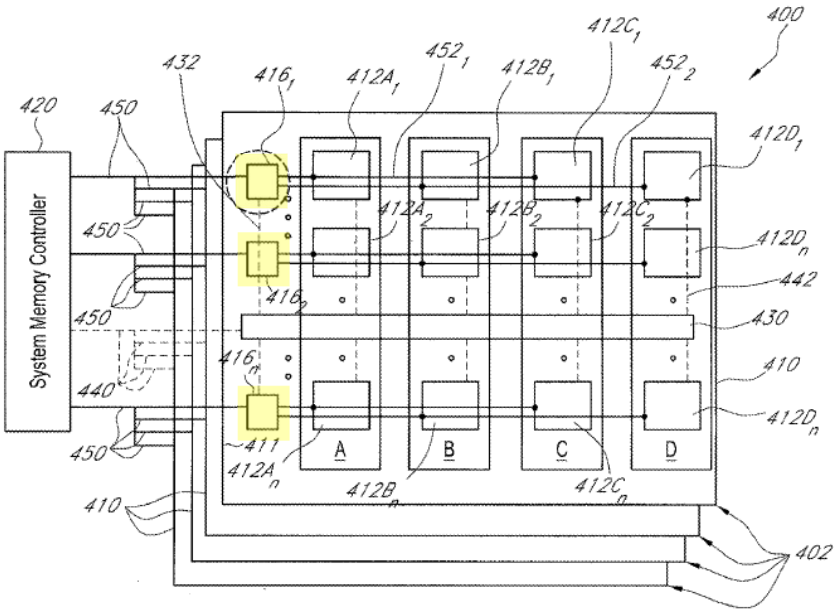


**FIG. 3A**

'339 Patent, Figure 3A. As shown above, Figure 3A depicts a memory subsystem 400 including memory modules 402 comprising memory devices 412, data transmission circuits 416 (highlighted above), and module control circuits 430. The data transmission circuits 416 operate to reduce the load experienced by the memory controller 420 to improve performance of a read or write operation. *Id.* at 17:14-44 ("Referring again to FIG. 3A, when the memory controller 420 executes read or write operations, each specific operation is targeted to a specific one of the ranks A, B, C, and D of a specific memory module 402. The data transmission circuit 416 on the specifically

targeted one of the memory modules 402 functions as a bidirectional repeater/multiplexor, such that it drives the data signal when connecting from the system memory controller 420 to the memory devices 412. The other data transmission circuits 416 on the remaining memory modules 402 are disabled for the specific operation. . . . Thus, the memory controller 420, when there are four four-rank memory modules, sees four load-reducing switching circuit loads, instead of sixteen memory device loads. The reduced load on the memory controller 420 enhances the performance and reduces the power requirements of the memory system . . . .”). In certain embodiments, “the data transmission circuit 416 comprises or functions as a byte-wise buffer. In certain such embodiments, each of the one or more data transmission circuits 416 has the same bit width as does the associated memory devices 412 per rank to which the data transmission circuit 416 is operatively coupled.” *Id.* at 13:31-36.

**<u>The ’918 Patent</u>**

27. The ’918 Patent is entitled “Flash-DRAM Hybrid Memory Module.” Netlist owns the ’918 Patent by assignment from the listed inventors Chi-She Chen, Jeffrey C. Solomon , Scott H. Milton, and Jayesh Bhakta. The ’918 Patent was filed as Application No. 17/138,766 on December 30, 2020, issued as a patent on May 25, 2021, and claims priority to, among others, U.S. Application No. 13,559,476 filed on July 26, 2012, U.S. Application No. 12/240,916 filed on September 29, 2008, and U.S. Application No. 12/131,873 filed on June 2, 2008 as well as to two provisional applications, filed on June 1, 2007 (No. 60/941,586) and July 28, 2011 (No. 61/512,871).

28. Samsung had knowledge of the ’918 Patent no later than August 2, 2021 via its access to Netlist’s patent portfolio docket via notice of U.S. Patent Application No. 12/240,916 and U.S. Patent Application No. 12/131,873 on August 2, 2021.

29. As summarized in the Abstract, the '918 Patent discloses a memory module that includes a printed circuit board with an interface that couples it to a host system for provision of power, data, address and control signals, and additionally features "[f]irst, second, and third buck converters [that] receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage." Ex. 3, Abstract.

30. The '918 Patent discloses, *inter alia*, a power module that provides power to various components of the memory system as depicted in Figure 16, shown below.

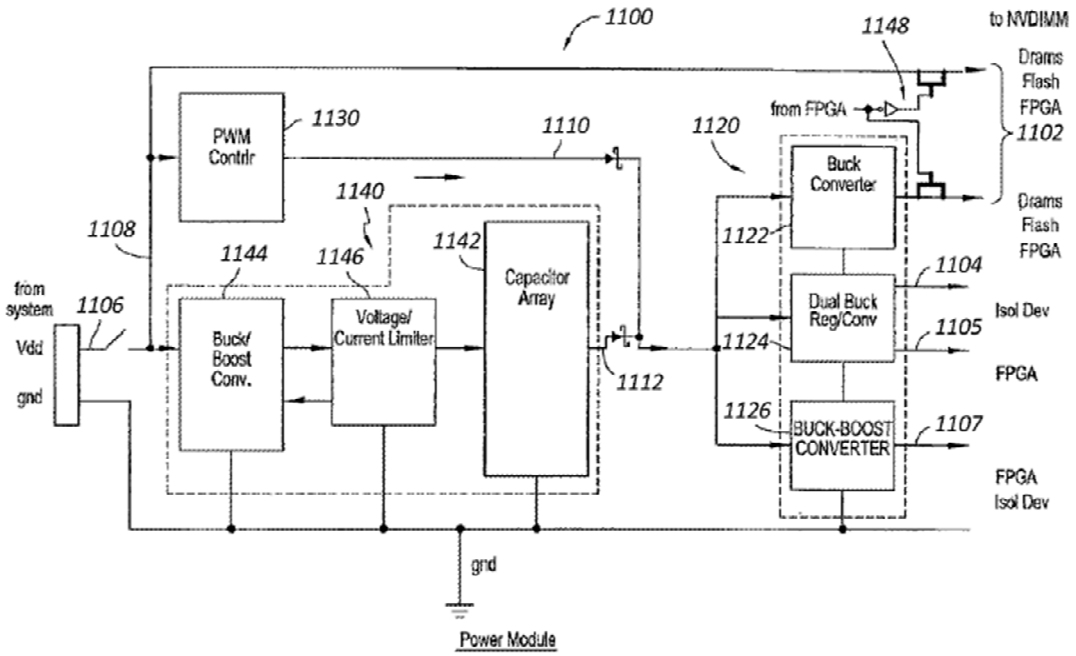


*FIG. 16*

31. The '918 Patent explains that "[t]he power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems

1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller." *Id.* at 28:3-15. "The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters." *Id.* at 29:18-19.

32. Relatedly, on December 10, 2021, the United States Patent and Trademark Office issued a Notice of Allowance for the pending claims of Application No. 17/138,019, a continuation of the '918 Patent. *See* Ex. 4 (allowed claims of App. No. 17/138,019). Netlist intends to assert the allowed claims of App. No. 17/138,019 upon issuance against Samsung.

33. The inventions of the '918 Patent and App. No. 17/138,019 provide for the effective operation of DDR5 memory modules, by enabling, among other benefits, greater power efficiency than previous generations of DDR technology. The DDR5 standard is characterized by the use of an on-module power management system. Samsung itself notes "[t]he on-DIMM PMIC further boosts power management efficiency and power supply stability." Ex. 12 at 5.

**Samsung's Infringing Activities**

34. Samsung is a global technology company that manufactures semiconductor memory products such as DRAM, NAND Flash and MCP (Multi-Chip Package). Samsung develops, manufactures, sells and imports into the United States memory components and memory modules designed for, among other things, use in servers such as those supporting cloud-based computing and other data-intensive applications.


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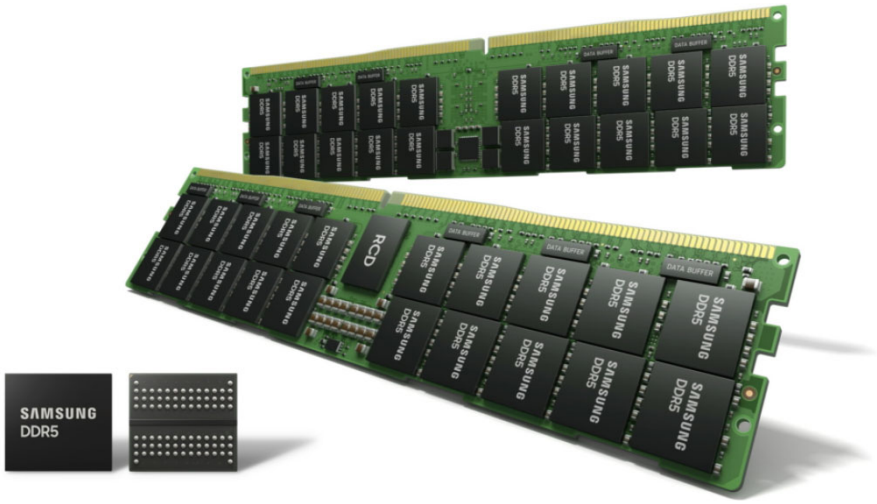
35. Samsung was a licensee of Netlist until July 15, 2020. *See Netlist Inc. v. Samsung Elecs. Co., Ltd.*, No. 20-cv-993, Dkt. 186 at 20-21 (C.D. Cal. Oct. 14, 2021). Immediately after Samsung's license was deemed terminated, Samsung filed an improper declaratory judgment action in the District of Delaware concerning unrelated patents directed at different aspects of memory module technology than the patents in the present suit. *See Samsung Elecs. Co., Ltd. et al v. Netlist, Inc.*, No. 21-cv-1453, Dkt. 1 (D. Del. Oct. 15, 2021). Netlist has moved to dismiss each count of Samsung's declaratory judgment complaint in Delaware.

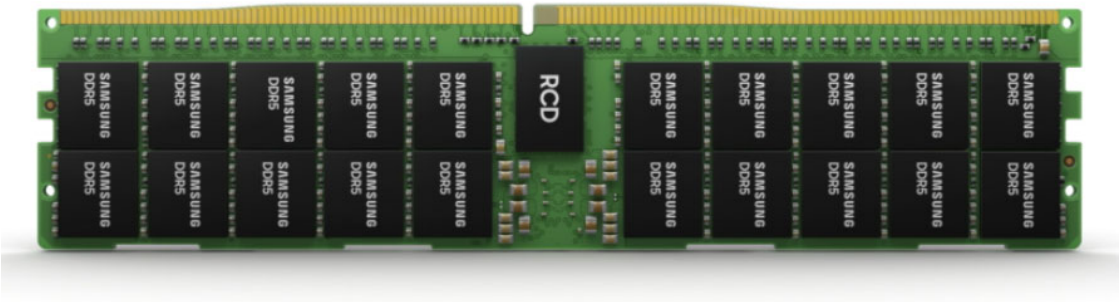
36. On information and belief, Samsung makes, uses, sells, offers to sell, and/or imports within this District and elsewhere in the United States, without authority, infringing DDR4 LRDIMMs, DDR5 LRDIMMs, DDR5 RDIMMs, DDR5 SODIMMs, DDR5 UDIMMs, and other products that have materially the same structures and designs in relevant parts (the "Accused Instrumentalities").

37. The accused DDR4 LRDIMMs include, without limitation, any Samsung DDR4 LRDIMM products made, sold, used and/or imported into the United States by Samsung. By way of non-limiting example, the accused DDR4 LRDIMMs products include, Samsung products having the following part numbers: M386A4K40BB0-CRC, M386A8K40BM1-CRC, M386A8K40BM2-CTD, M386A8K40BMB-CRC, M386A8K40CM2-CRC, M386A8K40CM2-CTD, M386A8K40CM2-CVF, M386A8K40DM2-CTD, M386A8K40DM2-CVF, M386A8K40DM2-CWE, M386AAG40AM3-CWE, M386AAG40MM2-CVF, M386AAG40MMB-CVF, M386AAK40B40-CUC, M386AAK40B40-CWD, M386ABG40M50-CYF, M386ABG40M51-CAE, M386ABG40M5B-CYF. Further examples of Samsung's DDR4 LRDIMM products can be found via Samsung's module-selector web page. *See Module: Memory Modules For Extensive Use*, Samsung, *available at* https://www.samsung.com/semiconductor/dram/module.

38. As further example, the Accused Instrumentalities include, without limitation, any Samsung DDR5 LRDIMM and DDR5 RDIMM products made, sold, used and/or imported into the United States by Samsung that are JEDEC-standard compliant memory modules. By way of non-limiting example, the accused DDR5 LRDIMM and DDR5 RDIMM products include products marketed and publicized in an October 12, 2021 Samsung Press release, as shown below.




Ex. 5 at 1 (depiction of a Samsung DDR5 LRDIMM).




*Id.* at 3 (depiction of a Samsung DDR5 RDIMM).

## IV. FIRST CLAIM FOR RELIEF – '506 PATENT

39. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

40. On information and belief, Samsung directly infringed and is currently infringing at least one claim of the '506 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example, and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '506 Patent.[1]

41. For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus. As an example, Samsung's website markets and contains datasheets for the accused DDR4 LRDIMMs.

**LRDIMM**

**Load Reduced DIMM**

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

42. Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM). Each LRDIMM includes "a register for enhancing clock, command and control signals" as well as data buffers for "[e]nhanced

[1] The theories set forth herein are based on Netlist's present understanding of the Samsung Accused Instrumentalities. Netlist reserves the right to supplement or amend these contentions as permitted by the Local Rules and any Orders of the Court as discovery progresses. Further, Netlist's contentions contain images and examples illustrating Netlist's infringement theories. As such, the images and examples are not intended, and should not be read, as narrowing or limiting the scope of these contentions.

data signal." *Id.* It communicates with a server's memory controller via control and address signal lines in a memory bus as well as a data bus. For example:

Rev. 1.4

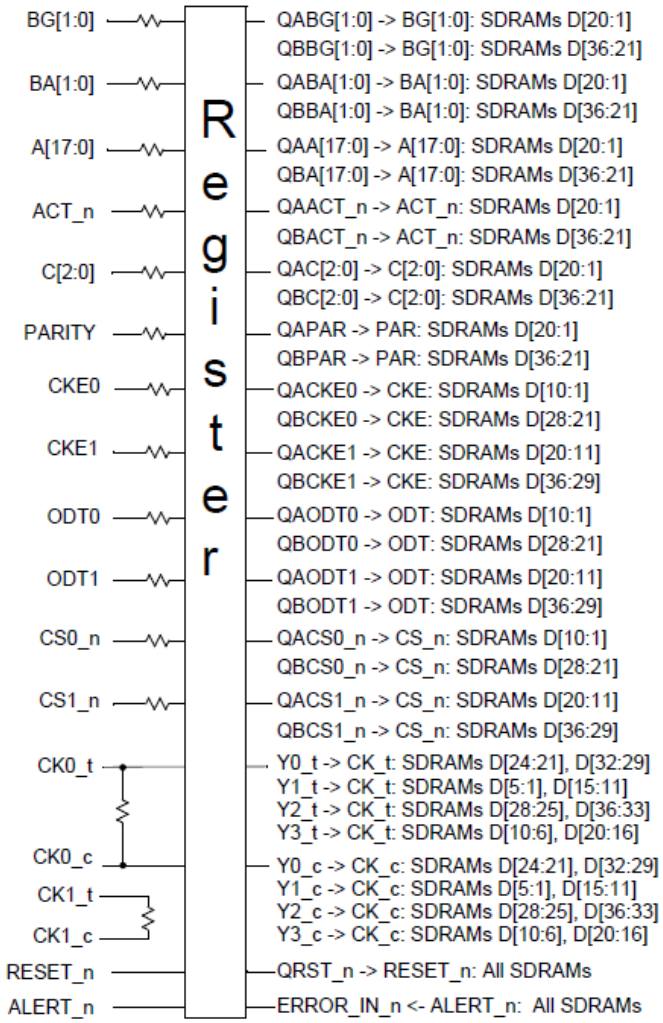
Load Reduced DIMM datasheet DDR4 SDRAM

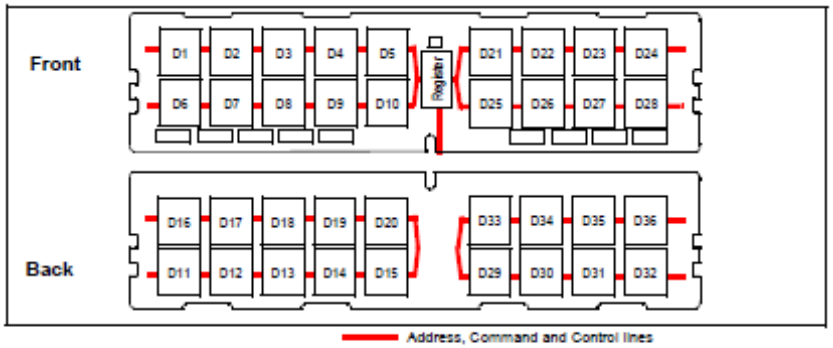
## 5. Pin Description

| Pin Name | Description | Pin Name | Description |
|---|---|---|---|
| A0–A17[1] | Register address input | SCL | I2C serial bus clock for SPD/TS and register |
| BA0, BA1 | Register bank select input | SDA | I2C serial bus data line for SPD/TS and register |
| BG0, BG1 | Register bank group select input | SA0–SA2 | I2C slave address select for SPD/TS and register |
| RAS_n[2] | Register row address strobe input | PAR | Register parity input |
| CAS_n[3] | Register column address strobe input | VDD | SDRAM core power supply |
| WE_n[4] | Register write enable input | VPP | SDRAM activating power supply |
| CS0_n, CS1_n, CS2_n, CS3_n | DIMM Rank Select Lines input | VREFCA | SDRAM command/address reference supply |
| CKE0, CKE1 | Register clock enable lines input | VSS | Power supply return (ground) |
| ODT0, ODT1 | Register on-die termination control lines input | VDDSPD | Serial SPD/TS positive power supply |
| ACT_n | Register input for activate input | ALERT_n | Register ALERT_n output |
| DQ0–DQ63 | DIMM memory data bus | RESET_n | Set Register and SDRAMs to a Known State |
| CB0–CB7 | DIMM ECC check bits | EVENT_n | SPD signals a thermal event has occurred |
| DQS0_t–DQS17_t | Data Buffer data strobes (positive line of differential pair) | VTT | SDRAM I/O termination supply |
| DQS0_c–DQS17_c | Data Buffer data strobes (negative line of differential pair) | RFU | Reserved for future use |
| CK0_t, CK1_t | Register clock input (positive line of differential pair) | | |
| CK0_c, CK1_c | Register clocks input (negative line of differential pair) | | |

NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Ex. 7 (M386AAK40B40 Datasheet) at 6.




NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

- 10 -

SAMSUNG

*Id.* at 10 (red lines in original).

43. The accused DDR4 LRDIMMs further each comprise a module board having edge connections to be coupled to respective signal lines in the memory bus, as illustrated in the examples below.

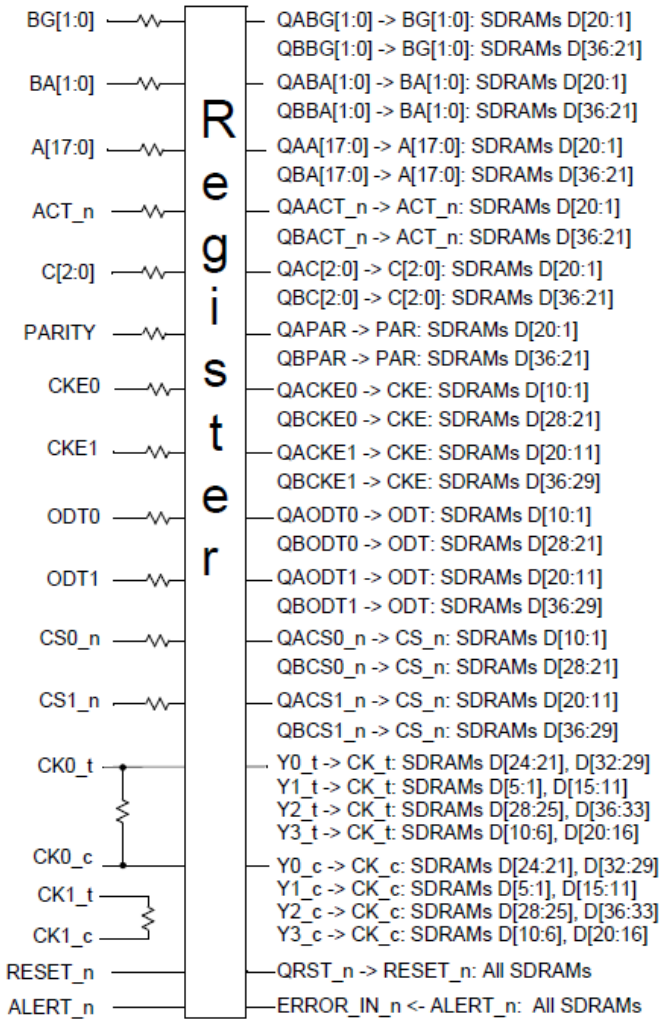
**LRDIMM**

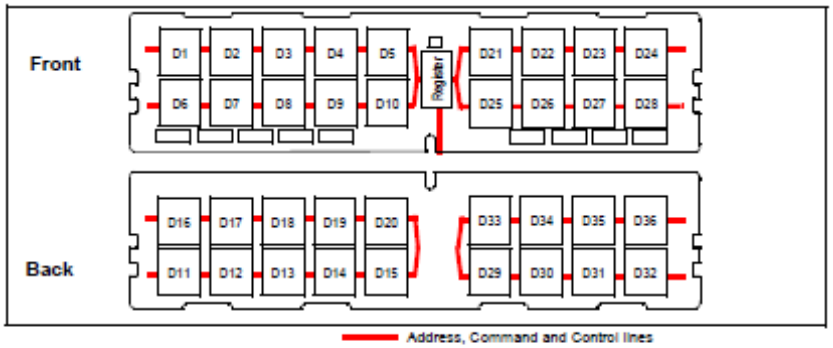
**Load Reduced DIMM**

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM); *see also* Ex. 7 (M386AAK40B40 Datasheet) at 42.

44. The accused DDR4 LRDIMMs further each comprise a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals, as illustrated in the example below.



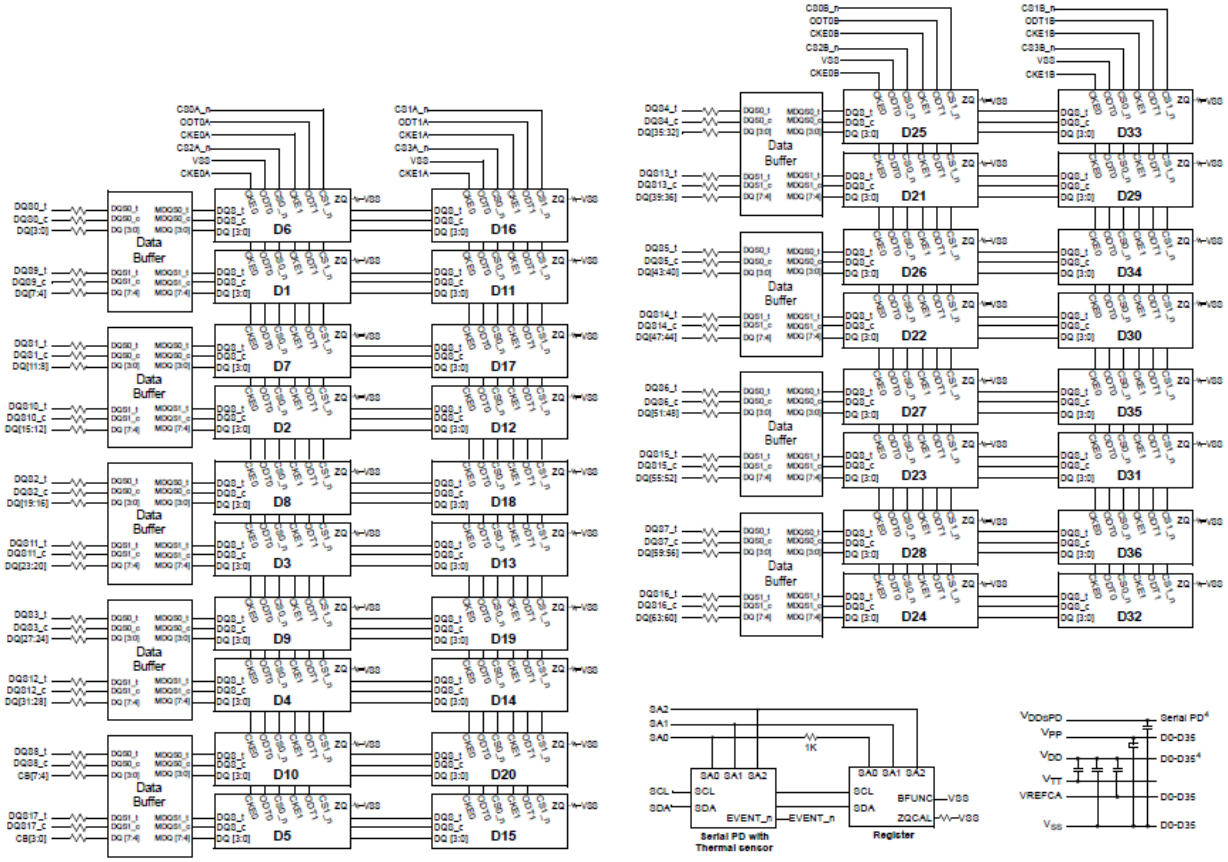




NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

- 10 -

SAMSUNG

Ex. 7 (M386AAK40B40 Datasheet) at 10; *see also id.* at 42.

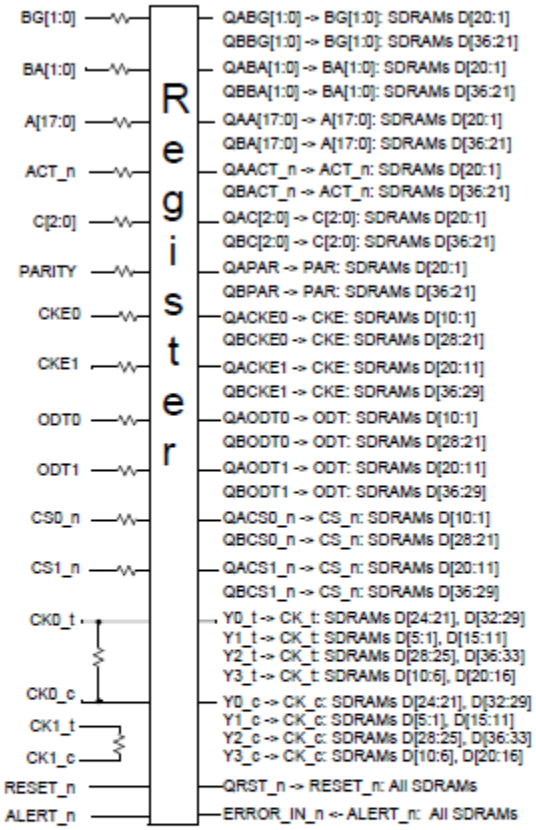


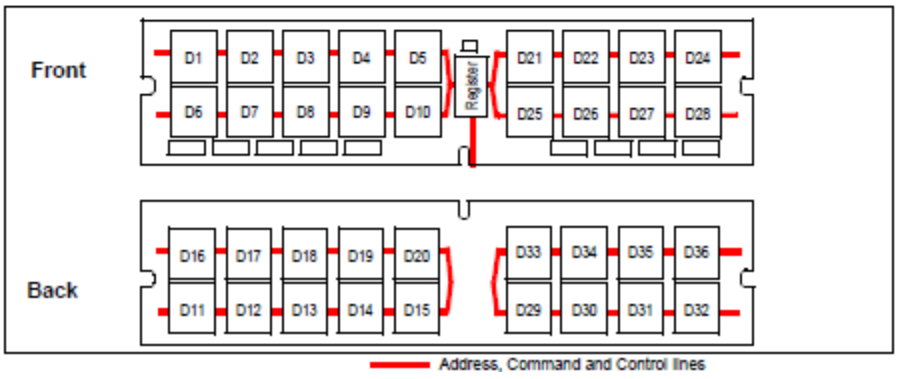

*Id.* at 11-12.

45. The accused DDR4 LRDIMMs also each include memory devices arranged in multiple ranks on the module board and coupled to the module control device (*e.g.*, RCD) via module C/A signal lines that conduct the registered C/A signals, as illustrated in the examples below.

**9.1 128GB, 16Gx72 Module**

**(Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAM**

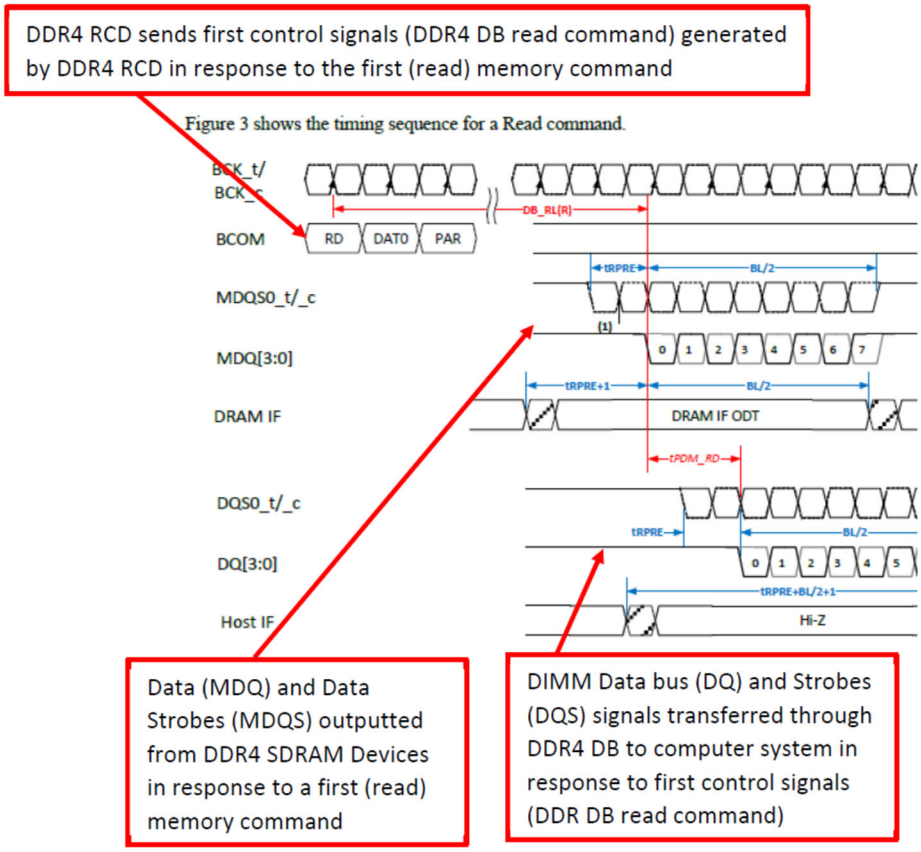


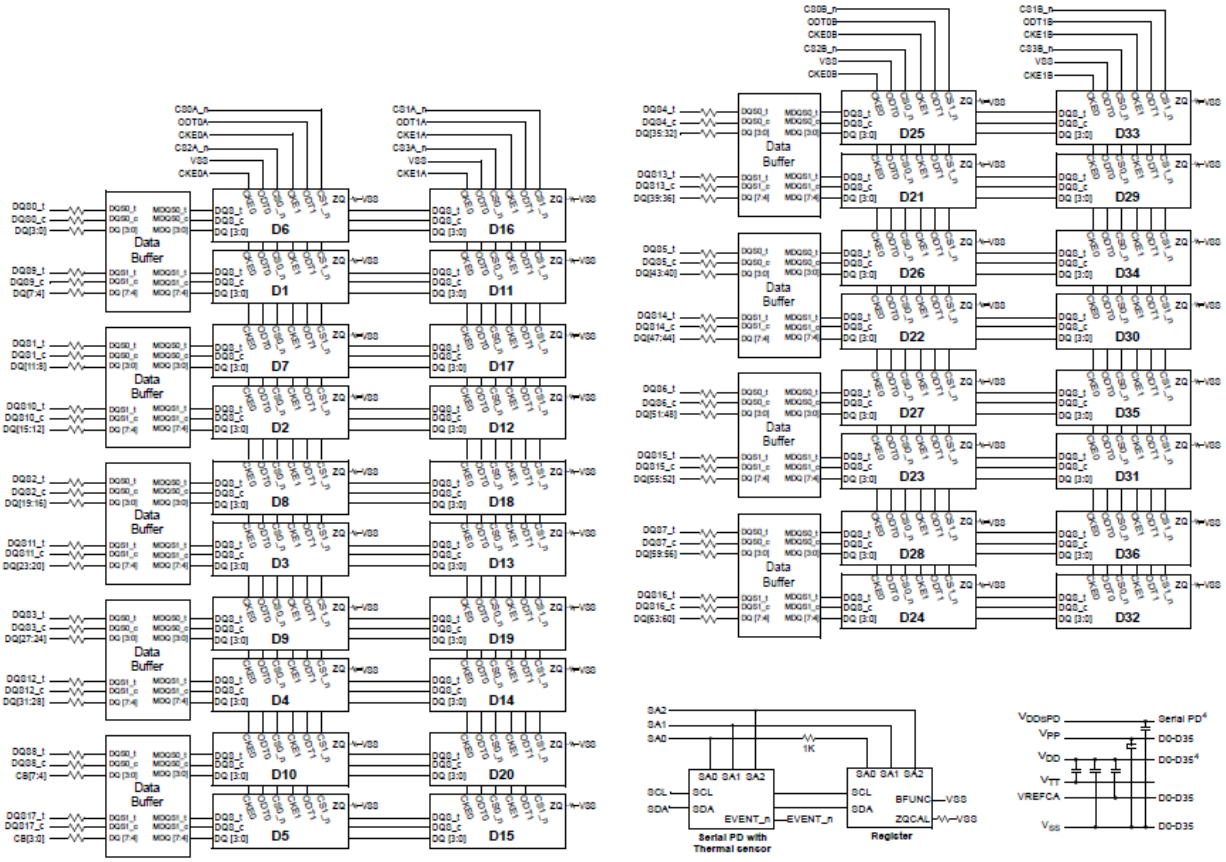

*Id.* at 10; *see also id.* at 42.

46. In each accused DDR4 LRDIMM's memory devices, the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a

first read strobe. For example, each accused DDR4 LRDIMM follows the timing sequence for a READ command shown below.



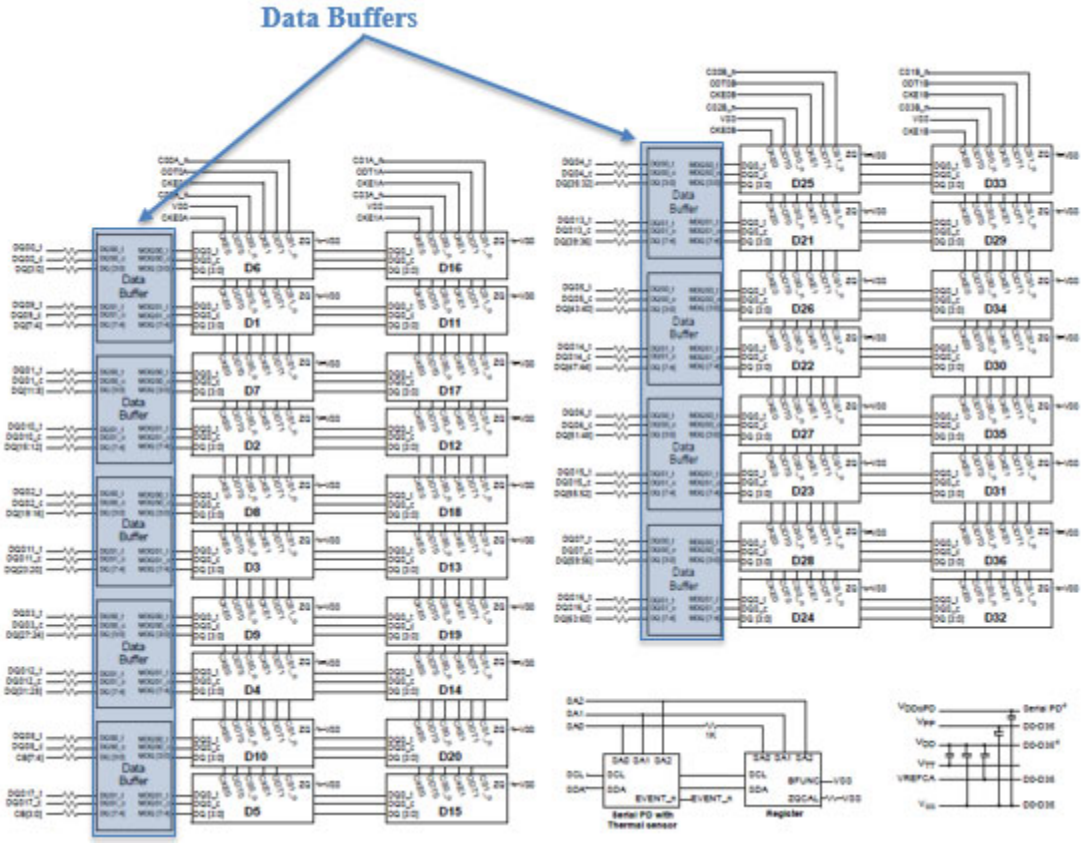

Ex. 9 (JEDEC JESD82-32A Standard), at 14 (annotated); *see also*, *e.g.*, Ex. 8 (M386A8K40BM1 Datasheet) at 11-12 (functional block for a representative product).




Ex. 8 (M386A8K40BM1 Datasheet) at 11-12.

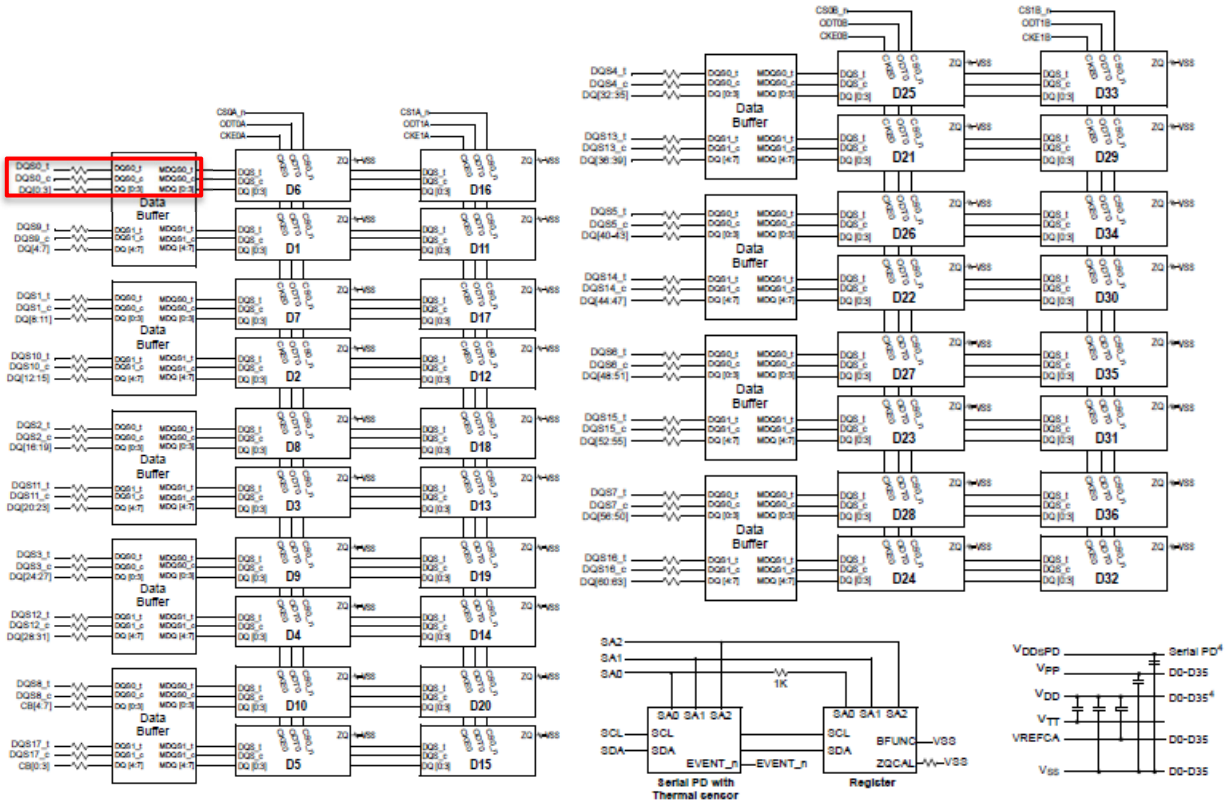
47. The accused DDR4 LRDIMMs further each include data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, as illustrated below.

Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM).




Ex. 8 (M386A8K40BM1 Datasheet) at 11-12 (annotated to illustrate data buffers coupled between the plurality of 72-bit wide ranks and the 72-bit wide data bus).

48. In each accused DDR4 LRDIMM, a first data buffer on the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals: delay the first read strobe by a first predetermined amount to generate a first delayed read strobe; sample the first section of the read data using the first delayed read strobe; and transmit the first section of the read data to a first section of the data bus; wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations. For example, the strobes MDQSO_t and MDQSO_c are delayed by a variable delay circuitry and produce DQS0_t, DQS1_t and DQS0_c, DQS1_c. The predetermined amount of delay is determined based on training.




Ex. 7 (M386AAK40B40 Datasheet) at 11-12.

49. On information and belief, Samsung also indirectly infringes the '506 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information

and belief, Samsung has induced, and currently induces, the infringement of the ’506 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM and other materially similar products that infringe the ’506 Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

50. On information and belief, Samsung also indirectly infringes the ’506 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung’s customers and end-users infringement of the ’506 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM and other materially similar products that infringe the ’506 Patent. On information and belief, the accused DDR4 LRDIMM products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM and other materially similar products would be covered by one or more claims of the ’506 Patents. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM and other materially similar products infringes at least one claim of the ’506 Patent.

51. Samsung’s infringement of the ’506 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the ’506 Patent since at least August 2, 2021. Samsung’s infringement of the ‘506 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement,


Samsung Ex. 1127, p. 26
Samsung Electronics Co., Ltd. v. Netlist, Inc., PGR2026-00001

and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

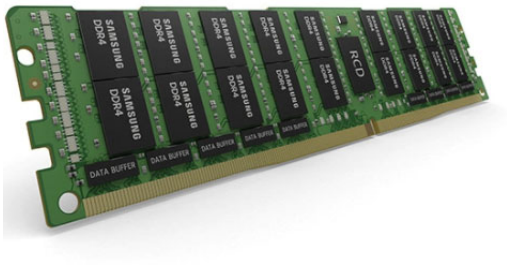
## V. SECOND CLAIM FOR RELIEF – '339 PATENT

52. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

53. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '339 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '339 Patent.

54. For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a N-bit-wide memory module (*e.g.*, 72-bit-wide) mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide. For instance, each LRDIMM includes "a register for enhancing clock, command and control signals" as well as data buffers for "[e]nhanced data signal." Ex. 6 at 2. It communicates with a server's memory controller via control and address signal lines in a memory bus as well as a data bus.


Samsung Ex. 1127, p. 27
Samsung Electronics Co., Ltd. v. Netlist, Inc., PGR2026-00001



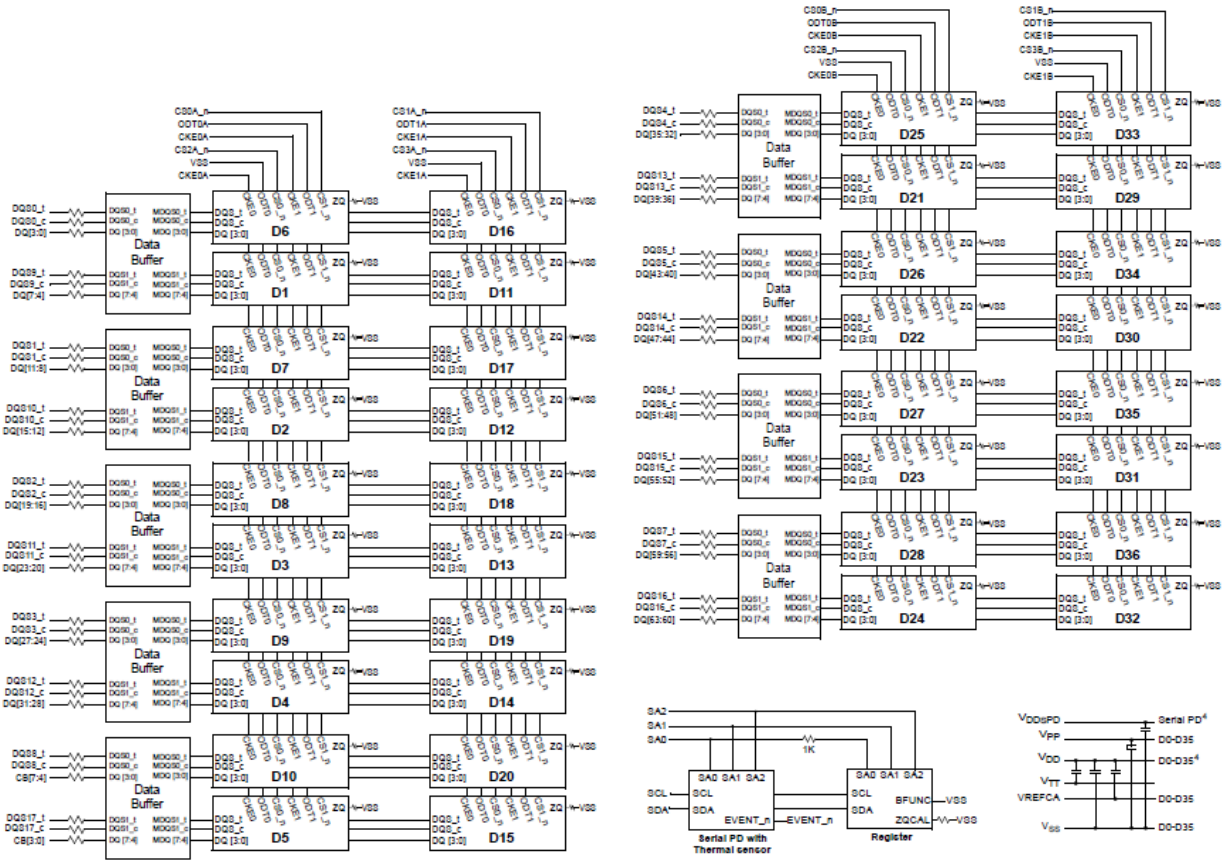
# LRDIMM

## Load Reduced DIMM

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

*Id.* at 2 (depiction of a Samsung DDR4 LRDIMM).

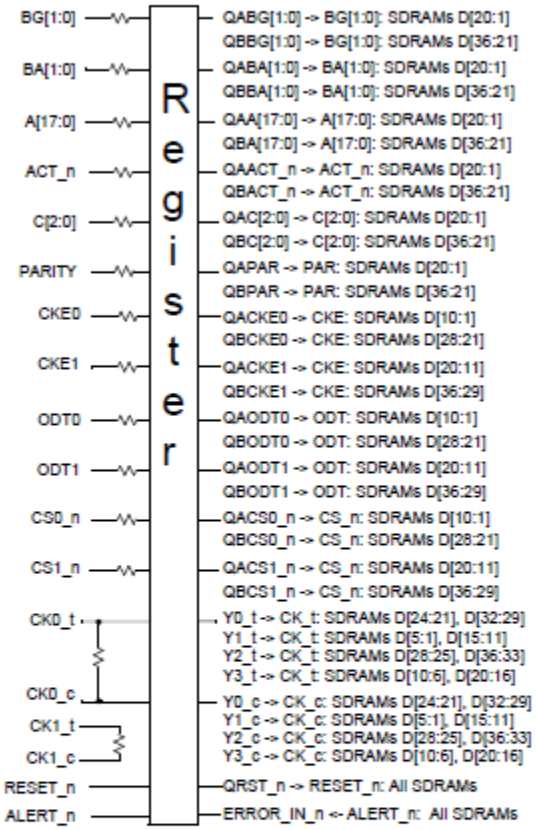
55. In the configuration above, there are 9 sets of byte-wide data signal lines for a 72-bit wide data signal lines. For example:

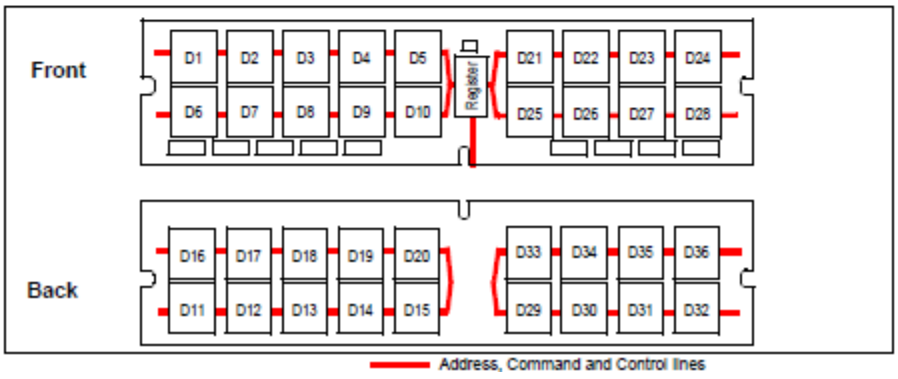


Ex. 8 (M386A8K40BM1 Datasheet) at 11-12.

**9.1 128GB, 16Gx72 Module**

**(Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAM**

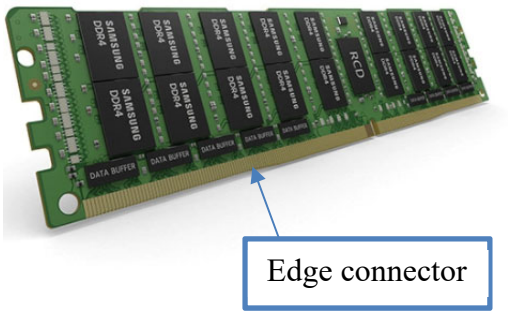



Ex. 7 (M386AAK40B40 Datasheet) at 10; *see also id.* at 42.

56. The accused DDR4 LRDIMMs each comprise a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of

the PCB and configured to be releasably coupled to corresponding contacts of the memory socket. For example:




**LRDIMM**

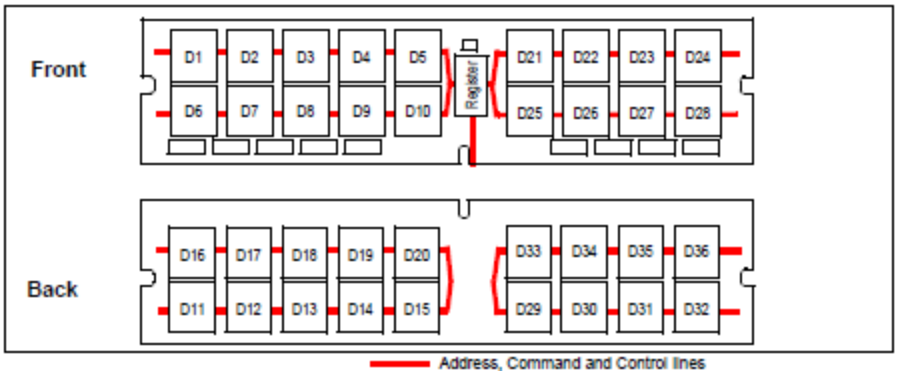
**Load Reduced DIMM**

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

Ex. 6 at 2 (depiction of a Samsung DDR4 LRDIMM).

57. The accused DDR4 LRDIMMs each include double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks. As shown above, each DDR4 LRDIMM module includes 9 ranks of memory devices.

58. The accused DDR4 LRDIMMs further comprise a module controller (such as a register clock driver, RCD) coupled to the PCB and operatively coupled to the DDR DRAM devices. For example:



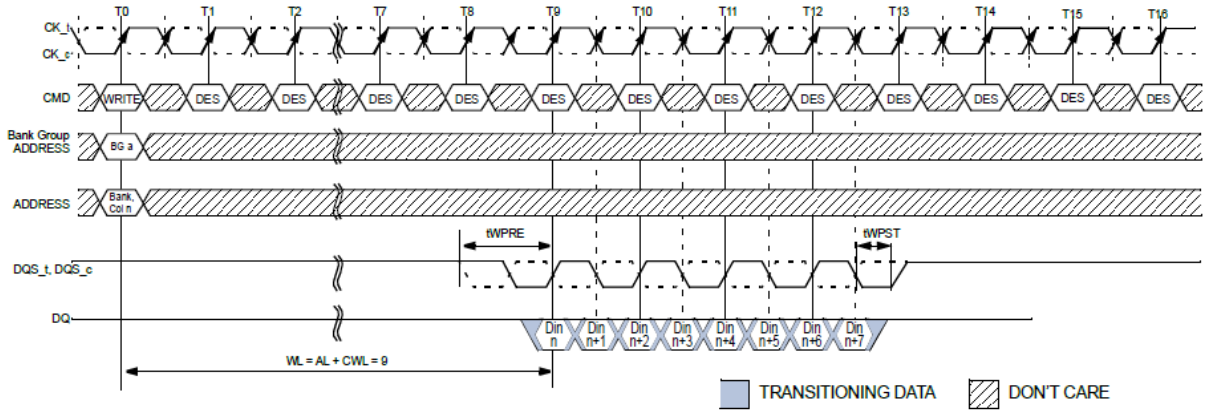

Ex. 7 (M386AAK40B40 Datasheet) at 10; *see also id.* at 42.

59. The module controller is configurable to receive from the memory controller via the address and control signal lines (e.g., red lines above) input address and control signals for a

memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation (when BCOM [3:0] is 1000) by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals. For example, a Write burst operation results in a burst of data and data strobes received by the DDR4 LRDIMM via the DQS/DQ pins of the memory bus, and to write the data via data buffers into a memory device as determined by input address and control signal (e.g., CS signal).

### 4.25.5 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.

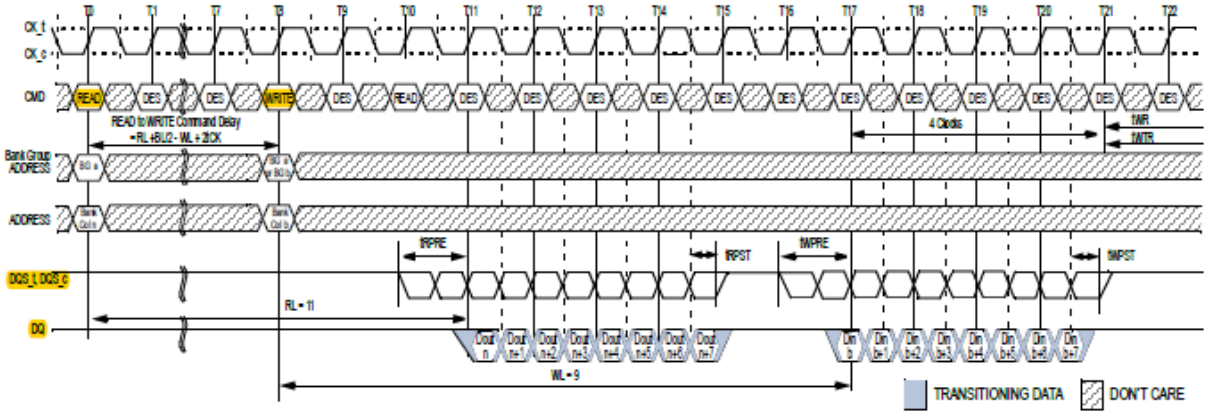



NOTE 1 BL = 8, WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
NOTE 2 DIN n = data-in to column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

**Figure 128 — WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)**

*See, e.g.*, Ex. 10 (JESD79-4C DDR4 SDRAM Standard), at 122.

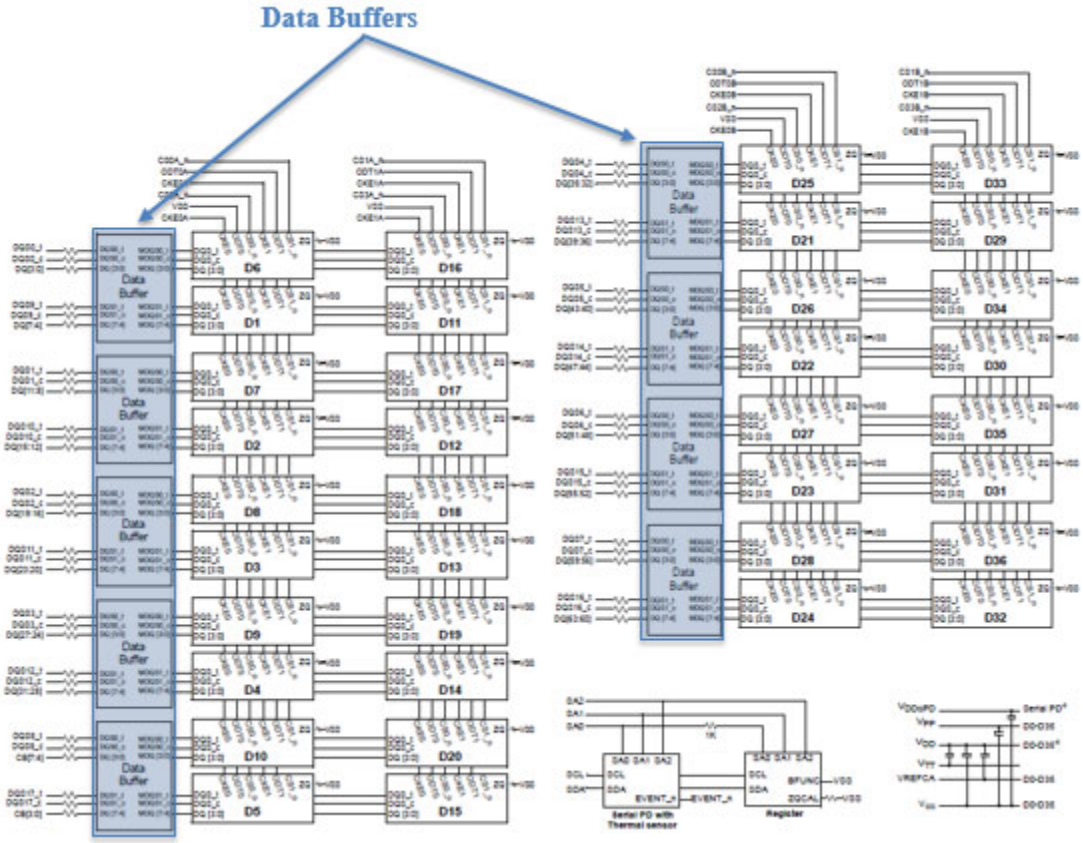
4.24.2 READ Burst Operation (cont'd)




NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

**Figure 98 — READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group**

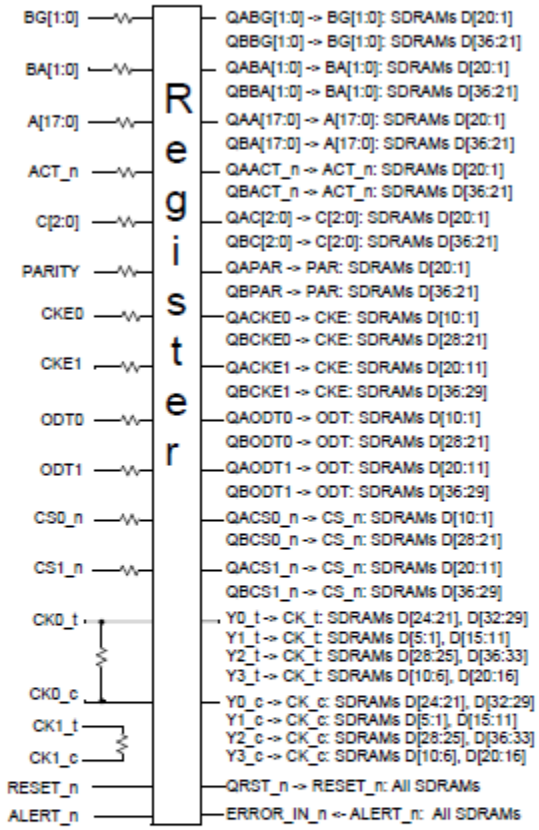
*See, e.g.*, *id.* at 105 (annotated) (showing burst operations used by various ranks in the Accused Instrumentality).

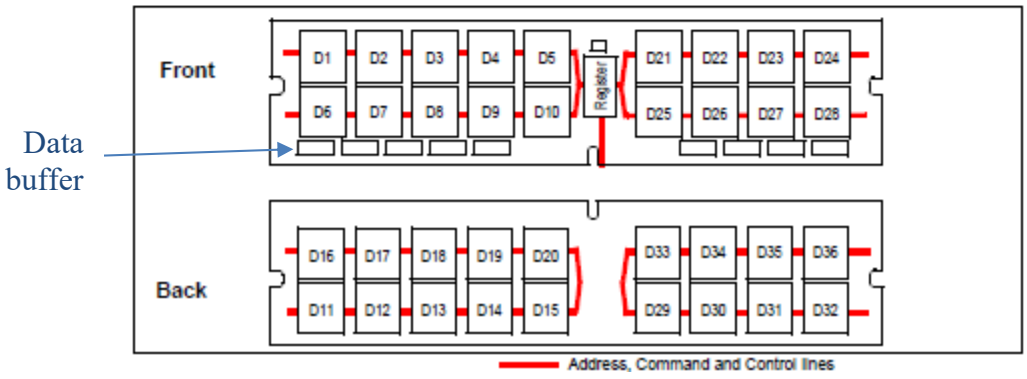



Ex. 8 (M386A8K40BM1 Datasheet) at 11-12.

**9.1 128GB, 16Gx72 Module**

**(Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAM**




Ex. 7 (M386AAK40B40 Datasheet) at 10; *see also id.* at 42.

60. Further, as illustrated above and below, the accused DDR4 LRDIMMs also each comprise a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals, wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second

side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side, wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines.

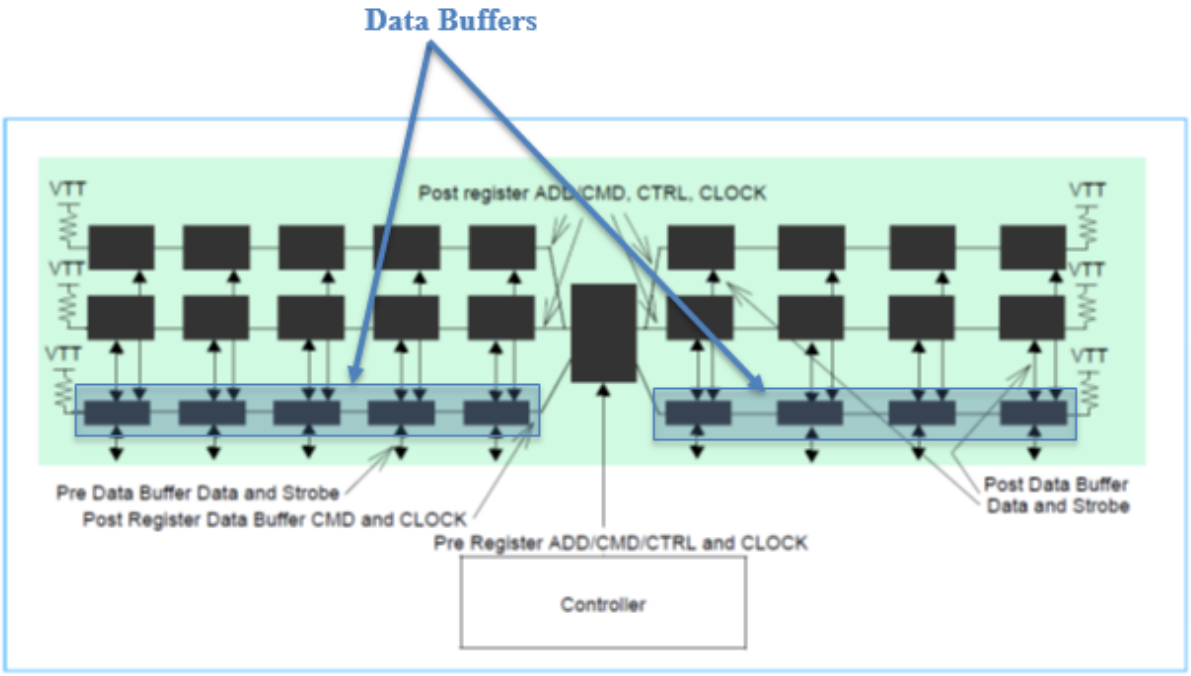



**Figure 3 — LRDIMM Topologies**

Ex. 11 (JEDEC 21C Standard), at 4.20.27-17.

61. In each of the accused DDR4 LRDIMMs, the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals and the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period. For example:

**4.61 Logic Diagram**

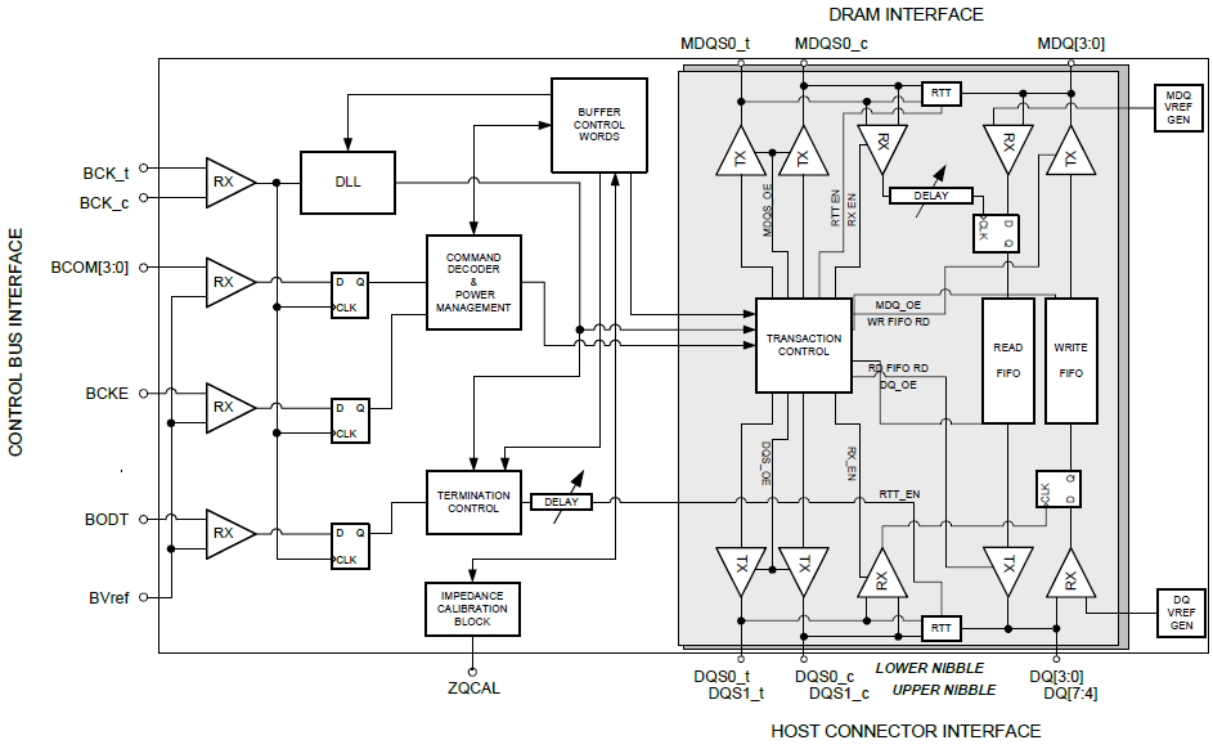
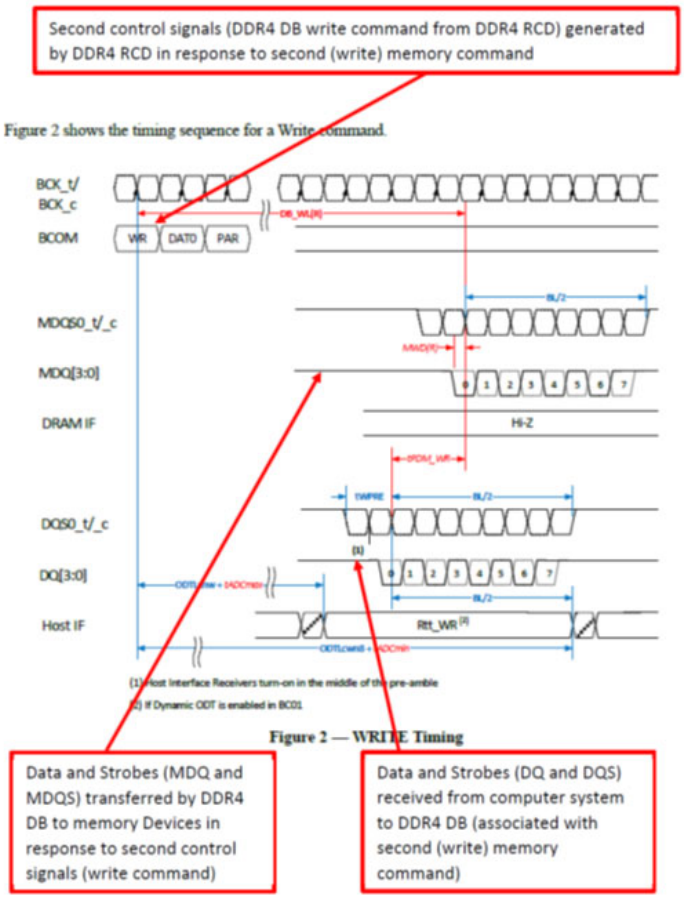



**Figure 15 — Logic Diagram**

Ex. 9 (JESD82-32A Standard), at 95.

62. The MDQ/MDQS driver can be disabled or enabled based on DRAM Interface MDQ Driver control word, such as DA[3:0] = 0xxx (enabled) and 1xxx (disabled).

63. In each of the accused DDR4 LRDIMMs, the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period. For example:




*Id.* at 13.

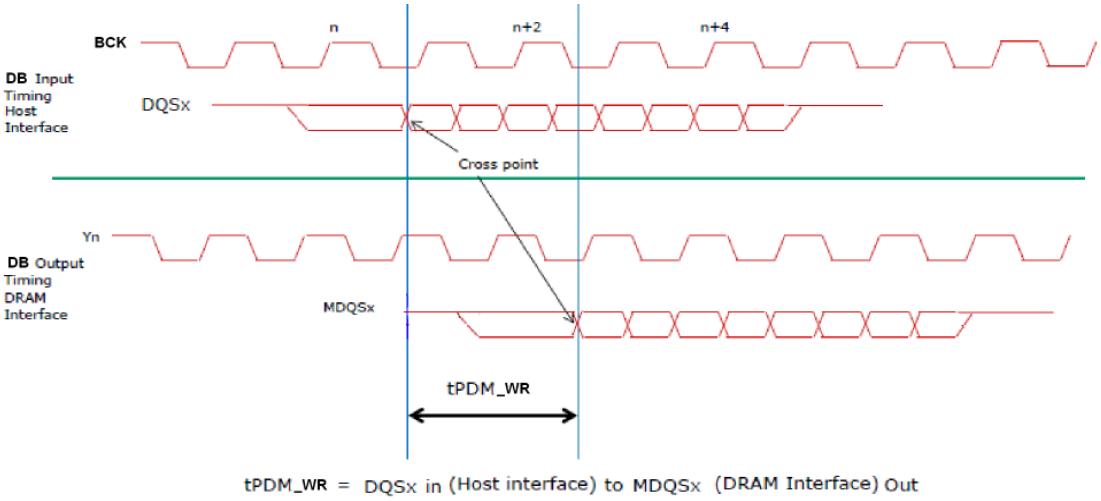



**Figure 56 — tPDM_WR Latency Measurement**

*Id.* at 165.

**Table 146 — WRITE Output Timings**

| | | DDR4-1600/ 1866/2133 | | DDR4-2400/ 2666 | | DDR4- 2933 | | DDR4-3200 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Min | Max | | |
| **Data Timing** | | | | | | | | | | | |
| tDVB | Data valid before MDQS | 0.38 | - | 0.36 | - | 0.36 | - | 0.36 | - | UI | |
| tDVA | Data valid after MDQS | 0.38 | - | 0.36 | - | 0.36 | - | 0.36 | - | UI | |
| **Data Strobe Timing** | | | | | | | | | | | |
| MDQS_t - MDQS_c differential output low time | tMQSL | 0.46 | - | 0.46 | - | 0.46 | - | 0.46 | - | tCK | 1, 3 |
| MDQS_t - MDQS_c differential output high time | tMQSH | 0.46 | - | 0.46 | - | 0.46 | - | 0.46 | - | tCK | 2, 3 |

Unit UI = tCK(avg).min/2

NOTE 1: tMQSL describes the instantaneous differential output low pulse width on MDQS_t - MDQS_c, as measured from on falling edge to the next consecutive rising edge

NOTE 2: tMQSH describes the instantaneous differential output high pulse width on MDQS_t - MDQS_c, as measured from on rising edge to the next consecutive falling edge

NOTE 3: The specification values are affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.). However, these parameters should be met whether clock jitter is present or not.

*Id.* at 169.

64. On information and belief, Samsung also indirectly infringes the ’339 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung’s customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the ’339 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM products and other materially similar products that infringe the ’339 Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

65. On information and belief, Samsung also indirectly infringes the ’339 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on

information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers and end-users infringement of the '339 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the '339 Patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM products and other materially similar products would be covered by one or more claims of the '339 Patent. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the '339 Patent.

66. Samsung's infringement of the '339 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the '339 Patent since at least August 2, 2021. Samsung's infringement of the '339 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

## VI. THIRD CLAIM FOR RELIEF – '918 PATENT

67. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

68. On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '918 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR5 LRDIMMs, DDR5 RDIMMs, DDR5 SODIMMs, DDR5 UDIMMs, and other products with materially the same structures in relevant parts. For example, and as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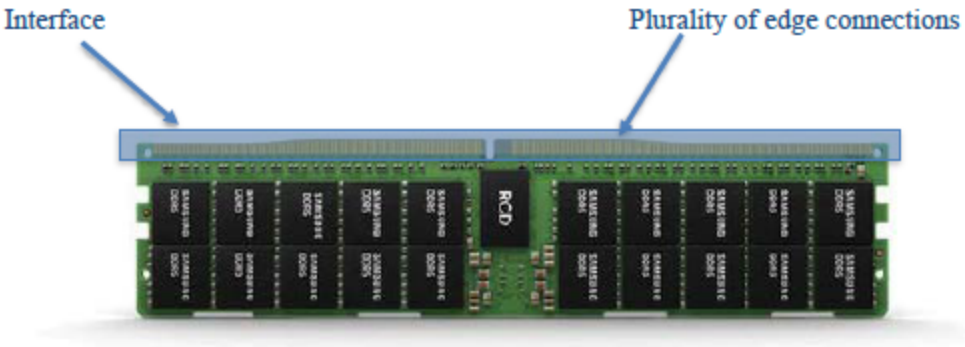
shown below, the accused DDR5 memory modules and other products with materially the same structures in relevant parts infringe at least one claim of the '918 patent.

69. For example, the accused DDR5 products comprise a memory module comprising: a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system, as illustrated below.

Ex. 5 at 1 (depiction of a Samsung DDR5 LRDIMM).



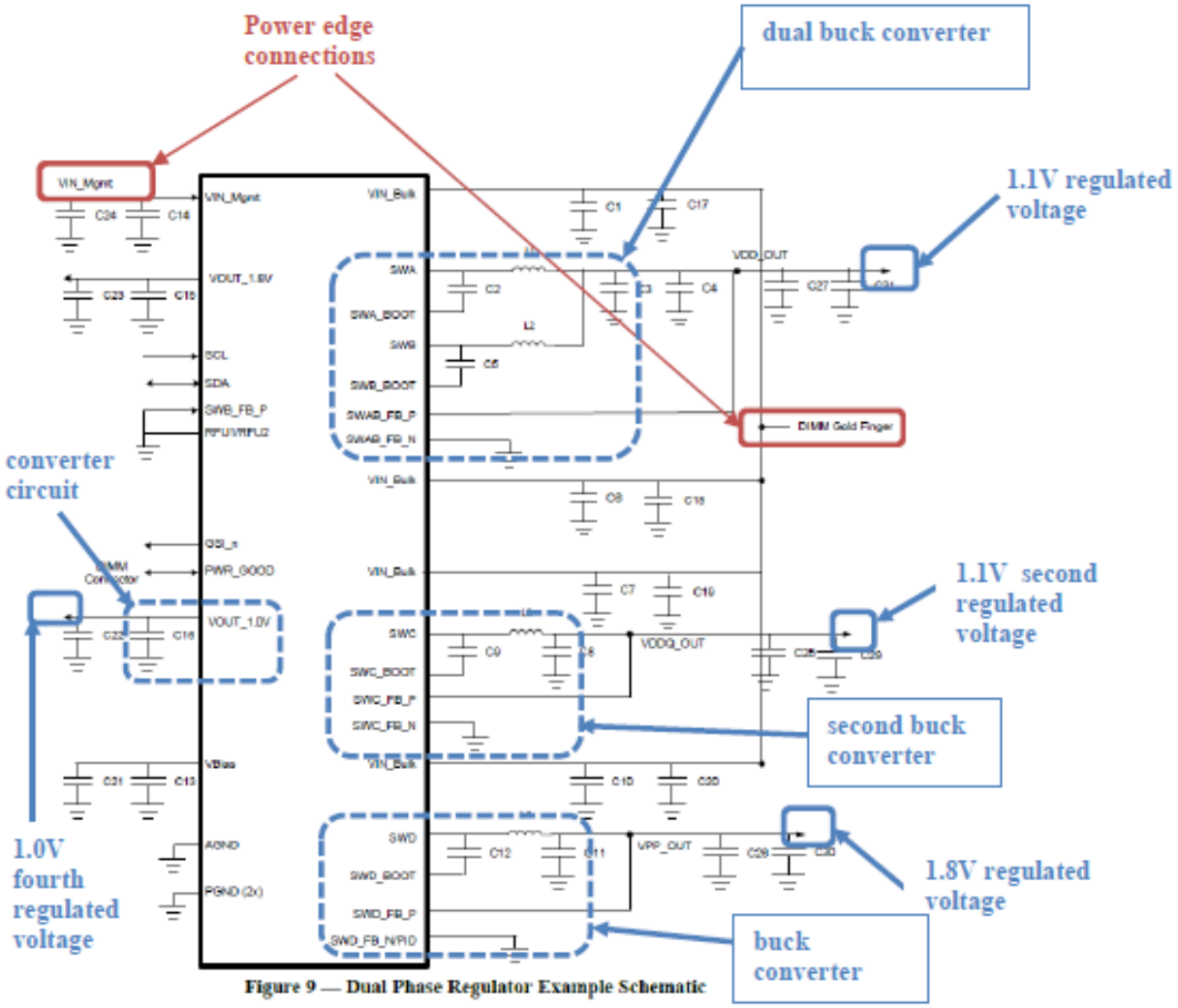

*Id.* at 3 (depiction of a Samsung DDR5 RDIMM).

70. The accused DDR5 products further comprise a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; and a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude. For example, Samsung notes on its web site that its DDR5 modules include an "on-DIMM PMIC" that "further boosts power management efficiency and power supply stability." Ex. 12 at 5; *see also* Ex. 13 at 2 ("One major design improvement to the newest generation DRAM solution involves integrating the PMIC into the memory module — previous generations placed the PMIC on the motherboard — offering increased compatibility and signal integrity, and providing a more reliable and sustained performance.").

71. Samsung's PMIC for DDR5 includes a high-efficiency hybrid gate driver and an asynchronous-based dual-phase buck control scheme. *Id.* The dual-phase buck control scheme "allows the DC voltage to step down from high to low with a fast transient response to changes in the output load current and adapts the conversion accordingly to efficiently regulate its output voltage at near-constant levels." *Id*.

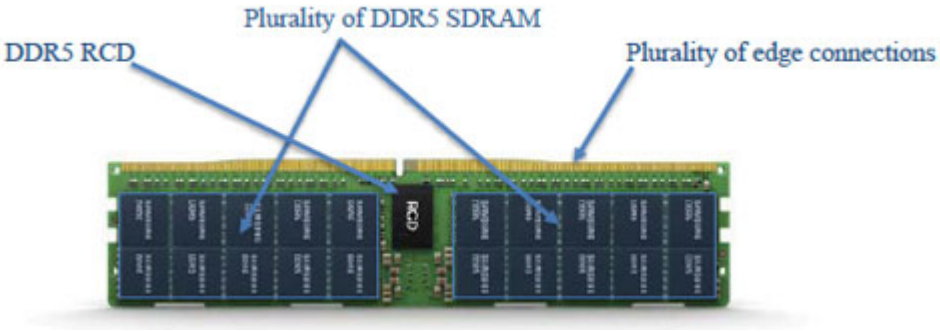
72. The PMIC provides the required regulated voltages, in accordance with the latest DDR5 standards.

Ex. 5 at 1 (depiction of a Samsung DDR5 LRDIMM).

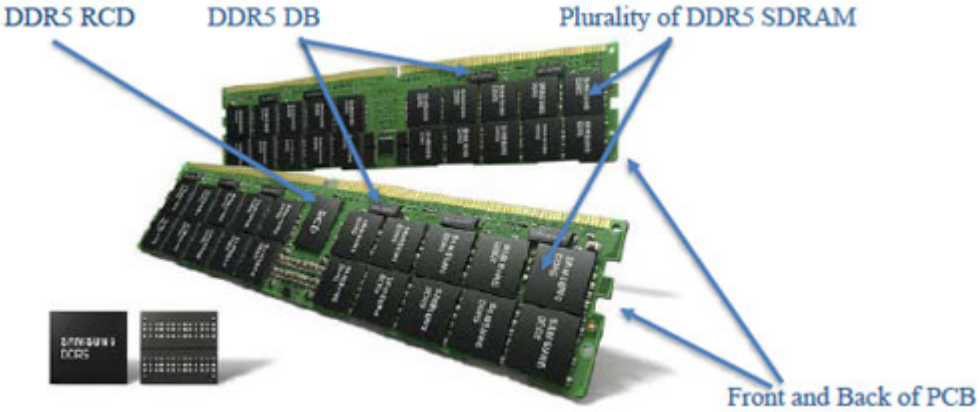



Ex. 14 (JEDEC Power Management Specification for DDR5) (annotated), at 19; *see also id.* at 20.

73. The accused DDR5 products further comprise a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising: a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and at least one circuit (*e.g.*, RCD) coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, as illustrated below.




Ex. 5 at 3 (depiction of a Samsung DDR5 RDIMM).




Ex. 5 at 1 (depiction of a Samsung DDR5 LRDIMM).

2.4 DDR5 SDRAM X4/8 Ballout using MO-210

Table 1 provides the ballout for DDR5 SDRAM X4/8 using MO-210.

**Table 1 — DDR5 SDRAM X4/8 Ballout Using MO-210**

| AN | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AL | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | |
| A | DNU | LBDQ | VSS | VPP | | | | ZQ | VSS | LBDQS | DNU | A |
| B | | VDD | VDDQ | DQ2 | | | | DQ3 | VDDQ | VDD | | B |
| C | | VSS | DQ0 | DQS_t | | | | DM_n, TDQS_t | DQ1 | VSS | | C |
| D | | VDDQ | VSS | DQS_c | | | | TDQS_c | VSS | VDDQ | | D |
| E | | VDD | DQ4 | DQ6 | | | | DQ7 | DQ5 | VDD | | E |
| F | | VSS | VDDQ | VSS | | | | VSS | VDDQ | VSS | | F |
| G | | CA_ODT | MIR | VDD | | | | CK_t | VDDQ | TEN | | G |
| H | | ALERT_n | VSS | CS_n | | | | CK_c | VSS | VDD | | H |
| J | | VDDQ | CA4 | CA0 | | | | CA1 | CA5 | VDDQ | | J |
| K | | VDD | CA6 | CA2 | | | | CA3 | CA7 | VDD | | K |
| L | | VDDQ | VSS | CA8 | | | | CA9 | VSS | VDDQ | | L |
| M | | CAI | CA10 | CA12 | | | | CA13 | CA11 | RESET_n | | M |
| N | DNU | VDD | VSS | VDD | | | | VPP | VSS | VDD | DNU | N |

Ex. 15 (JEDEC 79-5 DDR5 SDRAM Standard), at 3.

**Table 3 — Pinout Description (Continued)**

| Symbol | Type | Function |
|---|---|---|
| LBDQ | Output | Loopback Data Output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0]. |
| LBDQS | Output | Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0]. |
| RFU | Input/Output | Reserved for future use |
| NC | | No Connect: No internal electrical connection is present. |
| VDDQ | Supply | DQ Power Supply: 1.1 V |
| VDD | Supply | Power Supply: 1.1 V |
| VSS | Supply | Ground |
| VPP | Supply | DRAM Activating Power Supply: 1.8V |
| ZQ | Reference | Reference Pin for ZQ calibration. This ball is tied to an external 240 ohm resistor(RZQ), which is tied to $V_{SS}$. |

*Id.* at 5.

**10.1 Operating Electrical Characteristics**

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

**Table 189 — Operating Electrical Characteristics**

| Symbol | Parameter | Condition | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | DC Supply voltage[1] | 1.1 V Operation | 1.067 (-3%) | 1.1 | 1.166 (+6%) | V |
| $V_{DDIO}$ | DDR5RCD01 Sideband Interface I/O Supply Voltage | | 0.95 | 1.0 | 1.05 | V |

Ex. 16 (JEDEC DDR5 RCD Standard, JESD 82-511), at 176.

74. The at least one circuit (e.g., RCD) is operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices. For example:

**3.1 Description**

The DDR5RCD01 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

*Id.* at 5.

75. The at least one circuit is coupled to both the second regulated voltage and the fourth regulated voltage. For example, the RCD receives both 1.0V VDDIO and 1.1V VDD input, with the amplitude of VDDIO being less than the amplitude of VDD.

VDDIO (1.0V)
fourth regulated voltage

VDD (1.1V)
second regulated voltage

**Table 1 — Ball Assignment -240 ball FCBGA, 14 x 19 Grid, TOP VIEW**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NU | QB CA7_A | QB CA5_A | QB CA13_A | QB CA11_A | QB CA12_A | QB CA10_A | QB CA10_B | QB CA12_B | QB CA11_B | QB CA13_B | QB CA5_B | QB CA7_B | NU | A |
| B | QB CA1_A | $V_{SS}$ | QB CA9_A | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{DD}$ | $V_{SS}$ | $V_{SS}$ | $V_{SS}$ | QB CA9_B | $V_{SS}$ | QB CA1_B | B |
| C | QB CA6_A | $V_{SS}$ | QB CA8_A | $V_{DD}$ | ZQ CAL | SCL | DERROR _IN_A_n | DERROR _IN_B_n | SDA | $V_{DDIO}$ | $V_{DD}$ | QB CA8_B | $V_{SS}$ | QB CA6_B | C |
| D | QB CA3_A | $V_{SS}$ | QB CA2_A | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | | | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | QB CA2_B | $V_{SS}$ | QB CA3_B | D |
| E | QB CA0_A | $V_{SS}$ | QB CA4_A | $V_{DD}$ | QBCK _A_c | QBCK _A_t | $V_{SS}$ | $V_{SS}$ | QBCK _B_t | QBCK _B_c | $V_{DD}$ | QB CA4_B | $V_{SS}$ | QB CA0_B | E |

*Id.* at 3.

**10.1 Operating Electrical Characteristics**

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

**Table 189 — Operating Electrical Characteristics**

| Symbol | Parameter | Condition | Min | Nom | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | DC Supply voltage[1] | 1.1 V Operation | 1.067 (-3%) | 1.1 | 1.166 (+6%) | V |
| $V_{DDIO}$ | DDR5RCD01 Sideband Interface I/O Supply Voltage | | 0.95 | 1.0 | 1.05 | V |

*Id.* at 176.

76. On information and belief, Samsung also indirectly infringes the ’918 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung’s customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the ’918 Patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR5 products and other materially similar products that infringe the ’918

Patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR5 memory modules and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

77. On information and belief, Samsung also indirectly infringes the ’918 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung’s customers and end-users infringement of the ’918 Patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR5 memory modules and other materially similar products that infringe the ’918 Patent. On information and belief, the accused DDR5 products and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR5 products and other materially similar products may be covered by one or more claims of the ’918 Patent. On information and belief, the use of the product or process that includes the accused DDR5 products and other materially similar products infringes at least one claim of the ’918 Patent.

78. Samsung’s infringement of the ’918 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the ’918 Patent since at least August 2, 2021. Samsung’s infringement of the ‘506 Patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

## VII. DEMAND FOR JURY TRIAL

79. Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

## VIII. PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Samsung infringes the Patents-in-Suit;

B. all equitable relief the Court deems just and proper as a result of Samsung's infringement;

C. an award of damages resulting from Samsung's acts of infringement in accordance with 35 U.S.C. § 284;

D. that Samsung's infringement of the Patents-in-Suit is willful;

E. enhanced damages pursuant to 35 U.S.C. § 284;

F. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

G. an accounting for acts of infringement and supplemental damages, without limitation, prejudgment and post-judgment interest; and

H. such other equitable relief which may be requested and to which Netlist is entitled.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Dated: December 20, 2021

Respectfully submitted,

*/s/ Sam Baxter*

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